A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications

Reid R. Harrison, *Member, IEEE,* and Cameron Charles, *Student Member, IEEE*

***Abstract*—There is a need among scientists and clinicians for low-noise low-power biosignal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range while rejecting large dc offsets generated at the electrode–tissue interface. The advent of fully implantable multielectrode arrays has created the need for fully integrated micropower amplifiers. We designed and tested a novel bioamplifier that uses a MOS-bipolar pseudoresistor element to amplify low-frequency signals down to the millihertz range while rejecting large dc offsets. We derive the theoretical noise–power tradeoff limit—the noise efficiency factor—for this amplifier and demonstrate that our VLSI implementation approaches this limit by selectively operating MOS transistors in either weak or strong inversion. The resulting amplifier, built in a standard 1.5-μm CMOS process, passes signals from 0.025 Hz to 7.2 kHz with an input-referred noise of 2.2 μVrms and a power dissipation of 80 μW while consuming 0.16 mm^2 of chip area. Our design technique was also used to develop an electroencephalogram amplifier having a bandwidth of 30 Hz and a power dissipation of 0.9 μW while maintaining a similar noise–power tradeoff.**

***Index Terms*—Analog integrated circuits, biosignal amplifier, low noise, low-power circuit design, neural amplifier, noise efficiency factor, subthreshold circuit design, weak inversion.**

I. Introduction

THERE IS a great demand for technologies that enable neuroscientists and clinicians to observe the simultaneous activity of large numbers of neurons in the brain. Multielectrode neural recordings are becoming standard practice in basic neuroscience research, and knowledge gained from these studies is beginning to enable clinical and neuroprosthetic applications. Recent advances in MEMS technology have produced small (less than 4 mm in any dimension) arrays of microelectrodes containing as many as 100 recording sites [1], [2]. Next-generation neural recording systems must be capable of observing 100–1000 neurons simultaneously, in a fully implanted unit.

While integrated electronics have been developed for small-scale amplification of the weak bioelectrical signals [3]–[15], existing circuits typically have unacceptable noise levels or consume too much power to be fully implanted in large quantities. Implantable bioamplifiers must dissipate little power so that surrounding tissues are not damaged by heating. A heat flux of only 80 mW/cm^2 can cause necrosis in muscle tissue [16], so for small chronic implants, power dissipation should not exceed a few hundred milliwatts. For a 1000-electrode system, this results in a maximum power dissipation much less than 1 mW per amplifier, and this does not include power required by other components in the implanted system such as telemetry.

Manuscript received September 27, 2002; revised March 3, 2002. This work was supported by National Science Foundation CAREER Award ECS-0134336 and by the National Science Foundation under STTR Grant PID-2201089 through Bionic Technologies, LLC, Salt Lake City, UT.

The authors are with the Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112 USA (e-mail: harrison@ece.utah.edu).

Digital Object Identifier 10.1109/JSSC.2003.811979

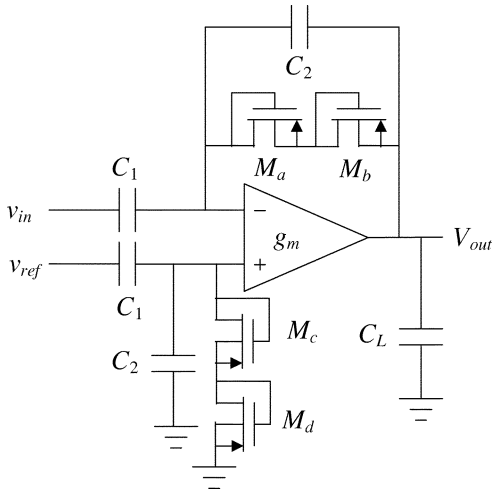

Fig. 1. Schematic of neural amplifier.

Due to electrochemical effects at the electrode–tissue interface, dc offsets of 1–2 V are common across differential recording electrodes [17]. Typical neural action potientials, or spikes, have amplitudes up to 500 μV when recorded extracellularly, with energy in the 100-Hz–7-kHz band [6], while low-frequency local field potentials (LFPs) have amplitudes as high as 5 mV and may contain signal energy below 1 Hz [8]. Some existing VLSI bioamplifier designs use off-chip capacitors in the nanofarad range to obtain a low-frequency cutoff that passes LFP signals while rejecting large dc offsets [7], [8], [10], [11]. This approach is not feasible for large numbers of implanted electrodes. If we restrict ourselves to a 15 mm $\times$ 15 mm die for a 1000-channel system, then each amplifier must consume less than 0.225 mm^2 of silicon area.

This paper reports on the design and testing of a fully integrated amplifier suitable for recording biological signals from the millihertz range to 7 kHz. We show that this amplifier rejects dc offsets at the input and offers the best power–noise tradeoff of any biosignal amplifier reported.

II. Neural Amplifier Design

Fig. 1 shows the schematic of our bioamplifier design. This circuit was first described in [18]. The midband gain A_M is set by C_1/C_2, and for the case where $C_1, C_{\rm L} \gg C_2$, the bandwidth

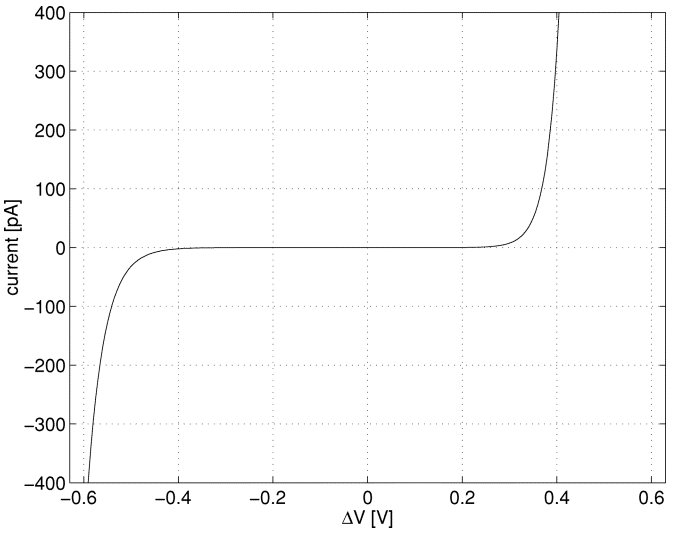

Fig. 2. Measured current–voltage relationship of MOS-bipolar element (M_a–M_d in Fig. 1) [19].

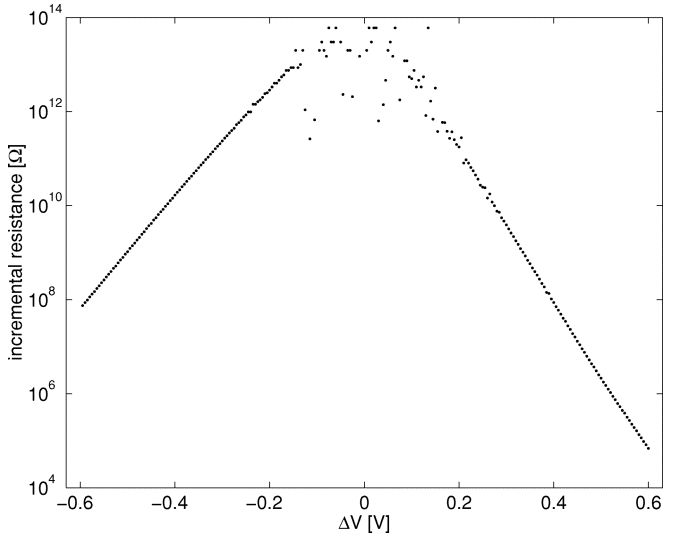

Fig. 3. Incremental resistance of single MOS-bipolar element. For low voltages, the incremental resistance exceeds $10^{12}\ \Omega$.

is approximately $g_m/(A_M C_{\rm L})$, where g_m is the transconductance of the operational transconductance amplifier (OTA).

A. MOS-Bipolar Pseudoresistor Elements

Transistors M_a–M_d are MOS-bipolar devices acting as pseudoresistors. With negative $V_{\rm GS}$, each device functions as diode-connected pMOS transistor. With positive $V_{\rm GS}$, the parasitic source–well–drain p-n-p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT [19] (see Fig. 2). Each transistor was sized 4 μm $\times$ 4 μm. For small voltages across this device, its incremental resistance $r_{\rm inc}$ is extremely high (see Fig. 3). For $|\Delta V| < 0.2$ V, we measured $dV/dI > 10^{11}\ \Omega$. It was difficult to measure dV/dI accurately in this region due to the low current, which was near the limit of our measurement capabilities.

We use two MOS-bipolar devices in series to reduce distortion for large output signals. The low-frequency cutoff $\omega_{\rm L}$ of the ac-coupled amplifier is given by $1/(2r_{\rm inc}C_2)$. Despite the long

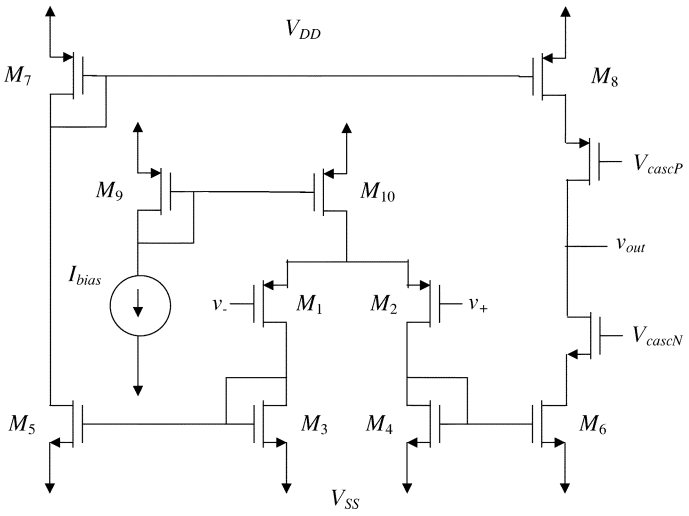

Fig. 4. Schematic of OTA used in neural amplifier.

time constant, a large change in the input causes a large voltage across the MOS-bipolar elements, reducing their incremental resistance and giving a fast settling time. Recent bioamplifier designs have used transistors biased in the subthreshold region to approximate large-valued resistors [13], [14]. This technique yields similar results but requires additional biasing circuitry. Another design uses diode-connected nMOS transistors as pseudoresistors to achieve an equivalent resistance of greater than $10^{10}\,\Omega$, though it is not stated whether a body–source connection is used to create a diode-connected bipolar transistor [15].

B. Low-Noise Low-Power OTA Design

Fig. 4 shows a schematic of the current-mirror OTA used in the bioamplifier. The bias current and cascode bias voltages were generated by standard circuits [20], and the power consumption of these biasing circuits was not included in our power measurements since an arbitrary number of OTAs can share the generated voltages. Although the circuit topology is a standard design suitable for driving capacitive loads, the sizing of the transistors is critical for achieving low noise at low current levels. The bias current $I_{\rm bias}$ is set to 8 μA, giving devices M_1–M_8 drain currents of 4 μA. At this current level, each transistor may operate in weak, moderate, or strong inversion depending on its W/L ratio. For each device, we calculate the moderate inversion characteristic current I_S [21], given by

$$I_S = \frac{2\mu C_{\rm ox} U_{\rm T}^2}{\kappa} \cdot \frac{W}{\rm L} \tag{1}$$

where $U_{\rm T}$ is the thermal voltage kT/q, and κ is the subthreshold gate coupling coefficient. Note that κ has a typical value of 0.7 and is equivalent to $1/n$, where n denotes the reciprocal of the change in surface potential ψ_{sa} for a change in gate-to-body voltage $V_{\rm GB}$ [21], [22].

The inversion coefficient (IC) for each transistor may then be calculated as the ratio of drain current to the moderate inversion characteristic current, as follows:

$$\text{IC} = I_D/I_S. \tag{2}$$

A device having IC > 10 operates in the strong inversion region and has a transconductance proportional to the square root

TABLE I
OPERATING POINT OF OTA TRANSISTORS FOR NEURAL AMPLIFIER

Devices	W/L (μm)	I_D (μA)	Inversion Coefficient	g_m/I_D (V^{-1})	$V_{EFF} = V_{GS} - V_t$ (V)
M_1, M_2	800.0/4.0	4.0	0.43	20.6	-0.076
M_3, M_4, M_5, M_6	12.0/44.8	4.0	110	2.5	+0.770
M_7, M_8	6.4/12.8	4.0	171	2.0	+0.960
M_9, M_{10}	20.0/20.0	8.0	171	2.0	+0.960
M_{cascN}	12.0/3.2	4.0	7.8	8.1	+0.200
M_{cascP}	6.4/3.2	4.0	43	3.9	+0.481

of drain current. A device having IC < 0.1 operates in the weak inversion (subthreshold) region and has a transconductance proportional to drain current [22], [23]. For devices operating in moderate inversion ($10 > \text{IC} > 0.1$), both strong and weak inversion expressions overestimate transconductance. For low-power circuit design, we use the EKV model, which is valid in all regions of inversion [24]. We estimate g_m by

$$g_m \approx \frac{\kappa I_D}{U_{\text{T}}} \cdot \frac{2}{1+\sqrt{1+4 \cdot \text{IC}}}. \tag{3}$$

Table I shows the dimensions and operating conditions of each transistor in the circuit. The input devices M_1 and M_2 are drawn with identical sizes, and we denote their transconductance as g_{m1} and their width-to-length ratio as $(W/L)_1$. Similarly, transistors M_3–M_6 are the same size $(W/L)_3$ and have transconductance g_{m3}. The pMOS current mirror transistors M_7 and M_8 have size $(W/L)_7$ and transconductance g_{m7}.

Analysis of this circuit reveals the input-referred thermal noise power to be

$$\overline{v_{ni,\,\text{thermal}}^2} = \left[\frac{16kT}{3g_{m1}}\left(1+2\,\frac{g_{m3}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right)\right]\Delta f. \tag{4}$$

If we size our devices such that $g_{m3}, g_{m7} \ll g_{m1}$, we can minimize the noise contributions of devices M_3–M_8. This can be accomplished by making $(W/L)_3, (W/L)_7 \ll (W/L)_1$, thus, pushing devices M_3–M_8 into strong inversion where their relative transconductance g_m/I_D decreases as $1/\sqrt{I_D}$. As shown in Table I, by operating M_1 and M_2 in the subthreshold regime, we achieve a high g_m/I_D ratio so that g_{m1} is much greater than g_{m3} and g_{m7}. We are operating near the maximum achievable g_m/I_D ratio of κ/U_{T} (approximately 27 V^{-1}), which is reached in deep weak inversion.

In practice, we cannot decrease g_{m3} and g_{m7} arbitrarily without danger of instability. If the total capacitance seen by the gate of M_3 (or M_4) is denoted as C_3, then the OTA has two poles at $\omega_p = g_{m3}/C_3$. Similarly, there is a pole at g_{m7}/C_7 caused by the pMOS mirror. To ensure stability, these pole frequencies must be several times greater than the dominant pole, g_{m1}/C_{L}. This criterion becomes easier to satisfy as C_{L} is made larger, so it becomes necessary to consider area limitations and bandwidth requirements. In our design, we decreased $(W/L)_3$ and $(W/L)_7$ as much as possible, trading off phase margin for lower input-referred noise. We designed our amplifier to have a phase margin of 52°. Transistors M_3–M_8 are narrow devices that require relatively large gate overdrive voltages, as shown in the last column of Table I, so output signal swing considerations or finite power-supply voltages may also limit the designer's ability to decrease g_m.

Flicker noise, or $1/f$ noise, is a major concern for a low-noise low-frequency circuit. We minimize the effects of flicker noise by using pMOS transistors as input devices and by using devices with large gate areas. Flicker noise in pMOS transistors is typically one to two orders of magnitude lower than flicker noise in nMOS transistors as long as $|V_{\text{GS}}|$ does not greatly exceed the threshold voltage [21], [25] and flicker noise is inversely proportional to gate area. All transistors should be made as large as possible to minimize $1/f$ noise. However, as devices M_3–M_8 are made larger, C_3 and C_7 increase, leading once again to a reduced phase margin. As M_1 and M_2 are made larger, the OTA input capacitance C_{in} increases. The input-referred noise of the bioamplifier can be related to the OTA input-referred noise by

$$\overline{v_{ni,\,\text{amp}}^2} = \left(\frac{C_1+C_2+C_{in}}{C_1}\right)^2 \cdot \overline{v_{ni}^2} \tag{5}$$

where C_1 and C_2 are the feedback network capacitors shown in Fig. 1. Since C_{in} contributes to a capacitive divider that attenuates the input signal, any increase in C_{in} increases the input-referred noise of the overall circuit [26]. An optimum gate area for M_1 and M_2 can be found to minimize $1/f$ noise.

Lateral p-n-p transistors can be built in standard CMOS technology for low-frequency applications, and exhibit lower $1/f$ noise than MOS transistors [27]. We did not use p-n-p devices for the input transistors M_1 and M_2 because the base current would have to flow through the MOS-bipolar devices. This dc current would bias the pseudoresistors toward an operating point with lower incremental resistance and raise the low-frequency cutoff. The inherently high g_m/I_C ratio of bipolar transistors makes them unsuitable for devices M_3–M_8 in our OTA design, as shown in (4).

C. Noise Efficiency Factor

Since we are interested in minimizing noise within a strict power budget, we must consider the tradeoff between power and noise. The noise efficiency factor (NEF) introduced in [7] quantifies this tradeoff:

$$\text{NEF} = V_{ni,\,\text{rms}}\sqrt{\frac{2I_{\text{tot}}}{\pi \cdot U_{\text{T}} \cdot 4kT \cdot \text{BW}}} \tag{6}$$

where $V_{ni,\,\text{rms}}$ is the input-referred rms noise voltage, I_{tot} is the total amplifier supply current, and BW is the amplifier bandwidth in hertz. An amplifier using a single bipolar transistor (with no $1/f$ noise) has an NEF of one; all practical circuits have higher values.

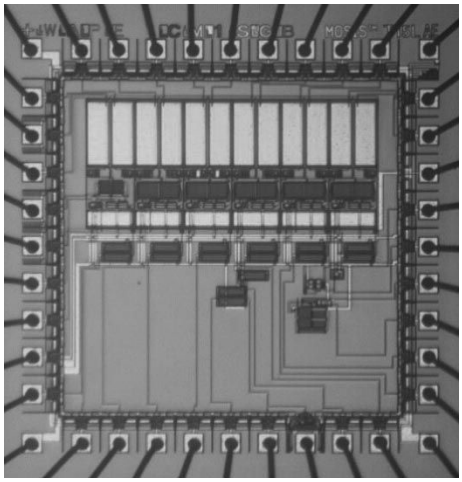

Fig. 5. Microphotograph of 2.2 × 2.2 mm chip containing six neural amplifiers.

Substituting the expression for amplifier thermal noise (4) integrated across the bandwidth BW into (6) and assuming g_{m3}, $g_{m7} \ll g_{m1}$, we find

$$\text{NEF} = \sqrt{\frac{4I_{\text{tot}}}{3U_{\text{T}}g_{m1}}} = \sqrt{\frac{16}{3U_{\text{T}}}\left(\frac{I_{D1}}{g_{m1}}\right)} \tag{7}$$

where I_{D1} is the drain current through M_1, which is 1/4 of the total amplifier supply current. From this expression, it is clear that if we wish to minimize the NEF, we must maximize the relative transconductance g_m/I_D of the input devices M_1 and M_2. In weak inversion, g_m/I_D reaches its maximum value of κ/U_{T}, so we make $(W/L)_1$ very large to approach subthreshold operation with microamp current levels. Using a more accurate model for thermal noise valid in weak inversion [21] yields

$$\text{NEF} = \sqrt{\frac{4}{\kappa U_{\text{T}}}\left(\frac{I_{D1}}{g_{m1}}\right)}. \tag{8}$$

In weak inversion, the expression for NEF reduces to

$$\text{NEF} = \sqrt{\frac{4}{\kappa^2}} \cong 2.9 \tag{9}$$

assuming a typical value of $\kappa = 0.7$. This is the theoretical NEF limit for an amplifier with this circuit topology constructed from MOS transistors, assuming current mirror ratios of unity. In practice, the NEF will be limited by stability constraints on g_{m3} and g_{m7}, as discussed earlier, and by $1/f$ noise.

III. Experimental Results

We fabricated the amplifier in the AMI ABN 1.5-μm two-metal two-poly CMOS process. We designed the amplifier for a gain of 100, setting C_1 to 20 pF and C_2 to 200 fF. Both C_1 and C_2 were built as poly–poly capacitors for maximum linearity. The bandwidth-limiting load capacitor C_{L} was built as an nMOS capacitor with a value of 17 pF. One amplifier circuit uses 0.16 mm^2 of silicon area, and 67% of this area is taken up by capacitors. A die photograph of a 2.2 mm × 2.2 mm chip containing six amplifier variants is shown in Fig. 5.

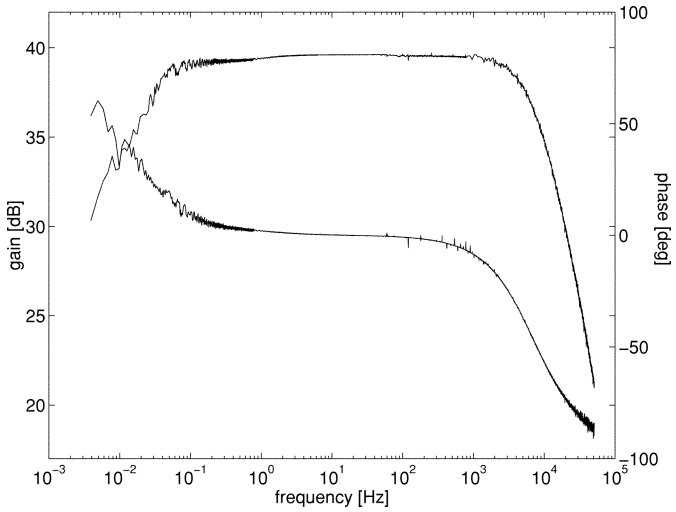

Fig. 6. Measured transfer function of amplifier. Midband gain is 39.5 dB, and single-pole rolloff occurs at 7.2 kHz. Low-frequency rolloff occurs at 0.025 Hz.

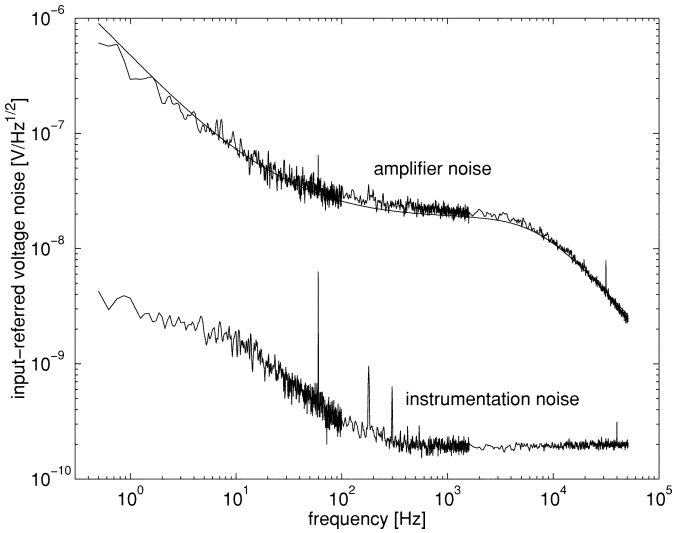

Fig. 7. Measured and simulated (smooth curve) amplifier input-referred voltage noise spectrum. Integration under this curve yields an rms noise voltage of 2.2 μVrms.

A. Testbench Results

Fig. 6 shows the measured amplifier transfer function from 0.004 Hz to 50 kHz. The midband gain is 39.5 dB, which is slightly lower than our design specification of 40 dB. This discrepancy is likely caused by fringing fields on the small C_2 capacitors, yielding a larger capacitance than drawn. The low-frequency cutoff f_{L} is approximately 0.025 Hz. This corresponds to a MOS-bipolar element incremental resistance $r_{\text{inc}} > 10^{13}\,\Omega$.

Fig. 7 shows the measured input-referred voltage noise spectrum. The thermal noise level is 21 nV/$\sqrt{\text{Hz}}$ and the $1/f$ noise corner occurs at 100 Hz. Integration under this curve from 0.5 Hz to 50 kHz yields an rms noise voltage of 2.2 μVrms. This noise measurement was confirmed by recording the output noise waveform and dividing by the gain to generate an input-referred noise waveform whose rms value is 2.2 μVrms (see Fig. 8). Surprisingly, $1/f$ noise is not the dominant noise source in the circuit. If $1/f$ noise were eliminated entirely,

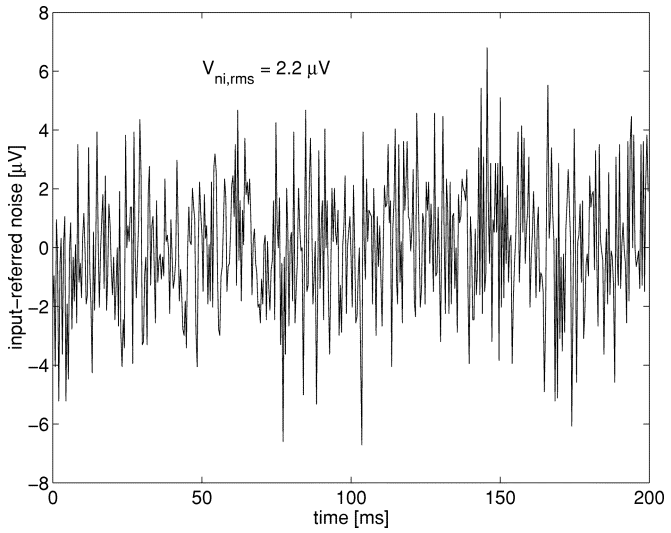

Fig. 8. Measured amplifier input-referred noise (i.e., output noise divided by amplifier gain). The rms value is 2.2 μV, which agrees with the noise spectrum measurements in Fig. 7.

the circuit would have an input-referred noise of 2.1 μVrms. The low noise corner is due partially to the use of pMOS input devices with large gate areas, as discussed in Section II, but also to the relatively high thermal noise level of 21 nV/$\sqrt{\text{Hz}}$. This noise level is acceptable because of the low bandwidth of the circuit and the requirement that the input-referred noise only be lower than the typical extracellular neural background noise of 5–10 μVrms over this bandwidth [28].

Table II summarizes these and other measurements along with simulation results. We achieved noise simulations that closely matched experimental data by using SPICE BSIM3v3 Level 49 transistor models with $1/f$ noise coefficients of KF $= 6 \times 10^{-27}$ (pMOS), KF $= 3 \times 10^{-25}$ (nMOS), and AF $= 1$ (pMOS and nMOS). The smooth curve in Fig. 7 shows the simulated noise spectrum. The measured NEF of our amplifier is 4.0, which is near the theoretical limit of 2.9 calculated in (9).

Distortion stays below 1% total harmonic distortion (THD) for inputs less than 16.7 mV peak-to-peak (larger than typical extracellular neural signals). If we calculate dynamic range assuming a distortion limit of 1% (a conservative definition), our dynamic range is 69 dB. We also fabricated an alternate circuit using only single MOS-bipolar pseudoresistor elements instead of two elements in series (see Fig. 2). This amplifier exhibited 1% THD for a 12.0-mV peak-to-peak input, resulting in a lower dynamic range of 66 dB.

The common-mode rejection ratio (CMRR) and the power-supply rejection ratio (PSRR) were measured and both exceeded 80 dB. Crosstalk was measured between amplifiers adjacent on the chip, and was -64 dB or less. The input-referred offset voltage was measured for four amplifiers and varied between 180 and 550 μV.

Fig. 9 shows the power–noise performance of our amplifier compared with estimated NEF values from previously published bioamplifiers [3]–[11]. (Only simulation results were presented in [12], and although circuits were built and tested in [13]–[15], no noise measurements were reported.) The amplifier presented here exhibits a significantly better NEF than existing designs.

TABLE II
SIMULATED AND EXPERIMENTAL CHARACTERISTICS OF NEURAL AMPLIFIER

Parameter	Simulation	Measured
Supply voltage	±2.5 V	±2.5 V
Supply current	16 μA	16 μA
Gain	40 dB	39.5 dB
Bandwidth	7.5 kHz	7.2 kHz
Low-frequency cutoff	0.130 Hz	0.025 Hz
Input-referred noise	2.1 μVrms	2.2 μVrms
Noise efficiency factor	3.8	4.0
THD (16.7 mVpp input)	not simulated	1.0%
Dynamic range (1% THD)	not simulated	69 dB
CMRR (10 Hz – 5 kHz)	≥ 42 dB	≥ 83 dB
PSRR (10 Hz – 5 kHz)	≥ 42 dB	≥ 85 dB
Crosstalk (f = 1 kHz)	not simulated	-64 dB
Area (in 1.5-μm CMOS)	n/a	0.16 mm^2

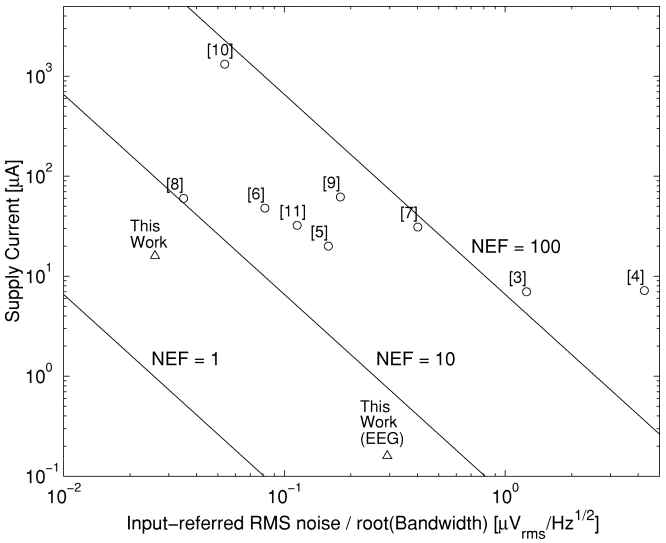

Fig. 9. Supply current versus normalized noise for amplifiers in [3]–[11] (circles) and the amplifiers described in this paper (triangles). Lines indicate constant NEF contours.

B. Biological Test Results

We used the bioamplifier described above as a preamplifier in a simple neural recording experiment to verify operation of the circuit when connected to a neural electrode. We recorded spontaneous neural activity in rat olfactory cortex using a platinum-tipped extracellular microelectrode (Bionic Technologies, Salt Lake City, UT). Due to the unshielded wires connecting the electrode array to the amplifier circuit, we observed strong interfering signals at 60 Hz and approximately 50 kHz. We used two single-pole filters after the bioamplifier circuit to attenuate frequencies below 300 Hz and above 30 kHz. Fig. 10 shows an action potential recorded from this system referred to the amplifier input. The peak-to-peak signal and noise levels recorded with our low-power system match those obtained using a commercially available rack-mount biosignal amplifier system (Bionic Technologies).

TABLE III
OPERATING POINT OF OTA TRANSISTORS FOR EEG AMPLIFIER

Devices	W/L (μm)	I_D (μA)	Inversion Coefficient	g_m/I_D (V^{-1})	$V_{EFF} = V_{GS} - V_t$ (V)
M_1, M_2	800.0/4.0	0.032	0.0034	27.1	-0.206
M_3, M_4, M_5, M_6	6.4/470.0	0.032	17	5.8	+0.304
M_7, M_8	6.4/104.0	0.032	11	7.0	+0.242
M_9, M_{10}	20.0/20.0	0.064	1.4	15.4	+0.059
M_{cascN}	12.0/3.2	0.032	0.063	25.7	-0.092
M_{cascP}	6.4/3.2	0.032	0.34	21.5	-0.017

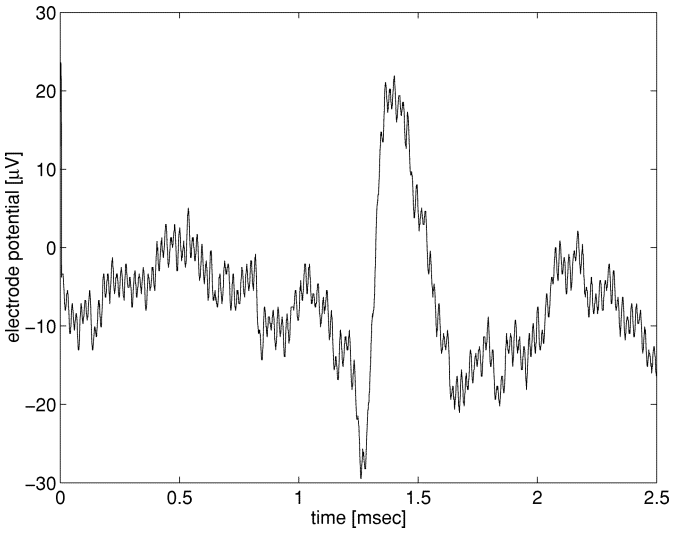

Fig. 10. Action potential from rat olfactory cortex recorded extracellularly using fully integrated CMOS amplifier. Waveform is referred to the amplifier input.

IV. ELECTROENCEPHALOGRAM (EEG) AMPLIFIER DESIGN

As a further demonstration of our amplifier design technique, we redesigned the neural signal amplifier demonstrated above for low-frequency biosignal applications such as EEGs or brain-surface electrodes. Electrical recordings from the scalp or brain surface show signal energy primarily below 30 Hz since individual neural action potentials cannot be observed from this distance. We modified our previous amplifier design to achieve a bandwidth extending from below 1 Hz to 30 Hz while maintaining a low NEF and a gain of 40 dB.

In order to lower the amplifier bandwidth, we increased the load capacitance C_{L} from 17 to 50 pF. Layout area considerations prevented us from increasing C_{L} beyond this value. The low value of g_m required to produce a 30-Hz bandwidth dictated a bias current of 32 nA for the differential pair transistors. Table III lists the dimensions and operating point of each transistor in the OTA. Transistors M_3–M_8 were drawn extremely long and narrow so that strong inversion operation could be achieved in the current mirrors at nanoampere current levels.

This amplifier was fabricated in the same 1.5-μm CMOS process described in Section III. Table IV summarizes the simulated and measured results for this amplifier. The EEG amplifier exhibited a bandwidth of 30 Hz at a power dissipation of 0.9 μW and an input-referred rms noise voltage of 1.6 μVrms. Despite low-frequency operation where $1/f$ noise power is high, an NEF of 4.8 was achieved by using high-g_m/I_D operation for the input differential pair and low-g_m/I_D operation for the current mirrors. Fig. 11 shows the measured transfer function of this amplifier. Fig. 12 shows the measured input-referred voltage noise spectrum. The $1/f$ noise corner frequency occurred at 2.3 Hz due to the relatively high thermal noise levels.

The chip area consumed by the EEG amplifier (0.22 mm^2) was slightly greater than the neural amplifier since a larger value of C_{L} was used. The measured dynamic range of 69 dB matches the performance of the neural amplifier, and the CMRR and PSRR exceeded 80 dB. The input-referred offset voltage was measured for four amplifiers and varied between 110 and 380 μV.

TABLE IV
SIMULATED AND EXPERIMENTAL CHARACTERISTICS OF EEG AMPLIFIER

Parameter	Simulation	Measured
Supply voltage	±2.5 V	±2.5 V
Supply current	128 nA	180 nA
Gain	40 dB	39.8 dB
Bandwidth	30 Hz	30 Hz
Low-frequency cutoff	2.2 Hz	0.014 Hz
Input-referred noise	2.4 μVrms	1.6 μVrms
Noise efficiency factor	6.0	4.8
THD (12.4 mVpp input)	not simulated	1.0%
Dynamic range (1% THD)	not simulated	69 dB
CMRR (1 Hz – 100 Hz)	≥ 88 dB	≥ 86 dB
PSRR (1 Hz – 100 Hz)	≥ 80 dB	≥ 80 dB
Area (in 1.5-μm CMOS)	n/a	0.22 mm^2

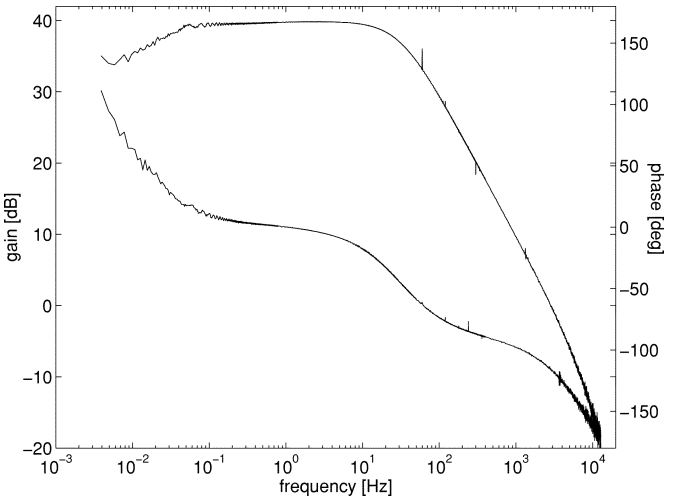

Fig. 11. Measured transfer function of EEG amplifier. Midband gain is 39.8 dB, and single-pole rolloff occurs at 30 Hz. Low-frequency rolloff occurs at 0.014 Hz.

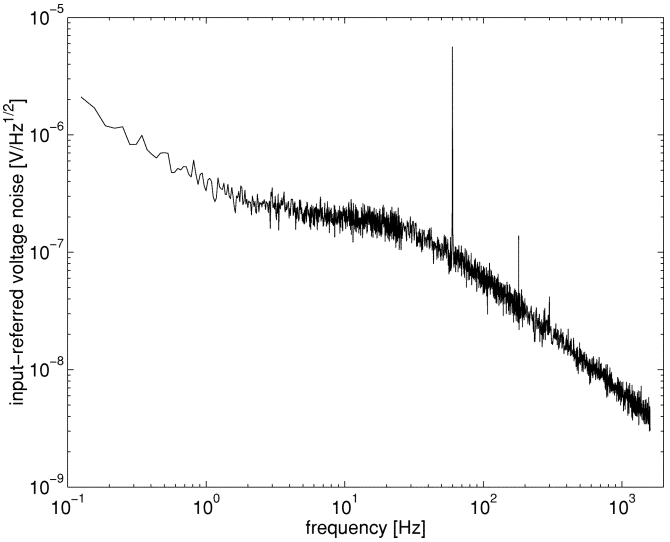

Fig. 12. Measured EEG amplifier input-referred voltage noise spectrum. Integration under this curve yields an rms noise voltage of 1.6 μVrms.

V. Conclusion

An 80-μW fully integrated CMOS biosignal amplifier with an input-referred noise of 2.2 μVrms over a 7.2-kHz bandwidth has been demonstrated. The amplifier rejects dc offsets commonly encountered in microelectrode recording applications, but passes low-frequency signals in the millihertz range while using no off-chip components. By taking advantage of the high g_m/I_D ratio of devices operating in subthreshold, we were able to achieve the best power–noise tradeoff reported among biosignal amplifiers. A 1000-channel amplifier would consume only 80 mW and fit on a 13-mm $\times$ 13-mm silicon die in a 1.5-μm process (pads excluded), allowing for large-scale implantable neural recording systems. We applied the same design approach to an EEG amplifier application and achieved a similar NEF at a much lower bandwidth and power dissipation.

A complete multichannel recording system will also require an analog multiplexer (MUX) and analog-to-digital converter (ADC) with milliwatt power dissipation. For systems with large numbers of channels, the hardware required for serialization and digitizing of neural signal data may become the dominant source of power consumption. Low-power MUX and ADC design will be essential for fully implanted neural recording systems.

The low-frequency ac coupling provided by the MOS-bipolar element may also have applications in the baseband circuitry of direct-conversion RF receivers. The direct-conversion architecture is attractive for low-power fully integrated receivers, but device mismatch and substrate coupling lead to large dc offsets that may be much larger than the received signal [29]. The amplifier presented in this article achieves ultralow-frequency ac response while completely rejecting large dc offsets, and may be of use in integrated direct-conversion systems.

Acknowledgment

The authors would like to thank M. Lehmkuhle for assistance with the neural recording experiment, and R. Normann and S. Guillory for valuable discussions and comments.

References

[1] A. C. Hoogerwerf and K. D. Wise, "A three-dimensional microelectrode array for chronic neural recording," *IEEE Trans. Biomed. Eng.*, vol. 41, pp. 1136–1146, Dec. 1994.

[2] C. T. Nordhausen, E. M. Maynard, and R. A. Normann, "Single unit recording capabilities of a 100-microelectrode array," *Brain Res.*, vol. 726, pp. 129–140, 1996.

[3] M. Degrauwe, E. Vittoz, and I. Verbauwhede, "A micropower CMOS instrumentation amplifier," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 805–807, June 1985.

[4] P. M. van Peteghem, I. Verbauwhede, and W. M. C. Sansen, "Micropower high-performance SC building block for integrated low-level signal processing," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 837–844, Aug. 1985.

[5] M. G. Dorman, M. A. Prisbe, and J. D. Meindl, "A monolithic signal processor for a neurophysiological telemetry system," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1185–1193, Dec. 1985.

[6] K. Najafi and K. D. Wise, "An implantable multielectrode array with on-chip signal processing," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 1035–1044, Dec. 1986.

[7] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1163–1168, Dec. 1987.

[8] A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events," *Med. Biol. Eng. Comput.*, vol. 29, pp. 1035–1044, 1986.

[9] J. Ji and K. D. Wise, "An implantable CMOS circuit interface for multiplexed microelectrode recording arrays," *IEEE J. Solid-State Circuits*, vol. 27, pp. 433–443, Mar. 1992.

[10] J. J. Pancrazio, P. P. Bey, Jr., A. Loloee, S. Manne, H. C. Chao, L. L. Howard, W. M. Gosney, D. A. Borkholder, G. T. A. Kovacs, P. Manos, D. S. Cuttino, and D. A. Stenger, "Description and demonstration of a CMOS amplifier-based-system with measurement and stimulation capability for bioelectrical signal transduction," *Biosensors Bioelectron.*, vol. 13, pp. 971–979, 1998.

[11] R. Martins, S. Selberherr, and F. A. Vaz, "A CMOS IC for portable EEG acquisition systems," *IEEE Trans. Instrum. Meas.*, vol. 47, pp. 1191–1196, 1998.

[12] M. Dagtekin, W. Liu, and R. Bashirullah, "A multichannel chopper modulated neural recording system," in *Proc. IEEE EMBS Int. Conf.*, 2001, pp. 757–760.

[13] A. P. Chandran, K. Najafi, and K. D. Wise, "A new DC baseline stabilization scheme for neural recording microprobes," in *Proc. IEEE BMES/EMBS Conf.*, 1999, p. 386.

[14] P. Mohseni and K. Najafi, "A low power fully integrated bandpass operational amplifier for biomedical neural recording applications," in *Proc. IEEE EMBS/BMES Conf.*, 2002, pp. 2111–2112.

[15] R. H. Olsson, III, M. N. Gulari, and K. D. Wise, "Silicon neural recording arrays with on-chip electronics for *in-vivo* data acquisition," in *Proc. IEEE-EMBS Special Topic Conf. Microtechnol. Medicine Biol.*, 2002, pp. 237–240.

[16] T. M. Seese, H. Harasaki, G. M. Saidel, and C. R. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating," *Lab. Invest.*, vol. 78, no. 12, pp. 1553–1562, 1998.

[17] C. D. Ferris, *Introduction to Bioinstrumentation*. Clifton, NJ: Humana, 1978.

[18] R. R. Harrison, "A low-power, low-noise CMOS amplifier for neural recording applications," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, 2002, pp. 197–200.

[19] T. Delbrück and C. A. Mead, "Analog VLSI adaptive, logarithmic wide-dynamic-range photoreceptor," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 4, 1994, pp. 339–342.

[20] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.

[21] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. Boston, MA: McGraw-Hill, 1998.
[22] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley, 1989.
[23] E. A. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. 12, pp. 224–231, June 1977.
[24] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrat. Circuits Signal Process.*, vol. 8, pp. 83–114, 1995.
[25] C. Jakobson, I. Bloom, and Y. Nemirovsky, "$1/f$ noise in CMOS transistors for analog applications from subthreshold to saturation," *Solid-State Electron.*, vol. 42, no. 10, pp. 1807–1817, 1998.
[26] M. Steyaert, Z. Y. Chang, and W. Sansen, "Low-noise monolithic amplifier design: Bipolar versus CMOS," *Analog Integrat. Circuits Signal Process.*, vol. 1, pp. 9–19, 1991.
[27] E. A. Vittoz, "MOS transistors operated in the lateral bipolar mode and their application to CMOS technology," *IEEE J. Solid-State Circuits*, vol. 18, pp. 273–279, June 1983.
[28] K. S. Guillory and R. A. Normann, "A 100-channel system for real time detection and storage of extracellular spike waveforms," *J. Neurosci. Methods*, vol. 91, pp. 21–29, 1999.
[29] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

Reid R. Harrison (S'98–M'00) received the B.S. degree in electrical engineering from the University of Florida, Gainesville, in 1994 and the Ph.D. degree from the California Institute of Technology, Pasadena, in 2000.

He is currently an Assistant Professor with the Electrical and Computer Engineering Department, University of Utah, Salt Lake City, where he holds an adjunct appointment with the Bioengineering Department. After working at the Jet Propulsion Laboratory and at Los Alamos National Laboratory for a brief time, he joined the Computation and Neural Systems program of the California Institute of Technology. His research interests include low-power analog and mixed-signal CMOS circuit design, biomedical electronics for neural interfaces, and hardware for biologically inspired vision systems.

Dr. Harrison recently organized the 2001 IEEE SSCTC Workshop on Low-Power Circuits, Arlington, VA. He received the National Science Foundation Career Award in 2002.

Cameron Charles (S'00) was born in Toronto, ON, Canada, in 1977. He received the B.S. degree in computer engineering from the University of Waterloo, Canada, in 2001. He is currently working toward the M.S. degree in electrical engineering at the University of Utah, Salt Lake City. His thesis involves the design of fully differential low-noise amplifiers for biomedical recording applications.