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Technology development for 4k × 4k, back-illuminated, fully depleted scientific CCD imagers

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***Abstract*—We have developed scientific charge-coupled devices (CCDs) that are fabricated on high-resistivity, n-type silicon substrates, and have demonstrated fully depleted operation for substrate thicknesses of 200–675 μm with formats as large as 2048 × 4096 (15 μm pixels) and 3512 × 3512 (10.5 μm pixels). The main application area for these devices is space and ground-based astronomy, and the CCDs are operated at cryogenic temperatures with slow-scan readout for good performance in terms of dark current and noise. In this work we describe the technology development efforts needed to realize a 4k × 4k (15 μm pixel) CCD with a die area of (64 mm)^2. In particular, we describe improved gettering techniques for low dark current and high charge transfer efficiency that have been developed in order to improve fabrication yields for these very large format CCDs.**

I. Introduction

FOCAL plane array cameras consisting of multiple, large format charge-coupled devices (CCDs) are presently in use at astronomical observatories. Examples include the Canada-French-Hawaii Telescope Megacam consisting of 40, 2048 × 4162 (13.5 μm pixel) CCDs [1], and the Multiple Mirror Telescope Observatory MegaCam that contains 36, 2048 × 4162 (13.5 μm) pixel CCDs [2].

Larger focal plane arrays are planned or in progress, and these include the Subaru Hyper-Suprime camera with approximately 200 2k × 4k CCDs manufactured at Hamamatsu [3], the Dark Energy Survey (DES) camera with approximately 70 2k × 4k devices that are fabricated at DALSA Semiconductor and Lawrence Berkeley National Laboratory (LBNL) [4], and the Pan-STARRS cameras consisting of 4, 1.4 Gpixel cameras each containing 60 orthogonal transfer CCDs produced at Lincoln Laboratory [5]. One of the 1.4 Gpixel cameras was installed in August 2007 [6]. In addition, the proposed SuperNova Acceleration Probe (SNAP), a space-based mission to study dark energy, will require approximately 40 3.5k^2, 10.5 μm pixel CCDs [7]. In each of these 4 projects the imagers are fully depleted CCDs fabricated on high-resistivity silicon substrates, a concept that was originally developed and demonstrated in our laboratory [8], [9].

In order to produce the required number of CCDs at a reasonable cost it is necessary to develop high yielding fabrication processes. In addition, the use of high-resistivity substrates requires extra care in processing in order to not contaminate the silicon with metallic impurities that could increase the dark current, alter the resistivity, and degrade the charge transfer efficiency (CTE).

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In this work we describe the development of large-format CCDs in partnership with a commercial CCD foundry. Techniques for the gettering of metallic impurities are described, and results from CCDs fabricated with the improved processing techniques are presented.

II. CCD development at Lawrence Berkeley National Laboratory

The CCD fabrication technology in use at LBNL has been described earlier [10], [11]. The majority of the fabrication steps are performed at a commercial foundry (DALSA Semiconductor), with the steps needed to produce back-illuminated devices done at LBNL. Specifically the standard thickness, about 650–675 μm, high-resistivity, n-type substrates are procured from Siltronic AG by DALSA Semiconductor. Standard CCD processing steps are done at DALSA Semiconductor on the normal thickness wafers. A small number of wafers in the 24-wafer lot are completely finished at DALSA Semiconductor as quality control monitors, with the remaining wafers sent to LBNL after 8 of the 11 masking steps are completed at DALSA Semiconductor.

The partially-processed wafers are thinned to the desired thickness, which is typically 250 μm for most applications. The target for SNAP CCDs is 200 μm in order to meet the spatial resolution requirements for that project. Once the wafers are thinned the remainder of the processing is done at LBNL on the thinned wafers using standard semiconductor processing equipment. Processing steps at LBNL include deposition of a thin backside ohmic contact layer, lithography and etching steps, and deposition of anti-reflection coatings on the backsides of the wafers. Figure 1 shows photographs of 150 mm diameter wafers with various CCDs presently being fabricated at DALSA Semiconductor and LBNL. Figure 1 a) shows 3512^2, 10.5 μm pixel CCDs for SNAP. The large CCDs in Fig. 1 b) are intended for use in the DES camera, and the format is 2048 × 4096 with 15 μm pixels. Figure 1 c) shows 4128 × 4114 and 4114 × 2040, 15 μm pixel CCDs for ground-based astronomy.

III. Gettering techniques for CCD wafer fabrication

The high-resistivity, n-type silicon used in this work is produced using float-zone refining [12], and the material is specified to have a minimum resistivity of 4 kΩ-cm with some wafers having resistivities as high as 13 kΩ-cm. A resistivity of 10 kΩ-cm corresponds to a donor doping density

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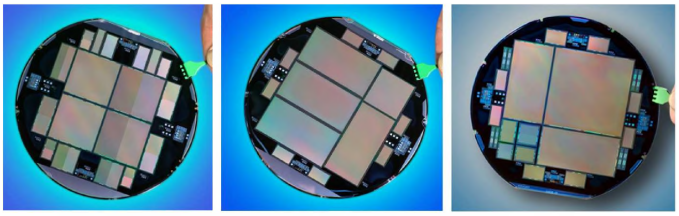
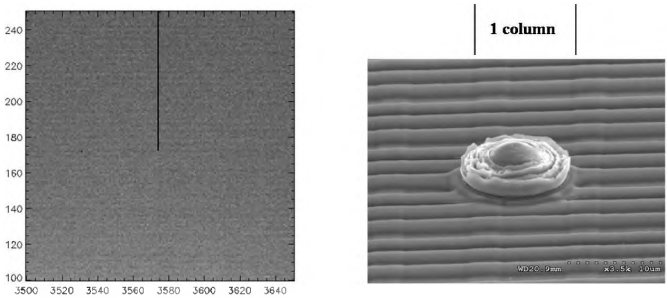


a) b) c)

Fig. 1. Photographs of 150 mm diameter wafers containing CCDs under development at LBNL. a) CCDs for the SuperNova Acceleration Probe. The format is 3512 × 3512, 10.5 μm pixel. b) CCDs for the Dark Energy Survey camera. The format is 2048 × 4096, 15 μm pixel. c) 4128 × 4114 and 4114 × 2040, 15 μm pixel CCDs for ground-based astronomy.



a) b)

Fig. 2. a) CCD sub-image showing one blocked column as a vertical dark line on the background due to uniform light exposure. The readout direction is to the bottom of the image. b) Scanning electron micrograph showing a defect due to the ISDP gettering process. The image was taken on a fully processed CCD. The horizontal lines in the picture are the polycrystalline silicon gate electrodes. The vertical stripes are the channel stops. Two of these channel stops run parallel to the bars at the top of the figure, which are added to emphasize the size of the defect relative to the column width.

of 4.3 × 10^{11} cm^{-3}, or roughly one dopant atom per 10^{11} silicon atoms.

We have described the use of in-situ doped (phosphorus) polycrystalline silicon (ISDP) on the backside of high-resistivity silicon substrates for gettering purposes [13]. The function of the gettering is to remove metallic impurities from the silicon substrate. Metal contamination can lead to increased dark current, resistivity changes, and reduced CTE. The presence of titanium contamination in an epitaxial layer was noted as the likely cause of CTE degradation in early versions of the pn CCD [14], [15].

Several thin film deposition steps are done to place the ISDP on the backside of the wafer, and prior to CCD processing the accumulated layers on the front side of the wafer are removed by etching. However, we have noted that the complete removal of the front-side films is difficult, and that significant numbers of particles remain on the front side of the wafer. We have correlated CCD defects including blocked columns and regions with excessively high dark current with some of the larger particles that remain after the gettering process. Blocked columns are columns that do not transfer the full signal or sometimes any signal for rows above the defect causing the blocked column.

Figure 2 a) is a CCD sub-image showing a blocked column, and Fig. 2 b) shows a defect that was correlated with blocked columns. The defect shown in Fig. 2 b) is approximately the width of one CCD column, and is disruptive to the following process steps that form the polycrystalline silicon gate electrodes. As a result it is not surprising that blocked columns result from such defects. More insidious, however, is the fact that we have also observed that these defects can cause electrical conduction between the gate electrodes and the CCD channels, and in some cases this problem is only seen after the CCD has been operated for some amount of time. In fact, we have seen blocked columns convert to columns with high dark current over time, resulting in long-term reliability concerns. We believe that insulator breakdown occurs between the gate electrodes and the CCD channels due to high electric fields resulting from the sharp edges that are formed during etching of the films that are deposited over the defects.

Since the large defects from the ISDP gettering process affect both the yield and the long-term reliability of the CCDs, it is important to minimize their occurrence and develop screening tests for their presence [11]. Particles of the type shown in Fig. 2 b) appear to be ubiquitous to the ISDP gettering process, and have also been observed in thick ISDP films deposited at LBNL. A likely contributor to the problem is the long deposition time on the order of 6–7 hours that is necessary to deposit a 1 μm thick ISDP layer.

In the following sections we describe two approaches to solving the particle problems observed with the ISDP gettering process.

A. *Re-polishing process with ISDP gettering*

One solution to the ISDP particle problem that has been implemented involves a re-polishing of the wafer surface after the ISDP gettering process is complete. The front-side films that accumulate during the gettering process are etched away as before. Following this the wafers are re-polished using a commercially available, chemical-mechanical polishing process. The particles are mechanically removed during the re-polishing step with typically not more than 10 μm loss of the silicon substrate.

Figure 3 shows wafer maps of particles taken with laser-based particle counters after the ISDP process (Fig. 3 a)) and after ISDP and re-polishing (Fig. 3 b)). The few particles that remain after re-polishing in the case of Fig. 3 b) are all sub-micron in size, and this is a typical result.

After re-polishing and wafer cleaning, a sampling of wafers are sent to a commercial testing laboratory where total reflection x-ray fluorescence (TXRF) measurements are done as a quality control monitor of the re-polishing process [16]. This technique can detect surface contamination for many metals at levels below about 1 × 10^{10} cm^{-2}, which corresponds to less than 10^{-4} of a monolayer on the silicon surface.

Wafer-level probing at -45°C is used as the first screening test of the finished CCDs, and the automated software analysis program can detect and report defects including blocked columns, backside defects, and pixels and columns with high dark current [11]. Table I shows the number of blocked columns seen for large-format CCDs that were fabricated on re-polished substrates. As can be seen, the re-polishing process

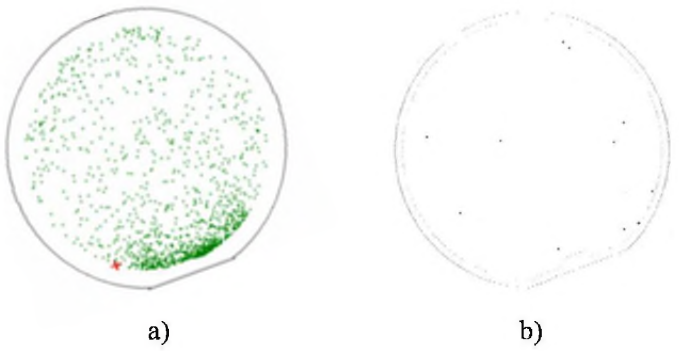


Fig. 3. a) Map of particles detected on a 150 mm diameter wafer after the ISDP gettering process. b) Map of particles detected on a 150 mm diameter wafer after the re-polishing process. All of the particles in b) are below 1 μm^2 in size.

TABLE I
BLOCKED COLUMN COUNTS FROM WAFER PROBING AT -45°C.

CCD Format	Wafer Finishing	# CCDs Tested	# Blocked Columns	Total # Columns	% Blocked Columns
2k ×4k	LBNL	23	17	47,104	0.04
2k ×4k	DALSA	23	8	47,104	0.02
3.5k^2	DALSA	14	0	49,168	0.0

is yielding less than a blocked column per large format CCD, which is a significant improvement when compared to ISDP-gettered wafers without the re-polishing step. The pixel size for the 2k × 4k CCD is 15 μm, and is 10.5 μm for the 3.5k^2 device. The CCDs finished at DALSA are 650–675 μm thick, while the CCDs finished at LBNL are nominally 250 μm thick.

Figure 4 shows images taken on packaged SNAP CCDs operated at -140°C that were fabricated on re-polished, ISDP gettered wafers. The CCDs were finished at DALSA Semiconductor and are 650–675 μm thick. Figure 4 a) shows an image taken with uniform illumination at a substrate bias voltage of 100V, and Fig. 4 b) shows the results of a 20 minute dark exposure taken at 200V. The events in Fig. 4 b) are due to cosmic rays and Compton electrons from background radiation in the local environment, and the starting material resistivity was sufficiently large such that the CCD is fully depleted at a substrate bias voltage of 200V. The dark current at -140°C and 200V was 0.4 e$^-$/pixel-hour. Neither CCD has blocked columns or pixels with large dark current. Measurements on another CCD from this lot with readout through 4 amplifiers yielded a per quadrant average ^{55}Fe energy resolution of 125 eV FWHM, serial and parallel CTE's exceeding 0.999999, and read noise of 3.9 e$^-$ rms, all at a readout rate of 100 kpixels/sec, substrate bias voltage of 100V, and operating temperature of -140°C.

The above results demonstrate very good fabrication yield on large area CCDs for the ISDP gettering process with re-polishing of the wafer surfaces to remove the surface particles.

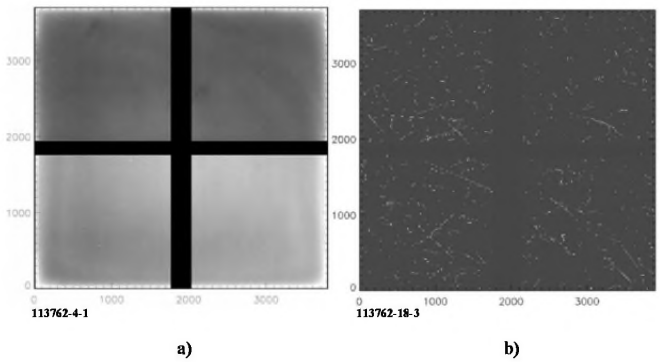


Fig. 4. a) CCD image taken with uniform illumination. The substrate bias voltage was 100V. The CCD was finished at DALSA Semiconductor and is 650–675 μm thick. b) Another CCD from the same lot as in a) but operated for 20 minutes in dark conditions at a substrate bias voltage of 200V.

B. Gettering layer supplied by the wafer manufacturer

The other approach to gettering that was investigated was to fabricate CCDs on high-resistivity silicon wafers that already include a backside gettering layer. Siltronic AG offers an undoped backside polycrystalline silicon gettering layer for their high-resistivity, float-zone refined silicon that is referred to for brevity as "poly backseal". Silicon starting material with poly backseal was obtained, and the mean resistivity for the lot was 11.1 kΩ-cm with a range of 9.1–13.1 kΩ-cm. CCD lots using the designs of Figs. 1 b) and c) were fabricated with the poly backseal material.

A concern was the possible reduced gettering efficiency of the undoped poly backseal layer when compared to ISDP. CCD performance can be adversely affected by ultra-low levels of metallic contamination, as evidenced by the report of poor CTE in pn CCDs arising from titanium levels of only about 10^{10} cm^{-3} [14]. The phosphorus that is incorporated into the ISDP films is very effective as a gettering layer, and the combination of backside polycrystalline silicon layers with phosphorus doping has been reported to be more effective in terms of gettering than either method used alone [17].

Another concern was the possibility of dark current artifacts in CCDs with the poly backseal coating due to the lack of a heavily doped, backside ohmic contact layer. This would affect the standard thickness CCDs that are fully processed at DALSA Semiconductor as quality control devices since CCDs finished at LBNL have a thin ISDP layer on the back of the device. Given that the minority carrier lifetime is very large in high-resistivity silicon, it was felt that one might see anomalously high dark currents in the undoped poly backseal devices due to dark-current-generating defects that are located in the backseal layer or at the interface with the single-crystal silicon. For quality control devices with the ISDP gettering, the ISDP layer itself provides the heavily doped, ohmic contact. This layer supplies electrons that fill the dark-current generation sites which reduces the dark current injected from the backside ohmic contact.

The recent development of high-voltage compatible, fully depleted CCDs with improved spatial resolution for SNAP [18] has resulted in the ability to sometimes fully

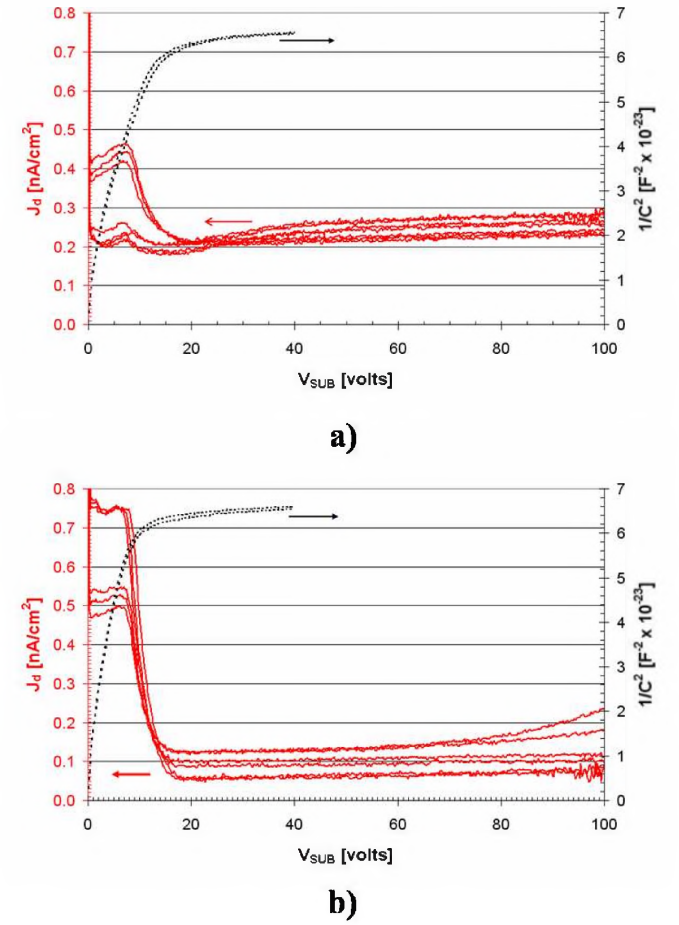


Fig. 5. Current-voltage and inverse square capacitance-voltage measurements on 2 mm^2 p-i-n diodes fabricated on the same wafers as the CCDs. a) Results for an ISDP-gettered wafer with re-polishing. b) Results for an undoped poly backseal wafer with phosphorus doping of the backseal layer during the processing.

deplete the standard thickness, quality control CCDs that are completely finished at DALSA Semiconductor. These thick, fully depleted CCDs could have applications in direct x-ray detection. One would expect that the dark current concerns noted above with the undoped poly backseal layer would be even more of an issue for a fully depleted device, where we have shown the existence of backside defects that generate dark current when the depletion region extends to the backside of the CCD [11], [18]. The CCD of Fig. 4 b) is an example of a 650–675 μm thick CCD that was fully depleted at a substrate bias voltage of 200V.

Given these considerations, one lot of wafers were processed with the undoped poly backseal gettering with some of the wafers receiving a phosphorus diffusion into the backseal layer. In addition, another lot was processed with roughly half of the wafers processed with phosphorus-doped poly backseal, and the other half with ISDP gettering and re-polishing.

Figure 5 shows dark current and capacitance measurements on 2 mm^2 p-i-n diode test structures that are fabricated on the same wafers as the CCDs. In this case the wafers were

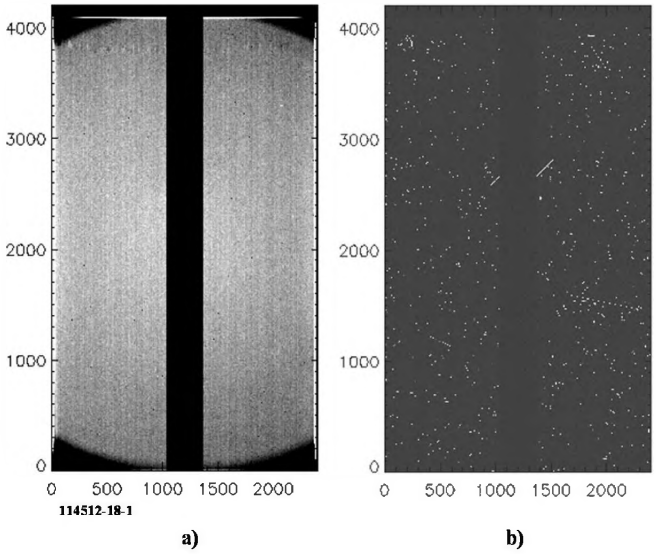


Fig. 6. CCD images taken on a 2k $\times$ 4k CCD fabricated with the undoped poly backseal gettering layer that was doped with phosphorus during the process. a) Image taken under the conditions of uniform illumination. b) 30 minute exposure under dark conditions. All measurements were done at a substrate bias voltage of 40V and an operating temperature of -140°C. The CCD thickness is 250 μm and the wafer was finished at LBNL.

thinned to 250 μm thickness and completed at LBNL. As mentioned above, a thin, approximately 20 nm thick ISDP layer is used as the backside contact in order to achieve good quantum efficiency at short wavelengths [9]. Figure 5 a) shows measured data for the ISDP-gettered process with re-polishing, and Fig. 5 b) presents the results for the poly backseal gettering with phosphorus doping during the process. The wafers were from the same fabrication lot, and therefore the comparison between the gettering techniques is valid. Both methods achieve sub-nA/cm^2 dark current with depletion voltages of about 20V that are determined by the leveling off of the inverse square capacitance curves.

Our experience with the testing of packaged poly backseal CCDs at low temperatures is somewhat limited to date. One item of note is the appearance of localized areas with poor CTE observed on some devices with the undoped poly backseal that was doped with phosphorus at the beginning of the CCD process. This has been limited to the center of the wafer and the source of the CTE degradation is not known at the present time. Figure 6 shows results measured on a back-illuminated, 2k $\times$ 4k CCD fabricated with the phosphorus-doped, poly backseal gettering layer and finished at LBNL. This device was not located in the center of the wafer and has no obvious CTE problems. The dark current measured at -140°C was 5.2 e$^-$/pixel-hour, and the read noise at a readout rate of 70 kpixels/sec was 3.1 e$^-$ rms. To date we have not observed CTE problems with CCDs fabricated with the undoped poly backseal gettering, i.e. no doping with phosphorus during the processing at DALSA Semiconductor.

Figure 7 shows a dark current comparison for wafers with the undoped poly backseal gettering process. It is seen that the dark current on the standard thickness wafer is anomalously high, and given the above discussion we attribute this to the

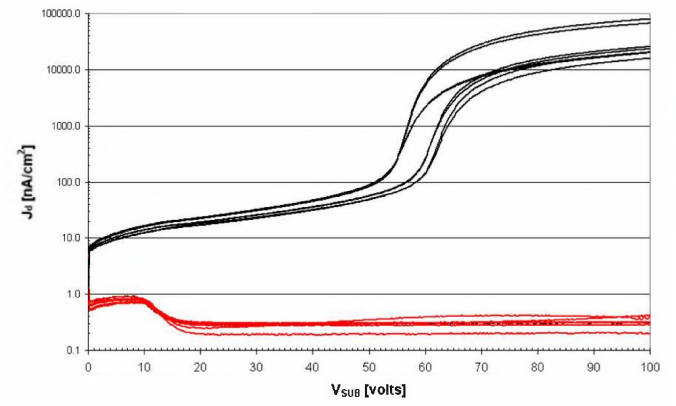


Fig. 7. Current-voltage measurements on 2 mm^2 p-i-n diodes fabricated on the same wafers as the CCDs, and also fabricated on wafers with undoped poly backseal gettering. The high dark currents were seen on a standard thickness, 650–675 μm thick wafer fully finished at DALSA Semiconductor. The low dark current data is for a 250μm thick wafer finished at LBNL with an approximately 20 nm thick ISDP layer on the backside of the wafer.

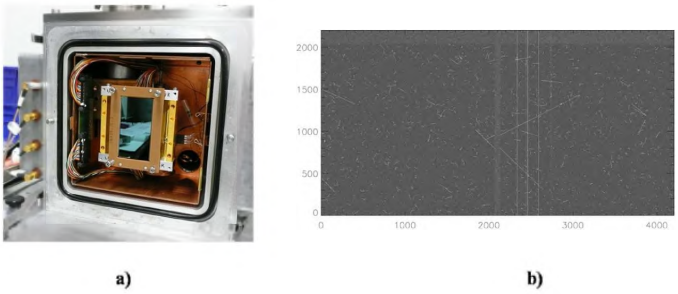


Fig. 8. a) Photograph of a 4k $\times$ 2k, 15 μm pixel CCD installed in a test dewar. b) Image taken after a 30 minute exposure under dark conditions. The substrate bias voltage was 100V and the operating temperature was -140°C. The CCD thickness is 250 μm and the wafer was finished at LBNL.

lack of electron filling of generation sites in the undoped poly backseal layer and interface with the single-crystal silicon. However, the test p-i-n diodes show excellent dark current when the wafers are thinned to a thickness of 250 μm and completed with the thin ISDP layer described above, as shown in Fig. 7. This is further evidence that the high dark current seen in Fig. 7 is not due to poor gettering but rather is an artifact due to the lack of a heavily-doped, backside ohmic contact in that case. Similar effects have been noted on packaged CCDs that were tested at cold temperatures. CCDs with undoped poly backseal layers have high dark current when fully depleted, but devices finished at LBNL have dark currents comparable to the ISDP-gettered CCDs.

IV. Progress towards the development of 4k $\times$ 4k, 15 μm pixel CCDs

The improvements in CCD fabrication yield described in the previous sections are necessary in order to contemplate very large area CCDs fabricated on high-resistivity silicon. The DALSA Semiconductor CCD process has produced extremely large CCDs on low-resistivity silicon, including a 111 Megapixel CCD with a format of 10,560 $\times$ 10,560 with 9 μm pixels [19]. Given this high yielding process and the improvements in the gettering techniques described earlier for high-resistivity substrates, we have begun the development of a 4k $\times$ 4k, 15 μm pixel CCD with a die size of about (64 mm)^2.

In parallel with the CCD fabrication efforts we are developing a packaging technique with a major emphasis on good die flatness after packaging. This is based on earlier work by Stover *et al* [20], and involves holding the CCD die and AlN support plate on separate vacuum chucks. The chuck holding the CCD is machined to be very flat, and the function of this chuck is to take out the inherent bow of the thinned silicon die. The two chucks are brought in proximity with each other, and the AlN plate is glued to the front-side of the CCD while each piece is held on their individual vacuum chucks. The AlN both mechanically supports and serves as the thermal contact to the CCD.

Figure 8 a) shows a photograph of a fully finished, 250 μm thick 4k $\times$ 2k CCD installed in the dewar with the flat packaging technique described above. The packaging method is achieving at room temperature total flatness variations over the die of about 5 μm with a range of 3–7 μm for the 4k $\times$ 2k die.

The 4k $\times$ 4k and 4k $\times$ 2k CCDs, shown earlier in Fig. 1 c), were designed to be compatible with large substrate bias voltages [18]. This allows for good spatial resolution for thinned devices, and possible full depletion of thick devices if the starting resistivity is sufficiently large.

Fig. 8 b) shows an image taken at -140°C after a 30 minute exposure in dark conditions. The dark current was 3.9 e$^-$/pixel-hour. The CCD was read out through 2 of the 4 amplifiers. One amplifier was non-functional. The CCD has 4 columns with above average dark current, although only one of the four had saturated pixels due to dark current in the 30 minute exposure. CTE measured with ^{109}Cd K_α x-rays was 0.999997 (parallel) and $>$ 0.999999 (serial). The CCD was operated at a substrate bias voltage of 100V, which amounts to about 80V of overdepletion. Poly backseal gettering was used, and the gettering layer was doped with phosphorus near the beginning of the fabrication process.

Packaging development for the larger 4k $\times$ 4k CCD is in progress, with preliminary results showing slight degradation in the flatness achieved to date when compared to the 4k $\times$ 2k results.

V. Conclusion

In conclusion, improved gettering techniques have been demonstrated to allow for both effective gettering of high-resistivity silicon substrates and high fabrication yield due to the elimination of the surface particles that have plagued the ISDP gettering process. Re-polishing of ISDP-gettered wafers has been shown to work well, and gettering with backside undoped polycrystalline silicon layers supplied by the wafer manufacturer appears to be promising as long as the devices are finished with a proper backside ohmic contact. These advancements should allow for the fabrication of very large format, fully depleted CCDs.

VI.

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