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Wireless Integrated Circuit for 100-Channel Neural Stimulation

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***Abstract*—We present the design of an integrated circuit for wireless neural stimulation, along with bench-top and *in-vivo* experimental results. The chip has the ability to drive 100 individual stimulation electrodes with constant-current pulses of varying amplitude, duration, interphasic delay, and repetition rate. The stimulation is done using a biphasic (cathodic and anodic) current source, injecting and retracting charge from the nervous system. Wireless communication and power are achieved over a 2.765-MHz inductive link. Only two off-chip components are needed to operate the stimulator: a 10-nF capacitor to aid in power supply regulation and a coil for power and command reception. The chip was fabricated in a commercially available 0.6-µm 2P3M BiCMOS process. The chip was able to activate motor fibers to produce muscle twitches via a Utah Slanted Electrode Array implanted in cat sciatic nerve, and to activate sensory fibers to recruit evoked potentials in somatosensory cortex.**

I. Introduction

There has recently been much success and research into applications for electrical neural stimulation including deep brain stimulators, visual and auditory neural stimulators, and neuromuscular stimulators for the purpose of contracting paralyzed or otherwise disabled muscles [1-3]. At the University of Utah, we have undertaken a research project to design and implement a low-power, implantable, wireless neural stimulator. Recent advances in circuit integration have led to the ability to flip-chip bond microchips directly to the back of a 100-channel MEMS Utah Slanted Electrode Array (USEA) or Utah (non-slanted) Electrode Array (UEA) [4]. The stimulator under development will take advantage of the selectivity inherent in the USEA or UEA, and could, for example, be used in next-generation prosthetic devices to provide tactile and proprioceptive sensation to persons with amputations. The internal feedback could be created by injecting and retracting charge from sensory nerves in the residual limb. The stimulator could also activate motor fibers in nerve to reanimate paralyzed muscles, or activate cortical neural tissue to restore lost sensory function. This Integrated Neural Interface (INI) stimulator project is an extension of and a complementary design to an INI neural recording system also developed at the University of Utah [5].

In this paper, we present a fabricated and tested 100-channel wireless neural stimulator chip. The first integrated neural interface stimulator chip (INIS1) uses a biphasic constant current source (Fig. 1) to provide neural stimulation. The rapid injection and retraction of charge changes the local extracellular potential sufficiently to trigger action potentials in nearby axons. In order to deliver precise and reproducible control, the neural stimulator controls stimulation timing onboard after the desired values are programmed via wireless command transmission. Stimulation parameters may be reprogrammed at any time, and individual electrode sites may be activated or shut down at any time. Only two off-chip components are needed to operate the stimulator: a 10-nF capacitor to aid in power supply regulation and a coil for power and command reception. System-level chip designs as well as experimental results from bench-top testing and *in-vivo* nerve stimulation sessions are presented here.

II. INIS1 System Design

The 4.6 × 5.4 mm^2 INIS1 integrated circuit was fabricated in a commercially available 0.6-µm 2P3M BiCMOS process (Fig. 2). The majority of the layout area is occupied by a 10 × 10 array of stimulation cells with bond pads that match the 400-µm pitch of a USEA or UEA. Each of the 100 stimulation sites can be independently programmed and controlled. Power is supplied to the chip via a 2.765-MHz inductive link. The voltage rectifier converts the ac coil voltage to an unregulated dc voltage; an on-chip regulator provides a nominal 5-V supply. The system clock is also obtained from the ac coil voltage; commands are sent to the chip via amplitude-shift keying (ASK) of the 2.765-MHz power signal [5]. The power link frequency is divided by two in order to obtain the system clock frequency of 1.38 MHz.

The 10×10 array of stimulators is controlled by one master finite state machine (FSM). The master FSM interprets commands received from the ASK-modulated power signal and communicates with the selected electrode site to program the current pulse amplitude, duration, interphasic delay, and repetition rate for that specific site. Each stimulator has independent values for each parameter that are stored in local registers. In order to produce the needed biphasic current pulse, each stimulator is made up of both analog and digital components. Fig. 3 illustrates the system-level design as well as the components of a typical stimulator. Each site contains a digital-to-analog converter (DAC), output stage, charge recovery circuit, internal FSM, token cell, counter, and register bank.

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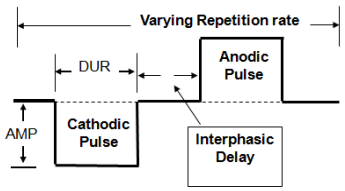

Figure 1. Diagram of biphasic current pulse produced by INIS1 chip.

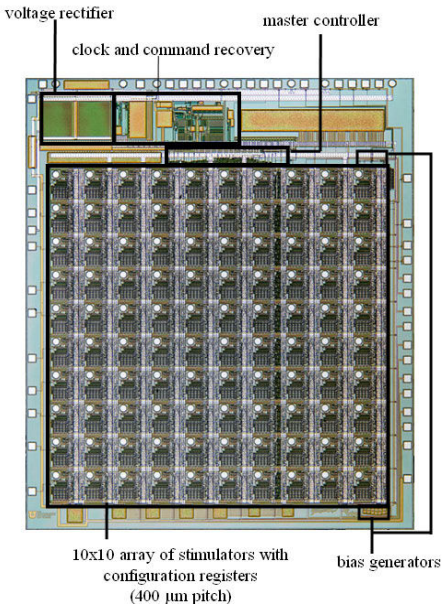

Figure 2. Microphotograph of 4.6 × 5.4 mm^2 INIS1 wireless neural stimulation chip, fabricated in a commercial 0.6-µm 2P3M BiCMOS process.

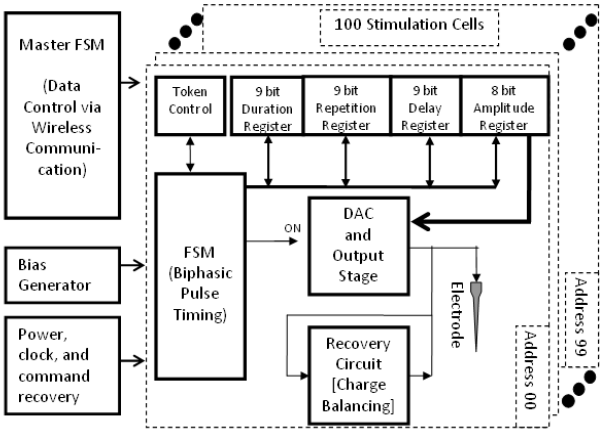

Figure 3. Block diagram of the master finite state machine, bias generator, power, clock, and command recovery, and electrode contact.

The digital components for each stimulation site set the timing and control of the analog circuitry. The analog circuitry generates the current amplitude and direction for stimulation specified by the digital components. Each stimulation cell consists of three analog subcircuits: An 8-bit MOSFET *R*-2*R* DAC [6] to provide a stimulation current; an output stage to amplify and control whether the current is sourcing or sinking from/to the electrode; and a charge recovery circuit to bleed off or supply small amounts of current to the electrode to ensure proper charge balancing. The entire chip contains one analog bias generator network to provide currents and cascode voltages used in the analog components of the individual stimulation cells.

The output stage (Fig. 4) serves multiple purposes. First, to conserve power, the DAC was designed to produce a current of 0.1 to 25 µA, a tenth of the desired stimulation current of 1-250 µA. The output stage amplifies the current by a factor of ten. Second, the output stage provides the ability to source or sink current from/to the electrode, with the sourcing and sinking well matched in order to maintain a charge balance on the electrode. Third, the output voltage swings close to the power rails of ± 2.5 V to maximize the compliance voltage.

The layout of the output stage uses wide-swing cascode current mirrors to achieve a wide operating range. Transistors M3 and M4 are used to switch between sourcing or sinking current to the electrode. The gates of these two transistors are controlled by the internal FSM. Transistors M1, M2, M5, and M6 were sized ten times larger than transistors M10, M9, M8, and M7 to produce the current needed to stimulate the neurons. Transistors M2, M5, M8, and M9 are used as cascode devices. These transistors are used to bias the drain-to-source voltages of transistors M1, M6, M7, and M10 so that they remain just above the triode region. Holding the drain voltages just above the triode region allows for a larger output swing voltage at the output node while maintaining near-constant current operation. Though all of the transistors are operating in the saturation region, second-order effects will cause a slight mismatch between cathodic and anodic output currents; thus, the need for a charge recovery circuit. We use an operational transconductance amplifier (OTA) configured as a buffer and biased in the subthreshold region to implement a weak charge recovery operation. The OTA amplifier, designed to have a maximum current output of ±235 nA, acts as a small secondary sink or source dependent on the residual charge remaining in the tissue.

The digital components on a single stimulator store and control the parameters of the biphasic current pulse. The communication to the external world happens via the master FSM. The master FSM decodes the incoming command bits to obtain a specific site address as well as preparing the data to be stored in the registers for the individual electrode. The master FSM routes the command data to the correct stimulator location. It also serves as a handshaking tool that ensures that the data are properly stored before allowing access to another site. The internal FSM for each site is used to store the data transmitted from the master FSM to the site registers. The on-site FSM, along with a counter, controls the timing for the biphasic pulse. Each stimulator contains four registers to store the amplitude, duration, interphasic delay, and repetition rate. The amplitude register consists of eight bits and allows the current to range from 1 - 255 µA with a resolution of 1 µA. The duration register consists of nine bits, allowing the duration to range from 1.45 - 370 µs with a resolution of 725 ns. The interphasic delay register has the same scale and resolution as the duration register. The repetition register consists of nine bits, but the highest order bit is used to determine if the cell is active or not. The actual repetition rate

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range is 0.66 - 168 Hz, with a repetition period resolution of 6 ms. Having the registers on chip and local to each stimulator gives precise, reproducible control over each biphasic pulse.

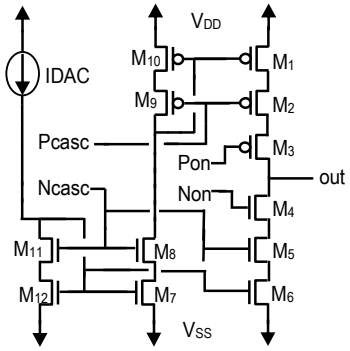

Figure 4. Schematic of wide swing cascoded output stage.

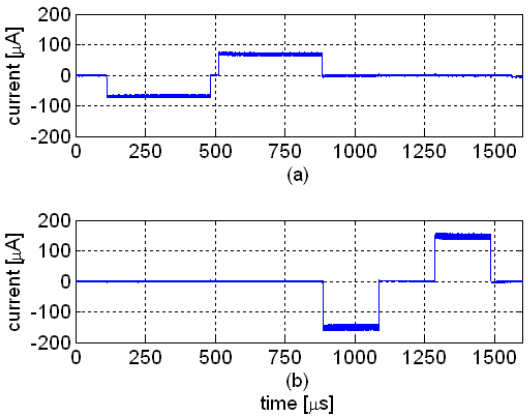

Figure 5. Stimulation pulses over 10 kΩ resistive load with the following parameters: Electrode 1 programmed with amplitude of 75 μA, duration of 370 μs, and interphasic delay of 30 μs; Electrode 2 programmed with amplitude of 150 μA, duration of 200 μs, and interphasic delay of 200 μs.

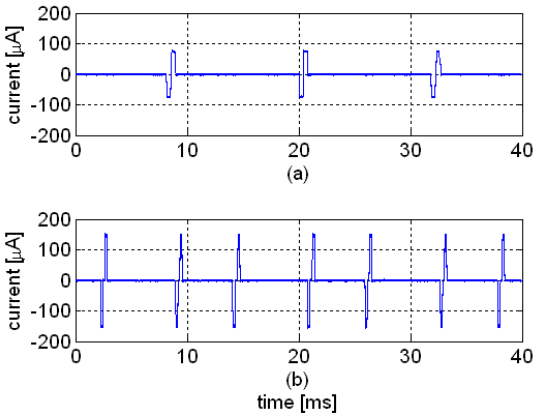

Figure 6. Stimulation pulses from Fig. 5 viewed on a wider time scale: Electrodes 1 and 2 were programmed with repetition rates of 88 Hz and 166 Hz, respectively.

An important system-level digital component in our chip is the token cell. If all the stimulators were firing simultaneously, the power dissipation would exceed a safe limit, given thermal safety considerations for the surrounding tissue. As a safety precaution, a token method was implemented to coordinate chip-wide stimulation patterns. Individual stimulation cells may fire a pulse only if the token is present in the current cell. If a current pulse is due, the cell performs the firing sequence and then immediately passes the token along to the neighboring stimulator. If a current pulse is not due at a particular stimulator, then the token is simply passed to the next site with a delay of one clock cycle. This token system prevents two electrodes from firing simultaneously. This limits power dissipation to safe levels at the expense of true simultaneous multi-electrode stimulation. In the (unrealistic) upper limit in which all 100 electrodes are activated with the maximum pulse width of 370 μs, the maximum stimulation frequency for any one electrode would be 9.1 pulses/s.

III. Bench-Top Testing

After fabrication, the INIS1 chips were first tested for basic functionality in a bench-top configuration. Because of process variations, the on-chip bias generators produced slightly smaller currents than the nominal simulation values. This limited the total output current to a range of 0.85 to 216 μA. Figs. 5 and 6 show (at different time scales) biphasic pulses generated during a bench-top experiment with power, clock, and command signals delivered wirelessly over an inductive link. The experiments were performed with a simple 10 kΩ resistor acting as a simplified electrode model. Electrodes 1 and 2 were successfully programmed with pulses of different current amplitudes, durations, interphasic delays, and repetition rates. Note that electrode 2 begins to fire as soon as electrode 1 finishes its firing sequence, because of the token method described earlier.

IV. *In-Vivo* Experiments

To validate the operation of the INIS1 chip with biological tissue, we performed *in-vivo* nerve stimulation experiments. A USEA was inserted into the sciatic nerve in the left leg of an anesthetized cat, and the INIS1 chip was used to stimulate the nerve through various individual electrodes in the array. Most importantly, INIS1 was able to activate both motor and sensory nerve fibers via multiple different electrodes.

Because complete flip-chip integration is not yet complete, all experiments were performed using an INIS1 chip on a small circuit board. A stimulator from the chip was wired to a separate electrode array, and chip ground was wired to a reference wire near the array. The only other off-chip components connected to the chip were a 10-nF capacitor and a 5.8-cm power receive coil. Power, clock, and command signals were sent wirelessly from a 5.8-cm transmit coil positioned 1.8 cm from the receive coil.

As expected, the measured voltage on a USEA electrode during INIS1 stimulation co-varied with the current amplitude (Fig. 7) and duration. The shape of the electrode voltage curves reveals both the resistive and capacitive elements of the electrode-tissue interface. When stimulation was delivered through this electrode with a pulse duration of 370 μs, current amplitudes greater than 15 μA evoked observable muscle twitches in the leg. At current levels between 33 and 100 μA,

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the electrode and tissue impedance limited the amount of charge that could be injected into the tissue given our limited compliance voltage, as indicated by the curves in Fig. 7.

We tested the ability of INIS1 to recruit physiological responses on ten of 74 USEA electrodes that had separately been demonstrated to be capable of evoking motor responses via 2.2-V, 370-µs monophasic negative pulses delivered by a conventional stimulator. On all 10 electrodes, stimulation via INIS1 was able to recruit motor responses, as monitored visually and via EMG wires implanted in four leg muscles. Motor responses evoked by INIS1 were studied more systematically for two electrodes by varying the current amplitude or the duration of the stimulus pulses, and measuring the amplitude of the resultant evoked compound muscle action potentials (Fig. 8). For both electrodes, the evoked responses grew systematically with increasing stimulus strength (either amplitude or duration), and activation of muscles showed a high degree of selectivity. EMG responses saturated below 100 µA, in some instances perhaps because of INIS1's limited compliance voltage. Still, strong muscle contractions were produced at this level of stimulation.

Stimulation via INIS1 also elicited evoked potentials (EPs) in primary somatosensory cortex, as monitored by recordings from screws in the overlying skull. EPs exhibited a short onset latency (5 ms) and were spatially localized over somatosensory cortex (Fig. 9). Further, cortical EPs persisted after severing the nerve distal to the array, which abolished muscle contractions and hence possible secondary activation of sensory systems. These results indicate that INIS1 can also directly activate sensory nerve fibers and thus may be able to provide illusory tactile or proprioceptive information.

V. Conclusions

We have demonstrated *in-vivo* functionality of a programmable wireless neural stimulation chip that produces biphasic current pulses. The precise and reproducible control of the nerve stimulator allowed us to elicit continuously-varying muscle contractions from nerve stimulation. Wireless operation provided isolation and remote configurability of the integrated circuit. This chip ultimately will be bonded to the back of a USEA or UEA, producing a fully implantable neural interface capable of nerve or cortical stimulation.

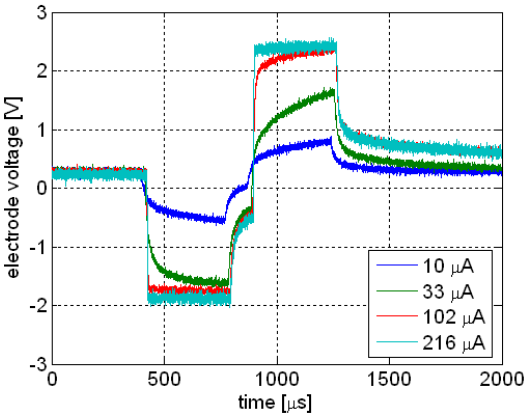

Figure 7. Electrode voltage curves *in vivo*, captured while stimulating the sciatic nerve of an anesthetized cat.

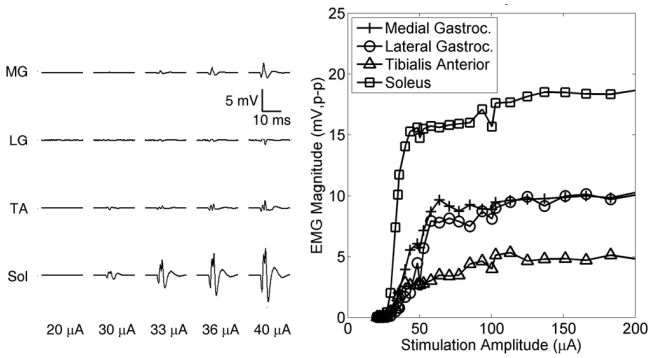

Figure 8. Evoked raw (left) and quantified (right) EMG activity resulting from INIS1 370-µs pulses with amplitudes as indicated.

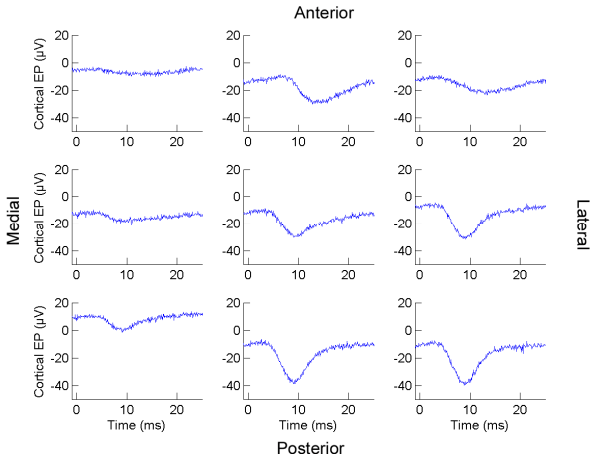

Figure 9. Wireless stimulation of sciatic nerve evokes potentials localized over primary somatosensory cortex. Each trace represents the averaged EP recorded from one of nine skull screws in a 3×3 grid with ~5-mm spacing.

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