Challenges and Solutions in Measuring Computer Power Supply Efficiency for 80 PLUS® Certification

Faisal H. Khan, Thomas D. Geist, Baskar Vairamohan, Brian D. Fortenbery, Eric Hubbard
Electric Power Research Institute
942 Corridor Park Blvd.
Knoxville, TN 37932, USA

***Abstract*- This paper discusses the techniques, challenges, and results of measuring computer power supply (CPS) efficiency, power factor (PF), and input harmonic currents for the 80 PLUS® program since its beginning in 2002. To date, over 750 power supplies have been tested with many certified for the 80 PLUS® program. In spite of the large number of power supplies tested and years of testing, there is uncertainty within the computer power supply industry about the correct method for measuring efficiency, power factor, and harmonics. Moreover, in order to improve efficiency at light loading, manufacturers are adopting a duty-cycle control approach to power factor correction that raises even more questions on the proper measurement techniques. This paper presents detailed results of years of computer power supply testing, provides a detailed technical analysis on measurement accuracy with background on why specific measurement techniques were adopted, and looks to the future on upcoming technical difficulties and offers solutions for overcoming these difficulties.**

I. Introduction

The personal computer (PC) has become an indispensable appliance in modern offices and homes. One of the effects of the ever-rising number of PCs has been their increasing share of electrical power consumption. As a result, utilities and their customers are concerned about the performance of PCs as electrical loads. The power consumption issue is particularly important in view of the historically low efficiency of PC power supplies. Not long ago, efficiencies between 50% and 60% were common for power supplies used in desktop computers. Industry efforts as well as government initiatives such as the EPA Energy Star program have led to significant improvements in power supply efficiencies.

There are still numerous opportunities to build on the progress already achieved by reducing overall power consumption in computers. In particular, computers still consume an appreciable amount of power during the times when they are on but are not being used. The time that a computer spends in this "idle" mode can add up to several hours of every day. Overall PC energy efficiency (in terms of energy consumed per useful work performed) can be measurably enhanced by reducing PC power consumption during these idle periods.

In addition to their standby power consumption, other load characteristics of PCs also demand proper investigation. Specifically, the harmonic currents generated by PC power supplies can affect their interaction with other local loads and may have impacts on the entire power system. PCs are also susceptible to external disturbances, such as voltage sags and power interruptions, originating elsewhere on the power grid. The ways that PC power supplies affect the bulk power system, as well as their reaction to disturbances, constitute the field of "system compatibility," and is another important area of study. While this area has been studied extensively in the past, there is some concern that more efficient power supplies may behave differently from previous systems, requiring some investigation into the differences between new products and their older counterparts.

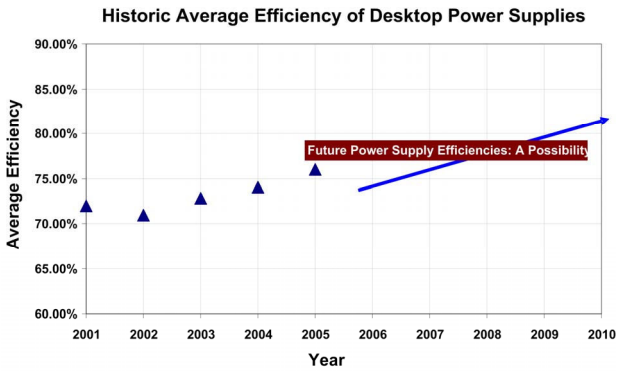
The efficiency of a state of the art computer power supply (CPS) for desktop and server may reach anywhere from 85-92%; however, it was only 60-70% six years ago [1]-[10]. Various modifications in the architecture, better component selection and improvements in the circuit design have elevated the efficiency of the CPS unit. Industry efforts as well as government initiatives such as the EPA Energy Star program have led to this significant improvement in efficiency [6]. A continuing effort towards reduction of power consumption in PCs has resulted in a number of government and industry initiatives, including programs such as 80 PLUS®, which advocates the replacement of conventional power supplies with new, highly-efficient models. The historic efficiency profile of the CPS is shown in Fig. 1.

A concerted effort towards the development and adoption of more efficient power supplies began in 2002, when ECOS Consulting presented a paper to the Natural Resources Defense Council (NRDC) that U.S. electricity consumption could be reduced by more than 1% yearly – over 32 billion kWh of energy worth at least $2.5 billion in annual savings. In the years since, a diverse body of stakeholders, including the NRDC, the California Energy Commission (CEC), the Environmental Protection Agency (EPA) Energy Star program, ICF Consulting Group, ECOS Consulting, Lawrence Berkeley National Laboratory (LBNL), EPRI and many others, with expertise in the technical, economic, marketing, and public policy aspects of energy efficiency, have led the effort to develop better, more efficient power supplies for electronics used in the United States.

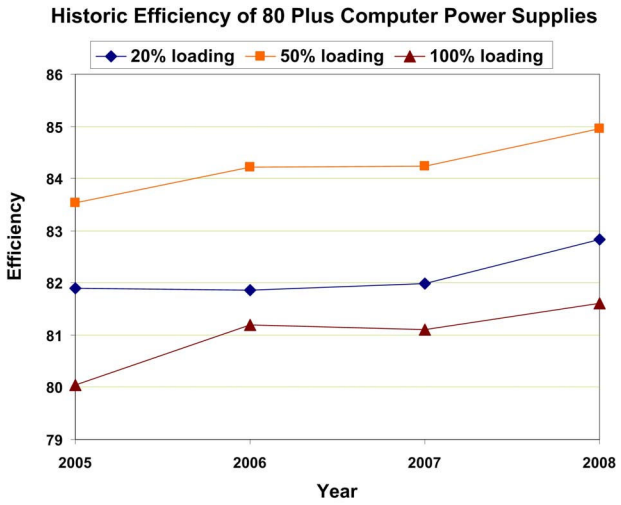
II. The 80 PLUS® Compliance Definition

80 PLUS® is a standard originally proposed by ECOS Consulting and Electric Power Research Institute (EPRI) back

978-1-422-2812-0/09/$25.00 ©2009 IEEE



(a)



(b)

Fig. 1. (a) Historical average efficiency of OEM computer power supplies from 2001-2005, (b) average efficiency of 80 PLUS® power supplies from 2005-2008 time period [1].

in 2002 [11]. The outcome of various investigations reveals that a typical CPS offers the highest efficiency at 50% loading condition [1]. Because of the inductive energy transfer method (IETM) architecture, these CPSs offer degraded efficiency profile at 20% or at 100% load [12]. Therefore, ECOS and EPRI proposed a standard with some suggested modifications in the circuit design. This initiative was a key factor to save a substantial amount of energy that used to be lost in millions of CPSs every year. According to the definition, a power supply which complies with the 80+ standard must operate at 80% efficiency at 20%, 50%, and 100% loading conditions and should also have 90% power factor at 100% loading conditions [11].

III. Various Major Parts in a Power Supply

Multiple voltage buses with different current supplying capabilities are present in a typical modern CPS. These bus voltages usually comply with a standard defined by the computer manufacturers. In spite of the variations in the different standards, the 3.3V, 5V and the 12V buses are present in any power supply designed in the last eight (8) years. However, there are usually multiple 12 V buses in present day's power supplies in order to provide additional power for the CPU and other components of the computer [5][13]. The various sections in a present day CPS is shown in Fig. 2.

Most of the present days' power supplies are equipped with an active power factor (PF) correction circuit at the input side of the CPS. A passive rectifier followed by a boost stage is typically used for the PF correction. This stage produces a dc bus voltage approximately at 380V, and the PF correction circuit provides a wide input voltage operation (90-250V ac) as an additional advantage. The 380V dc bus is then traced through isolated dc-dc converter stages to produce various voltage levels needed for a computer. A modern power supply typically delivers a significant portion of the total power through the 12V buses.

IV. Test Algorithm and Efficiency Definition

For power supplies with multiple output voltage buses, it is difficult to define a consistent loading-criteria because each bus has a rated dc output current. Loading the busses to their individual current maximums often will exceed the overall rated dc output power of the power supply. Maximum power rating of the power supply and maximum current rating of individual buses are generally mentioned on the nameplate of the power supply. For a typical power supply with three voltage buses, if these maximum current ratings are x, y, z for 12V, 5V and 3.3V respectively, the maximum power supplied by the power supply would be T = 12x+5y+3.3z at an extreme condition. However, the maximum power handling capability M of the CPS would be significantly less than T in most cases. For this reason, a scaling factor known as the "Derating Factor (DF)" needs to be included so that the total power sourced by these buses does not exceed the overall maximum value [14]. Thus,

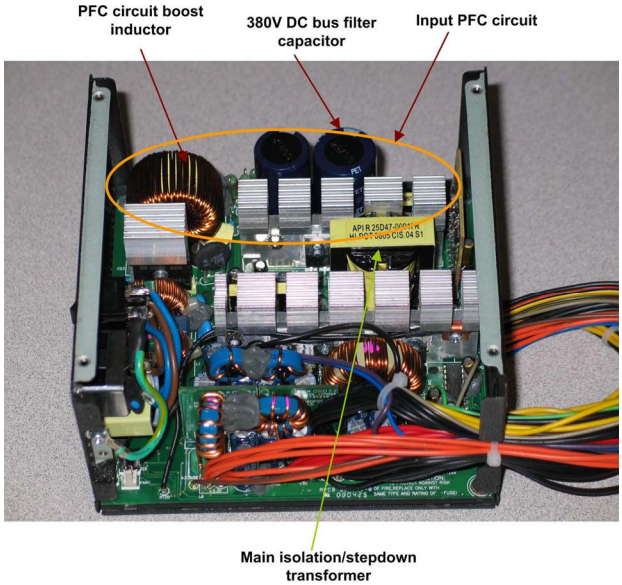


Fig. 2. Various components of a recent computer power supply with 80 plus compliance.

$$DF = \frac{P}{(V_1 * I_1) + (V_2 * I_2) + (V_3 * I_3) + (V_4 * I_4)} \quad (1)$$

Where, V and I are the voltages and currents of various buses, and P is the maximum overall power handling capability of the CPS. Generally DF is less than 1, and it used accordingly to deduce the current magnitude for a particular loading condition. Thus,

$$I_{load} = I_{rated} \bullet DF \bullet (LF/100) \quad (2)$$

Where, LF is the loading factor of the bus in %, I_{load} is the load current, and I_{rated} is the maximum current limit of that particular bus. Typically, power supplies are tested at 20%, 50% and 100% loading conditions (LF). Thus, the efficiency at a certain LF would be,

$$\eta = (V_1 \bullet I_{load1} + V_2 \bullet I_{load2} + \ldots\ldots\ldots + V_n \bullet I_{loadn}) / P_{in}(ac) \quad (3)$$

The computation acquires an additional degree of complication when the manufacturer also defines the maximum power handling capability of a sub-group of buses inside the CPS. In some cases, the power supply manufacturer specifies the rated dc output power for a subgroup of busses in addition to the overall rated dc output power of the power supply. An example of this type of power supply is a computer power supply with an overall rated dc output power of 330 W and a rated dc output power of 150 W for the +5 V and +3.3 V busses combined. Loading each bus to its individual rated dc output current may now exceed both the overall power supply's rated dc output power and the subgroup's rated dc output power. This section outlines a procedure for ensuring that both the subgroup and overall current ratings are not exceeded.

Assume a power supply with six output voltage busses with an overall rated dc output power P_T. Let the rated dc output power for subgroup busses 1 and 2 be P_{S1-2} and a rated power for subgroup busses 3 and 4 be P_{S3-4} and the ratings for bus 5 and 6 be simply equal to the product of their individual voltages and currents. A sample output specification of this power supply is shown in Table 1. The calculation of the derating factors are performed in two steps.

TABLE 1.
MAXIMUM CURRENT AND POWER RATINGS OF VARIOUS VOLTAGE BUSES AND SUB-GROUPS IN A CPS.

Output voltage of each output bus	Maximum rated output current of each bus	Maximum rated output wattage for subgroups V_1, V_2 and V_3, V_4	Maximum Power Supply Total Rating
V_1	I_1	P_{S1-2}	P_T
V_2	I_2		
V_3	I_3	P_{S3-4}	
V_4	I_4		
V_5	I_5	P_{S5}	
V_6	I_6	P_{S6}	

Step 1: Derating factors DF_{S1} to DF_{S6} for each of the subgroups are calculated using (4).

$$DF_{S1-2} = \frac{P_{S1-2}}{(V_1 * I_1 + V_2 * I_2)}$$
$$DF_{S3-4} = \frac{P_{S3-4}}{(V_3 * I_3 + V_4 * I_4)}$$
$$DF_{S5} = \frac{P_{S5}}{(V_5 * I_5)} \quad (4)$$
$$DF_{S6} = \frac{P_{S6}}{(V_6 * I_6)}$$

If the derating factor DS $\geqslant$ 1, then it is clear that when the subgroup is loaded to the rated dc output currents, the subgroup rated output powers will not be exceeded and there is no need for derating. However, if one or more DS factors are less than 1 then the subgroup power will be exceeded if the outputs are loaded to their full output currents and there is a need for derating.

Step 2: There is also a need to check whether the sum of the subgroup maximum rated powers is greater than the total maximum power rating of the power supply (P_T). If the sum of the subgroup maximum rated powers is greater than the overall power rating of the power supply then a second derating factor DF_T must be applied. This factor is calculated as shown in (5).

$$DF_T = \frac{P_T}{P_{S1-2} + P_{S3-4} + P_5 + P_{S6}} \quad (5)$$

If $DF_T \geqslant 1$ then no derating is needed.

If $DF_T < 1$ then the derating for each of the outputs has to be applied and is shown in Table 2. It shows the guideline for X% loading of the power supply based on $DF_S < 1$ and $DF_T < 1$.

V. DIFFICULTIES IN THE MEASUREMENT

There are many hidden obstacles to measure the power supply efficiency and achieve accuracy to some degree of precision. When the power supply is energized by ac input, it is very important to maintain a steady voltage level. The input voltage for the test is controlled and conditioned by a UPS followed by a 10% step up/down transformer to stabilize the voltage to 115 V. Another major issue is to minimize the voltage drop across the various connectors in the dc side of the system. Especially for the 5 V, 3.3 V and some 12 V buses can be heavily loaded in the test where the current could be more than 15 A. A current magnitude of this degree may cause significant heating and power loss due to a weak connection. This is why current carrying conductors are properly chosen, and connections are properly made. In addition, voltages are measured by connecting leads to appropriate locations to minimize errors caused by line voltage drops.

The other major issue in measuring the efficiency involves the calibration of the measuring instruments and variations in recorded data in different test conditions. A circuit parameter

TABLE 2.
COMPUTATION OF DERATING FACTORS FOR A CPS WITH MULTIPLE VOLTAGE BUSES AND SUB-GROUPS

Output Voltage	Output Current Rating	Subgroup	Output Loading Current
V_1	I_1	1-2	$DF_T * DF_{S1-2} * I_1 * \frac{X}{100}$
V_2	I_2		$DF_T * DF_{S1-2} * I_2 * \frac{X}{100}$
V_3	I_3	3-4	$DF_T * DF_{S3-4} * I_3 * \frac{X}{100}$
V_4	I_4		$DF_T * DF_{S3-4} * I_4 * \frac{X}{100}$
V_5	I_5	5	$DF_T * DF_{S5} * I_5 * \frac{X}{100}$
V_6	I_6	6	$DF_T * DF_{S6} * I_6 * \frac{X}{100}$

such as a voltage or current generally has a range of values depending on the state of calibration and test condition. This eventually creates a cascaded effect in the test circuit where all small variations in multiple measurement variables could create a significant overall error. Thus, the measured efficiencies vary within a range with best case and worst case situations and some uncertainties exist in the measurement.

The origin of the measurement error and the uncertainty in the measured values greatly depend on the accuracy of the measuring equipments. The error in a voltage measurement is contributed by the reading tolerance and the range tolerance. Thus, the recorded value may be different if the input data range of the device is changed. As an example, when the voltage output of a 12V bus inside a CPS is measured, the meter will display a certain reading when the 20V measuring range is selected in the meter, and the reading may be different if it is measured with a 200V range. The amount of variation depends on the tolerance level involved in the associated range of the device. Because of this tolerance, there will be a maximum and a minimum measured value of any measurement input. Thus,

the maximum value

$$MX = RD \bullet (1 + RDT) + (RG \bullet RGT) \quad (6)$$

and, the minimum value

$$MN = RD \bullet (1 - RDT) - (RG \bullet RGT) \quad (7)$$

Where,

RD = reading of measured value

RDT = reading tolerance

RG = range assigned for the measurement

RGT = range tolerance

The uncertainty level is not a significant factor when only one prime quantity (voltage or current) is measured, and there exists three possible measurement data (RD, MX, MN) for any prime variable. However, when a complex measurement such as power is measured, it will have a range of nine (9) possible values considering three voltage values and three current values exist. Among these values, there will be a maximum power reading and a minimum power reading. The uncertainty level present in this measurement is computed by comparing the actual power reading with the maximum and minimum power values.

The complexity in this computation is elevated when the total power output of the CPS is measured by summing up various subgroup outputs. For an example if the total power is calculated from the 12V bus and 5V bus power levels, it will have eighty one values considering that the 12V power will have nine values and the same for the 5V bus. The number of possible power readings will have an outrageous figure depending on the number of voltage buses in the CPS. To illustrate this, a mathematical computation using three voltage buses is performed, and the various parameters of these buses are shown in Table 3.

TABLE 3
VARIOUS VOLTAGE AND CURRENT TOLERANCES TO ESTIMATE THE MEASUREMENT UNCERTAINTY

V_1	V_1 Tolerance	V_1 Range	Range Tolerance
12	**0.001**	**20**	**0.001**
I_1	I_1 Tolerance	I_1 Range	Range Tolerance
8	**0.002**	**10**	**0.001**
V_2	V_2 Tolerance	V_2 Range	Range Tolerance
5	**0.001**	**20**	**0.001**
I_2	I_2 Tolerance	I_2 Range	Range Tolerance
12	**0.002**	**20**	**0.001**
V_3	V_3 Tolerance	V_3 Range	Range Tolerance
3.3	**0.001**	**20**	**0.001**
I_3	I_3 Tolerance	I_3 Range	Range Tolerance
10	**0.002**	**20**	**0.001**

Equations (6) and (7) were used to measure the maximum and minimum values of each voltage and current magnitudes. As mentioned earlier, there exist nine power values for any voltage bus. When the total power is calculated by adding the three voltage bus powers, a combination of 729 possible values (9•9•9=729) can be found. A MATLAB scrip is written to estimate these values, and a plot is generated that shows the diversity of these values. This plot is shown in Fig. 3.

Fig. 3 reveals some interesting facts regarding the level of uncertainty involved in the measurement of the total power delivered by the 12V, 5V and the 3.3V bus. If there is no

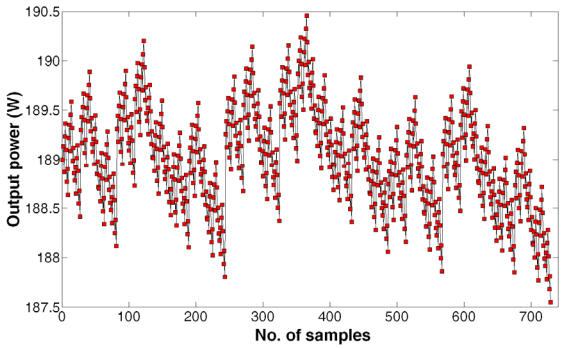


Fig. 3. The various possible values of the total power measured from three voltage buses.

measurement and tolerance errors, the output power should be (V_1•I_1 + V_2•I_2 + V_3•I_3) 189W according to the parameters assigned in Table 3. However, due to the measurement and range tolerances the calculated output power is scattered to create 729 data points around 189W. From the analytical computation, the maximum output power found was 190.46W and the minimum value was 187.55W. Thus the maximum percentage of uncertainty was 0.77% although the maximum equipment tolerance was only 0.2%. The average of these 729 data points is 189, which indicates that the calculation is correct. The standard deviation was only 0.499 meaning most of the data points were around 189W level.

At the beginning of the 80 Plus program an accuracy specification did not exist. Consequently, the focus of the test fixture design was good accuracy with excellent precision. That goal was achieved. Today, now that manufacturers are achieving efficiencies of 90% or better, accuracy of the test fixture is very important with 0.5% suggested as an overall accuracy target. EPRI is in the process of upgrading the test fixture to meet this improved accuracy.

VI. Test Set up

The accuracy of the test results greatly depends on the correctness of the instrument readings and the setup of the test bench. The Yokogawa WT2030 power measurement device used in the test is calibrated once in a year by a certified agency, and all the load banks are calibrated with the Yokogawa 2030 to ensure the repeatability. Other instruments are calibrated periodically with a Fluke/ Yokogawa calibrator and the overall test setup is tested periodically with a reference power supply. The purpose of this overall system testing with a reference power supply is to achieve a consistency in the measurement accuracy that confirms the integrity in the test method. The laboratory test setup is shown in Fig. 4 and the test schematic is shown in Fig. 5.

A 9kVA UPS followed a 10% step up/down transformer is used to provide continuous and conditioned ac input to the CPS under test. Regardless of the ac source type, the THD of the supply voltage when supplying the CPS in the specified mode shall not exceed 2%, up to and including the 13th harmonic (as specified in IEC 62301). The peak value of the test voltage shall be within 1.34 and 1.49 times its RMS value (as specified in IEC 62301) confirming the crest factor to stay within a specified range. The Yokogawa WT2030 power analyzer is used to measure the input voltage, current, power, power factor and output dc voltages. Circuit specialist 3711A and 3710A load banks are used as dc loads at different voltage buses. A Fluke 41 meter with serial interface is used to monitor the current wave shape.

VII. Test Results

Over 750 computer power supplies were tested in EPRI facility over the last five years for 80 PLUS® compliance. Based on the design and price, a CPS (for desktop computer) may produce efficiency as high as 89% at its best operating point. Usually around 50% loading condition takes a CPS to the sweet spot on the efficiency curve, and the efficiency drops at other loading conditions. However, efficiency can be improved even more by paying attention to components whose losses are not dependent on load. For example, losses in the fan, control circuits, and magnetics (transformers and inductors) can be considered as fixed losses, consuming the same amount of power regardless of the amount of output being produced by the power supply. Increasing efficiency of a switched-mode power supply at light load has to focus more on reducing these load-independent losses. In addition, choosing improved switching devices, fast gate drive circuit and superior magnetics will reduce the load dependent losses significantly. Traditionally server power supplies come with most of these enhancements to achieve efficiency figure more than 90%. As a practical example, the loading vs. efficiency relationship of a typical 80 PLUS® desktop power supply (power supply 1) along with a very efficient desktop power supply (power supply 2) are shown in Fig. 6. PS2 achieves 4.5% more efficiency at the sweet spot than PS1.

A very unique error checking methodology is adopted in this test setup that maintains the overall consistency and authenticity of the test results. The test setup is periodically tested with a reference power supply to detect any degradation in connectivity or calibration that is typical over a prolonged

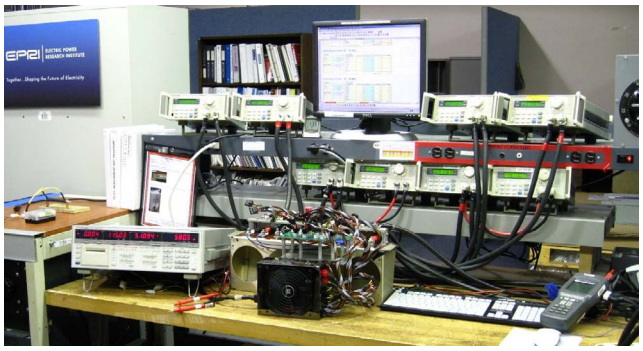


Fig. 4. Actual laboratory test set up of the power supply testing.

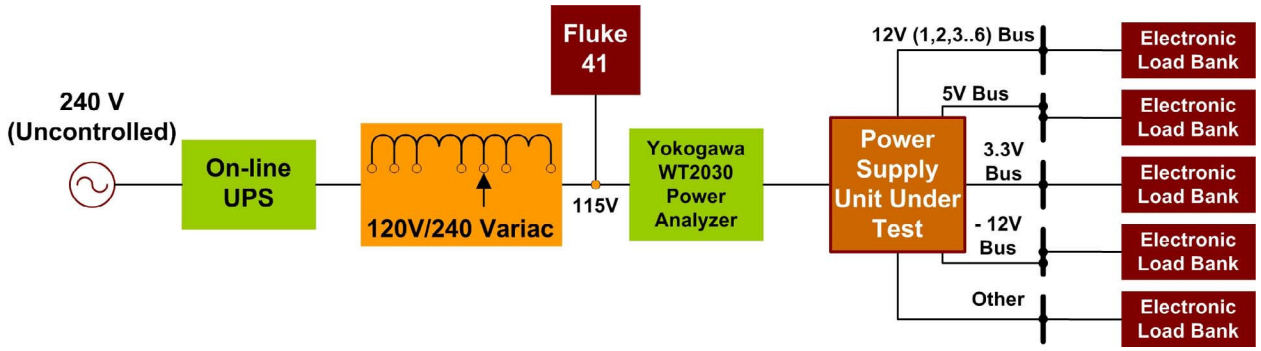


Fig. 5. Schematic of the power supply testing system.

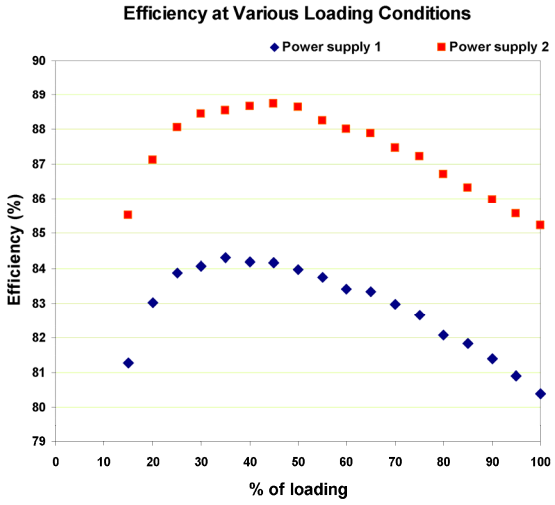


Fig. 6. Efficiencies of two recent CPS at various loading conditions.

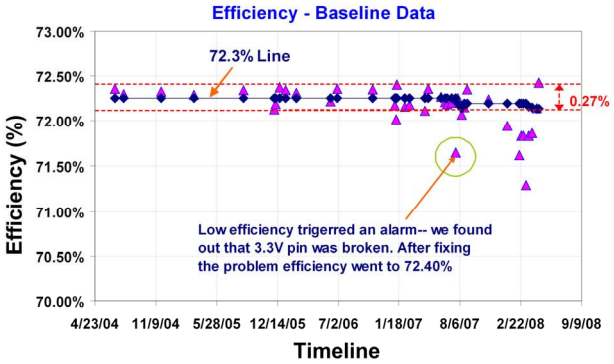


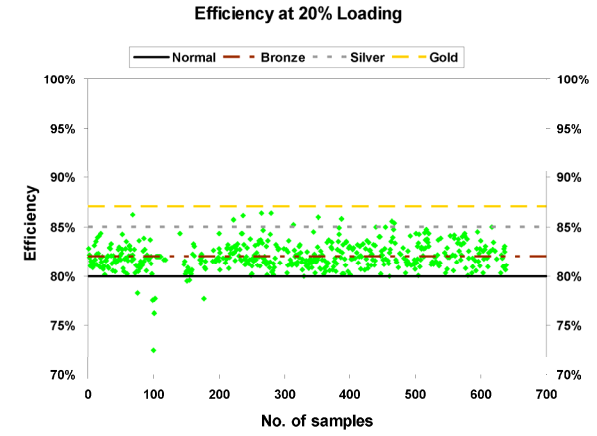
Fig. 7. Efficiency variation of the reference power supply over time. The efficiency stays close to a constant line over time for a precisely controlled test environment.

time duration. This reference power supply should give a steady reading over time if the test setup has proper calibration, and test methods remain consistent. Due to any malfunction with any measurement devices, the recorded data should deviate from the expected value and go beyond a specified range. The test results of the measurement system with the reference power supply as a load are shown in Fig. 7. A bad connection was found that affected the reading by a few percent, and it is shown in this figure. The connection was fixed, and the measured value became consistent again.

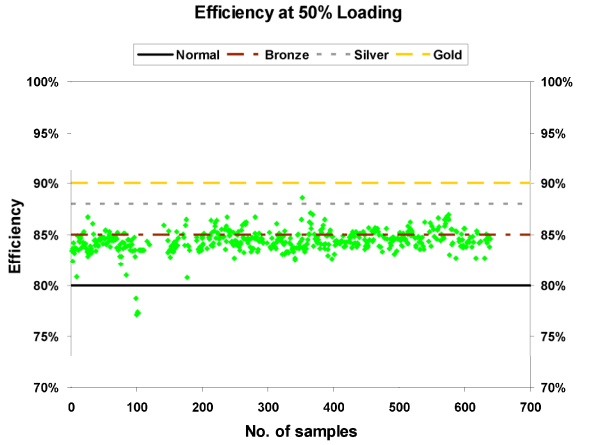
Power supplies manufactured by various vendors greatly vary by power factor, harmonic contents and above all the efficiency. In 2007-2008, over 600 power supplies were tested for efficiency, power factor and input current distortion at 20%, 50% and 100% loading conditions. This is a standardized way to test CPS according to many research agencies. Fig. 8 shows populated efficiencies for those CPSs at different loading conditions. Figure 8(b) shows the efficiency of all these power supplies at 50% loading conditions, and it is prominent that CPSs achieve the highest efficiency at this loading condition compared to 20% and 100% loading. Fig. 9(a) and Fig. 9(b) present the PF and I_{THD} of over 80 power supplies tested in 2008. By virtue of the active PFC circuit, most CPSs offer more than 95% PF at all loading conditions. One prominent trend was observed in both Fig 8(a) and 8(b) that shows that greater power factor is achieved at higher loading (100%) and the input current distortion is the lowest at this loading. One of the power supplies shows 85% THD with more than 90% power factor. This seems to be a measurement error and not consistent with the other measured values.

VIII. Conclusions and Future Work

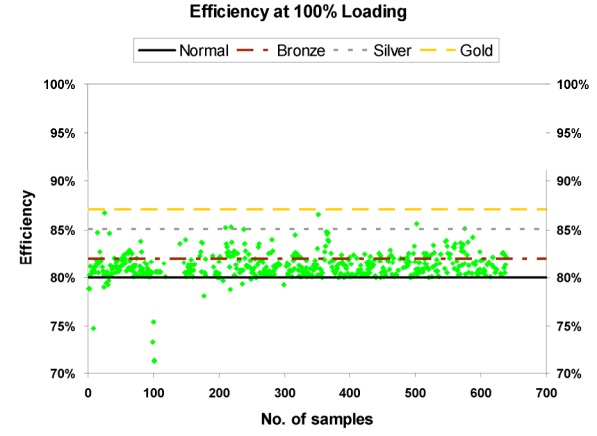
This paper presents the various issues involved in measuring various parameters such as efficiency, power factor and input current distortion of a computer power supply. In addition, the historic power supply efficiency and the measurement technique followed in EPRI has been discussed with experimental data. It was observed that the measurement error increases substantially when the number of voltage buses increases, and the uncertainly level in the measurement could be many times greater than the instrument tolerance. The other key factor observed in these tests is the direct relationship between the percentage of loading and PF or THD. In spite of having active power factor correction circuit, a CPS tends to produce higher harmonics and achieve lower PF at lighter load.



(a)



(b)



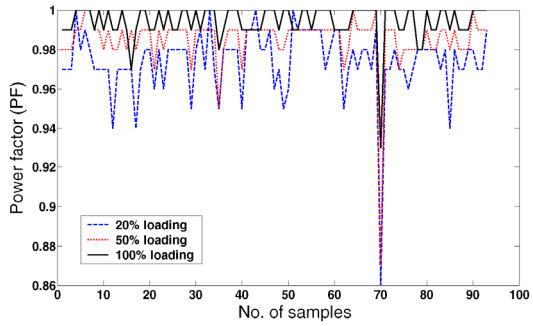
(c)

Fig. 8. Populated efficiencies of over 600 power supplies at (a) 20% loading, (b) 50% loading, (c) 100% loading.

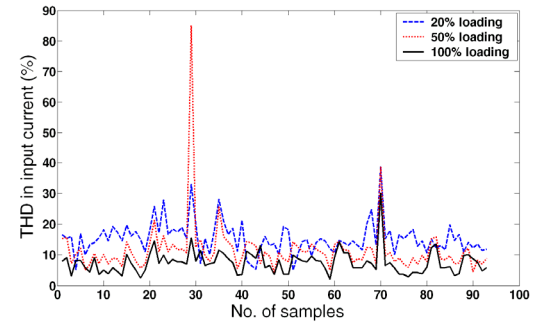
With all the success in the last six years, EPRI is still continuing the research in reducing the existing uncertainty level and improving the accuracy in measuring the efficiency and other parameters of the CPS.

ACKNOWLEDGEMENTS

The authors would like to thank Doug McIlvoy of Power Electronics Strategies (Redmond, OR) and Jason Boehlke of ECOS Consulting (Portland, OR) for their contributions.



(a)



(b)

Fig. 9. Populated data from various power supplies of 2008 at different loading conditions. (a) input power factor, (b) input current harmonics.

REFERENCES

[1] EPRI Solutions Report, "COMPUTER POWER SUPPLIES – EFFICIENCY AND PERFORMANCE EVALUATION TEST REPORT", Sep. 2005.

[2] "Climate Savers Computing Initiative -www.climatesaverscomputing.org", a white paper on smart and efficient computing by Intel and Google. http://www.intel.com/technology/docs/whitepaper_climate-savers-initiative.pdf

[3] U.S. Department of Energy: Energy Information Administration, "Annual Energy Outlook 2006," http://www.eia.doe.gov/oiaf/aeo/overview.html#consumption .

[4] www.EfficientPowerSupplies.org

[5] B. Fortenbery, P. M-Ostendorp and C. Calwell, "The Efficiency of Internal Power Supplies: Test Procedure and Policy Developments", APEC 2006,

[6] "ENERGY STAR® Program Requirements for Computers: Version 4.0", http://www.energystar.gov/ia/partners/product_specs/program_reqs/Computer_Spec_Final.pdf

[7] Internal and External Power Supply Test Methods: http://www.efficientpowersupplies.org/methods.asp

[8] P. Ostendorp, K. Herb and C. Calwell, "In Search of Synergy - The role of benchmarking in measuring and enhancing computer efficiency", ISEE 2006

[9] K. Herb, P. M-Ostendorp, C. Calwell and R. Duff, "Lean, Green, and Solid State: Measuring and Enhancing Computer Efficiency", ACEEE, 2006

[10] http://efficientpowersupplies.epri.com/pages/Latest_Protocol/Generalized_Internal_Power_Supply_Efficiency_Test_Protocol_R6.2.pdf

[11] www.80PLUS.org

[12] M. T. Zhang, M. M. Jovanovic´, and F.C. Y. Lee, "Analysis and Evaluation of Interleaving Techniques in Forward Converters," IEEE Transactions on Power Electronics, vol. 13, no. 4, pp. 690-698, July 1998.

[13] http://www.formfactors.org/developer/specs/PSU_DG_1_0.pdf

[14] A, Mansoor, B. Fortenbery, B. Vairamohan, T. Geist, P. M-Ostendorp, C. Calwell, and R. Rasmussen, "Generalized Test Protocol for Calculating the Energy Efficiency of Internal Ac-Dc Power Supplies Revision 6.3" May 2008.