A Three-Dimensional Architecture for a Parallel Processing Photosensing Array

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Abstract—**A three-dimensional architecture for a photosensing array has been developed. This silicon based architecture consists of a 10 × 10 array of photosensors with 80 μm diameter, through chip interconnects to the back side of a 500 μm thick silicon wafer. Each photosensor consists of a 300 × 300 μm pn-junction photodiode. The following processes were used to create this photosensing architecture: 1) thermomigration of aluminum pads through an n-type silicon wafer; 2) creation of pn-junction photosensors on one side of the wafer; and 3) creation of aluminum pad ohmic contacts to the thermomigrated, through chip interconnects and the substrate on the back side of the wafer. The electrical and optical characteristics of the three-dimensional architecture indicates that it should be well suited as a photosensing framework around which a "silicon retina" could be built.**

Introduction

THE value of parallel processing has become increasingly apparent in the past years as the need for speed and more complex signal processing has increased. Parallel architectures are commonly used to increase the throughput of a circuit and the speed of computations. While most parallel processes implemented in hardware today use the well developed silicon planar technology, the complexity of the parallelism suggests that other technologies should be investigated. This has led to the development of three-dimensional architectures using amorphous silicon [1], [2], laser-recrystallization technology [3], and other architectures using interconnects both through and between silicon wafers [4].

A typical application of these three dimensional architectures is in data acquisition and signal processing from sensor arrays. Specifically, a two-dimensional array of sensors often requires multiplexing and/or signal processing circuitry which controls or selects the sensors and this circuitry can occupy a significant portion of the total surface area of the chip. If a three-dimensional architecture could be used to move the multiplexing and/or signal processing circuitry away from the sensors, the sensors could be made larger and sensor sensitivity could be increased without decreasing the density of the sensor array. The development of a three-dimensional architecture could have greater impact on monolithic systems containing more complex multiplexing or signal processing circuitry, where the sensitivity could be substantially increased for the same density of sensors. One such three-dimensional architecture involves fabrication of the sensors on one surface of a silicon die and fabrication of the multiplexing and/or processing circuitry on the other side of the silicon die, with through-the-die interconnects connecting the sensors in the array with the processing circuitry.

Potential applications of three-dimensional data acquisition architectures are in the area of chemical or neurophysiological sensing where the sensors need to be both electrically and chemically isolated from the signal processing circuitry [3], [5]. An area where a three-dimensional architecture could have a substantial benefit is in "smart" photosensor arrays. A silicon retina, which includes extensive real-time signal processing, is an example of such a smart two dimensional photosensor array [6]–[8]. Extensive signal processing is necessary to mimic such functions as real-time spatial and temporal filtering of optical signals transduced by an array of high sensitivity photosensors. When additional retinal functions are implemented on these smart photosensing arrays, the required signal processing circuitry will be even more complex and occupy even more silicon area. If these functions are to be realized using a two-dimensional architecture, there will be an obvious tradeoff between photosensor sensitivity and the complex signal processing circuitry. Intelligent photosensor chips, using a two-dimensional architecture, have been developed to perform some of the processing on the sensor chip and some of the digital signal processing off chip [9]. A foveated, retina-like sensor using CCD technology has also been developed [10]. Both approaches are novel; however, as the functionality and parallelism is increased it can be advantageous to use a three dimensional architecture. The use of a three-dimensional architecture in the creation of a silicon retina, with sensors and signal processing circuitry fabricated on different planes in a laminar structure will eliminate the tradeoff between sensitivity and circuitry complexity, since the sensors and the signal processing circuitry will not compete for the same silicon surface area.

As a first step towards the creation of such a three-dimensional silicon retina, we have developed a three-di-

Manuscript received January 23, 1992; revised May 29, 1992. This work was supported by the William H. and Mattie Wattis Harris Foundation.

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IEEE Log Number 9204054.

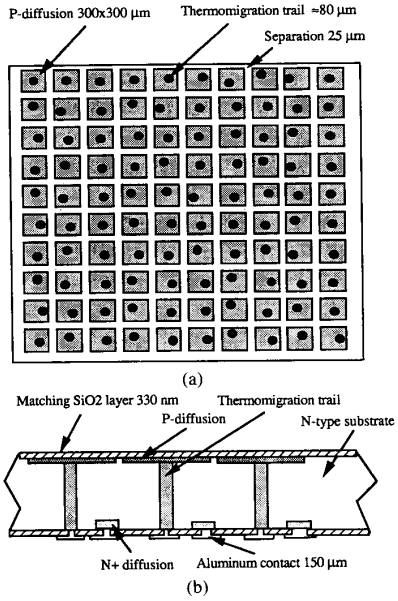

Fig. 1. A three-dimensional architecture for a parallel processing photosensing array. Top view (a) and side view (b).

mensional architecture for a parallel processing photosensing array, a 10 × 10 array of photodiodes that fully occupy one surface of a silicon die. The output of each sensor is transmitted directly through the silicon die to its rear surface where a 10 × 10 array of bonding pads has been formed. These bonding pads form the first generation output structure of the photosensing array. This paper describes how the architecture has been built and quantifies the characteristics of the system.

The Architecture of the Three-Dimensional Photosensing Array

The three-dimensional architecture for a parallel processing photosensing array consists of a 10 × 10 array of photodiodes with interconnects through the wafer as shown in Fig. 1. The photodiodes are pn-junction silicon photodiodes formed by boron diffusion into the n-type silicon substrate. Each of the one hundred photodiodes has a dimension of 300 × 300 μm and is separated from its neighboring photodiodes by 25 μm. The photosensing side with the pn-junctions is referred to as the "front side" of the die. The interconnects between the front side and the back side are thermomigrated trails made using the temperature gradient zone melting process (TGZMP) developed by Anthony and Cline [11]–[13]. This is a high-temperature process where a thermal gradient is produced across the silicon wafer, causing aluminum, deposited on the surface of the wafer, to migrate through the wafer as an Al–Si alloy droplet. As the droplet moves through the wafer, it leaves behind a highly conductive trail of p-doped silicon. Each thermomigration trail has an average diameter of 80 μm. Aluminum square pads, 150 μm on a side, make contact to the p-doped trails which emerge from the silicon die. The side of the wafer containing the aluminum contact pad is referred to as the "back side" of the wafer. Thus, the highly conductive p-type thermomigrated trails connect the photodiodes to the aluminum contacts on the back side of the die. An additional set of aluminum pads on the back side of the wafer make a low resistance ohmic contact to the n^+-doped silicon substrate.

Since this is a double-sided semiconductor process, cleanliness of both the front and back side of the wafer was essential. Single-sided photolithography does not protect the back side of the wafer while processing the front side and vice versa. Therefore, a "double-sided photolithographic process" was developed to protect the side of the die that was not being processed.

Methods of Preparation

Sample Preparation

Single-crystal, 3 in diam ⟨100⟩ silicon wafers were used for the fabrication of the three-dimensional photosensing arrays. These were 10 Ω-cm n-type phosphorus doped wafers and were 1900 μm thick with only one side polished. After a hydrogen peroxide based wafer cleaning procedure [14], approximately 3 μm of aluminum was evaporated onto the silicon wafer. Positive photolithography was used to form 24 arrays, each of which contained a matrix of 10 × 10 aluminum squares. The aluminum squares were 100 μm on a side and were placed with their centers 325 μm apart. A dicing saw with a 50 μm wide blade was then used to scribe indexing marks into the silicon surface for subsequent aligning of the masks used during the double-sided silicon photolithographic processes.

Thermomigration

The temperature gradient zone melting process (TGZMP) was used to form the interconnects between the front and back sides of the wafer. The TGZMP is a process in which a liquid zone in the form of a sheet, rod or droplet migrates through a solid under the driving force of a temperature gradient. Since aluminum is a p-type dopant, the remaining trails are highly conductive p^+ silicon. The TGZMP apparatus and procedure we used to create these structures is described elsewhere [15].

Wafer Polishing

After the thermomigration, the 3 in wafer was cut on a dicing saw into six squares with dimensions of approximately 20 × 20 mm. Each of the six silicon wafers contained four 10 × 10 arrays of aluminum trails. The thermomigration process damaged both sides of the wafer. At the entry side of the silicon dice, aluminum oxide and residues of the aluminum were left not only above the surface but also below the surface and therefore this surface had to be repolished. The exit sides of the aluminum also tended to "smear out" considerably after it com-

pletely migrated through the wafer. Thus, the dice were ground down from the exit side to a thickness of approximately 500 μm before they were polished. Both sides of the wafers were then polished removing approximately 30 μm on each side, starting with a 30 μm diamond compound on a polishing wheel and continuing with compound sizes of 15, 6, 1, and $\frac{1}{4}$ μm. After the polishing, the silicon dice had a double sided polish and contained a matrix of p-trails through the n-type substrate. Before subsequent oxidation processes and the diffusion processes the wafers were put through a series of cleaning steps a second time to remove any metals, organic compounds or other contaminates.

Photodiode Processing

The 300 × 300 μm p-doped regions on the front side of the wafer were formed next. A layer of SiO_2 was thermally grown at 1000°C on the silicon wafers first in a dry oxygen atmosphere for 10 min followed by a wet oxidation for 70 min. This yielded a 380 nm layer of SiO_2.

Since the creation of the photosensor array is a two-sided process, a double-sided photolithograpic process was developed. Cleanliness of both the front and back sides was essential during the double-sided photolithographic processes. In order to protect the side of the silicon wafer that was not being processed during the photolithography, a special holder, machined from polyethylene, kept one side of the wafer clean except for the very outer edges. The photoresist was spun on and cured in an oven at 130°C for 30 min. This photoresist protected the back side of the silicon die from scratches and contaminates during the photolithographic process. The holder was used one more time when photoresist was spun on the other side of the wafer. The silicon wafer was then processed with conventional single sided photolithographic steps.

After the photolithography, the silicon wafer was coated with a layer of spin-on dopant (boron atom concentration of 10^{21} cm^{-3}) on the front side of the wafer to form the photodiodes. This was given a drive-in treatment at 992°C for 15 min to form pn-junction photodiodes with a junction depth calculated to be 0.25 μm. The 300 × 300 μm square boron diffused p-region areas were aligned over the p-type thermomigration trails to ensure that the trails contacted the p-regions. The doped spin-on glass was removed from the die and another silicon oxidation was performed for the next process step. The same steps in the photolithographic process were applied as before, but now the photosensing side of the wafer was protected with a layer of hard-baked photoresist. To make low resistance ohmic contacts to selected sides on the silicon substrate, a spin-on phosphorus dopant glass was used as a source to create heavily doped n^+ contact regions. The spin on dopant was given a drive-in treatment at 1000°C for 15 min to form a high-low doping transition at a depth calculated to be 0.8 μm. All the SiO_2 was removed and a new layer of SiO_2 was thermally grown at 1000°C first in a dry oxygen atmosphere for 5 min followed by a wet oxidation for 55 min, resulting in a 330 nm layer of SiO_2. This was done to produce a second order, $\frac{1}{4}$-wave matching layer for the photons striking the photosensing side of the wafer and as a masking layer on the opposite side of the wafer. Again, "double side" photolithography was performed to etch the holes in the SiO_2 for contacts to the p-trails and to the phosphorus doped substrate. A 8000 Å layer of aluminum was evaporated onto the wafer and patterned to have square, 150 μm contact pads. Aluminum alloy was formed at 425°C for 30 min in hydrogen and nitrogen ambient.

Experimental Results

Yield

Out of the sixteen 10 × 10 arrays of photosensors that survived the manufacturing processes, 98% of the thermomigration trails made contact to the p-diffusion regions. Two percent of the thermomigration trails failed to contact the photosensor p-region due to the random walk nature of the TGZMP process. In this particular application, random walk, a well-known phenomena in the thermomigration process [15], [16] was not a major concern as long as the trails migrated sideways less than 150 μm. If the TGZMP trail deviated more than 150 μm from the center, it made contact to a neighboring p-region. It is also possible for the trail to make contact to two neighboring p-diffusion regions if the center of the trail exits the silicon wafer between two p-diffusion regions and makes contact to both regions. Thus, the random walk had to be limited to a deviation of 150 μm from the center to achieve a 100% yield. The random walk of the trails can be seen in Fig. 2. Detailed results of the TGZMP process are presented in a separate paper [15].

PN-Junction Characteristics

The pn-junction characteristics depend both upon the quality of the pn-junction of the p-doped TGZMP trail and the spin-on boron dopant. Approximately half of the total pn-junction area was formed by the thermomigration process and half by the diffusion and drive-in treatment of the boron-dopant spin-on glass.

The current-voltage characteristics of these junctions were measured with an HP4145 analyzer. The forward biased characteristics for currents ranging from 100 pA to 1 mA are shown in Fig. 3 and show an approximately logarithmic dependence of current upon forward bias voltages over about 5 log units. Deviations from the log is due to a series resistance or a high level injection of carriers.

The current in the pn-junction for different reverse bias voltages, shown in Fig. 4, is a generation current in the pn-junction which increases as the voltage across the reverse biased junction increases. The dark current increases linearity with the reverse biased voltage across the junction from 0 pA (with zero bias) to 1.9 nA (at 5 V) due to the increase in generation current. Since the di-

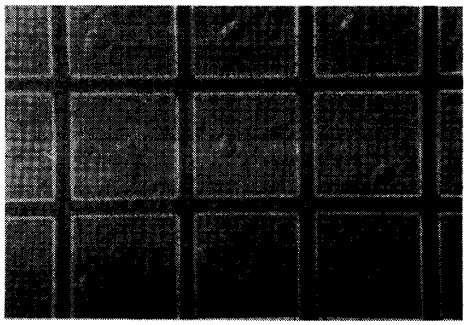

Fig. 2. Nine pixels out of the 10 × 10 array of photosensors. The circular objects are the thermomigrated trails that make contact with the p-diffusion photosensor regions. The random walk of the thermomigration trails can be observed. Each photodiode is 300 μm on a side.

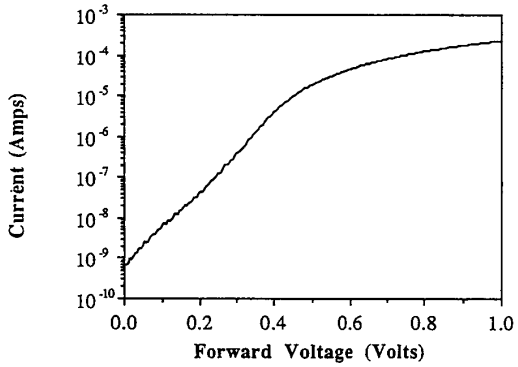

Fig. 3. Forward bias characteristics of a typical pn-junction at different voltages. The forward bias characteristics show an approximately logarithmic relation between current and forward bias voltages across the pn-junction over about 5 log units.

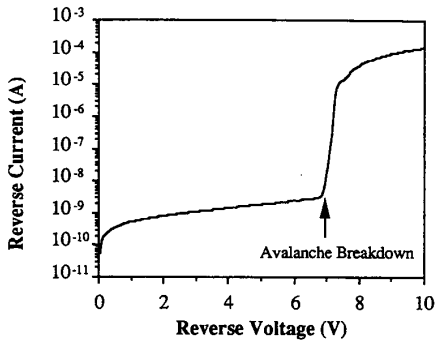

Fig. 4. Reverse bias characteristics of a typical pn-junction. The reverse bias characteristics show a linear relation between current and reverse bias voltage across the pn-junction over about 7 V.

ameter of the circular shaped thermomigration trail varies at different depths in the silicon die, only an estimate of the leakage current per μm^2 can be made. Calculations based on average thermomigration trail diameter of 80 μm results in a leakage current of 1.1×10^{-6} A/cm^2 at 5 V. The relatively high leakage current and ideality factor (n = 1.65, Fig. 3) is due to the high recombination rate in the depletion region around the thermomigrated column.

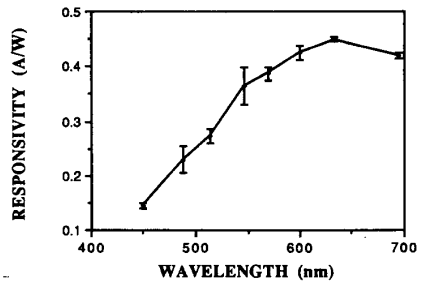

Fig. 5. Spectral sensitivity of the photodiodes in the visual spectrum. The photosensors have a peak responsivity of 0.45 A/W at approximately 650 nm. The error bars show the standard deviation of the measurements in ten photodiodes.

The reverse breakdown voltage of the pn-junctions varied from 7 to 10 V with an average break down voltage of 8.5 V. The low avalanche breakdown voltage is due to the very shallow p-diffused photosensor region.

Optical Characteristics

The optical characteristics were determined over the visual spectrum with eight different interference filters (Edmond Scientific). The photodiode current was measured using a current-to-voltage amplifier. The responsivity of the zero biased photosensors in the visual spectrum is shown in Fig. 5. The responsivity reached a peak of 0.45 A/W at approximately 650 nm. The responsivity of a photodiode without a thermomigrated trail would be higher because of a larger depletion volume. The peaking of responsivity at this low wavelength is mainly due to the shallow depth of the pn-junction and to the added 330 nm thick layer of SiO_2. The SiO_2 layer on the photosensors acts like an antireflection coating to improve the performance of the photodiodes. The $\frac{1}{4}$ wave, second harmonic matching layer of SiO_2 increases the sensitivity in the visual spectrum with an anti-reflection maximum at 610 nm.

The responsivity is expected to increase a few percent with the photodiode back biased, since the width of the pn-junction depletion region increases. The reverse biased peak responsivity was 0.49 A/W at reverse biased voltage of 5 V compared to 0.45 A/W for a zero biased junction, a 9% increase in responsivity for a reverse biased pn-junction.

Blooming

Photons absorbed in one sensor can inject current into an adjacent sensor. This undesired current injection is known as blooming and is a potential problem in many photosensor arrays. A potential barrier in the form of an n^+ doping region between the neighboring sensors is often used to minimize blooming.

Blooming was measured by connecting two adjacent photodiodes as a pnp transistor and sending current through the base emitter junction. A transistor gain (beta) of 1/10 000 was measured with an I–V curve tracer. This

indicates that the photosensors are disconnected due to the large distance between them and/or the short carrier lifetime in the n-type substrate. Photodiodes not adjacent to the sites of current injection showed no measurable blooming (a beta of less than 10^{-6}).

Discussion

We have shown that a three dimensional architecture of photodiodes and cross wafer interconnects results in a parallel processing photosensing array of relatively high quality. Before this architecture can be used in a silicon retina application, three important issues need further consideration. The first is the reduction of the dimensions of the photosensors. There are three major factors that limit the dimensions of the structures used in this device; the size of through chip interconnects which can be thermomigrated through the wafer, the warping of the wafer when the thermomigration occurs at high temperatures, and the random walk of the thermomigration columns. Thermomigration columns as small as 100 μm have been reported [3] and we have occasionally thermomigrated columns as small as 15 μm through the wafer. However, this was achieved at such a high temperature and with such an uneven temperature distribution across the wafer, that a warping of the silicon wafer was often produced. Such warped wafers can not be used for further processing. The problem of warping of the silicon wafer and the thermomigration process is discussed further in a separate paper [15]. The random walk which occurs in the thermomigration process is a well known phenomena [16] and Anthony and Cline have reported ways to reduce the problem. However, because of the relatively large size of the photodiode "targets" used in this array, random walk was not a significant problem. Smaller photodiode targets will require greater control over the random walk problem.

The second important issue that must be addressed is the complexity of the photosensor signal processing circuitry on the back side of the silicon die. The possibility of putting multiplexing circuitry and/or signal processing circuitry on the back side of the sensor array is a question of processing techniques. The cleanliness of both surfaces while processing will be essential. Basically, the same process techniques described herein can be used to fabricate transistors on the back side; however, the polishing of the wafer surfaces has to be improved with a chemical polishing step to achieve high quality transistors. Instead of fabricating circuitry on the back side of the silicon die, another die containing signal processing circuitry can be mounted using solder bump technology to the three dimensional architecture photosensing die, Fig. 6 [17]. This approach may be more cost and process effective.

Third, the benefits accruing from a three dimensional structure may not justify the added manufacturing complexity. The increase in performance associated with the use of the three dimensional architecture will vary with the size and design of the signal processing circuitry and the size of the photosensors. Three main design criteria have to be considered; signal-to-noise ratio (S/N), sensitivity and density of sensors.

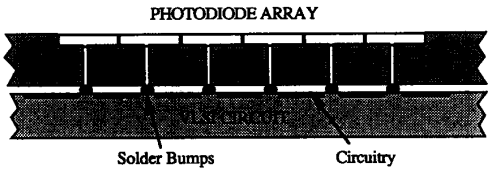

Fig. 6. The three-dimensional architecture photosensing die and a silicon die containing signal processing circuitry are connected using solder bump technology.

The signal-to-noise ratio is degraded by going from a 2-D to the three dimensional architecture described in the paper because of the extra dark current associated with the thermomigration trails to the back side of the silicon die. However, the S/N degradation is minimized as the size of the thermomigration trails are reduced. If the increase in dark current due to the thermomigration trails does not limit or significantly degrade the performance of the signal processing circuitry, the performance of the three dimensional parallel architecture can be beneficial.

On the other hand, the sensitivity of the sensor can be improved with the three-dimensional architecture because the signal processing circuitry can be removed from the plane of the sensors. This allows an enlargement of the photosensor area and increases the number of photons which can be absorbed by the photosensors. The increase in sensitivity which can be realized by the three-dimensional architecture is therefore a function of the ratio of photosensitive area and signal processing circuitry area. The more complex the signal processing circuitry, the more the sensitivity can be improved by moving the circuitry to the back side of the array.

The density of the array of sensors can also be improved with a three-dimensional architecture. The size of the thermomigration trail and the size of the circuitry sets limits on the improvement of the density of the sensor array. Since the size of the thermomigration trails can be relatively large in comparison to the size of the pixels, the density of the sensors is in many cases limited by the size of the thermomigration trail. The other limitation to the density of the pixels is the size of the signal processing circuitry associated with each pixel. For large numbers of photosensors, the silicon area of each photosensor should be equal to the area of the signal processing circuitry on the back side of the array. Thus, the size of this circuitry will generally set a limit on the photosensor density.

Our main interest in developing the three-dimensional photosensing array described herein is that it will provide a functional foundation for a silicon retina. Different signal processing circuits have already been developed to mimic the functions in the retina. Important preprocessing functions produced by the human retina are spatial and temporal filtering as well as gain control by the photoreceptors themselves. First, generation silicon retinas contained analog signal processing circuitry with most of the silicon real estate occupied by the processing circuitry [8].

Later versions have improved the ratio of photosensitive area to circuit area [6], but as more of the functionality of the human retina is implemented in the signal processing circuitry, the ratio of sensor area to circuitry area, and photosensitivity must decrease [7]. A three-dimensional silicon retina with sensors and signal processing circuitry fabricated on different planes in a laminar structure will eliminate this tradeoff, since the sensors and the signal processing circuitry will not compete for the same real estate. Thus, such a three-dimensional silicon architecture with its retinal signal processing will not only mimic some of the functions of the human retina but it will achieve this function using a laminar architecture similar to that of the retina.

ACKNOWLEDGMENT

The authors wish to thank D. Petelenz for many useful discussions and L. Sadwick for his help with some of the measurements.

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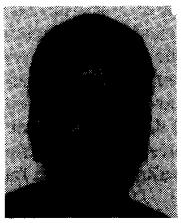

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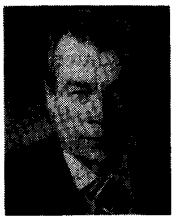

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