Design and Testing of an Integrated Circuit for Multi-Electrode Neural Recording

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Abstract

We have developed a single-chip neural recording system with wireless power delivery and telemetry. The 0.5-µm CMOS IC is designed to be bonded to the back of a 100-channel Utah Electrode Array. A pad near each amplifier allows connection of the chip to the MEMS electrode array. The complete Integrated Neural Interface will receive power wirelessly through a 2.64-MHz inductive link. A clock, regulated supply, and commands are derived from the power signal .The neural amplifiers each have a gain of 60 dB. A 10-bit charge-redistribution ADC is used to digitize the signal from one amplifier selected with an analog MUX. Digitizing all channels simultaneously would generate prohibitively high data rates; therefore, we perform data reduction by incorporating one-bit "spike detectors" into each amplifier. Neural data is transmitted off chip using an -integrated 433-MHz FSK transmitter. The chip measures 4.7×5.9 mm^2 and consumes 13.5 mW of power.

1. Introduction

In the past decade, neuroscientists and clinicians have begun to use implantable MEMS multielectrode arrays (e.g., [1]) to observe the simultaneous activity of many neurons in the brain. By observing the action potentials, or "spikes," of many neurons in a localized region of the brain it is possible to gather enough information to predict hand trajectories in real time during reaching tasks [2]. Recent experiments have shown that it is possible to develop neuroprosthetic devices – machines controlled directly by thoughts – for disabled humans if the activity of multiple neurons can be observed [3].

Currently, data is recorded from implanted multielectrode arrays using bundles of fine wires and head-mounted connectors; all electronics for amplification and recording is external to the body. This presents three major barriers to the development of practical neuroprosthetic devices: (1) the transcutaneous connector provides a path for infection, (2) external noise and interfering signals easily couple to the wires conveying weak neural signals (<500 µV) from high-impedance electrodes (>100 kΩ), and (3) the connector and external electronics are typically large and bulky compared to the ~5 mm electrode arrays. To eliminate these problems, data from the implanted electrodes should be transmitted out of the body wirelessly. This requires electronics at the recording site to amplify, condition, and digitize the neural signals from each electrode. These circuits must be powered wirelessly since rechargeable batteries are relatively large and have limited lifetimes. Low power operation is essential for any implanted electronics as elevated temperatures can kill neurons.

We are developing a wireless, fully-implantable neural recording system to facilitate neuroscience research and neuroprosthetic applications (see Fig. 1). The system is based on the Utah Microelectrode Array (UEA), a 10 × 10 array of platinum-tipped silicon extracellular electrodes [1]. This paper describes the development of a mixed-signal integrated circuit that will be flip-chip bonded to the back of the UEA using Au/Sn reflow soldering. This chip will directly connect to all 100 electrodes, amplify the neural signals from each electrode, digitize this data, and transmit it over an RF link (see Fig. 2). Power will be delivered to a 5-mm coil mounted on the back of the

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chip using an inductive link. (This coil is under development; the chip is currently tested using dc power for initial tests and a 19-mm coil for wireless tests.) The entire device will be coated in parylene and silicon carbide to protect it from body fluids.

2. System and circuit design

The integrated circuit, first presented in [4], measures 4.7×5.9 mm^2 and was fabricated in a commercial 0.5-µm 3M2P CMOS process (see Fig. 3). An on-chip bridge rectifier and bandgap-referenced low-dropout voltage regulator provide a 3.3 V dc power supply from a 2.64-MHz ac coil power signal. External capacitors are used to resonate with the power coil and smooth the unregulated dc supply. A system clock is recovered from the coil frequency, and ASK modulation of the power signal allows the external user to send commands and configuration data to the chip at 6.5 kbps [5]. (See [6] for a similar power link.)

Data is encoded using an amplitude modulation scheme where short-duration pulses of increased amplitude encode a zero and long-duration pulses of increased amplitude encode a one. Fig. 4(a) shows the voltage at one terminal of the power receive coil during amplitude modulation of the transmitted power signal. An on-chip envelope detector circuit tracks the amplitude of the coil voltage [see Fig. 4(b)]. A low-pass filter calculates a running average of the envelope, and a comparator determines if the instantaneous output of the envelope detector is higher or lower than the long-term running average. The comparator produces a binary signal [see Fig. 4(c)], but this signal may contain glitches at the low-to-high and high-to-low transitions.

A finite state machine (FSM) on the chip implements a robust algorithm for recovering this binary command data in the presence of glitches. The FSM first waits for a low-to-high transition. When this occurs, a timer starts counting. When the timer reaches a specified time (97 µs in our circuit), the binary data stream is sampled. A pulse longer than 97 µs in duration will be sampled as a one; a pulse shorter than 97 µs in duration will be sampled as a zero. Fig. 4(d) shows the sample signal generated by the FSM. After a falling edge is detected, a second timer is triggered. This timer freezes the FSM for an additional 12 µs before allowing it to return to its initial state and wait for the next low-to-high transition. This waiting period lasts beyond any low-to-high transitions caused by glitches on the falling edge of the pulse and prevents these glitches from falsely retriggering the circuit.

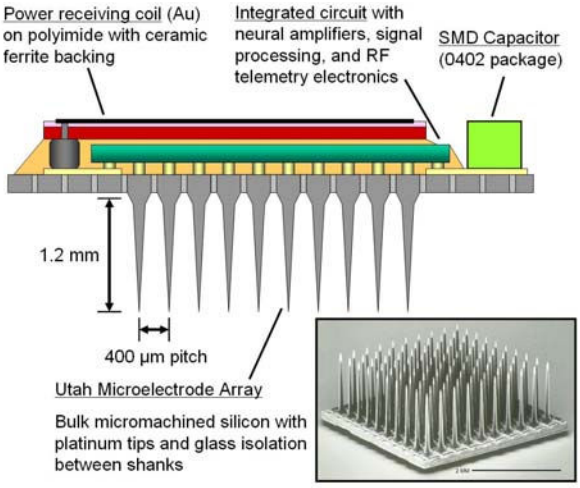

Figure 1. Complete Integrated Neural Interface (INI) assembly concept. Inset shows Utah Microelectrode Array (UEA).

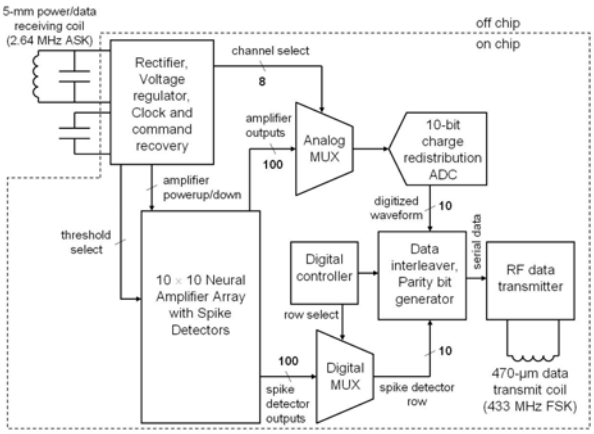

Fig. 2. Integrated Neural Interface (INI) system block diagram.

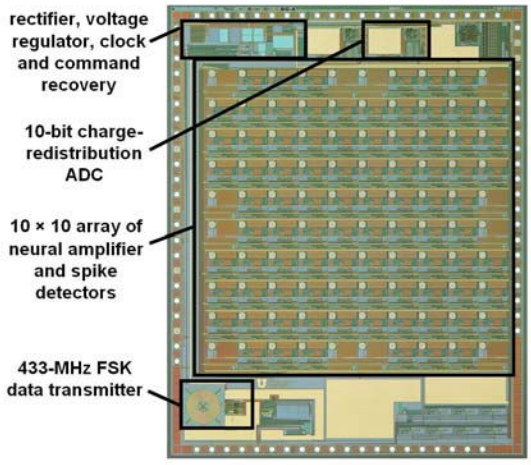

Fig. 3. Die photo of 4.7 mm × 5.9 mm integrated neural interface chip (INI2).

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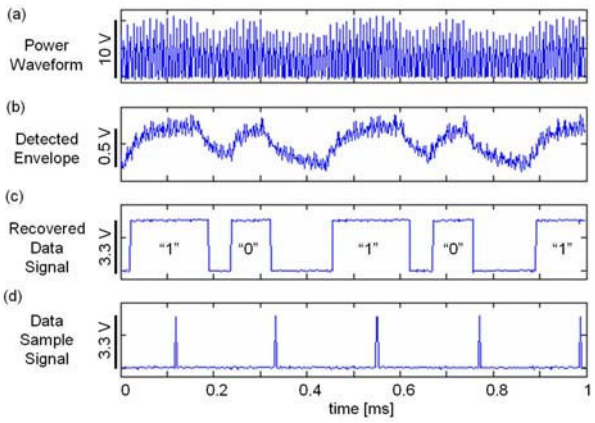

Fig. 4. Command recovery from ASK power waveform. (a) Power waveform at power receive coil. (b) Signal from envelope detector. (c) Binarized amplitude. (d) Sample signal to distinguish short pulses from long pulses.

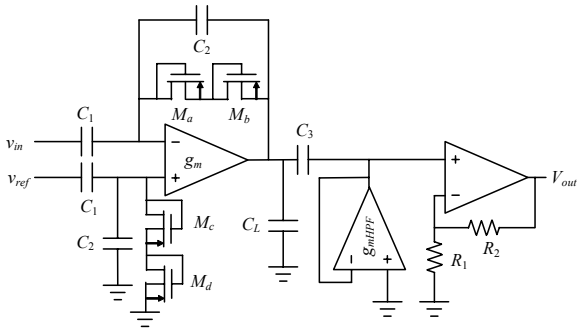

Fig. 5. Schematic of neural signal amplifier. A 40-dB front-end amplifier is followed by a g_m-C high-pass filter and finally a 20-dB gain stage.

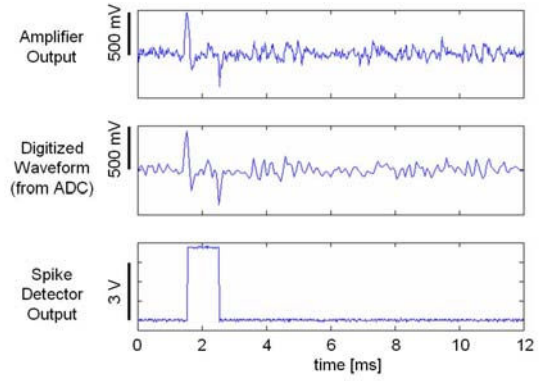

Fig. 6. Response of wireless-powered chip to neural waveform played from waveform generator: analog output of a neural signal amplifier (top), waveform reconstructed from ADC output (middle), output of corresponding spike detector (bottom). Data was taken while chip was powered wirelessly.

The center of the chip consists of a 10 × 10 array of amplifiers laid out in a 400 μm pitch, corresponding to the inter-electrode spacing. A bond pad local to each amplifier allows direct connection of the chip to the UEA. Twelve of the 100 platinum-tipped electrodes are used as "ground" or "reference" electrodes; the remaining 88 electrodes are connected to integrated low-noise neural signal amplifiers. The amplifiers are ac-coupled to eliminate the large dc offset found at the electrode-tissue interface; their bandwidth extends from 1-5 kHz to pass neural spikes and reject low-frequency local field potentials (see Fig. 5). The amplifiers have a measured gain of 60 dB and input-referred noise of 5.1 μVrms. Each amplifier draws only 12.8 μA of supply current; we use the design techniques presented in [7] to minimize noise and power consumption. Individual amplifiers may be powered down with a command signal so that unused electrode channels do not dissipate power.

A 10-bit charge-redistribution ADC is used to digitize the signal from one amplifier at 15 kSamples/s. The ADC consumes less than 30 μA, and has measured INL and DNL <0.8 LSB for all but the lowest 50 codes. Digitizing all 88 neural waveforms simultaneously would generate prohibitively high data rates (>10 Mbps) for low-power RF transmission. Therefore, we perform on-site data reduction by incorporating one-bit "spike detector" comparators into each amplifier block.

The spike detection threshold is set by a 7-bit DAC. The user selects the detection threshold level and also controls an analog MUX that routes the desired electrode amplifier signal to the ADC. The chip produces a 330 kbps data stream that interleaves ADC data from one selected amplifier, spike detector data from all amplifiers, and parity bits. Fig. 6 shows recorded neural data (courtesy of K. Shenoy, Stanford University) played through a neural amplifier on the chip; either the complete digitized waveform or simply the detected spikes may be transmitted. The format of a data frame is illustrated in Fig. 7. (An alternate approach to neural data reduction is presented in [8].)

Digitized neural data is transmitted using a fully-integrated 433-MHz FSK transmitter (see Fig. 8). The VCO uses a planar spiral inductor (54 nH, $Q \approx 3$) optimized for maximum LC parallel-circuit equivalent resistance to minimize power consumption [9] (see Fig. 9). The inductor also serves as a transmitting antenna. At an operating supply current of 1.9 mA, we are able to receive FSK-modulated data (at -86 dBm) at a distance of 13 cm using a half-wave resonant dipole antenna (see Fig. 10).

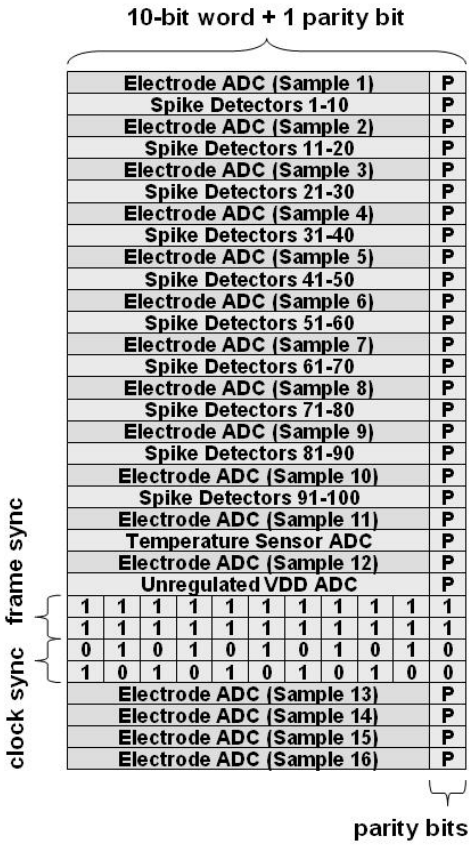

Fig. 7. Single 352-bit data frame of interleaved ADC and spike detector data used for FSK transmission.

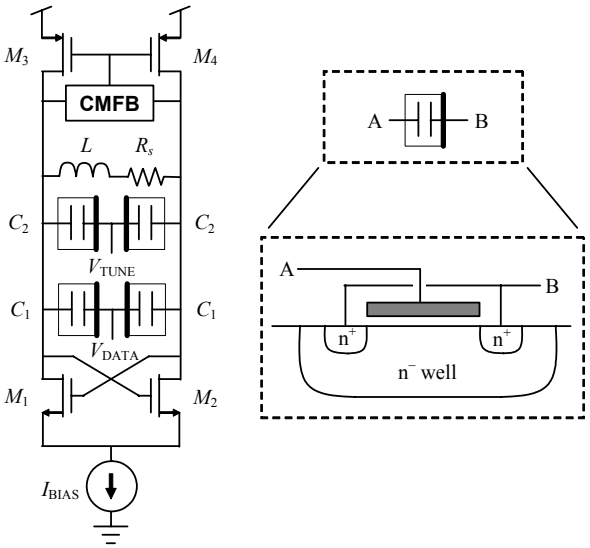

Fig. 8. Schematic of VCO used for FSK transmission. Accumulation-mode varactors are used to vary the frequency of oscillation.

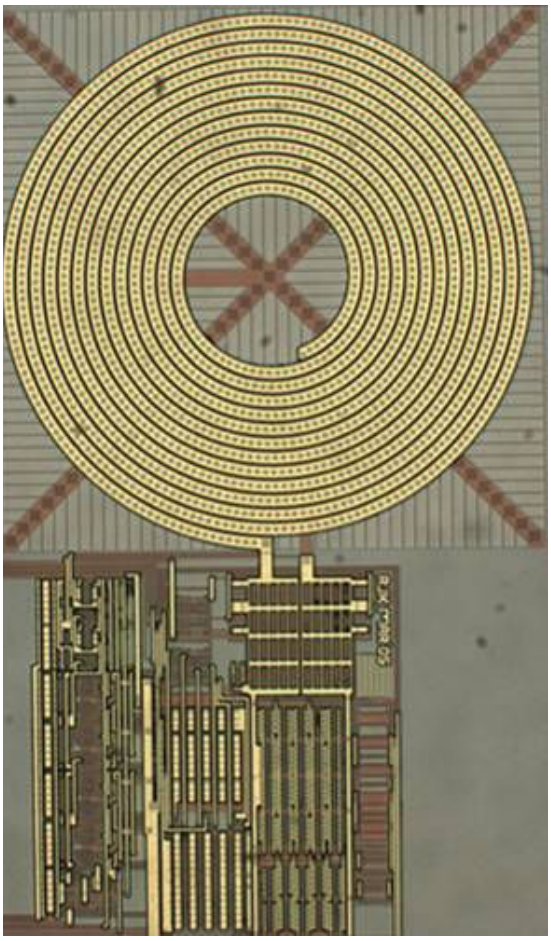

Fig. 9. Photo of FSK transmitter. The 54-nH inductor measures 470 µm in diameter and has $Q \approx 3$ at 433 MHz.

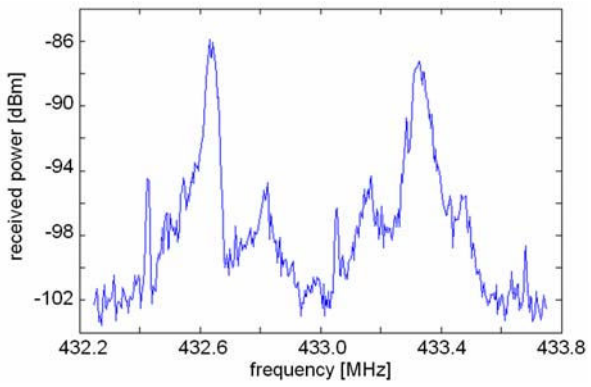

Fig. 10. Spectrum of FSK data transmitter sending a typical data frame at 330 kbit/s. Dipole antenna was positioned 13 cm from chip.

3. Wireless recording from cortex

While all the subsystems on our chips work well in isolation, at the system level we have with problems of crosstalk and digital interference with the sensitive analog circuits. When the digital FSMs and ADCs are running, interference appears on the neural amplifiers. Noise in the on-chip reference voltages also degrades neural amplifier performance. We have tracked down likely paths for this interference, and we believe they can be fixed through better layout and isolation of reference voltages. The FSK transmitter also exhibits diminished performance (increased BER) when all digital systems on the chip are active. Again, we believe this can be improved through more careful isolation of reference voltages used across the chip.

While the digital interference did not prevent us from seeing the large (nearly 500 μV at the input to the amplifier) pre-recorded neural signals in Fig. 6, most spikes recorded with extracellular electrodes have amplitudes in the range of 50 – 150 μV. In order to test our system in an *in vivo* experiment, we used two INI chips in concert: we used an amplifier from one chip to boost the signal by 60 dB, and we used the ADC and FSK transmitter on a second chip to digitize and transmit the neural data. Since the digital systems were turned off on the first chip, digital interference did not affect the neural signal amplifier. This two-chip configuration did not permit the use of the spike detectors, and it required that we power the chips from a battery instead of a coil.

We obtained neural signals from a 10 × 10 UEA implanted in the auditory cortex of a cat. The UEA was attached to a head-mounted transdermal connector via 100 insulated wires, represented by the dotted line in Fig. 11. A shielded cable approximately 40 cm in length was used to connect the neural signal amplifier to one selected electrode from the 100-pin connector. The frame of the connector, which was in contact with the animal's skin and skull, was tied to ground. The chips, which were packaged in ceramic LCC packages, were mounted on small printed circuit boards with the output of the amplifier from the first chip connected to the ADC input of the second chip. A resonant dipole receiving antenna was positioned 2 cm from the second chip. The demodulator/receiver recovered a 330 kb/s binary data from the 433-MHz FSK signal. A custom microcontroller system located and interpreted data frames (see Fig. 7) in the binary data stream, and sent the digitized neural signal to a PC via a USB connection.

Fig. 12 shows 30 superimposed neural spikes (with the mean waveform shown as a bold line) recorded from an electrode on the UEA and transmitted wirelessly 2 cm to a receiving antenna and FSK demodulator/receiver. The spikes have been aligned and superimposed in software to facilitate comparison and analysis. We wirelessly recorded neural signals from the same UEA in the same animal twice a week over a period of five weeks. Future versions of the chip should permit fully-integrated, coil-powered recording from live cells.

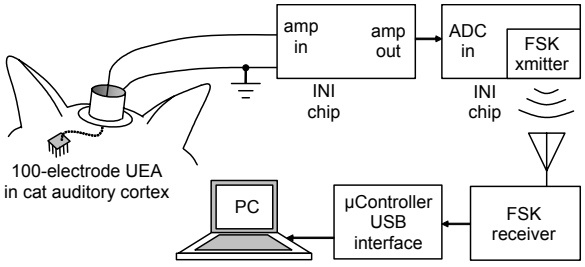

Fig. 11. Diagram of wireless cortical recording experiment. One INI chip was used to amplify the neural signal by 60 dB. A second INI chip digitized and transmitted the signal to an antenna 2 cm away.

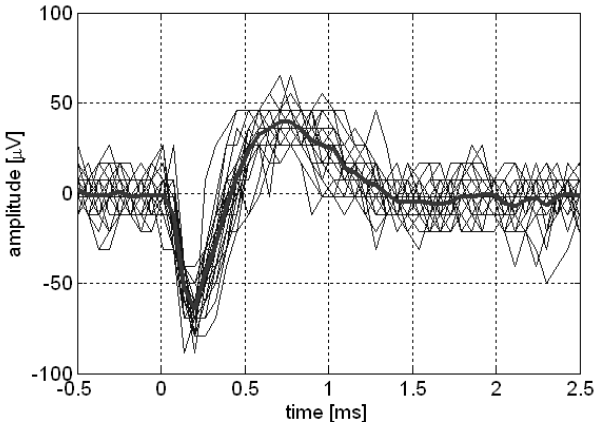

Fig. 12. Electrode-referred neural signals recorded from auditory cortex of cat using a Utah Electrode Array and transmitted wirelessly. The figure shows 30 super-imposed spikes along with the average waveform (bold line).

4. Conclusions

The complete INI chip dissipates 13.5 mW of power when the unregulated dc voltage is at its minimum allowable level of 3.55 V. (Since the efficiency of linear voltage regulators decreases with higher unregulated voltage, it is desirable to operate at the lowest allowable coil voltage; at 3.55 V, the

regulator consumes about 7% of the total system power.) The FSK transmitter consumes 50% of this power, and the low-noise neural signal amplifiers consume 30% with all amplifiers powered up. The transmitter power could be reduced by using a process with a thick-metal option to increase inductor *Q*.

The design of any implantable neural recording device for neuroprosthetic applications is driven by two dominant factors. First, the system is severely limited in its power dissipation due to tissue heating concerns. Second, large amounts of continuously streaming data must be transmitted wirelessly out of the body with very little latency. These two concerns dictate almost every aspect of circuit and system-level design. Power limitations strongly suggest that the implanted device perform only the minimum required functions of amplification, data reduction and/or compression, and telemetry; any additional computation is best performed outside the body where size and heat dissipation is not as much of a concern.

Future neural recording systems may use specialized circuits to isolate and record LFP energy [10] or perhaps perform spike sorting – distinguishing between several distinct neurons recorded by a single electrode on the basis of their action potential shapes [11]. Adding spike sorting does improve the accuracy of neuroprosthetic control somewhat, but at a substantial cost in terms of system complexity. A "middle ground" approach such as transmitting a small number of spike "features" and then clustering the spikes on the basis of these extracted features using external computational power may be the best solution when power is taken into account. Whatever the solution to these problems, the field of neuroprosthetics poses interesting challenges for integrated circuit designers in the years ahead.

5. Acknowledgments

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