Signal Amplification, Detection and Transmission in a Wireless 100-Electrode Neural Recording System

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Abstract—**We are developing a fully-implantable neural recording system with wireless power and data transfer. As part of this system, we have developed a low-power integrated circuit that performs power rectification and regulation, reception of configuration data, neural signal amplification and filtering, spike detection, neural signal digitization and RF transmission. The chip includes 88 amplifiers having a gain of 60 dB from 1 to 5 kHz. An integrated ADC operates at 15 kSamples/sec with 9-bit resolution. A 433-MHz RF transmitter uses FSK modulation to transmit one digitized neural signal and spike detection data from all channels. Total power consumption is 13.5 mW.**

I. Introduction

Multi-channel neural recording is necessary in neuroscience research and in potential prosthetic applications. Current technology requires wires to connect the electrode array to an external bank of amplifiers. These wires penetrate the skull and skin and increase the risk of infection. Long wires can also degrade signal quality by coupling to noise sources. Additionally, in neuroscience experiments, wires restrict the subject's movement. A wireless neural recording system would alleviate many of these problems: amplifiers would be connected directly to the electrodes, the skin would remain intact, and the subject's movement would be less restricted, enabling neural recording in more natural situations.

This paper describes a single-chip, low-power integrated circuit which was developed for a fully-implantable wireless neural recording system. The integrated circuit, which was fabricated in a commercial 0.5-µm 3-metal, 2-poly CMOS process, is designed to be flip-chip bonded onto the back of a 100-channel Utah Electrode Array (UEA) [1]. The chip includes circuitry for wireless power and data reception, neural signal amplification and digitization, action potential ("spike") detection, and FSK data transmission. The complete chip measures 4.7 mm × 5.9 mm and contains over 30,000 transistors and 5,000 passive components.

In this paper, we first discuss the fully-implantable wireless neural recording system under development. We then discuss the integrated circuit we have developed as part of that system. We describe the subsystems of the chip, including the wireless link for power and configuration data, the neural signal amplification and detection, the ADC, and the RF transmitter. Measurements from bench-top testing of the chip are then presented. Finally, we discuss current work on an improved version of this chip.

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II. Neural Recording System Under Development

The complete wireless Integrated Neural Interface (INI) system will consist of a 100-channel UEA with an integrated circuit flip-chip bonded directly to the electrodes. In addition to the UEA and the integrated circuit, three SMD capacitors and a 6-mm diameter coil for wireless power reception will be included in the system. The entire system will be encapsulated with SiC and parylene prior to implantation. A diagram of the system is presented in Figure 1.

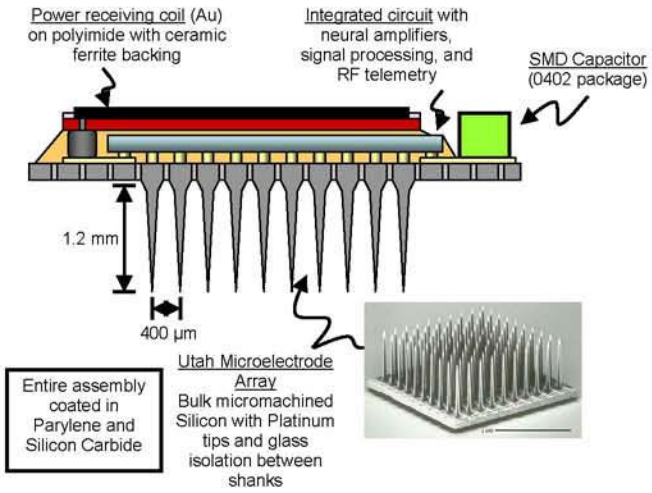

Fig. 1. Proposed wireless neural recording system, consisting of a Utah Electrode Array with an IC flip-chip bonded directly to the electrodes. A Low Temperature Co-fired Ceramic (LTCC) coil will be mounted on the IC to receive the power signal.

Because the system will be implanted in a living organism, several severe design constraints were imposed. First and foremost, power dissipation of the chip must be kept to a minimum to avoid heating and damaging biological tissues. The total area of the chip is also constrained to be slightly larger than the 4 mm by 4 mm UEA; circuits dedicated to a single electrode are confined to a 400 μm by 400 μm area, corresponding to the inter-electrode spacing. Finally, the data rate is limited by the complexity of the RF transmitter and its restricted power budget. The chip was designed with these constraints in mind. All systems were designed to be as simple as possible to establish an infrastructure which could be refined and expanded upon in the future.

On the chip, first described in [2], neural amplifiers are laid out in a 10 × 10 array at a 400 μm pitch, corresponding to the inter-electrode spacing. Twelve of the 100 electrodes are used to provide the reference potential. The remaining 88 electrodes are connected to neural signal amplifiers. A small bond pad local to each amplifier allows connection of the chip to the electrode array. The neural signal amplifiers are designed to amplify action potentials and reject local field potentials; each has a gain of 60 dB over a bandwidth from 1 kHz to 5 kHz. Because digitizing the signals from all electrodes would lead to prohibitively large data rates, we chose to digitize the waveform from one electrode and detect spikes on the remaining electrodes. A 9-bit successive-approximation ADC with a charge redistribution DAC is used to digitize the signal from one amplifier selected with an analog MUX. Data are digitized at the rate of 15 kSamples/sec. Comparators in each amplifier block perform spike detection by means of threshold crossings, with a programmable threshold set by a 7-bit *R*-2*R* DAC. The chip produces a 330-kbps data stream that interleaves the ADC data from a single amplifier, spike detector data from all amplifiers, and parity bits. Digitized neural data is transmitted off chip using a fully-integrated 433-MHz FSK transmitter. Measured power dissipation is 13.5 mW.

III. Wireless Power and Configuration Data

Power will be provided to the implanted system by means of an inductive link with an external transmitter. In the final integrated system, a 6-mm low temperature co-fired ceramic (LTCC) coil will be mounted on the chip to receive the power signal. The received power signal is rectified by a fully integrated, CMOS-compatible full-wave rectifier [3]. The rectified power signal is then regulated to 3.3 V. In addition to providing power, the inductive link provides a clock signal and configuration data to the chip. The clock derived from the frequency of the 2.64-MHz power signal. This frequency was chosen because biological tissue does not absorb much RF energy in this frequency range. Configuration data are transmitted using ASK modulation of the power signal. Configuration data are used to selectively power down amplifiers connected to electrodes with no neural activity, to set the threshold for spike detection, and to control the multiplexer at the input of the ADC. The circuits used to receive the clock and configuration data are described in [4].

IV. Amplification, Detection and Digitization

A. Amplification

Each electrode in the UEA is bonded directly to the input of a low-noise amplifier, shown in Figure 2. The neural signal amplifiers were designed to provide a gain of 60 dB on the bandwidth 300 Hz to 5 kHz. This high gain is necessary because extracellular action potential waveforms typically have amplitudes in the range of tens or hundreds of microvolts. The amplifier consists of three stages: a low-noise amplifier with a gain of 100, a high-pass filter, and a second amplifier with a gain of 10. Because we are performing spike detection based on threshold crossings, it is desirable to eliminate low-frequency local field potentials as much as possible. These signals occur at frequencies up to 100 Hz and can have amplitudes as great as the spikes. Our amplification system provides second-order roll-off at both the high-pass and low-pass corner frequencies. The neural signal amplifiers each occupy 0.0884 mm^2 of chip area and use 12.8 μA of current. The measured amplifier gain is 60.1 dB over a bandwidth of 1 kHz to 5 kHz. The input-referred noise is 5.1 μVrms, which is lower than typical background noise levels in extracellular neural recordings.

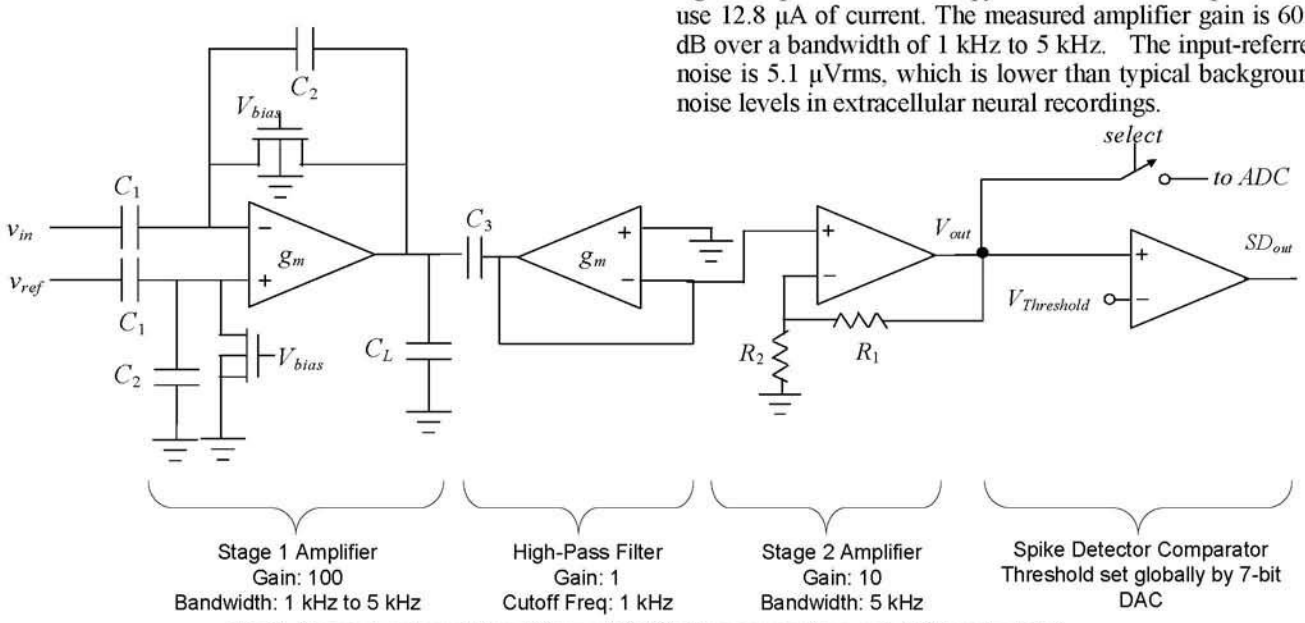

Fig. 2. Neural signal amplifiers, filters, spike detection comparators, and ADC analog MUX

The first stage low-noise amplifier is based on the design described in [5]. The previous design used MOS-bipolar elements in the feedback network to set a high-pass corner frequency below 1 Hz. In the current design, we use an nMOS transistor instead of the MOS-bipolar element to set the high-pass corner frequency of the first stage. By biasing the nMOS transistor in weak inversion, the high-pass corner can be tuned in the range 100 Hz-3 kHz. The use of this transistor in the amplifier's feedback led to relatively high levels of harmonic distortion because of its exponential voltage-current relationship. For this reason, MOS-bipolar elements will be used in future designs, possibly with higher-order high-pass filtering in subsequent stages. The low-pass characteristic of the first stage is set by the dominant compensation pole, which is set to 5 kHz.

The high-pass filter consists of a poly-poly capacitor and a wide-range OTA operating in the subthreshold regime. It was designed to have a high-pass corner frequency in the range of 300 Hz. The input linear range of the OTA is approximately 80 mV, which is more than sufficient for neural signals that have been amplified by 40 dB, which will be in the range of tens of millivolts. While testing the high-pass filters, it was found that parasitic poles in the OTA led to peaking in the frequency response when the corner frequency was set below 1 kHz. This problem has been rectified in our current redesign.

Finally, the second stage amplifier provides another 20 dB of gain from DC to 5 kHz. This amplifier is a standard two-stage integrated op-amp, with high resistance polysilicon resistors providing the feedback network. The cutoff frequency of this stage is set by the compensating dominant pole of the amplifier.

B. *Spike Detection*

Spike detection is accomplished by means of threshold crossings. In the current system, the threshold is set globally by a 7-bit DAC with an LSB of 4.8 mV (4.8 μV referred to the electrodes). The DAC output ranges from the reference voltage to 614 mV above reference. The DAC consists of a two-stage operational amplifier with an *R*-2*R* ladder of high-resistance polysilicon resistors [6]. It occupies 0.133 mm^2 and consumes 6.58 μA of current. The comparators are a standard track-and-latch design. They each occupy 4400 μm^2 and consume 1.78 μA of current. The comparators are clocked at a rate of 15 kHz, which is fast enough to detect any neural spike. If a spike is detected, the result is latched and held until the result has been polled; this occurs at the rate of 1 kHz. The latches are reset after polling has been completed.

C. *Analog-To-Digital Conversion*

The output of one neural signal amplifier is digitized by a successive approximation ADC using a charge-redistribution DAC. This architecture was chosen because of its low power consumption and because the excellent matching of integrated capacitors will lead to good ADC linearity. The ADC was designed to have 10-bit resolution operating on the range from 0 to $0.75xV_{DD}$ with a sampling rate of 15 kSamples/sec. The ADC's LSB is 2.4 mV (2.4 μV referred to the electrode). When testing the chip, it was found that the MSB of the ADC did not operate properly at full speed; for further testing, we only used the bottom 9 bits, and biased the outputs of the amplifiers at the midpoint of this range. The problem with the MSB has been corrected in the current redesign of the chip. The ADC occupies 0.501 mm^2, and consumes 45.7 μW of power.

Waveforms from the neural amplifiers, spike detectors, and ADC are presented in Fig. 3. For this measurement, we played previously recorded neural data into the input of one of the neural signal amplifiers. The neural data were taken from a rhesus monkey at the Neural Prosthetic Systems Laboratory at Stanford University. During this measurement, the chip was powered wirelessly. Bench-top equipment was used to provide bias currents to the chip. These waveforms were measured via wired connections to the chip; the RF receiver is still under development. Additional bench-top chip measurements are presented in Table I.

V. Data Transmission

The digitized neural signal from one electrode is interleaved with the spike detector data from all 88 recording electrodes for transmission. Parity is computed on each 10-bit word. Synchronization bits are also transmitted periodically. These data are organized into 352-bit frames and transmitted at 330 kbps (one frame every 1.06 ms). The data frame is transmitted off-chip by a fully-integrated *LC* VCO operating at 433 MHz. The digital data modulate the carrier frequency to 433 MHz ± 660 kHz. The integrated inductor in the VCO also serves as the transmit antenna. The received FSK spectrum is shown in Fig. 4.

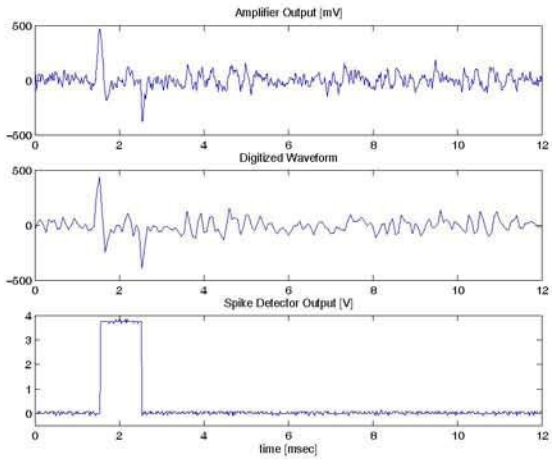

Fig. 3. Neural data at the output of a neural amplifier (top) and digitized by the ADC (middle). The output of the spike detector for this electrode is shown at bottom. These waveforms were captured while the chip was powered wirelessly. Neural data courtesy of K. Shenoy, Stanford University.

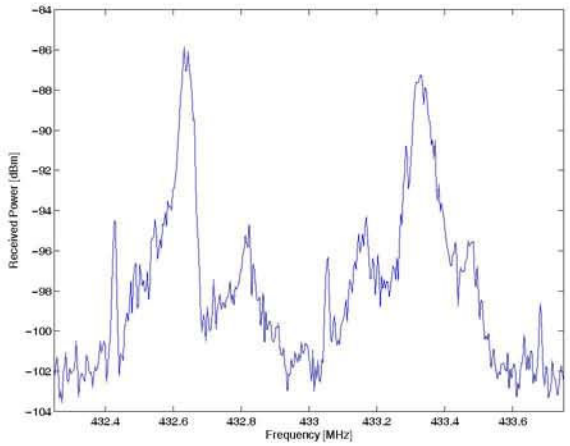

Fig. 4. Received FSK spectrum from the integrated RF transmitter. The signal was received using a 433-MHz resonant dipole at a distance of 13 cm from the chip.

VI. Conclusion

We have described the implantable wireless neural recording system under development at the University of Utah and the integrated circuit that has been designed and tested as part of this system. We have also presented bench-top testing results for the various subsystems in this integrated circuit.

A revision of this chip is currently being fabricated. Several improvements have been made in the revised system. Current and voltage biases are now fully integrated. The ADC will operate at full speed with 10-bit resolution.

TABLE I
MEASURED PERFORMANCE OF INI CHIP

Power/command signal frequency	2.64 MHz
Minimum required receive coil voltage amplitude	5.7 V (peak)
3.3 V voltage regulator dropout (I_L = 3 mA)	250 mV
Load regulation (I_L = 2-10 mA)	0.15 %
Line regulation ($Vunreg$ = 3.5 V – 8.0 V)	< 0.30 %/V
Maximum command input data rate (ASK)	6.5 kbps
Number of channels/electrodes	88 signal, 12 ground
Neural signal amplifier gain	60.1 dB (1.1 – 5 kHz)
Input referred noise	5.1 μVrms
Individual amplifier supply current	12.8 μA
ADC resolution (LSB = 2.4 μV electrode-referred)	9 bits
ADC sampling rate	15.0 kSamples/s
ADC INL/DNL error (codes 50-511)	±0.8 LSB/ ±0.6 LSB
Spike detector threshold resolution (LSB = 4.8 μV electrode-referred)	7 bits
FSK data transmission frequency	433 MHz
FSK data rate	330 kbps
Received signal power at distance of 13 cm	-86 dBm
Total chip power dissipation	13.5 mW
Total chip area (0.5-μm, 2P3M CMOS)	27.3 mm^2

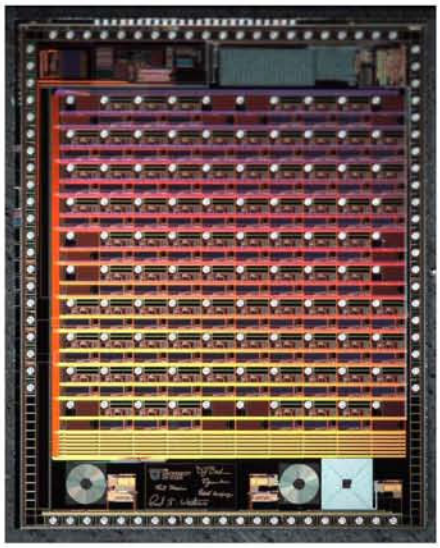

Fig. 5. Die photo of the Integrated Neural Interface chip. The chip was fabricated in a commercially available 0.5 um, 3 metal 2 poly CMOS process.

The voltage regulator has been refined to have reduced ripple on the supply lines. Each electrode now has its own DAC to set a local spike detection threshold. A temperature sensor has been included in the system to measure self-heating. A scaled version of the unregulated supply voltage will be digitized and transmitted wirelessly for closed-loop control of the power transmitter. The redesigned neural amplifiers have lower harmonic distortion, and the high-pass filters' cutoff frequencies are programmable. The VCO will also operate on lower power.

Acknowledgments

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