30.2 A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System

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In the past decade, neuroscientists and clinicians have begun to use implantable MEMS multielectrode arrays (e.g., [1]) to observe the simultaneous activity of many neurons in the brain. By observing the action potentials, or "spikes," of many neurons in a localized region of the brain it is possible to gather enough information to predict hand trajectories in real time during reaching tasks [2]. Recent experiments have shown that it is possible to develop neuroprosthetic devices – machines controlled directly by thoughts – if the activity of multiple neurons can be observed.

Currently, data is recorded from implanted multielectrode arrays using bundles of fine wires and head-mounted connectors; all electronics for amplification and recording is external to the body. This presents three major barriers to the development of practical neuroprosthetic devices: (1) the transcutaneous connector provides a path for infection, (2) external noise and interfering signals easily couple to the wires conveying weak neural signals (<500μV) from high-impedance electrodes (>100kΩ), and (3) the connector and external electronics are typically large and bulky compared to the ~5mm electrode arrays. To eliminate these problems, data from the implanted electrodes should be transmitted out of the body wirelessly. This requires electronics at the recording site to amplify, condition, and digitize the neural signals from each electrode. These circuits must be powered wirelessly since rechargeable batteries are relatively large and have limited lifetimes. Low power operation (<100mW) is essential for any implanted electronics as elevated temperatures can easily kill neurons.

A wireless, fully-implantable neural recording system is being developed to facilitate neuroscience research and neuroprosthetic applications (see Fig. 30.2.1). The system is based on the Utah Microelectrode Array (UEA), a 10×10 array of platinum-tipped silicon extracellular electrodes [1]. This paper describes the development of a mixed-signal integrated circuit that will be flip-chip bonded to the back of the UEA using Au/Sn reflow soldering. This chip will directly connect to all 100 electrodes, amplify the neural signals from each electrode, digitize this data, and transmit it over an RF link (see Fig. 30.2.2). Power will be delivered to a 6mm coil mounted on the back of the chip using an inductive link. (This coil is under development; the chip is currently tested using dc power for initial tests and a 19mm coil for wireless power tests.) The entire device will be coated in parylene and silicon carbide to protect it from internal body fluids.

The integrated circuit measures 4.7×5.9mm² and was fabricated in a commercial 0.5μm 3M2P CMOS process (see Fig. 30.2.7). An on-chip bridge rectifier and bandgap-referenced low-dropout voltage regulator provides a 3.3V dc power supply from a 2.64MHz ac coil power signal. External capacitors are used to resonate with the power coil and smooth the unregulated dc supply. A system clock is recovered from the coil frequency, and ASK modulation of the power signal allows the external user to send commands and configuration data to the chip at 6.5 kb/s (see [3] for a similar power/data link). The center of the chip consists of a 10×10 array of amplifiers laid out in a 400μm pitch, corresponding to the inter-electrode spacing. A bond pad local to each amplifier allows direct connection of the chip to the UEA. Twelve of the 100 platinum-tipped electrodes are used as "ground" or "reference" electrodes; the remaining 88 electrodes are connected to integrated low-noise neural signal amplifiers. The amplifiers are ac-coupled to eliminate the large dc offset found at the electrode-tissue interface; their bandwidth extends from 1-5kHz to pass neural spikes and reject low-frequency local field potentials (see Fig. 30.2.3). The amplifiers have a measured gain of 60dB and input-referred noise of 5.1μVrms. Each amplifier draws only 12.8μA of supply current; we use the design techniques presented in [4] to minimize noise and power consumption. Individual amplifiers may be powered down with a command signal so that unused electrode channels do not dissipate power.

A 9b charge-redistribution ADC is used to digitize the signal from one amplifier at 15kSamples/s. The ADC consumes less than 30μA, and has measured INL and DNL <0.8 LSB for all but the lowest 50 codes. Digitizing all 88 neural waveforms simultaneously would generate prohibitively high data rates (>10Mb/s) for low-power RF transmission. Therefore, we perform on-site data reduction by incorporating one-bit "spike detector" comparators into each amplifier block. The spike detection threshold is set by a 7b DAC. The user selects the detection threshold level and also controls an analog MUX that routes the desired electrode amplifier signal to the ADC. The chip produces a 330 kb/s data stream that interleaves ADC data from one selected amplifier, spike detector data from all amplifiers, and parity bits. Figure 30.2.4 shows recorded neural data (courtesy of K. Shenoy, Stanford University) played through a neural amplifier on the chip; either the complete digitized waveform or simply the detected spikes may be transmitted. (An alternate approach to neural data reduction is presented in [5].)

Digitized neural data is transmitted using a fully-integrated 433MHz FSK transmitter. The VCO uses a planar spiral inductor (54nH, $Q \approx 3$) optimized for maximum LC parallel-circuit equivalent resistance to minimize power consumption (see Fig. 30.2.7). The inductor also serves as a transmitting antenna. At an operating supply current of 1.9mA, we are able to receive FSK-modulated data (at -86dBm) at a distance of 13cm using a half-wave resonant dipole antenna (see Fig. 30.2.5).

The complete chip dissipates 13.5mW of power when the unregulated dc voltage is at its minimum allowable level of 3.55V. The FSK transmitter consumes 50% of this power, and the low-noise neural signal amplifiers consume 30% with all amplifiers powered up. The transmitter power could be reduced by using a process with a thick-metal option to increase inductor Q. The measured performance of the integrated neural interface chip is summarized in Fig. 30.2.6.

References:

[1] C.T. Nordhausen, E.M. Maynard, and R.A. Normann, "Single Unit Recording Capabilities of a 100-Microelectrode Array," *Brain Res.*, 726: 129-140, 1996.

[2] J. Wessberg, et al., "Real-Time Prediction of Hand Trajectory by Ensembles of Cortical Neurons in Primates," *Nature*, vol. 408: 361-365, 2000.

[3] H. Yu and K. Najafi, "Low-Power Interface Circuits for Bio-Implantable Microsystems," *ISSCC Dig. Tech. Papers*, pp. 194-195, Feb., 2003.

[4] R.R. Harrison and C. Charles, "A Low-Power, Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE J. Solid State Circuits*, vol. 38, no. 6, pp. 958-965, June, 2003.

[5] R. Olsson and K. Wise, "A Three-Dimensional Neural Recording Microsystem with Implantable Data Compression Circuitry," *ISSCC Dig. Tech. Papers*, pp. 558-559, Feb., 2005.

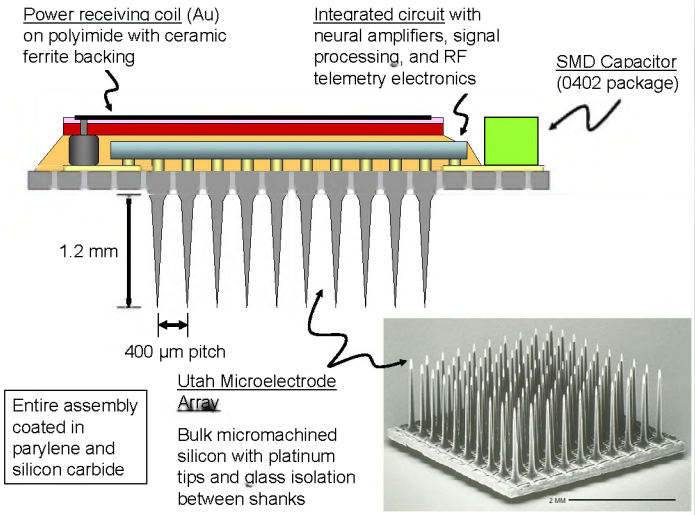


Figure 30.2.1: Complete Integrated Neural Interface (INI) assembly.

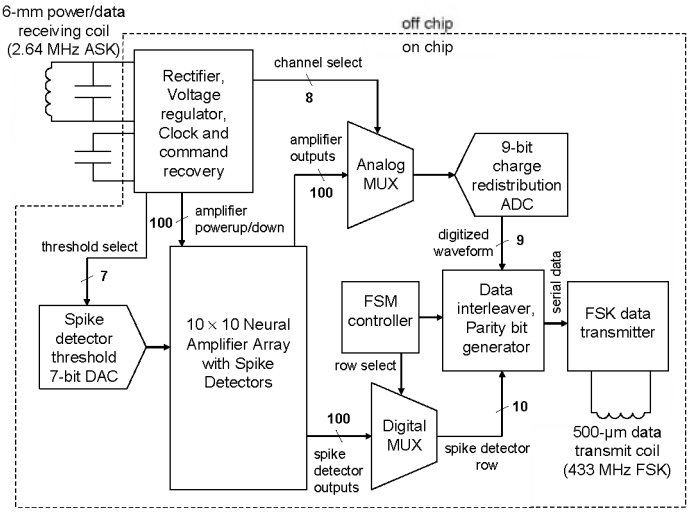


Figure 30.2.2: Integrated Neural Interface system block diagram.

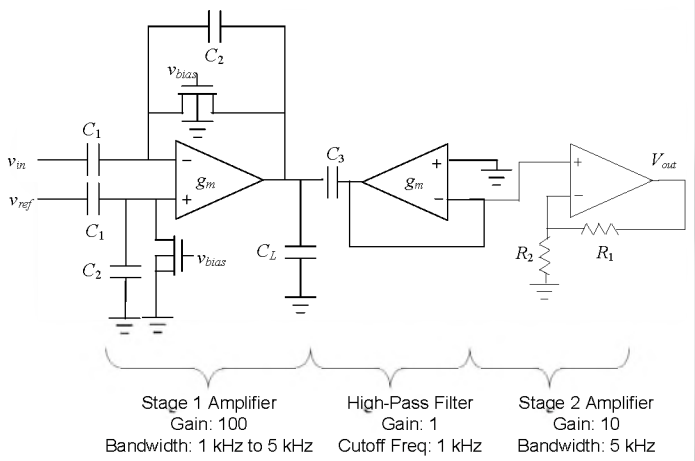


Figure 30.2.3: Schematic of neural signal amplifier. Resistors are made from high-resistance polysilicon.

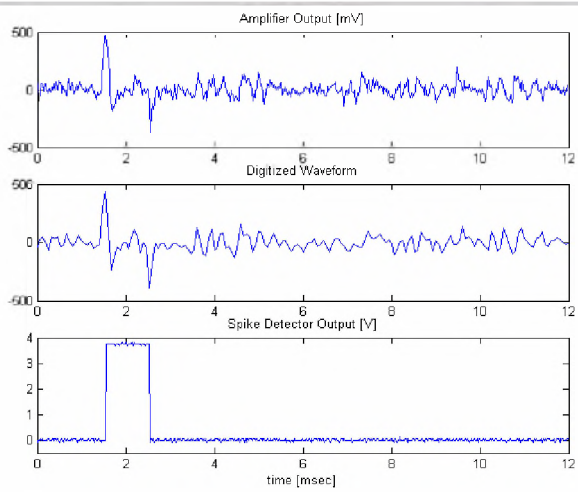


Figure 30.2.4: Response of wireless-powered chip to neural waveform played from waveform generator: analog output of a neural signal amplifier (top), waveform reconstructed from ADC output (middle), output of corresponding spike detector (bottom).

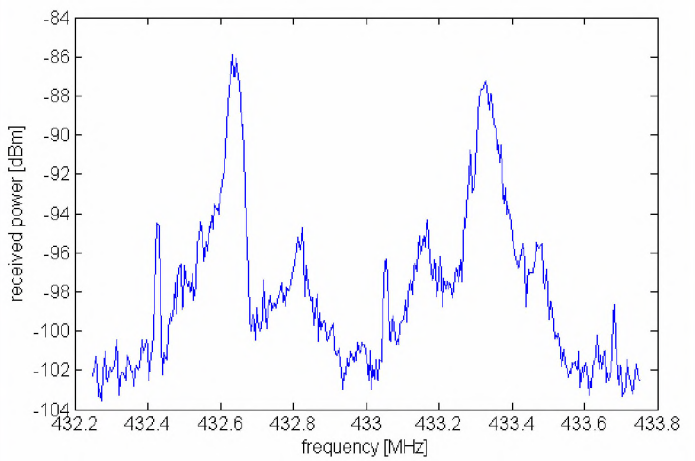


Figure 30.2.5: Spectrum of FSK data transmitter sending a typical data frame at 330kb/s. Dipole antenna was positioned 13cm from chip.

Integrated Neural Interface IC Measured Performance	
Power/command signal frequency	2.64 MHz
Minimum required receive coil voltage amplitude	5.7 V (peak)
3.3-V voltage regulator dropout (I_L = 3 mA)	250 mV
Load regulation (I_L = 2-10 mA)	0.15 %
Line regulation (V_{unreg} = 3.5 V – 8.0 V)	<0.30 %/V
Maximum command input data rate (ASK)	6.5 kbps
Number of Channels/Electrodes	88 signal, 12 ground
Neural Signal Amplifier Gain	60.1 dB (1.1 – 5 kHz)
Input Referred Noise	5.1 µVrms
Individual Amplifier Supply Current	12.8 µA
ADC resolution (LSB = 2.4 µV electrode referred)	9 bits
ADC sampling rate	15.0 kSamples/s
ADC INL/DNL error (codes 50-511)	±0.8 LSB/ ±0.6 LSB
Spike detector threshold resolution (LSB = 4.8 µV electrode referred)	7 bits
FSK data transmission frequency	433 MHz
FSK data rate	330 kbps
Received signal power at distance of 13 cm	-86 dBm
Total chip power dissipation	13.5 mW
Total chip area (0.5-µm, 2P3M CMOS)	27.3 mm^2

Figure 30.2.6: Table summarizing measured INI chip performance.

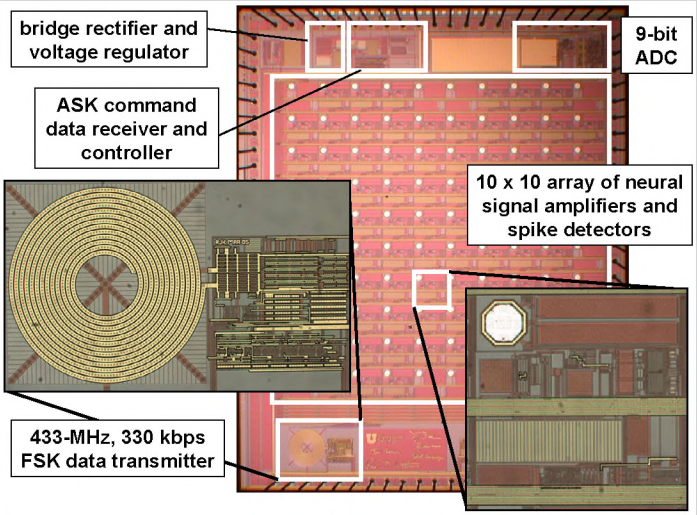
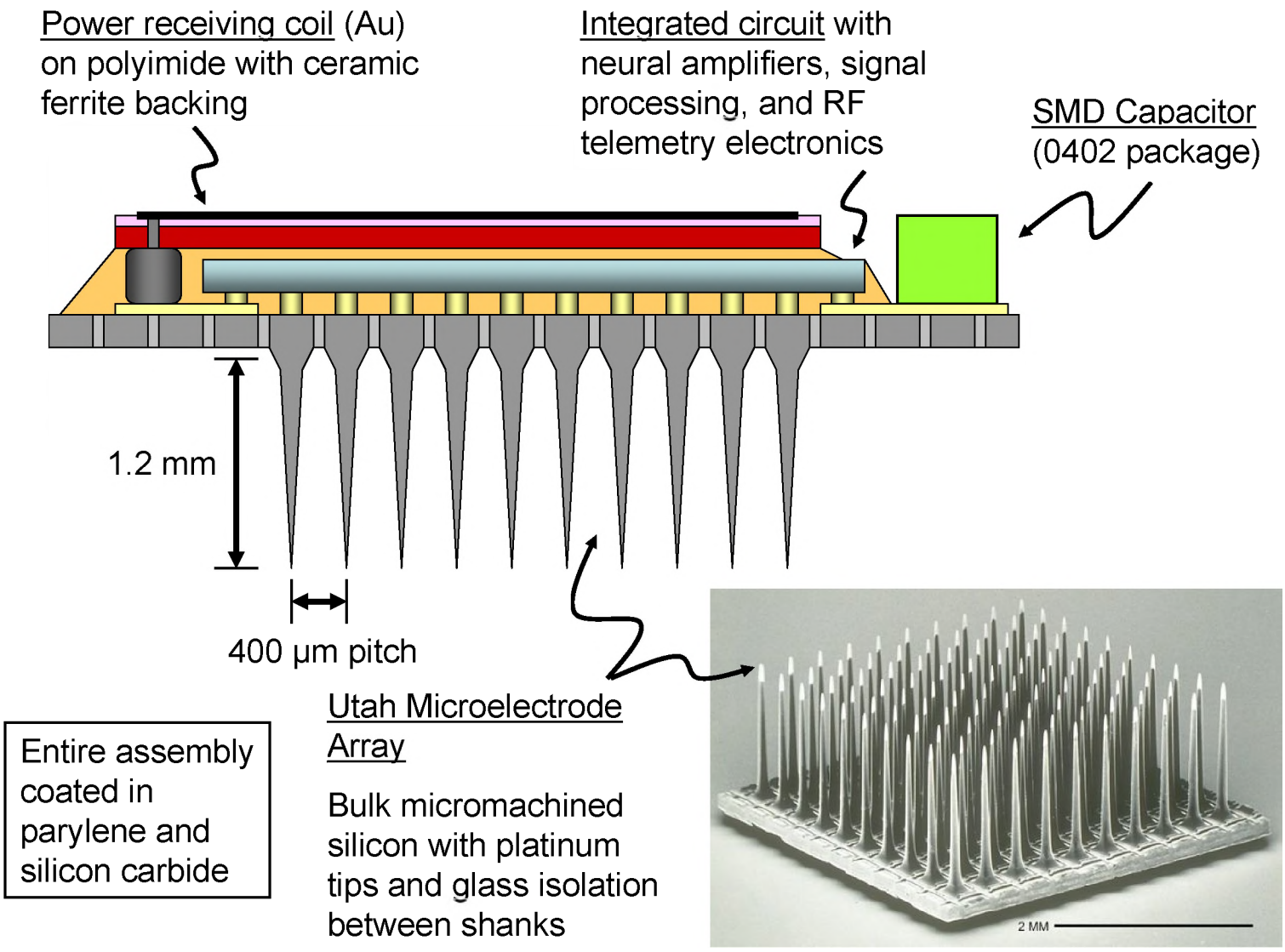


Figure 30.2.7: Die photo of 4.7×5.9mm² integrated neural interface chip. Insets show FSK data transmitter with integrated 54 nH inductor (left) and neural amplifier/spike detector cell (right).



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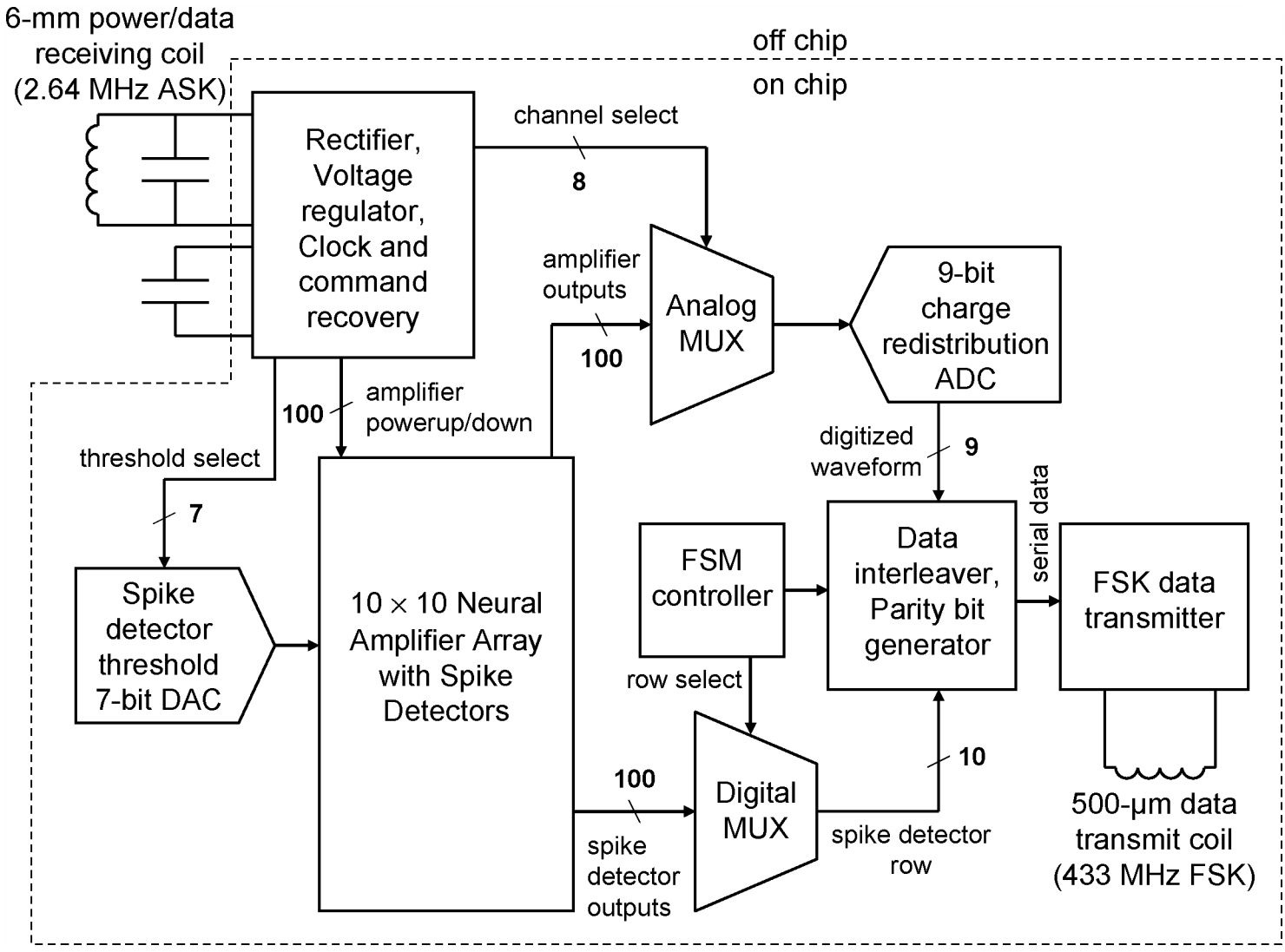

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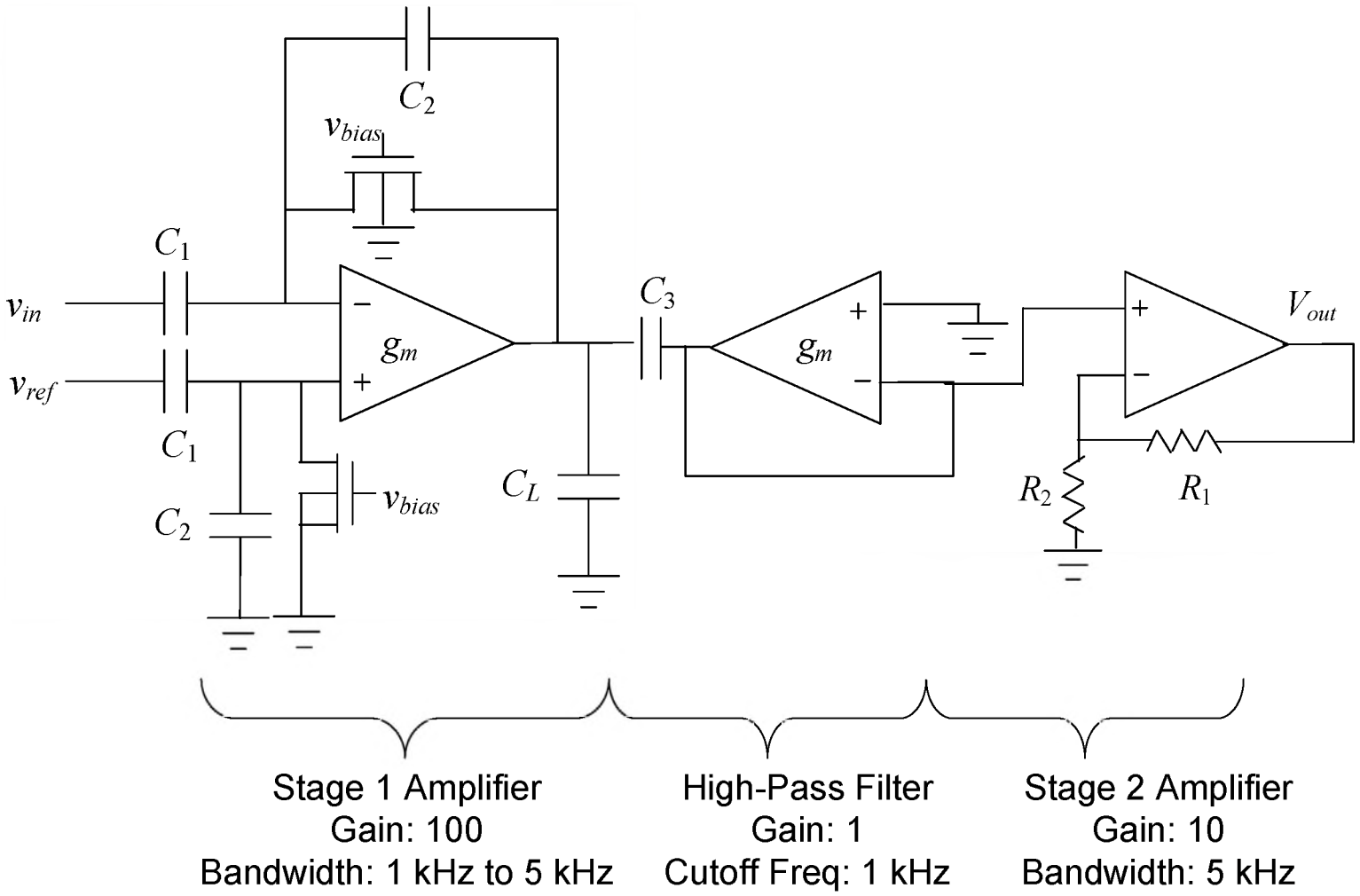

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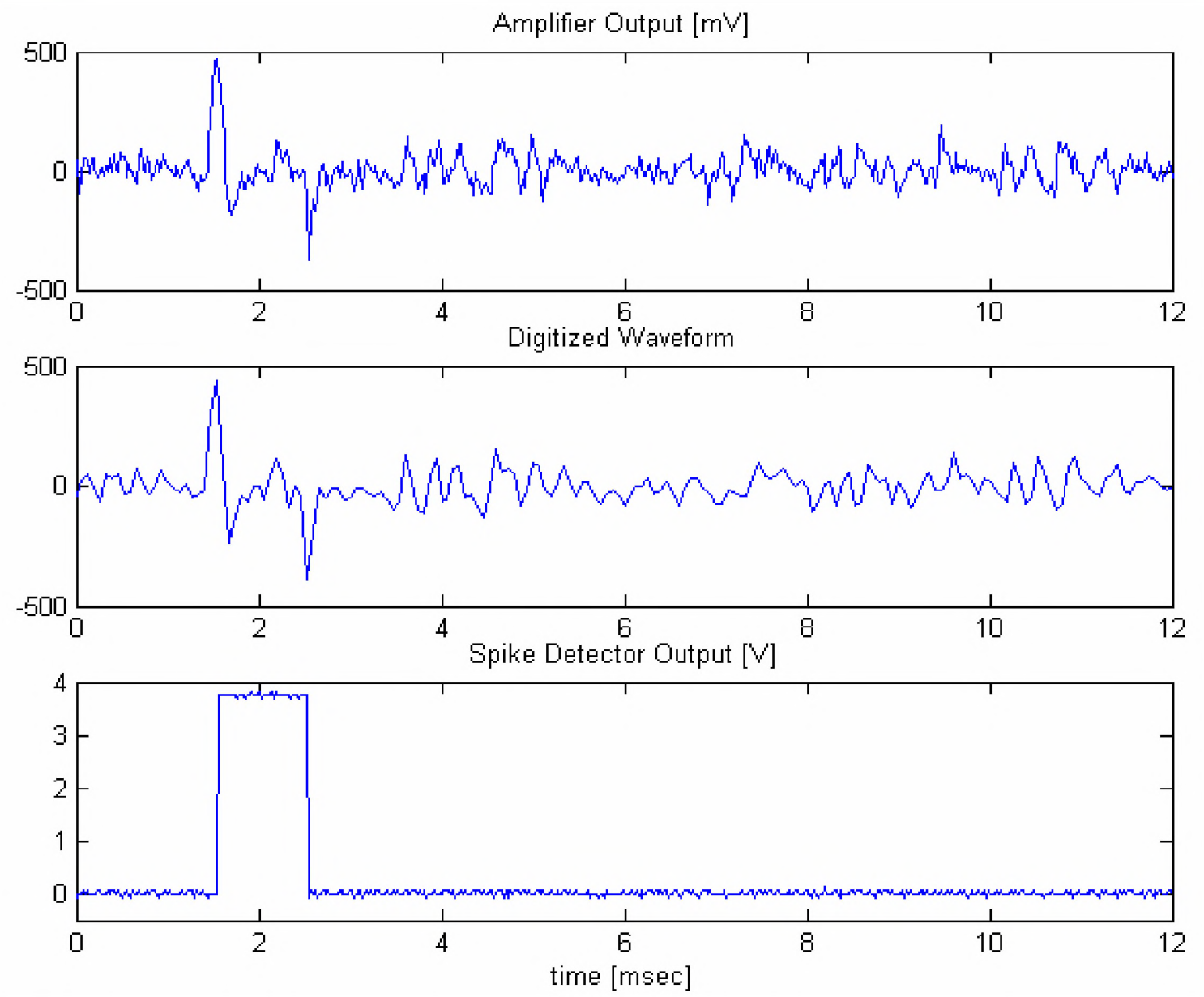

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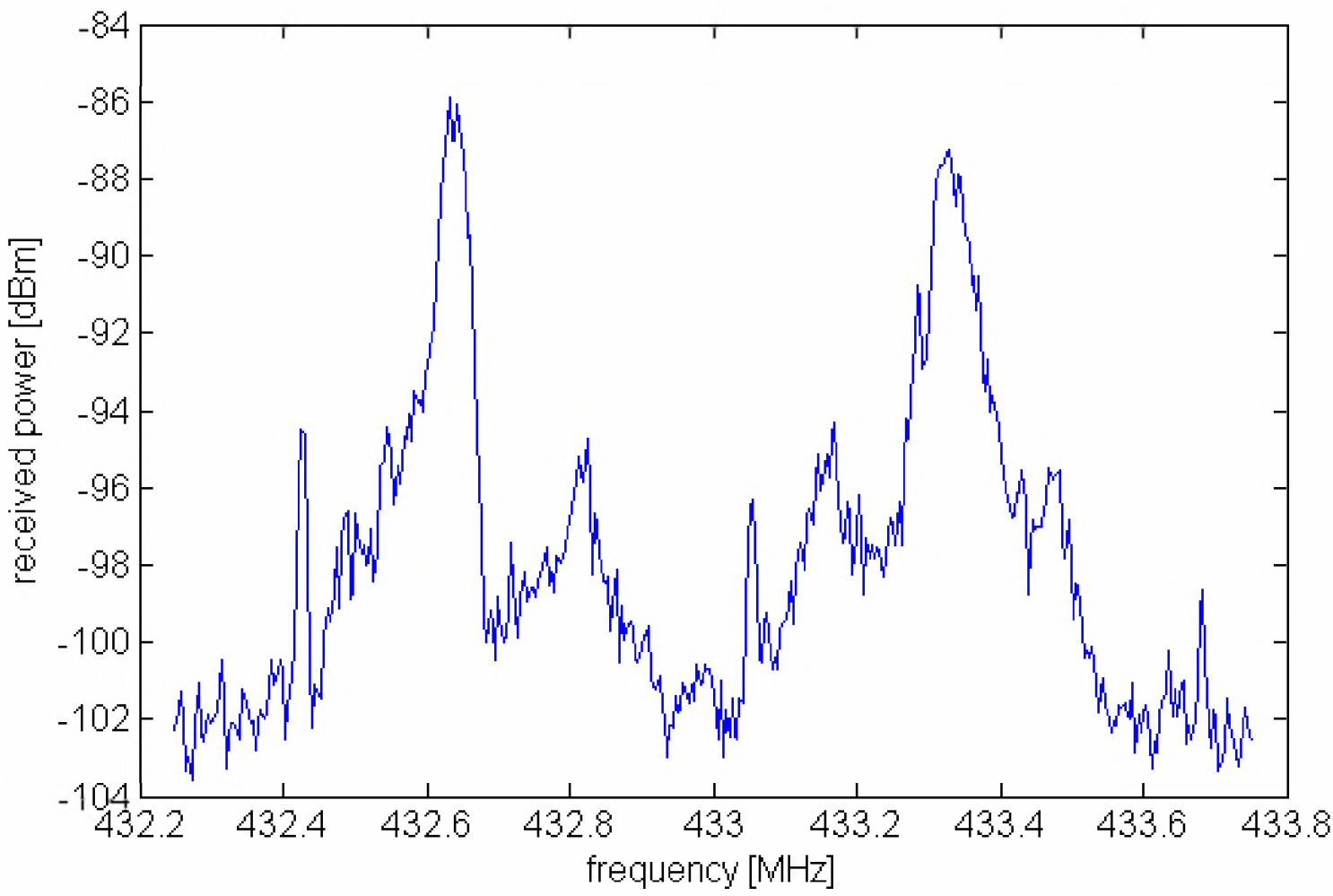

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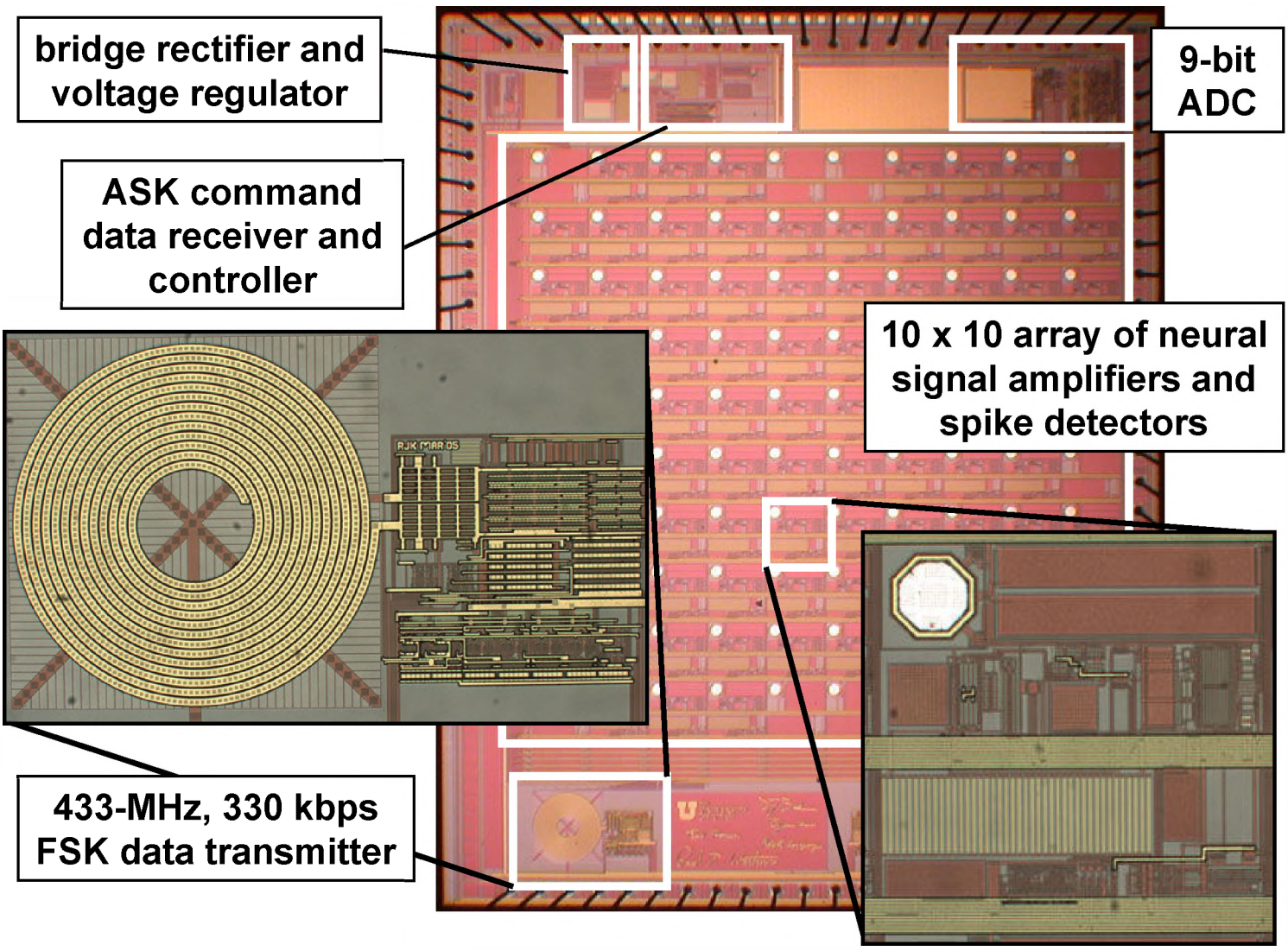

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