A LOW-POWER, LOW-NOISE CMOS AMPLIFIER FOR NEURAL RECORDING APPLICATIONS

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ABSTRACT

There is a need among scientists and clinicians for low-noise, low-power biosignal amplifiers capable of amplifying signals in the mHz to kHz range while rejecting large dc offsets generated at the electrode-tissue interface. The advent of fully-implantable multielectrode arrays has created the need for fully-integrated micropower amplifiers. We designed and tested a novel bioamplifier that uses a MOS-bipolar pseudo-resistor to amplify signals down to the mHz range while rejecting large dc offsets. We derive the theoretical noise-power tradeoff limit – the noise efficiency factor – for this amplifier and demonstrate that our VLSI implementation approaches that limit. The resulting amplifier, built in a standard 1.5μm CMOS process, passes signals from 0.1mHz to 7.2kHz with an input-referred noise of 2.2μVrms and a power dissipation of 80μW while consuming 0.16mm^2 of chip area.

1. INTRODUCTION

There is a great demand for technologies that enable neuroscientists and clinicians to observe the simultaneous activity of large numbers of neurons in the brain. Multi-electrode neural recordings are becoming standard practice in basic neuroscience research, and knowledge gained from these studies are beginning to enable clinical and neuroprosthetic applications. Recent advances in MEMS technology have produced small (less than 4mm in any dimension) arrays of microelectrodes containing as many as 100 recording sites. "Next generation" neural recording systems must be capable of observing 100-1000 neurons simultaneously, in a fully-implanted unit.

While integrated electronics have been developed for small-scale amplification of the weak bioelectrical signals [1]–[9], existing circuits typically have either unacceptable noise levels or consume too much power to be fully implanted in larger quantities.

Recording neural signals with fully-integrated, low-power circuits is challenging. Extracellular neural signals have amplitudes of 10-100μV, and typical electrode impedances are around 100kΩ at 1kHz. Due to electrochemical effects at the electrode-tissue interface, dc offsets of 1-2V are common across differential recording electrodes. Neural "spikes" contain energy in the 100Hz – 7kHz band, while the energy of local field potentials (LFPs) extends below 1Hz. Some existing VLSI bioamplifier designs use off-chip capacitors in the nF range to obtain a low-frequency cutoff that passes LFP signals while rejecting large dc offsets [5],[6],[8],[9]. This approach is unfeasible for large numbers of implanted electrodes.

We designed and tested a fully-integrated amplifier suitable for recording biological signals from the mHz range to 7kHz. The amplifier rejects dc offsets at the input and offers the best power-noise tradeoff of any biosignal amplifier reported.

2. AMPLIFIER DESIGN

Figure 1 shows the schematic of our bioamplifier design. The midband gain A_M is set by C_1/C_2, and the bandwidth is $g_m/(A_M C_L)$, where g_m is the transconductance of the operational transconductance amplifier (OTA). Transistors M_a-M_d are MOS-bipolar devices acting as "pseudo-resistors". With negative V_{GS}, they function as diode-connected *p*MOS devices. With positive V_{GS}, the parasitic source-well-drain *pnp* bipolar transistor is activated, and the device acts as a diode-connected bipolar [10] (see Figure 2). For small voltages across this device, its incremental resistance r_{inc} is extremely high. For $|\Delta V| <$ 0.2V, we measured $dV/dI > 10^{10}\Omega$. We use two MOS-bipolar devices in series to reduce distortion for large output signals. The low-frequency cutoff ω_L is given by $1/(2r_{inc}C_2)$. Despite the long time constant, large changes in the input cause a large voltage across the MOS-bipolar elements, reducing their incremental resistance and giving a fast settling time.

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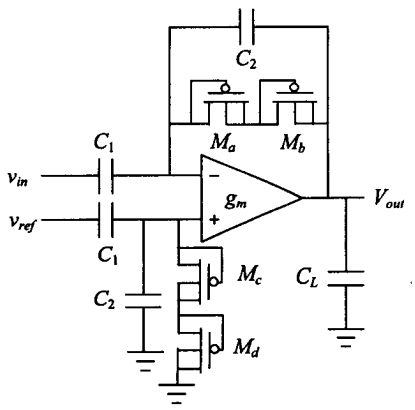

Figure 1: Schematic of neural amplifier.

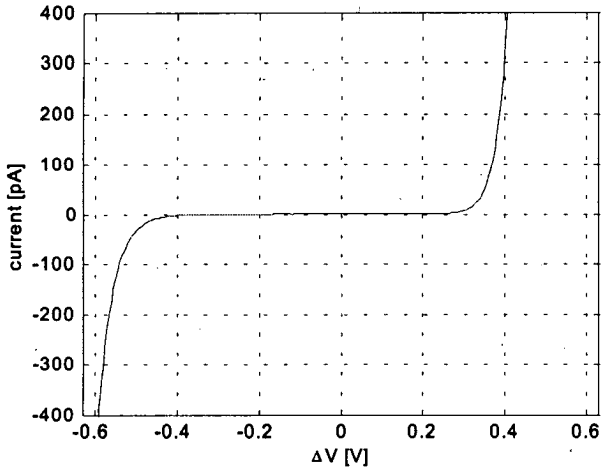

Figure 2: Measured current-voltage relationship of MOS-bipolar element (M_a-M_d in Figure 1). For low voltages, the incremental resistance exceeds $10^{10}\Omega$. See also [10].

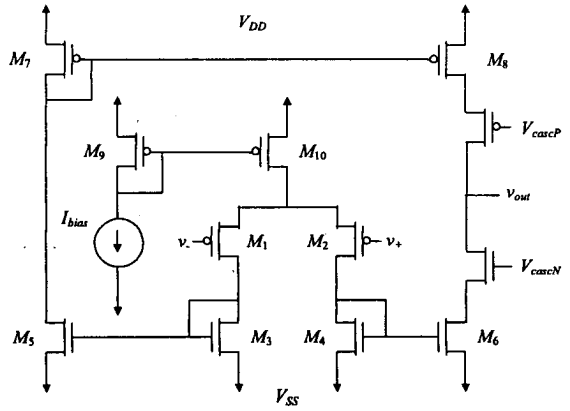

Figure 3: Schematic of operational transconductance amplifier (OTA) used in neural amplifier.

Figure 3 shows a schematic of the OTA used in the bioamplifier. Although the circuit topology is a standard design suitable for driving capacitive loads, the sizing of the transistors is critical for achieving low noise at low current levels. The bias current is set to 8μA, and the transistors may operate in either weak or strong inversion depending on their W/L ratio.

Note that transistors M_1-M_8 have the same dc drain current. The input devices M_1 and M_2 are drawn with identical sizes, and we denote their transconductance as g_{m1} and their width-to-length ratio as $(W/L)_1$. Similarly, Transistors M_3-M_6 are the same size $(W/L)_3$ and have transconductance g_{m3}. The pMOS current mirror transistors M_7 and M_8 have size $(W/L)_7$ and transconductance g_{m7}.

Analysis of this circuit reveals the input-referred thermal noise power to be

$$\overline{v_{ni,\text{thermal}}^2} = \frac{8kT\gamma}{g_{m1}}\left[1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right] \qquad (1)$$

If we size our devices such that g_{m3}, $g_{m7} << g_{m1}$, we can minimize the noise contributions of devices M_3-M_8. This can be accomplished by making $(W/L)_3$, $(W/L)_7 << (W/L)_1$, thus pushing devices M_3-M_8 into strong inversion where their relative transconductance g_m/I_D decreases as $1/\sqrt{I_D}$.

In practice, we cannot decrease g_{m3} and g_{m7} arbitrarily without danger of instability. If the total capacitance seen by the gate of M_3 (or M_4) is C_3, then the OTA has two poles at $\omega_p = g_{m3}/C_3$. Similarly, there is a pole at g_{m7}/C_7 caused by the pMOS mirror. To ensure stability, these pole frequencies must be several times greater than the dominant pole, g_{m1}/C_L. This criterion becomes easier to satisfy as C_L is made larger, so it becomes necessary to consider area limitations and bandwidth requirements. We decreased $(W/L)_3$ and $(W/L)_7$ as much as possible, trading off phase margin for lower input-referred noise.

All transistors must be made as large as possible to minimize $1/f$ noise. However, as devices M_3-M_8 are made larger, C_3 and C_7 increase, leading once again to a reduced phase margin. As M_1 and M_2 are made larger, the OTA input capacitance increases. This increase in C_{in} reflects more of the OTA noise to the bioamplifier input, so an optimum size must be found [11].

Since we are interested in minimizing noise within a strict power budget, we must consider the tradeoff between power and noise. The noise efficiency factor (NEF) introduced in [5] quantifies this tradeoff:

$$\text{NEF} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot \text{BW}}} \qquad (2)$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total amplifier supply current, U_T is the thermal voltage kT/q, and BW is the amplifier bandwidth. An amplifier using a single bipolar transistor (with no $1/f$ noise) has an NEF of one; all practical circuits have higher values.

Substituting the expression for amplifier thermal noise (1) integrated across the bandwidth BW into (2) and assuming g_{m3}, $g_{m7} << g_{m1}$, we find

$$\text{NEF} = \sqrt{\frac{2\gamma I_{tot}}{U_T g_{m1}}} = \sqrt{\frac{8\gamma}{U_T}\left(\frac{I_{D1}}{g_{m1}}\right)}$$

where I_{D1} is the drain current through M_1, which is one fourth of the total amplifier supply current. From this expression, it is clear that if we wish to minimize the NEF, we must maximize the relative transconductance g_m/I_D of the input devices M_1 and M_2. In weak inversion, g_m/I_D reaches its maximum value of κ/U_T, so we make $(W/L)_1$ very large to ensure subthreshold operation with microamp current levels. Using a more accurate model for thermal noise valid in weak inversion [12] yields

$$\text{NEF} = \sqrt{\frac{4}{\kappa U_T}\left(\frac{I_{D1}}{g_{m1}}\right)}$$

where κ is the subthreshold gate coupling coefficient.

In weak inversion, the expression for NEF reduces to

$$\text{NEF} = \sqrt{\frac{4}{\kappa^2}} \cong 2.9 \qquad (3)$$

assuming a typical value of $\kappa = 0.7$. This is the theoretical NEF limit for an amplifier with this circuit topology constructed from MOS transistors. In practice, the NEF will be limited by constraints on g_{m3} and g_{m7} as discussed above, and by $1/f$ noise.

3. EXPERIMENTAL RESULTS

We fabricated the amplifier in a 1.5μm 2-poly commercially-available CMOS process. We designed the amplifier for a gain of 100, setting C_1 to 20pF and C_2 to 200fF. Figure 4 shows the measured amplifier transfer function from 0.7Hz to 50kHz. The midband gain is 39.5dB, which is slightly lower than our design specification of 40dB. This discrepancy is likely caused by fringing fields on the small C_2 capacitors, yielding a larger capacitance than drawn. Figure 5 shows the output of the amplifier in response to a 0.006Hz square wave. (Note that the time scale is in units of seconds.) Based on the slow adaptation of the output, we estimate the low-frequency cutoff f_L to be approximately 0.1mHz.

Figure 6 shows the measured input-referred noise power spectral density (PSD). The thermal noise power is $21\ \text{nV}/\sqrt{\text{Hz}}$ and the $1/f$ noise corner occurs at 100Hz. Integration under this curve yields an rms noise voltage of 2.2μVrms. This noise measurement was confirmed by recording the output noise waveform and dividing by the gain to generate an input-referred noise waveform whose rms value is 2.2μVrms (see Figure 7).

Table I summarizes these and other measurements along with simulation results. Our simulated noise levels exceeded measurement due to conservative estimates of $1/f$ noise coefficients. The NEF of our amplifier is 4.0, which is near the theoretical limit of 2.9 calculated in (3).

Distortion stays below 1% THD for inputs less than 16.7mV peak-to-peak (larger than typical extracellular neural signals). If we calculate dynamic range assuming a distortion limit of 1% (a conservative definition), our dynamic range is 69dB. Crosstalk was measured between amplifiers adjacent on the chip, and was -64dB or less.

Figure 8 shows the power-noise performance of our amplifier compared with estimated NEF values from previously published bioamplifiers [1]–[9]. The amplifier presented here exhibits a better NEF than existing designs.

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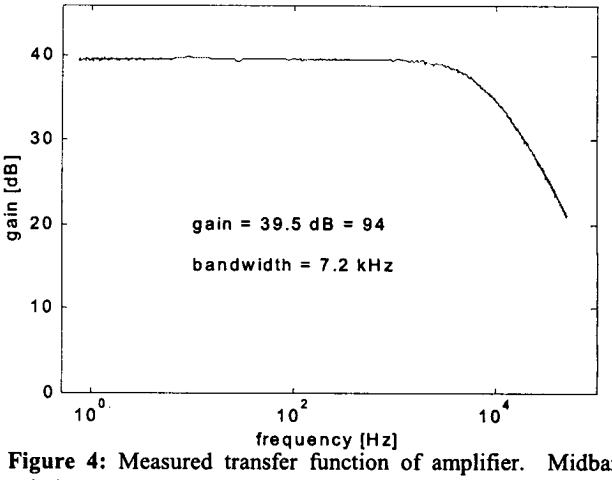

Figure 4: Measured transfer function of amplifier. Midband gain is 39.5dB, and single-pole roll-off occurs at 7.2kHz.

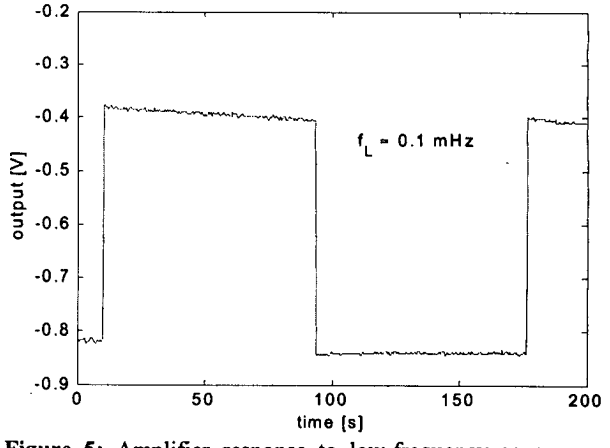

Figure 5: Amplifier response to low-frequency square wave. Based on the decay, we estimate the high-pass cutoff frequency f_L to be approximately 0.1mHz. Note time scale is in seconds.

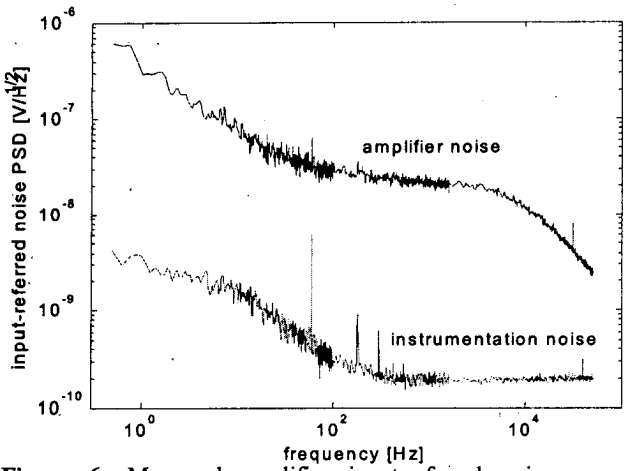

Figure 6: Measured amplifier input-referred noise power spectral density. Integration under this curve yields an rms noise voltage of 2.2μVrms.

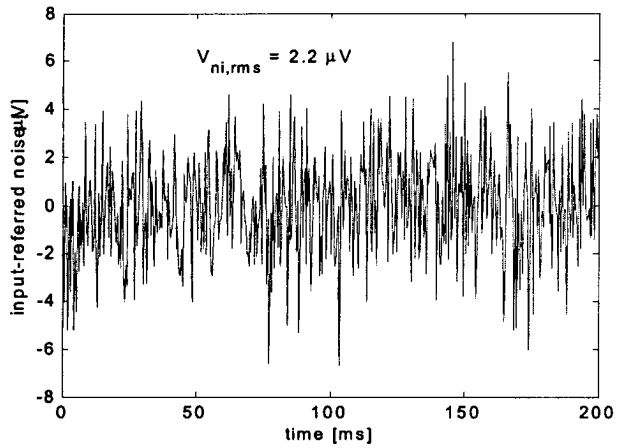

Figure 7: Measured amplifier input-referred noise (i.e., output noise divided by amplifier gain). The rms value is 2.2μV, which agrees with the noise PSD measurements in Figure 7.

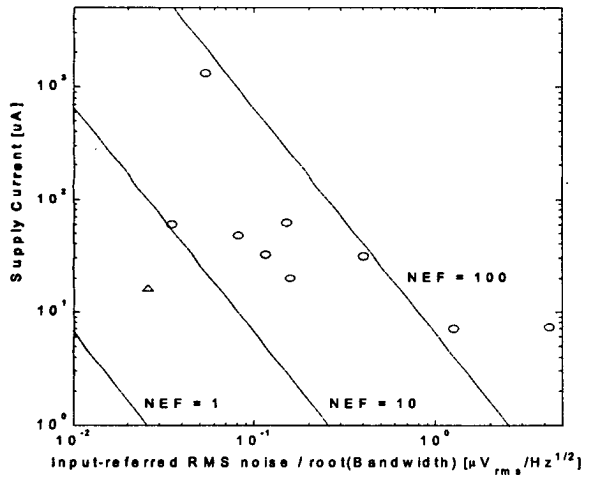

Figure 8: Supply current vs. normalized noise for amplifiers in [1]–[9] (circles) and the amplifier described in this paper (triangle). Lines indicate constant NEF contours.

TABLE I
SIMULATED AND EXPERIMENTAL CHARACTERISTICS OF AMPLIFIER

Parameter	Simulation	Measured
Supply voltage	±2.5 V	±2.5 V
Supply current	16 μA	16 μA
Gain	40 dB	39.5 dB
Bandwidth	7.5 kHz	7.2 kHz
Low-frequency cutoff	130 mHz	~0.1 mHz
Input-referred noise	3.1 μVrms	2.2 μVrms
Noise efficiency factor	5.6	4.0
THD (16.7 mVpp input)	not measured	1.0%
Dynamic range (%1 THD)	not measured	69 dB
CMRR (10 Hz – 5 kHz)	≥ 42 dB	≥ 83 dB
PSRR (10 Hz – 5 kHz)	≥ 42 dB	≥ 85 dB
Crosstalk (f = 1 kHz)	not measured	-64 dB
Area (in 1.5μm technology)	n/a	0.16 mm^2

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