Depth dependent carrier density profile by scanning capacitance microscopy

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The depth dependent carrier density was measured on an arsenic implanted silicon sample using scanning capacitance microscopy (SCM). The capacitance versus voltage scan was performed by applying dc biases with a dither ac signal. A strong dc bias dependence was observed at the interface of an abrupt junction between n^+ and p. The bias dependent SCM images show good agreement with quasi-three dimensional simulations, suggesting that they can be used to map a device structure. © *1997 American Institute of Physics.* [S0003-6951(97)03537-7]

With the recent developments in silicon submicrometer technology, the characterization of the three dimensional carrier density profile in a device has become one of the most important issues. For example, in a complementary metal oxide semiconductor (CMOS) device, it is difficult to make the gate channel length less than 0.1 μm. It is even more difficult to measure the carrier density profile around the gate directly because many tools only measure the profile averaged over a large area. Secondary ion mass spectrometry (SIMS) and spreading resistance profilometry (SRP) have been widely used to measure dopant profiles. The tomographic approach[1] and the angle lapping technique[2] have been developed to measure two dimensional profiles with improved resolution. Recently nano-SRP, utilizing scanning probe microscopy, has further improved spatial resolution.[3–5]

Since the advent of the scanning tunneling microscope (STM) and the atomic force microscope (AFM), the geometrical and electrical measurements of a semiconductor surface have become possible with atomic resolution. As a probe is scanned over a specific area while regulating the probe/sample gap (d_{PS}) using the atomic force or tunneling current, the carrier density profile,[6] the potential across abrupt junctions,[7] the impurity distribution,[8] and the carrier scattering near defect centers[9] can be measured at the same time. The carrier density of a semiconductor can be mapped by the capacitance-voltage ($C-V$) dependence, while the geometrical structure can be measured by STM or AFM. In order to have a good spatial resolution, the sensitivity of the detector has to be better than 10^{-19} F.[10] The scanning capacitance microscope (SCM) can be operated under ambient conditions using a sample with only a capping oxide without any further extensive sample preparation. However, it only measures the carrier density rather than the dopant concentration of the semiconductor surface. If the dopant density does not vary abruptly within a few Debye lengths, it can be estimated from the measured $C-V$ dependence.[11] In an earlier SCM, the capacitance signal was fed back to control d_{PS}, achieving a 25 nm lateral resolution.[10] The SCM was able to detect the small variations in capacitance even at highly doped regions by sensing the depletion modulation.[12] The carrier density profile at one point and the two dimensional (2D) map at a fixed bias were measured, showing good agreement with SIMS results within the dopant range of $10^{17}-10^{20}$/cm^3.[13–17] The dopant profile could be estimated by comparing the measured $C-V$ dependence with the SIMS result. In this work, by measuring the $C-V$ dependence at every point, dc voltage dependent capacitance images, which are similar to a quasi-3D carrier density profile, can be obtained. The measured dc bias dependent images were compared with the simulated result.

The SCM used in this study is similar to the one previously described.[12–17] Briefly, a contact mode AFM using the beam deflection method was used. An RCA video disc sensor that operates at 915 MHz was used to detect the capacitance signal. This high frequency enables us to detect a relative capacitance variation of less than 10^{-18} F.[18] The tip used was first coated with 50-nm-thick Ti (or Cr) by e-beam evaporation and annealed shortly before being attached to the capacitance sensor. A dc bias (-5–5 V) with an ac modulation (mainly 20 mV$_{pp}$, 50 kHz) was applied to the sample to obtain the $C-V$ dependence. It was found either by experiment or by circuit simulation that with the ac modulation more than 90% of the dc bias can be applied to the sample. Since the resistance of a semiconductor sample is inversely proportional to the carrier density, the applied dc bias voltage should be rescaled by considering the carrier density (substrate resistance) and the oxide thickness (oxide resistance). The capacitance signal measured by the RCA sensor was fed into a lock-in amplifier and recorded by a computer. The measured signal sensitivity (5 μV) was large enough to scan at the rate of 1.25 s/line. Since the force between the probe and sample was regulated by the AFM, the topographic and capacitance images can be obtained si-

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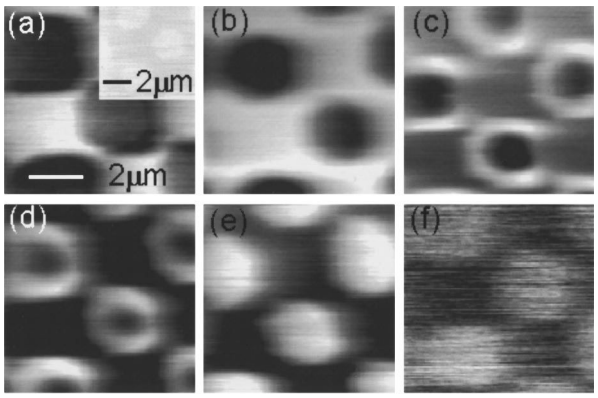

FIG. 1. Capacitance images which depend on the sample biases with grounded tip (a) sample bias $V_s=+1.3$ V and topography (inset), (b) +0.9 V, (c) +0.4 V, (d) +0.3 V, (e) −0.15 V, (f) −0.7 V, 7×7 μm^2.

multaneously. The sample used was a p-type Si substrate (boron doped, $10^{15}/cm^3$). With an oxide mask, arsenic with the dose of $2\times10^{13}/cm^2$ was implanted at 40 keV energy. The sample was then annealed at 950 °C subsequently under N_2 ambient. Finally, the oxide mask was removed and a 25 nm gate oxide was grown for the capacitance measurement.

Figure 1 shows bias dependent derivative capacitance images scanned over 7×7 μm^2. Since an array of circular masks was used, arsenic was mainly implanted only outside the circular patterns (lateral straggle should be considered in strict sense). The topography shows a height difference of less than 3 nm between the circles, even after removing the mask oxide [inset in Fig. 1(a)]. This could be due to the different etching rates when the oxide mask was removed by hydrofluoric acid. The contrast in the derivative capacitance images comes from the spatial variation of the dC/dV at a given dc bias. A dark edge ring appeared on the unimplanted area at a positive sample bias [Fig. 1(a)], then the ring got brighter with decreasing the sample bias [Figs. 1(b) and 1(c)]. The width was broadened toward the center of circle [Fig. 1(d)] and the ring disappeared at −0.15 V [Fig. 1(e)]. The image contrast between two areas was too low to image clearly at <-0.7 V [Fig. 1(f)]. Since the active region of a device is often depleted even at zero bias, it is difficult to measure the impurity concentration within the depletion layer with SCM. This can be overcome by varying the applied dc bias controlling the depletion width. This method can show the carrier distribution of a real device under the operating voltage. Therefore the images in Fig. 1 are quite different from the 2D SCM results on a cleaved sample surface. Thus the present image inversion and edge effects are due to a true 3D effect caused by varying the depletion width.

High frequency dC/dV-V dependence at one point in Fig. 2 is very similar to earlier results[11,19] for a large area contact. The slight deviation from the ideal nonequilibrium dC/dV-V curve may be caused by the excess carriers generated in the depletion region from the scattered laser light in AFM. The carriers can move out of that region before recombination caused by the field produced by the built-in potential of the pn junction or by the externally applied bias.[19] Humidity, mobile ions on the surface, immobile charges trapped in the oxide may make shunt paths, or a

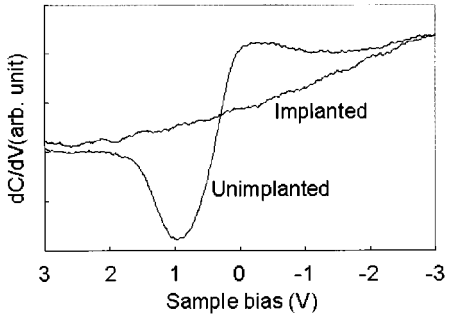

FIG. 2. High frequency dC/dV-V characteristic curve ranged from $V_s=3$ V to −3 V (considering the tip as a gate, the voltage is varied from accumulation to inversion as usual. Therefore plus sign at sample bias is same as minus at gate bias).

local high electric field resulting in a deviation. As the probe moves away from the junction edge to the unimplanted region, the measured curve shifts to the right with little change of its shape. The curve of the implanted area keeps nearly the same shape irrespective of the tip position. The image contrast can then be inverted at a fixed bias and an edge ring appears as in Fig. 1.

At present, there are no proper simulation packages by which a 3D $C-V$ dependence under a nonequilibrium condition can be calculated. We have modified the TSUPREM-4 and MEDICI packages to explain our results.[20] The depletion layers for various probe/sample biases were calculated in a cross sectional plane along the ZZ' direction as shown in Fig. 3(a). The edge of the dark area denotes a line of equal arsenic and boron dopant concentration. By scanning a 50-nm-wide simulated rectangular shaped electrode along the ZZ', the depletion lines were calculated. The lines of depletion were drawn at the position where the density of the majority carrier (hole) is half. Figure 3(b) shows a character-

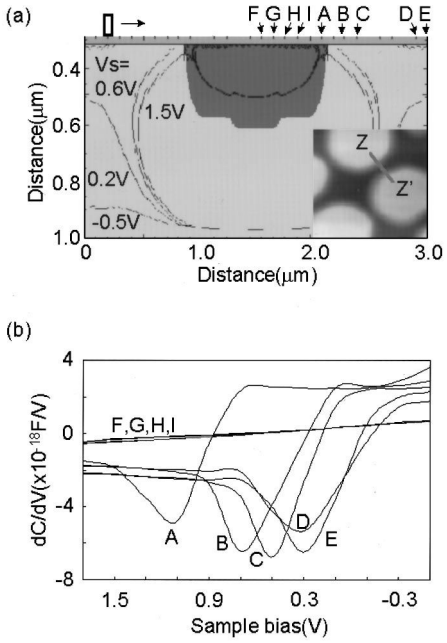

FIG. 3. Depletion layers formed by scanning with the 50-nm-wide rectangular electrode calculated by TSUPREM-4 in 2D (a), and one dimensional dC/dV-V characteristic curve calculated at marked points of (a) with MEDICI (b).

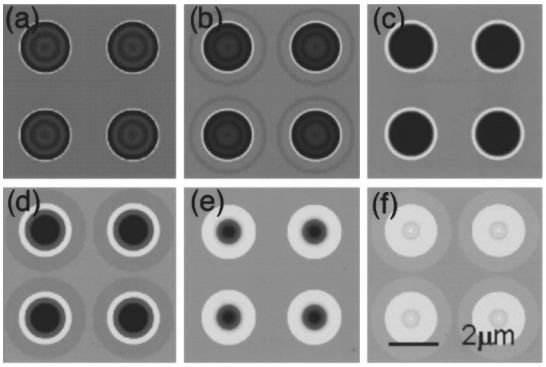

FIG. 4. Simulated capacitance images after 2D calculation by MEDICI (a) $V_s=+1.3$ V, (b) $+1.1$ V, (c) $+0.7$ V, (d) $+0.5$ V, (e) $+0.3$ V, (f) -0.1 V.

istic 1D dC/dV-V curve calculated at the marked points of Fig. 3(a). The series resistance effect of the inversion layer[11] with a depleted capacitance was considered. As an electrode moves from A to E, the curve shifts to the right but as it moves from F to I (implanted area), it is nearly unchanged. Thus the image at the sample bias of -0.1 V will look like an inverted one at 1.3 V while a bright edge ring appears at $\sim$ 0.5 V. The derivative capacitance images were calculated by the process simulation assuming that this system has a rotational symmetry about the center of the oxide mask as shown in Fig. 4. This is in good agreement with the experimental results only with a shift of 0.2 V of the $C-V$ dependence in the accumulation region of the unimplanted area. This may be caused by the previously described deviations in dC/dV-V from the ideal one. At highly doped implanted areas this effect is negligible, but at unimplanted areas this effect gives similar results to that of hole injection caused by applying a positive bias to the sample. The image calculation can be refined further by considering realistic probe-sample geometries.[16]

Quasi-3D information of the impurity profile was measured by the position dependent dC/dV-V. Inversion of the image contrast was observed with the applied sample bias. These results agree well with a quasi-3D simulation. The applied bias is not only a function of the carrier density of the sample but also of the circuit parameters of the sensor. Therefore one has to take this into account when comparing the measured data with the calculated results. An improved simulation scheme to interpret the measured results is demanded.

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[20] Computer code TSUPREM-4 and MEDICI (Technology Modeling Associates, Inc. 595, Lawrence Expressway, Sunnyvale, CA 94086-3922, versions 6 and 2.1, respectively).