TOTAL IONIZING DOSE CHARACTERIZATION OF A COMMERCIALLY FABRICATED ASYNCHRONOUS FFT FOR SPACE APPLICATIONS*

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ABSTRACT

The total ionizing dose characterization of the radiation-hardened implementation of a novel architecture for high-performance, energy efficiency FFT engines is presented. Simulations and test chip measurement results indicate that a radiation-tolerant 1024-point FFT based on this architecture will achieve an efficiency of 120 nJ/Unit-Transform and 2 μs throughput. The proof-of-concept chip shows a total ionizing dose hardness of 1 Mrad (SiO_2).

INTRODUCTION

Digital signal processing (DSP) is an essential function for a majority of military and commercial space platforms. Various DSP and general-purpose processors are available and typically used for this purpose. One of the most common DSP functions is the Fast Fourier Transform (FFT). The Air Force has developed a specific architecture for designing high-performance, energy efficient FFT integrated circuits (ICs) [1]. Simulation data indicates that a 1024-point FFT based on this architecture has a predicted efficiency of 120 nJ/Unit-Transform and 2 μs throughput [2]. A subset of this architecture was implemented in a proof-of-concept chip that was fabricated on a commercial process using a hardened-by-design gate array [3]. The proof-of-concept chip has clearly demonstrated a total ionizing dose hardness well beyond 1 Mrad (SiO_2).

BACKGROUND

The Air Force received a patent on an asynchronous, pipelined FFT architecture for implementing energy-efficient high-performance FFT designs in 1997 [1]. We present a proof-of-concept FFT test chip demonstrating a subset of this architecture designed at the Air Force Institute of Technology (AFIT) as part of a thesis effort sponsored by the Air Force Research Laboratory (AFRL) [2]. The design of the proof-of concept chip was limited to a four-point FFT (FFT-4) with a fixed-point data path of 16-bits for each data word in the complex domain.

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The FFT-4 was fabricated on the Hewlett-Packard 0.5 µm (gate oxide thickness of 9.4 nm) commercial CMOS process through MOSIS using a hardened-by-design (HBD) gate library that has been demonstrated and characterized previously [3]. This HBD approach is based on the use of annular transistors and guard bands, among other hardening approaches, as shown in Figure 1.

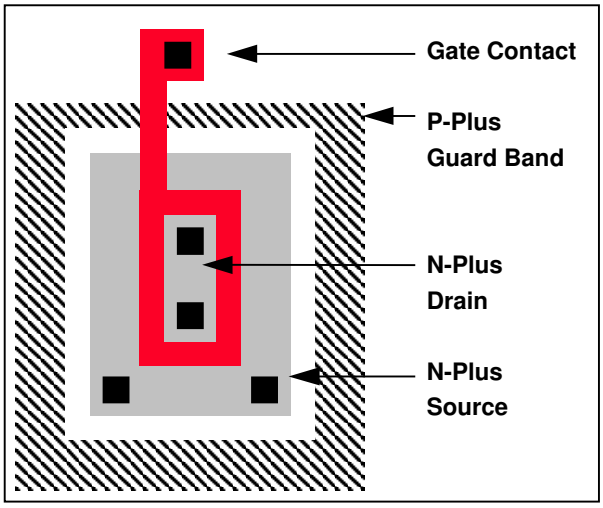

Figure 1. Simplified schematic of a re-entrant n-type transistor [3]

The HBD approach offers numerous benefits with a sacrifice in area. The re-entrant n-type transistor eliminates the edge leakage phenomenon observed in commercial CMOS circuits in a total ionizing dose (TID) radiation environment, which is the predominant failure mechanism. Guard bands are used to eliminate the inter-transistor leakage associated with the oxide charging under the field oxide between adjacent transistors. The guard bands, in conjunction with proper transistor spacing, serve to suppress single event latchup (SEL) by eliminating the parasitic transistor. The single event upset (SEU) energy threshold is raised by utilizing properly ratioed high drive strength transistor pairs. [2][3]

The primary motivation for this approach is to leverage the affordability and availability of commercial foundries while achieving a circuit hardened to total ionizing dose and single event effects. However, this particular gate array design, including the annular transistor and guard bands, suffers a factor of four area penalty. [3]

Initial performance characterization of the FFT-4 reveals an efficiency of 36 nJ/Unit-Transform and a transform throughput of 380 ns. Previous simulations of the FFT-4 predicted an efficiency of 4.25 nJ/Unit-Transform and a throughput of 180 ns [2]. The substantial performance discrepancy between simulation results and device measurements is readily justified. The simulation results did not include the delays and power consumption of the input and output pads or the capacitive losses from the test chip packaging. In a larger system these losses will not be realized since the FFT engine will be part of a larger DSP system and will be connected all on one die. Additional simulation results indicate that a full FFT-1024 based on this architecture has a projected efficiency of 120 nJ/Unit-Transform and a throughput of 2 µs [2]. Comparing this performance data to other *unhardened* commercial and research based DSP devices reveal a significant performance advantage as illustrated in Figure 2.

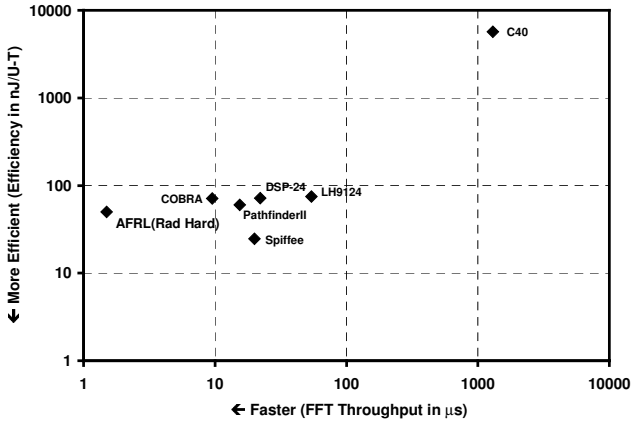

Figure 2. FFT Performance Diagram

Table 1 summarizes performance details for each FFT engine listed in Figure 2. An FFT implemented with unhardened library cells

using this architecture would have an even greater efficiency.

Table 1. FFT Comparison Table

Processor	Design Feature	Dataword Size & Type	V_{SS} (V)	FFT-1024 through-put(µs)	FFT-1024 Efficiency (nJ/U-T)
Air Force	**Rad-Tolerant Research FFT**	**16-bit Fixed Point**	**3.3**	**2**	**120**
DSP-24 [5]	Unhardened Commercial DSP	24-bit Fixed Point	3.3	22	71.8
TI C40 [6]	Unhardened Commercial DSP	32-Bit Floating Point	5.0	1298	5704
Spiffee [7]	Unhardened Research FFT	20-bit Fixed Point	3.3	30	24.7
COBRA [8]	Unhardened Research FFT	23-bit Fixed Point	5.0	9.5	71.4
LH9124 [9]	Unhardened Commercial DSP	24-bit Fixed Point	5.0	54	75
PathfinderII [10]	Unhardened Commercial DSP	32-bit Floating Point	3.3	15.4	60

There are several benefits of using the Air Force s FFT architecture. This architecture uses a pipelined approach, reduces global data and control bus structures and requires no shared memory. Computation of the top-level FFT is executed through a combination of smaller FFTs and complex multipliers. To conserve energy, the entire design is implemented in an asynchronous fashion, which uses local handshaking between functional blocks, thereby eliminating inefficient global clock circuitry [4].

TOTAL IONIZING DOSE EVALUATION

The FFT-4 was evaluated for its total ionizing dose response to 20 KeV (average energy) X-rays at the Low-Energy X-Ray (LEXR) facility and to high energy Gamma radiation at the large area Cobalt-60 (Co-60) source. Five FFT-4 devices were evaluated at each source. Both evaluations adhered to the guidelines set forth in MIL-STD-883, Test Method 1019.5. Each source used the same device under test (DUT) board and biasing technique to ensure the worst-case bias condition of the FFT-4. A pre-irradiation electrical performance baseline was taken for all devices immediately prior to irradiation. One FFT-4 irradiated at each radiation source was annealed under bias for 168 hours at 100 °C after the final radiation exposure.

The AFRL LEXR facility is a room cell containing a Philips X-ray tube, model MCN-165. The beam is filtered by a 0.002" Al sheet placed 10.0 cm from the source to suppress the very low energy X-ray spectrum and is collimated with a 0.500" lead hole collimator. Dosimetry was accomplished at 25.0 cm from the source using an ARACOR PIN diode, model number CS-1003. For this characterization, a dose rate of 92.95 rad(SiO_2)/sec was achieved at a distance of 25.0 cm from the source for a X-ray tube voltage of 50 kV and a current of 10 mA. The dose rate is specified in rad(SiO_2) due to the fact that Si and SiO_2 have different scaling factors for energy deposition depending on the photon energy. At 20 keV, the theoretical energy deposition ratio (Si/SiO_2) is approximately 1.8. [11]

The AFRL Co-60 facility is a panoramic room cell containing a J.L. Shepherd Type 7810 Co-60 source. The DUT assembly was enclosed in a lead-aluminum box to eliminate the low energy photons resulting from back-scattering. Dosimetry was accomplished by a Rad-Cal Model 2025 ion chamber dosimeter. A dose rate of 92.3 rad(SiO_2)/sec was measured at the DUT at a distance of 8.0 cm from the source.

The DUT board used was compatible with the Hewlett-Packard 82000 integrated circuit evaluation system. The DUT board has provisions for biasing the FFT-4 during irradiation. Bias power was continuously supplied either through a hard wired power supply during irradiation or a battery during transport between the HP 82000 and the radiation source. The voltage on the board and current flowing through the FFT-4 was monitored during each irradiation. The HP 82000 was programmed to evaluate the FFT chip with a suite of test vectors to verify functionality, maximum operating frequency, operating current, standby current and input leakage current. Before each irradiation, the FFT-4 was initialized with an input sequence. Upon the completion of the irradiation, a corresponding

output sequence was read from the FFT-4 to ensure that there were no data upsets and that the circuit remained under bias throughout the irradiation.

The results of the total ionizing dose evaluation indicate that there are no measurable changes to the FFT-4 s performance until a level of 250 krad(SiO_2) is reached. After that point, a very shallow degradation takes place until the end of the evaluation, which was at 1.5 Mrad(SiO_2). At that point, the operating current only increased to a maximum of 4 mA (3.5%) above the nominal value, depending on the DUT. Figure 3 reveals an increase of the operating current in response to the total dose in the LEXR. Figure 4 shows the operating current response in the Co-60. Note that the baseline operating current of most DUTs was 115 mA, however a few DUTs had a baseline of 117 mA. This type of variance is typical in a process run from MOSIS and the values are all within 2% of each other, which is actually quite exceptional.

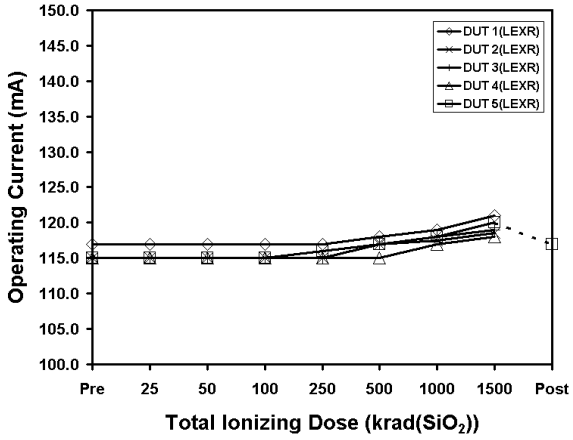

Figure 3. Response of Operating Current to TID (LEXR)

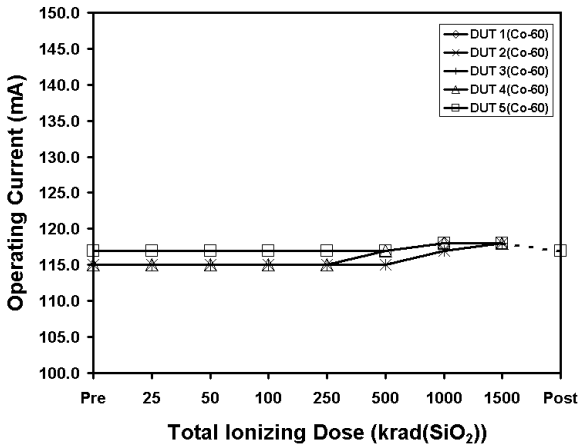

Figure 4. Response of Operating Current to TID (Co-60)

The other key parameter that was measured during the evaluation was the critical path lengthening. Due to the fact that the circuit is not a traditionally clocked (synchronous) circuit, there is no clock frequency that can be adjusted to compensate for slower operation of the circuit. The computational speed of the asynchronous FFT-4 is based on the input data. Therefore, to determine if there was any slowing of the device, the longest computational cycle (critical path) was compared to the baseline performance after each exposure level. During the course of the evaluation, the critical path lengthened to a maximum of 4 ns above the normal value of 380 ns as shown in Figure 5 and Figure 6, for the LEXR and Co-60 sources, respectively.

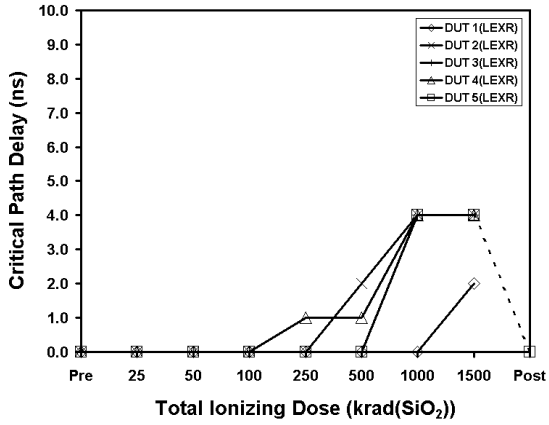

Figure 5. Critical Path Lengthening in Response to TID (LEXR)

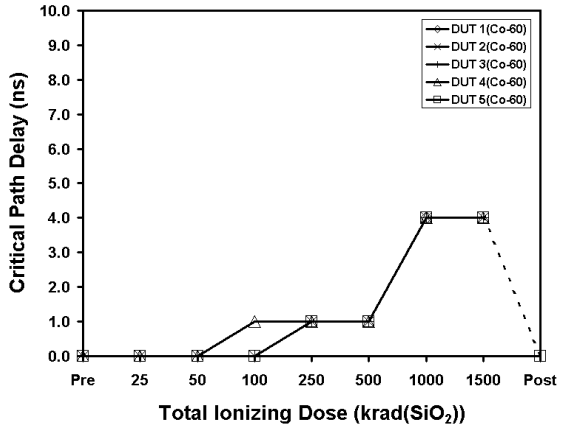

Figure 6. Critical Path Lengthening in Response to TID (Co-60)

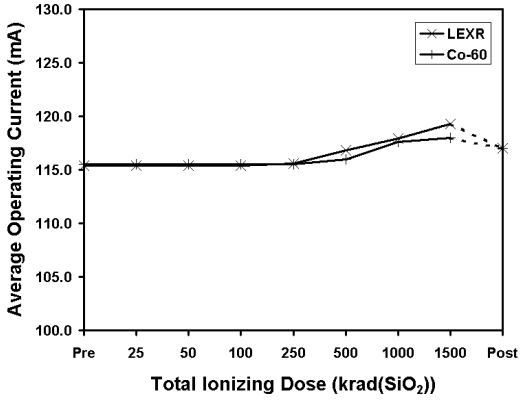

Figure 7. Comparison of Operating Current

The predominant degradation mechanism, which caused the increased leakage current in this case, is the leakage current through the field oxide caused by charge buildup. The slower response time is due to the build up of interface traps, which soften the response of both transistor types. HBD techniques can only minimize these phenomena—they cannot eliminate them entirely.

A secondary purpose of this study was to further investigate the claim that a low-energy X-ray source can be used to approximate the results that are seen in a gamma radiation source in complex CMOS circuits. To compare results from each source, the results from each source were averaged and then compared. Figure 7 compares the response of the operating current in each source. Figure 8 compares the lengthening of the critical path. The response in each source for both parameters is nearly identical.

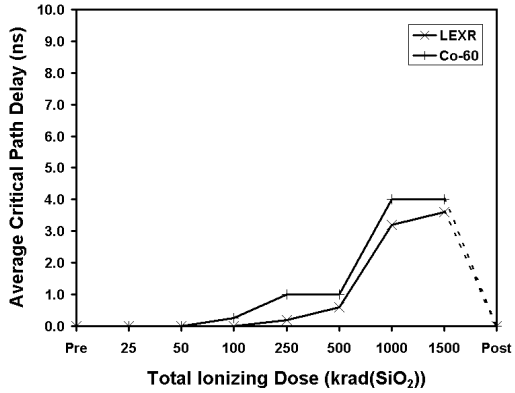

Figure 8. Comparison of Critical Path Delay

FUTURE EFFORTS

The design of an FFT-16 and FFT-64 based on similar design principles used in the design of the FFT-4 has been completed. The FFT-16 will be fabricated on the Massachusetts Institute of Technology/Lincoln Laboratory 0.18 μm, fully depleted, silicon-on-insulator (SOI) line using a HBD gate array. It is expected, that the smaller feature size along with the reduced capacitance of the SOI fabrication process will further enhance the efficiency and throughput of the FFT. In addition, packaging and I/O efficiency losses will become less of a factor due to the circuit area becoming the dominant structure in comparison to the I/O structure. A full radiation environment characterization of the FFT-16 will be accomplished and published. The FFT-64 is the last major building block in the implementation of an FFT-1024. The design

and fabrication of the FFT-1024 is scheduled to take place by the end of 2000.

SUMMARY AND CONCLUSIONS

The design of the Air Force s FFT architecture is presented. The asynchronous nature of the design has enabled high efficiency and throughput, which yields a significant performance improvement over commercial *unhardened* DSP designs. The total ionizing dose response is minimal up to 1 Mrad (SiO_2) for both the low-energy X-ray source and the Co-60. This research is paving the way for the next generation of high performance DSPs for space applications.

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