A WIDE-LINEAR-RANGE SUBTHRESHOLD CMOS TRANSCONDUCTOR EMPLOYING THE BACK-GATE EFFECT

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ABSTRACT

We present a CMOS circuit that utilizes the back-gate effect to extend the linear range of a subthreshold MOS transconductor. Previous designs of wide-linear-range transconductors using bipolar transistors employed multiple differential pairs with input offset voltages used to shift the individual transfer functions. These voltages were chosen to maximize the linear range of the summed differential pair currents. Equivalent offset voltages were generated by sizing emitter areas appropriately. Similar techniques may be applied to MOS circuits by scaling *W*/*L* ratios, but transistor size increases exponentially as we extend the linear range by adding more differential pairs. We introduce a method of adding equivalent offset voltages by biasing the back gate (i.e., body) of well devices appropriately. Test circuits built in a standard 0.5μm CMOS process and using few transistors exhibit improved linear range over standard single-differential-pair transconductors.

1. INTRODUCTION

Transconductors built from MOS transistors operating in weak inversion suffer from limited linear range in the same way as transconductors built from bipolar transistors. The reason is the same: a high g_m/I ratio. For a bipolar transistor, $g_m/I_C = 1/U_T$, where U_T is the thermal voltage kT/q. For a subthreshold MOS transistor, $g_m/I_D = \kappa/U_T$, where κ is the subthreshold gate coupling coefficient typically having a value between 0.6 and 0.8.

Several circuits have been proposed for building wide-linear-range transconductors from either bipolar [1], [11] or subthreshold MOS [2]–[6], [9] transistors. In this paper we present a subthreshold MOS transconductor that achieves wide linear range by employing multiple differential pairs and using the back gate (i.e., body effect) to shift the operating point of each differential pair. Previous work has also taken advantage of the reduced transconductance of the back gate [5], [9], [10].

2. TRANSCONDUCTOR DESIGN

2.1. Circuit topology

Our circuit is based on linearization technique employed by Tanimoto et al. for bipolar circuits [1]. Multiple differential pairs are tied together so that their output currents sum, effectively adding their transfer functions (see Figure 1). Inputs are identical except for an offset voltage that is applied to certain transistors. These offset voltages serve to shift the transconductance curve of a particular differential pair away from zero. The proper choice of offset voltages (e.g., V_1 and V_2 in Figure 1) and current scaling factors (e.g., β, α_1, and α_2 in Figure 1) superimposes individual diff-pair transfer functions in a way that maximizes linear range.

Tanimoto and colleagues derived optimal values for β and α_N analytically for circuits with small number of differential pairs. For larger circuits, numerical optimization techniques may be used. Our numerical optimizations indicate that as the number of differential pairs grow large (e.g., greater than 10), the current scaling factors become very similar (i.e., $\beta = \alpha_1 = \alpha_2 = \ldots$) and the offset voltages are evenly spaced (i.e., $V_1 = \Delta V$, $V_2 = 2\Delta V$, $V_3 = 3\Delta V$, ...).

2.2. Circuit design

In practical circuits, it is not feasible to build floating voltage sources to provide offset voltages, so the emitter area of the transistor is resized to create an equivalent offset voltage at the input. This technique may be applied to subthreshold MOSFETs as well by scaling the *W*/*L* ratio. However, the required *W*/*L* ratio (or emitter area ratio) grows exponentially with offset voltage. In weak inversion, the drain current of an *n*MOS transistor is given by

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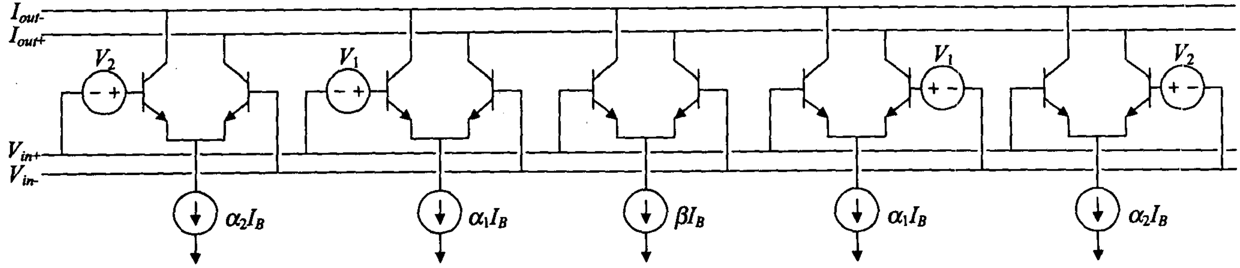

Figure 1: Linearization technique employed by Tanimoto et al. Figure adapted from [1].

$$I_D = I_{S1} \cdot \frac{W}{L} \cdot \exp\left(\frac{\kappa(V_{GB} - V_T) - V_{SB}}{U_T}\right) \quad (1)$$

where V_{GB} is the gate-to-body voltage, V_{SB} is the source-to-body voltage, V_T is the threshold voltage, and

$$I_{S1} = \frac{2\mu C'_{ox} U_T^2}{\kappa} \quad (2)$$

where μ is the carrier mobility and C_{ox}' is the gate oxide capacitance per unit area [7],[8].

Rewriting (1) and assuming $V_{SB} = 0$, we find

$$I_D = I_{S1} \cdot \exp\left(\frac{\kappa\left(V_{GB} - V_T + \frac{U_T}{\kappa}\ln\frac{W}{L}\right)}{U_T}\right) \quad (3)$$

Here, we have expressed the effect of the W/L ratio as an equivalent offset voltage $(U_T/\kappa)\cdot\ln(W/L)$ at the gate. The exponential dependence of transistor width with offset voltage is evident.

We may also achieve an equivalent gate offset voltage by setting $V_{SB} > 0$ and employing the back gate effect whereby the body potential influences the surface potential through the depletion capacitance [7]–[9]. We can rewrite (1) as

$$I_D = I_{S1} \cdot \frac{W}{L} \cdot \exp\left(\frac{\kappa(V_{GS} - V_T) + (1-\kappa)V_{BS}}{U_T}\right) \quad (4)$$

where the effect of the back gate voltage V_{BS} is evident. We can rewrite (4) to find the equivalent gate offset voltage produced by a particular value of V_{SB}:

$$I_D = I_{S1} \cdot \frac{W}{L} \cdot \exp\left(\frac{\kappa\left(V_{GS} - V_T - \frac{1-\kappa}{\kappa}V_{SB}\right)}{U_T}\right) \quad (5)$$

Of course, for an nMOS transistor in an n-well process the body must always lie at the substrate potential. However, we may use a pMOS transistor in an isolated well and modulate the well potential. Rewriting (5) for a pMOS device, we get

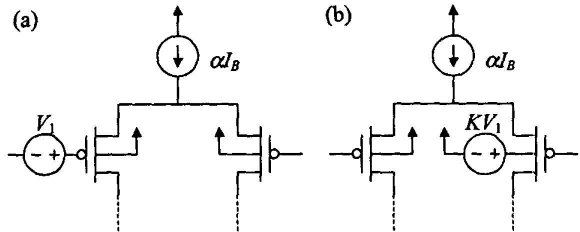

Figure 2: Adjusting equivalent gate voltage offset (a) by back gate offset (b).

$$I_D = I_{S1} \cdot \frac{W}{L} \cdot \exp\left(\frac{\kappa\left(-V_{GS} + V_T + \frac{1-\kappa}{\kappa}V_{SW}\right)}{U_T}\right) \quad (6)$$

where V_{SW} is the source-to-well potential, which must always be negative. Thus if we wish to create an equivalent gate offset voltage of V_{offset}, we must lower the well potential by KV_{offset}, where

$$K = \frac{1-\kappa}{\kappa} \quad (7)$$

For typical values of κ, K ranges from 0.18 to 0.43.

Figure 3 shows a wide-linear-range MOS transconductor using multiple differential pairs with offset voltages applied through the back gate (i.e., well). The circuit shown has 5 differential pairs (N = 5) biased symmetrically, producing gate-referred offset voltages equivalent to those shown in Figure 1. We have built the circuit for the "large N" case where our numerical experiments show the current sources to be nearly identical and the offset voltages to be spaced evenly (i.e., in multiples of ΔV) to maximize linear range.

All W/L ratios are identical, which results in a substantial area savings relative to the prior method of creating offset voltages by scaling W/L ratio. Of course, isolated wells must be used, and this adds to circuit area, but this is a fixed penalty unlike the exponential cost of W/L scaling shown in (3).

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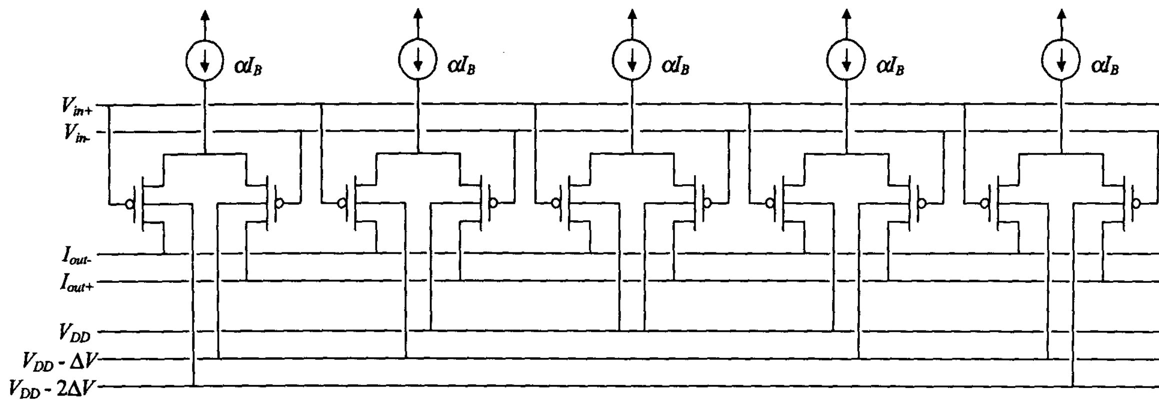

Figure 4: Wide-linear-range transconductor with multiple differential pairs using the back-gate effect to provide equivalent gate voltage offsets.

3. EXPERIMENTAL RESULTS

We fabricated the circuit in a commercially-available 0.5μm CMOS process. All transistors were drawn 3μm/1.2μm. The bias current for each differential pair was set to 100nA to ensure subthreshold operation. An on-chip *n*MOS current mirror was used to achieve a non-differential, bi-directional output current.

Figure 4 shows measured normalized transfer functions for both a single differential pair ($N = 1$) and our wide-linear-range transconductor with 11 differential pairs ($N = 11$) under three different biasing conditions: ΔV = 300mV, ΔV = 500mV, and ΔV = 650mV. Linear range appears to extend as we increase ΔV. Simulations indicate that if ΔV is made too large, the transconductance will exhibit ripples as the transfer function assumes a "stairstep" appearance.

Another limit to the magnitude of ΔV is the danger of forward-biasing the source-well junction in the outer differential pairs. For ΔV = 650mV, the lowest well potential in our test circuit (using V_{DD} = 5.0V) was 1.75V. If the source of any differential pair transistor exceeds this value, the parasitic *pnp* bipolar device inherent in the *p*MOS device turns on. This effect is visible in curve (d) of Figure 4 for V_{in} > 0.7V. This effect may be avoided by lowering the common-mode input voltage.

Figure 5 shows the transconductance for each case, normalized to its maximum value. Transconductance was simply calculated by differentiating the data in Figure 4. The widening linear range is apparent in this data. Figure 6 shows theoretical plots of the transconductance for the same cases. The theoretical plots were generated using the expression for weak inversion current given by (6), using a value of $\kappa = 0.84$. Some small discrepancy from the data can be expected since our 100nA bias currents put the transistors near the moderate inversion region, where the exponential current-voltage relationship begins to change [7]. Still, it is notable that simple expressions based on (6) matched our data far better than simulations performed using the BSIM3v3 level 49 MOSFET model (simulation data not shown).

From Figures 5 and 6, it is clear that as we increase ΔV, we add ripple to the transconductance curve. This ripple could be reduced by adding additional differential pairs and reducing ΔV.

Currently, we are biasing the differential pair wells with an off-chip series of resistors. Since the wells draw only small leakage currents, large resistors may be used, ensuring low-power operation. All transconductors on a single chip may share the same few bias voltages.

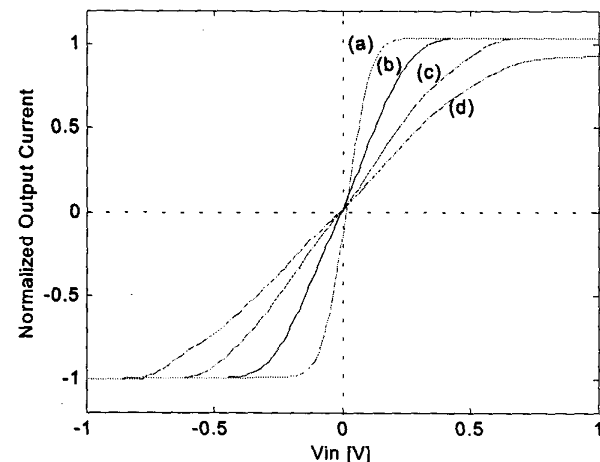

Figure 4: Measured *I-V* curves from: (a) single *p*MOS differential pair ($N = 1$); (b) back-gate circuit with $N = 11$, ΔV = 300mV; (c) ΔV = 500mV; (d) ΔV = 650mV. Note the reduced current for V_{in} > 0.7V due to parasitic bipolar action.

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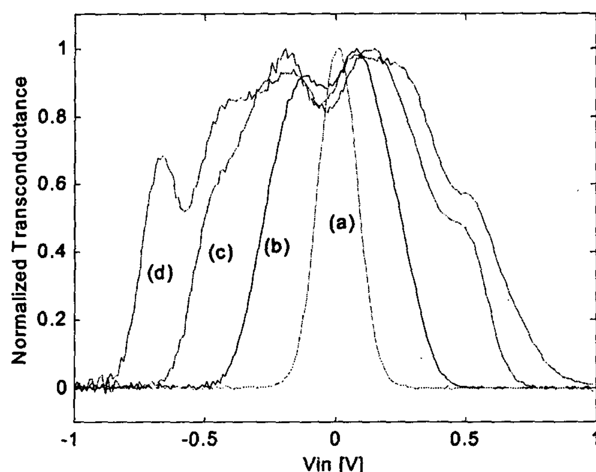

Figure 5: Measured normalized transconductance of: (a) single *p*MOS differential pair ($N = 1$); (b) back-gate circuit with $N = 11$, $\Delta V = 300$mV; (c) $\Delta V = 500$mV; (d) $\Delta V = 650$mV.

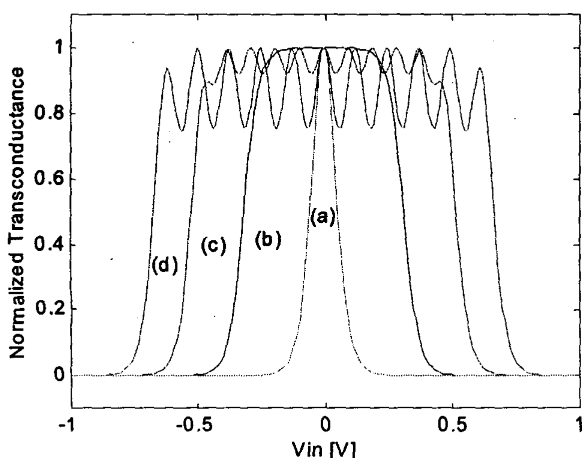

Figure 6: Theoretical normalized transconductance of: (a) single *p*MOS differential pair ($N = 1$); (b) back-gate circuit with $N = 11$, $\Delta V = 300$mV; (c) $\Delta V = 500$mV; (d) $\Delta V = 650$mV. Theoretical plots were based on the expression for weak inversion current in (6). A value of $\kappa = 0.84$ was used.

It is interesting to note that a transconductor similar to the one presented here could be built using differential pairs with floating-gate MOSFETs. Offset voltages could be programmed as stored charge on the floating gates [12], effectively shifting each transistor's threshold voltage.

The transconductor described in this paper allows linear range to be extended by adding more differential pairs. This comes at the expense of chip area and possible ripple in the transconductance. though the penalty does not grow exponentially as in the *W/L* scaling method. Also, dc input range must be limited to prevent parasitic bipolar activation. Nevertheless, this approach uses a small number of transistors to extend linear range in a low-power circuit.

REFERENCES

[1] H. Tanimoto, M. Koyama, and Y. Yoshida, "Realization of a 1-V active filter using a linearization technique employing plurality of emitter-coupled pairs," *IEEE J. Solid-State Circuits* 26:937-945, 1991.

[2] P.M. Furth and H.A. Ommani, "Low-voltage highly-linear transconductor design in subthreshold CMOS," In: Proc. 1997 Midwest Symp. Circ. Syst., Sacramento, CA, August 1997.

[3] P.M. Furth and A.G. Andreou, "Linearized differential conductors in subthreshold CMOS," *Electronics Letters* 31:545-547, 1995.

[4] L. Watts, D.A. Kern, R.F. Lyon, and C.A. Mead, "Improved implementation of the silicon cochlea," *IEEE J. Solid-State Circuits* 27:692-700, 1992.

[5] R. Sarpeshkar, R.F. Lyon, and C.A. Mead, "A low-power wide-linear-range transconductance amplifier," *Analog Integrated Circuits and Signal Processing* 13, 1997.

[6] T. Delbrück, "Bump circuits for computing similarity and dissimilarity of analog voltages," In: *IJCNN-91*, vol. I, pp. 475-479, Seattle, WA, 1991.

[7] Y. Tsividis, *Operation and Modeling of the MOS Transistor, 2nd edition*, McGraw-Hill, 1998.

[8] C.A. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley, 1989.

[9] P. Furth, *On the Design of Optimal Continuous-Time Filter Banks in Subthreshold CMOS*, Ph.D. dissertation, Johns Hopkins University, 1996.

[10] M.H. Cohen and A.G. Andreou, "Current-Mode Subthreshold MOS Implementation of the Herault-Jutten Auto-adaptive Network," *IEEE J. Solid-State Circuits* 27:714-727, 1992.

[11] P.J.G. van Lieshout and R.J. van de Plassche, "A Power-Efficient, Low-Distortion Variable Gain Amplifier Consisting of Coupled Differential Pairs," *IEEE J. Solid-State Circuits* 32: 2105-2110, 1997.

[12] R.R. Harrison, P. Hasler, B.A. Minch, "Floating-Gate CMOS Analog Memory Cell Array," *Proc. IEEE International Symposium on Circuits and Systems (ISCAS) 1998*, 2:204-207, 1998.

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