AC Solar Cells: An Embedded "All in one" PV Power System

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Abstract— **Power converters constructed from discrete components are difficult to mass produce, and the installation involves a significant labor cost to have the proper interconnection among the panel, inverter and the grid. These facts indicate that the present PV technology may not be able to address the challenges involved in reaching the DOE target of $1/W. Therefore, a paradigm shift in the design of the entire PV power system is needed to reach this goal. In order to increase the converter reliability and watts/$, the active and passive elements of a power converter (especially capacitors and active switches such as MOSFETs, JFETs or IGBTs) could be embedded on the same substrate material used for fabricating the p-n junctions in the photovoltaic panel. To the knowledge of the author, there is no prior work in cell level power conversion, and therefore, this project idea could be considered as an "Out of the box" kind. A novel fabrication process is proposed in this paper demonstrating the integration of PV cells and two major components needed to build a power converter. Because of the cell level power conversion, PV panels constructed from these cells are likely to be immune to partial shading and hot-spot effects. The end goal of this research is to produce 120V/240V ac output directly from the panel. An extremely accurate device simulator (*Silvaco Athena/Atlas) was used to generate reasonably accurate characteristics of the proposed PV system.**

I. INTRODUCTION

Power converters are indispensible elements in a renewable energy harvesting system. A grid-synchronized PV power system is constructed from a group of power converters – a dc-dc converter ensuring the maximum power point tracking (MPPT) cascaded by a grid synchronized inverter [1]. For photovoltaic (PV) power generation system, the actual power generating device (solar to electrical) is the solar panel, and it has much longer life than that of the power converters. As a result, the power conversion units become the weakest link in the entire power conversion process, and they are comparatively vulnerable to line voltage anomalies such as temporary over-voltages, impulses and short circuits. In special applications such as military use in a battlefield or in extreme weather conditions, repair or replacement of the inverter is not an option, and a highly reliable PV based power system is needed which is compact and highly mobile in nature. In order to achieve this milestone, today's converter technology should overcome three big hurdles – i) enhanced MTBF of twenty years without enhancing the manufacturing cost to a great extent, ii) high efficiency operation in order to reduce cost and system footprint, iii) suitable for mass production.

Micro inverters have been recently deployed in residential segment of PV based power generation where small PV panels (~200W) are interfaced directly with the 120V/240V micro-grid [4]. A myriad of topologies have been proposed in the last ten years with many favorable features and limitations [2] [3] [6]. In general, these circuits use several electrolytic capacitors and discrete semiconductor devices to realize the power conversion stages. Large electrolytic capacitors used for energy decoupling are known to be the weakest link in these power converter circuits [1] [3] [5]. Especially, when the ambient temperature is substantial, these electrolytic capacitors significantly suffer from shorter life cycle.

An extensive literature study reveals a plethora of existing inverter topologies for PV power generation [2] [18]. Most of those topologies could be grouped into three major kinds: a) central string, b) multi-string ac module, c) multi string dc modules [2]. The last kind is especially suitable to eliminate the partial shading problem of large PV modules. The basics of these topologies are quite similar, they have an isolated DC-DC converter (mostly fly-back), and half-bridge or full-bridge inverter with PWM control.

II. LIMITATIONS OF DISCRETE COMPONENTS

The key factor to limit the lifespan of a PV inverter is the huge electrolytic capacitor used across the dc bus (the input of the inverter) for energy decoupling [1] [5]. References [19] and [20] show that the average lifespan of these electrolytic capacitors are less than six years; whereas the PV modules have a average life expectancy of over 20 years. This reliability issue introduces significant cost increment to the PV power system installation because the users need to replace the inverter a few times before the installation reaches the payback period of the initial cost. A detailed computational analysis on the electrolytic capacitor lifetime can be found in [21]. Even though the reliability issue of the electrolytic capacitor is addressed, the power MOSFET reliability is a major concern to ensure the uninterrupted operation of the inverter and the future development of the PV power system. Power MOSFETs are also affected by the

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operating temperature. Proper cooling could increase the reliability of the MOSFET; however, it comes with a higher manufacturing cost and larger converter footprint. This limitation could be eliminated using high band-gap semiconductors such as SiC or GaN [15] [16] [17]. However, the fabrication technology for SiC/GaN is still not mature, and it is more convenient to use Si for this integration purpose. **The authors envision to integrating the entire power converter (including gate drives and control circuits) capable of processing PV power and generating 120/240V ac output directly from the panel.**

The present and near future trend of PV power system is shown in Figure. 1(a) and the proposed architecture is shown in Figure. 1(b). In this paper, a tentative process technology to fabricate the necessary power electronic circuit components along with the PV cells has been proposed. The initial target of this project is to fabricate capacitors, MOSFETs, and PV cells on the same wafer. The simulated characteristics of the MOSFETs and PV cells are provided for a better understanding of the proposed concept. Finally, a capacitor-clamped converter (MMCCC) [37] - [39] is constructed with the proposed fabrication processes and simulated in Smart Spice of the Silvaco software to investigate the possibility of designing a PV system comprised of only PV cells, MOSFETs and capacitors. The simulation results suggest that an MMCCC circuit can be embedded on the same silicon wafer used for fabricating the PV cells.

III. Existing Silicon Processing for PV Fabrication

Today's PV production is dominated by Crystalline silicon (c-Si) based technologies [22]. Single crystal (SC-Si) technologies have several advantages such as i) an established technology base, ii) superior material quality, and iii) improved efficiency and stability over the two other conventional solutions (thin film and polycrystalline). For integration purposes, SC-Si technologies must be explored first. The individual components of grid tied inverters (MOSFETs, diodes, inductors, and capacitors) have already been fabricated on the c-Si wafer to implement power processing units inside microprocessors. . Other than being the most commercialized and most mature technology, there is another reason for which SC-Si technology based solar cell can be the prime candidate for integration. The efficiency of cells made from SC-Si is higher than that of all multi-crystalline and thin film solar cells (that have been developed so far) [13] [14] [22] by a significant amount. Solar cells with efficiency of 20%-26% on commercialized Czochralski (Cz) wafers have been reported. The main disadvantage is the higher fabrication cost compared to multi-crystalline and thin film solar cells [22], and it can be justified if the combination of the cell and the power processing unit could achieve an extended lifespan. However, SC-Si based solar cells require the smallest footprint for a certain power level, and this is advantageous over other PV technologies when space issue is prevalent.

IV. Existing Silicon Processing for Circuit Component Fabrication

In general, a typical power converter may have six different kinds of active and passive components. These components are - 1) capacitor, 2) power MOSFET, 3) inductor, 4) diode, 5) resistor, and 6) any integrated circuits for gate driving and control. Among these components, capacitors and power MOSFETs are the most sensitive to any overstressed situation such as elevated temperature, over voltage, over current and so on.

Capacitors:

There are many known techniques to form capacitance on Silicon. The electrolytic capacitor used at the dc bus of the inverter can be replaced by a metal-silicon capacitance with an internal SiO_2 layer. When a MOSFET is fabricated in a silicon process, it needs an additional oxide layer which could be exploited for fabricating a large capacitance [23]. Using a conventional 0.35 µm CMOS foundry process, it is possible to grow poly diffusion capacitance of about 5 nF/mm^2 with an oxide thickness of 5-10 nm [24]. Making high aspect ratio pores in Si by deep reactive ion etching (DRIE), 30 nF/mm^2 capacitance can be realized with standard insulator (SiO_2/Si_3N_4) [25]. Moreover, insulators with high di-electric constant (Al_2O_3) can produce very high capacitance (440 nF/ mm^2) while fabricating higher aspect ratio pores [26]. MIM (metal- insulator-metal) capacitance is promising to give the highest capacitance for the integration purposes (5- 40 nF/ mm^2) [27] [28].

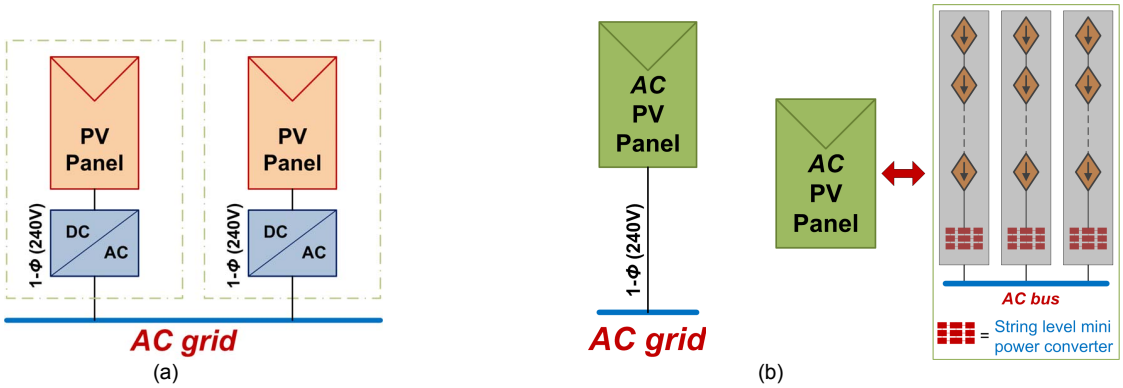


Figure 1. (a) Present and near future PV power system using grid-tied micro inverters, (b) proposed architecture with PV panels capable of generating ac output directly from the strings

MOSFET:

Commercially available power MOSFETs are trench MOSFET. A detailed literature study reveals various techniques for trench MOSFET fabrication [29] [30] [31]. Reference [31] shows a good process steps that can be easily integrated with the power diode.

Inductor:

Researchers have achieved significant progress in fabricating inductors on Si. Various thin films such as NiFe alloy, CoHfTaPd have been investigated to form the magnetic cores to be used for inductors or transformers [24]. A detailed study shows that core loss density in thin films are quite low compared to that of conventional ferrite materials [24]. These thin films are deposited by using conventional semiconductor fabrication techniques such as sputtering, spinning or electroplating. To complete the process, the deposition of conducting (Cu) and insulating materials are necessary as well. Sequential patterning of these three layers is done by photolithography [24]. However, all these efforts suffer from high winding resistances. To achieve sufficiently large inductance, the resistance of the pattern also becomes high, thus yielding a low Q factor. This high resistance limits the current carrying capability of the inductor, therefore limiting the integrated inductor application to the low power circuit. However, to eliminate magnetic elements (or at least minimize them), the best practice would be designing a converter without using any magnetic elements, and this is why the capacitor clamped converters would be an excellent choice for this integration.

This discussion clearly states that the fabrication of embedded components is possible although many technological challenges exist. Implementing inductors would be the most difficult process; whereas, MOSFETs and capacitors could be fabricated using a similar process flow.

V. Proposed Fabrication Process

The reliability of the PV system could be greatly enhanced by integrating the capacitors and the MOSFETs on the same die used for fabricating the PV cells. However, there are multiple fabrication related challenges involved in this implementation. Conventionally MOSFETs are fabricated on a *n*-type substrate in order to realize n-MOSFETs for power circuits. *n*-MOSFETs have superior performance compared to *p*-MOSFETs because of higher carrier mobility. In contrast, *p*-type substrates are conventionally used to fabricate PV cells. Multiple reasons justify the choice for *p*-substrate over *n*-type [32]. Historically the development and commercialization of PV cells started with the space program in mid sixties. While tested under controlled irradiation, PV cells fabricated from *n*-type substrate showed significant degradation of the minority carrier lifetime and junction characteristics resulting in substantial loss of output power over the lifetime of the cell. Although these cells achieved a higher beginning of life performance, their inferior performance compared to the *p*-type cells put them in the second place. Therefore, PV cells fabricated from *p*-substrate exhibit superior lifespan over the counterpart when cells are exposed to space radiation. In addition, electrons are minority carriers in a *p*-type cell, resulting in yielding a higher mobility compared to holes (about three times). This was the prime factor for *p*-type cells to achieve high efficiency. Therefore, these process requirements thus placed big hurdles to combine PV cells and MOSFETs on the same substrate because they require different type substrates to begin with.

Interestingly, a small number of publications have been identified where PV cells were successfully realized on *n*-type substrates [33] [34] [35], and commercialized [35], and they suggest that *n*-type PV cells and *n*-MOSFETs can be fabricated on the same substrate. At the present time, cells are becoming thin and mostly used for terrestrial applications, space radiation and corresponding performance degradation issues are not the dominant factors to decide the fabrication material. However, if *n*-type wafer is used for this integration, the drain terminal of the MOSFET and the substrate of the solar cell are internally tied together. This situation makes any converter configuration almost impossible to operate.

Further literature study [36] shows that a lateral *n*-MOSFET fabricated on a *p*-type wafer can be used to solve this fabrication difficulty. This *p*-type substrate can be used as the base of the PV cells, whereas the drain of the MOSFET is epitaxially grown on the *n*-type layer. Thus, the separated *n*-type epitaxial layers will separate MOSFETs; therefore, converter can be easily embedded with the PV cells.

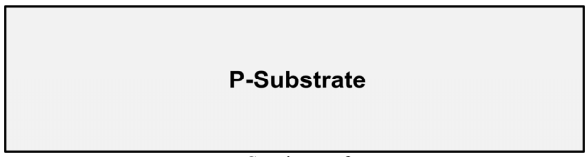
The process proposed in this paper starts with a <100> p-type (~10^{15} cm^{-3} doped with phosphorus) prime Cz wafer. The processes steps are given in Table I and also demonstrated in **Figure 2** graphically. The whole process takes 11 lithographic steps.

Table I: Processing steps to integrate power devices with PV cell

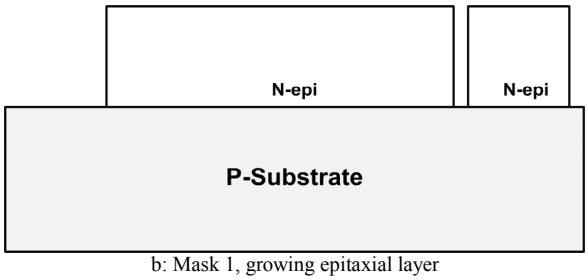
1.	Using an oxide mask, a 2 μm n-type epitaxial layer is grown on top of the substrate. There are two epitaxial layers: one for MOSFET and the other for MOS capacitor. The phosphorus doping density is about $2x10^{16}$ cm^{-3}(Figure 2b).
2.	The next mask is used to define the position of the oxide spacer of the MOSFET. This oxide spacer plays a critical role in determining the breakdown voltage of the MOSFET. The vertical trenches are created by deep reactive ion etching (DRIE) method. The trenches are filled with oxide and are planarized using CMP (third lithographic step) (Figure 2c).
3.	Boron diffusion (doping density about $2x10^{17}$ cm^{-3}) through ion implantation (120 keV) is carried out to create 0.8 μm deep p-type body region (fourth mask) (Figure 2d).
4.	Ion implantation is carried out to form n+ source region, and n+ drain region of the MOSFET and Emitter of the PV cells (phosphorus doping of $1x10^{20}$ cm^{-3}, 80 keV) (fifth mask) (Figure 2e).
5.	To protect the surrounding region from DRIE, 1000 nm thick SiO_2 is deposited using LPCVD process Lithography (sixth mask) and etching is performed to open the region for gate (MOSFET and capacitor) trench formation. Through this region, 1 μm deep Si trench is created by DRIE (Figure 2f).
6.	100 nm of gate oxide is grown thermally. This oxide also acts as the dielectric layer of the capacitor.
7.	300 nm of poly-silicon is deposited by LPCVD process. This poly-silicon is doped by phosphorus to reduce the resistivity of the poly-Si. Another 700 nm of un-doped poly-Si is deposited to ensure trench fill up. Two step RIE is used to planarize the poly-Si (seventh mask). This poly-Si also acts as the upper electrode of the capacitor, and the n-type epitaxial layer works as the other electrode of the capacitor (Figure 2g).
8.	A 500 nm thick inter-metal oxide layer is deposited by LPCVD process. The eight mask is used to open windows in the inter-metal dielectric film for contacts. A Ti/Al layer (0.4-0.8 μm) is deposited by sputtering. Patterning of Al (ninth lithographic step) is done to separate gate, capacitor's upper and lower electrodes, source, drain, and emitter (of solar cell).

9.	Next mask opens up the area for bond pads, and the final mask (eleventh) is used to pattern them. In this way, six pads are created for six terminals - gate, capacitor's upper and lower electrodes, source, drain, and emitter (of solar cell).
10.	A metal stack is deposited on the back surface to create the contact for the base of solar cell. A metal stack consists of a thin Ti film, a thin Ni barrier layer, and a thick Al layer. This stack functions as a heat sink for the entire structure also.

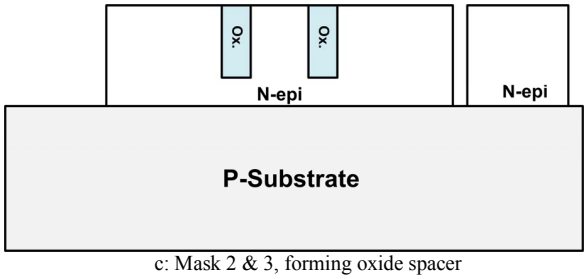
However, the number of process steps could be significantly reduced by fabricating a low-power lateral MOSFET in place of vertical MOSFET. A simpler process flow to implement a lateral MOSFET, a capacitor and a PV cell will be narrated in the following section. The key advantage of this process is the compatibility with the standard CMOS process. If the converter is integrated only for a few cells, converters constructed from lateral MOSFETs could easily withstand the low voltage and current stress. However, components with high breakdown voltage will be required if the converter is integrated with large number of



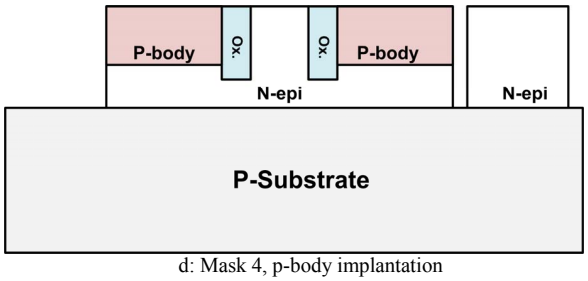
a: Starting wafer



b: Mask 1, growing epitaxial layer

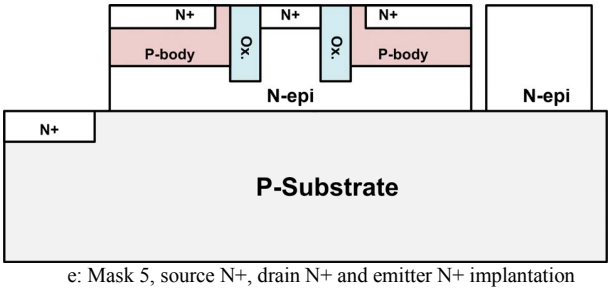


c: Mask 2 & 3, forming oxide spacer

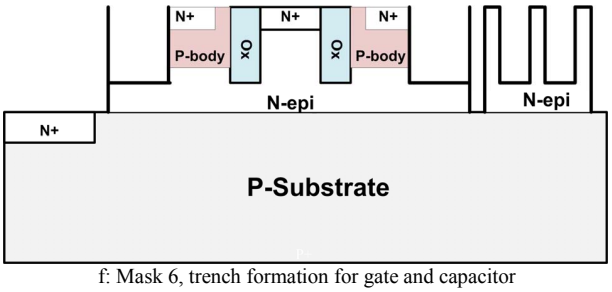


d: Mask 4, p-body implantation

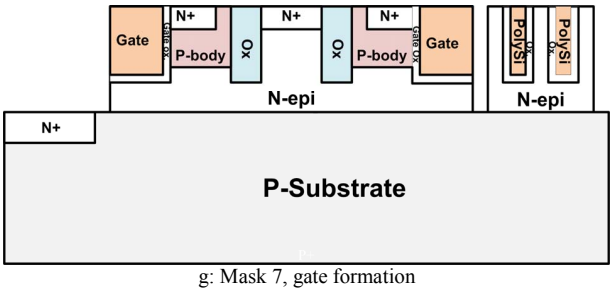
Figure 2: (a-d) Key processing steps for fabricating power MOSFET, Capacitor with the PV cells (Cross-sections are not drawn to the scale)



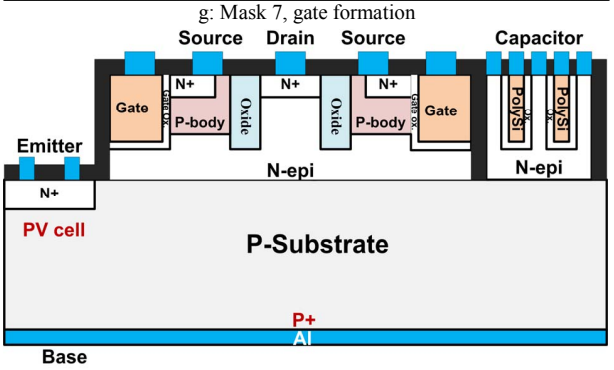
e: Mask 5, source N+, drain N+ and emitter N+ implantation



f: Mask 6, trench formation for gate and capacitor



g: Mask 7, gate formation



h: Complete device cross-section

Figure 2 (continued): (e-g) Key processing steps for fabricating power MOSFET, Capacitor with the PV cells (Cross-sections are not drawn to the scale)

cells. Fabrication of several low power converters will not be an issue as the process is compatible with standard CMOS process, and feasibility of these low power converters can be found in [40].

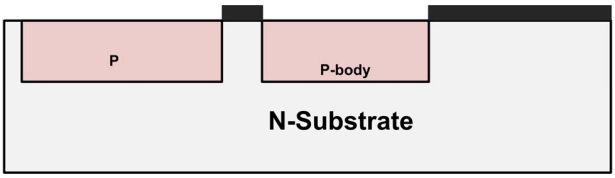
The proposed process implementing converter circuits constructed from lateral MOSFETs starts with a <100> n-type (~10^{15} cm^{-3} doped with phosphorus) prime Cz wafer. The processes steps are given in Table II and also demonstrated in **Figure 3** graphically. The entire process takes only 7 lithographic steps.

Table II: processing steps to integrate CMOS devices with PV cell

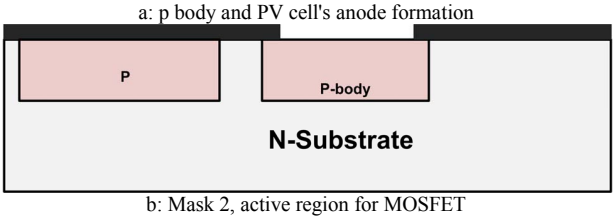
1.	Using an Oxide mask, Boron diffusion (doping density about $2x10^{17}$ cm^{-3}) through ion implantation (120 keV) is carried out to create 0.8 µm deep p-type body region (p-well) as well as anode region for PV (Figure 3a).
2.	Second oxide mask blocked the region for PV cell and opened up area for active region (Figure 3b)
3.	10 nm of gate oxide is grown thermally. 1000 nm of poly-silicon is deposited by LPCVD process. This poly-silicon layer was patterned to open areas for source and drain (third mask). The remaining poly layer act as gate as well as one electrode of the capacitor (Figure 3c)
4.	Ion implantation is carried out to form n+ source region, and n+ drain region of the MOSFET (Phosphorus doping of $1x10^{20}$ cm^{-3}, 80 keV) (Figure 3b). The poly layer also gets doped to reduce its resistivity (Figure 3c).
5.	Rests of the process are similar to processes described in 8 –10 of the previously described process.

VI. Simulation Results

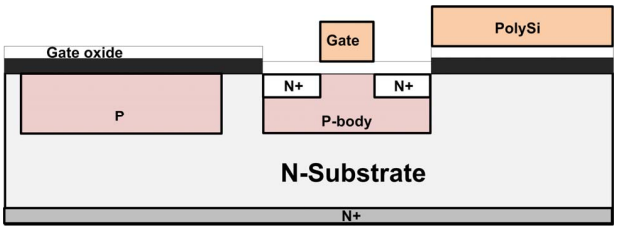
The simplified process described in the previous section has been implemented in ATHENA process simulator and the fabricated device characteristics have been obtained using ATLAS device simulator. These characteristics have been shown in Figure 4. The integrated PV cell has a fill factor of 76%, and the efficiency is found to be 14%. The Atlas software takes significant amount of time to generate simulation results due to the complexity of the device. In order to reduce simulation time, the Si substrate was considered to be only 12 µm thick, which is very thin to absorb light properly. Therefore, the open circuit voltage, current density and efficiency are found to be lower than usual (Figure 4a). The simulated value of the metal poly capacitor was 4 nF/mm^2, and the MOSFET's threshold voltage and break-down voltage were achieved as 0.75 V and



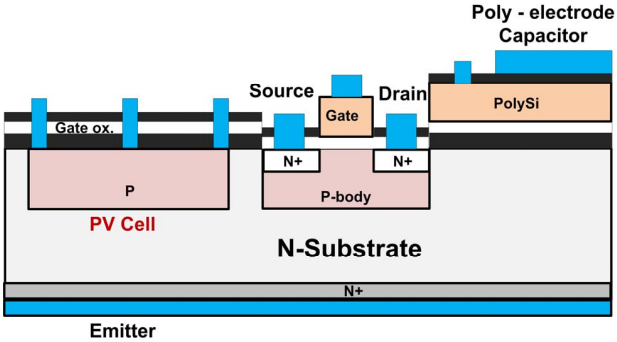
a: p body and PV cell's anode formation



b: Mask 2, active region for MOSFET

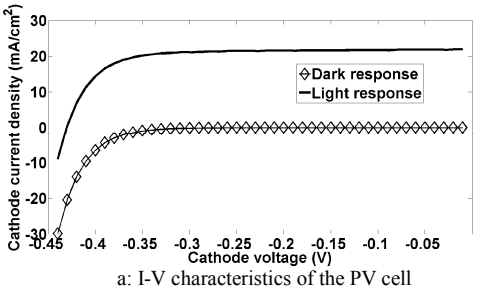


c: Mask 3, poly patterning and source-drain implantation

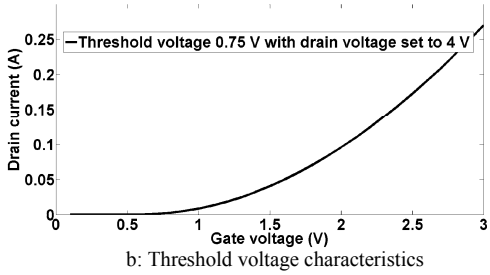


d: Complete device cross-section

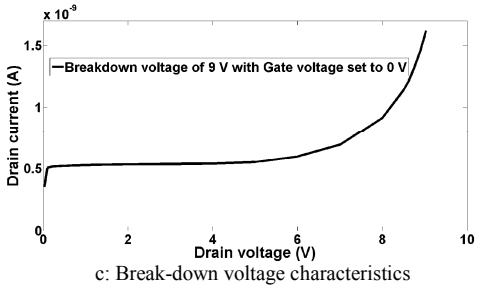
Figure 3: (a-c) Key processing steps for fabricating MOSFET, Capacitor with the PV cells (Cross-sections are not drawn to the scale)



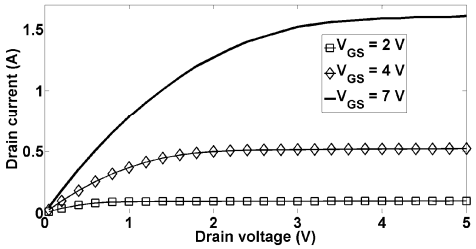
a: I-V characteristics of the PV cell



b: Threshold voltage characteristics



c: Break-down voltage characteristics

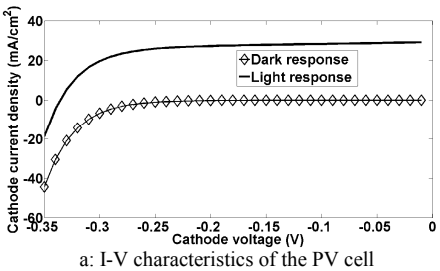


d: I-V characteristics of the MOSFET

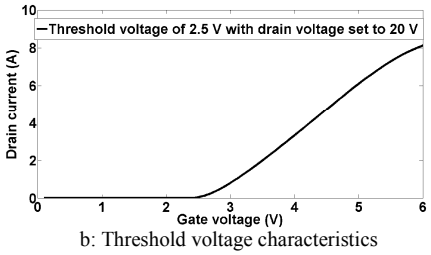
Figure 4: Characteristics of the PV cell and MOSFET for the proposed processes in Section V

9 V respectively (Figure 4b & 4c). The boosting operation of the embedded MMCCC power converter is illustrated in Figure 7 – the input was a PV cell with constant illumination and output load was 25 Ω. **This entire converter was fabricated in ATHENA process simulator, and simulated in Smart Spice of Silvaco.**

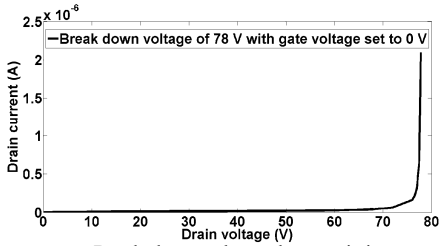
The process describing the fabrication steps to implement the converter based on power MOSFETs, capacitor with PV cells have been constructed in ATHENA, and ATLAS generated characteristics are shown in Figure 5. The integrated PV cell has a fill factor and efficiency almost similar to the previous case. The threshold voltage of the MOSFET is about 2.5V (Figure 5b). Varying the channel length (creating shallow trench), the threshold voltage can be changed. The breakdown voltage of the MOSFET is about 78 V (Figure 5c). This voltage can be modified to any level by varying the oxide spacer depth and width.



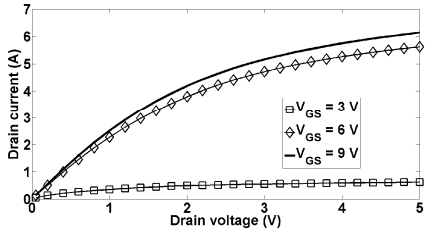
a: I-V characteristics of the PV cell



b: Threshold voltage characteristics



c: Break-down voltage characteristics



d: I-V characteristics of the MOSFET

Figure 5: Characteristics of the PV cell and power MOSFET for the proposed processes in Section V

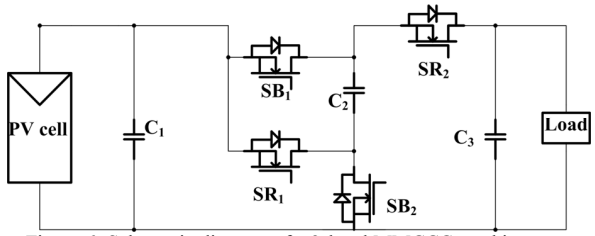


Figure 6: Schematic diagram of a 2-level MMCCC used in smart spice

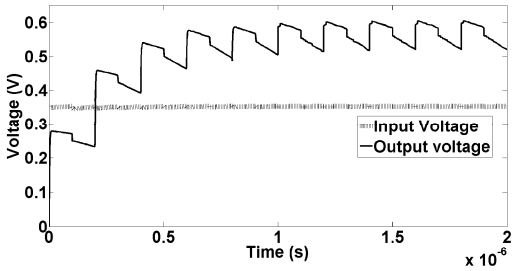


Figure 7: Voltage boosting operation of the embedded MMCCC

The capacitance of the trenched MOS capacitor is about 1 nF/ mm^2. Deep trenches were created to increase the area of the electrode, which in turn increased the capacitance. However, the small value of the capacitance is caused by thick oxide layer (100 nm) needed for high breakdown voltage (about 80 V). Creating much deeper trenches and using very high dielectric material such as Al_2O_3 in place of SiO_2, the capacitance can be further increased. However, this would increase the number of process steps as well.

VII. Conclusion and Future Works

The proposed embedded architecture is likely to make a breakthrough in the design and implementation of conventional PV based power system. The fabrication complexity, cost and processing time could be greatly reduced over time only with continuing research. Simulated characteristics of the MOSFET, capacitor and a PV cell fabricated on the same wafer are presented in this paper, and these MOSFETs and capacitors can be used to construct a highly efficient MMCCC to harvest solar energy. The interaction between the MMCCC and a PV module has been demonstrated in this paper to show how a capacitor clamped converter could be a potential candidate for this proposed integration although the most appropriate power converter has not been identified yet. Presently this paper demonstrates how power can be processed in an embedded fashion, and the authors envision embedding the entire inverter on the substrate to generate 120V ac output. Research effort is in place to achieve these targets within the next three years.

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