Analog MAP Decoder for (8, 4) Hamming Code in Subthreshold CMOS

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Abstract — **An all-MOS analog tail-biting MAP decoder is presented for an (8,4) Hamming code. The decoder implements a probability propagation algorithm using subthreshold CMOS networks. Physical results verify the expected behavior of the decoder and demonstrate robustness of analog decoding circuits.**

The authors of [1] present a class of analog VLSI circuits which can be used to implement a general probability propagation algorithm for soft-decision decoding. The proposed circuits can be implemented using either bipolar transistors or weak-inversion (subthreshold) MOS devices. Researchers have implemented analog decoders in BiCMOS [2][3].

MOS transistors scale to smaller sizes than bipolar, and they may be fabricated using more common digital processes. The analog Hamming decoder was fabricated in an AMI .5μm digital process, and verifies that analog decoding can be performed using only MOS devices.

Simulation and performance verification for large analog decoder networks cannot be carried out using SPICE. An intermediate model has been produced using VHDL which accounts for the physical behavior of the analog cells. This model allows prediction of the behavior of analog networks, and is used to produce the performance curves of Fig. 1. Measured output of the decoder circuit is shown in Fig. 2. The results of Fig. 2 are obtained by switching between two input patterns at 2MHz. The decoder uses 3.8 mW of power, most of which is thought to be consumed in the interfaces.

BiCMOS analog decoders are expected to be faster because MOS circuits are limited to weak-inversion (device currents below ~100nA). Devices whose currents exceed this range are said to operate in strong inversion, and the assumptions made in [1] are no longer valid. The Hamming decoder nonetheless continues to function in strong inversion. Allowing device currents on the order of 10μA, decoding is possible up to 5 MHz (20 Mbit/s). For analog circuits, higher device currents generally provide faster operation.

Analog decoders are expected to degrade gracefully in response to other non-ideal circumstances such as mismatch, device noise, and process variation. Much of this flexibility arises from the parallelism inherent in the probability propagation algorithm. The Hamming decoder provides an exceptional example of robustness in that it functions in spite of a layout error. Fig. 1 compares performance of an optimal MAP decoder, the analog decoder with layout error, and a corrected analog decoder.

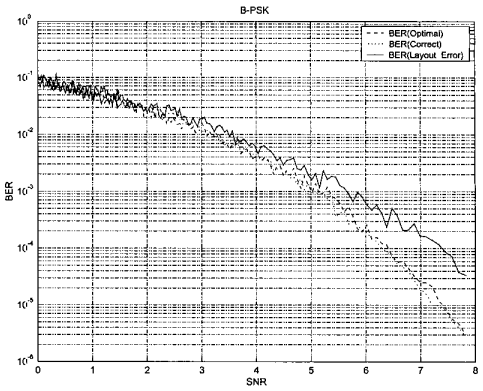

Fig. 1: Simulation results using VHDL model.

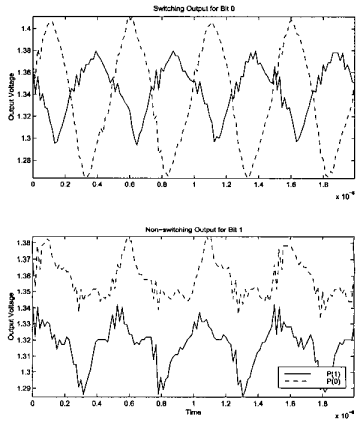

Fig. 2: Measured response of the Hamming decoder.

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References

[1] H.-A. Loeliger, F. Lustenberger, M. Helfenstein, and F. Tarköy, "Probability Propagation and Decoding in Analog VLSI," *IEEE Trans. on Information Theory*, pp. 837-843, February 2001.

[2] F. Lustenberger, M. Helfenstein, H.-A. Loeliger, F. Tarköy, and G. S. Moschytz, "All-Analog decoder for a binary (18,9,5) tailbiting trellis code," *Proc. European Solid-State Circuits Conference*, pp. 362-365, Duisburg, September 1999.

[3] M. Moerz, T. Gabara, R. Yan, and J. Hagenauer, "An analog .25μm BiCMOS tailbiting MAP decoder," *IEEE Proc. International Solid-State Circuits Conference*, pp. 356-357, San Francisco, February 2000.

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