A Methodology for Physical Design Automation for Integrated Optics

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***Abstract*—Advancements in silicon photonics technology are enabling large scale integration of electro-optical circuits and systems. To fully exploit this potential, automated techniques for design space exploration and physical synthesis for integrated optics must be developed. This paper investigates how conventional VLSI physical design automation techniques can be adapted for integrated optics applications. We present an overall methodology for cell-placement, global routing, and detail routing for physical synthesis of optical circuits. In addition, we highlight optics-specific constraint models, design rules and optimization criteria that will have to be accounted for in physical design automation.**

1. Introduction

Recent breakthroughs in silicon-based integrated optics – dubbed *Silicon Photonics* – are establishing the viability of silicon for integrated optics. The use of silicon enables fabs to leverage already existing and mature silicon processes and infrastructure for optical device fabrication as well as integration for electro-optical systems. Investment in Si-photonics integration is significant [1], [2]; also significant are the open foundary initiatives and developmental programs such as the OPSIS framework [3]. These developments will also enable applications far beyond traditional roles of optics in communications – such as *optical routing and photonic networks-on-chips* [4], *signal processing* [5], and also *optical digital logic* [6], [7], *quantum and reversible computation* [8], [9].

As the availability and applications of integrated optics expand, the need for automated design space exploration, optimization, and physical synthesis of integrated electro-optical systems is also beginning to appear. For this reason, the Electronic Design Automation (EDA) community is investigating how automatic design space exploration techniques can be adapted to the photonics domain [6], [10]–[12].

Contemporary Photonic Design Automation: A great focus of current investigations is in *architectural explorations* for photonic interconnection networks in multi-core processor systems [4], [11], [13]. In addition, at the functional/logic-design level, there have been investigations into use of optical components as building-blocks, connected by waveguides, to design optical computing systems [6], [14], [15]. High-level synthesis, using technology-mapping with a library of optical device building-blocks, has also been presented [10]. The focus of these works is on architectural and functional analysis and optimization; physical design and fabrication details are beyond the scope of such works.

At the much lower (physical) level, [12] demonstrates a *full-custom layout* of photonic structures using a commercial CMOS-based layout editor (Cadence Design Systems Virtuoso). Waveguide curves are discretized at a fine level into rectangular geometry, enabling waveguides to be represented in a format that traditional foundries accept. This methodology is significant in that it provides a building-block pathway for producing foundry-ready layouts and masks for non-Manhattan device geometries (rings, arcs, waveguide curvature). However, "design automation" is essentially absent, and the design must be conceived of and optimized manually. Similarly, the commercially available RSoft [16] Photonics CAD suite provides a framework for physical device design, analysis and (FDTD) simulation engines for performance analysis of optical design components. However, automated techniques for design space exploration during physical synthesis – *automated floorplanning, placement, waveguide routing while optimizing for physical parameters such as insertion-loss, bend-loss, phase coherence issues, etc.* – are not available.

A. Applications and Motivations for Design Automation

This paper also takes a step forward in this direction and investigates *physical design automation for integrated electro-optical circuits and systems*. We show that an EDA design style methodology–i.e. placement, global routing, detailed routing– is applicable to optical layout and routing, and techniques/algorithms used for VLSI physical design can also be suitably adapted. In this paper we highlight how constraint models, design rules, and optimization criteria will drive and govern physical design automation techniques for hybrid electro-optical system integration.

The main motivation for investigating this problem stems from physical design of integrated *electro-optical logic circuits* [6], [7], [15], [17]. Such circuits are complex in their device interconnections, often featuring high device counts and large amounts of feedback loops. These designs comprise a set of pre-designed optical devices – modulators, switches, splitters – placed on a planar substrate, connected together via waveguides. For example, in our previous work [6], we present a complete multi-level logic synthesis methodology for implementing logic in such hybrid integrated electro-optical technology. Similar optical logic design concepts have also been proposed [7], [15], [17]. These demonstrate how optical designs can scale beyond the ability of custom design. The physical synthesis of such applications now has to be addressed.

The paper is organized as follows: 1) we first describe the design constraints of our problem formulation; 2) we then outline our EDA-style design flow methodology; 3) the details of each step of the design flow are described, including how such methods are adapted for optics; 4) how design rules for waveguide routing are accounted for in the routing grid.

This research was funded in part by a sub-contract to AFOSR grant FA9550-09-1-0661.

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2. Design Constraints

At the physical automation level, we identify signal power and substrate area as our core guiding metrics.

Signal Power: Signal power is the primary guiding metric in our methodology. All devices, including bulk waveguides, have insertion losses, measured in decibels (dB). Our assumption is that these losses are pre-characterized through device-analysis (FDTD, etc.) for the following type devices:

- **Pre-designed devices** (e.g. modulator devices, switches, splitters, etc.). Losses are characterized from inputs to outputs. For example, waveguide splitters have their signal power from the input effectively halved at each output (a 3dB loss).
- **Waveguide crossings.** As the optical substrate is planar, signals can only cross perpendicular to each other. Such crossings could be considered pre-designed devices, but given their use in our routing, we keep them separate. Losses on order of 0.1-0.2dB ($3.5-4.5\%$) per crossing [18], [19].
- **Waveguide bends**, especially for 90° bend transitions. Losses will depend on the radius of curvature, as this increases the effects of wall-surface roughness losses even above the minimum radius of curvature [20].
- **Bulk waveguides.** This would include straight waveguides and bends far larger than the minimum radius of curvature. Waveguide wall-surface roughness is the main cause of loss. Losses are relatively small, measured in dB/cm.

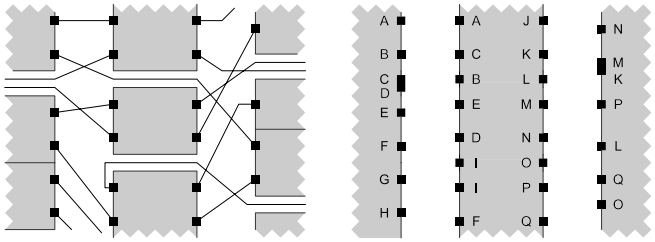
Losses due to the presence of pre-designed devices are effectively fixed. Therefore, the design automation problem concerns itself with designing within the permitted losses *between* such devices–the routing fabric. We identify three main routing loss mechanisms in descending importance: 1) *waveguide crossings,* which induce a relatively large fixed loss per crossing; 2) waveguide bends, especially bends close to the minimum radius of curvature 3) bulk waveguides, which generally have low losses; however surface roughness can induce losses over larger distances for smaller waveguides.

SOI waveguides: Si-photonic waveguides, with their large refractive index differentials, provide strong mode confinement, and therefore bends can be much sharper, saving area. While waveguide bends can be effectively lossless given a large enough radius of curvature, accepting small per-bend losses can be advantageous in reducing the area occupied by a bend [20]. The choice of minimum routing grid size can therefore affect the weighting of metrics used to guide the routing, whether losses due to bends, waveguide crossings [18], or area.

Area: Many optical devices, such as those used for switching, are designed such that their input and output ports appear on only opposing sides. This feed forward device design often extends to the device networks as a whole, resulting in overall networks that are very wide. Wide substrates may not be desirable when integrating optics into designs, and a more suitable aspect ratio may need to be enforced. The side-effect of this is that devices must be rearranged on the substrate in a manner that can affect inter-device locality as well as increase waveguide routing complexity. This becomes an important part of the placement phase of our methodology.

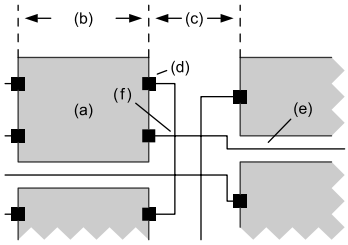
3. Methodology

We propose the following methodology for the overall physical design problem for integrated optics. As depicted in Fig.1(c), pre-designed optical devices are represented as rectangular blocks (a) that are arranged (placed) in fixed-width columns (b). Such a placement gives rise to *vertical routing channels* (c), which are routing regions that separate the placed devices. Waveguides are routed between devices at "ports" (d) that face the channels. For ports in different columns, these waveguides may pass through *horizontal routing channels*, as depicted in (e). While the substrate is planar, waveguides may also cross each other perpendicularly (f) without sharing signals.



(a) Columns of optical devices, and global routes

(b) Resulting channels for detailed routing



(c) Ports, routes and channels

Fig. 1: Overall Physical Design Methodology

Overall, the physical design methodology requires that the problem be solved in three steps:

- Placement of optical switching devices into columns, i.e. a grid-based layout.
- Global routing of waveguides that connect these devices. Global routing solution will determine the overall routing topology of all the nets.
- Detailed routing of all the nets, which manifests itself as a well-defined channel routing problem.

While this methodology is analogous to that employed in the VLSI domain, the design and optimization constraints imposed by the optical technology are different. Any CAD solution to this problem will have to incorporate such technology specific constraint models and design rules.

4. Device Placement

Pre-designed optical devices are placed into columns of devices Consider the layout of devices in Fig.1(a). While

devices maintain ports on only their left and right sides, connections may be made to any other device in the network by routing through vertical columns and between columns. In such a manner, connectivity is preserved, but the overall network has a smaller aspect ratio. This transformation does not come without issues: the column arrangement may affect the locality of connected devices, which in turn affects routing congestion and losses due to routing length, crossings, and bends. The problem of device locality and connectivity is not limited to optics, and has been studied extensively for VLSI chip planning. Placement techniques, such as those used for row placement and chip floorplanning [21], can therefore be employed for placing devices within an optical substrate.

The placement of devices into columns enables us to utilize routing techniques designed for such placement strategies. In our applications we use the Capo placer [21] to arrange devices in rows given a specific aspect ratio. Connected devices are localized as much as possible, reducing congestion.

5. Waveguide Routing

Routing is performed in two phases: 1) *global routing,* which determines the general routing path and horizontal routing channel placement, and 2) *detail routing,* which is formulated as *planar waveguide channel routing*.

Global routing: Global routing determines the high level topology a signal may take through the channels from source to destination. The chosen routes induce bends and crossings with other nets. The optimization goal of the global router is to minimize losses due to waveguide crossings and waveguide bends. In addition, global routing also takes into account overall net lengths and routing congestion.

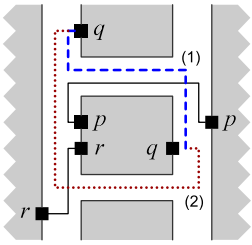
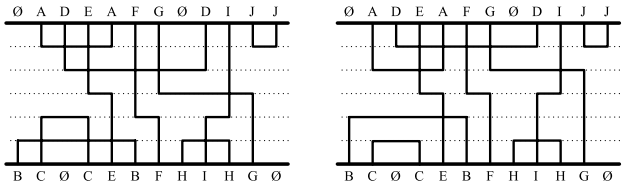


Fig. 2: Two global routes affects interactions between nets

Consider the nets in example Fig.2, where a net q can utilize one of two distinct routes (1) and (2). Route (1), though shorter than route (2), must cross the chosen route for p; to avoid the crossing, route (2) could be utilized. Route (2), however, crosses over the chosen route for r. Should route r have less stringent loss constraints than p route (2) may be chosen over (1), despite a longer overall path. Ultimately, the final route choice is derived from a combination of all loss factors. These types of constraints are incoporated into the global routing model.

In our global routing technique, we employ a mixed integer linear program (MILP) to optimize all global routes by taking into account inter-route crossings, waveguide bends, and route lengths.

Channel routing: The global router provides a set of vertical routing channels with net/port connectivity, such as depicted in Fig.1(c). At this stage detail routing is performed, determining the actual placement of horizontal and vertical connections within the vertical channel. For optical device networks, detailed routing involves a modified form of traditional and well-known VLSI channel routing techniques [22], adapted for waveguides in a planar substrate.



(a) Standard track-optimized (5 tracks, 10 crossings)

(b) Crossing-constrained (5 tracks, 8 crossings)

Fig. 3: Channel routing solution for track and crossing minimization

Consider the routing channels depicted in Fig.3. The channel routing area is the rectangular grid between the pins on the top and bottom edge, where vertical connections from the pins are made to connecting horizontal spans. The horizontal spans are located at fixed vertical positions, denoted *tracks*. Traditional VLSI channel routing seeks to minimizing area by minimizing the number of tracks of a fully routed channel– the track *height.* For example, the channel routing obtained via the well-known left-edge track assignment algorithm [23] in Fig.3(a) is minimal in the number of tracks.

In our channel routing formulation, however, track height is secondary to signal loss for purposes of optimization. Net crossings, in particular, are a major loss mechanism and our channel routing techniques seek to avoid crossings whenever possible. The routed channel depicted in Fig.3(b) is a crossing-minimal solution for the same channel in Fig.3(a).

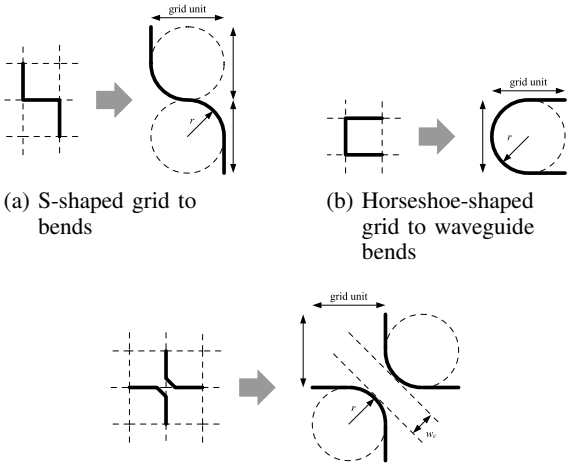
In our channel routing technique, we employ the same type of track assignment algorithms cited above [23]; however, we can optimize for crossings by introducing additional vertical track constraints for avoiding crossings as a primary goal, track height secondary. In addition, we are investigating sorting-based [24] channel routers, which are well suited for crossing minimization, but suffer in terms of area minimization.

6. Design rules: Routing grid realization

The result of routing algorithms must be transformed into the physical waveguide layout. This entails converting the routing grids into waveguide bends satisfying the material bend constraints, which are generally defined in terms of minimum radius of curvature and coupling distance.

A. Mapping routing grids to waveguides

A rectilinear routing grid is realized as waveguides by converting all 90° grid transitions to 90° waveguide bends. This requires that such bends complete within a quarter of the routing grid. This is illustrated in Fig.4(b) where a horseshoe-shaped bend utilizes two 90° waveguide bends, each taking place within a quadrant of the routing grid. This mapping



(a) S-shaped grid to bends

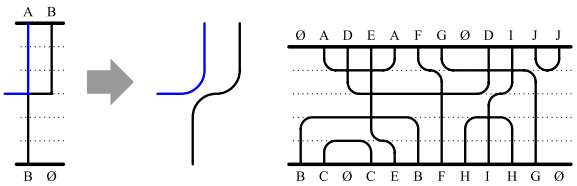
(b) Horseshoe-shaped grid to waveguide bends

(c) Knock-knee grid with 90° bends, radius of curvature r, and minimum coupling distance w_c

Fig. 4: Conversion of grid units to waveguide curves

represents the smallest grid that can be suitably used for complete routing routing grid flexibility.

The physical routing can also exploit the spacing between curves at the corners of grids. These "knock-knee" style bends, depicted in Fig.4(c), enable additional track sharing– potentially reducing the overall number of tracks needed for a routing. For example, the channel problem in Fig.3(a) can be routed allowing for knock-knees, resulting in the solution depicted in Fig.5(b). The knock-knee bends between signals C-E, F-G, D-I, and G-J allow each respective pair to occupy the same track, with the net effect of reducing the total number of tracks to four (4). Routing techniques enabling knock-knee track sharing must account for shared rectilinear grid locations, e.g. Fig.5(a), during channel construction.



(a) Shared grid corners enable knock-knees

(b) Channel routing incorporating knock-knee bends (4 tracks, 8 crossings)

Fig. 5: Knock-knee model for for grid spacing

The waveguide's minimum radius of curvature r has an important role in determining the routing grid's minimum size. In some cases, r may be chosen for area reduction, at the expense of per-bend losses [20]. For example, to enable knock-knee routing patterns, the distance w_c in Fig.4(c) must be sufficient to prevent significant coupling between waveguides.

7. Conclusion

This paper presents a physical design automation methodology for silicon nanophotonic circuits and systems. Automation will be key to large scale system synthesis. We demonstrated that traditional VLSI physical design flows of placement, global routing, and detailed routing can be adapted to the optics domain. While this methodology is analogous to that in the VLSI domain, the design and optimization constraints imposed by the optical technology are different. We have described the design constraints and optimization criteria that are imposed by such optical technology, and show how they can be incorporated into the placement and routing formalisms.

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