Use of Spread Spectrum Time Domain Reflectometry to Estimate State of Health of Power Converters

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***Abstract*— A new online measurement and analysis method has been presented in this paper to identify the state of health of power converter circuits. Using spread spectrum time domain reflectometry (SSTDR), impedance in the various current paths inside the converter as well as any fault can be identified without interrupting the circuit's normal operation. Multiple sets of test data have been generated while the SSTDR process is applied to each of the components i.e. the power MOSFETs, the dc bus capacitor and the load. These obtained test data are analyzed to show how these test results are consistent with the impedances in various current paths. An impedance matrix was formed for a non-aged converter and a corresponding matrix using SSTDR data was formed as well. The matrices could be formed for any power converter, and the impedance matrix for the non-aged converter could be considered as a "Reference matrix" for comparison purpose. By comparing these two matrices, the variation in path impedances due to aging could be determined. This research aims to identify the measurable quantities to characterize the aging process, their origins of these quantities and propose convenient methods to measure them.**

Keywords-Reflectometry, Time Domain Reflectometry (TDR), Spread Spectrum Time Domain Reflectometry (SSTDR), Equivalent Series Resistance (ESR), ON – state resistance

I. INTRODUCTION

Power converters are widely used in industrial manufacturing processes, and the uninterrupted operation of those converters is critical. In addition, power converters are becoming a part of the residential power system because of the widespread adoption of grid-tied PV inverters. The overstressed conditions i.e. over voltage, over current or switching impulses could permanently damage various components in a power converter. In addition, the functionality and performance of a power converter degrades with time, and the degradation rate depends on several associated factors such as any overload, ambient temperature, connected load types, radiation, and so on. Power converters are periodically replaced in an industrial process, but without identifying the remaining life of the aged converter. Therefore, effectiveness and utilization factor of power converters could be greatly enhanced if the power converters' state of health could be identified with certain accuracy. Electrolytic capacitors are mostly affected, and switching devices such as MOSFETs, IGBTs, BJTs are some of the primarily affected components in power converters due to aging. Components with degraded electrical characteristics eventually cause secondary and tertiary effects that can accelerate the aging process in a circuit having multiple control loops. Aging can degrade individual component's performance as well as the overall circuit's efficiency and reliability.

II. AGING FACTORS AND STATE OF THE ART SOLUTIONS

MOSFETs and electrolytic capacitors are known to be the two major components responsible for converter failure, and they have significantly higher failure rate than other components used in power converters. From the failure survey of two different types of switched mode power supplies, 60% and 72% power supply failures are due to electrolytic capacitor breakdown and 31% of the total failure occurs due to the failure of semiconductor switches [1], [2]. Degradation and failure of these components may be due to long time operation under normal operating condition or due to short time operation under extreme stress condition i.e. high ambient temperature, high voltage, reverse bias and high ripple current.

Electrical stress at the gate area was implemented in [3][4] by applying high voltage at gate terminal and the corresponding impacts were studied. Here it was found that the threshold voltage increases with aging. An increase in threshold voltage directly corresponds to an increase in switching time. Threshold voltage deviation is generally occurred due to the degradation in gate oxide region and the interface of gate oxide and semiconductor region. The degradation rate depends on the thickness of the gate oxide.

The ON – state resistance is found to be the most significant aging factor in power MOSFETs [5], and two aging measurement techniques for power MOSFETs have been presented in [6]. During the first test, the drain current was increased from 3A to 15A and the device fails to turn off when the gate voltage reaches to zero. This phenomenon indicates the loss of gate control, and the ON – state resistance (R_{DS}) exhibits a sudden drop due to elevated drain current. Therefore, higher R_{DS} is consistent with aging and a sudden

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drop in the value of R_{DS} is the indicator of the loss of gate control. According to the second method of aging presented in [6], the failure occurred as a result of increased resistance inside the device. As a result, the drain current dropped and the transistor failed to switch. Degradation at the contact area of bonding wire – metallization is reflected in the MOSFET ON – stare resistance (R_{DS}). R_{DS} increases due to the degradation at metallization and at the contact area of bonding wire – metallization [7]. Reference [8] also concluded that R_{DS} increases due to thermal aging of MOSFET. Reference [9] described a technique of using ON – state resistance of the device to find out the junction temperature. Die solder degradation is observed in reference [10][11] by applying thermal stress to the device, and the R_{DS} increased due to the degradation.

[12] presents the effect of high temperature gate bias (HTGB) stress on large area (0.56 cm^2) SiC power MOSFETs with voltage and current ratings of 1200V and 67A respectively. This analysis showed that if the device is being operated under high temperature with high stress at gate, it will eventually have higher/lower threshold voltage depending on the type of stress and types of MOSFET (n channel or p channel). Reference [13] explains how threshold voltage, transconductance, and collector-emitter ON voltage could be used to identify aging of IGBTs. There are several real time methods to estimate the state of health of power converters [14]-[17]. However, they are suitable for detection of degradation of a specific component in the converter. SSTDR can be applied in an energized circuit and it can generate real time data depending on the impedance discontinuity between the test points. It is possible to estimate the overall health state of converter using the data generated by SSTDR hardware.

III. Proposed Methodology

Most of the conventional techniques estimate components' aging by measuring individual components while they are disconnected from the circuit. Even they are characterized in real time; results applicable to individual components are not suitable to predict the overall converter reliability. In order to eliminate this limitation, spread spectrum time domain reflectometry (SSTDR) could be used to obtain several parameters of the individual components as well as the converter circuit. Reflectometry is conventionally used for locating wiring faults, and several novel solutions using reflectometry could locate the fault with a greater precision [18]-[22]. Using reflectometry, a high frequency electrical signal is sent down the wire and it reflects from any impedance discontinuity. The reflection co-efficient gives a measure of how much signal is returned and is given by ρ.

$$\rho = \frac{Z_t - Z_o}{Z_t + Z_o} \quad \text{(i)}$$

Where Z_0 is defined as the characteristic impedance of the transmission medium and Z_t is the impedance of the terminating end of the transmission line. The time or phase delay between the incident and reflected signals provides the distance to the fault, and the observed magnitude of the reflection co-efficient provides the impedance at discontinuity. Time domain reflectometry (TDR) method was identified as a potential method to identify small anomalies in the test cable due to it's large bandwidth [23]. TDR was used in [24] to measure the parasitic parameters on printed circuit boards (PCB). In addition, TDR was used in [25], [26] to detect two interconnect failure: solder joint cracking and solder pad separation. The method of extracting series resistance of capacitors is presented in [27] using TDR. The major limitation of TDR is the higher cost compared to other techniques and inability to use in live networks. In order to overcome the limitations of TDR, SSTDR was used to estimate the state of health of power MOSFETs in this paper. SSTDR is a combination of TDR and spread spectrum method. A high frequency PN signal is sent down to the wire and the incident and reflected signals are correlated in SSTDR technique. The location of the various peaks in the correlation indicates the location of impedance discontinuities such as open circuits, short circuits, and arcs (intermittent shorts). Unlike TDR technology, SSTDR can identify small intermittent faults in cable and it can be used in a live network.

Due to aging, the equivalent series resistance (ESR) of capacitor increases [28] and the equivalent capacitance decreases i.e. impedance is being changed. In case of MOSFETs, the channel "ON – state resistance" (R_{DS}) is increased due to aging. Therefore, reflectometry method can be used to identify these gradual changes in a power converter by comparing these values with the reference values consistent with a non-aged (new) converter.

IV. Experimental Results

A test circuit was built to identify the variation in MOSFET's ON – state resistance (R_{DS}) as a function of aging, and the schematic shown in Figure 1 was used for this purpose. The other key objective of this test was to verify if the SSTDR technique can identify this R_{DS} variation. Five MOSFETs (M_1 – M_5) having different aging levels were used for this measurement. These MOSFETs were aged using accelerated stress in a controlled environment, and five FDP 3672 N-channel power trench MOSFETs were used for this test. The case temperature was stabilized between 110°C~120°C during this accelerated aging process. M_5 was used as the reference MOSFET as zero stress was applied to it.

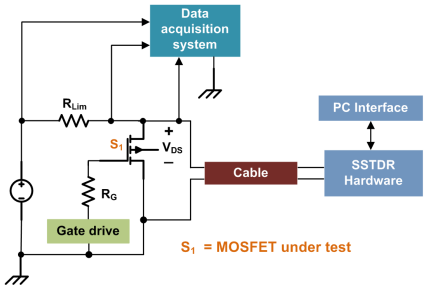


Figure 1. Test schematic to identify the R_{DS} variation of aged MOSFETs using SSTDR system.

Figure 2(a) demonstrates how the MOSFETs R_{DS} varies with the level of aging. This R_{DS} measurement was done using a data acquisition system. For a V_{GS} of 5V, R_{DS} will vary from

50 mΩ to 55 mΩ after 3 hours of accelerated aging. This variation is reflected in the SSTDR measurement as well. The relationship between the correlated output and the level of aging has been summarized in Figure 2(b). Apparently, the SSTDR method can identify the variation in R_{DS} at different aging conditions.

Once the MOSFET characterization was performed, the SSTDR signal was applied to a power converter circuit shown in Figure 3. The key objective of this test was to observe the correlated outputs across various components. There are four test points in this circuit (Figure 3). SSTDR technique was applied in different combinations to map these four test points. A 3.53 V (RMS), 60 Hz AC voltage was applied to the circuit, and the load resistor R_L was 10 Ω.

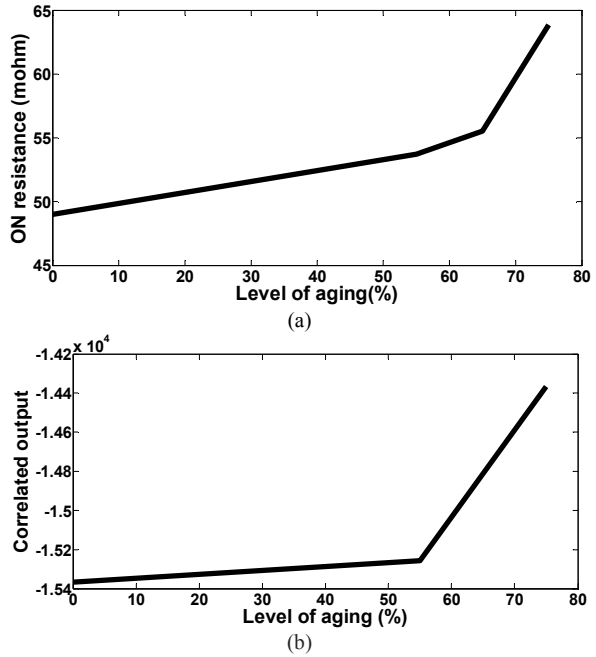


Figure 3. The variation in R_{DS} as a function of aging. There is a significant increase in R_{DS} once the MOSFET is subjected to stress. a) R_{DS} was calculated using the data acquisition system, b) correlated output as a function of R_{DS} was measured using the SSTDR setup.

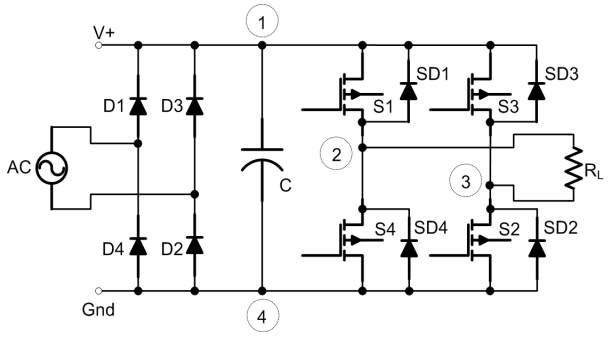


Figure 3. Schematic of the AC-AC converter used to test the effectiveness of the SSTDR system.

A 30 foot cable was connected between the SSTDR hardware and any node pairs. When SSTDR was applied between test points 1 and 2, different values of correlated output were found. This is due to the presence of different path impedances between these two nodes. The equivalent circuits of these current paths are shown in Figures 4 and 5.

The internal resistances of diodes D1, D2, D3 and D4 are considered as equal for simplicity. Here, R_D is the diodes' internal resistance, R_S is the source's internal resistance, ESR is the equivalent series resistance of the DC bus capacitor, and R_{DS1}, R_{DS2}, R_{DS3}, R_{DS4} are the ON – state resistances of MOSFETs S1, S2, S3, S4 respectively. The frequency of applied PN signal in SSTDR method is 24 MHz ~ 96 MHz. The MOSFET capacitances were neglected in calculating the equivalent path impedances as the capacitive impedances are very high at 24 MHz ~ 96 MHz compared to MOSFET ON – resistances. The ON – resistances will be dominant when they are in parallel with MOSFET capacitances during the circuit's operating mode. ESR is always in parallel to the series combination of two diode resistances and the source resistance. If S1 and S2 are activated, the equivalent path impedance between test points 1 and 2 is the parallel combination of the two branches shown in Figure 4(b). As $R_{DS1} << (R_{eq}+R_L+R_{DS2})$, the equivalent path impedance can be approximated as R_{DS1} shown in Figure 4(c). When S3 and S4 are activated, the equivalent path impedance between test nodes 1 and 2 is the series combination of R_{eq} and R_{DS4} (Figure 5). Similarly, the path impedance between 1 and 3 will be R_{DS3} or the series combination of R_{DS2} and R_{eq}.

The equivalent path impedance between nodes 1 and 4 is always R_{eq} (Figure 6), and the equivalent path impedances between nodes 2 and 3 are "$R_{DS1} + R_{eq} + R_{DS2}$" or "$R_{DS3} + R_{eq} + R_{DS4}$" (Figure 7). All the equivalent path impedances between the test pairs have been derived. The SSTDR hardware will generate different values of correlated outputs depending on the path impedances. In addition, there may be few data points which will not give any consistent results during the switching transition of the power MOSFETs. A similar MOSFET with a DC voltage applied at the gate terminal was tested in a DC chopper circuit to estimate the steady state R_{DS}. The correlated output was "-23516". There is a discrepancy in SSTDR data generated for similar MOSFETs in different circuit. SSTDR data were generated in steady state condition for H – bridge converter to find out the reason of the discrepancy. All the SSTDR data (steady state operation and 60 Hz operation) and corresponding path impedances were given in Table 1. The steady state data are consistent with the data generated in a DC chopper circuit. Proper synchronization is required between the SSTDR hardware and the switching pulse generator to obtain accurate results.

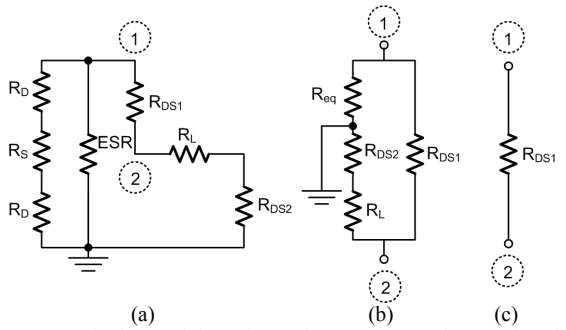
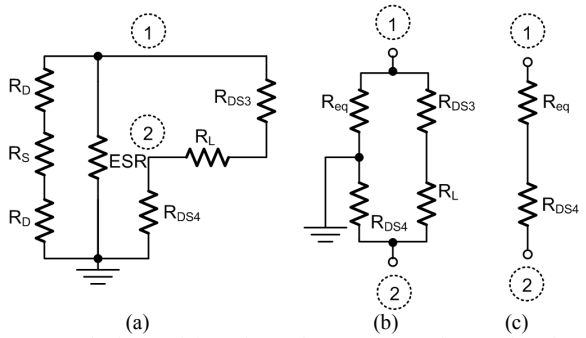
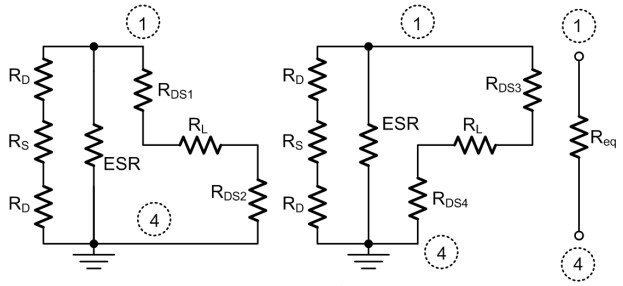


Figure 4. Equivalent path impedances between test nodes 1 and 2 when S1 and S2 are activated.



(a) (b) (c)

Figure 5. Equivalent path impedances between test nodes 1 and 2 when S3 and S4 are activated.



(a) (b) (c)

Figure 6. Equivalent path impedances between test nodes 1 and 4 for both switching states.

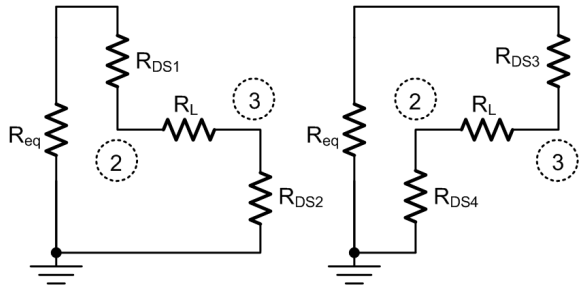


Figure 7. Equivalent path impedances between test nodes 2 and 3 for both switching states.

Table 1. Experimental correlated output across various current paths in the non-aged AC-AC converter.

Test points	Path impedance	Correlated output	
		60 Hz	Steady state
1 and 2	R_{DS1}	-13700	-23016
	$R_{eq} + R_{DS4}$	-10942	-19347
1 and 3	R_{DS3}	-13415	-22821
	$R_{eq} + R_{DS2}$	-12101	-20635
2 and 4	R_{DS4}	-13178	-23057
	$R_{eq} + R_{DS1}$	-10505	-19232
3 and 4	R_{DS2}	-12319	-22865
	$R_{eq} + R_{DS3}$	-10212	-20287
2 and 3	$R_{DS1} + R_{eq} + R_{DS2}$	-7367	-19372
	$R_{DS3} + R_{eq} + R_{DS4}$	-5960	-19912
1 and 4	R_{eq}	-16601	-21173

V. MATRIX ANALYSIS

An impedance matrix was built from the single phase AC – AC converter shown in Figure 8. For i=1-4 and j=1-4, X_{ij} represents correlated output between any two test points among the four different nodes. X_{ij} = -1 (normalized value) for i=j because it would be a short circuit. Therefore, all the diagonal elements of this matrix is "-1". From the previous discussion, there exist two impedance matrices for two different operating states of the converter. $X_{12} - X_{13}$ represent the correlated output across upper side MOSFETs (S1 and S3), and X_{14} represents the correlated output across the dc bus capacitor. In the same way $X_{42} - X_{43}$ represent the correlated output across lower side MOSFETs (S2 and S4).

The experimental values of the ON – resistances during steady state condition, the capacitor ESR, and the load impedance are given in Table 2. Using these values, the equivalent path impedances for each test pairs were calculated using simulations in PSIM software. The reference impedance matrix was formed using these calculated values shown in Figure 9. The corresponding SSTDR matrix using steady state data was formed shown in Figure 10.

The values of matrices shown in Figure 9 and 10 will eventually be changed as the converter ages. These variations could be incremental for normal aging or substantial for any failure. This matrix could be formed for any power converter, and a "Reference matrix" could be constructed from a non-aged power converter for comparison purpose. For example, if MOSFET S1 is aged, it's ON – resistance may increase to 50 mΩ, and these path impedances should be impacted accordingly. Using this new assumed value of R_{DS1} while other values remaining unchanged, a PSIM simulation was performed to calculate the path impedances. A matrix was formed using these path impedances and it is clearly observable that only few matrix elements changed due to aging of S1 (Figure 11). In this case, second row and second column are affected only during the state when S1 and S2 are activated and no changes were found during the state when S3 and S4 are activated. Therefore, it is possible to determine the aged component by observing the matrix elements. The location of the elements indicates which component is aged and the value of the elements indicates how much the component is aged. The test set up of experiments is shown in Figure 12.

$$\mathbf{A}= \begin{pmatrix} X_{11} & X_{12} & X_{13} & X_{14} \\ X_{21} & X_{22} & X_{23} & X_{24} \\ X_{31} & X_{32} & X_{33} & X_{34} \\ X_{41} & X_{42} & X_{43} & X_{44} \end{pmatrix}$$

Figure 8. Impedance matrix.

Table 2. Experimental values of MOSFET ON – resistances, capacitor ESR and load resistance

Name of the components	Corresponding resistance
S1	37.78 mΩ
S2	37.28 mΩ
S3	33.67 mΩ
S4	39.17 mΩ
C	33 mΩ
R_L	10 Ω

When S1, S2 are "ON" and S3, S4 are "OFF"

$$\text{Reference A} = \begin{pmatrix} 0 & 37.6397 & 68.962 & 31.854 \\ 37.6397 & 0 & 106.11 & 69.247 \\ 68.962 & 106.11 & 0 & 37.1435 \\ 31.854 & 69.247 & 37.1435 & 0 \end{pmatrix}$$

When S1, S2 are "OFF" and S3, S4 are "ON"

$$\text{Reference A} = \begin{pmatrix} 0 & 70.6178 & 33.558 & 31.854 \\ 70.6178 & 0 & 103.707 & 39.019 \\ 33.558 & 103.707 & 0 & 65.1981 \\ 31.854 & 39.019 & 65.1981 & 0 \end{pmatrix}$$

Figure 9: Reference Impedance matrix.

$$\text{Reference A} = \begin{pmatrix} -23706 & -23016 & -20635 & -21173 \\ -23016 & -23706 & -19372 & -19232 \\ -20635 & -19372 & -23706 & -22865 \\ -21173 & -19232 & -22865 & -23706 \end{pmatrix}$$

When S1, S2 are "OFF" and S3, S4 are "ON"

$$\text{Reference A} = \begin{pmatrix} -23706 & -19347 & -22821 & -21173 \\ -19347 & -23706 & -19912 & -23057 \\ -22821 & -19912 & -23706 & -20287 \\ -21173 & -23057 & -20287 & -23706 \end{pmatrix}$$

Figure 10: Matrix formed by SSTDR generated data in steady state condition.

When S1, S2 are "ON" and S3, S4 are "OFF"

Only S1 aged [Assuming R_{DS4} = 50 mΩ],

$$\text{A} = \begin{pmatrix} 0 & 49.754 & 68.962 & 31.854 \\ 49.754 & 0 & 117.824 & 81.873 \\ 68.962 & 117.824 & 0 & 37.1435 \\ 31.854 & 81.873 & 37.1435 & 0 \end{pmatrix}$$

When S1, S2 are "OFF" and S3, S4 are "ON"

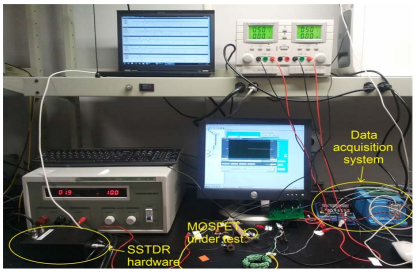
Only S1 aged [Assuming R_{DS4} = 50 mΩ],

$$\text{A} = \begin{pmatrix} 0 & 70.6178 & 33.558 & 31.854 \\ 70.6178 & 0 & 103.707 & 39.019 \\ 33.558 & 103.707 & 0 & 65.1981 \\ 31.854 & 39.019 & 65.1981 & 0 \end{pmatrix}$$

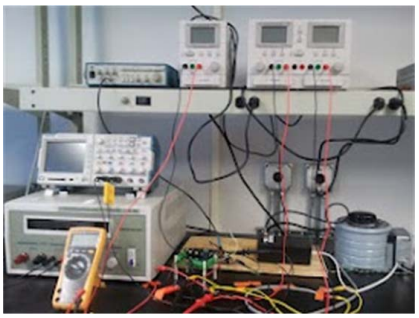
Figure 11: Impedance matrix assuming S1 is aged. The impedances that are changed due to aging of S1 indicated as red marked.

VI. CONCLUSIONS

This paper presented a non-intrusive measurement and computation technique to estimate the state of health of power converters. SSTDR was applied in a single phase AC-AC converter between different test point pairs and corresponding correlated output for different path impedances were obtained. The proposed method involves a new technique to identify the variation in the path impedance in a non-interfering manner, and this paper shows the feasibility of using SSTDR method to identify the aging of power MOSFETs and other components. In addition, the test results suggest that this technique could be used to identify the aging of the entire power converter once numerical computation is performed with the impedance matrix. This matrix could be formed for any power converter, and a "Reference matrix" could be constructed from a non-aged power converter for comparison purpose. By comparing these two matrices, it is possible to identify the impedance variation in various current paths due to aging and predict the relative state of health of the converter.



(a)



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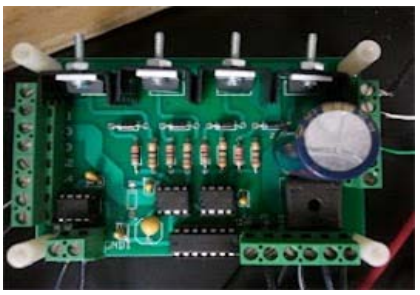

(c)

Figure 12. Experimental set up. (a) Test set up when SSTDR is applied to a MOSFET in a chopper circuit, (b) Test set up when SSTDR is applied to different components of an AC-AC converter, (c) AC-AC converter under test.

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