# A FLOATING GATE COMMON MODE FEEDBACK CIRCUIT FOR LOW NOISE AMPLIFIERS

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## ABSTRACT

Most low noise amplifier designs focus on eliminating sources of noise that are intrinsic to the amplifier (thermal noise, $1/f$ noise). As integrated circuit design moves increasingly towards mixed signal implementations, the design of low-noise analog amplifiers must be re-evaluated to consider the switching noise generated by on-chip digital circuitry. We designed three fully differential versions of a previously reported single-ended low-noise amplifier for biomedical applications. Each design uses a different common mode feedback (CMFB) circuit. The first uses a standard continuous-time CMFB circuit, the second uses a switched capacitor CMFB circuit, and the third uses a novel floating gate CMFB circuit. A test chip has been fabricated in a 1.5 μm CMOS process. The fully differential amplifiers outperform the single-ended amplifier in the presence of switching noise. The amplifier with the floating gate CMFB circuit has the lowest total harmonic distortion over the critical range and exhibits the smallest fluctuation in the common mode output level.

## I. INTRODUCTION

There are many applications in modern electronics where it is necessary to amplify low voltage signals while adding minimal noise. Most low noise amplifier designs focus on eliminating sources of noise that are intrinsic to the amplifier (thermal noise, $1/f$ noise). As integrated circuit design moves increasingly towards mixed signal implementations, the design of low noise analog amplifiers must be re-evaluated to consider the switching noise generated by the on-chip digital circuitry.

We designed a fully differential version of a previously reported single-ended low-noise amplifier (LNA) for biomedical applications [1]. The amplifier is fully integrated and is suitable for recording biological signals in the range from below 1 Hz to 7.2 kHz. The major difference between the design of a single-ended amplifier and a fully differential amplifier is the need for a common mode feedback (CMFB) circuit in the latter design. We designed three different versions of the fully differential LNA, each using a different CMFB circuit. The first uses a standard continuous-time CMFB circuit, the second uses a standard switched capacitor CMFB circuit, and the third uses a novel floating gate CMFB circuit. A floating gate CMFB circuit has been previously reported in [2], however our circuit differs by using only one floating gate and making provision for tuning through setting the charge on the floating gate. Detailed characterization results were not given for the previous design, so we can not compare the performance of the CMFB implementations. Many other variations of CMFB circuits have been proposed, including ones using resistive averaging for common mode detection, and multiple gain stages for a reduced common mode error voltage [3]. Detailed comparisons of many of the more common CMFB circuits are given in [4] and [5]. In this paper we demonstrate that our novel floating gate CMFB circuit has advantages over the two standard designs tested, and that the fully differential designs outperform the single-ended design in the presence of digital interference.

This report is divided into six main sections. Section II summarizes the important design features of the LNA, which hold for all three of the fully differential amplifiers. Section III gives the circuit descriptions of the CMFB circuits used in the fully differential amplifiers. Section IV reports the simulation results that were obtained prior to fabricating the test chip. Section V reports the experimental results obtained from the test chip. Finally, section VI summarizes the findings and presents conclusions on the use of fully differential low noise amplifiers and the relative performances of the CMFB circuits.

## II. AMPLIFIER DESIGN

Figure 1 shows the schematic of the amplifier design. The midband gain $A_M$ is set by $C_1/C_2$, and the bandwidth is $g_m/(A_M C_1)$, where $g_m$ is the transconductance of the operational transconductance amplifier (OTA). Transistors $M_a$-$M_d$ are MOS-bipolar devices acting as "pseudo-resistors" [6]. For small voltages across these devices, their incremental resistance is very high.

Figure 2 shows the schematic of the OTA used in the amplifier, omitting the CMFB circuit. The circuit topology is a standard design suitable for driving

capacitive loads, but the sizing of the transistors is critical for achieving low noise at low current levels. The input transistors $M_1$ and $M_2$ are sized with a large W/L ratio to push them into weak inversion, maximizing their $g_m/I_D$ ratio. Transistors $M_3$-$M_9$ are sized with a small W/L ratio to keep them in strong inversion, minimizing their $g_m/I_D$ ratio. Since the input-referred thermal noise power is expressed as

$$\overline{v^2_{ni,thermal}} = \frac{8kT\gamma}{g_{m1}}\left[1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right] \quad (1)$$

these size choices minimize thermal noise. All transistors are sized as large as possible to minimize $1/f$ noise. As devices $M_3$-$M_8$ are made larger, their gate capacitances increase, which moves the secondary poles closer to the dominant pole created by $C_L$. This reduces the phase margin, so the device sizes are chosen as a compromise between noise and stability.

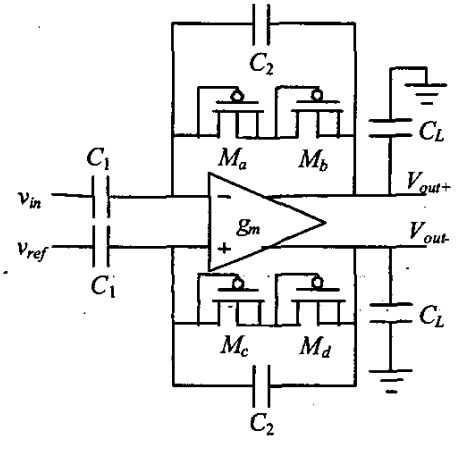


Figure 1: Schematic of fully differential low noise amplifier

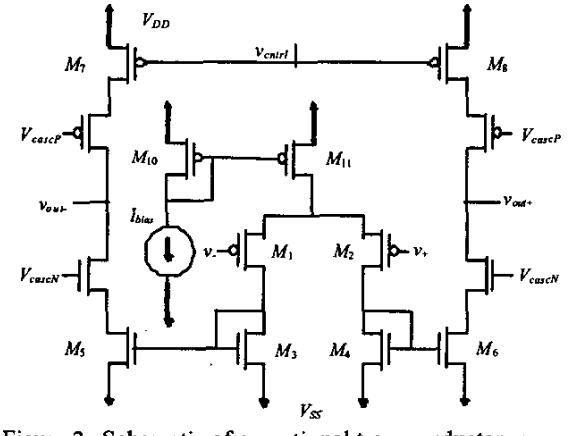


Figure 2: Schematic of operational transconductance amplifier used in low noise amplifier

## III. COMMON MODE FEED BACK CIRCUITS

### A. Continuous-Time Design

Figure 3 shows the schematic of the continuous-time CMFB circuit [7]. If the common mode level of the outputs increases, the currents through $M_{12}$ and $M_{15}$ increase, decreasing the currents through $M_{13}$ and $M_{14}$. This causes $v_{cntrl}$ to increase and reduces the common mode level of the outputs. The disadvantage of this design is the limited linear range of the differential input pairs formed by $M_{12}$-$M_{15}$. This restricts the allowable signal swing at the outputs. Our implementation maximizes the allowable signal swing by sizing $M_{12}$-$M_{15}$ with a very small W/L ratio, thereby reducing their $g_m$ and increasing their linear range.

### B. Switched Capacitor Design

Figure 4 shows the schematic of the switched capacitor CMFB circuit [7]. This circuit uses capacitive voltage division to average the output voltages and adds the appropriate bias voltage. If the common mode level of the outputs increases, the average voltage produced by the $C_C$ capacitors increases, increasing $v_{cntrl}$ and reducing the common mode level of the outputs. The $C_S$ capacitors were chosen to be 1/5 the size of the $C_C$ capacitors. This sizing is a compromise between larger capacitors which unnecessarily overload the OTA, and smaller capacitors which suffer from charge injection from the transistor switches. The output signal swing is larger for this implementation than for the continuous-time implementation and is only limited by the transistor switches, since the capacitors are linear over the entire range of output voltages. The disadvantage of this design is that it can only be used in discrete time applications because of clock feed-through glitches.

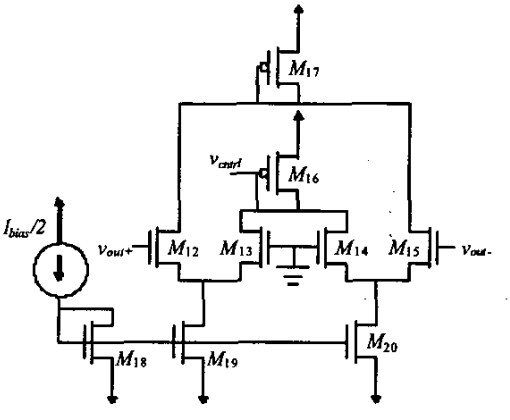


Figure 3: Schematic of continuous-time common mode feedback circuit

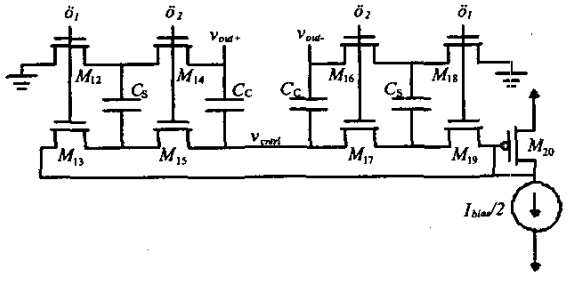


Figure 4: Switched capacitor common mode feedback circuit

### C. Floating Gate Design

A floating gate is a polysilicon node surrounded by $SiO_2$, which traps charge on the gate indefinitely. Figure 5 shows the schematic of the floating gate CMFB circuit, omitting the circuitry for setting the charge on the floating gate. This design combines the advantages of the two previous designs presented. The operation is similar to that of the switched capacitor CMFB circuit. The voltage at node $v_1$ is set by a combination of the common mode level of the outputs and the stored charge on the floating gate node. The stored charge can be programmed to achieve the proper bias voltage for the desired common mode voltage, and the common mode voltage of the outputs is then fed back by the averaging capacitors $C_C$ to keep the common mode voltage at the desired level. Analyzing this circuit yields the following expression for $v_1$:

$$v_1 = \frac{C_{TOT}}{C_F} V_{REF} - \frac{C_C}{C_F}\left(v_{out+} + v_{out-}\right) - \frac{Q}{C_F} \qquad (2)$$

$$C_{TOT} = C_C + C_C + C_F \qquad (3)$$

where $Q$ is the stored charge on the floating gate node, and $V_{REF}$ is a reference voltage that is supplied to the circuit. It can be seen that $V_{REF}$ and $Q$ perform a similar role to $M_{20}$ in the switched capacitor CMFB circuit. The negative sign in front of the averaged output voltage is compensated for by $M_{12}$ and $M_{13}$.

The circuitry for programming the floating gate charge is based on a design reported in [8], and a simplified version is shown in Figure 6. Electrons are removed from the floating gate using Fowler-Nordheim tunneling across the tunneling junction $C_{TUN}$. The voltage needed to create an electric field large enough for this tunneling to take place is 25-35V in the 1.5 µm technology used for our chip, and is lower for smaller technologies with thinner oxides. The AND gate used to control the tunneling is a high voltage design which uses nFETs with lightly doped drain regions (using well diffusion) that have breakdown voltages of over 45V. Electrons are added to the gate using hot electron injection in a pFET device, shown as $M_{12}$ in Figure 6. The hot electron injection is controlled through the NAND gate. A $V_{DS}$ of 7-10V is needed for hot electron injection to occur in the 1.5 µm technology used for the test chip. Once the charge on the floating gate has been set, it will remain there indefinitely.

Like the switched capacitor CMFB circuit, the floating gate circuit uses capacitors to achieve better linearity than the continuous-time circuit for large signal swings. Since no clock is needed, there is no digital switching noise, so this CMFB circuit can be used in either continuous or discrete time applications. Another advantage is that the charge on the floating gate can be set to eliminate any DC common mode offset. The only added complexities are that a stable $V_{REF}$ must be provided and the charge on the floating gate must be programmed. Different values of $V_{REF}$ are needed for circuit operation and for programming the floating gate, so it could be switched between a bandgap voltage reference for normal operation and an arbitrary value for programming the floating gate.

## IV. SIMULATION RESULTS

The circuits were simulated using the TSPICE simulator with a BSIM3v3 level 49 transistor model. Programming of the floating gate through tunneling and

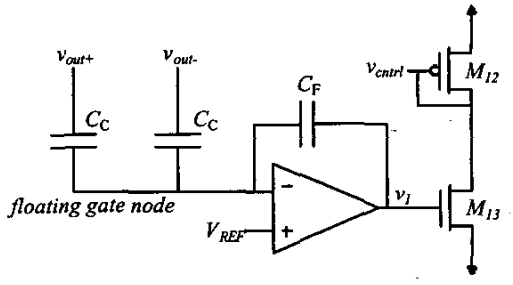


Figure 5: Schematic of floating gate common mode feedback circuit

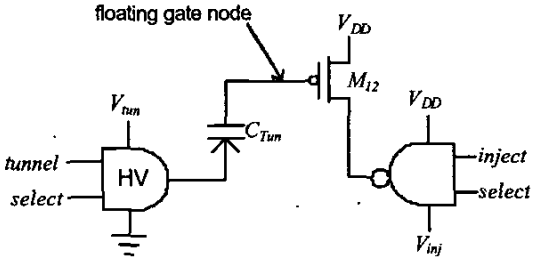


Figure 6: Simplified schematic of circuitry used for programming the floating gate

injection was not simulated. The trapped charge on the floating gate was simulated by specifying an initial condition for the voltage, and the simulation was made to converge by connecting a very large resistance ($>10^{20}$ ohms) from the floating gate node to ground. Figure 7 plots the common mode level of the outputs for each of the fully differential amplifiers for a 10 kHz input with 25 mV amplitude. The power supplies for the circuits are ±2.5 V, and the gains are approximately 40 dB. From this plot it can be seen that the switched capacitor and floating gate CMFB circuits stabilize the common mode level of the outputs more effectively than the continuous-time CMFB circuit.

## V. EXPERIMENTAL RESULTS

A test chip has been fabricated in a 1.5 µm CMOS process with the three versions of the fully differential output LNA, and the single-ended LNA. The fully differential amplifiers are similar in size, and consume about 23% more area than the single-ended design they are based on. The chip includes a pin for injecting digital switching noise. The pin is connected to a wire running over the amplifier outputs. A die photograph of the chip is shown in Figure 8.

The input-referred noise was similar for the floating gate and continuous fully differential amplifiers, at 2.5 µVrms. This compares favorably to the single-ended amplifier, for which the input-referred noise was measured at 2.6 µVrms. As expected, the input-referred noise for the switched capacitor fully differential amplifier was significantly higher (5.3 µVrms) due to the digital switching noise of the switched capacitor components. To simulate the presence of digital noise on the chip, we injected a 1 kHz square wave of 2.5 V amplitude using the pin included for this purpose. In the presence of this digital interference, the benefits of the

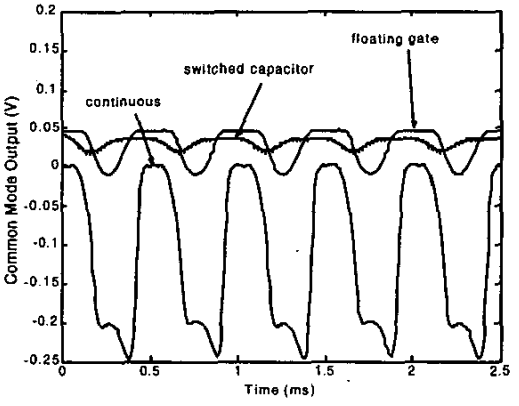


Figure 7: Transient simulation of the common mode output levels of each amplifier

fully differential amplifiers were evident. The input-referred noise of the continuous and floating gate amplifiers increased from 2.5 to 2.6 µVrms, while the input-referred noise of the single-ended amplifier increased from 2.6 to 4.5 µVrms.

A good measurement of the nonlinear interaction between the common mode and differential mode components of an amplifier is the total harmonic distortion (THD) [5]. Figure 9 plots the THD of each of the fully differential amplifiers against the RMS voltage in the fundamental harmonic at 1 kHz. For RMS output voltages below 1.3 V, all of the amplifiers have similar performance, with a THD of < 0.5%. For RMS output voltages above this level, the floating gate amplifier has a lower THD than the other amplifiers. This range, from a THD of 0.5% to about 5%, is the critical range where the performance of the amplifiers will differ. For inputs below this range all of the amplifiers have negligible distortion, and for inputs above this range all of the amplifiers have too much distortion to be useful. The THD curves are not as widely separated as we would expect from measurements of the effectiveness of the different CMFB circuits at controlling the common mode level of the outputs. We suspect that this is due to the distortion from the amplifier core (Figure 2) overwhelming the distortion from the CMFB circuits for input signals in this range.

Figure 10 displays the common mode output levels for each of the CMFB implementations for a 20 mV, 1 kHz input signal. The floating gate implementation had the smallest variance in the common mode output signal, with a peak to peak excursion of 3.8 mV, followed by the switched capacitor implementation at 15.2 mV. The continuous time version was much less effective at controlling the common mode output voltage, with a signal excursion of 220 mV peak to peak. The plot also shows that the floating gate implementation is the only one with the common mode output voltage centered around 0 V, since this can be tuned by setting the charge on the floating gate or by changing the reference voltage provided to the circuit (see figure 5).

Figure 11 displays similar results as Figure 10, but in the frequency domain. A differential mode input was applied to each of the amplifiers at varying frequencies, and the amplitudes of the common mode output fluctuations were measured, and are shown in Figure 11. The input signal amplitude was 20 mV. The continuous CMFB performed worst with an average common mode output fluctuation of 188 mV peak to peak, followed by the switched capacitor CMFB with an average fluctuation of 13.4 mV peak to peak. The floating gate CMFB had the lowest average fluctuation at 2.2 mV peak to peak. Table 1 summarizes the characterization measurements for each of the amplifiers.

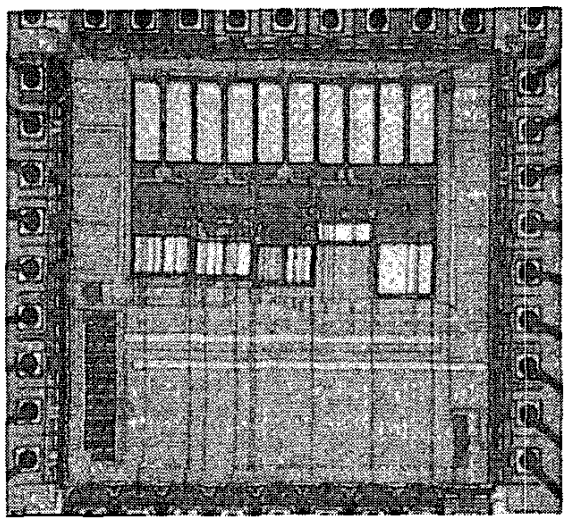

Figure 8: Test chip photograph

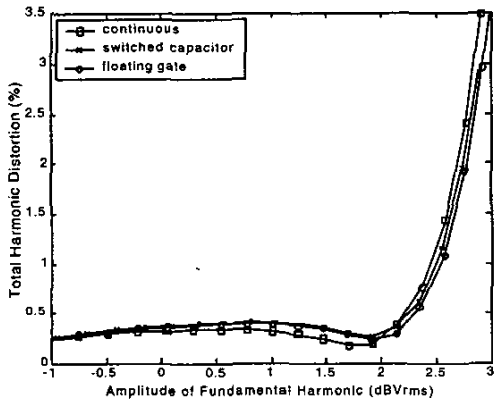


Figure 9: Measured total harmonic distortion at 1 KHz for each of the fully differential amplifiers

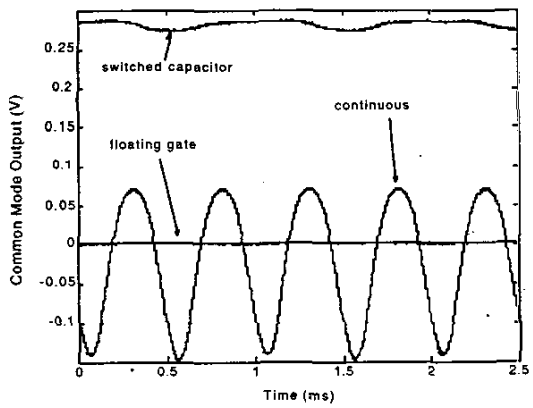


Figure 10: Measured common mode output levels of the amplifiers for a 20mV 1 kHz peak to peak input signal

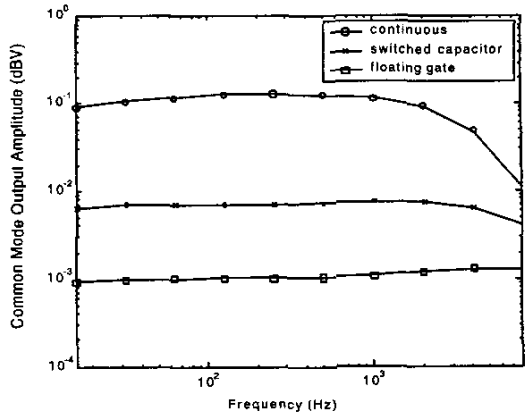


Figure 11: Measured differential input amplitude to common mode output amplitude over frequency for each amplifier

| Parameter | Continuous-time | Switched capacitor | Floating gate |
|---|---|---|---|
| Supply voltage | ±2.5V | ±2.5V | ±2.5V |
| Supply Current* | 36 μA | 32 μA | 37 μA |
| Gain | 39.4 dB | 39.2 dB | 39.3 dB |
| Bandwidth | 6.8 kHz | 7.2 kHz | 6.9 kHz |
| Input-referred noise (μV rms) | 2.5 | 5.3 | 2.5 |
| Dynamic range (1% THD) | 76 dB | 80 dB | 77 dB |
| CMRR (10 Hz – 5 kHz) | >83 dB | >87 dB | >91 dB |
| PSRR (10 Hz – 5 kHz) | >72 dB | >73 dB | >69 dB |
| Area (1.5 ìm technology) | 0.205 $mm^2$ | 0.207 $mm^2$ | 0.212 $mm^2$ |

Table 1: Experimental measurements of amplifiers (* denotes measurement taken from simulation)

## VI. CONCLUSIONS

We have designed and simulated a novel floating gate CMFB circuit. This circuit combines a large output 'signal swing with continuous-time operation. A test chip' has been fabricated, and experimental results demonstrate that the fully differential amplifier with the floating gate CMFB circuit has the lowest THD over the critical range. The use of the floating gate circuit provides the advantages of the switched capacitor CMFB circuit (i.e., lower distortion, larger output signal swing) with no switching noise, which allows it to be used in continuous-time applications. We have also compared the noise

performance of single-ended and fully differential versions of a LNA designed for biological signals. Noise performance was similar in the absence of digital interference, but when an interfering digital signal was included, the fully differential versions had a clear performance advantage.

## VII. ACKNOWLEDGEMENTS

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