Characterization of Aging Process in Power Converters Using Spread Spectrum Time Domain Reflectometry

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***Abstract*— This paper aims to find a new technique to predict the state of health of power converters by characterizing the most vulnerable components in the converter without affecting the normal circuit operation. Spread spectrum time domain reflectometry (SSTDR) can detect most of the aged components inside the converter while the converter is operational. Semiconductor switches and electrolytic capacitors are the two most sensitive components in power converter circuits, and this paper demonstrated how SSTDR can be used to determine the degradation of these components. Multiple sets of test data have been generated while the SSTDR process is applied to the power MOSFETs, IGBTs connected in a chopper circuit and to the aluminum electrolytic capacitors connected in an RC circuit. Analysis is done on these obtained test data to show how the SSTDR generated data are consistent with the aging of power MOSFETs, IGBTs and electrolytic capacitors.**

I. INTRODUCTION

Power converters are widely used in industrial applications where the uninterrupted operation is essential. These converters are subjected to high voltage, high power and high temperature applications. In the line of duty, these power converters experience sudden voltage or current anomalies. These anomalies could create permanent damage or severe deterioration of components used in the converter. In addition, the performance of a power converter degrades with time, and the degradation rate depends on several associated factors such as overload, ambient temperature, switching impulses, and so on. Power converters are periodically replaced in an industrial process, but without identifying the remaining life of the aged converter. If the power converters' state of health could be idntified with reasonable accuracy, the effective use of those converters could be ensured. To the knowledge of the authors, there is no established technique to predict the remaining life of the power converter in real time, and it is not possible to pinpoint the time to replace the converter so that any potential failure can be avoided. In order to identify the state of health of an entire converter, the aging process as well as state of health of affected components need to be measured first. A converter specific reliability model can be built based on the measured data for individual components.

Electrolytic capacitors and switching devices such as MOSFETs, IGBTs, BJTs are the primarily affected components in power converters. Components with degraded electrical characteristics eventually cause additional degradation which can lead to accelerated aging in a circuit provided the ciruit operates in closed loop (to stabilize voltage or current). Experimental study shows that the ON resistance or the junction voltage of a switching device (MOSFET, IGBT, diode etc.) increases with time, and this particular behavior could be explained using device physics. This higher ON resistance is responsible for increased conduction loss resulting in degraded performance. Equivalent series resistance (ESR) in a capacitor increases with aging which leads to additional loss across the device. Therefore, aging can affect the reliability of individual components as well as the reliability of the overall circuit. This research project applies SSTDR to identify the aging of power semiconductor switches in a simple chopper circuit with interchangable MOSFETs/IGBTs, and of electrolytic capacitors in parallel RC circuits with interchangable capacitors. The block diagram of the test setup using SSTDR is demonstrated in Figure 1.

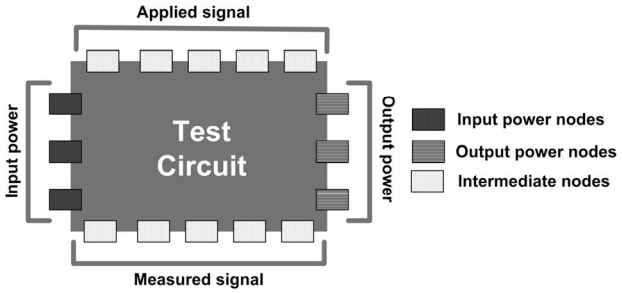


Figure 1. The proposed technique to identify aging of various components using reflectometry without altering the main power flow of the converter.

II. State of the Art Solutions to Identify Device Failure Mechanisms

Power semiconductor switches and electrolytic capacitors are known to be the two major components responsible for converter failure, and they have significantly higher failure rates than other components used in power converters. These converter failures may take place due to long time operation under regular operating conditions or due to short time operation under extreme stress conditions.

A. MOSFET: According to reference [1], 60% of the total failure occurs due to electrolytic capacitors breakdown and 31% of the total failure occurs due to the failure of semiconductor switches. Gate interface of power MOSFETs are susceptible to damage from any high voltage applied at the gate. In order to reduce switching loss, faster switching speed is required and hence smaller gate area is needed. Moreover, a thinner gate oxide layer assists in keeping the threshold voltage reasonably low. Therefore, this thin oxide layer makes the MOSFET susceptible to permanent damage caused by temporary over-voltages at the gate. The effect of this damage could be accumulated over time and would lead to a decrease in performance. Eventually this MOSFET will exhibit a complete switching failure.

The threshold voltage V_T of a MOSFET tends to increase with aging [2][3]. Increased threshold voltage is directly related to any increase in switching time. Therefore, the change in the threshold voltage can be considered as the precursor to failure [3]. ON resistance was found to be the most significant aging factor of power MOSFETs [4], and two aging measurement techniques for power MOSFETs are presented in [5]. The first technique demonstrates aging by introducing a thermal overstress situation having a constant operational temperature. During this test, the drain current was increased from 3A to 15A and the device fails to turn off when gate voltage reaches to zero. This phenomenon indicates the loss of gate control, and the ON resistance (R_{DS}) exhibits a sudden drop due to elevated drain current. Therefore, higher R_{DS} is consistent with aging and a sudden drop in the value of R_{DS} indicates the loss of gate control.

According to the second method of aging presented in [5], a stepped temperature (each cycle had duration of 50 minutes, and the device failed in 2.5 hours) is used to apply stress to the devices. The failure occurred as a result of increased resistance inside the device. As a result, the drain current dropped and the transistor failed to switch.

The effects of high temperature gate bias (HTGB) stress are presented in [6] on SiC power MOSFETs with voltage and current ratings of 1200V and 67A respectively. Devices were stressed at 150ºC temperature with gate to source voltage (V_{GS}) = +15V or -15V. Drain to source voltage V_{DS} was maintained at 0V during HTGB. Positive bias temperature stress (V_{GS} = +15V with 150^0C temperature) generally produces a positive shift in the threshold voltage (V_T) and negative bias temperature stress (V_{GS} = -15V with 150^0C temperature) induces a negative shift in V_T. Here it was shown that V_T tends to have a larger shift for larger temperature stress. Therefore, if the device is being operated under high temperature, eventually it will have higher/lower threshold voltage depending on the type of applied stress.

The major failure mechanism of discrete power MOSFETs for the stress conditions is the die attachment degradation [7]. The ON resistance was identified as a precursor of failure for the die-solder degradation failure mechanism for discrete power MOSFETs [8][9]. From the X-ray image taken after the degradation, it was observed that the die solder has migrated and voids have formed. This confirms that the thermal resistance from junction to case has increased during the test. This corresponds to the increase in the junction temperature and the ON resistance [7].

B. IGBT: Several studies are focused on precursor failure parameters for discrete IGBTs under thermal degradation caused by power cycling overstress. Collector-emitter voltage was identified as a health indicator in [10]. In [11], the maximum peak of the collector-emitter ringing at the turn off transient was identified as the degradation variable. In [12], the switching turn-off time was recognized as failure precursor; and switching ringing was used in [13] to characterize degradation. Reference [14] explains how threshold voltage, transconductance, and collector-emitter ON voltage could be used to identify aging. Here it was found that the oxide damage affects the threshold voltage; die attach degradation affects transconductance and the collector-emitter ON voltage.

C: Capacitor: The performance of electrolytic capacitor is affected by operating conditions such as voltage, current, frequency, and temperature. The primary failure mechanism of the electrolytic capacitor is the evaporation of the electrolyte solution. The evaporation is accelerated during operation due to ripple currents, over voltage, and temperature increase [15]. As the electrolyte solution dries up, the effective contact area between the electrodes decreases. This results in decrease in capacitance and increase in effective series resistance (ESR) which further increase with temperature (losses due to increase in ESR). This further accelerates the degradation and eventually leads the capacitor to fail completely.

Electrolyte loss causes a continuous rise of ESR according to $ESR = ESR_0/v^2$ [16]. $v=V/V_0$ denotes the normalized electrolyte volume. The capacitor will reach the end of its useful lifetime if it loses 30% to 40% of its electrolyte i.e. ESR increases by a factor of 2 to 3 [17].

Hence, there exist several real time methods to estimate the state of health of power converters [18]-[21]. However, they are suitable for detection of degradation of a specific component in the converter.

III. PROPOSED METHODOLOGY

A. Fundamentals of SSTDR: Most of the conventional techniques estimate converter relibility by measuring individual components' characteristics while they are disconnected from the circuit. Even they are characterized in real time, results applicable to individual components are not suitable for the prediction of the overall converter reliability. In order to overcome this limitation, spread spectrum time domain reflectometry (SSTDR) could be used to obtain several parameters of the individual components as well as the converter circuit. Reflectometry is conventionally used for locating wiring faults, and reference [22]-[28] presented several reflectometry techniques to identify aircraft wiring faults and aging. Using reflectometry, a high frequency electrical signal is sent down the wire and it reflects from any impedance discontinuity. The reflection co-efficient gives a measure of how much signal is returned and is given by ρ.

$$\rho = \frac{Z_t - Z_o}{Z_t + Z_o} \quad \text{(i)}$$

Where Z_0 is the characteristic impedance of the transmission medium and Z_t is the impedance of the terminating end of the transmission line. The time or phase delay between the incident and reflected signals provides the distance to the fault, and the observed magnitude of the reflection co-efficient provides the impedance at discontinuity.

It was discuussed in the previous sections how the electrolytic capacitors' ESR increases, capacitance decreases and MOSFETs' channel "ON resistance" (R_{DS}) increases due to aging. As the aging of these components' is directly related to the impedance variation, reflectometry method can be used to identify these gradual changes of impedance in a power converter by comparing these values with the reference values consistent with a new converter.

Time domain reflectometry (TDR) method was used in [29] to measure the parasitic parameters on printed circuit boards (PCB). [30] Presented characterization of interconnect parasitics in switching power converters using TDR. In addition, TDR was used in [31] [32]to detect two interconnect failure: solder joint cracking and solder pad separation. Techniques for prognostics solder joint degradation using TDR has been discussed in [33]. Capacitance of the pad in the CMOS process is estimated using "on wafer" TDR measurement system [34], and the method of extracting series resistance of capacitors is presented in [35] using TDR. The major limitation of TDR is the higher cost compared to other techniques and inability to use in live networks. In order to overcome the limitations of TDR, SSTDR was used to estimate the state of health of power semiconductor switches and electrolytic capacitors. SSTDR uses a sine wave modulated PN code as the test signal. SSTDR can be used for locating faults in aircraft wires [26] as well. A SSTDR setup is shown in Figure 2.

B. SSTDR operation: A sine wave generator (operating at 30–100 MHz) is being used as the master system clock in Figure 2. This generator's output is converted to a square wave via a shaper, and the resulting square wave drives a pseudo-noise digital sequence generator (PN gen). In order to use the SSTDR technique (S1 and S2 in position "2"), the sine wave is multiplied by the output of the PN generator, and the test signal is injected into the cable, and the other end of the cable is connected across the device under test. The received signal from the cable (including any digital data or AC signals on the cable, and any reflections observable at the receiver) is fed to a correlator circuit along with a reference signal. The received signal and the reference signal are multiplied, and the result is fed to an integrator. The output of the integrator is sampled with an analog-to-digital converter (ADC). A full correlation can be collected by repeatedly adjusting the phase offset between the two signal branches and the correlator output. The location of the various peaks in the full correlation indicates the location of impedance discontinuities such as open circuits, short circuits, and arcs (intermittent shorts).

C. Description of the test setup: The schematic of the test set up to find the correlated output using SSTDR is shown in Figure 3. A data acquisition system was used to continuously monitor and record the drain to source voltage (V_{DS}) of the MOSFET under test and the voltage across the series resistance, R_{Lim}; and R_{DS} of the test MOSFET is calculated from these two voltages. A basic chopper circuit was considered to test the MOSFET/IGBT using SSTDR method. The test circuit of electrolytic capacitor will be described in the next section. A personal computer was interfaced with the SSTDR hardware to control and monitor the correlated output. A thirty five foot long "CAT 5 twisted pair" cable was connected in between the chopper circuit and the SSTDR test system. Because of the uniformity of the CAT 5 cable impedance, a peak in correlated output is observed only at the starting point (due to the impedance mismatch between SSTDR hardware and CAT 5 cable) and at the far end of the cable (due to the impedance mismatch between CAT 5 cable and test point). The amplitude of the peak is dependent on the value of R_{DS} of the MOSFET under test, on the equivalent resistance of IGBT under test and on the value of impedance of the capacitor under test.

IV. EXPERIMENTAL RESULTS

A. SSTDR applied to power MOSFETs

Multiple power MOSFETs were aged using power stress in a controlled environment. A 2 V DC voltage was applied across the FDP 3672 N-channel power MOSFETs to apply power stress and the MOSFETs were kept in controlled temperature chamber at 110°C using a Delta 9059 environment chamber. The gate voltage was 12 V during the accelerated aging procedure. Due to the high power dissipation (~8W) in each MOSFET, the case temperature

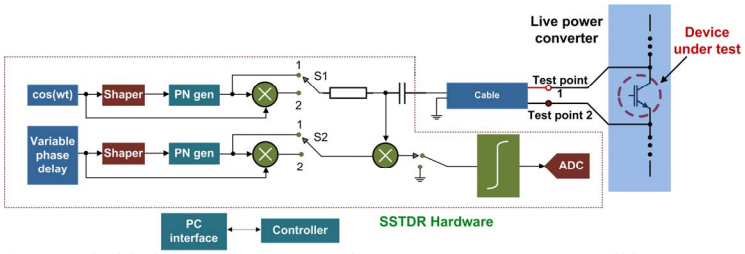


Figure 2. The block diagram of an STDR/SSTDR test system (S1, S2 will be at position "1" for STDR and S1, S2 will be at position "2" for SSTDR) [26].

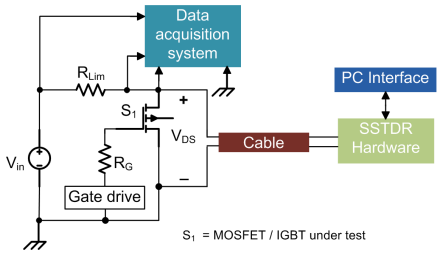


Figure 3. The test set up to apply SSTDR in MOSFET/IGBT.

reached at 170°C within 10 minutes which was stabilized between 160°C~170°C during this accelerated aging process. The above procedure was applied to four different MOSFETs M2, M3, M4 and M5. M1 was used as the reference MOSFET as zero stress was applied to it. These stressed MOSFETs were cooled down to the room temperature after accelerated aging, and the ON resistances (R_{DS}) were measured using data acquisition system. It was found that R_{DS} increases with aging for all four MOSFETs. Change in R_{DS} was in the range of 2 ~ 20 mΩ for these MOSFETs under test.

SSTDR was applied to M1 – M5 in order to compare the characteristics of M1 with the aged MOSFETs. Data from SSTDR test system were analyzed in MATLAB, and the correlated outputs vs distance characteristics are shown in Figure 4.

The correlated amplitude is the true measure of the reflected power and the reflected power is a function of the impedance at the far end of cable. If correlated waveform can be normalized to the highest peak in the data, all amplitudes would be a fraction of the maximum. "R_{DS}" calculated from the data acquisition system, and the peak amplitude of the correlated output at the far end of the cable found in SSTDR test system (Figure 4) for M1 – M5 are shown in table 1. From the difference in correlated output (Figure 5) at the far end of the cable, it was found that for higher difference in R_{DS} (between M1 and M5), the difference in amplitude of correlated output was also higher and, for lower difference in R_{DS} (between M3 and M4), the difference in amplitude of correlated output was also lower. SSTDR hardware generates several sampled values of correlated outputs along the CAT 5 cable. As the MOSFETs were connected at the far end of the cable, the peak value of correlated amplitude at this point is different for various MOSFETs under test. These differences were calculated by subtracting the correlated amplitudes of one MOSFET from another MOSFET. The difference in correlated output was 147 when difference in R_{DS} was 20.48 mΩ, and the difference in correlated output was 3 when difference in R_{DS} was 0.64 mΩ. So, the difference in ON resistance can be predicted from the variation in amplitude of the correlated outputs. As the value of ON resistance is directly related to the state of health of power MOSFETs, the variation in

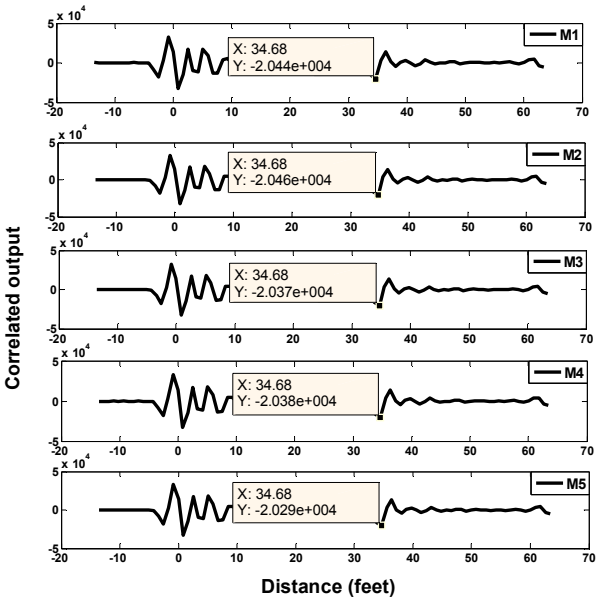


Figure 4. Correlated output and for five different MOSFETs (M1, M2, M3, M4 and M5) with respect to distance.

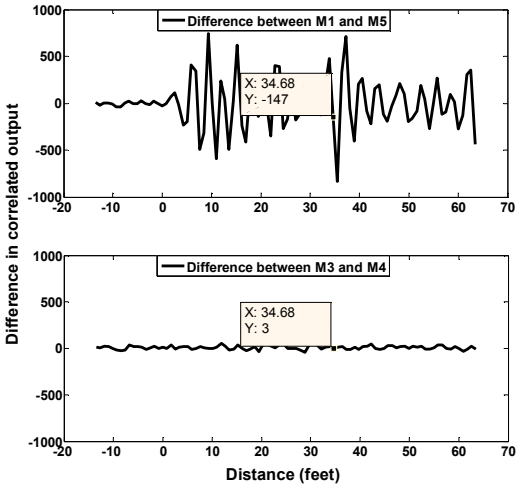


Figure 5. Difference in correlated output.

correlated output is a true representation of the MOSFET aging.

Table 1: Correlated output and measured R_{DS} for several MOSFETs aged by applying both power and temperature stress.

MOSFETs	**M1 [New]**	**M2 [Aged]**	**M3 [Aged]**	**M4 [Aged]**	**M5 [Aged]**
Duration of aging	--------	60 Minutes	120 Minutes	180 Minutes	240 Minutes
R_{DS} (mΩ) before aging	44.02	44.3	43.95	44.31	44.5
R_{DS} (mΩ) after aging	44.02	45.8	51.63	51.90	64.5
Correlated amplitude	-20435	-20463	-20373	-20376	-20288

B. SSTDR applied to IGBTs

Three IRGI4090PbF trench IGBTs were stressed in a controlled environment, and SSTDR technique was applied to identify the aging of these IGBTs. A 2.4 V DC voltage was applied between collector and emitter of the IGBTs and due to the high power dissipation (~8.5W) across it, the surface temperature increased to 150°C within ten minutes. The IGBTs were placed in a controlled temperature chamber at 110°C. The above procedure was applied to three different IGBTs for different time durations. The devices were cooled down to the room temperature, and the characteristics were measured after aging. It was found that the collector to emitter voltage (V_{CE}) siginificantly increased due to this accelerated aging. SSTDR technique was applied to the aged IGBTs (G2, G3, G4) and to the new IGBTs (G1) for comparison purpose. Due to the change in V_{CE}, the equivalent resistance of these IGBTs also changed. V_{CE}, equivalent resistance (R_{CE}), and corresponding SSTDR correlated amplitudes for both aged and new IGBTs are given in Table 2. The gate voltage was 15V, series resistance (R_{Lim}) was 4Ω and V_{in} was 12V (Figure 3) while taking the measurements shown in Table 2.

Table 2: Correlated output and measured R_{CE} for several IGBTs aged by applying power stress.

IGBTs	**G1 [New]**	**G2 [Aged]**	**G3 [Aged]**	**G4 [Aged]**
Duration of aging	--------	60 Minutes	120 Minutes	180 Minutes
V_{CE} (V) before aging	0.953	0.957	0.955	0.957
V_{CE} (V) after aging	0.953	0.975	1.1	1.5
R_{CE} (mΩ) before aging	35.01	36.04	36.004	36.04
R_{CE} (mΩ) after aging	35.01	36.79	41.706	60.606
Correlated amplitude	-21038	-20902	-20841	-20705

C. SSTDR applied to electrolytic capacitors

Three SEK102M010ST aluminum electrolytic capacitors were aged using temperature stress in a simple parallel RC circuit. The circuit diagram is shown in Figure 6. Capacitors C2, C3, C4 were aged at 150℃, 160℃, and 170℃ resopectively for one hour. The change in capacitance and ESR were measured after reaching at room temperature using an LCR meter at 60 Hz. SSTDR was applied to these aged capacitors (C2, C3, C4) and a new capacitor (C1) while the applied voltage in Figure 6 was 2.83 V (rms) 60 Hz AC instead of DC. The change in capacitance, in the

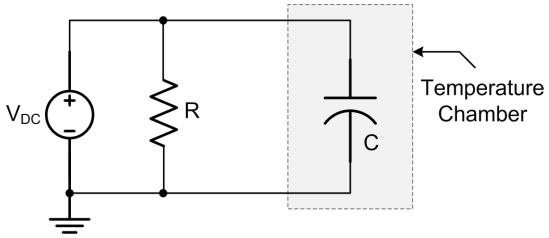


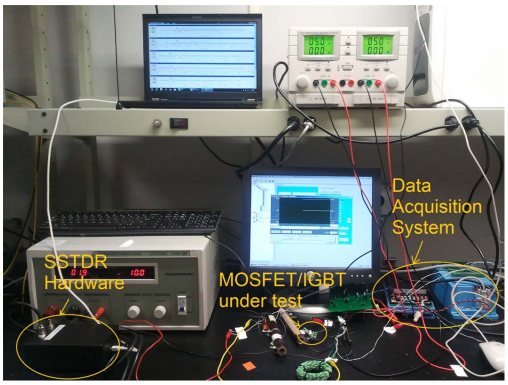
Figure 6: Aging procedure of electrolytic capacitor.

Table 3: Variation in correlated output with ESR and capacitance variations of electrolytic capacitors under temperature stress.

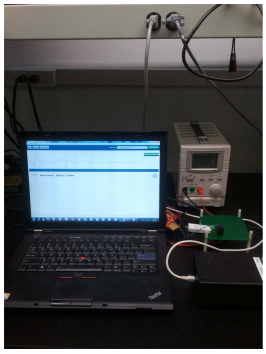
Capacitors	**C1 [New]**	**C2 [Aged]**	**C3 [Aged]**	**C4 [Aged]**
Capacitance (μF) before aging	1003	1001	998	997
Capacitance (μF) after aging	1003	968	953	942
ESR (mΩ) before aging	197	197	200	195
ESR (mΩ) after aging	197	208	223	220
Correlated amplitude	-17460	-17311	-16402	-16440
Ripple voltage (V) before aging (p-p)	1.88	1.82	1.86	1.86
Ripple voltage (V) after aging (p-p)	1.88	1.94	1.96	1.96

ESR, and correlated outputs from SSTDR hardware for aged capacitors (C2, C3, C4) and the new capacitor (C1) are given in Table 3.

It is quite clear from Table 3 that the ESR and the capacitances change due to thermal aging, and the SSTDR technique can identify these variations. Capacitor ripple voltages increased due to the variations in ESR and self capacitance. The experimental setup used to identify and measure the aging in components is shown in Figure 7.



(a)



(b) (c)

Figure 7: Experimental set up. (a) SSTDR technique applied to MOSFET/IGBT under test, (b) Accelerated aging of MOSFET/IGBT in temperature chamber, (c) SSTDR technique applied to electrolytic capacitor under test.

I. CONCLUSIONS

A new measurement technique to identify the aging process of various components used in power converters has been presented in this paper. This method involves SSTDR to identify the aging of various components in a non-interfering manner, and this paper shows the feasibility of using SSTDR method to identify the aging of power MOSFETs, IGBTs, and electrolytic capacitors from the impedance variation due to aging. The aging procedure i.e. power stress, thermal stress were applied to make semiconductor switches and electrolytic capacitors aged and the corresponding measurable quantities were identified. These individual SSTDR data could be used to predict the overall reliability of the converter, and the task to estimate the remaining life of a specific power converter has been left as a future work.

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