Low Cost High Linearity Solid State Digital Double Boxcar*

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In this article, we describe a digital solid state double boxcar of infinite holding time and very high linearity. It uses a Hewlett–Packard (HP2212 A-M3) voltage-to-frequency converter (VFC) whose output is accumulated on a running counter, thereby providing signal averaging with an infinite holding time. The combination of FET signal gates with zero offset and the highly linear VFC results in a linearity of better than $\pm 0.01\%$ over an input range of ± 1.0 V, which is a considerable improvement over that available with other digital boxcars. Integrated circuit pulse generators of high stability provide gating times from a fraction of a microsecond to many seconds. A unique monitoring system allows ease of adjustment with a simultaneous "master" display of all gating and signal functions. Other features of this boxcar are extreme compactness, low cost, and very high stability.

INTRODUCTION

ONE of the most common problems which plague an experimentalist is the problem of improving the signal-to-noise ratio. For this reason a number of devices utilizing phase sensitive detection and signal averaging have been developed: the cw integrator, or "lock-in," and the gated integrator, or "boxcar." The former circuit is appropriate to situations in which a periodic signal has a very narrow frequency spectrum whereas the latter is appropriate to situations in which a periodic signal has a broad spectrum. The boxcar is particularly valuable in pulsed nuclear magnetic resonance applications.

The early boxcars were analog, or finite storage time, devices[1–4] in which a capacitor is used both to store and to integrate the signal. There are in the double boxcar two capacitors. The signal capacitor samples the signal at a particular interval in time whereas the reference capacitor samples the signal baseline at a later time. Since only the difference voltage is recorded, the low-frequency "noise," or drift, is greatly attenuated. The capacitors must hold the information for a time long compared to the time between cycles; accordingly, the finite discharge time of even the best available capacitors limits the use of this boxcar to situations in which the spin–lattice relaxation time T_1 is of moderate length ($\sim$100 sec). A recent advance occurred with the digital, or infinite storage time device, of Ware and Mansfield[5,6] (WM). This circuit does not require that the capacitors store information for the entire measurement interval; rather, they must store information only so long as is required to convert the information to a "permanent" form, such as the reading on a counter. The capacitors can then be discharged until the next sampling cycle. Once the voltage is digitized, days could pass before the next sampling without degradation of the averaging process. In the WM digital boxcar, the voltage is converted to a time interval through a comparator and ramp circuit and is in turn recorded on a time interval counter. Unfortunately, the linearity of their boxcar is limited to approximately 1%.[5] This linearity would provide only marginal accuracy in the measurement of NMR relaxation times. An added disadvantage of the WM boxcar is that it uses tubes and is thus somewhat bulky and expensive to construct. For these reasons we developed an economical solid state digital double boxcar which combines the advantages of the WM digital boxcar with a great improvement in linearity, compactness, and cost.

I. PRINCIPLE OF OPERATION

The heart of the present boxcar circuit is a voltage-to-frequency converter made by Hewlett–Packard. A *direct* application of this VFC as a signal averager is not appropriate to pulsed NMR in solids where decay times can be of the order of microseconds, since the VFC has a relatively low count rate (100 kc/V). Fortunately, however, this difficulty can be circumvented by using the VFC only to monitor the voltage on previously charged capacitors. Hence the VFC acts as an analog-to-digital converter rather than as a signal averager. The signal averaging is done later using a counter. As an ADC the Hewlett–Packard instrument has much to offer. It has very high linearity and long term stability. A full scale input on the least sensitive or 1 V range produces an output of 100 kc which is more than adequate under these conditions. The input is differential and of very high input impedance, which allows direct attachment to the integrating capacitors. Polarity lights and an electrical signal provided by the VFC indicate whether the counts are to represent the magnitude of a positive or a negative input.

The signal is initially fed into an integrated circuit operational amplifier source follower with an input impedance of 1 MΩ and an output impedance of less than 0.2 Ω (Fig. 1). This prevents loading of the signal while the charging gates are on. These are series gates using junction

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[1] D. F. Holcomb and R. E. Norberg, Phys. Rev. **98**, 1074 (1955).
[2] R. J. Blume, Rev. Sci. Instrum. **32**, 1016 (1961).
[3] J. Reichert and J. Townsend, Rev. Sci. Instrum. **35**, 1692 (1964).
[4] D. C. Ailion, Ph.D. thesis, University of Illinois (unpublished).
[5] D. Ware and P. Mansfield, Rev. Sci. Instrum. **37**, 1167 (1966).
[6] A solid state version of the Ware and Mansfield circuit has been constructed by members of C. P. Slichter's research group [C. P. Slichter (private communication)].

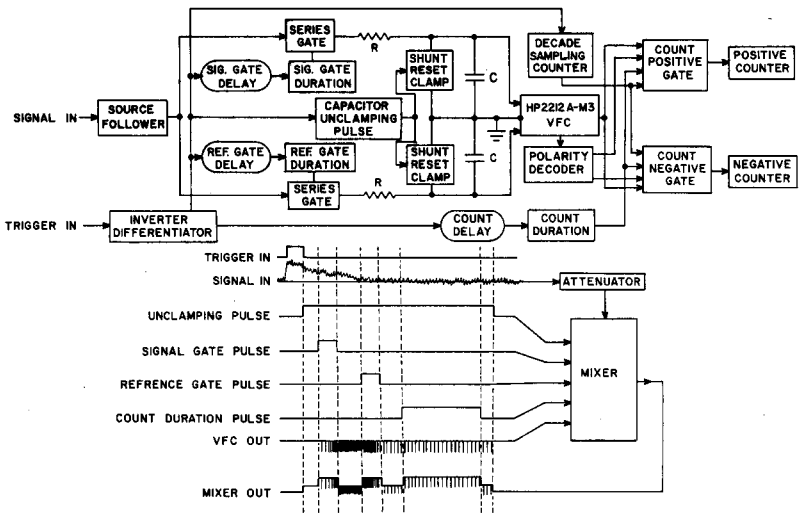

FIG. 1. Block diagram of boxcar circuit.

field effect transistors. In addition, shunt FET gates keep the integrating capacitors grounded except during the sampling period. After both capacitors receive their charges, the output frequency of the VFC, which is directly proportional to the voltage difference between the two integrating capacitors, is fed into a digital counter for a set period of time. Succeeding samplings generate counts which are automatically accumulated with the rest. By keeping track of the total number of samplings a signal average is obtained, thereby improving the signal-to-noise by the square root of the number of samplings taken.[5]

A potential problem can occur when the signal changes sign relative to the reference since the VFC can produce an output frequency proportional only to the *absolute* value of the input. This problem is particularly acute when the signal is less than the noise, for then the average noise difference between signal and reference would be rectified. The problem can be avoided in two fashions. One method would be to bias the reference input to the VFC to a level greater than the noise level, thereby guaranteeing that the polarity of the signal channel output relative to the reference channel output never changes. However, this requires a sizable offset, which has the disadvantage of limiting the precision and stability. An alternative method, which is employed in this circuit, is to use the polarity indicator connection on the back of the VFC to operate gates which allow positive and negative readings to accumulate on separate counters. Subtracting these two averages removes this "noise rectification," thus allowing operation about the zero level with negligible offset.

II. CIRCUIT DETAILS

A. Source Follower and Function Switch

The source follower input (Fig. 2) is constructed from a Motorola MC1433P operational amplifier integrated circuit, which has provisions for adjusting out the voltage and current offsets. This is fed into a function switch S_1 (Fig. 3) which has the following provisions:

(1) In the "double" position, the circuit operates in the differential mode.

(2) On "single," single boxcar operation is obtained with the reference gate held off.

(3) The "RC cal" position is used to adjust the integrator RC of the signal input to equal the charging gate width of the signal gate, thereby allowing the signal capacitor to charge always to about 63% of the input. This conveniently provides some integration even for a single sampling.

(4) The "balance" position connects the differential input to a constant voltage level so that the RC of the reference input can be matched to that of the signal input by producing a null output.

In practice, we gang switch the different values of integrating capacitors simultaneously and have separate potentiometers to control the R values.

One disadvantage of this source follower is that its bandwidth is only 100 kc. If it is desired to study the shape of

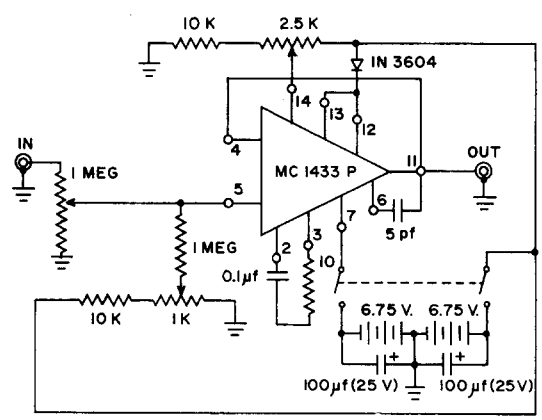

FIG. 2. Source follower schematic diagram.

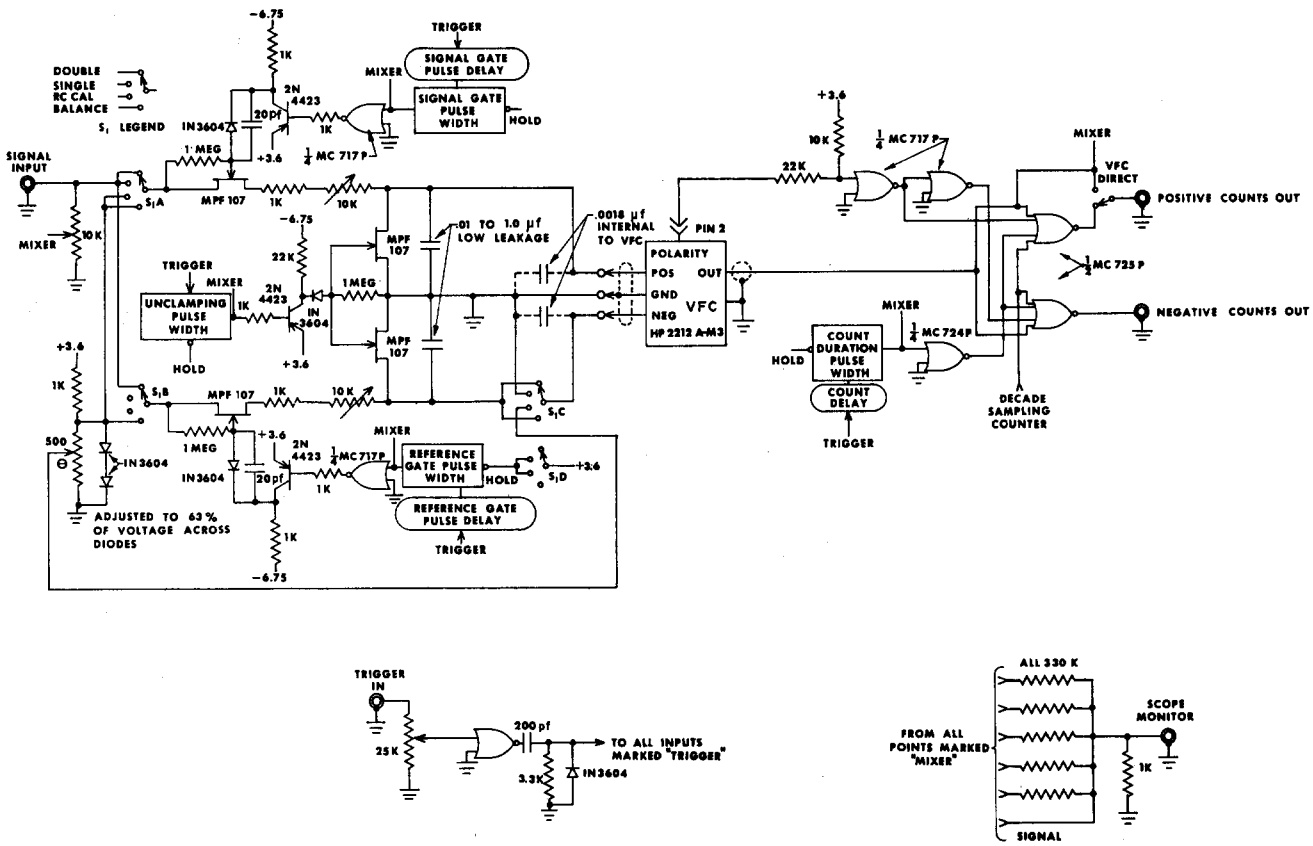

FIG. 3. Boxcar schematic diagram. (The unmarked nor gate following the trigger input is ¼ MC724P.)

signals whose decay times are less than 10 μsec, one should remove the source follower and suffer the resulting reduction of signal due to loading.

B. Series Gates and Shunt Reset Clamps

Fixed 1 kΩ resistors in series with the gates minimize the slightly nonlinear, current dependent resistances of the FET gates. Other than this, the FET's are ideal gates since they act as simple resistors for both positive and negative excursions about their dynamic origins with no offset problems and no gate pulse feedthrough.

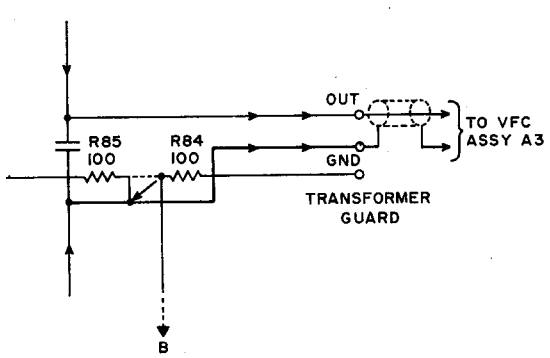

FIG. 4. Modification of HP2212A-M3. Disconnect R85 from R84 and connect to ground as shown.

The reset gates, which are also FET's, very effectively reset the capacitors exactly to ground level between each sampling period since again no offset voltage exists. This avoids the problem of drift due to temperature variations of an offset voltage, a problem which plagues WM's boxcar.[5]

C. Voltage-to-Frequency Converter

The VFC has three input connections: positive, negative, and common (which is grounded). The output and input leads are in cables that connect through a plug to the rear of the unit. Provision is made at the plug for the polarity indicator connection, but a new wire must be added to bring this signal out for decoding. Another slight modification must be made internally to the input circuit of the VFC to make the input refer to ground instead of to its common mode (Fig. 4). This isolation is necessary in order to suppress cross channel coupling between the signal and the reference channels.

D. Integrated nor Gates Used in Switching Circuits

One-shot multivibrators of very low pulse jitter and good stability against power supply variations can be made from MRTL (Motorola) integrated circuits.[7] Each integrated package consists of four gates, each of which

[7] D. E. Lancaster, Electron. World 75, No. 3, 50 (1966).

contains two high speed transistors back-to-back with a common load resistor [Fig. 5(a)]. An input on either transistor will saturate the output to near ground level. Supply voltage requirements are not critical since the 3.6 V specified is nominal and up to 4.5 V is acceptable. Figures 5(b) and (c) illustrate the manner in which these gates are wired as one-shots. The high value internal collector resistor of the MC717P on the left of the basic one-shot circuit allows this stage to saturate with a very small input current, permitting "R" to be fairly large (200 kΩ); whereas the small internal collector resistance of the MC724P on the right provides fast recovery, about two times the minimum pulse width. The trigger must be positive and short compared to the pulse width. It is applied to the companion transistor in the gate on the right, forcing the other collector to ground and initiating the pulse. Care should be used to shield the leads going to the capacitors mounted on the appropriate range switches and to the variable pots, since these are high impedance circuits and pickup from adjacent pulses can false trigger them. By differentiating the output of the right hand one-shot stage, the circuit provides a sharp positive going spike at the end of its pulse sequence. This produces a delayed trigger for the succeeding pulse generator [see Fig. 5(b)] which uses the same basic one-shot circuit but in addition has a saturated stage which serves as an inverting buffer to square the output. This produces a square fast rising positive pulse which controls the switching gates [Fig. 5(c)]. In order to obtain good temperature stability, we used silver mica and (for the longer pulses) tantalytic capacitors, since these have very good temperature coefficients. We found that the pulse width is of the order of 0.7 RC and the rise time is less than 100 nsec. Each of the gating functions plus the VFC output combined with the input signal can be monitored simultaneously on a 'scope.

E. Polarity Decoder and Gate

The polarity of the VFC input can be decoded by noticing that, at pin 2 of the power plug, the voltage is

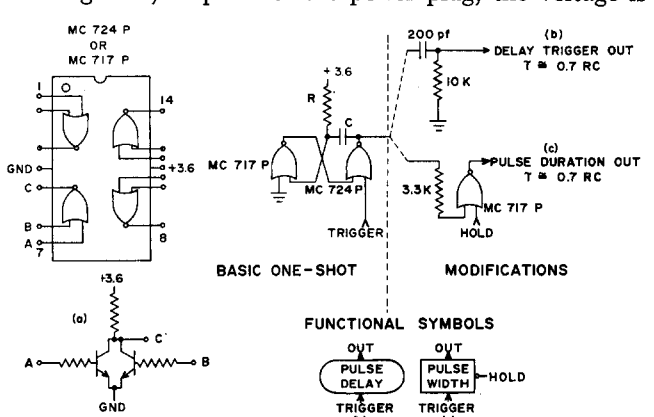

FIG. 5. Integrated pulse generator schematics. (a) Basic integrated circuit, (b) one-shot delay trigger, and (c) one-shot pulse width generator.

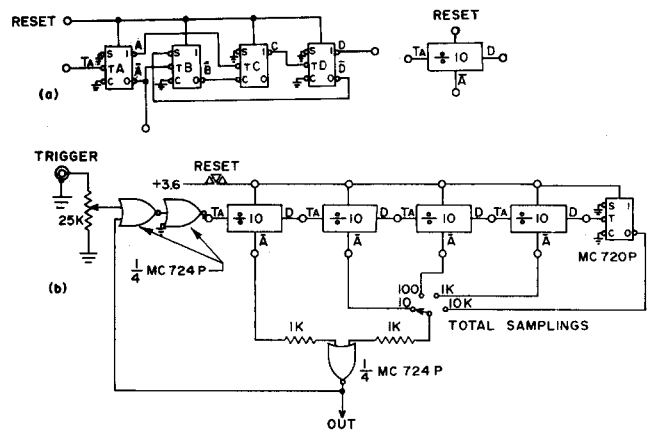

FIG. 6. Sampling counter. (a) Basic decade counter schematic (basic divide by 10 circuit with functional symbol; each J-K flipflop ¼MC776P). (b) Sampling counter schematic.

zero when the input is positive and −27 V when the input is negative. The polarity decoder (see Fig. 3) consists of two MC717P gates biased so that when the VFC input polarity goes from positive to negative the two decoder gates switch such that the first gate goes from zero to +4 V and the second gate goes from +4 V to zero. These outputs and the VFC output are simultaneously applied to two MC725P four-input nor gates. The outputs of these have the counts diverted into positive and negative channels and then fed into counters. Other inputs to the four-input gates come from the count duration pulse width generator which controls the total counts per sampling and from a decade sampling counter. The decade sampling counter (Fig. 6) records the accumulated samplings taken and stops the VFC output after 10, 100, 1000, or 10 000 samplings as desired. This makes it easy to calculate the average counts per sampling.

III. OPERATING CONSIDERATIONS

A. Power Requirements

Power requirements are nominal, less than 40 mA for all but the sampling counter which requires about 200 mA. Good regulation is required for the boxcar power supply to assure stable pulse widths. We observed that a 1% increase in power supply voltage resulted in a 0.3% decrease in pulse width. However, the sampling counter is less critical. The −6.75 V supply consists of a mercury battery wired directly into the circuit since current requirements are extremely low.

B. Equipment Requirements

Total equipment needed, in addition to the source follower, boxcar circuit, and digital sampling counter (which can all be constructed), are the following: a voltage to-frequency converter, like the HP2212A-M3; two simple pulse counters[8]; and appropriate power supplies.

[8] The pulse counters which we used can be cheaply constructed and are described in the succeeding paper.

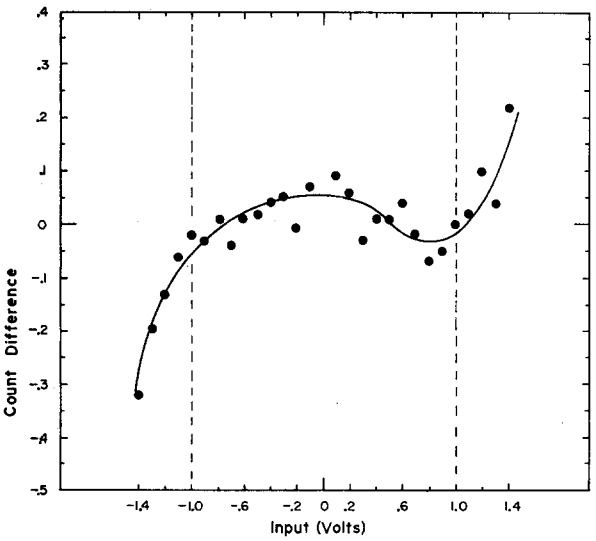

FIG. 7. Linearity plot. The vertical axis represents the *difference* between the actual number of counts and the number of counts that would have been obtained from a perfect straight line through the ±1.0 V points. The horizontal axis represents the input voltage. The average slope drawn through ±1.0 V points ≈ 630 counts/V.

C. Calibration Procedure

(1) Switch the VFC range to +cal and adjust the count duration pulse for total counts per sampling. This represents the 1 V input (e.g., 10 msec gives 1000 counts/V).

(2) Adjust signal gate widths as desired (signal gate and reference gate equal).

(3) With the VFC range on 1 V, switch the boxcar to "RC cal" and adjust the signal RC to null (no output from VFC). If the RC calibrate pot has been adjusted to 63% of its maximum range, then the signal RC equals the signal gate width.

(4) Switch the boxcar to "balance" and adjust the reference RC until null is reached. This gives optimal common mode rejection.

IV. PERFORMANCE

A. Linearity

We have been careful to keep nonlinearity to a minimum. We used an operational amplifier of 60 000 open loop gain as a source follower with unity feedback and 0.01% linearity. The VFC is stated to be linear to within 0.02% over short term. In fact, it is much better. The nonlinear FET gates are probably the worst offenders. We measured the linearity of the system by feeding to the boxcar a mechanically chopped signal in 0.1 V steps from −1.4 to +1.4 V. The signal amplitude was measured before the chopper to an accuracy of ±0.1 mV using a Fluke differential voltmeter. Plots were made of output vs input (Fig. 7) for an integrating R equal to 11 kΩ. As can be seen, the count difference varied by less than ±0.1 counts over a 1200 count interval corresponding to inputs from −1.0 to 1.0 V.[9] Thus we have a total system linearity of better than ±0.01%. We repeated the measurement for R of 1 kΩ (the minimum value) and found that the system linearity was then ±0.02%. The slight deterioration in linearity obtained using a small R is consistent with the notion that the nonlinearity is due to the FET gates, since a variation in the resistance of the FET's will have a proportionately larger effect with a small series resistance than with a larger series resistance. We observed no measurable baseline drift and no offset once the VFC zero adjustment was made.

B. Repeatability

The repeatability in number of counts was measured using the +cal input of the VFC. The counts were measured on repeated samplings and were found to vary by no more than ±1 count per 10 000. This can also be observed by inspecting the deviations from the mean slope of the right hand side of the curve of Fig. 7.

C. Long Term Stability

The long term drift was observed to be 0.1 count out of 600 counts over a 2 h interval after warmup. This excellent stability (0.01%/h) is of the order of the repeatability and is undoubtedly due to three features of our circuit: First, the HP2212A-M3 has a rated long term stability of 0.001%; the use of FET gates with zero offset to clamp the capacitors to ground has avoided offset instabilities as discussed in Sec. II.B; and, finally, the use of solid state devices and highly regulated power supplies has avoided all drift due to power supply variation and ac pickup.

ACKNOWLEDGMENTS

We wish to thank Professor C. P. Slichter, M. Schwartz, and P. Spencer for sending us a copy of their solid state version of the Ware Mansfield boxcar, as this gesture certainly inspired our present effort. We also wish to thank Professor W. Seward and Dr. J. F. Harmon for reading our manuscript. M. D. Julian aided us in obtaining the linearity data.

[9] In order to obtain optimum linearity, it is necessary to adjust the +1 V and −1 V calibration controls on the VFC to give equal counts for equal positive and negative signals.