Plasma-etched polymer waveguides for intrachip optical interconnects

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ABSTRACT

Optical intrachip communication offers the potential advantages of high speed and lack of electrical interference. We report on progress made on an interconnect design using GaAs LEDs, polymer waveguides, and photodiodes in a silicon substrate. The polymer waveguides are fabricated in polyimide or polystyrene materials, and are patterned by reactive ion etching with a tri-level resist system. The photodiodes are of two designs, including one in which the depletion layer lies directly below the waveguide. The LEDs are fabricated from GaAs deposited by MOCVD on a Ge lattice-matching layer placed between the GaAs and the silicon substrate. Test results are presented for the individual components.

1. INTRODUCTION

Digital interconnection using optical transmission is receiving attention as a means for short-range communication, both between separate integrated circuit chips (interchip connections) and within components on the same chip (intrachip connections). The advantages of optical techniques over conventional metallic wires or lines include high speed and immunity to noise pickup and generation, a problem especially associated with capacitive coupling on closely-spaced high speed electronic connectors. The purpose of this paper is to present progress made toward investigating polymeric rectangular waveguides used in conjunction with integrated optical sources and detectors for intrachip communication on a single silicon chip.

We selected a test configuration which has several examples of each of the three elements needed for intrachip connection on one layout: LEDs, waveguides with various lengths, and photodiodes of two different styles. The plan for the test configuration is shown in Figure 1.

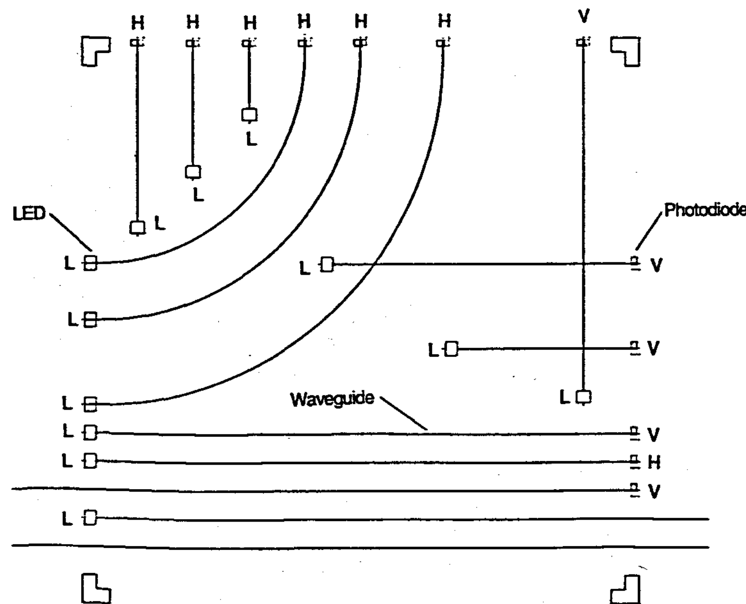


Figure 1. Test layout for the intrachip optical interconnect system, showing LED sources (labeled L*), waveguides, and two styles of photodetectors (labeled* V *and* H*).*

As can be seen, the waveguides linking the LEDs to the photodiodes include both straight and curved sections as well as intersections, since these elements may be expected to be found in any practical application of intrachip waveguiding. The photodetectors fall into two categories, as described in detail in a later section.

As a substrate, we chose a wafer of p-type silicon (Monsanto, boron doping, approximately 25 ohm-cm) with thickness of 0.016" and 100 orientation. A 1.47 μm thick layer of SiO_2 was plasma deposited on the entire surface of the wafer to act as an insulator and optical cladding for the waveguides. Several 1.25 x 1.25 cm test chips were cut from this wafer by a diamond saw. These samples then became test pieces for fabricating waveguides, detectors, and sources. In the initial tests reported here, each of the components was evaluated separately.

2. POLYMER WAVEGUIDES

Polymeric materials were selected for this waveguide study due to three attributes of polymers: 1) their ability to flow, planarize, and fill gaps which occur at the edges of the sources and detectors due to the processing steps; 2) the ease of forming the waveguide sides by dry etching; and 3) their relatively low temperature deposition and processing, avoiding disruption of deeper electronic layers by late high temperature processing.

Since the waveguide material must have a higher optical index of refraction than the SiO_2 cladding region (n=1.48) for true guiding to occur, we investigated polyimide (n=1.7) and polystyrene (n=1.58). Figure 2 shows the design dimensions of the waveguide cross-section, with the polymer guide situated on top of the SiO_2 cladding layer. The guide is multimode; for a 2 μm x 8 μm polyimide guide on SiO_2, there are approximately 28 E^y modes whose electric field is polarized predominantly parallel to the SiO_2 cladding, and approximately 20 E^x modes polarized predominantly perpendicular to the cladding layer.

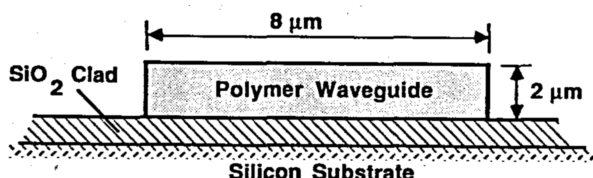


Figure 2. End view of polymer waveguide dimensions. SiO_2 forms the cladding layer.

The polyimide (DuPont PI-2550) was applied uniformly to the entire chip surface by spin-casting at 5000 rpm for 120 seconds; its thickness was approximately 2 μm by SEM measurement. Chips with no electronic components were used for these initial waveguide characterization tests. The film was baked at 170°C for 70 minutes, then cured in a 260°C oven for 150 minutes.

The polystyrene was spun cast on additional pieces at 2500 rpm for 60 seconds. Its thickness was approximately 1.1 μm. This layer was baked at 170°C for 70 minutes, but no further curing of the polystyrene was done.

Both polymer samples were patterned into the waveguide structures shown in Figure 1 by using a reactive ion etching (RIE) process in conjunction with the special tri-level resist scheme shown in Figures 3 and 4. A layer of SiO_2 (32 nm thick) was first plasma-deposited on top of the polymer. Then standard photoresist was spun on top of this SiO_2 layer, and optically patterned and wet etched. This photoresist pattern formed the mask for a 3 minute CHF_3 RIE of the SiO_2 upper layer as shown in Figure 3. This layer then became the mask for a 15 minute O_2 RIE of the polymer layer, resulting in the waveguide sides as diagrammed in Figure 4.

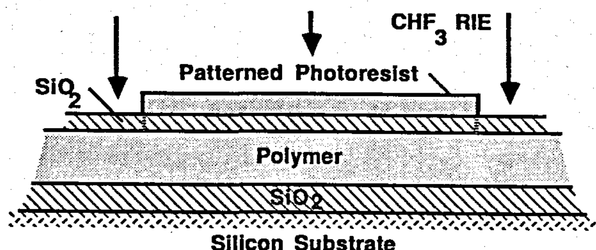


Figure 3. First step of tri-level resist technique for RIE of polymer, in which SiO_2 is patterned by CHF_3.

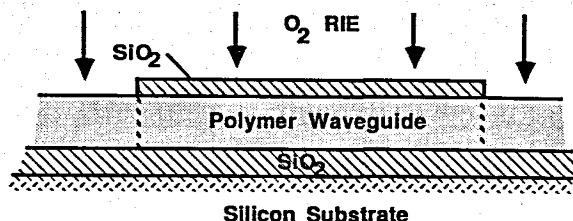


Figure 4. Using SiO_2 as a mask, the polymer is patterned into waveguides by O_2 RIE.

Being a directed dry etch, RIE has the advantage over wet etching techniques of producing very straight, smooth sidewalls on the waveguides, with little undercutting. An SEM of the resulting guides of both polyimide and polystyrene showed clean, sharply defined sidewalls, especially in the polyimide.

3. PHOTODETECTOR DESIGN

The photodetectors must possess relatively good sensitivity at the wavelength produced by the LEDs, and must couple light efficiently from the end of the waveguide. Since the LEDs are made from GaAs, their peak emission is near 870 nm. Fortunately, photodiodes fabricated directly in the silicon substrate have high responsivity at this wavelength, so designs incorporating an n+ doped region in the p substrate were investigated. For effective coupling, these designs are of the tapered-cladding type, shown in side view in Figure 5, where the cladding is gradually terminated at the detector site, allowing the waveguide to lie directly over the junction region. Since the index of refraction of silicon is much higher than the waveguide material, the normally guided modes are lost into the silicon for efficient collection at this point.

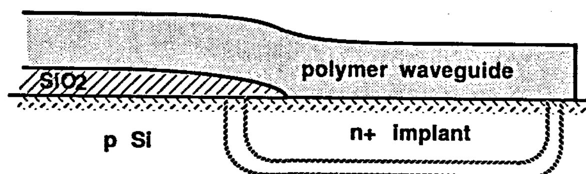
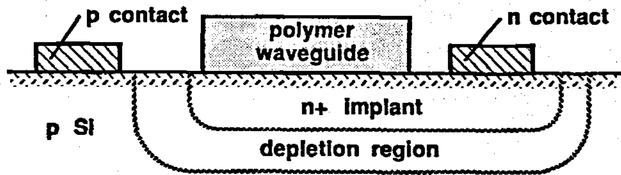


Figure 5. Side view of the tapered-cladding photodetector design.

Two styles of photodiode doping patterns were tried, differing in the lateral position of the depletion region associated with the junction. The first design, shown in end view in Figure 6, has an n+ region that extends entirely under the width of the guide; the depletion region (where effective hole-electron pair generation takes place) therefore also stretches under the entire width. This design is labeled a "horizontal" photodiode. A drawback of this diode is that photons from the waveguide must pass through the n+ region before reaching the depletion layer. Any photons absorbed in the n+ region produce minority carriers which quickly recombine without adding to the detector current.

To place the depletion region closer to the waveguide, the "vertical" design shown in Figure 7 was investigated. Here the n+ doping region stops short of the waveguide width, placing the depletion layer directly under the guide. Most photons from the guide enter the depletion region immediately.



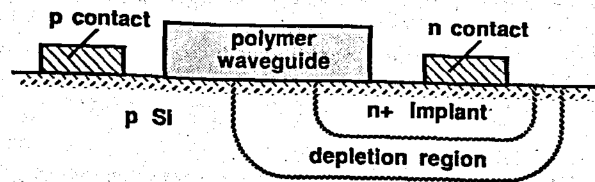


Figure 6. End view of the "horizontal" style photodiode, with the implant region under the waveguide width.

Figure 7. End view of the "vertical" style photodiode, with a vertical section of the depletion region under the waveguide.

Samples of each of the photodiode styles were fabricated in the silicon chips by standard photoresist techniques. The layer of SiO_2 was patterned for use as an ion implantation mask for a 300 KeV beam of As^+ dopant to form the n+ region. The n impurity level achieved was approximately $9 \times 10^{18}/cm^3$. A p+ region (not shown) immediately under the p contact was formed by ion implantation with B^+ dopant at 60 KeV. Contacts were evaporated using Si-saturated aluminum by the lift-off technique.

The finished photodiodes were tested for responsivity versus back-bias voltage using a HeNe laser and high-accuracy current amplifier. The results for samples of each style are shown in Figure 8. As can be seen, the typical vertical photodiode design exhibited a higher responsivity (apparently due to the proximity of the depletion region) than the horizontal style photodiodes. The values of both, however, were good.

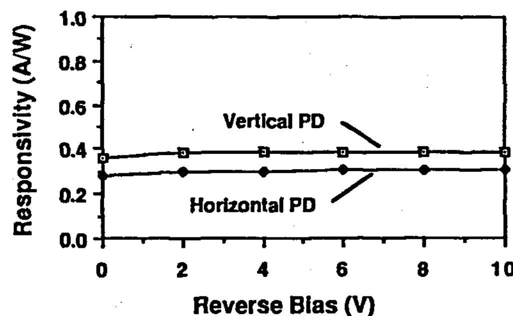


Figure 8. Responsivity curves for both styles of photodiode designs.

4. LED DESIGN

Since silicon is an indirect bandgap semiconductor, efficient emitters in silicon are difficult. We decided to fabricate the LEDs using MOCVD deposition of GaAs. Because of the large mismatch in lattice constant between Si and GaAs, a thin matching layer of single-crystal Ge in needed between the two materials. The design of the sources is shown in Figure 9. The polymer waveguide lies over the top and down the edge of the LED, so both surface and edge emission from the junction may be trapped and guided by the waveguide. The planarization properties of the polymer are advantageous to fill any voids for optimal coupling from source to guide.

Pads for the LEDs were wet etched in the SiO_2 layer, and a 250 nm matching layer of Ge was deposited by e-beam evaporation. GaAs was deposited over the Ge by MOCVD: first a 1.8 µm layer

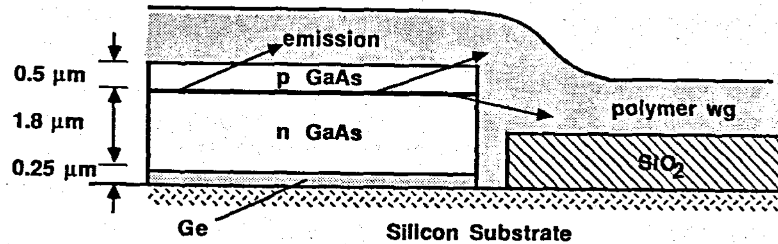


Figure 9. Side view of LED design, showing coupling of emission to waveguide.

of n GaAs (Se dopant, $10^{18}/cm^3$), then a 0.5 µm layer of p GaAs (Zn dopant, $10^{19}/cm^3$). After cleaning the polycrystalline Ge and GaAs from the field outside the LED itself, contacts were evaporated: AuGeNi/Ag/Au for the n contact, and Ag/Mn/Ag for the p contact.

Photoluminescence studies of the completed LEDs showed peak emission at 868 nm. A curve of optical output power as a function of diode current is given in Figure 10 for a typical LED device. As can be seen, threshold current is rather large for these samples, indicating poor efficiency, probably due to lattice defects from the Ge matching layer reaching into the junction area.

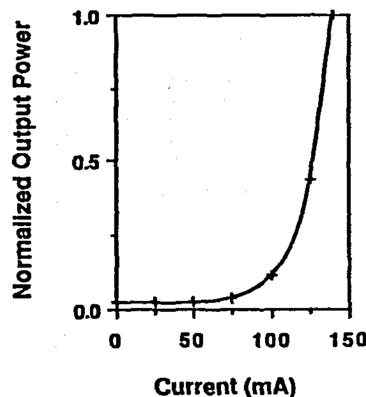


Figure 10. Optical power versus current for a GaAs LED sample grown on silicon.

5. CONCLUSIONS AND FUTURE WORK

All three components were fabricated and tested individually. The waveguides and photodiodes appeared to be near design specifications. The LEDs, however, did not emit efficiently, probably due to the complex fabrication steps required for depositing good single crystal GaAs on a silicon substrate. When improvements are accomplished in the LED fabrication, all three components needed for the intrachip optical interconnect can be tested together as a complete system.

6. ACKNOWLEDGEMENTS

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