Power, Clock, and Data Recovery in a Wireless Neural Recording Device

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***Abstract*—For many medical applications, neural recording systems should be fully implantable. Transcutaneous wires must be completely eliminated, and this necessitates the wireless transfer of power, clock, and configuration data to the device. We have developed, fabricated, and tested circuits that recover power from a wireless power transmitter and produce a clock from its carrier. A novel data recovery scheme is also presented that allows configuration and command data to be recovered from the amplitude-modulated power waveform. This scheme is robust against glitches and offsets, and requires a minimum modulation depth of 29%. All of these circuits together consume 0.366 mm^2 of area in a 0.5-µm CMOS process and have a total current draw of 511 µA.**

I. Introduction

Studying neural activity in the brain is a fast-growing area of research. The understanding developed through these studies has the potential to benefit many victims of spinal cord injury and other neurological disorders. Clinical trials have recently begun that enable severely motor-impaired individuals to manipulate a computer interface or prosthesis via a direct link from the brain [1]. As these technologies mature, many applications that are not currently practical will become feasible. These will significantly benefit both medicine and science.

Neural data is frequently obtained using microelectrode arrays, such as the Utah Electrode Array (UEA) [2], [3]. However, current systems using these microelectrode arrays require a direct wired connection through the skin to equipment outside the body. These transcutaneous cables can introduce noise into the neural signals and also increase the risk of mechanical failure and infection [4], [5]. An alternative is to include electronics with the implant that can amplify the signals, digitize them, and transmit the information outside the body via RF telemetry. This method, however, requires that the microelectronics included with the implant also be powered without the use of wires passing through the skin. In addition, it is important to be able to communicate clock and configuration information to the implant along with this power signal.

We have developed circuits that can wirelessly recover power, clock, and configuration data for a fully-implantable neural recording system. These circuits are part of a proposed neural interface that will include an integrated circuit (IC) that can amplify neural signals and transmit them outside the body. This IC is flip-chip bonded onto the back of the Utah Electrode Array. A specially fabricated gold on polyimide pickup coil [6] and a few surface mount devices (SMDs) are also included in the package.

The coil will receive the AC power signal, and electronics on the IC will rectify and regulate it to a stable 3.3 VDC supply to be used across the rest of the chip. Configuration data will be amplitude modulated on top of the power waveform, and clock information will be taken from the carrier frequency of the same signal. Power, clock, and data recovered by these circuits are all crucial to the operation of the neural amplifiers, analog-to-digital converter (ADC), and transmitter included on the IC.

Amplitude modulation is a common method used for sending configuration data into implantable devices at fairly slow data rates [7], [8]. Care must be taken to select an encoding scheme that is compatible with the demodulation circuitry. Higher data rates have recently been achieved using FSK (Frequency Shift Keying) modulation [9], but the slower rate is adequate for our application.

The remainder of this paper is organized as follows. Section II describes the circuits that will rectify the power signal and regulate it to a stable dc supply voltage, as well as the method of clock recovery. Section III introduces a novel data recovery scheme that is compatible with low-power, robust data recovery circuitry, and describes this circuitry in detail. Testing and results are discussed in Section IV, and conclusions are drawn in Section V.

II. Power and Clock Recovery

A. Power recovery

Power in the proposed system will be transmitted over an inductive link operating at a frequency of 2.64 MHz. A 5-mm diameter receiving coil on the implant will be used for

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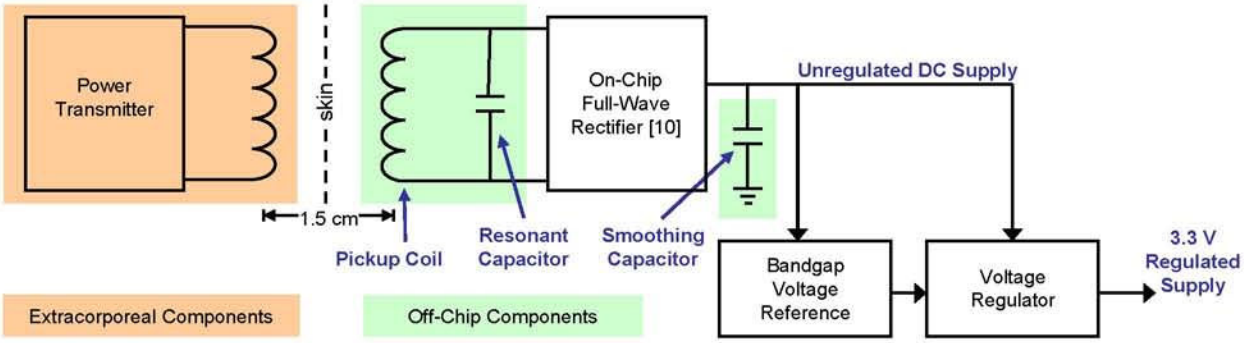

Figure 1. Components required for power recovery.

power reception, and one or two off-chip SMD capacitors are used to resonate with the coil. All the required blocks for power recovery are shown in Fig. 1. With the exception of the coil, resonating capacitors, and a fairly small smoothing capacitor, all of this circuitry is included on a single integrated circuit.

The integrated rectifier was adapted from [10] and uses floating wells and parasitic diodes to approximate the behavior of a standard discrete-diode full-wave bridge rectifier. The output of the rectifier requires a prohibitively large capacitance for smoothing. This must be included with the implant as an SMD component, similar to the resonating capacitors.

The bandgap voltage reference, adapted from [11], and the pFET voltage regulator were developed previously in our lab [12]. The use of a pFET type voltage regulator allows for a very small dropout voltage. This is critical for low-power operation since all the currents on the chip are supplied through this circuit. The total power dissipation, then, is not $I_{total} \times V_{regulated}$, but $I_{total} \times V_{unregulated}$.

B. Clock Recovery

Clock recovery is accomplished using a Schmitt trigger that edge-triggers a D flip-flop with its inverting output tied to its input, as reported in [5]. The hysteresis of the Schmitt trigger provides a clean digital pulse, and the subsequent flip-flop reduces the frequency by half and guarantees a 50% duty cycle. This is necessary since the power waveform will have a constant frequency, but is not likely to have a duty cycle of precisely 50%. Dividing the clock down further can yield other clock frequencies, such as 330 kHz, which is convenient for the ADC and data recovery circuits.

III. Data Recovery

As discussed above, it is necessary to send configuration data to the implant. These data are used to select an electrode channel to be digitized by the ADC, to set a global threshold level for spike detection, and to power on or off individual amplifiers across the chip. In future implants, these data could be used to communicate chip identification information, send commands to the RF transmitter, or modify other settings as determined at design time. The data is amplitude modulated on top of the power waveform, and must be demodulated, synchronized, and stored in a way that allows easy access to the information.

A. Data Recovery Scheme

A suitable data recovery scheme must provide some way of synchronizing to the incoming data signal to avoid bit skew or glitches near transitions. Also, the previously designed demodulator circuits require that the average value of the data signal be approximately halfway between its high and low values. Therefore, it is necessary to use an encoding scheme that ensures both high and low values for each bit of data, such as Manchester encoding. In addition, there may be offset voltages in the demodulator circuit that affect the average envelope value, so it would be helpful to have a scheme that could be easily adjusted to raise or lower this average value.

The data scheme chosen takes all of these factors into account. It consists of a short pulse to represent a low value and a long pulse to represent a high value as shown in Fig. 2. In order to sample the data, it is necessary to detect a low-to-high transition on the incoming data signal, and then count a fixed amount of time Δt before sampling. The data pulse widths are defined so that a short pulse is shorter than Δt and a long pulse is longer than Δt. Therefore, sampling at time Δt will yield a '0' for a short pulse and a '1' for a long pulse.

This scheme synchronizes to each bit individually so there is no possibility for bit skew. It has high and low values for each bit, but is insensitive to the space between the bits, so this time can be adjusted to account for offsets that may be present in the demodulator circuitry. In addition, the scheme is tolerant of glitches on the falling edge of pulses

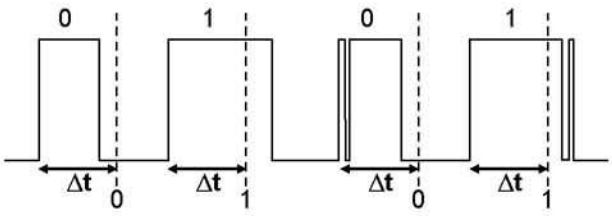

Figure 2. Proposed data scheme is robust against glitches and offsets.

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because it samples long before or long after the transition. It is also a simple matter to design the recovery circuitry to be robust against glitches on the leading edge on the pulses.

B. Data Recovery Circuits

The recovery circuitry required for the scheme described above consists of AM demodulation circuitry, a positive edge detecting circuit that triggers an input length counter, a circuit to check for a header for frame synchronization, a bit counter to shift in the correct number of bits, and a series of shift registers that can be placed across the chip for easy data access. Each of these components will be described in more detail in the following paragraphs.

1) AM Demodulator

The first step in the process of data recovery is to demodulate the signal from the power waveform. This was already developed in our lab [5] and consists of several pieces: (1) a pre-filter to attenuate the signal and avoid dangerously high voltages, (2) an envelope detector, (3) a low-pass filter to find the average value of the envelope, and (4) a comparator to compare the envelope to its average.

It should be noted that this circuit was designed to receive data at a rate of about 10 kbps. This is a very slow rate when compared with the operation of the rest of the chip. It is therefore suitable for configuration-type data only and not for real-time communication with the components on the chip. This is acceptable for our application. However, for future neural stimulation applications it will be necessary to redesign this circuitry for faster operation or design stimulation options that can be selected by configuration bits.

2) Edge Detection and Input Length Counter

Fig. 3 shows a high level view of the edge detection and Δt-counter. The counter and delay blocks are made up of flip-flops in standard configurations. While the edge detection circuit is waiting for a new bit, the value of the flip-flop in Fig. 3 is zero. This disables the counter, so that it cannot generate the Δt flag that causes data to be sampled. Qbar is high in this case, so a positive transition on the data will toggle the flip-flop and enable the counter. Qbar is then low, so the output of the AND gate will not change even if there is a glitch on the data signal.

Once the Δt-counter is enabled it will count a specified amount of time. We chose a Δt value of 48.5 µs. This corresponds to an approximate 10kbps data rate and is a convenient multiple of the local clock running at 330 kHz:

$$16 \times (1 / 330\text{kHz}) = 48.5\ \mu\text{s} \qquad (1)$$

With a counter using five flip-flops, the Δt signal will go high after 48.5 µs, signaling that a sample be taken and also feeding back to reset the edge detection flip-flop. This flip-flop in turn disables the counter and begins waiting for a new positive transition on the data signal. The delay buffer is necessary because of the feedback in the circuit and ensures a clean digital pulse on Δt.

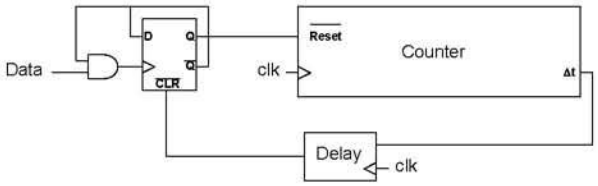

Figure 3. Circuits for edge detection and input length count.

3) Shift-Load Registers

The input length (Δt) pulse indicates when to sample the data signal. Rather than shifting all the data through each configuration register on the chip, we use two flip-flops for each configuration bit. These "shift-load" registers shift in data serially, but have another set of registers to act as working registers on the chip. These are all loaded in parallel once a frame of data has been completely shifted in.

4) Header Check and Bit Count

Fig. 4 shows the circuits for header check and frame bit count. We use a string of shift registers with their outputs tied to a four-input NAND gate as a header check. This corresponds to a header of four subsequent '1's. After identifying the header, the clock to the header-check shift registers is gated, making it blind to incoming data. At the same time, a counter is enabled which counts high enough to allow an entire frame of data to be received. The bit counter implemented is similar to that used to generate the Δt signal, but it contains eight flip-flops, counting to 128. This is currently more bits than shift-load registers on the chip (~95), but accepting extra bits eliminates the need for combinational logic on the output of the counter, and it is easy to provide spacer bits to make the count correct.

The output of the bit counter generates an update signal, indicating to the shift-load registers across the chip that the frame is complete and to load the working registers. This signal is also used to reset the header check, which in turn disables the bit counter. Everything rests in the initial state until another header is received. Again, delay buffers are used for feedback signals to eliminate unpredictable or glitchy behavior.

IV. Testing and Results

The circuits for power, clock, and data recovery were fabricated in 0.5-µm 3-metal, 2-poly CMOS process and

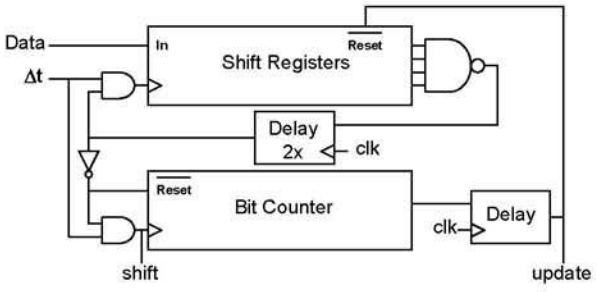

Figure 4. Header check and frame bit counter.

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together consumed an area of 915 µm x 400 µm. The results presented here were all obtained with the chip powered wirelessly over a 2.64 MHz inductive link. The distance between coils in this link was approximately 1.5 cm.

A. *Power Reception and Clock Recovery*

In order to obtain a 3.3 VDC output, the minimum required input coil voltage was 5.7 V_{peak}. The regulator dropout voltage with a load of 3 mA (typical for powering the entire implant) was 0.25 V. Load regulation from 2 to 10 mA was 0.15 % and line regulation from 3.5 to 8.0 V was better than 0.30 %/V. Ripple on the regulated supply was 250 mV_{pp}.

Current draw of the rectifier, bandgap, and regulator circuits was 440 µA. Note that the exact power consumption of all circuits on the chip may vary depending on the unregulated supply voltage, which may be significantly higher than the minimum required. Therefore, we will report power consumption for all circuits in terms of current draw.

The clock recovery circuit produced a clean digital signal with a frequency of 1.32 MHz and a 50% duty cycle as expected. Clock recovery current draw was 28 µA.

B. *Data Recovery*

Fig. 5 shows measured results from the operation of the data recovery circuitry. It shows the received power waveform on the internal coil, the recovered envelope of the waveform, the digital output of the demodulation circuitry, and the sample signal that indicates when to shift the data signal into shift registers.

Note that there is an erroneous sample pulse after the falling edge of the last data pulse. This is due to an oversight in the implementation of the proposed data scheme. After sampling the correct value of a pulse, the edge detection circuitry is re-enabled such that a glitch on the trailing edge of a long pulse may inadvertently trigger another input length count and sample. It is a simple matter to remedy this problem with a small amount of additional digital circuitry, which has already been developed for future revisions.

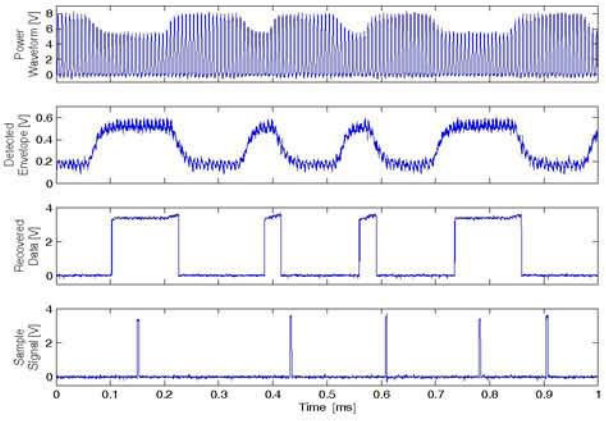

Figure 5. Measured waveforms of data being demodulated and sampled.

The maximum input bit rate was limited to 6.5 kbps by the external power transmitter (a class E amplifier). The minimum required modulation depth was 29%, resulting in a typical "low" receive coil voltage of 5.7 V_{peak} and a typical "high" receive coil voltage of 8.0 V_{peak}. Current draw for the data recovery circuitry was 43 µA.

V. Conclusions

We have presented circuits for power, clock, and data recovery to be used in a fully-implantable neural recording system. All of these circuits together draw 511 µA of current, corresponding to 1.81 mW with a minimum receive coil voltage. The rectifier used does not require bulky off-chip diodes and the clock recovery circuit produces a clock signal with a 50 % duty cycle regardless of the duty cycle of the received power waveform. A novel data recovery scheme has been proposed which is robust against offsets and glitches. Each of these circuits provides functionality that is critical to the realization of a fully-implantable biomedical implant.

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