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Self-aligned passivated copper interconnects: A novel technique for making interconnections in Ultra Large Scale Integration device applications

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Abstract

We have developed a technique to grow self-aligned epitaxial Cu/MgO films on Si (100) using a Pulsed Laser Deposition Method. In this method we deposit a uniform film of Cu/Mg (5-7%) alloy over Si (100) at room temperature using TiN as an intermediate buffer layer. As a result of HRTEM (with spatial resolution of 0.18 nm) and STEM-Z investigations we observed that when this film is annealed at 500°C (in a controlled oxygen environment), in less than 30 minutes time, all the Mg segregates at the top and at the bottom surface of Cu. This is understood to be the consequence of lower surface energy of Mg. At 500°C Mg is quite sensitive to oxygen and a thin layer of MgO is immediately formed at the top surface, we also observed a thin layer of MgO at the Cu/TiN interface. Thickness of the upper MgO layer was found to be 15 nm while that of lower layer was 10 nm. MgO underneath layer acts as a diffusion barrier and inhibits the diffusion of Cu in the system. Upper MgO layer acts as a passivating layer and improves the quality of copper against oxidation. Electrical resistivity measurements (in the temperature range 12-300 K) showed MgO/Cu/MgO/TiN/Si (100) sample to be highly conducting. We also observed that the resistivity of the system is insensitive to ambient oxygen environment. Self-aligned MgO (100) layer also provides a means to grow several interesting materials over it. This technique can be used to integrate high temperature superconductors like $YBa_2Cu_3O_7$ with silicon chip.

Introduction

The demand for improved performance in integrated circuits has led to the integration of an increasing number of semiconductor devices on chips of decreasing size. This has been achieved largely by scaling down the device feature size, while increasing the number of interconnect layers. As a result, the topography has become much more complicated with each successive device generation. In addition as metal line widths enter into the sub-half-micron regime, device speed is expected to be limited by the interconnect performance[1,2,3]. The current metallization material Al suffers from poor step coverage, poor electromigration and stress migration and stress resistance, and relatively high resistivity. As a result current interconnect schemes, which are based on Al alloy metallization, have become performance limiting.

The continuing drive for higher performance integrated circuit devices necessitates newer and improved materials for interconnections. Copper is receiving considerable attention [4,5,6] as a potential interconnection material in advanced metallization technology due to its outstanding electromigration resistance (exhibited resistance to electromigration above current densities of 10^9 A/cm^2) and lower resistivity (1.6 μΩ cm) [1,7] as compared to Aluminum. As a result, copper based interconnects posses the ability to operate at higher frequencies and not limited by current densities. However the use of copper as an interconnect has some limitations.

Copper is known as a fast diffuser [1,8] and can act to "poison" an active device, for example, the source/drain/gate region of a transistor. To alleviate the undesirable effects of copper diffusion, development of advanced diffusion barriers is required. Another drawback with copper is that it is more prone to oxidation than aluminum and hence requires the growth of a passivating layer [9-16] to protect it from the ambient atmosphere. Because of these reasons copper was not considered seriously in the past as a replacement for Aluminum. However, because of the recent development of copper passivation methods and diffusion barrier materials now it has become feasible to use copper interconnects. In this letter we present a novel method to grow simultaneously a diffusion barrier and a passivating layer for copper interconnects. In this method thin layers of MgO are formed above and below the copper interconnects, in a self-aligned geometry, which act as passivating and diffusion barrier layers, respectively.

Experimental Details

Now we describe our method and present the results about the growth of copper interconnects on Si (001) using a thin buffer layer of TiN. First step in this method is to deposit a thin layer of Cu-Mg alloy (% of Mg~5%) on Si (001) using a thin buffer layer of TiN. This was done in a pulsed laser deposition [17-19] chamber using a KrF excimer laser (λ=248 nm) in vacuum of 1×10^{-8} Torr. The stoichiometric hot pressed TiN and Cu-Mg alloy, mounted on a rotating polygon, were ablated using the focused laser beam. The energy density of the beam was ~2-3 Jcm^{-2} at 45° angle of incidence. The target was held parallel to (100) silicon substrate and 4.5 cm away from it. Silicon substrate was cleaned ultrasonically for five minutes in acetone and then for two minutes in methanol, followed by a dip in 20% HF for two minutes to remove the native oxide. TiN film was deposited at 650°C while Cu-Mg alloy film was deposited at room temperature. Now in the second step of this method Cu-Mg/TiN/Si (100) multilayer system was annealed for 30 minutes at 500°C in a partial oxygen pressure of 10 m-Torr. The multi-layered structure, thus obtained, was analyzed by X-Ray Diffraction (XRD) high-resolution transmission electron microscopy. Electrical resistivity measurements were performed in a closed cycle refrigerator in the temperature range of 12-300 K using a conventional four-probe technique.

Discussion

Fig 1 shows the XRD pattern of the final multi-layered structure. It is evident from this pattern that all the layers show preferential orientation (100) parallel to the substrate, suggesting the epitaxial growth of the multi-layered structure. In the 2θ range from 30-100° we observed peaks corresponding to (200) and (400) planes of TiN, and the (200) planes of copper and MgO. Fig 2 shows a cross-section TEM image of the annealed sample along the [011] zone axis of the Si substrate. Four distinct layers can clearly be seen. As result of EELS measurements these layers were identified as TiN, MgO, Cu and MgO. High-resolution transmission electron micrograph of the final structure is shown in Fig.3. Self aligned epitaxial nature of all the films is clearly delineated.

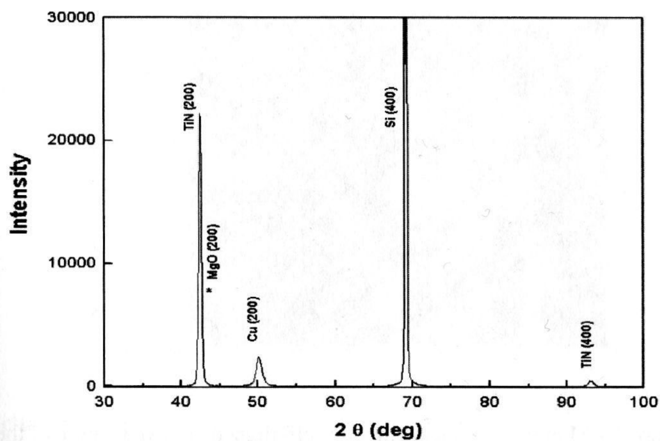

Figure 1. X-Ray diffraction from the annealed Cu-Mg/TiN/Si sample.

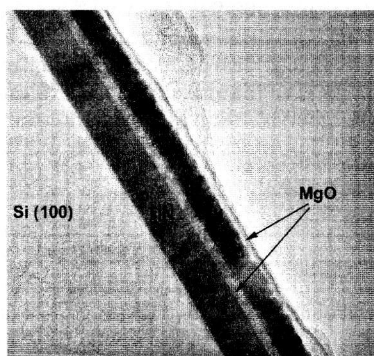

Figure2. The cross-section TEM image of the annealed sample along the (011) zone axis other Si substrate.

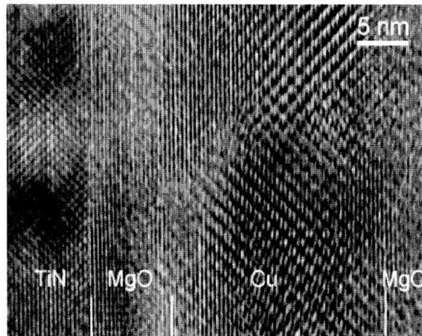

Figure 3. High Resolution TEM micrograph showing the self-aligned epitaxial nature of the TiN/MgO/Cu/MgO.

We studied the diffusion barrier characteristics of this structure by annealing it at several temperatures in the temperature range 500-900 °C. We did not observe any trace of copper in silicon till 800 °C. Above 800 °C our EELS measurements showed a slight diffusion of copper into the substrate. For a comparison we also performed similar annealing experiments on Cu/TiN/Si structures, in this case even the annealing at 600 °C caused significant copper diffusion into the silicon. In our method a thin MgO layer formed at the bottom of copper acts as an additional diffusion barrier and provides much improved resistance to copper diffusion into the substrate.

The MgO on the top of copper passivates it against the oxidation from ambient atmosphere. Furthermore, for improved performance in next generation cryoelectronics applications it is desirable to have interconnect materials with high conductivity and small variation with temperature. Pure copper interconnects have high conductivity but they also have very high value of temperature coefficient of resistivity. As a result when temperature goes down the interconnect resistance also decreases which affects the time constants of various devices and hence hampers the proper functionality of the devices. Our method offers a solution to this problem also. Self-aligned passivated copper interconnects have higher conductivity and much smaller variation with change in temperature. In table-I we have compared the values of electrical resistivities and temperature coefficient of resistivity of copper, aluminum and MgO/Cu/MgO layers. It can be seen that our passivated copper layers have higher conductivity compared to aluminum and at the same time smaller temperature coefficient of resistivity (TCR) compared to copper and aluminum. This is because of the fact that while Cu is metallic, both the top and the bottom layers of MgO are insulating, thereby resulting in the overall smaller TCR for this composite structure.

Table I. Room temperature electrical resistivity (ρ) and temperature coefficient of resistivity $\frac{1}{\rho}\frac{d\rho}{dT}$ of Cu, Al and passivated Cu interconnects.

	$\rho\ (\mu\Omega - cm)$	$\frac{1}{\rho}\left(\frac{\partial\rho}{\partial T}\right)$ **(K^{-1})**
Cu	1.6	3.80×10^{-3}
Al	2.8	3.40×10^{-3}
Passivated Cu	2.45	2.94×10^{-4}

Conclusion

In conclusion we have developed a novel method to make a self-aligned passivated copper interconnects for ULSI applications using Cu-Mg deposition followed by oxidation. These interconnects are found to have high conductivity and small temperature coefficient of resistivity. A thin MgO layer at the bottom of copper avoids its diffusion into the substrate while a thin MgO layer at the top of copper interconnects passivates it against the oxidation.

Acknowledgment

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References

1. A. Jain, T.T. Kodas, R. Jairath, M.J. Hampden, J.Vac.Sci. Technol. B **11**(6), 2107 (1993).
2. P.L.Pai and C.H. Ting, IEEE Trans. Electron Device Lett. **EDL-10**, 423 (1989).
3. P.L.Pai and C.H. Ting, *VLSI Multilevel Interconnection Conference, 1989. Proceedings Sixth International IEEE*, 258 (1989).
4. S. P. Murarka and S. Hymes, Crit. Rev. Solid State Mater. Sci. **20**, 87 (1995).
5. C. Whitman, M. M. Moslehi, A. Paranjpe, L. Velo, and T. Omstead, J. Vac. Sci. Technol. A **17**, 1893 (1999).
6. R. Liu, C. S. Pai, and E. Martinez, Solid-State Electron. **43**, 1003 (1999)
7. Hitoshi Itow, Yasushi Nakasaki, Gaku Minamihaba, Kyoichi Suguro, and Haruo Okano, Appl. Phys. Lett. **63** (7), 934 (1993).
8. J.D. Brayer, R.M. Swanson, and T.W. Sigmon, J. Electrochem. Soc. **130**, 1777(1983).

9. S. Hymes, S.P. Mukara, C. Shepard, W.A. Lanford, J. Appl. Phys. **71**(9), 4623 (1992).
10. P. J. Ding, W. Wang, W. A. Lanford, S. Hymes and S. P. Murarka, Appl. Phys. Lett. **65** (14), 1778 (1994)
11. Woo-Cheol Roh and Donggeun Jung, Jpn. J. Appl. Phys. **37**, L406 (1998).
12. H. Itow, Y. Nakasaki, G. Minamihaba, K. Suguro, and H. Okano, Appl. Phys. Lett. **63**, 934 (1993).
13. W. A. Lanford, P. J. Ding, W. Wang, S. Hymes, and S. P. Murarka, Thin Solid Films **262**, 234 (1995).
14. P. J. Ding, W. A. Lanford, S. Hymes, and S. P. Murarka, J. Appl. Phys. **74**, 1331(1993).
15. J. Li, J. W. Mayer, and E. G. Colgan, J. Appl. Phys. **70**, 2820 (1991).
16. N. Awaya and Y. Arita, J. Electron. Mater. **21**, 959 (1992).
17. R.D. Visputc, R. Chowdhury, P. Tiwari, and J. Narayan, Appl. Phys. Lett. **65**(20), 2565(1994).
18. Rajiv K. Singh and J. Narayan, Phys. Review B, **41**(13), 8843(1990).
19. J.Narayan, P. Tiwari, X. Chen, J. Singh, R. Chowdhary, and T. Zheleva, Appl. Phys.Lett., **61**(11), 1290(1992).