Rethinking DRAM Design And Organization For Energy-Constrained Multicores

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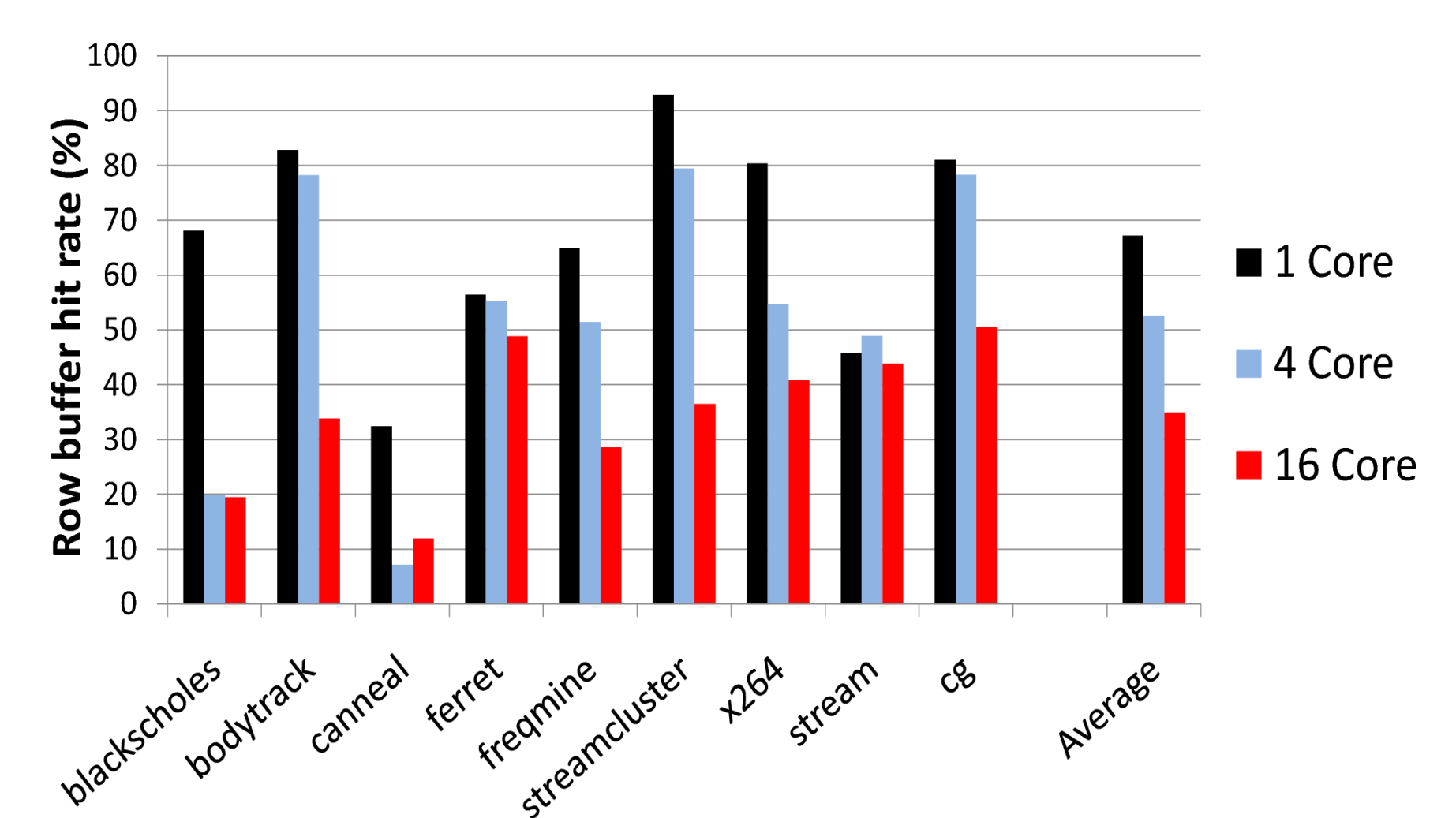
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DRAM Power Consumption

Modern data-centers consume anywhere between a few kWs to tens of MWs of power. The total cost of the electricity required to power and cool datacenters like the ones below was $4.5 billion in 2007.

DRAM accounts for about **40%** of the total power consumption

What happens next ?

As the number of cores increase, the row reuse gets worse.
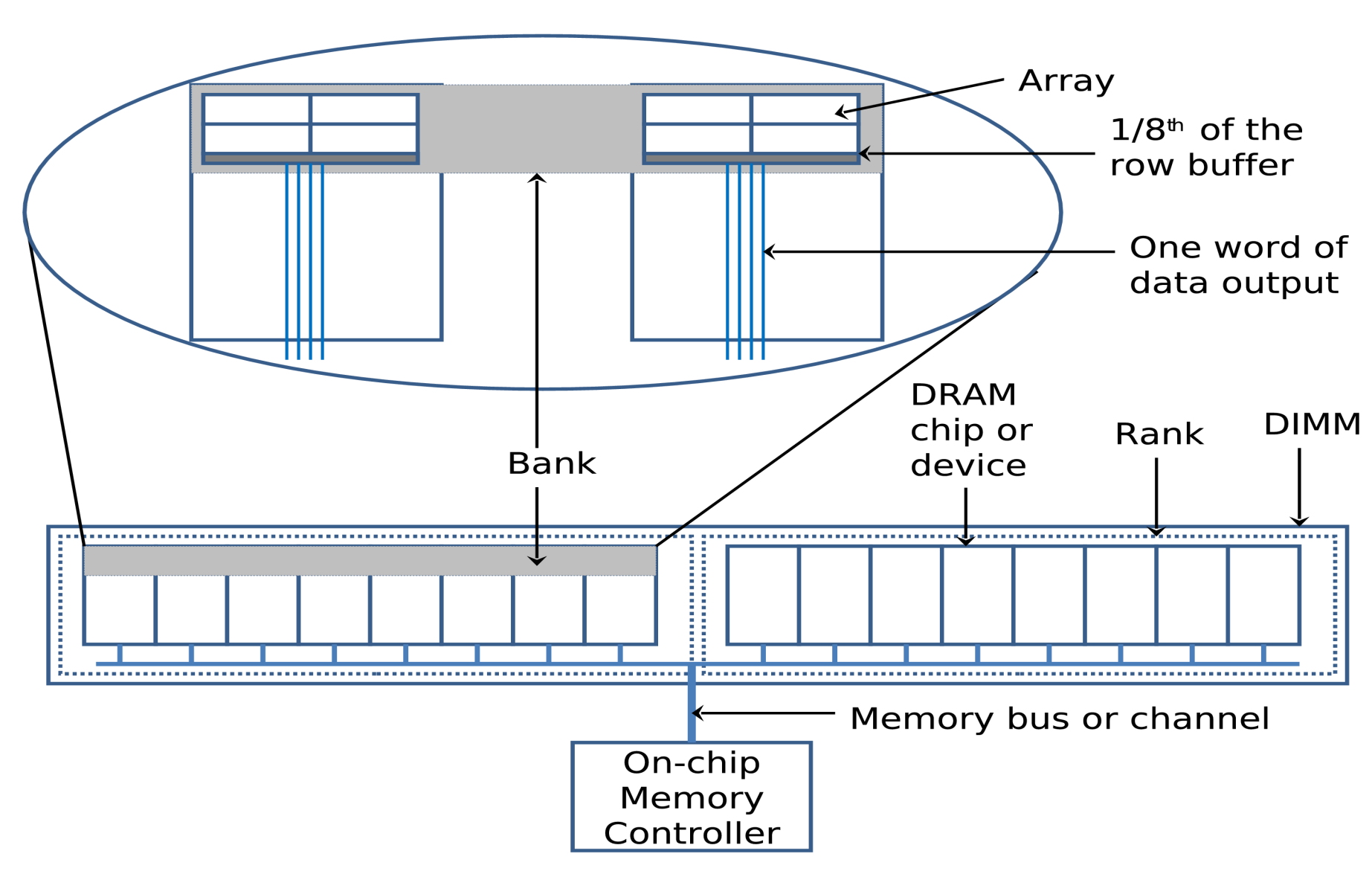
Investing in the future

Commodity
Cheap
Power-Hungry

Initial cost will be recovered through the significantly reduced operating costs over its lifetime
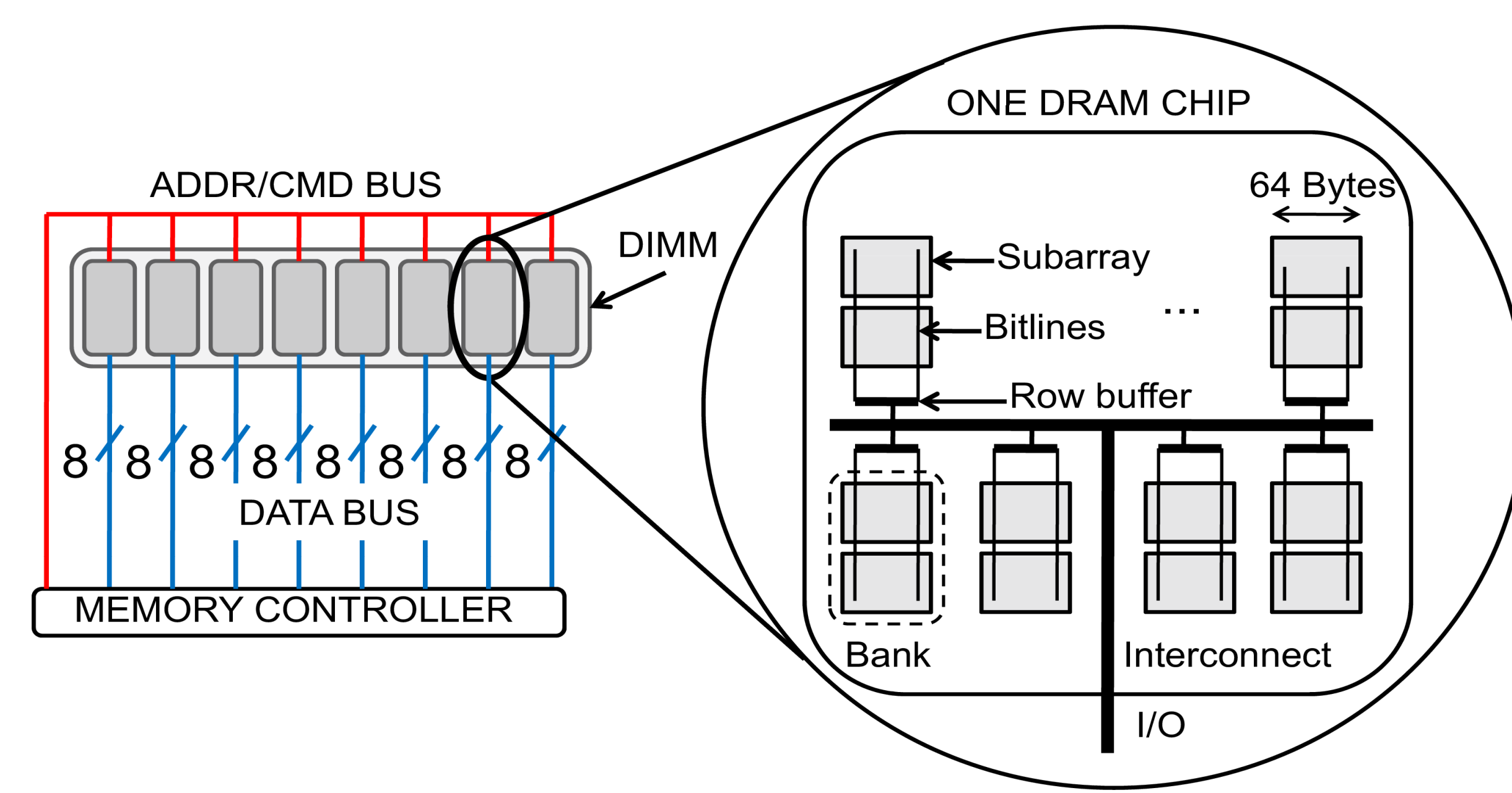
Baseline Organization & Overfetch

To access a cache-line worth of data (64 bytes), it is often necessary to read out as much as 16K Bytes from the DRAM arrays into the row-buffer.

Unless there is locality in the access stream, the row-buffer's data can't be reused and must be restored back in the arrays.

Single Sub-Array Access (SSA)

DRAM microarchitecture and data layout is changed so that a cache-line is read out of a single DRAM array .

Dynamic energy reduced due to lesser no. of arrays being activated & at the same time, inactive arrays can be put to sleep.
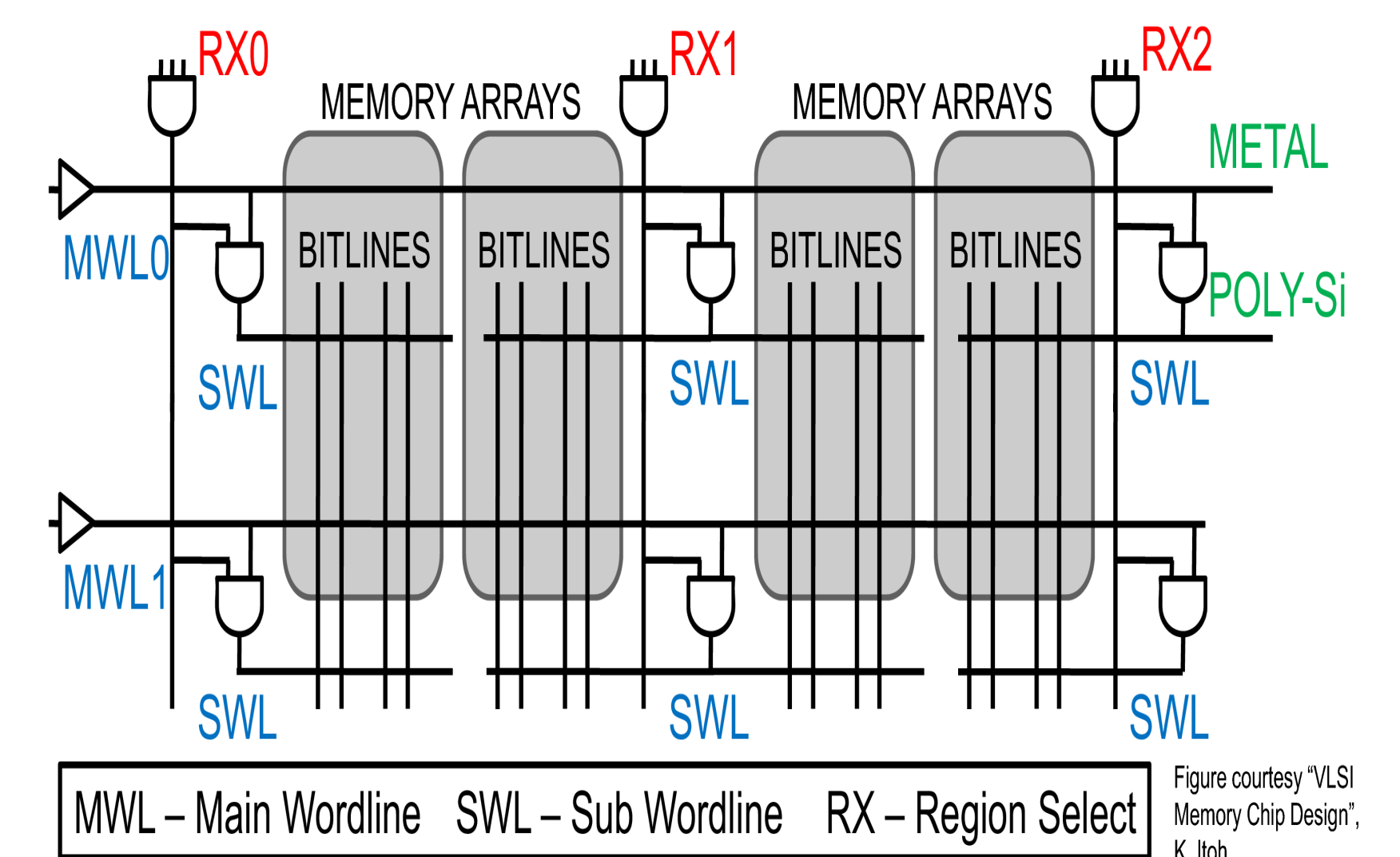
Each access now has to be serialized over several cycles – but there is more scope for concurrency in workloads with bank-level parallelism.

Motivation
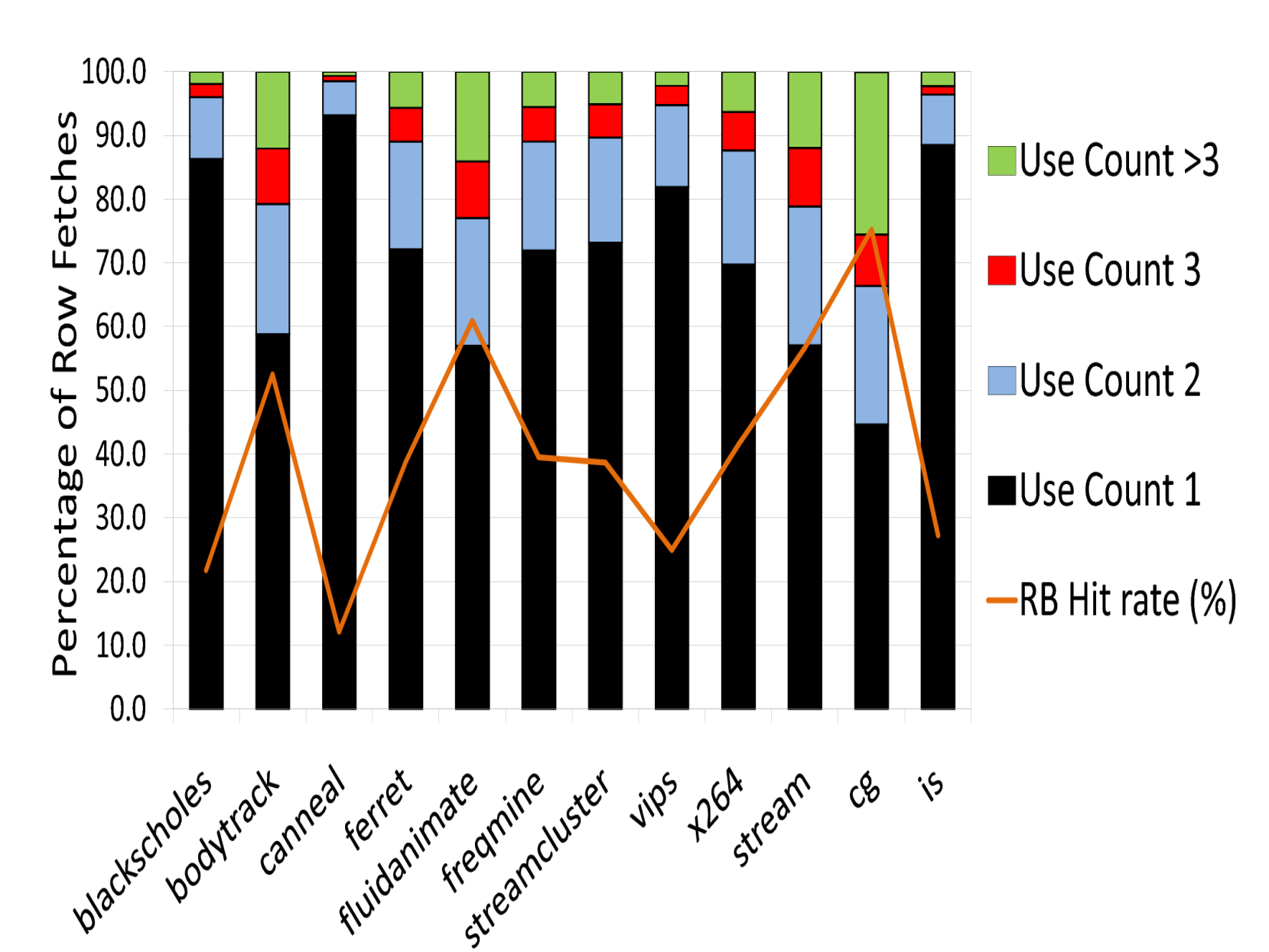
Data in a row buffer gets used only a few times before the row has to be closed due to a conflict.

Select Bitline Activate

MWL – Main Wordline   SWL – Sub Wordline   RX – Region Select

Figure courtesy "VLSI Memory Chip Design", K. Itoh

To reduce overfetch, we change the access mechanism so that only the bitlines corresponding to the requested cache-line get activated.
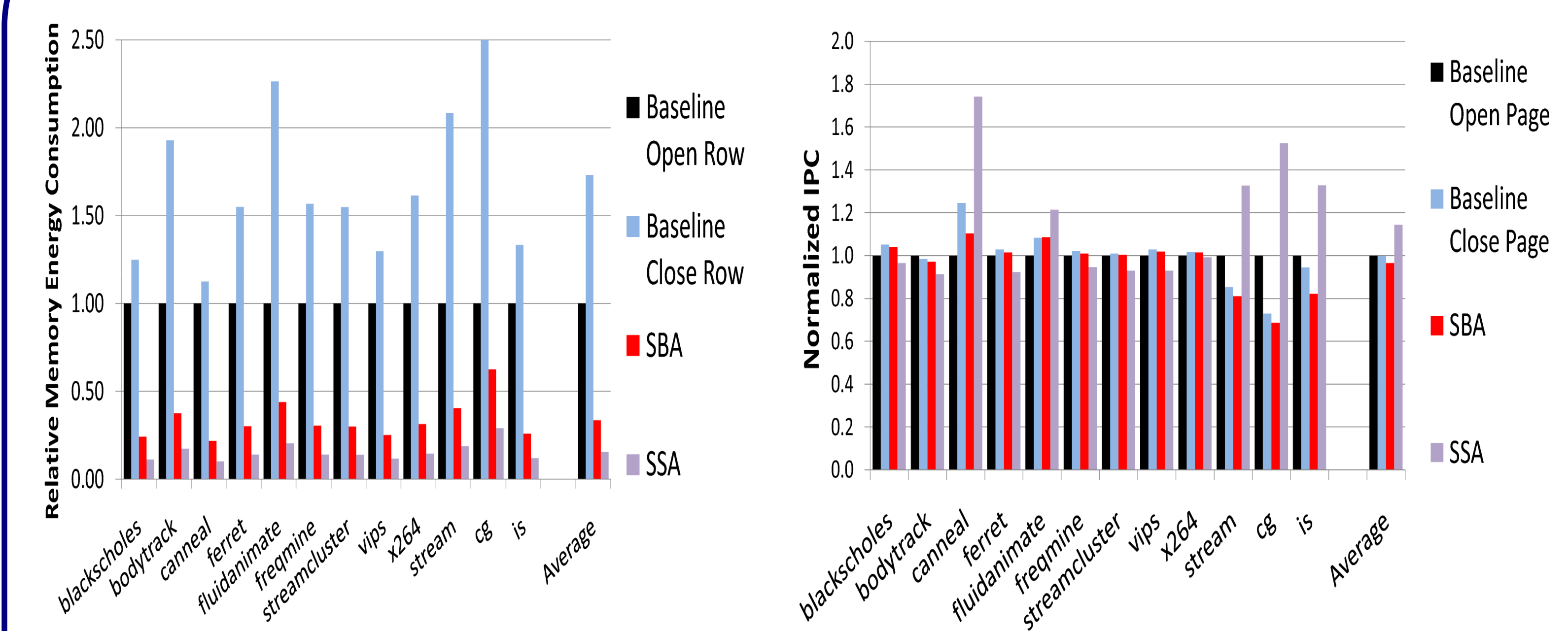
Chipkill

SCCDCD level reliability through a RAID like organization.
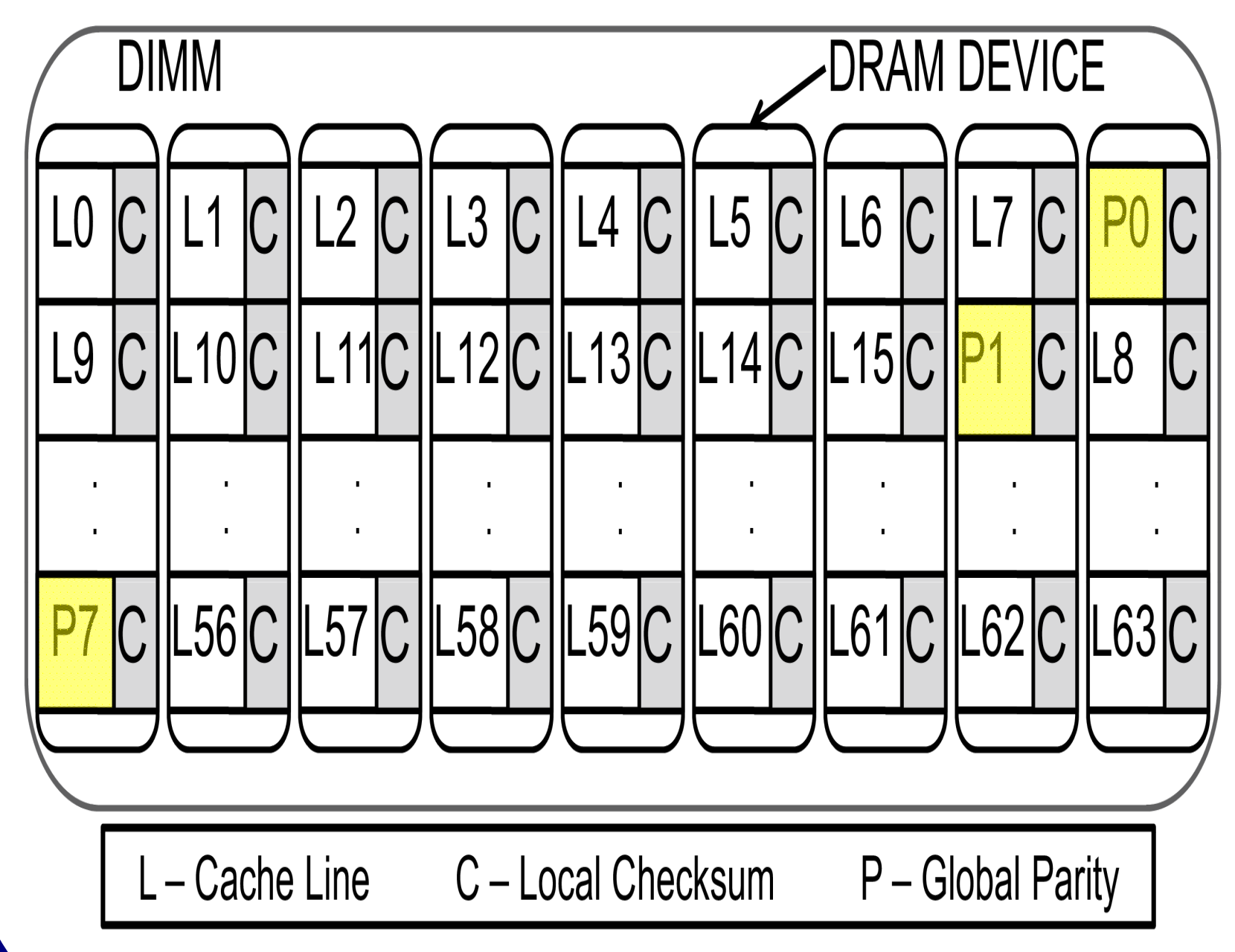
L – Cache Line   C – Local Checksum   P – Global Parity

Results

SSA : energy savings = 6.4X baseline   perf. degradation = 5.5%

SBA : energy savings = 3X baseline   perf. degradation = 3%