

# Microfluidic Device For Triggered Chip Transience

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**Abstract**— This paper presents the fabrication and testing of a microfluidic device for the triggered destruction (transience) of microchips. The device consists of a thin film array of sealed reservoirs patterned on a polymer film. Each reservoir encloses a corrosive chemical agent which upon release dissolves the surface of a microchip placed beneath. When transience is activated, an integrated micro-heater melts the bottom of the reservoirs thus releasing the chemical agent, which in a matter of minutes destroys key layers on the underlying electronic/sensor chip. Each reservoir consists of a 16  $\mu\text{m}$ -tall cavity holding 1  $\mu\text{L}/\text{cm}^2$  of 1000:1 BHF. The measured energy required to burst open a filled reservoir was  $\sim 35\text{mJ}/\text{cm}^2$  when the device rests on top of a glass substrate and  $\sim 100\text{mJ}/\text{cm}^2$  when the device rests on top of a 0.5  $\mu\text{m}$ -layer of silicon dioxide on a 0.5 mm silicon wafer.

**Index Terms**—Microfluidic device, chip transience, polymer reservoirs, chip destruction.

## I. INTRODUCTION

In every case of theft or loss of an important electronic device or system there is a ubiquitous fear of significant information landing in the hands of unwanted subjects. The utilization of access passwords and encryption are currently widely used as a first line of defense, but with sufficient effort these software protections can be eventually cracked. In mission critical military and financial applications, a hardware protection can offer an unbreakable level of protection. Such systems would intrinsically have a built-in hardware transience mechanism that can be triggered to destroy the sensitive information.

In this paper we present an add-on microfluidic device that can be used to irreversibly destroy a target electronic microchip and any information that it may contain within as shown in the schematic of Figure 1 below. The concept of using a microfluidic device for destruction of microchips has been conceived in [1] but not realized. In this work we implemented a micro-fluidic device that will destroy a target chip placed right beneath it by releasing a highly corrosive chemical agent on the chip, which otherwise remains safely contained in a reservoir. When the device is activated the released agent dissolves the top layers the microchip beneath it; thus irreversibly and permanently disabling the chip below. In the

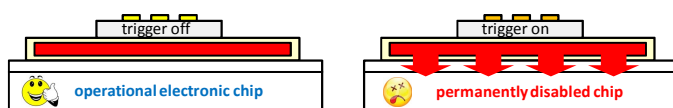


Figure 1. Schematic showing triggered chip transience action

following sections we discuss the transience device structure, the triggering mechanism, the fabrication device and experiments.

## II. DEVICE STRUCTURE

Figure 2 shows the schematic of the transience microfluidic device. It consists of a supporting polymeric film with a microfabricated heater, a reservoir enclosing a chemical agent and a sealing polymer wall. The device is very thin, and it can be attached or built at low processing temperatures on top of an existing electronic chip. In this paper we have selected dilute < 100:1 BHF as a demonstration transience chemical agent. BHF attacks both silicon oxide passivation layers and metal lines causing the failure of the chip below.

Microfluidic reservoirs can be fabricated in several ways

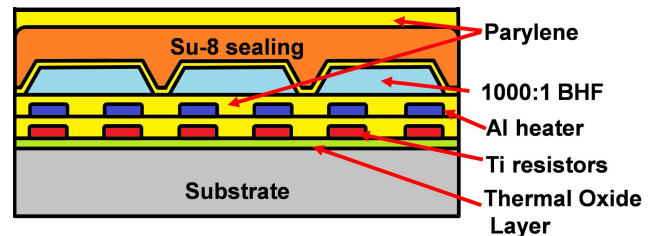


Figure 2. Schematic showing device along with the micro-heater attached to an integrated chip

[2-3], but our specific application presents three challenges that determine our materials and fabrication technology. First, the reservoir walls must be chemically inert to contain the chemical agent for extended periods of time. Second, a suitable method of filling the cavity with the agent and subsequent sealing must be selected, and third, the reservoir must burst open under electrical control to release the chemical agent triggering the chip transience.

*a) Materials Selection:* Parylene-C [4-6] is a common material used in microfluidic devices. Parylene can resist chemical attack by dilute BHF for long periods of time [7]; hence we utilize this material for the reservoir walls. The thickness of the reservoir wall is a critical device design parameter. Thick walls will contain the agent for long periods of time but may be difficult or impossible to burst open. On the other hand thin walls may burst easily but the agent may diffuse out [8]. In order to minimize the diffusion of the agent to the surrounding environment we use a thick wall at the top and a thin wall at the bottom of the reservoir. The thin wall will be in direct contact with the microchip surface. In these devices we use a parylene thickness of 5  $\mu\text{m}$  at the top and 1  $\mu\text{m}$  at the bottom of the reservoir. The top wall is made

thicker by subsequent deposition of additional polymer layers as shown in Fig. 2.

*b) Reservoir Sealing:* Several methods for sealing liquid-filled microcavities have been recently developed [9-15]. In particular since we want to store the chemical agent for long periods of time, a tight seal is desirable. The device presented here utilizes a two-step sealing procedure. We incorporate a primary seal at the lowest temperature possible to minimize agent evaporation. This is followed by a tighter secondary seal. After the chemical agent is introduced in an open chamber, we freeze the agent at low temperatures and subsequently clean the top surface. Next we form the primary seal by spin coating a 50  $\mu\text{m}$  thick layer of negative photoresist (SU-8) which hardens upon exposure to UV. The entire structure is next sealed again using a 5  $\mu\text{m}$  layer of parylene-C.

*c) Reservoir Bursting:* In order to release the chemical agent we must open holes on the lower wall of the reservoir. The electrical opening of microfabricated reservoirs was published by Santini et al [16]. In these devices a drug-laden reservoir was sealed using a thin Au wall. The wall was electrochemically dissolved to open the reservoir to release the drug. Since the presence of Au near electronic devices may adversely affect their operation we use instead a heated Al wire embedded inside the reservoir lower wall. If the wire temperature is sufficiently high the parylene will locally melt thus bursting the reservoir and releasing the chemical agent.

The heating of the wire is performed by quickly discharging a capacitor storing a finite amount of electrical energy. The total amount of energy necessary to burst the parylene wall  $U_B$  is

$$U_B \approx U_M + U_L \quad (1)$$

where  $U_M$  is the energy required to melt the parylene wall and  $U_L$  is the energy loss due to heat losses elsewhere. The melting energy is

$$U_M \approx V_P \rho_P (C_P \cdot (T_m - T_o) + L_M) + V_H \rho_H \cdot C_H \cdot (T_m - T_o) \quad (2)$$

where  $V_P$  and  $V_H$  are the parylene wall and heater volumes,  $C_P$  and  $C_H$  and  $\rho_P$  and  $\rho_H$  their respective heat capacities and densities,  $L_M$  is the latent heat of melting for parylene,  $T_m$  is the parylene melting temperature ( $\sim 290^\circ\text{C}$ ) and  $T_o$  is the ambient temperature. Note that in Eq. (2) we have neglected the heating of the stored agent because the wall melting action happens very quickly.

The energy loss term  $U_L$  is dominated by heat conduction to the substrate below. If we assume the power profile consists of a rectangular thermal pulse of width  $\tau$  then

$$U_L \approx \frac{1}{\Theta_T} \cdot \int_0^\tau (T_w - T_o) dt \approx \frac{(T_m - T_o) \cdot \tau}{\Theta_T} \quad (3)$$

where  $\Theta_T$  is the thermal resistance of the wall and substrate. If the energy pulse is applied by discharging a capacitor on the heater resistor, the time duration of the pulse is  $\tau \sim R_h C_d$ . From Eqs. (1-2), the burst energy  $U_B$  must be equal to the capacitor

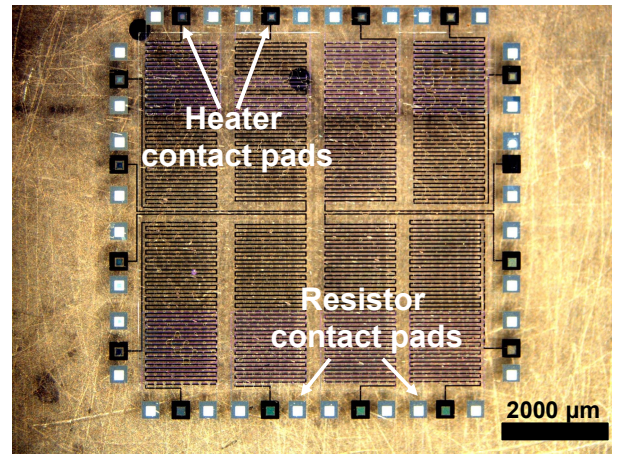


Figure 3. Optical image of transience test device.

stored energy =  $1/2 \cdot C_d \cdot V_B^2$ , the capacitor voltage required for bursting the wall can be easily calculated as

$$V_B \approx \sqrt{2 \cdot \left[ \frac{U_M}{C_d} + \frac{(T_m - T_o) \cdot R_h}{\Theta_T} \right]} \quad (4)$$

Note that the burst energy decreases as the thermal resistance of the substrate increases. The thermal resistance is essentially dominated by the thickness of underlying silicon dioxide chip insulation and substrate layers.

*d) Test Structures:* Transience tests were performed using the following test structures. The micro-fluidic test device consists of a series of hollow reservoir chambers consisting of polymer walls supported by pillar structures which rest on an array of Al micro-heaters. Instead of using a circuit microchip under the Al heaters we fabricated a substrate with an array of Ti resistors. The chip transience action will be demonstrated on these Ti resistors. The hollow polymeric chambers are filled up with a corrosive chemical agent, in this case 1000:1 BHF which chemically attacks Ti. When triggered, the heaters melt the bottom of the reservoir to release the BHF below thus etching the Ti resistors.

Fig. 3 shows an optical photograph of a completed test device with 1  $\text{cm}^2$  chambers holding 1  $\mu\text{L}/\text{cm}^2$  of 1000:1 BHF, and serpentine Al heater and Ti test resistors below. In the following sections we discuss the fabrication and testing of this test device.

### III. TEST DEVICE FABRICATION

Figure 4 shows a simplified fabrication process for the demonstration triggered transience device. The fabrication process starts by sputtering a layer of 0.2  $\mu\text{m}$ -thick Ti on a substrate (glass or oxidized silicon wafers) and patterning the layer to form titanium test resistors by lift-off. For this process we used 16 $\mu\text{m}$  thick positive photoresist AZ9260. The measured sheet resistance of the Ti was 15  $\Omega/\square$ . Next a 0.5  $\mu\text{m}$ -thick layer of parylene-C is deposited [Specialty Coating Systems, In, USA] on top of the Ti resistors. This is followed by the deposition of a 0.5  $\mu\text{m}$ -thick Al by e-beam evaporation.

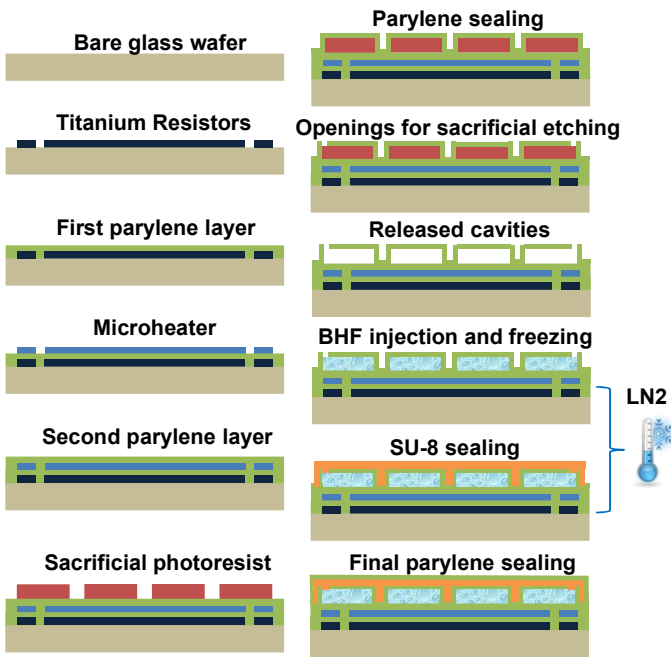


Figure 4. Simplified device fabrication process flow

The Al layer is patterned photolithographically using wet etching to define the heater layer. Next a second  $0.5\ \mu\text{m}$ -thick layer of parylene-C is deposited to encapsulate the heaters. The two parylene layers form the bottom wall of the reservoir. Microfluidic chambers are next fabricated using photoresist as sacrificial layer. In this process, a  $16\ \mu\text{m}$ -thick layer of AZ9260 resist is patterned on top of the parylene. Next a third  $5\ \mu\text{m}$ -thick parylene-C layer is deposited on the resist. Access orifices are next etched on the top parylene using a  $16\ \mu\text{m}$  thick AZ9260 photoresist as a mask. Next we sacrificially removed the photoresist by dipping the samples in acetone for 12 hours, and the samples were rinsed and dried in  $\text{N}_2$ .

The hollow chambers are next immersed in baths with various concentrations of the chemical agent, in this case 1000:1 BHF thus filling the chambers. The samples and the trapped BHF in the chambers are next frozen by placing the wafers on a cold metal block that was previously immersed in liquid nitrogen. While the samples are cold, first the top icy layer is cleanly removed using a  $\text{N}_2$  gun. Immediately after the drying, a  $50\ \mu\text{m}$ -thick layer of SU-8 photoresist is spin cast to form a primary seal of the orifices thus encapsulating the frozen BHF. The SU-8 was left to de-gas at atmospheric conditions for 30 minutes and then exposed to UV light. Finally a fourth  $5\ \mu\text{m}$ -thick layer of parylene-C is deposited to form a secondary seal that reduces permeability of the BHF through the reservoir walls. Contact holes to the Ti and Al

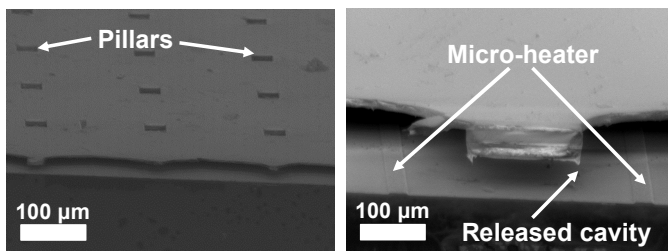


Figure 5. SEM pictures of the cross-section of the reservoir.

metal resistors were patterned using thick photoresist AZ9260 and then etched in  $\text{O}_2$  plasma. Figure 5 shows SEM pictures of the cross-section of the final device. Fig. 6(a) shows the presence of frozen BHF inside the reservoirs. Fig. 6(b) shows a photograph of frozen 1000:1 BHF at 200K sealed by the SU-8. Two types of devices were fabricated on (1) glass wafers and (2) oxidized silicon wafers with  $0.5\ \mu\text{m}$  of thermal silicon dioxide. After the samples were completely sealed the individual devices were diced and tested as discussed below.

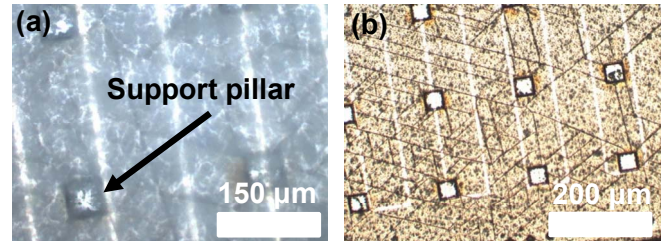


Figure 6. (a) BHF frozen inside the chamber, (b) Chamber with frozen BHF sealed by SU-8

#### IV. EXPERIMENTAL RESULTS

The transience characteristics of the micro-fluidic device were tested using two different electrical methods. In these experiments the resistance of the Ti test resistor was monitored as a function of time by connecting a  $100\ \text{k}\Omega$  resistor in series and driven by a  $15\ \text{V}$  DC power supply. The nominal Ti test resistance was  $60\ \text{k}\Omega$ . The voltage across the Ti resistor was next monitored using a Digital Storage Oscilloscope (Tektronix TDS 2024C). The resistance of the Ti test resistor was calculated from the recorder resistor divider voltage waveform.

*a) Static Burst Test:* We first determined the static power required to burst open the bottom wall by applying a DC voltage directly to the Al heater. The electrical resistance of the Al heater was approximately  $100\ \Omega$ . Fig. 7 shows photographs of a BHF filled chamber on glass substrate wafer at 20, 22, 25 and  $30\ \text{W}/\text{cm}^2$  of static power. Note that gradually the parylene wall is melted as the power is increased. In the last photograph the power was sufficient to puncture the bottom wall thus etching the bottom Ti test resistor. We also performed similar experiment on oxidized silicon wafer with  $0.5\ \mu\text{m}$  of thermal oxide. The power needed to melt parylene on oxidized silicon substrates was significantly larger,  $\sim 100\text{-}200\ \text{W}/\text{cm}^2$  due to the thermal conduction heat loss. Fig. 8 shows the plot of the Ti test resistance versus time after transience indicating that the resistor is being attacked by the BHF. The resistance becomes very high after roughly 15 seconds after the transience is activated.

*a) Energy Discharge Burst Test:* We also performed reservoir burst tests by rapidly discharging a  $0.47\ \mu\text{F}$  capacitor on the Al heater. This method of transience activation is much more efficient than the static method as the discharge time is very small thus minimizing energy loss due to thermal conduction to the substrate below. Experimentally we observed burst energies of  $\sim 35\ \text{mJ}/\text{cm}^2$  on highly-insulated glass wafers and  $\sim 100\ \text{mJ}/\text{cm}^2$  required for the onset of parylene melting on the oxidized silicon wafers.



We can now compare the experimental values to those predicted by Eq. (3). Using Eq. (2) with  $\rho_p=1.2\text{g/cm}^3$ ,  $T_m=290^\circ\text{C}$ ,  $\rho_H=2.7\text{ g/cm}^3$ ,  $C_p=1\text{ J/g-K}$ ,  $C_H=0.91\text{ J/g-K}$  and assumed typical value of latent heat of polymers  $L_p\sim 100\text{ J/g}$  we calculate a lossless melting energy of  $\sim 41\text{ mJ/cm}^2$ . If we consider the energy loss term, the burst energy increases considerably. In particular for the oxidized silicon substrate the thermal resistance of a  $0.5\text{ }\mu\text{m}$ -oxide on top of a  $0.5\text{ mm}$  silicon substrate is  $42\times 10^{-3}\text{ K cm}^2/\text{W}$ . Using an electrical resistance for the Al heater of  $100\text{ }\Omega$ , the discharge time constant is  $\tau\sim 50\text{ }\mu\text{s}$ . If these values are used in Eq. (3) we obtain a calculated burst energy of  $\sim 300\text{ mJ/cm}^2$ . This is consistent with the observed burst energy for the oxidized silicon devices.

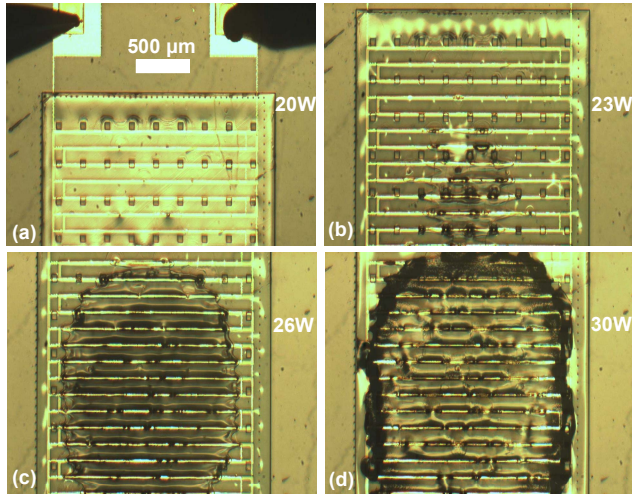


Figure 7. Parylene melting of sealed reservoir at different DC heater power conditions: (a) 20W, (b) 23W, (c) 26W and (d) 30W.

The experimental burst energies appear to be somewhat lower than those predicted by Eq. (3). This is expected as Eq. (3) assumes that all of the parylene is melted, but it is not necessary to melt the entire wall in order to trigger transience.

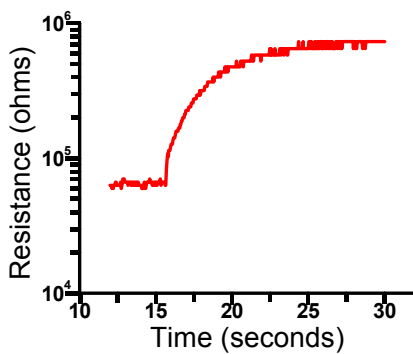


Figure 8. Ti test resistance vs time showing chemical attack about 15 sec after transience activation.

## V. CONCLUSION

This paper presents the fabrication and test of a microfluidic device used for triggered chip transience. The device consists of a microfabricated reservoir that holds a chemical agent which is released using an activation electrical

signal. The released chemical agent thus destroys a microchip placed below when transience is activated. The device was successfully tested using wafers containing Ti test resistors. Successful activation energies of  $35\text{-}100\text{ mJ/cm}^2$  were recorded for glass and oxidized silicon substrates.

## ACKNOWLEDGMENT

We would like to thank Rajesh Surapaneni, Tridib Ghosh, Shashank S. Pandey and Pradeep Pai of the University of Utah for their help and support during the development and testing of these devices.

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