Efficiency Characterization and Impedance Modeling of a Multilevel Switched-Capacitor Converter Using Pulse Dropping Switching Scheme

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***Abstract*—A pulse dropping switching technique (PDT) has been presented in this paper to accomplish variable conversion ratio (CR) in a multilevel modular capacitor-clamped dc–dc converter in the step-up conversion mode. The switching pattern is generated by comparing a triangular wave with a rectangular wave, and a proper output voltage regulation can be obtained by controlling the relative frequency and amplitude of these two waveforms. A state-space modeling technique has been applied here to estimate the variation in equivalent output resistance (EOR) for different operating conditions of the PDT. The EOR can be varied in a wide range without changing the operating frequency of the converter, and thereby the PDT enhances the degrees of freedom to accomplish voltage regulation in a two-phase switched-capacitor converter. Slow-switching limit of the converter has been derived to define the boundary of the EOR. Different challenges and limitations of the proposed modulation scheme has been discussed in detail, and the proposed analysis has been verified by comparing the analytical expressions with the simulation and experimental results for different switching frequencies, modulation indices, and number of active modules. In addition, variations in the CR, efficiency and ripple voltage for different number of active modules and switching conditions have been described in detail.**

***Index Terms*—Modeling, modular, modulation, multilevel, output resistance, state space, switched capacitor, voltage regulation.**

I. Introduction

SWITCHED-CAPACITOR converters (SCCs) typically have many favorable attributes such as high power density, compactness, high efficiency, low voltage stress on switches, and realization possibilities for system-on-chip (SOC) applications [1]–[29]. In general, an SCC can achieve very high efficiency for a fixed set of conversion ratio (CR), and the efficiency rapidly degrades with any regulation in the output voltage [23]–[29]. In [26], a four-level flying capacitor converter was presented for the plug-in hybrid electric vehicle (PHEV) and hybrid electric vehicle (HEV) applications that can achieve 97% or higher efficiencies for a continuous power range up to 30 kW. The multilevel modular capacitor-clamped converter (MMCCC) presented in [13] has reported to achieve efficiency higher than 94% in the step-up mode. A zero-current switching multilevel SCC that utilizes the stray inductances of the PCB and other components to achieve zero current switching has been reported to perform at 97% or higher efficiencies for the entire range of its operation [5].

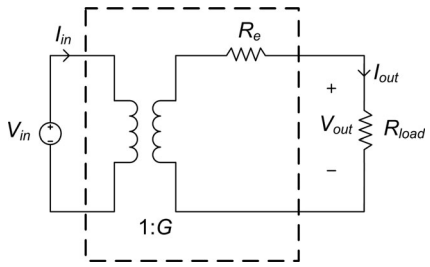

Fig. 1. Equivalent circuit model of an SCC (placed inside the dashed rectangle).

The most accepted steady-state model of an SCC is a transformer with a fixed gain and an equivalent output resistance (EOR) in series of the transformer [1], [10], [15]–[22], and an EOR represents all the conduction and switching losses inside the switches and capacitors. The equivalent circuit model of an SCC is shown in Fig. 1. Here, $V_{\rm in}$ is the input voltage, $R_{\rm load}$ is the output load resistance, R_e is the EOR, $I_{\rm in}$ is the input current, $I_{\rm out}$ is the output current, $V_{\rm out}$ is the output voltage, and G is a fixed gain that depends on the configuration of the SCC. Therefore, the upper limit of the efficiency of an SCC in terms of the previously mentioned parameters is given in (1) [1], [10]. This equation is derived based on the widely used transformer model of the SCC, and it is considered that the relation of the input and output current of an ideal transformer, i.e., $I_{\rm in} = G \times I_{\rm out}$ is applicable here as well

$$\eta_{\max} = \frac{V_{\rm out} I_{\rm out}}{V_{\rm in} I_{\rm in}} = \frac{V_{\rm out}}{V_{\rm in}} \frac{1}{G} = \frac{1}{1 + \frac{R_e}{R_{\rm load}}}. \tag{1}$$

Several methods have been proposed in the literature to determine the EOR of an SCC, and these methods are well described in [16], [20], [31], and [33]. In [16], EOR is presented as a function of two resistances: slow-switching limit $(R_{\rm SSL})$ and fast-switching limit $(R_{\rm FSL})$. The slow-switching limit is derived with the assumption that all switches and interconnects are ideal, and $R_{\rm SSL}$ is inversely proportional to the operating frequency of the SCC. Therefore, $R_{\rm SSL}$ is approximately equal to R_e of an SCC being operated at reasonably lower frequencies where the switching and conduction losses are significantly

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low compared to the losses associated with the charging and discharging operations of the capacitors. $R_{\rm SSL}$ becomes significantly small, and $R_{\rm FSL}$ constitutes most of the R_e at higher frequencies. $R_{\rm FSL}$ is considered when losses due to $R_{\rm DS(ON)}$ of the MOSFETs and interconnect parasitic dominates the total power loss. This method provides closed-form equations of $R_{\rm SSL}$ and $R_{\rm FSL}$, and these equations can be widely used in order to compare the performance of different SCCs. In [20], and [32], a state-space circuit analysis technique was proposed to calculate the steady-state EOR of different SCCs. This method is an excellent choice to characterize output resistance since it provides flexibility to analyze the asymmetric duty ratio, different dynamics, and other deviations from the ideal operation of an SCC.

Different methods to control the EOR of different SCCs, and therefore, to attain variable CR can be found in the literature. Since $R_{\rm SSL}$ is inversely proportional to the operating frequency, it is possible to achieve variable CR by varying the operating frequency of a two-phase SCC [11]–[20]. However, these $R_{\rm SSL}$ and $R_{\rm FSL}$ estimations were performed for only the two-phase variants of the SCC family. Variation in CR by controlling both the duty ratio and frequency of a reconfigurable buck-type SCC was presented in [23], and [24]. In [27], an interleaved SCC has been described that uses two sets of stages along with a pulse width modulation (PWM) technique to achieve wide range of variation in the CR for both step-up and step-down modes. A voltage regulation method for high power SCCs utilizing the presence of stray inductances was presented in [28], and the duration of the sinusoidal charging current was controlled to attain the desired voltage regulation.

This paper presents and summarizes the recent advancements in the voltage regulation technique applicable to an MMCCC circuit [21], [22]. The MMCCC, previously developed by the coauthor, is a highly efficient, completely modular, bidirectional SCC and provides many advantageous features: high switch utilization factor, multiple-load source integration, module bypass and fault-tolerant capability, etc. [12]–[14]. However, it is difficult to achieve significant output voltage regulation by duty ratio control [14], or sinusoidal charging current control due to the construction of the converter. Therefore, the proposed pulse dropping technique provides an excellent means to achieve variable CR using an MMCCC and adds some degrees of freedom beyond the general tuning parameters: operating frequency and number of active modules.

A brief summary of the MMCCC and its operation is described in Section I-A. In Section I-B, the pulse dropping technique (PDT) has been presented in detail, and the switching pattern is generated by comparing a square wave with a triangular wave. Similar to sinusoidal pulse width modulation (SPWM), two modulation indices are defined to explain the switching pattern. Different limitations and challenges of the proposed technique are summarized in Section I-C. State-space modeling technique presented in [20] has been used here to estimate the EOR of the converter for different operating conditions of the switching scheme. Constraints on the output load resistance have been derived in Section II to achieve a quasi-continuous conversion ratio (qCCR). The simulation and experimental results for a three-, four-, and five-module MMCCC are shown in Section III. Finally, conclusions and potential follow-up research activities have been documented in Section IV.

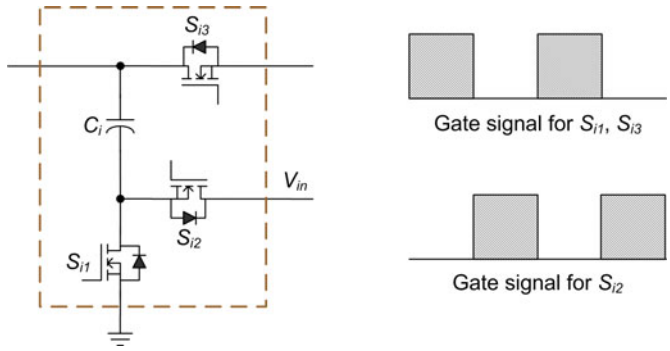

Fig. 2. Schematic diagram of an MMCCC module along with the complementary gate signals.

A. MMCCC: Structure and Operation

The MMCCC is a bidirectional two-phase modular SCC. The maximum CR of an MMCCC circuit is defined by the number of active modules. Schematic of an MMCCC module and the complementary switching pattern are shown in Fig. 2. Each module of the MMCCC circuit consists of a capacitor (C_i) and three switches (S_{i1}, S_{i2}, S_{i3}). Therefore, an N-module MMCCC requires $(N+1)$ capacitors and $(3\times N+1)$ switches including the output stage of the converter.

Inside each module, two switches are being operated in-phase and the third switch is operated out-of-phase. In Fig. 2, switches S_{i1}, and S_{i3} are operated in-phase, and S_{i2} is operated out-of-phase. Switches S_{i1} and S_{i2} of each module can be driven using a bootstrap gate driver circuit. S_{i3} forms a pair with the switch of the adjacent module that can be driven by another bootstrap gate driver circuit. Schematic diagram of a five-module MMCCC configured in the step-up mode is shown in Fig. 3. Here, $V_{\rm in}$ is the input voltage in the step-up conversion mode, and the switches with suffix B will have complementary operations to that of the switches with suffix R. Details of the operation of an MMCCC can be found in [12]–[14].

B. PDT

The proposed switching pattern can be generated by comparing a square wave signal with a triangular wave signal. Two modulation indices are defined to describe the generation of the switching scheme: amplitude modulation index (m_a) and frequency modulation index (m_f). Amplitude modulation index is defined as the ratio between the amplitudes of the square wave $(\widehat{v}_{\rm sqr})$ to the amplitude of the triangular wave $(\widehat{v}_{\rm tri})$ as shown in (2). Similarly, frequency modulation index is the ratio between the frequencies of the waveforms as shown in (3). Here, $f_{\rm sqr}$ and $f_{\rm tri}$ are the frequency of the square and triangular waves, respectively

$$m_a = \frac{\widehat{v}_{\rm sqr}}{\widehat{v}_{\rm tri}} \leq 1.0 \tag{2}$$

$$m_f = \frac{f_{\rm sqr}}{f_{\rm tri}} \geq 1.0. \tag{3}$$

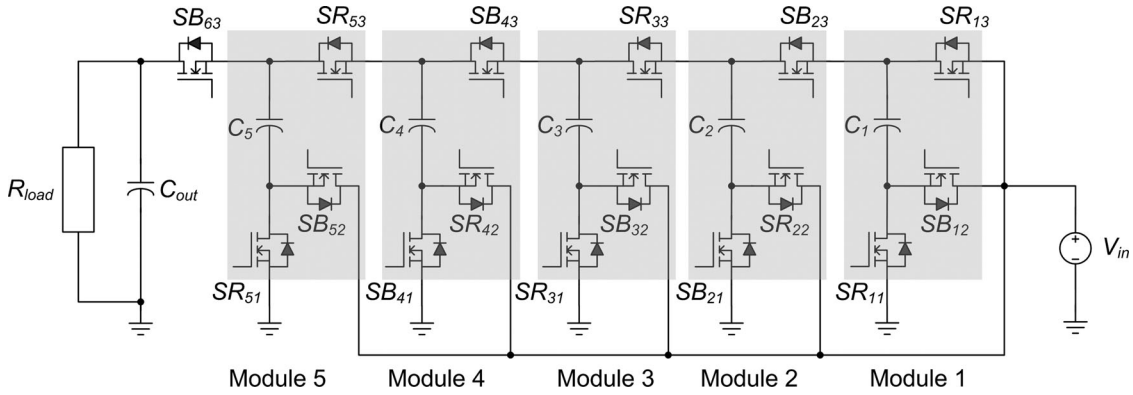

Fig. 3. Schematic diagram of a five-module MMCCC in the step-up mode.

Generation of the complementary switching patterns for different values of m_f and m_a is shown in Fig. 4. It should be noted that the resulting switching pattern has a time period T equal to the time period of the triangular wave ($1/f_{\rm tri}$), and the maximum number of ON-states within this time period depends on the value of m_f. For instance, the maximum number of ON-states for $m_f = 10$ is 10 for each of the complementary switching patterns. The number of times a switch is ON during this time interval T decreases with smaller m_a. For $m_f = 10$ and $m_a = 0.3$, any MOSFET in the MMCCC is ON three times during the switching period (T), and these ON time durations may have different lengths. Although an MMCCC is a two-phase SCC, it is considered here as a multiphase converter for better understanding. As an example, there are six phases present within the time period T shown in Fig. 5.

All the phases can be divided in two segments, and one of the segments (segment-I) consists of pulses with a width equal to the square wave's pulsewidth (phase 1 to phase 5) and the other segment (segment-II) consists of a fixed 1 or 0 (phase 6) depending on the switch under consideration. It should be noted that depending on the value of m_a, there might be a pulse in segment-I with a smaller pulsewidth than the pulsewidth of the square wave as illustrated in Fig. 6 for $m_f = 10$ and $m_a = 0.35$.

C. Limitations and Challenges of the PDT

Different aspects of the proposed modulation technique to achieve variable CR from an MMCCC converter have been discussed in the previous sections. However, the proposed technique has several limitations and challenges as well. One of the primary parameters used for varying the EOR using the PDT is the amplitude modulation index (m_a), and the correlation between the EOR and m_a is not linear. The EOR varies at a slower rate for any reduction in m_a starting from 1.0 and shows wide variation when m_a is close to zero. Moreover, continuous variation in m_a is not recommended where there might be a phase with ON/OFF duration smaller than the pulsewidth of the square wave signal, and these values of m_a have not been considered in this paper to avoid complexity in the analysis, control, and high input/output current ripples.

Since the proposed technique provides an additional degrees of freedom, the regulation of the SCC converter becomes a complex multiobject functional inequality constrained optimization problem similar to combined PWM and pulsed frequency modulation discussed in [34]. In [34], optimal duty cycle and switched period selection for a switched mode —dc–dc converter without the prerequisite of considering first-order approximations was discussed. Similarly, the correlation between the EOR and m_a is not linear, and this poses a higher order control issue than first-order approximation. The output voltage and current ripple as a function of load will make the optimization of the converter more complicated and this control issues are beyond the scope of the work. Moreover, the present research on the PDT to achieve variable CR does not address the circuit level design optimization of the converter to ensure optimal efficiency over wide range of load variation as described in [35].

Although the state-space model (SSM) and $R_{\rm SSL}$ estimation methods have been discussed in this paper for different operating points of the PDT, these methods have their own limitations. The $R_{\rm SSL}$ estimation can be applied for two-phase SCCs and this method assumes that the charge in the capacitor transfers impulsively which is not practical. However, the SSM provides the flexibility of analyzing multiphase SSCs and can handle nonuniform component parameters, variation in duty ratio, etc. Both of these analyses cannot account for the stray inductances of an SCC that may result from either the PCB or as parasitic component of other switches and capacitors. Moreover, the duty ratio of the MMCCC was fixed throughout the paper since it is not possible to achieve a significant voltage regulation by varying the duty ratio of the converter [14].

The qCCR ratio is attained if the variation in CR of 1.0 can be achieved for a fixed number of active modules, and it should be considered that it might not be possible to achieve a fine tuned variation in CR by varying m_a. Moreover, the analyses presented here for achieving different CR has been performed for resistive loads only, and analyses for other loads (*R–L* or *R–C*, etc.) have been left as a future research.

The proposed technique adds some additional degrees of freedom for achieving variable CR using an MMCCC, and at the same time, it becomes a challenge to prioritize the available choices. The $R_{\rm SSL}$ estimation described in Section II-B can be used for determining an initial estimation of $f_{\rm sqr}$ and m_f, and the frequency of the triangular wave $(f_{\rm tri})$ can be found using these parameters $(f_{\rm sqr}, m_f)$ from (3). These values can be used

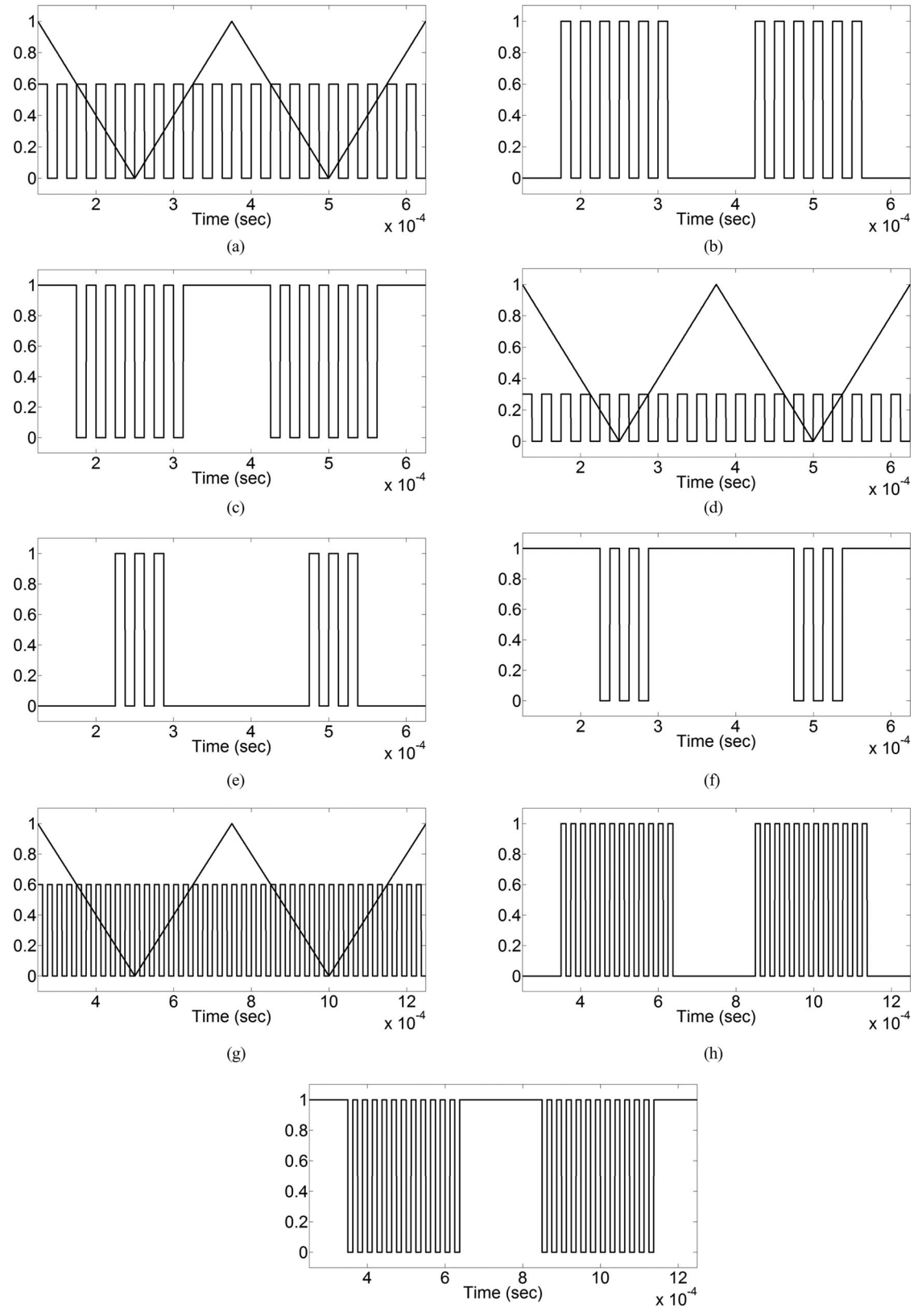

Fig. 4. Generation of the complementary switching pattern for: (a) $m_a = 0.6$ and $m_f = 10$, (d) $m_a = 0.3$ and $m_f = 10$, (g) $m_a = 0.6$ and $m_f = 20$. Complementary switching patterns for: (b) and (c) $m_a = 0.6$ and $m_f = 10$, (e) and (f) $m_a = 0.3$ and $m_f = 10$, (h) and (i) $m_a = 0.6$ and $m_f = 20$.

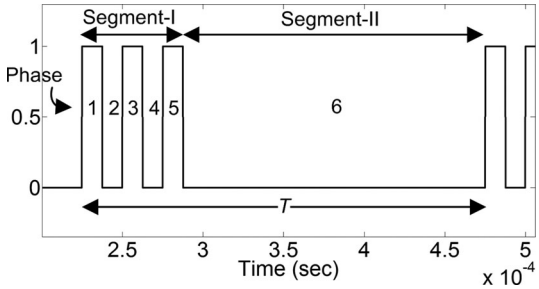

Fig. 5. Illustrating the multiphase switching pattern for an MMCCC using the PDT.

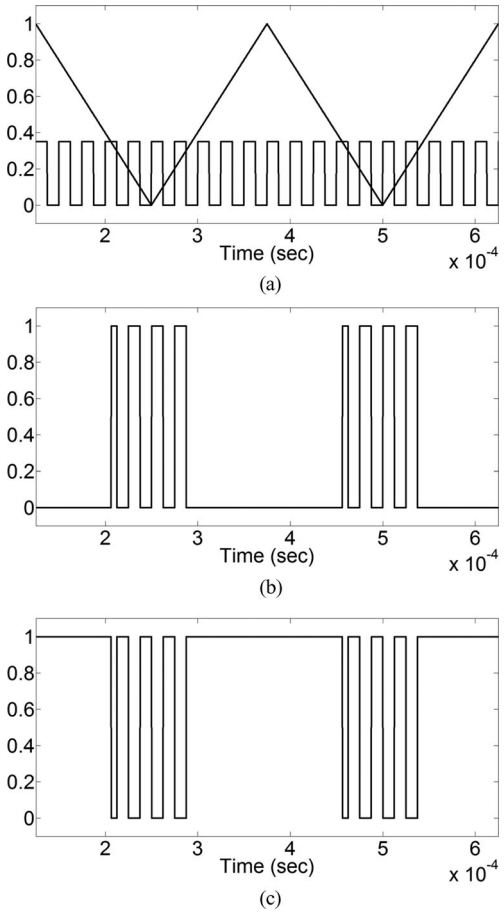

Fig. 6. (a) Generation of the complementary switching pattern for $m_a = 0.35$ and $m_f = 10$, (b) and (c) resulted complementary switching pattern.

for estimating the variation in EOR for different values of m_a using the state-space analysis shown in Section II-A. Therefore, the proposed modulation scheme provides another direction of research on control of different parameters of the PDT to achieve output voltage regulations using the MMCCC, and this will be covered in detail in future works.

II. Analysis of EOR for the PDT

An EOR estimation technique for complex SCCs using the conventional state-space circuit analysis technique was presented in [20], and this method has been utilized in this paper to estimate EOR of the MMCCC when a PDT is applied to accomplish variation in CR. However, this method does not provide any closed-form expression of EOR.

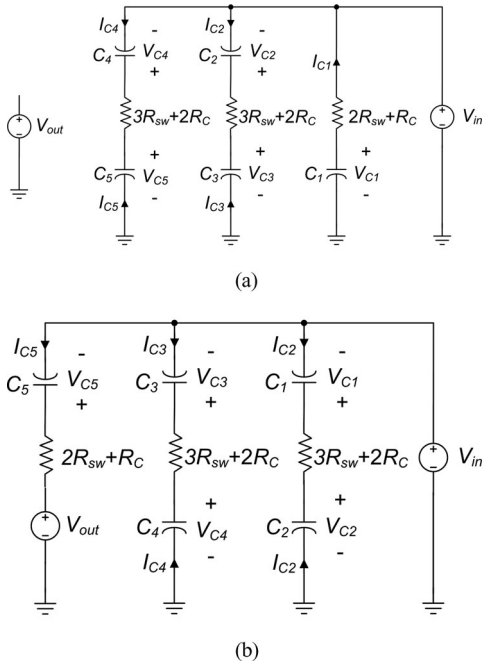

Fig. 7. Circuit configuration of a five-module MMCCC during two complementary phases of the clock signal. The activated switches are replaced with their ON-resistances, and R_c is the ESR of each capacitor.

In general, the operating frequency of an MMCCC is below 100 kHz and $R_{\rm SSL}$ provides a good approximation of EOR at that range of frequency [5], [12]–[18], [21], [22]. Moreover, it is possible to derive a closed-form equation of $R_{\rm SSL}$ using the method described in [15]–[18] as long as the SCC is a two-phase converter. Therefore, $R_{\rm SSL}$ has been derived at the boundaries of the PDT where the operations of the MMCCC can be interpreted as a two-phase SCC. This analysis provides a straightforward way to calculate an approximate range of EOR variation that can be used for constraining the output load resistance to attain qCCR using an MMCCC. Each additional level of an MMCCC adds a voltage gain equal to one, and qCCR is achieved when the variation in CR is equal to one.

The EOR estimation using the state-space modeling has been described in Section II-A and the estimation of $R_{\rm SSL}$ at the boundaries of the PDT switching is presented in Section II-B.

A. Analysis of EOR Estimation Using the SSM

The number of phases present in the switching cycle of the PDT (T) depends on values of m_f and m_a. There is maximum $(2 \times m_f)$ number of phases present during the time interval, T. However, there are only two sets of switches $(S_B$ and $S_R)$ that are ON in each alternative phases of the clock. Therefore, there are only two different circuit configurations for the MMCCC due to the complementary switching pattern of the converter. These circuit configurations for a five-module MMCCC are shown in Fig. 7. Here, $R_{\rm sw}$ and R_C are the ON-resistance of a MOSFET and equivalent series resistance (ESR) of a capacitor in a module of the MMCCC, respectively.

In Fig. 5, six phases constitute the gate signals for $m_a = 0.3$ and $m_f = 10$. KVL and KCL can be applied to derive N

independent equations for each phase of operation of an N-module MMCCC. These equations can be organized in a form shown in (4)

$$E_s i + F_s v + G_s u = 0. \tag{4}$$

Here, suffix s is the phase index. s is an odd number when SR switches are activated (ON) and s is even when SB switches are activated (ON). $\boldsymbol{v}$ and $\boldsymbol{i}$ are the column vectors of the voltages and currents of the capacitors, respectively. Input and output voltages of the converter form the vector: $\boldsymbol{u} = [V_{\text{in}} V_{\text{out}}]^T$. $\boldsymbol{E}$, $\boldsymbol{F}$, and $\boldsymbol{G}$ matrices are consist of coefficients of the KVL and KCL equations during each phase of the converter. Two sets of $\boldsymbol{E}$, $\boldsymbol{F}$, and $\boldsymbol{G}$ matrices for circuit configurations shown in Fig. 7 are given in (5) and (6), respectively. Here, the suffix o and e indicates whether s is an even or an odd number.

Considering the voltages across the capacitors of each module as state variables, the state-space equation for each

$$E_e = \begin{bmatrix} 0 & 3R_{\text{sw}} + 2R_C & 0 & 0 & 0 \\ 0 & 0 & 0 & 3R_{\text{sw}} + 2R_C & 0 \\ 0 & 0 & 0 & 0 & -(2R_{\text{sw}} + R_C) \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \end{bmatrix}$$

$$F_e = \begin{bmatrix} -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$G_e = \begin{bmatrix} -1 & 0 \\ -1 & 0 \\ -1 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{5}$$

$$E_o = \begin{bmatrix} 2R_{\text{sw}} + R_C & 0 & 0 & 0 & 0 \\ 0 & 0 & 3R_{\text{sw}} + 2R_C & 0 & 0 \\ 0 & 0 & 0 & 0 & 3R_{\text{sw}} + 2R_C \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

$$F_o = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & -1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$G_o = \begin{bmatrix} -1 & 0 \\ -1 & 0 \\ -1 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{6}$$

phase can be written in the form as shown in (7).

Here, $\boldsymbol{C}$ is a diagonal capacitance matrix with C_{kk} is the kth diagonal element and C_{kk} is equal to the capacitance of kth module. Considering the initial value of the state vector $\boldsymbol{v}$ is $\boldsymbol{v}(\boldsymbol{0})$, voltages across the capacitors at the end of each phase can be written as shown in (8). $\boldsymbol{\Phi}$ and $\boldsymbol{\Gamma}$ are derived from (9), where t_s is the duration of the phase s.

Since the converter is being operated under steady-state condition, voltage across any capacitor after the time period T is equal to the voltage across that capacitor at the beginning of the switching cycle [14]. This is shown in (10).

Each capacitor is charged and discharged in two consecutive phases. Therefore, the net amount of charge flow for charging/discharging a capacitor during a switching cycle of duration $T\,(=1/f_{\text{tri}})$ can be calculated using (11). Here, the suffix i is the index of the capacitors.

Unlike many other SCCs, each capacitor in the MMCCC shares the same amount of charge which is equal to the amount of charge transferred to the output load resistance

$$\begin{aligned} \dot{v} &= A_s v + B_s u \\ A_s &= -C^{-1} E_s^{-1} F_s \\ B_s &= -C^{-1} E_s^{-1} G_s \end{aligned} \tag{7}$$

$$\begin{aligned} V(1) &= v(t_1) = \Phi_1 v(0) + \Gamma_1 u \\ V(2) &= v(t_1 + t_2) = \Phi_2 \Phi_1 v(0) + (\Phi_2 \Gamma_1 + \Gamma_2) u \\ &\vdots \\ V(6) &= v(t_1 + t_2 + t_3 + t_4 + t_5 + t_6) \\ &= \Phi_6 \Phi_5 \Phi_4 \Phi_3 \Phi_2 \Phi_1 v(0) + (\Phi_6 \Phi_5 \Phi_4 \Phi_3 \Phi_2 \Gamma_1 \\ &\quad + \Phi_6 \Phi_5 \Phi_4 \Phi_3 \Gamma_2 + \Phi_6 \Phi_5 \Phi_4 \Gamma_3 \Phi_6 \Phi_5 \Gamma_4 + \Phi_6 \Gamma_5 + \Gamma_6) u \end{aligned} \tag{8}$$

$$\begin{aligned} \Phi_s &= e^{A_s t_s} \\ \Gamma_s &= A_s^{-1} (e^{A_s t_s} - \mathrm{I}) B_s \\ s &= 1, 2, \ldots, 6 \end{aligned} \tag{9}$$

$$\begin{aligned} V(6) &= v(t_1 + t_2 + t_3 + t_4 + t_5 + t_6) \\ &= \Phi_6 \Phi_5 \Phi_4 \Phi_3 \Phi_2 \Phi_1 v(0) + (\Phi_6 \Phi_5 \Phi_4 \Phi_3 \Phi_2 \Gamma_1 \\ &\quad + \Phi_6 \Phi_5 \Phi_4 \Phi_3 \Gamma_2 + \Phi_6 \Phi_5 \Phi_4 \Gamma_3 \Phi_6 \Phi_5 \Gamma_4 + \Phi_6 \Gamma_5 + \Gamma_6) u \\ &= v(0) \end{aligned} \tag{10}$$

$$q_i = \left\| c_i \left(\sum_{s=\text{odd}} V_i(s) - \sum_{s=\text{even}} V_i(s) \right) \right\| \tag{11}$$

$$i_{\text{out}} = q_i f_{\text{tri}} = q_i \frac{f_{\text{sqr}}}{m_f}$$

$$R_e = \frac{(N+1)V_{\text{in}} - V_{\text{out}}}{\mathrm{i}_{\text{out}}}. \tag{12}$$

Therefore, the EOR of the MMCCC (R_e) can be calculated according to (12).

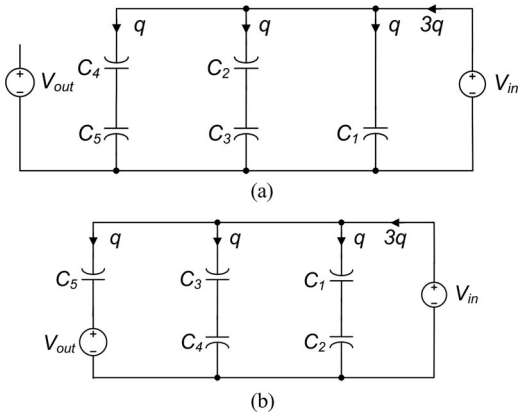

Fig. 8. Charge flow diagram of a five-module MMCCC for two phases of the clock.

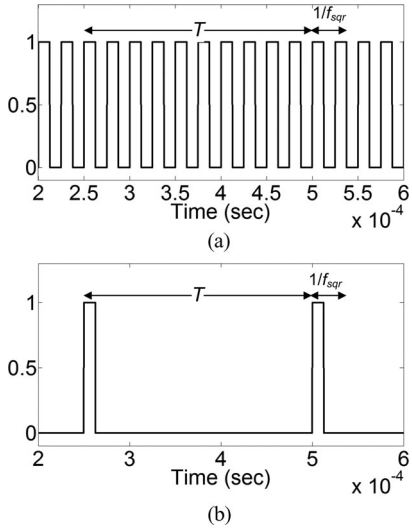

Fig. 9. Illustrating the boundaries of the PDT operation: (a) maximum number of phases is present for $m_a = 1.0$ and the effective switching frequency is equal to the frequency of the square wave, (b) minimum number of phases are present and the switching frequency is equal to the frequency of the triangular wave.

B. Derivation of $R_{\rm SSL}$ at the Boundaries of the PDT

The ON-resistance of the MOSFETs and ESR of capacitors are neglected when $R_{\rm SSL}$ of a two-phase SCC is derived and two charge multiplier vectors are defined for two phases of the clock as shown in (13) [18]

$$\begin{aligned} A_1 &= [\, q_{\rm out,1} \quad q_{c1} \quad q_{c2} \quad \ldots \quad q_{cN} \quad q_{\rm in,1} \,]\, /q_{\rm out} \\ &= [\, a_{\rm out,1} \quad a_{c1} \quad a_{c2} \quad \ldots \quad a_{cN} \quad a_{\rm in,1} \,] \\ A_2 &= [\, q_{\rm out,2} \quad -q_{c1} \quad -q_{c2} \quad \ldots \quad -q_{cN} \quad q_{\rm in,1} \,]\, /q_{\rm out} \\ &= [\, a_{\rm out,2} \quad -a_{c1} \quad -a_{c2} \quad \ldots \quad -a_{cN} \quad a_{\rm in,2} \,]. \end{aligned} \tag{13}$$

Here, N is the number of active modules in an MMCCC. Charge flow balance in a five-module MMCCC is shown in Fig. 8.

Any capacitor of an MMCCC shares the same amount of charge, and the charge multiplying vectors for the five-module MMCCC are given in (14)

$$\begin{aligned} A_1 &= [\, 0 \quad 1 \quad -1 \quad 1 \quad -1 \quad 1 \quad -3 \,] \\ A_2 &= [\, 1 \quad -1 \quad 1 \quad -1 \quad 1 \quad -1 \quad -3 \,]. \end{aligned} \tag{14}$$

Finally, the $R_{\rm SSL}$ of the five-module MMCCC can be derived from the following equation:

$$R_{\rm SSL} = \sum_{i=1}^{5} \frac{(a_{ci})^2}{C_i f_{\rm sw}} = \frac{5}{C f_{\rm sw}}. \tag{15}$$

Here, C is the capacitance of the capacitor in each module and $f_{\rm sw}$ is the switching frequency of the converter. For an N-module MMCCC, $R_{\rm SSL}$ can be written as shown in the following equation:

$$R_{\rm SSL} = \frac{N}{C f_{\rm sw}}. \tag{16}$$

It has been described in Section I-B that there are maximum $(2 \times m_f)$ and minimum two phases are present during the time interval T $(=1/f_{\rm tri})$. The $R_{\rm SSL}$ for an N-module MMCCC has been derived here at these boundaries of the PDT operation. The effective switching frequencies at these boundaries are $f_{\rm sqr}$ and $f_{\rm tri}$, respectively, and these are illustrated in Fig. 9. Therefore, the maximum and minimum values of $R_{\rm SSL}$ for an N-module MMCCC are shown in the following equation:

$$R_{\rm SSL,min} = \frac{N}{C f_{\rm sqr}} \tag{17a}$$

$$R_{\rm SSL,max} = \frac{N}{C f_{\rm tri}} = \frac{N \times m_f}{C \times f_{\rm sqr}} = m_f \times R_{\rm SSL,min}. \tag{17b}$$

It should be noted that there might be a phase with ON/OFF duration smaller than the pulsewidth of square wave signal within the period T (see Fig. 6). However, these values of m_a have not been considered in this analysis to avoid high input/output current ripples. qCCR can be accomplished using MMCCC in the step-up mode if the output voltage is reduced by a voltage equal to the input voltage [21], [22]. Therefore, the minimum EOR required to achieve qCCR can be calculated using (18)

$$R_{\rm qCCR} = \frac{R_{\rm load}}{N}. \tag{18}$$

The $R_{\rm SSL}$ estimation presented in this Section considers the losses associated with the charging/discharging of the capacitors only. MOSFET's switching and conduction losses as well as the losses incurred by the ESR of the capacitors have been neglected. However, this estimation of EOR in terms of $R_{\rm SSL}$ provides an simple closed-form equation that can be used as an initial design step for achieving required set of CRs, and more accurate estimation of EOR can be derived using the state-space method shown in Section II-A. A more detail guideline for the selection of design parameters has been discussed in later sections of this paper.

C. Computer-Based Numerical Simulation Results Generated by MATLAB for EOR Estimation Using the SSM

This section shows the computer-based numerical results obtained from the SSM described in Section II-A using MATLAB. Variation of EOR (R_e) of an MMCCC for variation in different

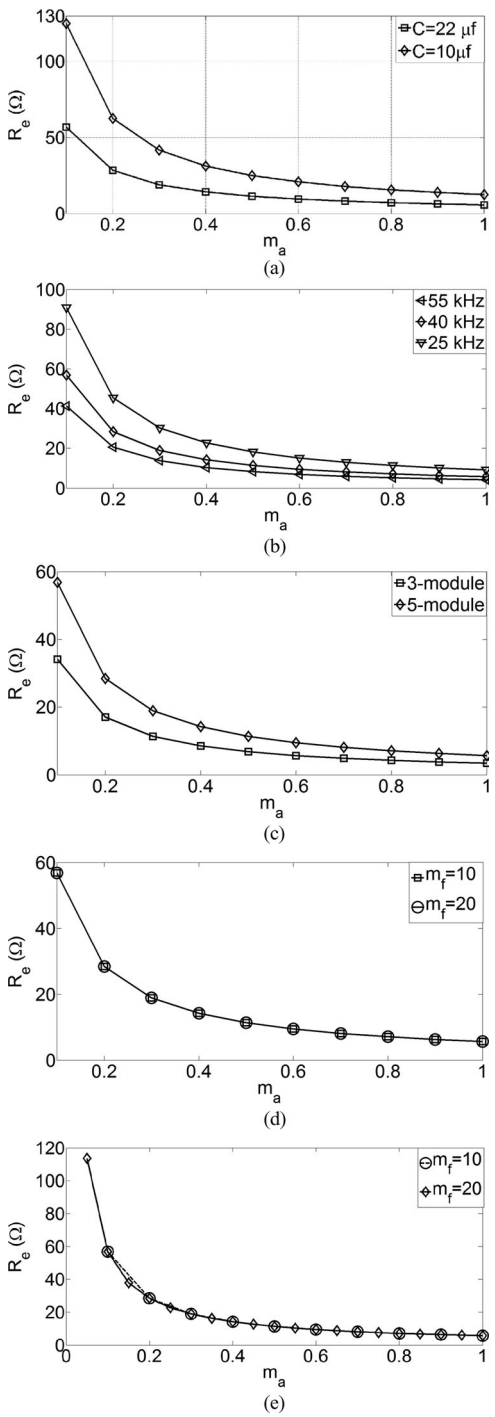

Fig. 10. Computer-based numerical simulation results generated by MATLAB for EOR estimation using the SSM. Variation in R_e as a function of m_a for (a) variation of capacitance in each module (b) variation in the square wave frequency, (c) variation in number of active modules, (d) variation in m_f, (e) illustrates the variation in R_e and its boundaries for two different values of m_f.

parameters is calculated in MATLAB, and the results are shown in Fig. 10. The ON-resistance of the MOSFETs $(R_{\rm sw})$ is set to 5.8 mΩ and the ESR of the capacitor (R_C) in each module is set to 10 mΩ. Duty ratio of the gate signals are set to 45%. Fig. 10(a) shows the variation in EOR versus m_a for a five-module

TABLE I
DEPENDENCY OF EOR ON DIFFERENT PARAMETERS

Parameter	Change in parameter	Change in EOR
m_a	Increase	Decrease
m_f	Increase	No change
f_{sqr}	Increase	Decrease
Number of Active modules	Increase	Increase

TABLE II
LIST OF DEFAULT PARAMETERS' VALUE USED IN THE SIMULATION

Parameter	Value
Square wave frequency	40 kHz
m_f	10
m_a	0.2-1.0
ESR of capacitor (R_c)	10 mΩ
MOSFET ON-resistance	5.8 mΩ
Diode threshold voltage	0.72
Diode resistance	2.66 mΩ
Capacitance of each module	22 μf
Output load	90 Ω

MMCCC for two different values of capacitance: $C = 22$ μf, 10μf. $f_{\rm sqr}$ and m_f are set to 40 kHz and 10, respectively. The EOR of MMCCC decreases in inverse proportion to the capacitance of each module, and this is applicable to the frequency of square wave $(f_{\rm sqr})$ as well. This is shown in Fig. 10(b) where the variation in EOR has been plotted for $f_{\rm sqr} = 25$, 40, and 55 kHz and $C = 22$ μf. The EOR of an MMCCC is proportional to the number of active modules as can be seen in Fig. 10(c). Interestingly, the EOR does not change with any variation in m_f. However, the lower limit of EOR is proportional to m_f. Therefore, a higher voltage regulation can be achieved by increasing the value of m_f, and these possibilities have been illustrated in Fig. 10(d) and (e). The effect of different parameters on the EOR (R_e) of the MMCCC is summarized in Table I.

III. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The EOR estimation analysis presented in Section II-A and the output voltage regulation concept using the PDT in an MMCCC have been verified through the simulation results using PSIM. A piecewise linear model of the drain to source diode is derived from the datasheet of IXTA160N10T7 power MOSFET [30]. Unless otherwise stated, the simulation has been performed using parameters listed in Table II. In order to estimate the EOR of the MMCCC, the output of the converter is connected to a dc current source only. The amplitude of the current source is varied from 0 A to 200 mA in steps of 50 mA, and the average output voltage was recorded. Finally, the average output voltage versus output current is plotted in MATLAB, and the EOR is measured from the slope of the best-fit straight line. All the simulation results are plotted along with numerical results for the SSM generated using MATLAB.

The variation in EOR of the converter as a function of m_a for two different values of capacitances: $C = 22$ and 10 μf

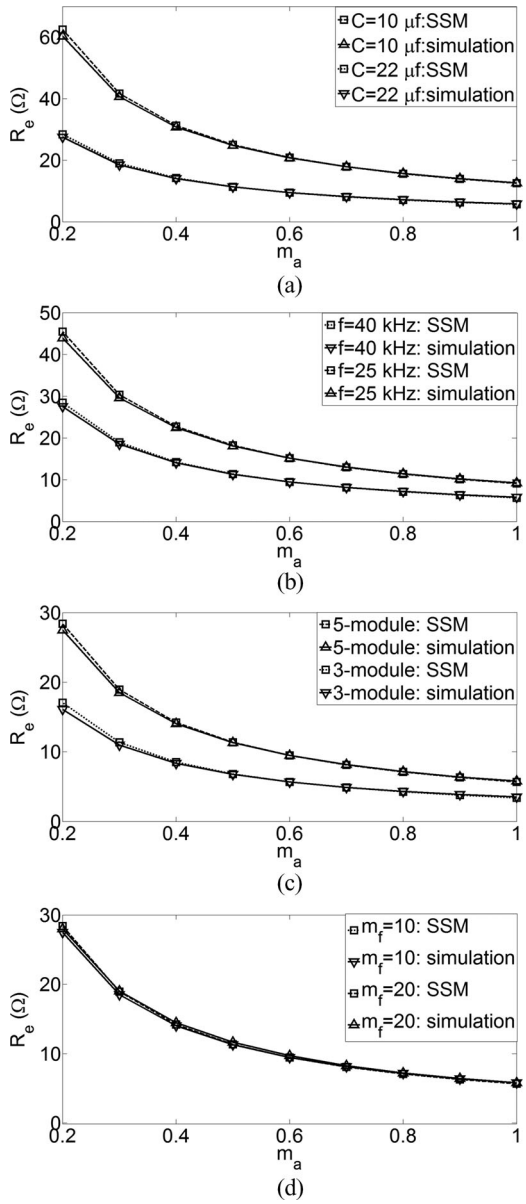

Fig. 11. Simulation results. Variation in R_e as a function of m_a for (a) variation of capacitance in each module (b) variation in the square wave frequency, (c) variation in number of active modules, (d) variation in m_f.

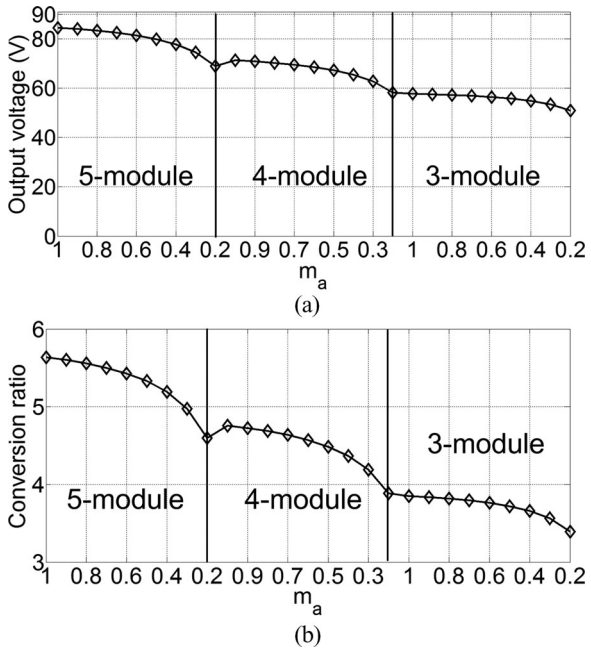

Fig. 12. Variation in (a) output voltage and (b) CR as a function of m_a and number of active modules.

are plotted in Fig. 11(a). The EOR of the MMCCC derived using the state-space analysis is in agreement with the result obtained from PSIM simulations. There are small deviations observed in the simulation results from the analytical model because of increased output voltage ripple with the decrease in m_a. However, input and output voltages are considered constant during the state-space analysis.

The variation in EOR for two different frequencies of the square wave: $f_{\rm sqr} = 25$, 40 kHz and two different modules are shown in Fig. 11(b) and (c), respectively. The EOR of the MMCCC increases for any decrease in the square wave frequency $(f_{\rm sqr})$ and increase in number of active modules. Variations in the EOR for two different values of m_f are depicted in Fig. 11(d). The simulations results show coherence with results obtained using the SSM.

The output of the MMCCC is then connected to a fixed 90 Ω resistor in place of the current source to demonstrate the range of attainable CRs using the PDT. The input voltage of the five-module MMCCC was set to 15 V and the output voltage was observed by varying m_a from 0.2 to 1. Simulations were repeated for the three-, four-, and five-module MMCCC, and the variation in output voltage and CR versus m_a for the three-, four-, and five-module MMCCC are shown in Fig. 12. It is possible to vary the CR from 3.39 to 5.63 by having a variation in m_a from 0.2 to 0.1, $m_f = 10$, and $f_{\rm sqr} = 40$ kHz using three different number of active modules. Although these results are described to demonstrate the competency of the PDT to achieve output voltage regulation, a guideline has been outlined in Section I-C to estimate PDT parameters to achieve the required CR using an MMCCC.

For a fixed number of active modules (N), time period $T\ (=1/f_{\rm tri})$, m_f, and load resistance, the output voltage is maximum when $m_a = 1.0$, and the output voltage regulation increases with decrease in m_a. The modulation index m_a needs to be gradually reduced until the desired voltage regulation is achieved using N active modules. In case of achieving even smaller CR, it requires bypassing one of the active modules which will result in $N-1$ number of active modules and m_a is set to 1.0 again to achieve the maximum output voltage attainable using $N-1$ active modules. This has been graphically shown in Fig. 12.

Priority should be given to the lowest number of active modules when the same CR can be achieved using different number of active modules. This is for ensuring higher efficiency of power conversion since the efficiency of an N-module MMCCC is the

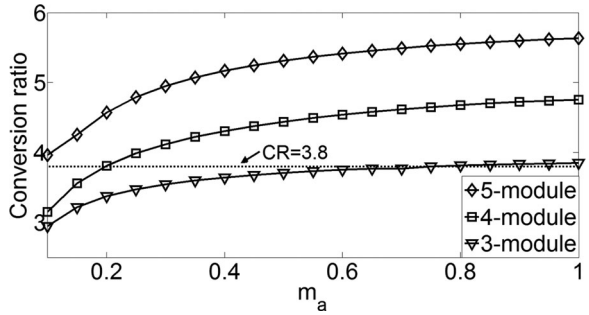

Fig. 13. Variation in CR versus m_a for $m_f = 20$. CR = 3.8 can be obtained using both four-module and three-module of the converter.

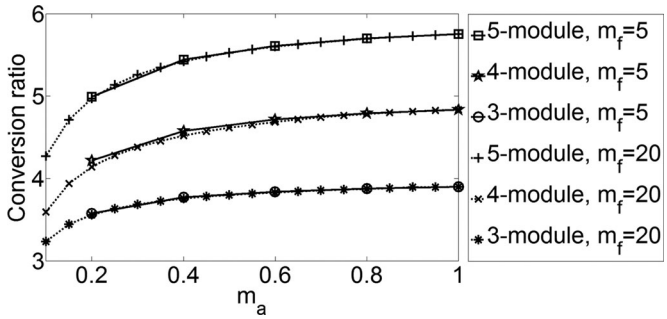

Fig. 14. CR versus m_a illustrating the effect of variation in m_f on CR.

highest when m_a is set to 1.0, and it decreases with any decrease in m_a. As an example: a CR of 3.8 could be achieved from a four-module MMCCC using either three modules or four modules. However, it is recommended to use three-module configuration since the same CR can be achieved using three-module MMCCC at $m_a = 0.8$ and at $m_a = 0.2$ with four-module MMCCC configuration. This has been depicted in Fig. 13.

It may not be possible to achieve the desired voltage regulation by varying only m_f and m_a, while the number of active modules remains fixed. This situation can be improved by decreasing the frequency of the square wave or increasing the value of m_f, or decreasing square wave frequency and increasing m_f together. The effects of varying square wave frequency and m_f have been illustrated in Figs. 14 and 15, respectively. In Fig. 14, increasing m_f from 5 to 20 while keeping the frequency of the square wave ($f_{\rm sqr}$) fixed at 40 kHz increases both the number of operating points and range of the CR variation. The effect of any variation in the square wave frequency on CR has been illustrated by considering two frequencies: $f_{\rm sqr} = 60$ kHz and $f_{\rm sqr} = 20$ kHz while keeping the value of m_f constant at 5. This is depicted in Fig. 15, and it is clear that the lower $f_{\rm sqr}$ provides wider variation in CR.

B. Experimental Results

A custom board has been designed that has two slots to accommodate two modules of the MMCCC, and any of the slots can be configured as an output stage as well. It is possible to control the number of active modules of an MMCCC by bypassing or deactivating one or more modules and this technique has been discussed in [12]. Within the scope of this project,

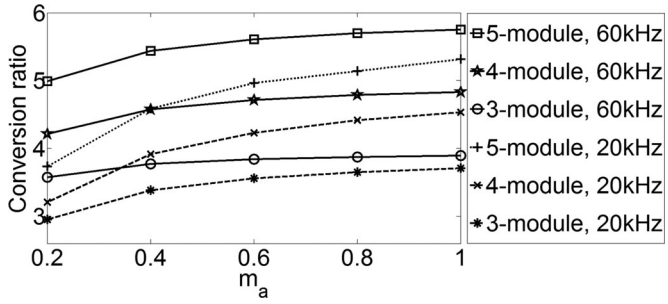

Fig. 15. CR versus m_a illustrating the effect of variation in $f_{\rm sqr}$ on CR.

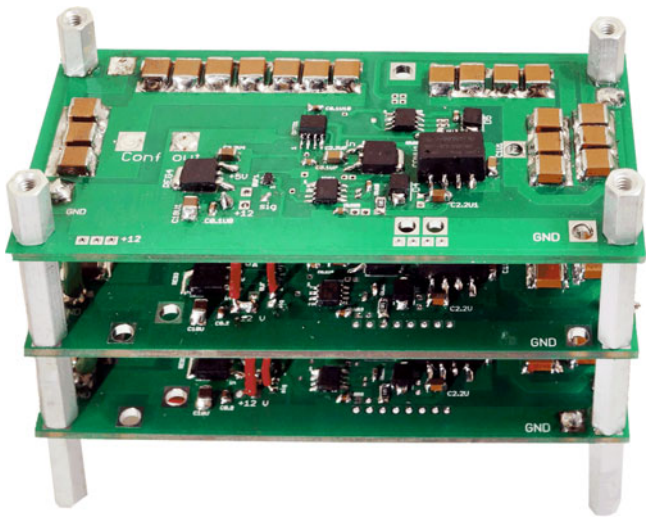

Fig. 16. Photograph of the five-module MMCCC prototype.

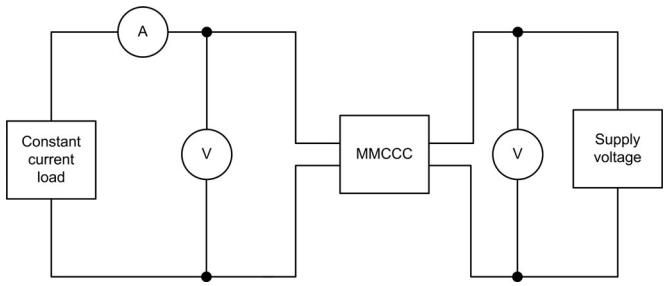

Fig. 17. Schematic diagram of the test setup used for estimating the EOR of the converter.

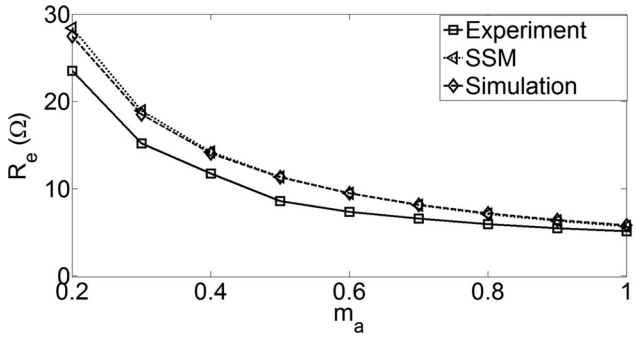

Fig. 18. Experimental results along with the simulation and analytical results showing the variation in R_e as a function of m_a.

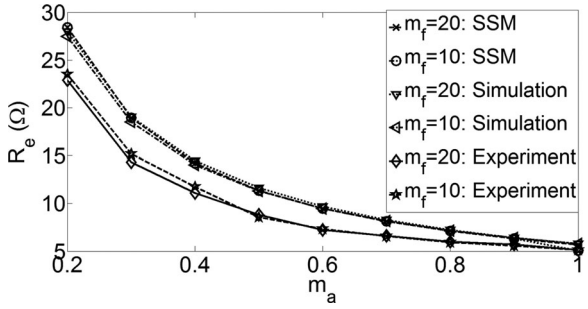

Fig. 19. Experimental and simulation results showing the variation of R_e versus m_a for two different values of m_f.

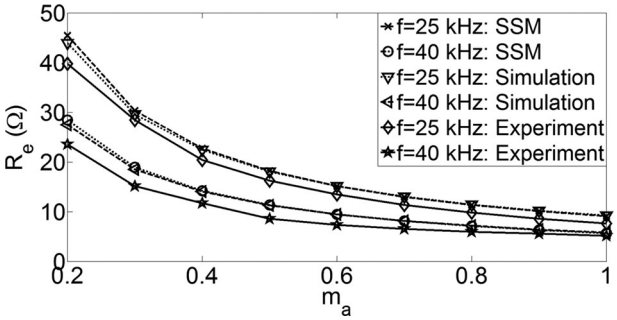

Fig. 20. Experimental and simulation results showing the variation of R_e versus m_a for two different values of the square wave frequency.

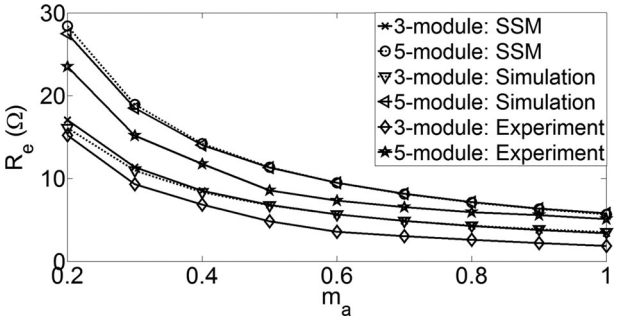

Fig. 21. Experimental and simulation results showing the variation of R_e versus m_a for the three- and five-module MMCCC.

three separate MMCCC prototypes with three, four, and five modules were built here for simplicity of operation so that no control scheme is needed to change the number of active modules. However, it is always possible to design a reconfigurable five-module MMCCC circuit, and the number of active modules could be changed in the range of 2–5 using the method presented in [12].

A photograph of the five-module MMCCC prototype is shown in Fig. 16. Ten 2.2-μf 250-V capacitors (C5750X7T2E225M250KE) are paralleled to form about 22-μf capacitance for each module. 100-V 160-A MOSFETs (IXTA160N10T7) are used as switches because they offer very low ON-resistance (5.8 mΩ typical) and high current carrying capability. IRS2183 bootstrap gate drivers from international rectifiers were used to drive each MOSFET pairs. Two parallel 10,000 μf electrolytic capacitors were used in parallel with the output of a bench-top power supply to reduce any voltage ripple at the input of the converter. The input voltage of the converter was fixed to 15 V. A TMS320F28335 microcontroller unit has been used to generate the necessary gate signals for the converter under test.

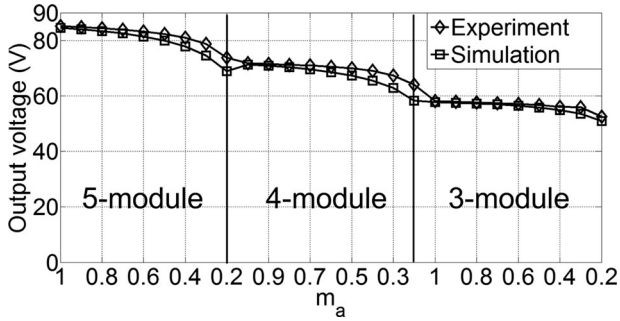

Fig. 22. Experimental and simulation results of output voltage versus m_a for different number of active modules.

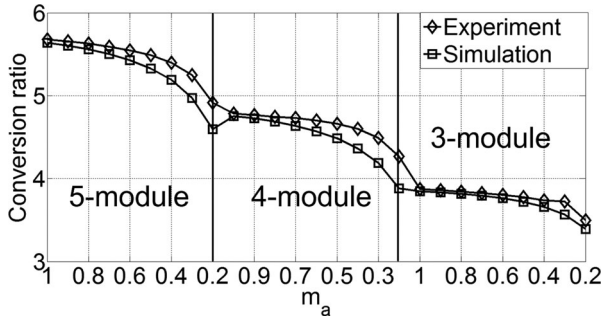

Fig. 23. Experimental and simulation results showing voltage CR versus m_a for different number of active modules.

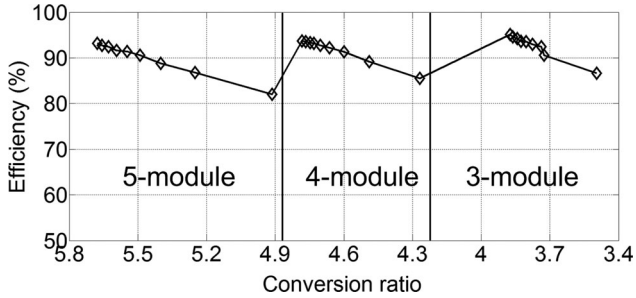

Fig. 24. Experimental results showing efficiency versus CR for different number of active modules.

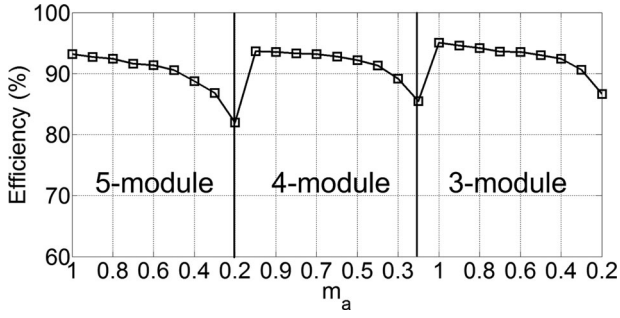

Fig. 25. Experimental results showing efficiency versus m_a for different number of active modules.

Fig. 26. (a)–(f) Oscilloscope capture of the gate signal (channel-1) and the output voltage (channel-2) of the converter for $f_{\mathrm{sqr}} = 40$ kHz, $m_f = 10$, $V_{\mathrm{in}} = 15$ V. (a) $m_a = 1.0$, five-module, (b) $m_a = 0.4$, five module, (c) $m_a = 0.9$, four-module, (d) $m_a = 0.4$, four-module, (e) $m_a = 0.8$, three-module, (f) $m_a = 0.2$, five module. Ripple voltage wave shapes for (g) $m_a = 0.2$, five-module, (h) $m_a = 0.2$, four-module, (i) $m_a = 0.2$, three-module MMCCC.

A schematic diagram of the setup used for estimating the EOR of the MMCCC is shown in Fig. 17. Two high precision fluke 8846A multimeters were used at the input and output of the converter. The output of the converter has been connected to a 3711-A dc electronic load, and it was configured as a constant current load. The output current was varied from 0 A to 200 mA in steps of 50 mA, and the output voltages were recorded. The EOR of the converter is measured by calculating the slope of the best-fit straight line of output voltage versus output current plot using MATLAB. The experimental results have been plotted in this section along with the simulation results for comparison.

The EOR variation of a five-module MMCCC for variation in m_a starting from 0.2 to 1.0 is shown in Fig. 18. The square wave frequency was set to 40 kHz, and m_f was set to 10. Any deviation in the EOR from the simulation and SSM values were contributed by the tolerance and variation of the capacitors, stray inductances of the circuit board, and parasitic inductances of the other components. The effect of variation in m_f is shown in Fig. 19. As previously described, the EOR values do not depend on any variation in m_f. Variations in EOR for the change in square wave frequency and number of active modules are shown in Figs. 20 and 21, respectively. EOR of the converter increases with any decrease in the square wave frequency or any increase in the number of active modules. Several oscilloscope captures of the microcontroller generated gate signals and the output voltage of the converter for different operating conditions are shown in the later part of this section.

In order to validate the variation in CR, the electronic load was configured as a constant resistive load with resistance equal to 90 Ω. The input power, output power, and efficiency of the converter were measured using PM3000ACE-001 power analyzer from Voltech Instruments Ltd. The output voltage and CR variation for the three-, four-, and five-module MMCCC as a function of m_a starting from 1.0 to 0.2 are shown in Figs. 22 and 23, respectively. m_f and $f_{\rm sqr}$ were set to 10 and 40 kHz, respectively. The variation of efficiency versus CR is plotted in Fig. 24, and the efficiency of the converter was varied from 95% to 82% for the range of the operation stated here and three different numbers of active modules of the MMCCC.

Similar to other SCCs, efficiency of the MMCCC decreases when CR is noninteger. The efficiency is also a function of the EOR and output load resistance $(R_{\rm load})$ of the converter as shown in (1). EOR increases more rapidly when m_a approaches to zero from its maximum value of 1.0, and the efficiency of the converter decreases drastically which is depicted in Fig. 25. Therefore, the spacing or efficiency difference between two points in Fig. 24 at high voltage regulation is wider than the spacing between two points at low-voltage regulation for a fixed number of active modules. For example, efficiency of the five-module MMCCC varies from 93.2% to 92.7% for a change in m_a from 1.0 to 0.9, and efficiency falls from 86.8% to 82% for variation in m_a from 0.3 to 0.2. The number of operating points on the efficiency versus CR plot depends on the maximum number of phases presents within the time period T $(=1/f_{\rm tri})$, and thereby can be controlled by varying m_f.

The correlation among the output voltage ripple, number of active modules, optimal design for efficiency over a wide load range, frequency of the triangular wave $(f_{\rm tri})$ and square wave $(f_{\rm sqr})$, capacitance of each module (C), and m_a require a more rigorous analysis similar to the complex optimal control for multiobjective functional inequality as discussed in [34], and [35], and it will be introduced in future publications.

It was observed that the output voltage ripple increases with any decrease in m_a. For any variation in m_a staring from 1.0 to 0.2, maximum ripple voltage is observed at $m_a = 0.2$. The output voltages at $m_a = 0.2$ for different number of active modules are captured in ac coupling mode using the oscilloscope as shown in Fig. 26 along with the gate signal generated by the microcontroller. The maximum percentage of ripple for the range of operation described here for the three-, four- and five-module MMCCC were 9.34%, 6.314%, and 8.435%, respectively. This amount of ripple ($<$10%) is tolerable in many applications of the SCC, especially in battery charging applications for HEV/PHEVs.

IV. Conclusion and Future Work

A new switching scheme/modulation technique termed as PDT has been presented in this paper to obtain variable CR in a multilevel SCC in the step-up conversion mode. The variation in EOR as a function of different parameters of the PDT has been analyzed using the state-space circuit analysis technique. Moreover, the range of EOR variation has been analyzed in terms of slow-switching limit as well that allows attaining qCCR variation by controlling different variables of the PDT. Since each additional module in the MMCCC adds a voltage gain equal to one, qCCR variation is referred to decrease in output voltage equal to the input voltage for a fixed number of active modules. These analyses have been verified through simulation and experiment results. Variation in CR ranging from 3.39 to 5.63 has been reported for the three-, four- and five-module MMCCC prototypes using the PDT, and the efficiency was varied within the range of 82%–95%. Moreover, a detail outline has been provided to control different parameters of the PDT to achieve a specific voltage regulation using an MMCCC. Therefore, the conducted study will provide a guideline to design a controller that can attain desired output voltage regulation for a fixed output load or attain constant output voltage irrespective of the output load variation. A closed-loop control for the MMCCC to interface dynamic input/output source/load is a potential extension of this study, and this will extend the application of SCCs in highly efficient sophisticated control systems: maximum power point tracking, automatic voltage regulators, and so on.

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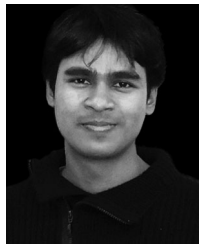

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