FROM CHIPS TO DUST: THE MEMS SHATTER SECURE CHIP

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ABSTRACT

This paper presents the implementation of a transience mechanism for silicon microchips via low-temperature post-processing steps that transform almost any electronic, optical or MEMS substrate chips into transient ones. Transience is achieved without any hazardous or explosive materials. Triggered chip transience is achieved by the incorporation of a distributed, thermally-activated expanding material on the chip backside. When heated at 160°C the expanding material produces massive chip cleavage mechanically shattering the chip into a heap of silicon dust.

INTRODUCTION

In today's critical military, financial and corporate applications microchips are increasingly used to process and store sensitive information. In every case of theft or loss of equipment there is a possibility of that such information being compromised by malicious subjects. The utilization of software data encryption and access passwords provides a first level of information protection, but encryption can eventually be cracked and the captured hardware can be copied and replicated. In these situations it is therefore increasingly more desirable to utilize microchips which incorporate triggered hardware destruction or disabling transience mechanisms that cannot be cracked.

Several hardware transience methods have been previously reported. These methods include the incorporation of energetic materials that ignite or explode chips [1-4] and chip dissolution by chemically corrosive agents [5-7]. In both of these methods the long term stability, safe handling, and disposal of these substances limits their practical lifetime and range of applications. Therefore it is highly desirable to develop a new transience mechanism that to does not use hazardous corrosive or explosive materials.

In this paper we demonstrate a new safer microchip transience mechanism. Instead of being based on corrosive or explosive materials, the new transience mechanism is based on mechanical stress generation. Mechanical stress is generated within the chip substrate using a distributed high-force actuating material. When the transience is activated, the actuator high level of stress mechanically shatters the chip literally reducing it to a heap of silicon dust as shown in Fig. 1.

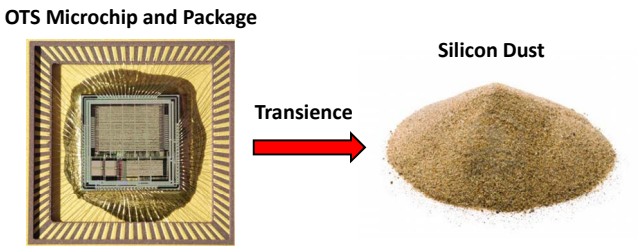

Figure 1: Schematic showing silicon chips being reduced to silicon dust by shatter transience action.

SHATTER TRANSIENCE

The actuating material is introduced into the silicon chips through low-temperature post-processing and micro-packaging steps; therefore the new method can transform almost any off-the-shelf silicon chip into a transient device.

First an OTS chip is partially diced on the backside with a series of closely spaced cuts at orthogonal directions. This dicing process produces a series of pillars and grooves that behave as cracks in the silicon substrate. The backside grooves are next refilled with the actuator material. The transience actuator consists of an expanding microscopic material that exerts pressure against the thin silicon walls or pillars left by the dicing process thus inducing fractures and shattering. If the induced stress is sufficiently large the cracks propagate all the way through to the top surface thus fracturing the chip into a large number of pieces as shown in Fig. 2 below.

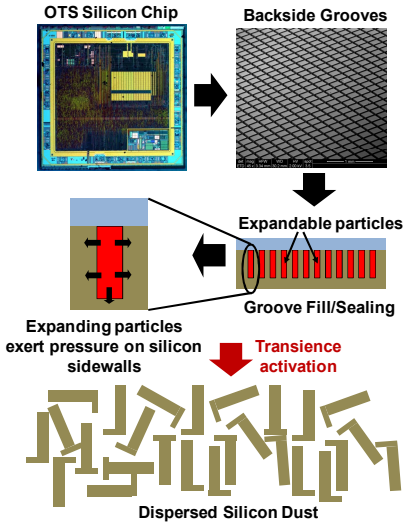

Figure 2: Schematic of the shatter-chip transience mechanism.

Each diced groove can be treated as a partial crack in the silicon substrate. In order to achieve transience the stress must be sufficiently high to propagate the crack to the top surface of the chip. The stress and pressure required to shatter the chip can be thus approximately calculated from fracture mechanics theory.

The Griffith fracture stress required for mode I (uniform stress) crack propagation as shown in Fig. 3 is

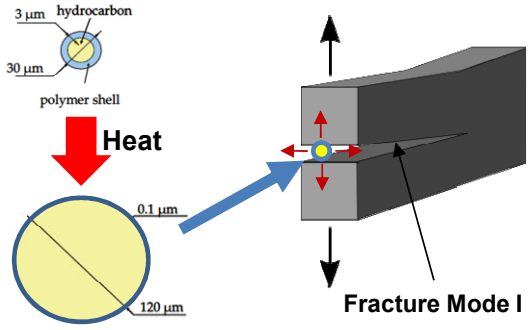

Figure 3: Large expansion of thermally expandable microspheres at elevated temperatures (130-160°C). The expanding microspheres produce a tensile stress that propagates a crack in the substrate causing chip fracture.

$$\sigma_f = (2E\gamma/\pi a)^{\frac{1}{2}} = K_{Ic}/\alpha\sqrt{\pi a} \qquad (1)$$

where E is the substrate Young's modulus, γ is the crystal free energy and a is the depth of the groove. The parameter K_{Ic} is the critical stress intensity factor or fracture toughness and α = 1 for edge cracks. For single-crystal silicon, K_{Ic} is typically 0.7-1.3 MPa $m^{0.5}$. A wedging force of 40N generated over a 5 mm long, 300 µm deep grooves corresponding to a uniform wedge pressure of 26 MPa is thus sufficient to cleave the silicon chip under mode I fracture.

3D Device simulation: The fracture stress calculated from Eq. (1) depends on the crack geometry and the energy release rate of the crack propagation. Bursting and cracking of silicon microstructures is well known to depend not only on the shape of the crack but also many unknown factors such as the roughness of the surfaces [8]. All of these factors produce fracture stresses much less than the silicon yield ~7 GPa. Because of these uncertainties simulations are unable to provide quantitative fracture stress information, but they can provide the most likely locations where cracks propagate. We have performed COMSOL device simulations to determine the locations of higher stress under constant internal pressure caused by the expanding material. Fig. 4 shows an example stress distribution at the bottom of the grooves. The highest stress

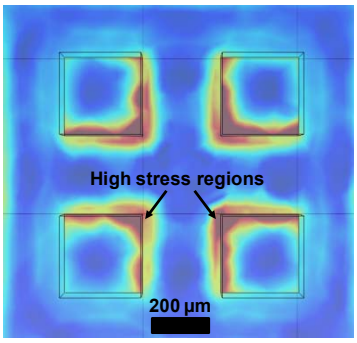

Figure 4: Normalized stress distribution at the bottom of the grooves. The points of highest stress are at the corner and edges of the grooves.

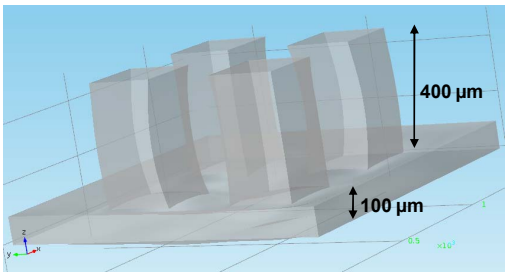

Figure 5: Example deformation of remaining silicon posts under uniform internal pressure and no pressure at the periphery.

occurs at the corners and along the edges. Fig. 5 shows qualitatively the deformation of the post structures and remaining silicon under internal pressure no side pressure. The deformation is consistent with a mode I fracture of a doubly supported beams. The actual type of fracture depends on the specific packaging scheme utilized.

Expanding actuating material: The expanding material used in our experiments consists of thermally expandable polymeric microspheres (Dualite U005-190D, Henkel) [9-17], 40 µm in diameter. These are polymeric core/shell particles in which a volatile hydrocarbon is encapsulated by a thermoplastic shell. When these microspheres are heated beyond a critical temperature (130-160°C) the hydrocarbon boils acting as a blowing agent and the pressure rises beyond the pressure required for plastic deformation of the shell. They thus expand and increase their volume dramatically expanding 60 times of their original volume. The volume increase is retained upon cooling thus leading to a density reduction from around 1100 kg m^{-3} to about 30 kg m^{-3}. The expanding particles thus create internal stresses and the crack wedging action inside the grooves.

Blowing agent pressure: Beyond the critical temperature the blowing agent is completely converted into a vapor; therefore we can estimate the pressure P_b exerted by the blowing agent pressure from its density and molecular weight.

$$P_b \approx \frac{k_B T \cdot N_b}{V_b} = \frac{k_B T \cdot \rho_l \cdot V_b \cdot G}{V_b\, m_w} = \frac{k_B T \cdot \rho_l \cdot G}{m_w} \qquad (2)$$

where N_b is the number of molecules of the blowing agent enclosed in the microparticle volume V_b and ρ_l and m_w are the liquid density and molecular weight of the blowing agent, respectively. G is Avogadro's number, T is the temperature, and k_B is Boltzmann's constant. Note that the maximum blowing agent pressure occurs when the blowing agent is instantaneously converted into a gas; hence Eq. (2) expression is independent of the volume of the microparticle. For a blowing agent such isopentane [15-16] with liquid density of ρ_l =626 kg/m^3, and molecular weight m_w=72.1 g/mole, at T=160°C, the blowing agent pressure is $P_b \approx$ 31 MPa. This is the maximum pressure available for stressing the microchip. The internal pressure varies between 20-30 MPa for common blowing agents. Experimentally it has been determined that stresses as high as 30 MPa are attained consistent with our simple estimate.

DEVICE FABRICATION

In order to convert a conventional silicon chip into a transient chip, first the chip backside is partially diced to form a network of narrow and closely spaced grooves. The dicing was done using Disco DAD 641 dicing machine with 250 µm thick diamond blades. The grooves were 250 µm wide and 400 µm deep spaced 250 µm apart. These grooves were then filled with the thermally expandable microspheres 40 µm in diameter and the excess particles were removed using a razor blade.

The chip backside is next attached to a pyrex glass cap with a room temperature adhesive thus sealing the filler material within the grooves. The seal assures that the filler particles do not force their way out of the grooves during expansion. Some of the chips were next packaged within a harness with the chips sandwiched between two aluminum plates tightly screwed together as shown in the schematic of Fig. 6. The harness ensures that the expanding

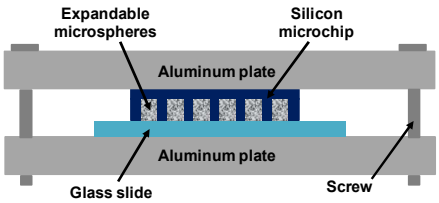

Figure 6: Schematic of packaging scheme and test fixture

microparticles exert pressure in all directions without delamination of the glass sealing cap. Tests were carried out on chips with and without the harness.

EXPERIMENTAL RESULTS

In order to test our concept, we incorporated the transience mechanism on a test off-the-shelf silicon microchip. The backside of the chip was diced into 250 µm wide deep grooves. Fig. 7(a) shows SEM pictures of the backside grooves. After dicing the grooves were filled with expandable microparticles up to the brim as shown in Fig. 7(b). Figs. 8(a) and (b) shows photographs of the backside

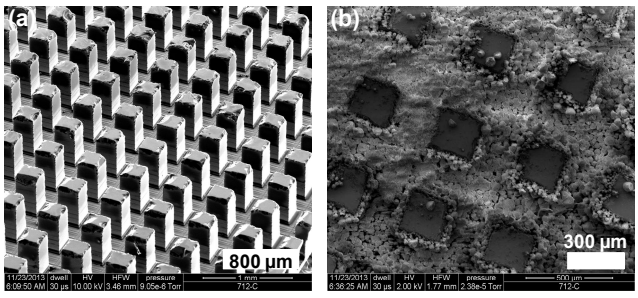

Figure 7: (a) SEM of dicing grooves on the chip backside. (b) SEM of grooves filled with thermally actuated microparticles.

of a chip backside after refill and under unconstrained expansion conditions at 160°C. Note that the microparticle volume increases greatly. A separate chip was next sealed with a glass cap and aluminum harness. The assembly was

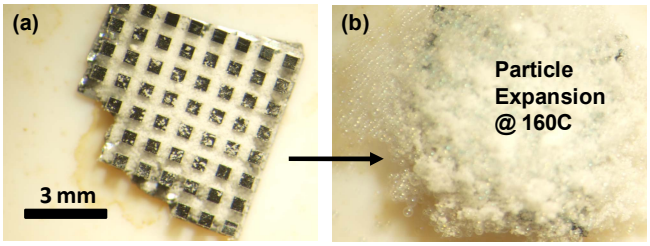

Figure 8: (a) Partially diced silicon chip with microparticle filled grooves. (b) Unconstrained expansion produces a 4-fold diameter expansion of the particles.

next placed on a heater at a temperature of 160°C. Within two minutes the polymeric microspheres start expanding rapidly and immediately fracture the whole microchip into small silicon pieces. Fig. 9 shows the typical results of constrained microparticle expansion for a chip with no harness. The chip is extensively fractured forming a three-dimensional heap of silicon dust and expanded particles. In

Figure 9: Chip transience is achieved via constrained expansion of the microparticles. The typical result is a heap consisting of a mixture of particles and silicon dust.

general the harness is not needed if the width of the grooves exceeds 200 µm.

Fig. 10 shows optical and SEM photographs of the chip before and after transience. The average distance between cracks is approximately the same as the groove pitch. The three dimensional nature of the heap facilitates the

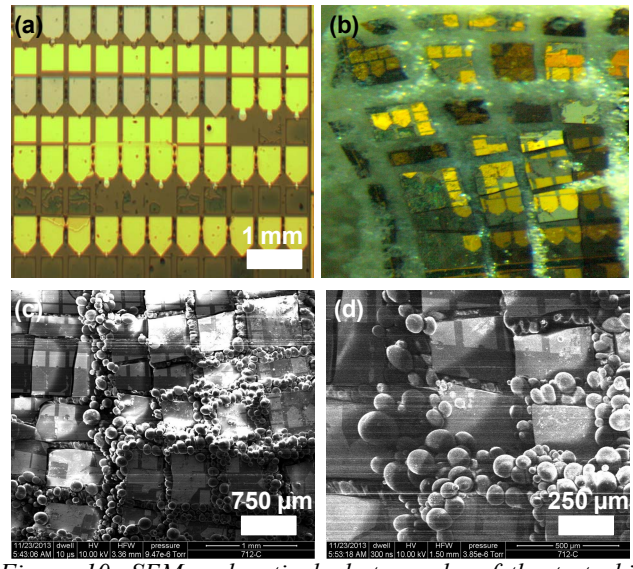

Figure 10: SEM and optical photographs of the test chip before and after transience showing chip shattering.

dispersion of the silicon dust to the surrounding environment. Experimentally we have tested several combinations of groove width and pitch ranging from 45-250 µm in width and 250-1000 µm pitch to produce the best results. In general we found that the shatter action is more effectively produced with wider grooves.

SUMMARY

This paper presents the successful implementation of a transience mechanism that can be incorporated in most microchips through low-temperature post processing. Chip transience is caused via the triggered expansion of thermally expanding microparticles stored within grooves formed on the backside of the chip. This transience mechanism does not utilize any corrosive agents or explosive substances therefore it produces transient chips that can be safely handled without any safety concerns. This transience method is modular and add-on thus it can be used to on-demand disable circuitry/sensors/chips serving diverse applications.

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REFERENCES

[1] G. Smolker, "Method and apparatus for protecting sensitive information contained in thin film microelectronic circuitry," United States Patent application number 425405, The United States of America as represented by the Secretary of the Navy, Washington, DC. May 1975.

[2] D. J. Shiel and D. L. Davis, "Method and appparatus for fast self-destruction of a CMOS integrated circuit," United States Patent application number 581436, Intel Corporation. Santa Clara. CA. April 1998

[3] F. Z. Keister and G. S. Smolker, "Single layer self-destruct circuit produced by co-deposition of Tungsten oxide and Aluminium," United States Patent application number 90204, The United States of America as represented by the Secretary of the Navy, Washington, DC. June 1973.

[4] S. Pandey and C. H. Mastrangelo, "An exothermal energy release layer for microchip transience," *Proc. IEEE Sensors Conf.*, Baltimore, Md, Nov. 3-6, 2013, pp. 1759-1762.

[5] S-W. Hwang et al. "A physically transient form of silicon electronics", *Science*, 337, 1640 (2012).

[6] N. Banerjee, Y. Xie, H. Kim and C. H. Mastrangelo, "Microfluidic device for triggered chip transience," *Proc. IEEE Sensors Conf.*, Baltimore, Md, Nov. 3-6, 2013, pp. 920-923.

[7] X. Gu, X. Lou, R. Song, Y. Zhao and L. Zhang, "Simulation research on a novel microfluidic self-destruct device for chips", *IEEE Nano/Micro Engineered and Molecular Systems*, pp 373-378, Xiamen, China, 2010.

[8] A. K. Henning, S. Patel, M. Selser and B. A. Cozad, "Factors affecting silicon membrane burst strength," in Reliability, Testing, and Characterization of MEMS/MOEMS III, edited by Danelle M. Tanner, Rajeshuni Ramesham, *Proceedings of SPIE* Vol. 5343 (SPIE, Bellingham, WA, 2004), pp. 145-153.

[9] Henkel microspheres home page: www.henkelna.com.

[10] Morehouse, D. S. J.; Tetreault, R. J. U.S. Pat. 3,615,972, 1964.

[11] J. Lundqvist, Eur. Pat. 0 486 080 B1, 1992.

[12] T. Yokomizo, K. Tanaka, K. Niinuma, Jpn. Pat. 9019635, 1997.

[13] M. Jonsson, O. Nordin, A. Larsson Kron, and E. Malmström, "Thermally expandable microspheres with excellent expansion characteristics at high temperature", *J. Applied Polymer Science,* 2010, 117, 384-392.

[14] M. Jonsson, O. Nordin, E. Malmström and C. Hammer, "Suspension polymerization of thermally expandable core/shell particles", *Polymer* 2006, 47, 3315-3324

[15] J. Fredlund, *Synthesis of Thermo Expandable Microspheres*, MSc Thesis, KTH Sundsvall, Sweden, 2011.

[16] J. Magnus, *Thermally Expandable Microspheres Prepared via Suspension Polymerization - Synthesis, Characterization, and Application,* PhD Thesis, KTH Stockholm, Sweden, 2010.

[17] Masayasu Fujino, Takashi Taniguchi, Yasuhiro Kawaguchi, Masahiro Ohshima, "Mathematical models and numerical simulations of a thermally expandable microballoon for plastic foaming," *Chemical Engineering Science*, Volume 104, 18 Dec. 2013, pp. 220-227.

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