TRANSMISSION LINES ON INTEGRATED CIRCUITS FOR HIGH SPEED COMMUNICATION

by

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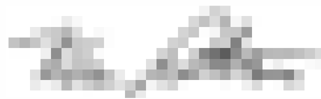

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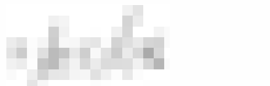

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ABSTRACT

As microelectronics continue to scale, the transistor delay decreases while the wire delay remains relatively constant or even increases. The wire or interconnect delay is quickly becoming the key performance limiting factor in integrated circuit design. This thesis is designed to determine the feasibility of replacing conventional diffusive wires with transmission lines and to compare the tradeoffs of the two systems. The transmission lines propagate signals at the speed of light in the medium and are much less dependent on repeaters than comparable diffusive wires. Therefore, the transmission line system has potentially large power and performance benefits. To compare the tradeoffs, five important design metrics are used: propagation delay, power consumption, maximum throughput, area requirements, and noise tolerance. The transmission lines prove to be an excellent replacement for diffusive wires especially as the length passes 500 μm. For a 1 cm interconnect, the transmission line shows more than a 90% improvement in delay and more than an 80% improvement in energy per bit transmitted. In practice, fabricating transmission lines on real integrated circuits is a difficult process because they require precise resistance, inductance, and capacitance parameter extraction. Using tools specially developed by Mentor Graphics for this thesis, the necessary wire dimensions to produce various transmission lines are calculated for in IBM's 65 nm process.

A la memoire de mes grandpères

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CHAPTER 1

MOTIVATION

Current microelectronics design and fabrication are two of the greatest feats of technology and science in recorded history. A pioneer in the field, Gordon Moore predicted as early as 1965 that the total number of transistors in an integrated circuit (IC) will double every year [1]. Ten years later while serving on the board of Intel, he modified this number to doubling every two years. The idea, later termed Moore's Law, became a self-fulfilling prophecy for semiconductor design houses. Industry began to make their future designs to follow this law. Initially assumed to last for approximately 10 years, Moore's Law has been correctly determining the path for semiconductor scaling for nearly 40 years, as seen in Figure 1.1.

The speed of these processors has been doubling every generation due to significant decreases in transistor delay. In synchronous digital design, the clock controls the speed of the IC. Two components, wire delay and transistor delay, dictate the minimum period of the clock. The transistor transit time, τ, is given by [2]

$$\tau = \frac{L^2}{\mu(V_{GS} - V_T}) \tag{1.1}$$

where L is the channel length, μ is the electron mobility, V_{GS} is the gate-to-source voltage, and V_T is the threshold voltage for the MOSFET. According to constant field scaling (all dimensions and applied voltages are multiplied by $s = 0.7$), the transit time also scales by s. This transit time is the minimum time required for a charge placed on the gate to result in a transfer of a charge through the channel onto the gate of another transistor and has historically been a figure of merit in semiconductor performance [2].

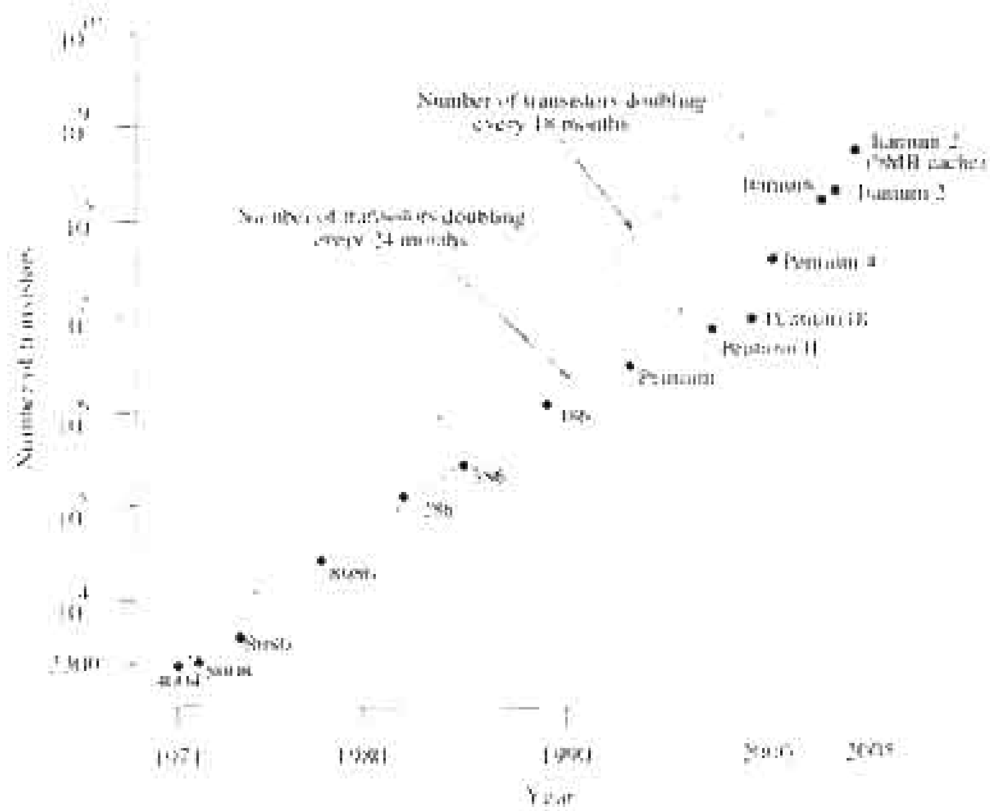

Figure 1.1 Moore's Law - Processor transistor count [2] Reprinted by permission of Escovar, R. (2006). *Tools for Impedance Extraction in Integrated Circuits (IC)*. Doctoral dissertation, Universite Joseph Fourier, Grenoble, France.

Although transistor delay decreased exponentially, the wire delay decreased at a much slower rate. Wire delay is proportional to the resistance and capacitance of the wire. According to simple first order models, the wire's resistance and capacitance are

$$R = \frac{\rho L}{wt} \tag{1.2}$$

and

$$C = \frac{\epsilon A}{d} \tag{1.3}$$

where L, w, t, and ρ are the wire's length, width, thickness, and resistivity, respectively. ϵ is the relative dielectric permittivity of the media, d is the distance to the next conductor, and A is the area of the metal facing the nearest conductor. These equations give the resistance of a rectangular wire and the capacitance of a wire modeled as two parallel plates. The wire delay is the product of these two equations. As semiconductors scale, all the physical dimensions scale. The material properties, however, do not scale; occasionally, they are replaced by new materials that make small improvements. Overall, the physical dimension scaling dominates the time constant for the interconnects.

Assuming that these parameters remain constant, the R scales by $1/s$ and C scales as s according to constant field scaling. Therefore, the wire delay remains constant. In order to better scale the wire delay, manufacturers do not scale the wires uniformly: the thickness scales much more slowly than the other dimensions in order to decrease the resistance. This phenomenon is shown in Figure 1.2. The cross section shows that the upper metal layers remain thicker than the lower layers to reduce the wire resistance. Copper replaced aluminum wires to decrease resistivity, and new insulators are used to decrease the capacitance. With all of these innovative solutions, the wire delay still does not scale very well.

As technology scales from the 250 nm node to the 32 nm node, the gate delay decreases over 80%, as seen in Figure 1.3. The delay of a global wire with repeaters

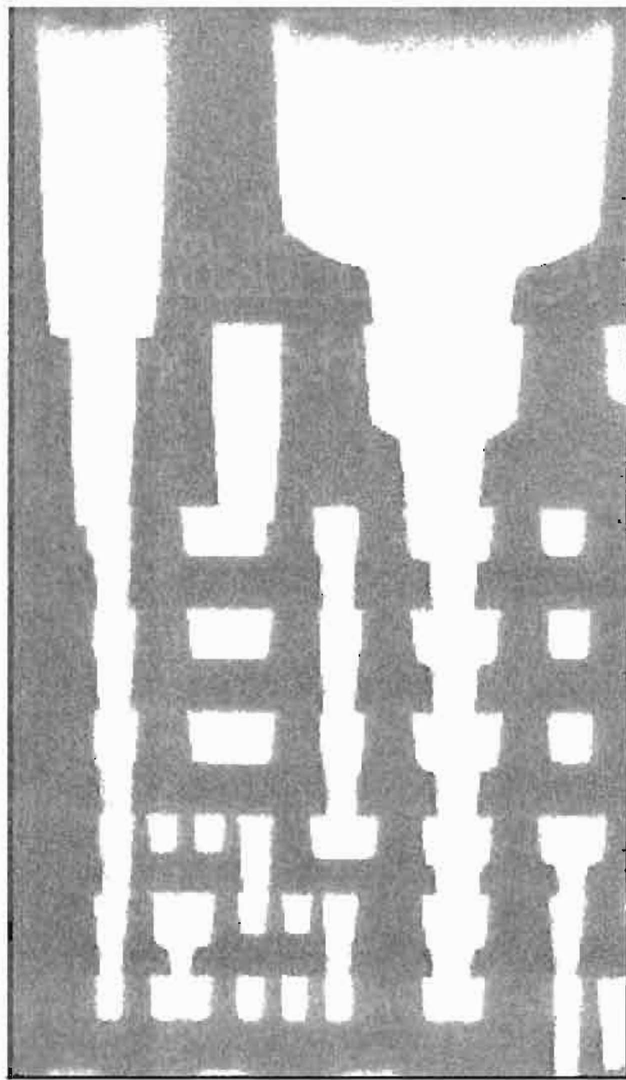

Figure 1.2. Cross section of various metal layers for Intel 65 nm process [3] ©2005 IEEE

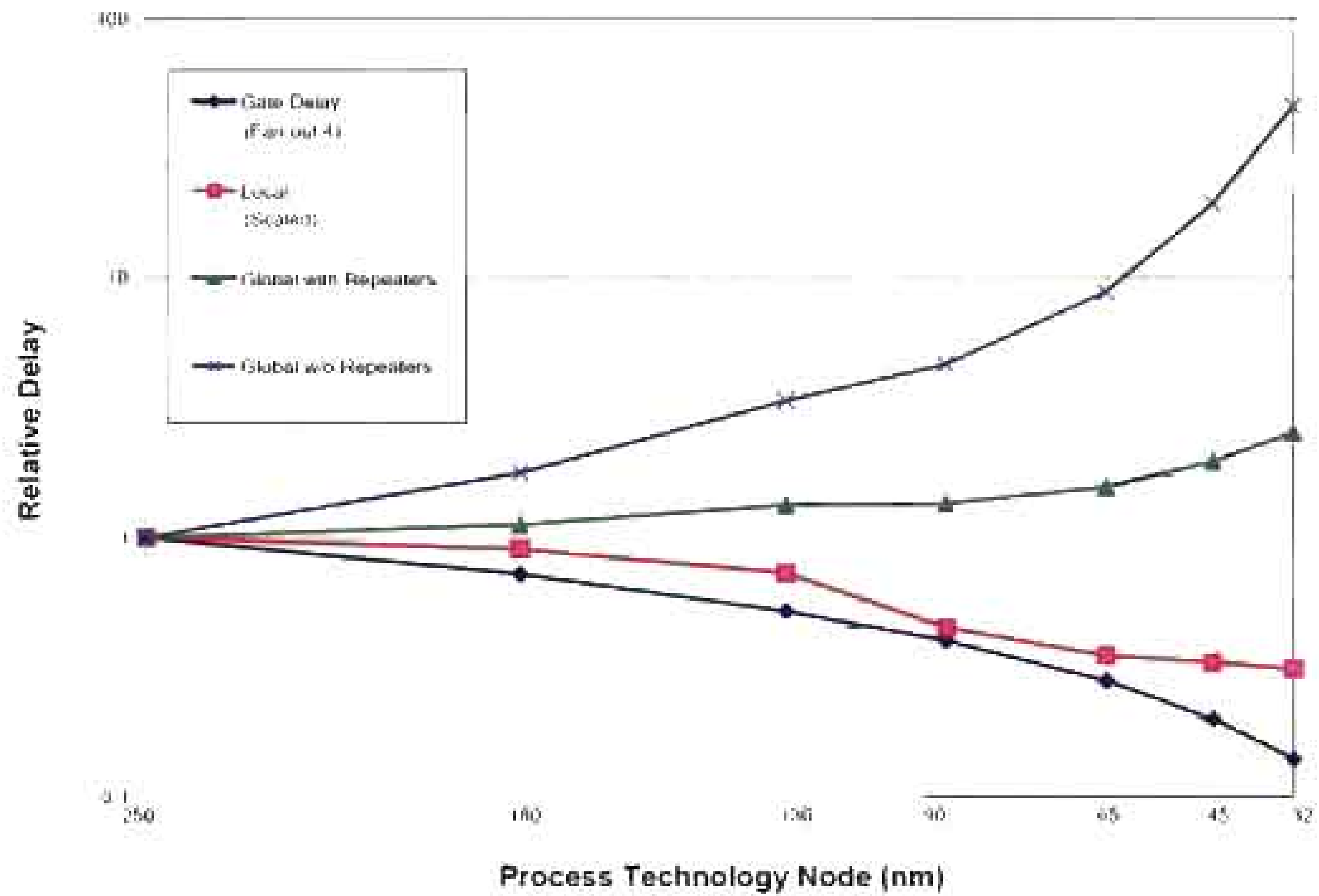

Figure 1.3. Delay for metal 1 and global wires versus feature size [4]©2005 ITRS

more than doubles, and the delay of global wire without repeaters increases by more than a factor of 50. Although Figure 1.3 shows relative numbers, Table 1.1 shows some absolute numbers for these technology nodes. Combining both sets of information gives a clear picture of the growing interconnect crisis.

Furthermore, as semiconductor technology continues to scale, a larger percentage of nets will require repeaters. If current trends continue, then most of the available cells in a circuit block will be repeaters. At the 90 nm node, roughly 6% of the cells are repeaters [6]. On the other hand, at the 32 nm node, 70% of the cells will be repeaters, as shown in Figure 1.4 [6], if current trends continue. Current wire scaling trends will not be able to meet the demands of future process nodes due to excessive power consumption and layout area. Other solutions are necessary as wire delay becomes the critical performance limiting factor.

Table 1.1. Delays for intrinsic devices and wires for various process nodes (adapted from [5]).

Tech. Node[nm]	250	180	150	130	100	70
Device intrinsic delay[ps]	70.5	51.1	48.7	45.8	39.2	21.9
1mm wire[ps]	59	49	51	44	52	42
2cm unoptimized[ps]	2080	1970	2060	2070	2890	3520
2cm optimized[ps]	890	790	770	700	770	670
Projected clock period[ps]	1333	833	714	625	500	400

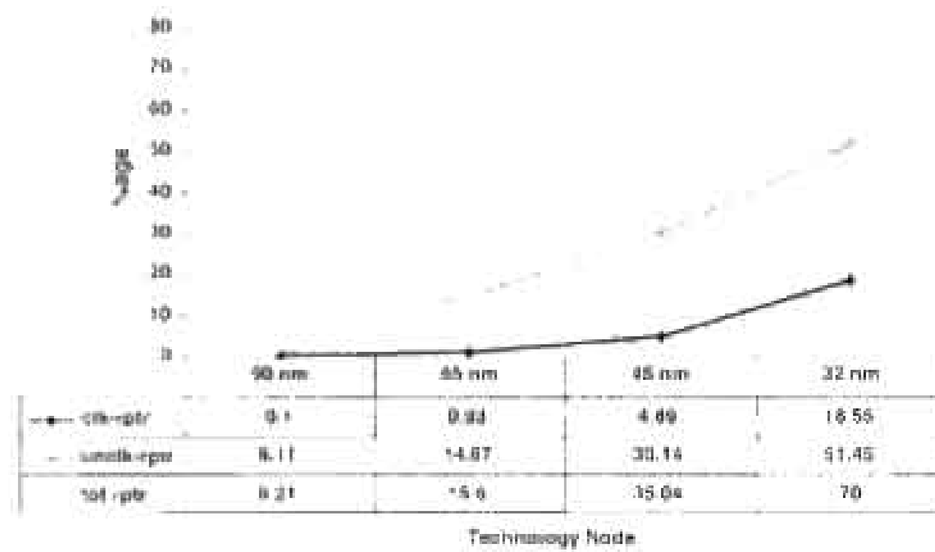

Figure 1.4 Intrablock communication repeaters as a percentage of the total cell count [illegible]

CHAPTER 2

INTRODUCTION

Current publications show a plethora of approaches to solve the interconnect problem, including the use of optics, radio frequency (RF) transmission, carbon nanotubes, and transmission lines. Each has unique advantages and disadvantages.

2.1 Optical Interconnects

Optical transmission is one solution that promises very high speed wave propagation for longer wires. The propagation delay of optical interconnects (OIs) are over 50% less than electrical interconnect systems [7]. Unfortunately, OIs require additional complex transmitter and receiver circuitry that add a fixed amount of delay regardless of the interconnect length. Without faster transmitters and receivers, only very long wires over 1 cm long have less delay than electrical interconnects [7]. Furthermore, building all the necessary optical devices (e.g., laser source, quantum well modulators, and photo detectors) on silicon is very costly and difficult. Many of these devices do not perform well and have a very large footprint [8].

OIs usually require off-chip laser sources due to the poor light emitting properties of silicon. As these devices improve, OIs will outperform electrical interconnects over 1 cm long [8]. In addition to a delay penalty due to the extra circuitry, a power penalty is associated with any optical interconnect that eliminates the power savings of using less repeaters; there is a critical length of 18 cm to 20 cm depending on the process node where the OIs consume less power than electrical interconnects, as shown in Figure 2.1 [9]. For higher required bit rates, the critical length decreases. Therefore, optical interconnects will have a smaller delay and consume less power

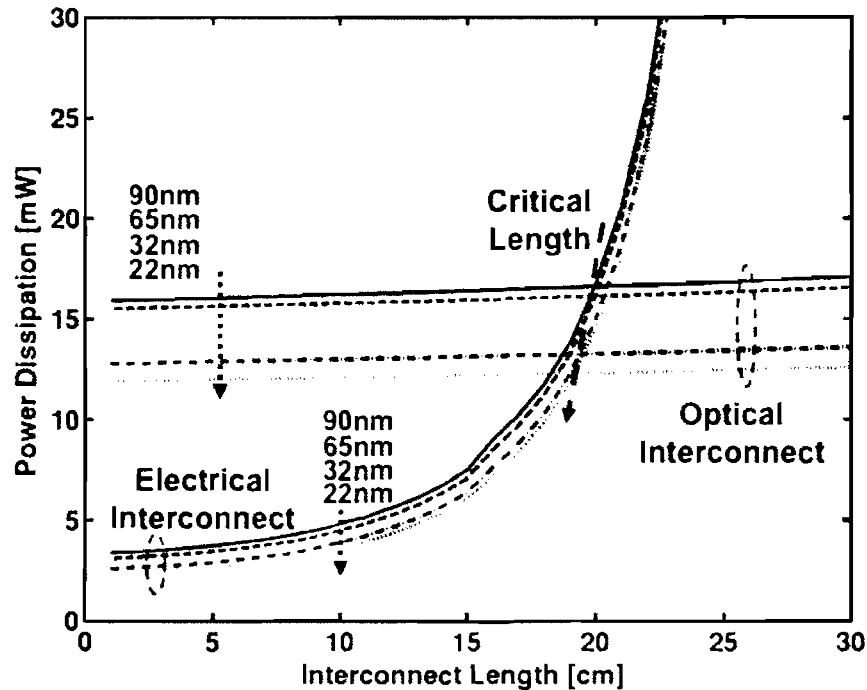

Figure 2.1. Power dissipation vs. interconnect length (optical and electrical interconnects) for a 30 Gb/s required bit rate and a detector capacitance of 25 fF [9] ©2005 IEEE

than electrical interconnects for very long wires (over 10 cm) and may be a viable solution to interchip communication.

2.2 Radio Frequency (RF) Interconnects

Utilizing recent developments in wireless communications, an alternative interconnect approach is an RF interconnect (RFI). RFIs use various algorithms to encode and transmit data. One such implementation using code division multiple access (CDMA) transmitted data at the rate of 100 Gbps/pin [10]. Similar to OIs, RFIs require a large amount of overhead to implement any RFI independent of the interconnect length. This circuitry includes analog components that require large amounts of area that do not scale well in future process nodes. If the RFI is not wireless, then carefully designed transmission lines or wave guides are necessary to maintain signal integrity while sending these high frequency signals. If the

interconnect is wireless, area intensive antennas must also be built. Furthermore, wireless communication is more likely to be affected by noise than other interconnect schemes. The overhead adds power and delay to any RFI interconnect. Figure 2.2 shows the measured and predicted power consumption of the transceiver pairs for various process nodes. A comparison of Figure 2.1 and 2.2 shows that the RFIs require less power than the OIs as technology scales. At the 32 nm node, both of these interconnects, however, only consume less power than electrical interconnects at lengths over 10 cm. Therefore, RFIs are an excellent option for transmitting large amounts of data between different circuits. For point to point communication, however, it is not a good option except for very long distances.

2.3 Carbon Nanotube Interconnects

A more exotic interconnect implementation is the use of carbon nanotubes (CNT). Unlike OIs and RFIs, the CNT interconnects do not require special transceivers for sending and receiving data. Although a single CNT has a high resistance, a bundle of CNTs has much lower resistance than copper wires assuming low resistance contacts [12]. Unfortunately, a bundle of CNTs has a higher capacitance than copper wires due to the multiple conductors in close proximity. Each carbon

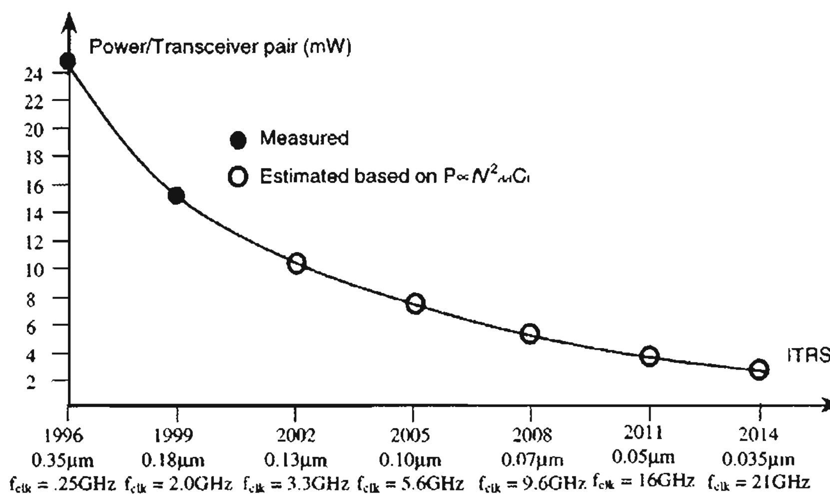

Figure 2.2. RF transceiver-pair power consumption [11] ©2001 IEEE

nanotube is capacitively coupled to the surrounding tubes, which makes the delay of CNT local wires greater than copper local wires. Intermediate and global wires are faster than copper wires, as shown in Figure 2.3. The performance benefits of CNT compared to copper wires at the 45 nm will be negligible but may be 80% faster at the 22 nm node [13]. This requires a high bundle density, a ground plane beneath the bundle to reduce capacitance, and perfect contacts for all of the CNTs. Bundles that would be useful for interconnects require a much higher CNT density than has been currently produced [12]. a bundle needs approximately 10^6 CNTs/μm^2 whereas current research has only produced less than 100 CNTs/ μm^2 [14]. CNT technology is still a very nascent field that does not have the yield necessary for commercial integrated circuit fabrication.

2.4 Transmission Line Interconnects

Transmission lines (TLs) are a very attractive solution to the interconnect problem for intrachip communication. The TLs can be implemented by placing two coplanar wires next to each other, which makes them easy to implement in any semiconductor process. Through numerous computer simulations, studies show that coplanar TLs can propagate signals near the speed of light in silicon dioxide (1/2 the speed of light in a vacumn) if designed properly [2]. Additionally, due to the low loss nature of TLs, they consume far less energy per bit, especially

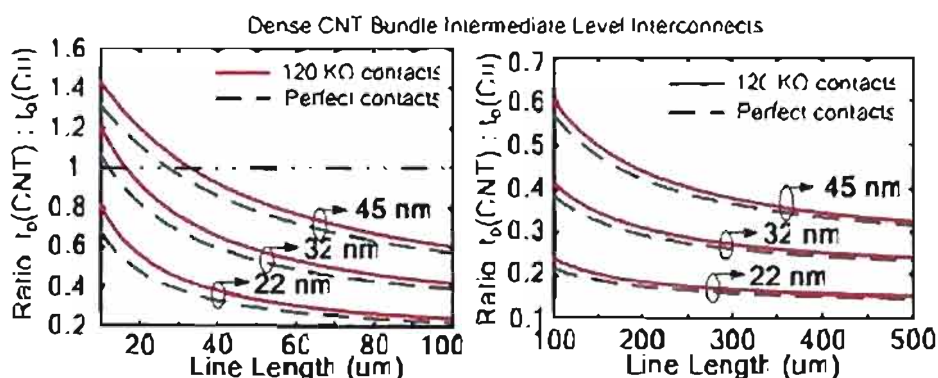

Figure 2.3. CNT interconnect delay compared to copper wire delay [12] ©2005 IEEE

as semiconductors continue to scale [15]. Figure 2.4 compares the energy per bit consumption of transmission lines (DTL) with other interconnect implementations such as conventional optimized wires (RC), optics (OPT), and carbon nanotubes (CNT). The number indicates the process node (e.g., RC90 indicates the 90 nm node for an optimized wire). The transmission lines are a very energy efficient solution.

Additionally, the delay for the transmission lines is very competitive with the other interconnects, as shown in Figure 2.5 [15]. A very exciting future solution may be transmission lines built from carbon nanotubes; the carbon nanotube transmission lines would be a fraction of the size of their metal counterparts.

Therefore, the TLs can propagate signals at very high speeds for a small amount of energy and can be designed for any semiconductor process by the designer; it does not require any process changes. The main negative tradeoffs of TLs consist of an area and a noise penalty. The TLs require three relatively wide wires to run in parallel, which requires more area in the routing metal layers. Minimum pitch wires are not a viable option due to their increased susceptibility to variation.

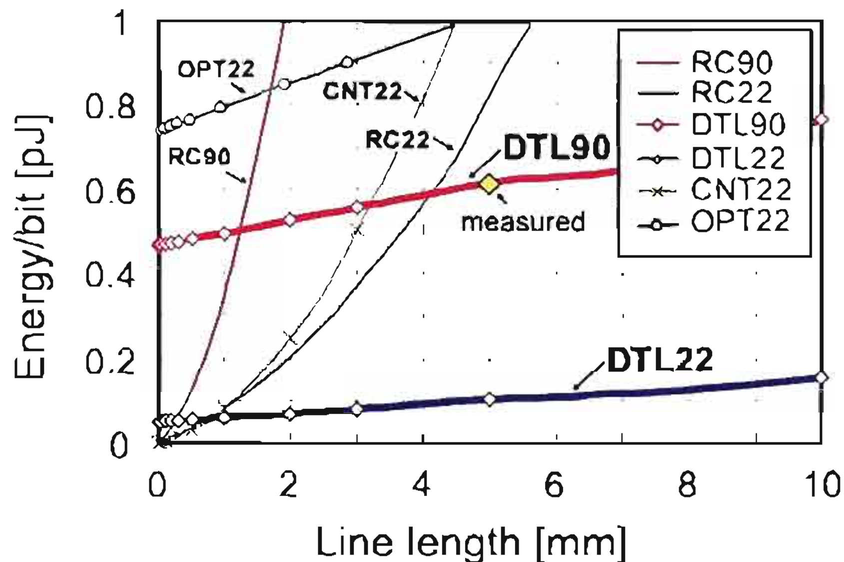

Figure 2.4. Energy comparison of various interconnect implementations [15] ©2006 IEEE

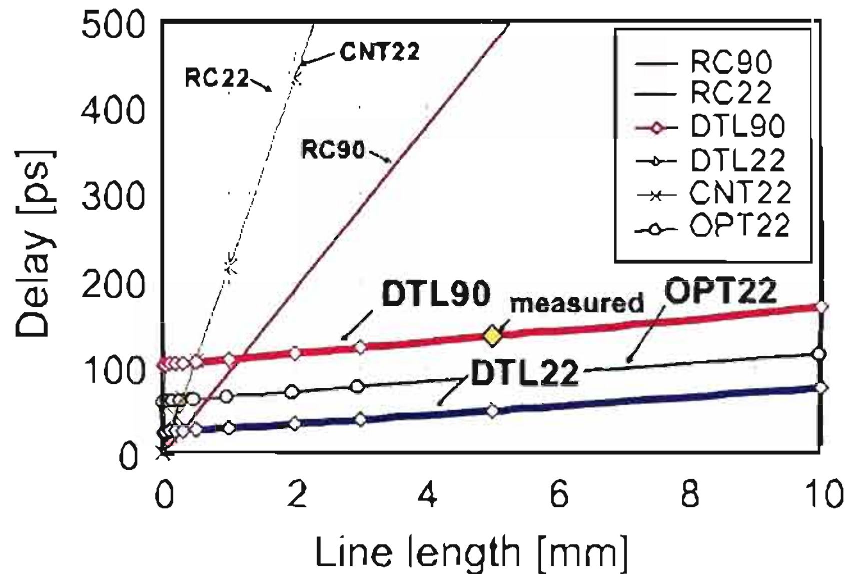

Figure 2.5. Delay comparison of various interconnect implementations [15] ©2006 IEEE

This makes it much more difficult to precisely control the characteristic impedance. Since they require fewer repeaters, however, less silicon and contact routing space are required.

Due to their inductive properties, TLs are much more susceptible to noise than other implementations due to reflections. TLs rely on changing magnetic and electric fields to propagate a signal. The signal integrity is not only dependent on the conductor properties but is also very dependent on the conductor geometry and insulator properties. Every time one of these changes (e.g., the driver connects to transmission line, the transmission line forks, or the transmission line connects to the receiver), the impedance can potentially change, which leads to reflections. The reflections can be mitigated by designing matched impedance drivers and designing receivers with hysteresis. Matched drivers reduce the amplitude of the noise, and the hysteretic receivers prevent the system from responding to the noise. Furthermore, using modern circuit parameter extraction programs such as Calibre from Mentor Graphics, the inductance effects can be accurately modeled well before fabrication.

Although each interconnect implementation has a unique set of advantages and disadvantages, transmission lines are potentially best suited to transmit signals for long intermediate and global wires on a single IC. As the wire becomes very long for interchip communication, then other solutions such as wireless RF and optical transmission become better options. Future high performance ICs will require different interconnects for different lengths of wire: conventional metal wires for local interconnect, transmission lines for intermediate and global wires, and RF or optical transmission for very long global wires and interchip communication. This thesis is designed to investigate and quantify the advantages of transmission lines over diffusive wires with optimally spaced repeaters for intermediate and global wires.

2.5 IBM 65 nm Process Parameters

Another goal of this thesis is to provide the necessary framework and preparations to build a test chip to compare the benefits and tradeoffs of transmission lines and diffusive wires. In order to observe the transmission line benefits, the test chip must be built in the most modern process available, as explained in Chapter 1. The best process available through MOSIS is the IBM CMOS10SF process. This corresponds to 50 nm physical gate lengths and 100 nm minimum transistor widths [16] and will be referred in this study as the 65 nm process based on the printed gate length. The 2007 ITRS report explains that there are currently "multiple drivers of scaling" and that it is misleading to refer to a node by a single highlighted driver [17]. Memory devices such as DRAM are pushed by the minimum metal pitch whereas MPUs and ASICs are pushed by the minimum poly pitch, as seen in Figure 2.6. Many of the models in the thesis rely on various process parameters. These are placed in Table 2.1 as a reference for the rest of the report. Different combinations of these layers are available to the designer depending on which metalization option is selected.

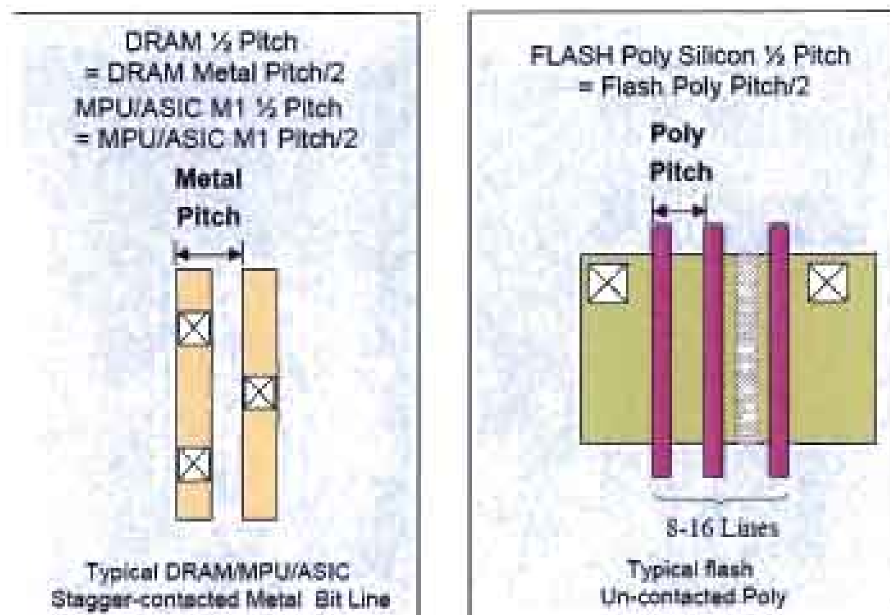

Figure 2.6. ITRS definition of pitches [17] ©2007 ITRS

Table 2.1. CMOS 10SF IBM process parameters (adapted from [16])

Layer Name	Min. Width [μm]	Min Spacing [μm]	Thickness [μm]	Notes
M1	0.09	0.09	0.135	
M2-6	0.10	0.10	0.175	
B1-4	0.20	0.20	0.350	2x thickness in low-k dielectric
BA,BB,BD-BG	0.20	0.20	0.350	2x thickness in TEOS/FTEOS dielectric
EA, EB	0.40	0.40	0.570	4x thickness in TEOS/FTEOS dielectric
LB	2.40	1.40	1.325	required top aluminum layer

CHAPTER 3

DIFFUSIVE WIRE MODELING AND SIMULATION

Conventional wires with optimally spaced repeaters were modeled and used as the reference point since the majority of IC designers currently use them. For this wire optimization scheme, long wires are divided into segments of length h. Repeaters that are k times the size of a minimum sized inverter are placed between the wire segments, as shown in Figure 3.1. The necessary parameters for the simulation were based on a study that derived circuit parameters for various process nodes [18] using the 2001 ITRS report. Ideally, the 2007 ITRS report would have been used, but this would have required repeating the simulations in the study.

According to the derivation [18], the delay per unit length is optimized when the distance between repeaters, h_{opt}, and the sizing, k_{opt}, are

$$h_{opt} = \sqrt{\frac{2r_s(c_o + c_p)}{rc}} \tag{3.1}$$

$$k_{opt} = \sqrt{\frac{r_s c}{r c_o}} \tag{3.2}$$

where r_s is the output resistance, c_o is the input capacitance, and c_p is the output parasitic capacitance of a minimum sized repeater (i.e., k =1). The remaining pa-

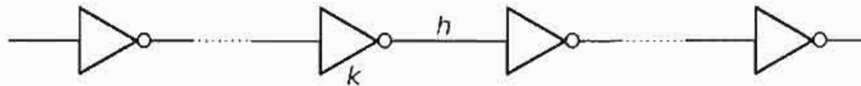

Figure 3.1. Diffusive wire repeater spacing, h, and sizing, k

rameters, r and c, are the resistance and capacitance per unit length of interconnect, respectively.

3.1 Minimum Width Wires

The resistance per unit length was found by dividing equation (1.2) by the length, L. Finding the capacitance per unit length was more complex. The model assumes that there are two contributions to capacitance for each metal wire. First, each conducting wire is capacitively coupled with the nearest conductor: this contribution is given by c_a. Secondly, there is a capacitance between the metal wire and the surrounding metal layers which is proportional to the insulator thickness, t_{ins}. This capacitance is found by multiplying t_{ins} and c_b. Assuming dense routing, Table 3.1 gives the value of these parameters that were found by using a FASTCAP [19] parameter extraction program. Therefore, the capacitance per unit length is equal to

$$c = c_a + c_b t_{ins} \tag{3.3}$$

The optimal repeater spacing and sizing were determined for various process nodes using equations (3.1), (3.2), (3.3), and Table 3.1. Table 3.1 shows the various values used. Table 3.2 shows the results calculated with Matlab. Note that the resistance rises dramatically due to wire scaling. The capacitance remains relatively constant. The nearest conductor contribution decreases: the product of the insulator permittivity and wire thickness scaling factors are less than the wire spacing scaling factor. The conductor-to-next layer capacitance increases because the distance from the conductor to the substrate is scaled more aggressively than the wire dimensions and dielectric constant of the insulator. These factors cancel each other out. Table 3.2 also confirms that the number of necessary repeaters is increasing rapidly, as shown by Saxena [6]. These parameters were used in the Spice simulations for the diffusive wire.

Table 3.1. Circuit parameters for top metal layers based on 2001 ITRS report [18]

Tech. Node[nm]	130	90	65	45
Width[nm]	335	230	145	103
Thickness[nm]	670	482	319	236
$t_{ins}[\mu m]$	6.3	4.7	3.9	2.9
ϵ_r	3.3	2.8	2.5	2.1
c_a[fF/mm]	207	181	165	143
$c_b[fF/\mu m^2]$	0.057	0.071	0.103	0.116
$r_s[k\Omega]$	6.23	9.04	9.6	13.2
c_o[fF]	1.33	1.1	1.03	0.9
c_p[fF]	3.32	2.04	1.22	0.6

Table 3.2. Interconnect parameters for top layer metal [min. pitch wires] (calculated using Matlab)

Tech. Node[nm]	130	90	65	45
$r[m\Omega/\mu m]$	76.6	155.2	371.9	707.6
$c[fF/\mu m]$	0.566	0.515	0.566	0.479
$h_{opt}[\mu m]$	1156	843	453	342
k_{opt}	186	165	119	99.7

The repeater spacing, h_{opt}, for the 65 nm node wires is 453 μm, as shown in Table 3.2. In VLSI design, the repeaters can not always be placed at the exact desired locations due to other design constraints. Similarly, for the simulations done here, the repeaters were placed every 500 μm. The result is a nearly optimal diffusive wire: it will have slightly more delay but less power consumption. Nalamalpu shows that a single repeater placed 40% away from the optimal location causes up to a 7% increase in delay in a 130 nm process [20]. The repeaters consist of inverters that are k_{opt} times the size of a minimum inverter. Figure 3.2 shows the outputs for diffusive wires constructed in this manner of lengths 2500 μm, 5000 μm, and 10000μm. The state of the output (inverted or noninverted) depend on whether or not an odd or even number of repeaters were placed on the wire.

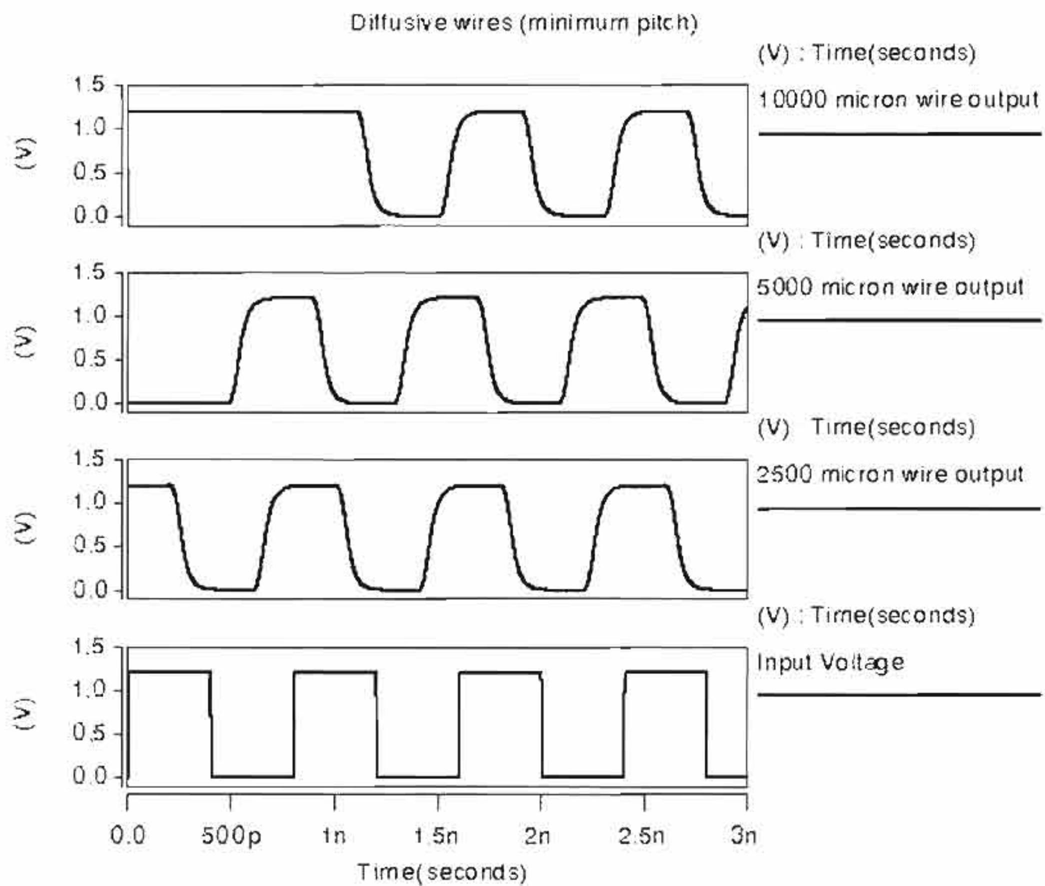

Figure 3.2. Diffusive wire output (using minimum pitch wires and IBM 65nm Spice models)

3.2 Diffusive Wire Results: Latency and Power

Figures 3.3 to 3.12 show the power consumption (Figure 3.3 and Figure 3.4), rise times (Figure 3.5), fall times (Figure 3.6), propagation delays (Figure 3.7, Figure 3.8, Figure 3.9. and Figure 3.10), and the maximum bandwidth (Figure 3.11 and Figure 3.12) for minimum pitch wires in the top metal layer. The frequency for all the simulations was one gigahertz except for the maximum bandwidth simulations. The bandwidth was measured by increasing the input frequency until the output did not swing between 10% and 90% V_{DD}.

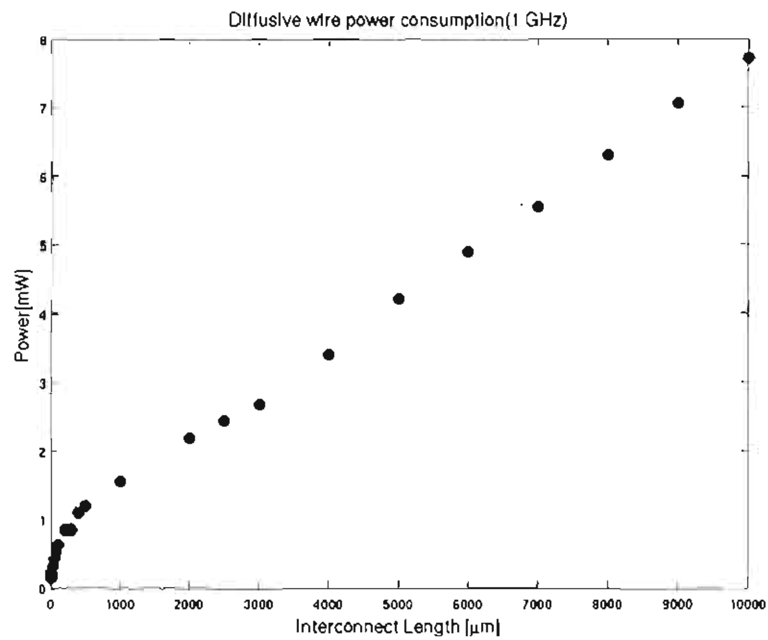

Figure 3.3. Diffusive wire power consumption (dynamic - 1 GHz)

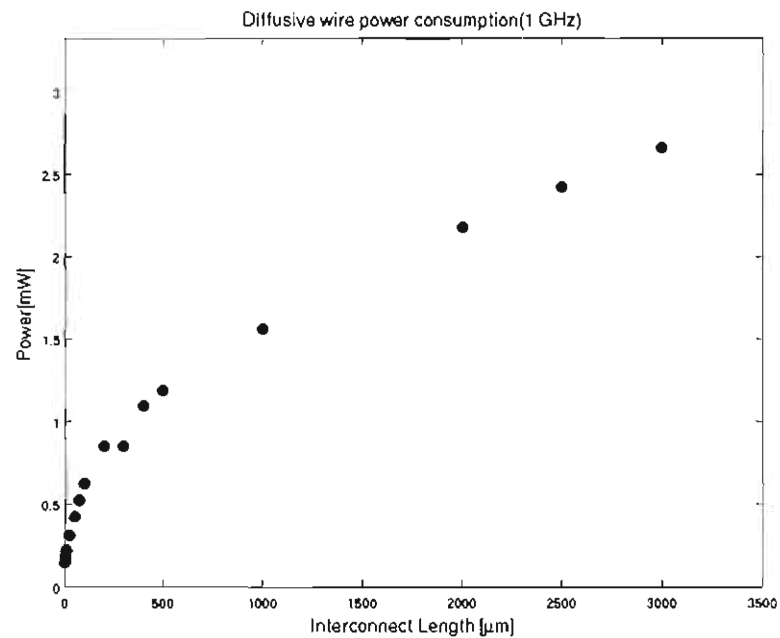

Figure 3.4. Diffusive wire power consumption (short interconnects) (dynamic - 1 GHz)

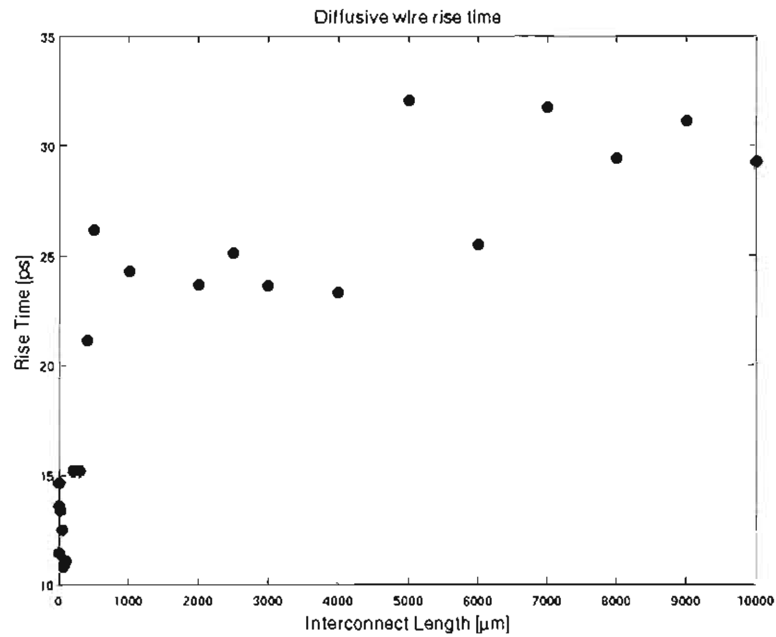

Figure 3.5. Diffusive wire rise times (1 GHz)

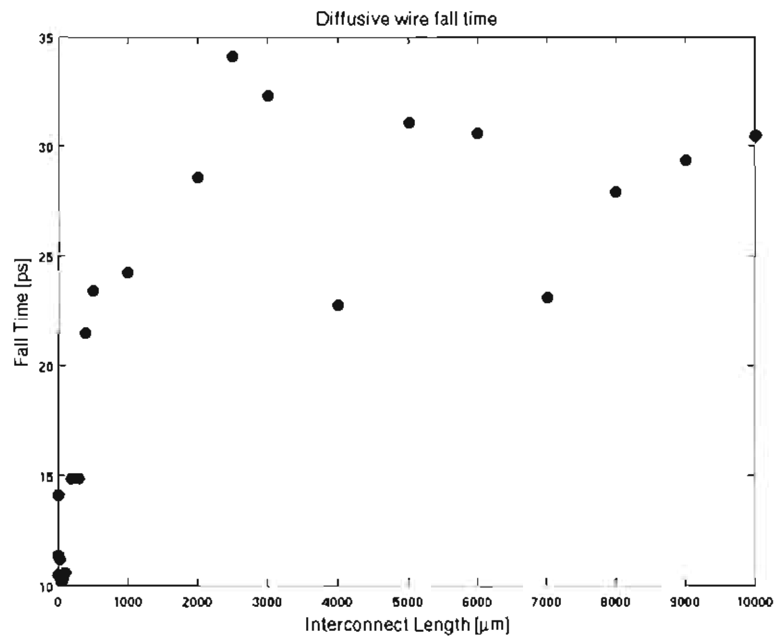

Figure 3.6. Diffusive wire fall times (1 GHz)

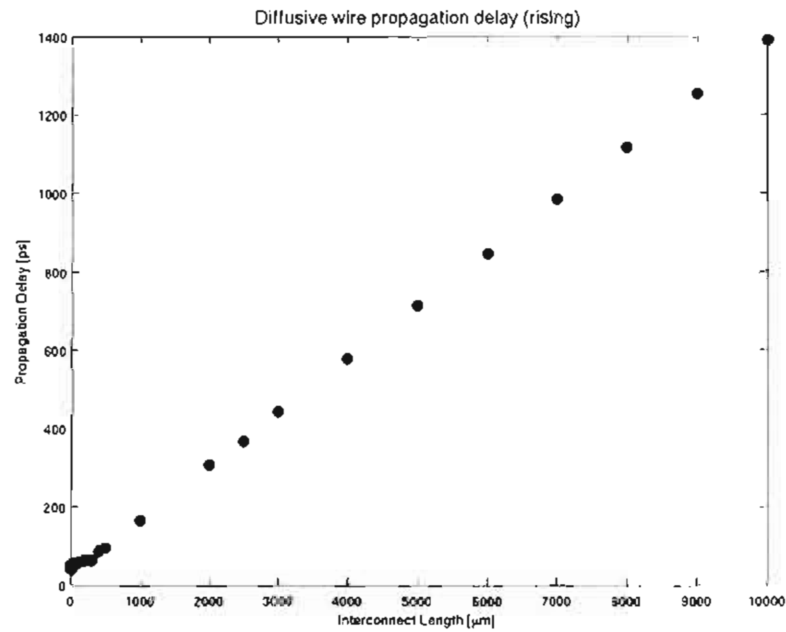

Figure 3.7. Diffusive wire propagation delays (rising) (1 GHz)

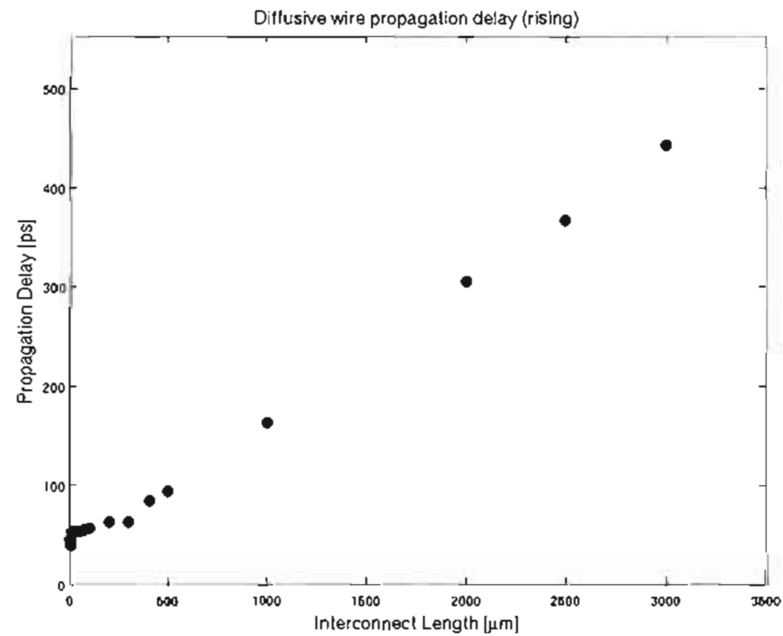

Figure 3.8. Diffusive wire propagation delays (rising) (short interconnects) (1 GHz)

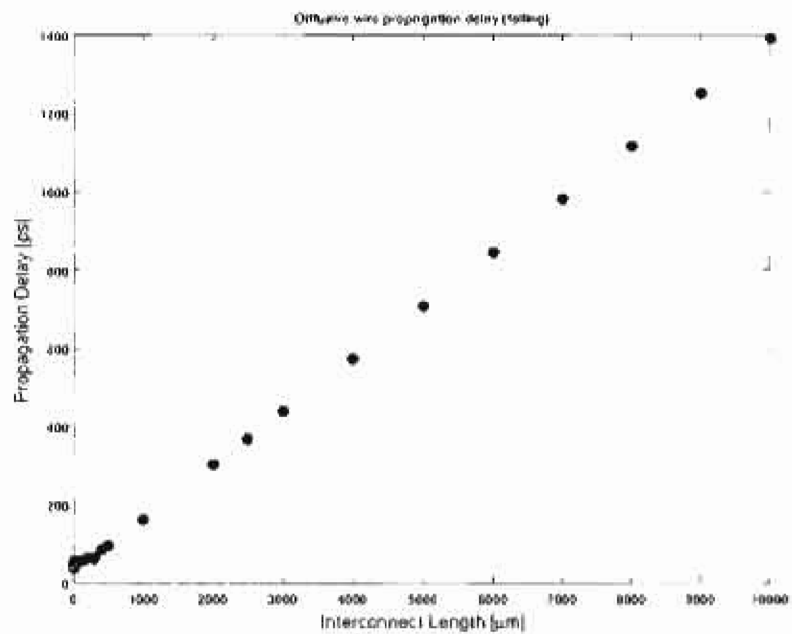

Figure 3.9. Diffusive wire propagation delays (falling) (1 GHz)

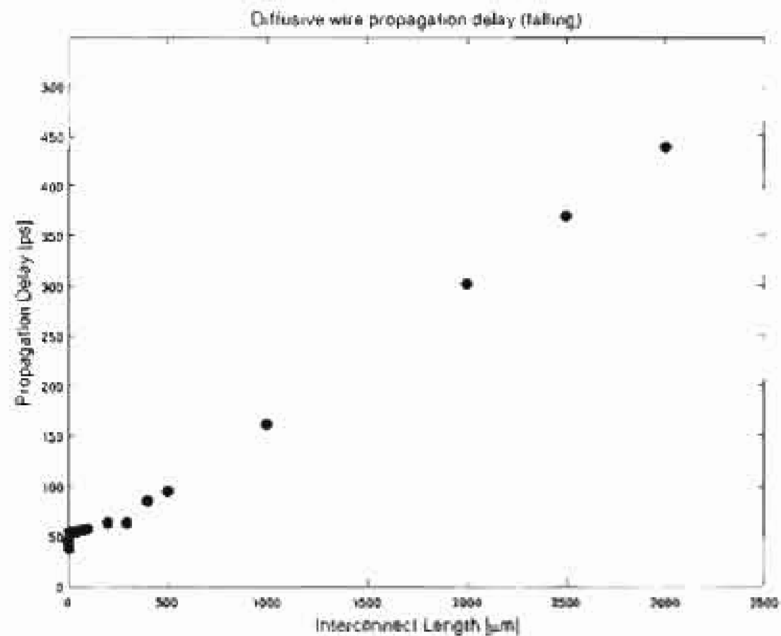

Figure 3.10. Diffusive wire propagation delays (falling) (short interconnects) (1 GHz)

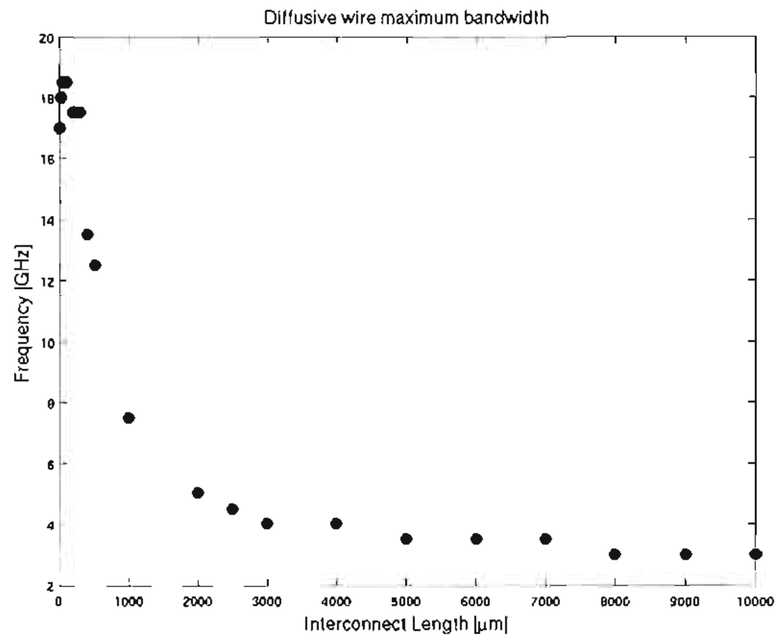

Figure 3.11. Diffusive wire maximum bandwidth

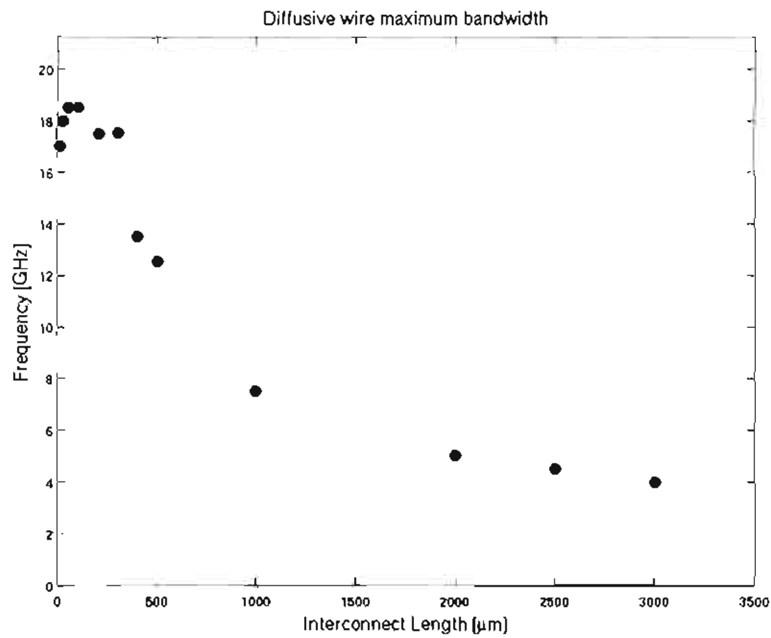

Figure 3.12. Diffusive wire maximum bandwidth (short interconnects)

3.3 Noise Tolerance

Two noise tolerance simulations were performed to measure both the transient and the propagated noise tolerance of each system. The transient analysis consisted of switching the input voltage quickly (~1 ps) and measuring the settling time. Since the diffusive wires operate in the *RC* domain, they do not suffer from reflections due to impedance mismatch. The wire's resistance contributes far more to the wire's impedance than the wire's inductance. Therefore, the settling times for the diffusive wires are the same as the rise and fall times shown in the figures in section 3.2.

To simulate the propagated noise analysis, a DC sweep on the input was performed. The diffusive wires use the same size inverter for the driver and the repeaters. The driver had a range of 200 mV where the output was between the required 10% to 90% V_{DD} values. By sending the voltage through multiple repeaters, however, this range decreased significantly; the range was 26 mV after the first repeater and 3 mV after two repeaters, as shown in Figure 3.13. Therefore, as long as the steady state noise does not move the repeater input between 500-700 mV, the noise will not be propagated to the next stage. To truly determine the noise tolerance, noise must be added to each stage to model the effects of various system components such as power supply jitter and wire coupling.

3.4 Area Requirements

Modern commercial processes produce one active silicon layer underneath several metal layers. Different metalization options can be chosen by the designer to determine the thickness of the upper metal layers and the type of insulator between them (either tetraethyl orthosilicate (TEOS/FTEOS) or a low-k dielectric) [16]. Although adding more metal layers makes building the interconnect possible, the number of devices on an integrated circuit is limited by the silicon base. Future processes will most likely involve 3D processes which include multiple semiconductor layers to build transistors. This technology still faces many challenges such as heat dissipation, multilayer interconnects, and nondestructive production measurements

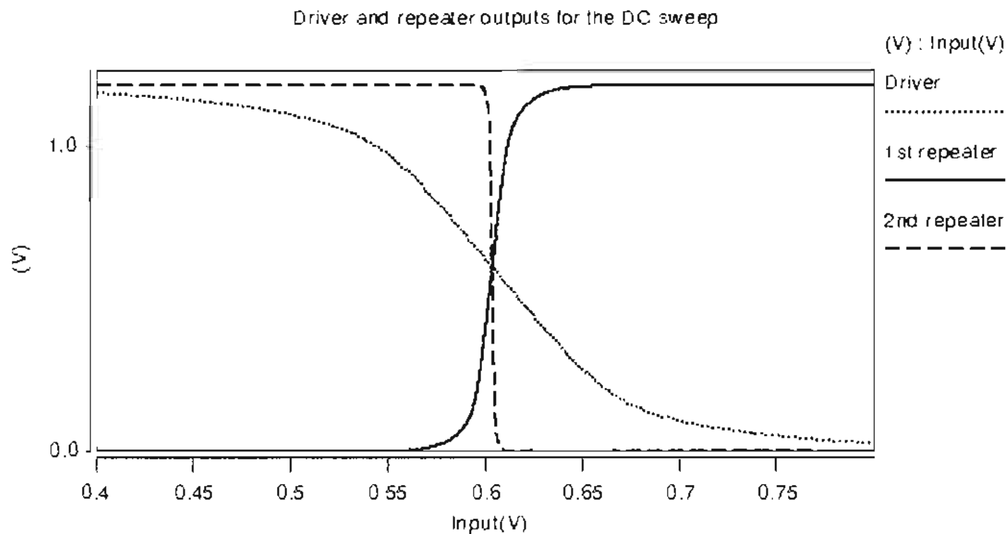

Figure 3.13. DC sweep of driver and two repeaters

while remaining economically feasible [17].

The amount of silicon area required to implement an optimized diffusive wire is proportional to the length of the line due to repeater placement. For minimum pitch wires in the IBM 65 nm process, a repeater was required every 500 nm. Figure 3.14 shows exactly how many repeaters are required for different interconnects of different lengths. Furthermore, Figure 3.15 shows the silicon area required by the complete diffusive wire system including the buffer, driver, repeaters, receiver, and a small load. The load only requires 0.4 μm^2 of area. Note that the area increases significantly for longer lines. The diffusive wires themselves are very small; the minimum pitch for the top metal layer diffusive wires under investigation is 0.20 μm.

Intermediate and long global wires (i.e., interconnects that are approximately 500 μm and longer) are usually placed on upper metal layers. The lower metal layers are reserved for connecting devices and local interconnects. Each repeater in an optimized wire requires a pair of vias connecting the wire to the substrate. These vias require metal contacts on every metal layer between the interconnect and the substrate which block metal routing on each layer. If the repeaters can be

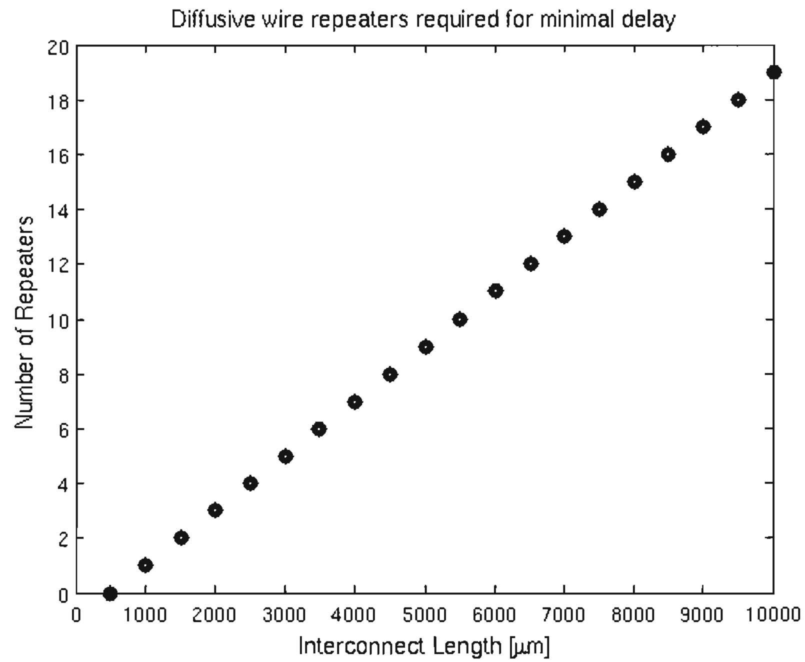

Figure 3.14. Number of repeaters required for optimized diffusive wire (upper metal layer and 500 nm spacing)

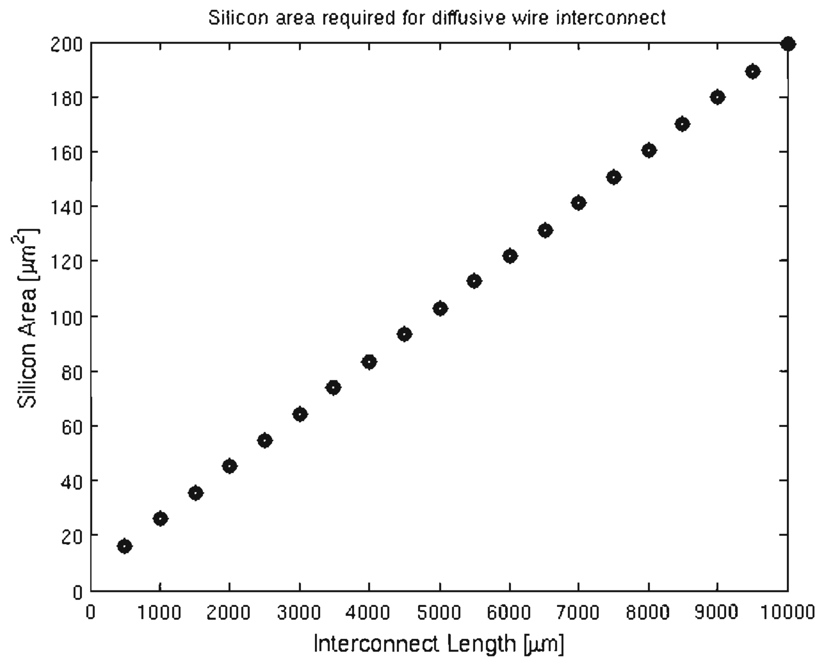

Figure 3.15. Silicon area required for diffusive wire driver, repeaters, and receiver

removed, more routing space for local interconnects will be available.

3.5 Low Resistance Wires

The wire delay is proportional to the resistance and the capacitance of the wire. Potentially, a designer could reduce the wire delay by reducing the resistance. According to equation (1.2), this can be done by either increasing the width or the thickness of the wire. Since the wire thickness is controlled by the foundry, the circuit designer can only control the wire width to change the wire delay. Unfortunately, as the wire width increases, the wire capacitance increases due to the parallel plate capacitance from wire-to-closest conducting layer beneath it.

The resistance decreases faster than the capacitance increases, so the RC delay for the wire decreases. Although the wires require roughly the same number of repeaters, the repeaters must be larger according to equation (3.2). Larger repeaters mean higher power consumption. Even with the decreased wire delay, it is still not close to the propagation speeds obtainable with transmission lines (for silicon dioxide - approximately 1/2 the speed of light). Figure 3.16 [21] shows how the diffusive wire delays changes with wire widths for a 180 nm process.

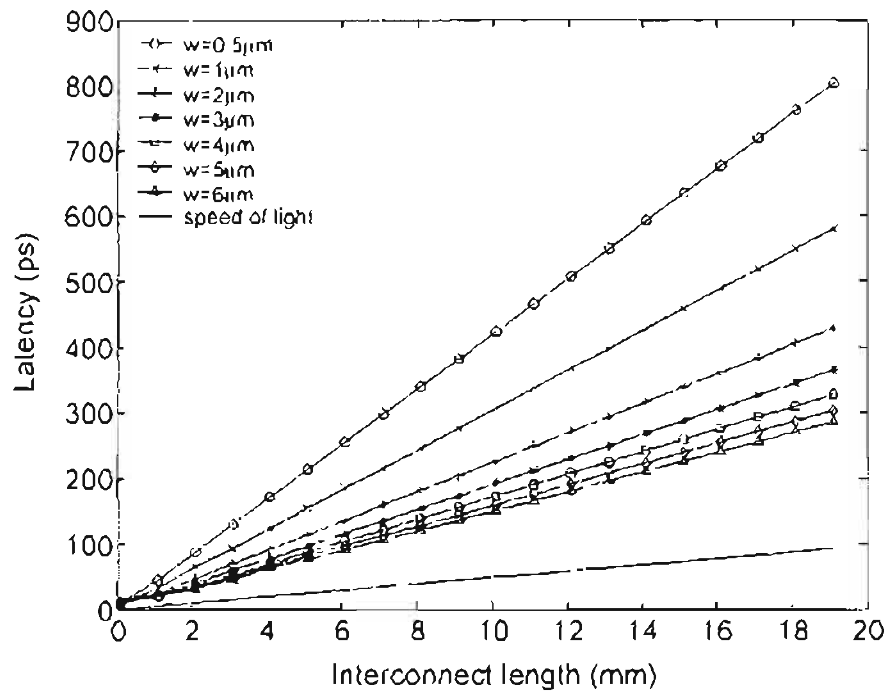

Figure 3.16. Low resistance wire latency (180 nm process) [21] ©2006 IEEE

CHAPTER 4

TRANSMISSION LINE MODELING

The characteristic impedance, Z_o, of a transmission line summarizes many important electrical properties of the line. Knowing the impedance allows the designer to make important decisions to ensure proper signal propagation and mitigate reflections. Determining Z_o for a given transmission line is a nontrivial task that requires accurate, fast modeling. All the transmission line dimensions were synthesized by a software tool developed at Mentor Graphics by Rafael Escovar for coplanar transmission lines, as shown in Figure 4.1. Since all the transmission line modeling in this thesis rely on this tool, a brief overview on how the tool operates will be given. Escovar's thesis contains a much more detailed explanation [2].

4.1 Transmission Line Synthesis

The characteristic impedance of the line is defined as the ratio of voltage to current experienced by a single waveform traveling on the line. Z_o is dependent on frequency. To derive Z_o, the transmission line is divided into small blocks consisting of a resistor and an inductor connected in series to a capacitor and conductor in parallel with values of R, L, C, and G, respectively.

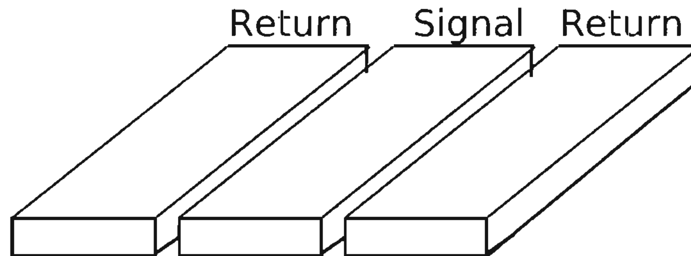

Figure 4.1. Transmission line geometry

Combining the series impedance and shunt admittance of each block and calling them z and y results in

$$z = j\omega L + R \tag{4.1}$$

$$y = j\omega C + G \tag{4.2}$$

Starting with one block with an impedance of $\tilde{Z}_c$, a second block can be added in series with it by combining the shunt admittance, y, in parallel with $\tilde{Z}_c$ and then combining the impedance z in series. Simplifying the resulting equation yields [22]

$$\tilde{Z}_c = \sqrt{\frac{z}{y} + z\tilde{Z}_c} \tag{4.3}$$

Dividing each block into n blocks, the R, L, G, and C values become R/n, L/n, G/n, and C/n. The impedance and admittance become z/n and y/n. By substituting these values into (4.3) and taking the limit as n approaches infinity, the last term of (4.3) goes to zero which yields

$$Z_c = \sqrt{\frac{z}{y}} \tag{4.4}$$

Substituting (4.1) and (4.2) into (4.4) yields

$$Z_c = \sqrt{\frac{j\omega L + R}{j\omega C + G}} \tag{4.5}$$

By taking the limit of (4.5) as the frequency, ω, goes to infinity, the equation becomes

$$Z_o = Z_c \approx \sqrt{\frac{L}{C}} \tag{4.6}$$

This equation demonstrates that, at high frequencies, the characteristic impedance becomes dependent only on the inductance and capacitance of the line. At lower frequencies, the resistance becomes more dominant than the inductance. For transmission lines surrounded by silicon dioxide, the conductance is negligible compared to the capacitance and can be neglected. Once the resistive component becomes greater than the inductive component, the transmission line enters the RC or diffusive wire region. Studious transmission line design requires the designer to ensure that the line remains in the RLC regime. Escovar's tool provides a minimum boundary that guarantees that the transmission line operates in this region. In other words, the region where delay is linearly proportional to the wire length and the speed of propagation equals the speed of light in the medium. Quadratic delay with interconnect length is a clear indication that the interconnect is in the RC region. As already discussed in Chapter 1, inserting optimally sized and spaced repeaters allows longer RC wires to have linear delay with interconnect length. The transmission lines, however, do not require these repeaters and propagate signals at much higher speeds than the RC wires.

4.1.1 Minimum Boundary Derivation

Escovar's thesis [2] contains a detailed derivation of this boundary based on a paper by Davis and Meindl [23] that produces simplified expressions to describe the transient response of high-speed distributed RLC interconnects. Meindl builds on previous papers that derived the same expressions for RC wires. The most important results of this derivation follows.

The expression for a voltage waveform [23] traveling down a lossy infinite length transmission line is

$$V_{inf}(x,t) = V_{DD}\frac{Z_o}{Z_o + R_{tr}}e^{-rx/2Z_o} \tag{4.7}$$

where R_{tr}, r, x, and t are the resistance of the source, resistance of the line per unit length, distance, and time, respectively. To perform proper switching at the end of

the transmission line, the voltage should be greater than 0.5 V_{DD} at the end of the line. By using equation (4.7) and an equation describing finite lines (equation (42) in [23]) the condition can be rewritten as [2]

$$\frac{4Z_o}{R_{tr} + Z_o} e^{-(rL/2Z_o)} > 1 \tag{4.8}$$

where L is the length of the wire. Solving for the ratio of the total resistance, rL, to the characteristic impedance, Z_o leads to

$$\frac{rL}{Z_o} < 2ln\frac{4Z_o}{R_{tr} + Z_o} \tag{4.9}$$

The left hand side of equation (4.9) will always be positive. Therefore, the logarithm on the right hand side must always be positive. Satisfying this condition means that

$$R_{tr} < 3Z_o \tag{4.10}$$

Satisfying equations (4.9) and (4.10) guarantees that the wire will act as a transmission line with a delay linearly proportional to length and a propagation speed equal to the speed of light in the medium. Escovar imposes another condition that R_{tr} must be greater than or equal to Z_o to eliminate overshoot [2]. In spice simulations of the circuits, this condition proved to be too restrictive; there was little overshoot even when R_{tr} was less than Z_o. Appendix A shows that these boundaries correspond to a minimum spacing between the transmission line wires to produce a minimum characteristic impedance.

4.1.2 RLC Calculations

Calculating the characteristic impedance and modeling the transmission lines requires accurate modeling of the resistance, inductance, and capacitance of the wires involved. For wires in silicon dioxide, the conductance is negligible and

set to zero. These parameters must be calculated many times to produce the desired transmission lines. Therefore, the modeling work needs to be very fast while providing an acceptable level of accuracy. Since resistance and inductance are frequency dependent, all parameters were calculated for a particular frequency.

4.1.2.1 Resistance Calculation

At low frequencies, the current flows uniformly throughout the entire conductor. Therefore, the resistance of a wire can be found using equation (1.2). As the frequency increases, however, the current no longer flows uniformly through the conductor due to magnetic fields within the conductor [24]. The fields cause the current to flow only in a shallow band at the conductor's surface. Since only a fraction of the conductor cross sectional area is being used for current flow, the resistance increases. This frequency dependent increase in resistance is known as the skin effect; it becomes noticeable at a certain skin-effect cutoff frequency [24], ω_s. At this frequency, the added resistance due to the skin effect becomes comparable to the conductor's resistance. Thicker conductors are required to attenuate the magnetic fields. The necessary thickness is called the *skin depth* and is given by equation (4.11),

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{4.11}$$

where ρ, ω, and μ are the resistivity of the conductor, the frequency of operation [rad/s], and the magnetic permeability of the conductor, respectively [24]. The skin effect becomes noticeable around 10 GHz wire dimensions under consideration in this thesis. To account for the skin effect, higher frequency signals require wider wires to maintain a low enough resistance. Escovar's tool takes into account the skin effect for resistance. For IBM's 65nm process, the highest frequency due to FO4 delays is approximately 15 GHz. Although the skin effect is limited at these frequencies, including it adds another degree of accuracy and makes the tool more flexible for calculating transmission line dimensions with future processes.

4.1.2.2 Inductance and Capacitance Calculations

The inductance extractor developed by Escovar [2] determines the inductance of the closed loop system. The extractor operates by dividing each wire into a large number of filaments. The tool is able to calculate the current for each of the filaments and add them together to determine the total current. Using these current values and the applied voltages, the line impedance and inductance can be determined. The reader should refer to Escovar's thesis [2] for a much more detailed explanation.

Escovar compared his tool to the standard used by academia, FastHenry [25]. Developed at MIT, FastHenry similarly divides the wire into a number of volume filaments. The tool uses a matrix solution algorithm to solve for the currents in the line. Escovar demonstrated that his tool produced results very close to FastHenry (usually less than 1% difference). His tool, however, operated at an order of magnitude faster; it required less than one tenth the time to do the same extraction [2]. The fast inductance extractor made it possible to quickly determine transmission line effects in real time. Furthermore, the inductance extractor takes into account the change in current distributions caused by the skin effect at higher frequency.

The capacitance was calculated using a FastCap approach [19]. Since all the charge is on the surface of the conductors, the skin effect does not affect the capacitance.

4.1.3 Transmission Line Dimensions

In order to not repeat the same transmission line calculations, the results from Escovar's tool were saved to a repository of transmission line dimensions. A summary of the repository is in Appendix A. The appendix shows many interesting trends in transmission line dimensions as various design parameters such as frequency, characteristic impedance, or length of the line change. It also shows the relationship between the total line resistance (i.e., the total loop resistance calculated by summing the resistance of the signal wire and the resistance of the parallel combination of the two return wires) and characteristic impedance. As the

total resistance goes up due to the skin effect or due to increasing line length, the wires need to be wider and the minimum spacing (S_{min}) increases.

Additionally, the appendix provides valuable information for designing and simulating the lines. One weak point of Escovar's tool is that it only calculates successful lines without determining the smallest total width necessary. The total width equals the sum of the signal wire width (W_S), twice the spacing ($S(Z_o)$), and twice the ground wire width (W_G). In Appendix A, only the transmission lines with the three smallest total widths are shown. Lengths with less than three designs indicate that the particular design space was not extensively studied.

The appendix definitely does not provide an exhaustive list of minimum dimensions to produce the desired set of transmission lines. Other wire dimension combinations and smaller widths may be possible. Application specific transmission lines may be even smaller. For example, if designing a multibit bus with several parallel transmission lines, then the ground wires can be built smaller with wider signal wires. Normally, the signal wire should be roughly the same width as the ground wires to ensure that the signal wire is properly coupled to the return wires. The parallel transmission lines, however, provide additional shielding and can use smaller wires. For this thesis, the possibility of sharing return paths was not investigated. The combination of return currents can affect the RLC parameters of the line and requires additional modeling to guarantee transmission line behavior.

4.2 Transmission Line Drivers

Driving transmission lines requires fast, low impedance drivers. The output of a MOSFET can be modeled as a voltage source connected in series with a source resistance. In order to minimize the noise, the drivers should have a constant output resistance. If the output resistance matches the impedance of the transmission line, reflections would be eliminated. This is called a source-series termination [26]. However, if the output resistance of the driver is comparable to the loop resistance of the transmission line, then it will not be able to drive the line. Furthermore, the driver's output resistance can not be too low compared to the line's resistance or

there will be potentially damaging overshoot at the line output.

To obtain a first order approximation for the transistor sizing, a spice simulation was designed to find the transistor widths corresponding to different transistor drive strengths. The first step was to assume a 50 ps rise time and set this value equal to the time constant (i.e., output resistance times the load capacitance). Next, solving this equation for the load capacitance gave

$$C_{load} = \frac{50ps}{R_{out}} \tag{4.12}$$

Substituting different values for the output resistance, R_{out}, gave different capacitances, as shown in Table 4.1. These capacitance values were attached to the output of the transistor, and the width was changed until the rise time equaled $50ps$. Using this method, the transistor width corresponding to any driver output resistance could be found. The resulting transistor widths for the three drivers using the IBM CMOS10SF spice models are given in Table 4.2.

Ideally, the driver should have a constant output impedance so it can be properly matched to the transmission line. Unfortunately, this is not the case for MOSFETs; they do not have a constant output resistance. When either the NMOS or PMOS

Table 4.1. Load capacitances used in spice to determine driver transistor sizes

$R_{out}[\Omega]$	$C_{load}[fF]$
80	333
100	500
150	625

Table 4.2. Measured rise times and device widths for various drivers

Predicted Driver Output Impedance $[\Omega]$	Measured Rise Time $[ps]$	NMOS Device Width $[\mu m]$	PMOS Device Width $[\mu m]$
80	50.4	11.25	22.5
100	50.4	9	18
150	50.0	6.05	12.1

device is fully on, the resistance is constant. When each device enters the linear region of operation (which occurs during every switching event), the resistance increases significantly. Figure 4.2 shows the nonconstant output impedance as the driver switches. As the driver size increases, the output resistance becomes more constant. The figure also shows that the driver's output resistance was much less than expected.

For the lossless transmission lines, overshoot was a major concern. However, switching to the lossly transmission lines (more accurate for modeling transmission lines on integrated circuits) showed that the resistance of the transmission line eliminates most of the overshoot. The main performance limiting factor was signal buffering and the FO4 delay; the measured FO4 delay for the process is 70 ps. The final driver size selected had an NMOS width of 20 μm and PMOS width of 40 μm compared to the diffusive wire repeaters that have an NMOS width of 12 μm and PMOS width of 24 μm. Figure 4.3 shows the output resistance of the driver. The resistance is about 38 Ω when the PMOS is on and 18 Ω when the NMOS is on. The final transmission line driver has a rise time of approximately 10 ps.

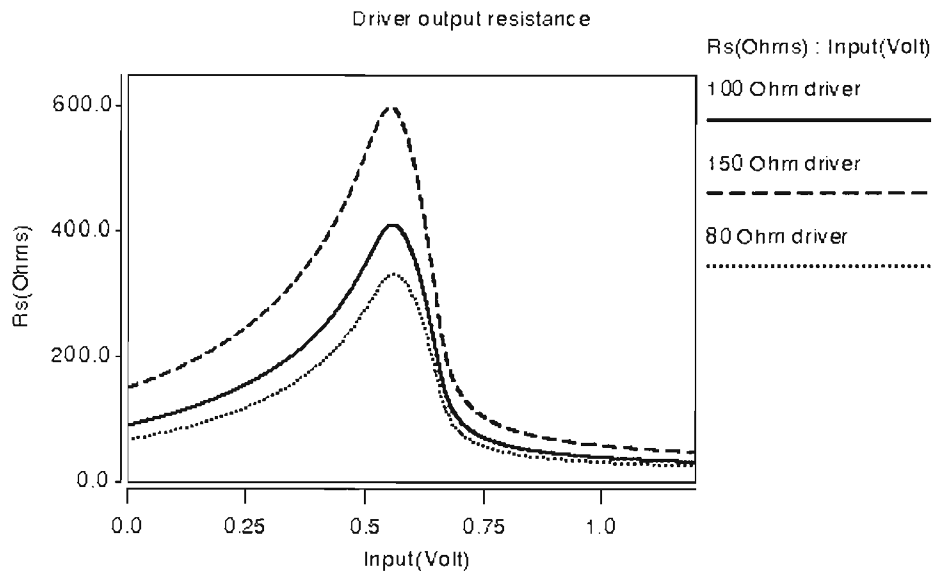

Figure 4.2. Driver output resistance

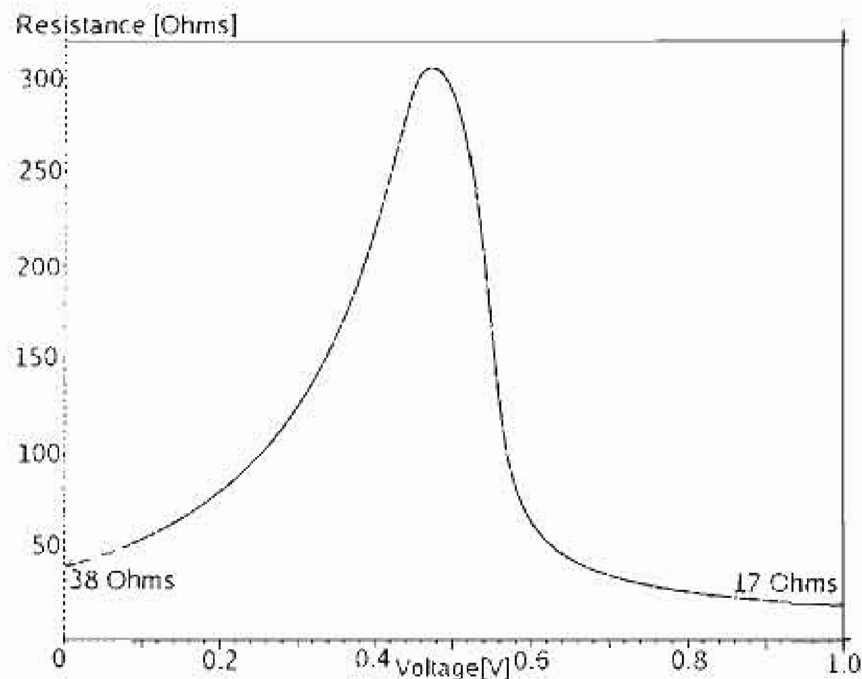

Figure 4.3. Final transmission line driver output resistance

4.2.1 Annular Drivers

In order to produce a faster, more constant driver, annular transistors were proposed. A conventional MOSFET consists of a gate with symmetrical source and drain on either side. The annular transistor has a circular or a square gate with the source on the outside and the drain on the inside, as shown in Figure 4.4. The main motivation for using this driver is to reduce the parasitics, to possibly produce lower resistance drivers, and to more easily match the impedances. In order to fully profit from the device, it needs to be sized so that W_S is as small as possible; the drain becomes merely a contact with a very small diffusion region around it. When designed in this fashion, some design rules for the process are broken such as connecting narrow gate polysilicon to other gates. Meeting all design rules results in a larger device that acts as four transistors placed in a circle. Currently, annular devices are only used for projects that need high radiation and noise immunity [27, 28, 29, 30]

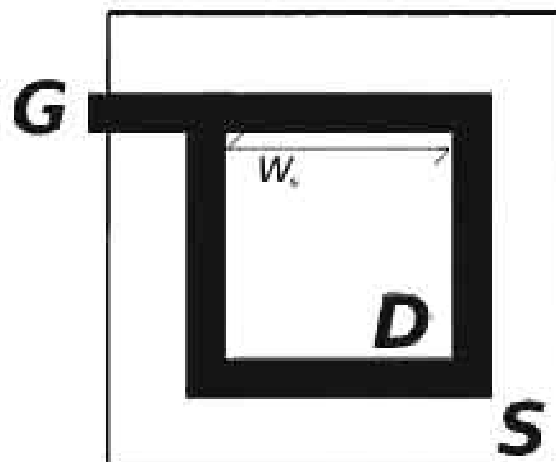

Figure 4.4. Aerial view of annular driver

The annular driver was modeled by calculating the area and periphery of the source and drain based on the width of a side, w_s, the gate length, and minimum diffusion design rules. These values were placed into the IBM spice MOSFET models used for the conventional transistors. The accuracy of this approach is unknown. Table 4.3 shows the parameters used in the spice model for the annular and conventional MOSFETS. The rule breaking annular MOSFET used in the simulations had $w_s = 150$ nm, which is also listed in Table 4.3. Also, it should be noted that the simulations for the annular and conventional MOSFETs did not use fingering; the annular MOSFETs used only the multiple (m), and conventional MOSFETS just used width (w) to increase the drive strength and transistor size. In practice, both
designs will have less area for the source and drain than listed. The only exception to this rule was in the area estimation. Overlapping the annular transistor squares as much as possible decreases the area significantly. In order to better compare this area with the conventional transistor area, they had to be corrected to take into account fingering. A better approach would be to use a semiconductor device simulator to model these devices better. For this thesis, however, a faster simulation that could be easily integrated into spice simulations was more important.

To compare the annular and rectangular drivers, both devices were attached to

Table 4.3. Model parameters for annular and conventional MOSFETs

Parameter Name	Annular MOSFET	Annular MOSFET (w_s=150nm)	Conventional MOSFET
Length [nm]	50	50	50
Width [nm]	$4w_s$	600	w
Drain Area [nm^2]	w_s^2-(90 nm)^2	14400	155w
Source Area [nm^2]	$(w_s+155)^2-(4w_s(50))+w_s^2$	40525	155w
Drain Periphery [nm]	$4w_s$	600	2w+2×155
Source Periphery [nm]	$4(w_s+w_s+2(155))$	2440	2w+2×155

equivalent capacitive loads (500 fF). By changing the number of annular drivers connected in parallel, the rise time also changed to match the rise time of the rectangular driver.

Since the largest performance limitation to the transmission line interconnect is the speed of the buffers, advantages in buffering are as important as driver advantages. The annular drivers were simulated against the rectangular drivers in two way: first, the transmission line system was tested with the rectangular buffers and the annular driver at the end: and second, with annular buffers and annular drivers. The setup of the buffer, driver, transmission line and receiver are shown in Figure 4.5.

In terms of area, the annular driver showed a 35% decrease in area, as shown in Table 4.4. The buffering did not show a comparable drop in area because the buffer

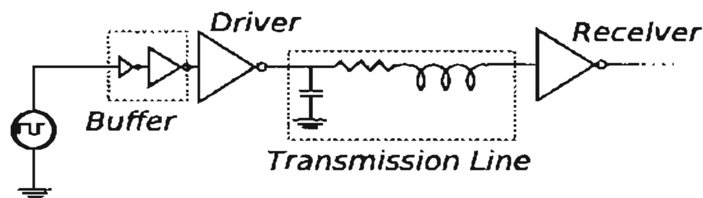

Figure 4.5. Buffer and driver simulation setup

Table 4.4. Driver (including buffer) area comparisons

Driver Type (Buffer Type)	Buffer Area [μm^2]	Driver Area [μm^2]	Total Area [μm^2]
CMOS Driv. (CMOS Buff.)	5.01	16.02	21.03
Annular Driv. (CMOS Buff.)	5.01	10.05	15.06
Annular Driv. (Annular Buff.)	4.19	10.05	14.24

sizes were limited to discrete sizes. The annular buffer drive strength is changed by changing the number of devices in parallel. This number must always be an integer so exact matching with the conventional devices was not possible. Many of the other performance differences for the devices can be explained by this size mismatch, as shown in Figure 4.6 through Figure 4.15. Figures 4.6 and 4.7 show large peaks and drops in power consumption. The effect is attributed to standing waves at multiples of the $\lambda/4$ value (refer to section 5.1.2 for a more in-depth explanation). All the setups had relatively similar overshoot parameters, as shown in Appendix B.

Furthermore, in order to obtain the maximum effect of reducing the drain area, the annular transistors need to be as small as possible. The smaller the devices become, the more design rules need to be broken. There are many rules regarding how transistor gates can be attached to other polysilicon blocks. For example, right angles are not allowed between two gates. Fixing the problem causes the width of each side to become larger, which increases the area of the drain and would reduce the area benefit. Overall, according to the simulations, the annular drivers do not show any performance benefit over the conventional drivers.

4.3 Transmission Line Receivers

The transmission line receivers are designed to accomplish three goals: reduce the reflections caused by impedance mismatch at the end of the transmission line, reduce the amount of transmission line noise propagated to digital stages, and reduce the latency of the receiver. In integrated circuit design, resistors, capacitors, and inductors require large amounts of area to build and are difficult to build with

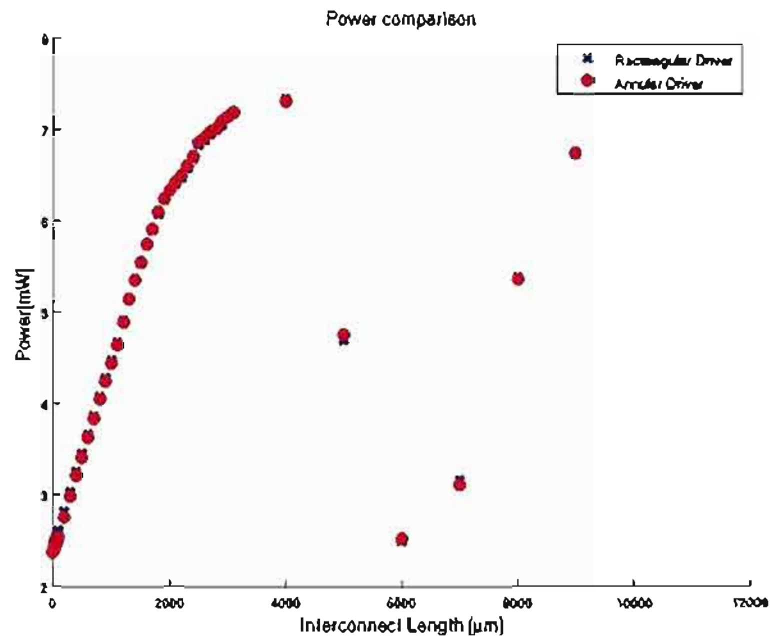

Figure 4.6. Power comparison (conventional buffer, annular driver)

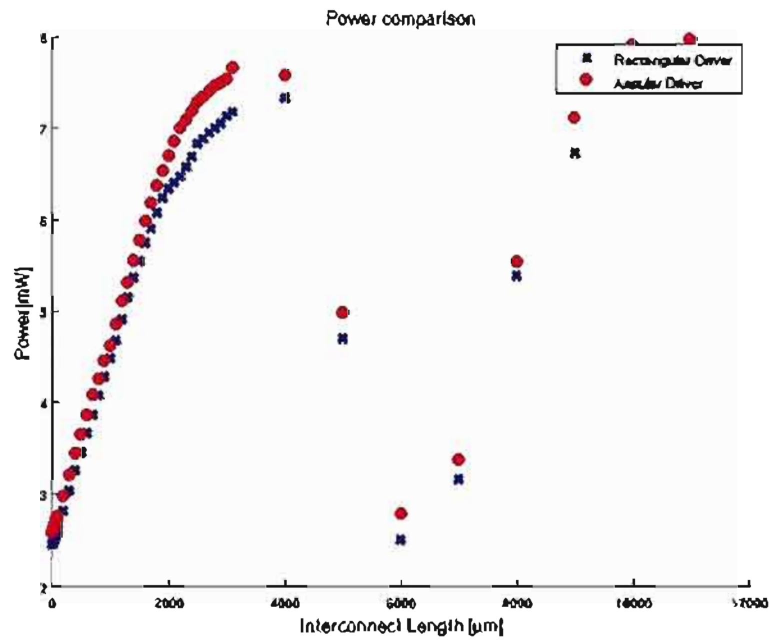

Figure 4.7. Power comparison (annular buffer, annular driver)

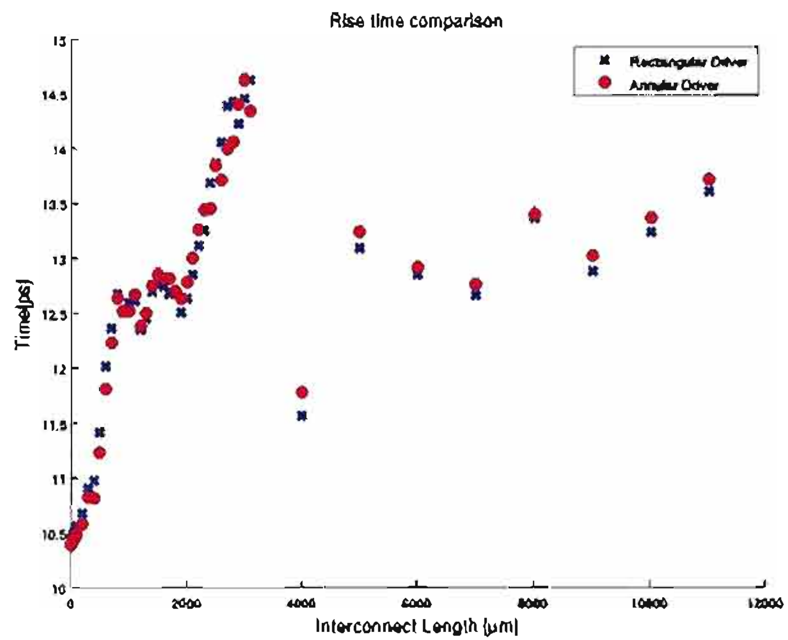

Figure 4.8. Rise time comparison (conventional buffer, annular driver)

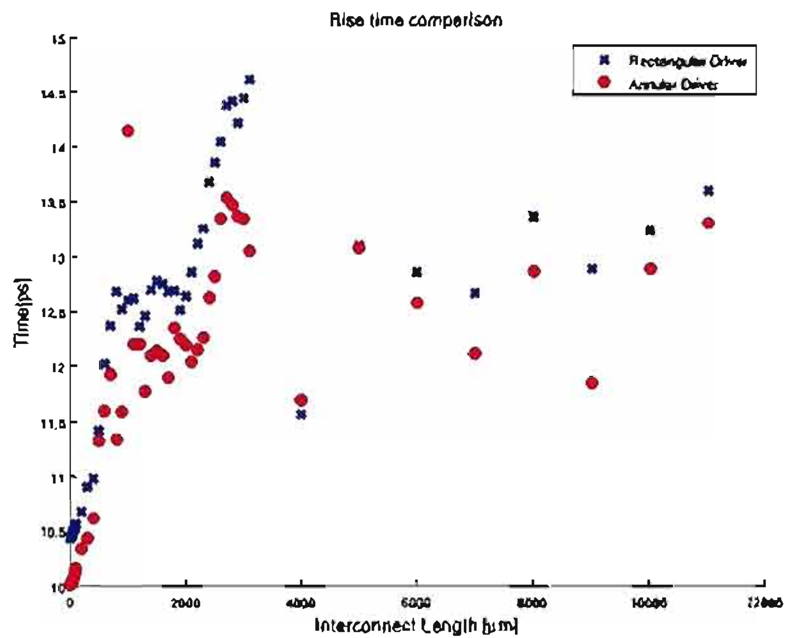

Figure 4.9. Rise time comparison (annular buffer, annular driver)

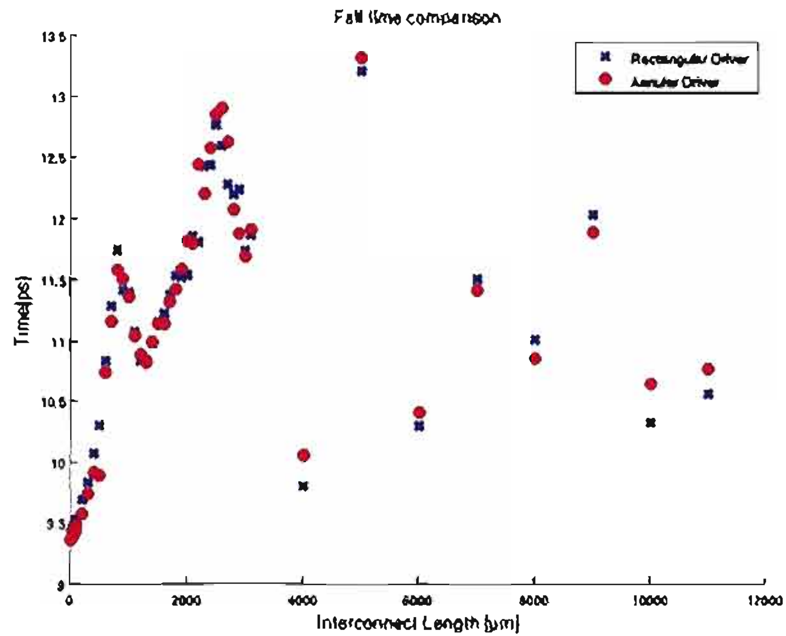

Figure 4.10. Fall time comparison (conventional buffer, annular driver)

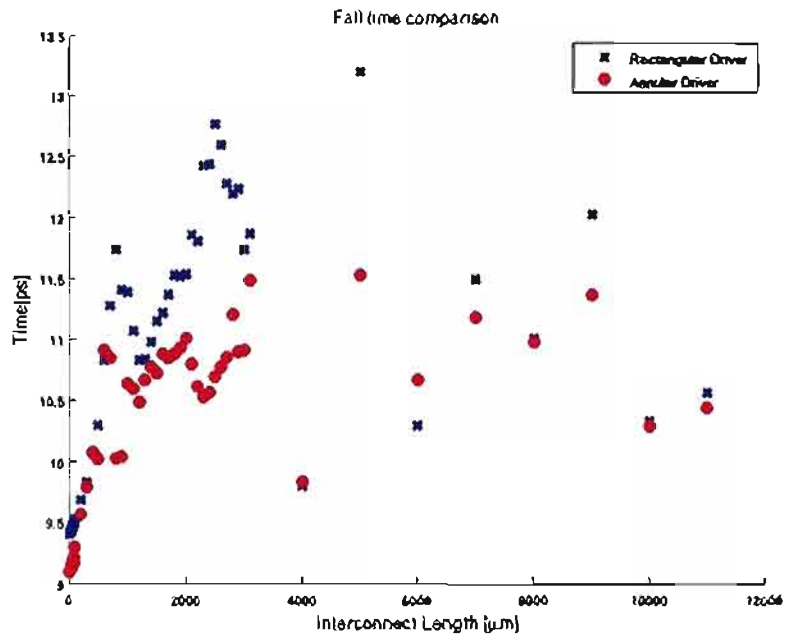

Figure 4.11. Fall time comparison (annular buffer, annular driver)

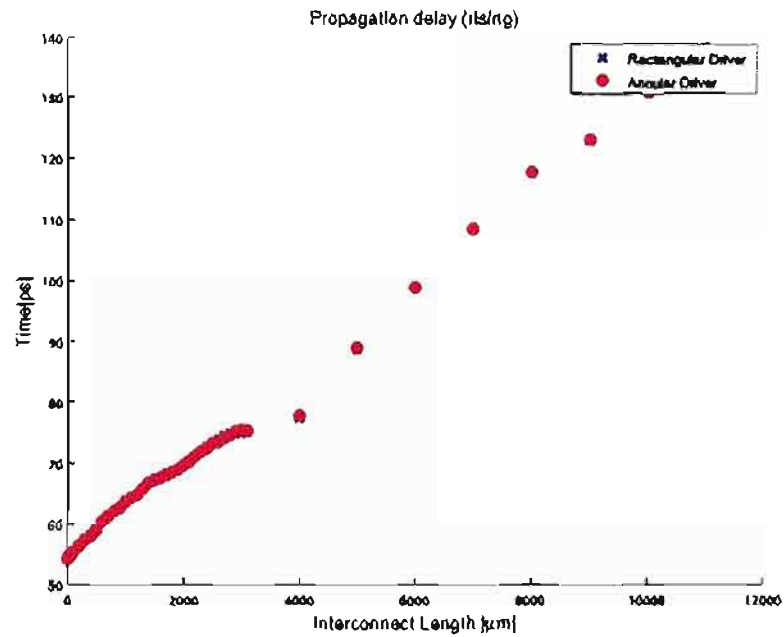

Figure 4.12. Propagation delay (rising) comparison (conventional buffer, annular driver)

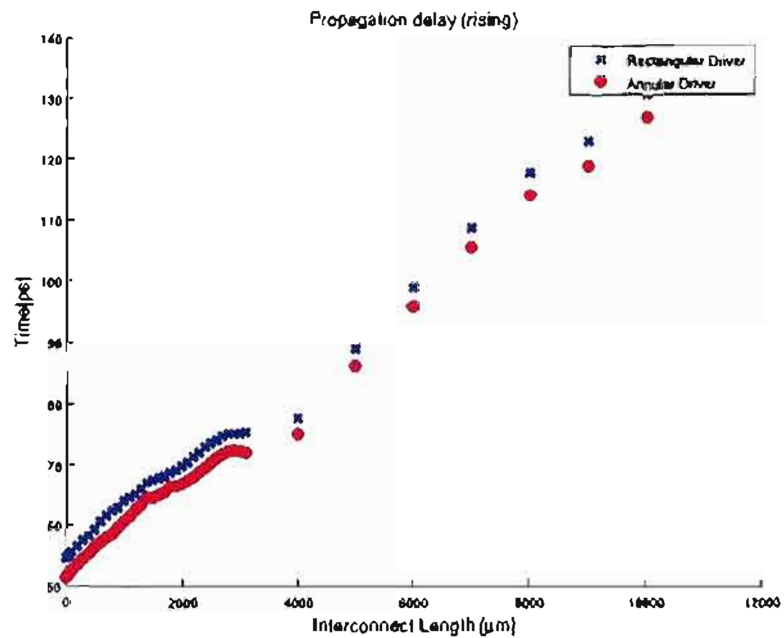

Figure 4.13. Propagation delay (rising) (annular buffer, annular driver)

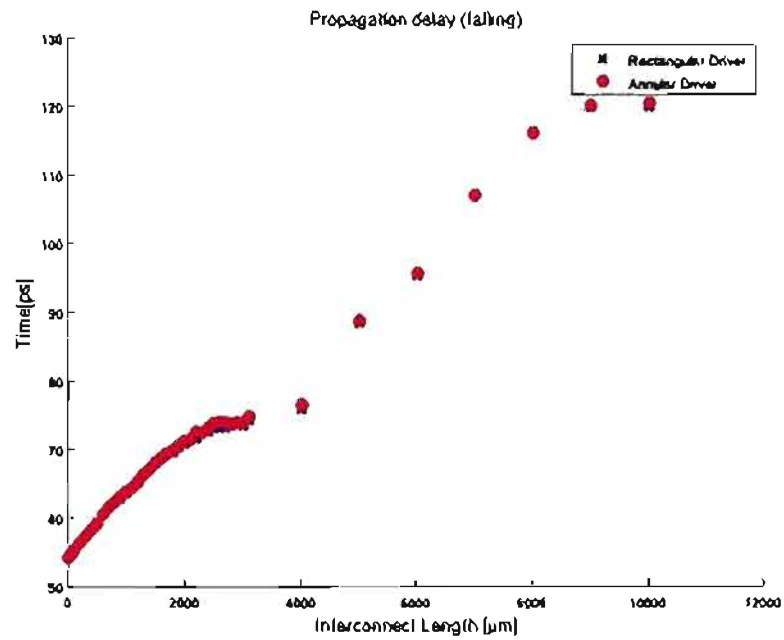

Figure 4.14. Propagation delay (falling) comparison (conventional buffer, annular driver)

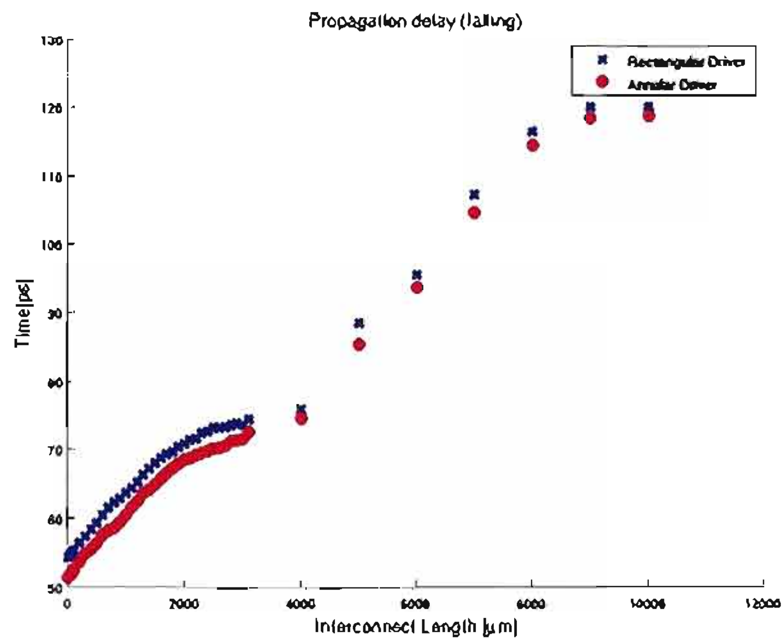

Figure 4.15. Propagation delay (falling) comparison (annular buffer, annular driver)

precise values. The digital designer avoids using these components if possible, which only leaves the size of the receiver as a means to match the transmission line impedance. In this thesis, initial simulations for the lossless transmission lines used minimum sized inverters as receivers. To better match the line impedance, these receivers were replaced with larger inverters. To reduce the propagated noise, hysteresis was added to the receivers by using complementary dynamic logic or jam latches. The proceeding discussion outlines the design process for these circuits along with a performance comparison of each receiver. Except for the lossless transmission line simulations and the receiver simulations in this section, all the simulations in this thesis were performed with the dynamic receiver with minimal hysteresis. This receiver was abandoned for the jam latch receiver late in the study.

4.3.1 Dynamic Receiver and Jam Latch

Noise cannot be eliminated. Therefore, the receivers must be noise tolerant. Complementary dynamic logic (CDL) is one way to increase the noise margin. These gates are implemented with dynamic logic but include a complementary gate that sets the noise margin to any amount desired [31]. The increased noise margin, however, comes at a price; there is a definite tradeoff between noise margin, power, and speed [31].

Utilizing a two-input CDL NAND gate, a noise tolerant receiver can be generated by connecting the precharge signal and one of the inputs that becomes the receiver input [32], which is shown in Figure 4.16. The remaining NAND gate input becomes a reset signal. This signal, however, can only partially reset the circuit. If the signal is low, the circuit output will not be able to switch low. Fully resetting the circuit requires the reset and the receiver input to be low.

By resizing the various transistors, the speed, noise margin, and switching voltage can be set arbitrarily. Larger devices increase the noise tolerance and speed of the gate but require more power. For the receiver simulations, a minimum sized inverter was used as a baseline. The transistors were sized to give the dynamic receiver rise and fall times comparable to the inverter. Table 4.5 shows the transistor widths corresponding to the schematic in Figure 4.16.

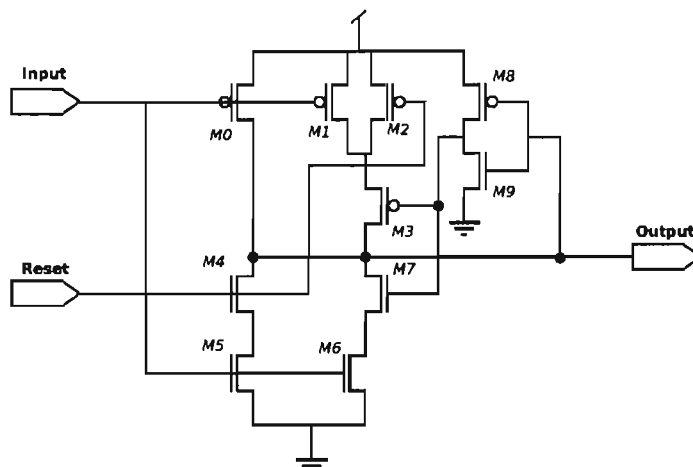

Figure 4.16. Dynamic receiver schematic

Table 4.5. Dynamic receiver transistor widths

Transistor Name	Type[$NMOS/PMOS$]	Width [nm]
M0	PMOS	1000
M1	PMOS	200
M2	PMOS	200
M3	PMOS	200
M4	NMOS	600
M5	NMOS	600
M6	NMOS	500
M7	NMOS	200
M8	PMOS	200
M9	NMOS	100

The receiver was further improved by removing the reset signal by connecting transistor $M5$ directly to the output and removing $M2$. By changing the ratios between various transistors in the design, the amount of hysteresis and the delay could be changed. Two designs with different amounts of hysteresis were tested. Although these pruned dynamic receivers had much better performance than its predecessor, they did not have significant benefits compared to the other receivers. Furthermore, the process of sizing the transistors to increase the amount of hysteresis was far from intuitive. The hysteresis was dependent on the drive strength

of $M8$ and $M9$, the drive strength of $M3$ and $M7$, and the channel resistance of $M1$ and $M6$. Figure 4.17 shows the response of an inverter to a rising and falling input. For the inverter, there is no hysteresis so the two plots are indistinguishable. Figure 4.18 and Figure 4.19 show the same response for the 40 mV and 60 mV dynamic receivers, respectively.

Eventually, the dynamic receiver design was abandoned in favor of a jam latch. The jam latch consists of a large conventional CMOS inverter with two small inverters connected in series to the output, as shown in Figure 4.20. For the simulations in this thesis, the output was taken directly after the first inverter attached to the input. By switching the output to the location in Figure 4.20, the noise tolerance improves and the load has less of an effect on the hysteresis. The first small inverter's input is connected to the output of the large inverter. The second inverter's output is also connected to the output of the large inverter. The small inverters add hysteresis by acting as keepers; they do not allow the output of the large inverter to change until the large inverter forces the first small inverter

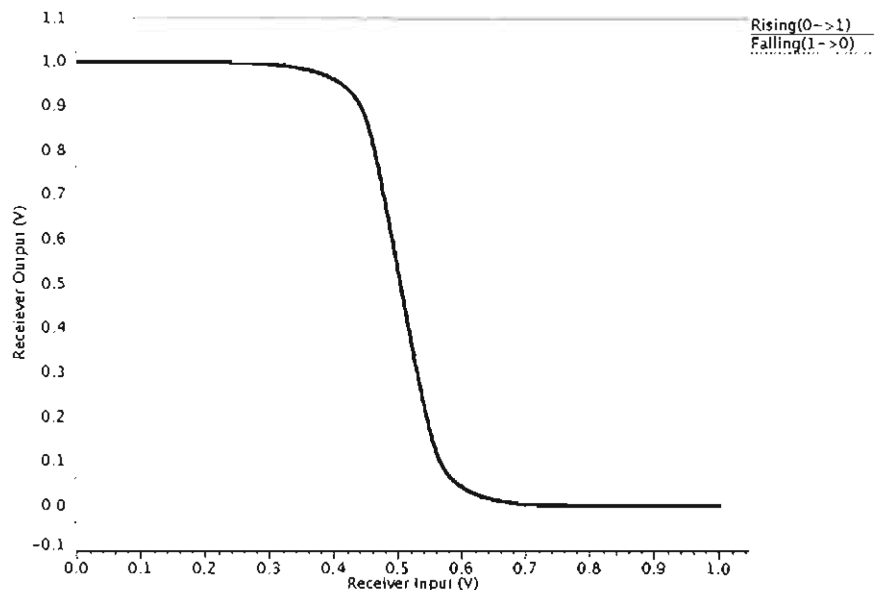

Figure 4.17. DC sweep of CMOS inverter (no hysteresis)

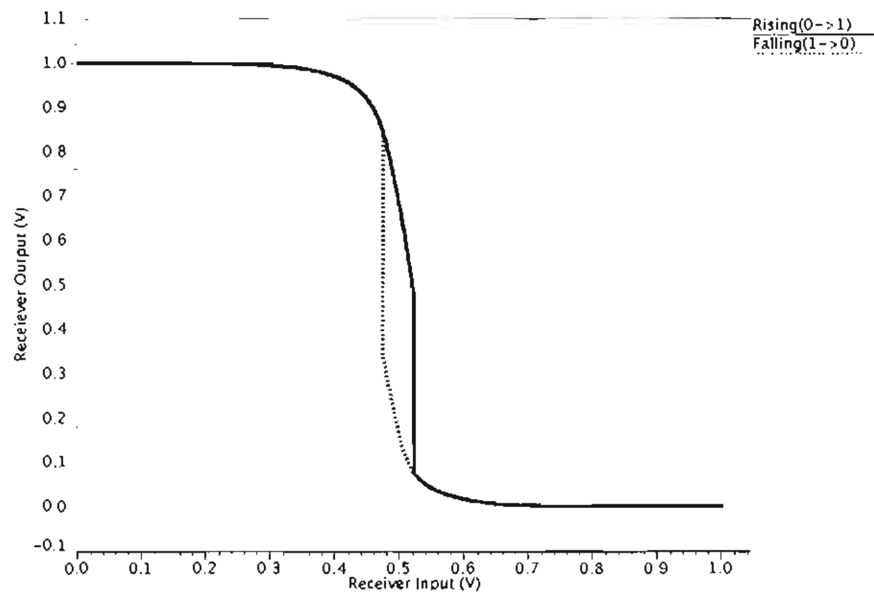

Figure 4.18. DC sweep of dynamic receiver (40 mV hysteresis)

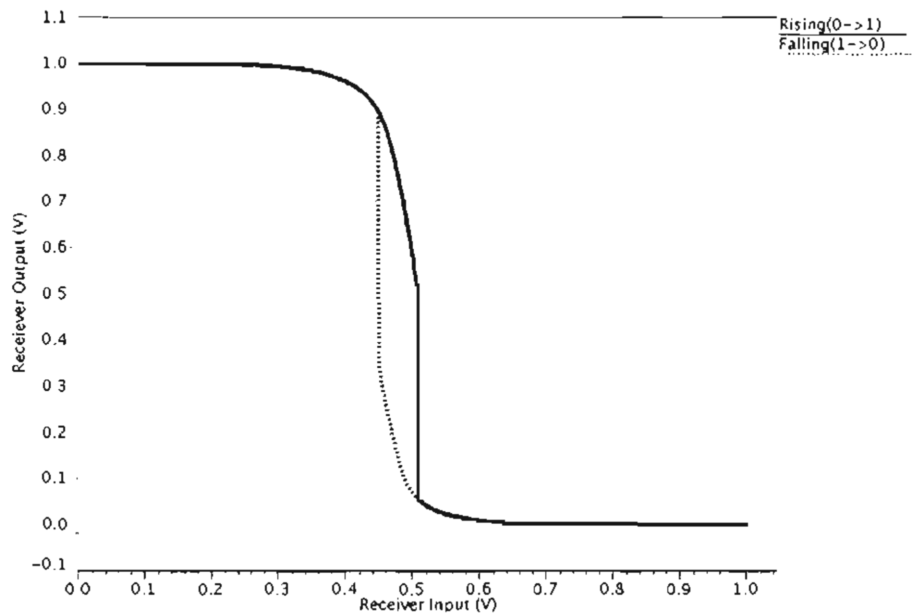

Figure 4.19. DC sweep of dynamic receiver (60 mV hysteresis)

Figure 4.20. Jam latch schematic

to change. The jam latch performed very well and the tradeoff between hysteresis and latency were very straightforward. Figure 4.21 shows the jam latch output response. Figure 4.22 shows the same plot with cursors showing the switching points and the amount of hysteresis (133 mV). This is the same design used in the receiver comparisons.

4.3.2 Receiver Comparisons

The simplest receiver is a CMOS inverter. As a baseline, a small inverter (10x minimum sized) and a larger inverter (75x minimum sized) were compared against two dynamic receivers and a midsized jam latch. Table 4.6 compares the total

Figure 4.21. DC sweep of jam latch receiver (130 mV hysteresis)

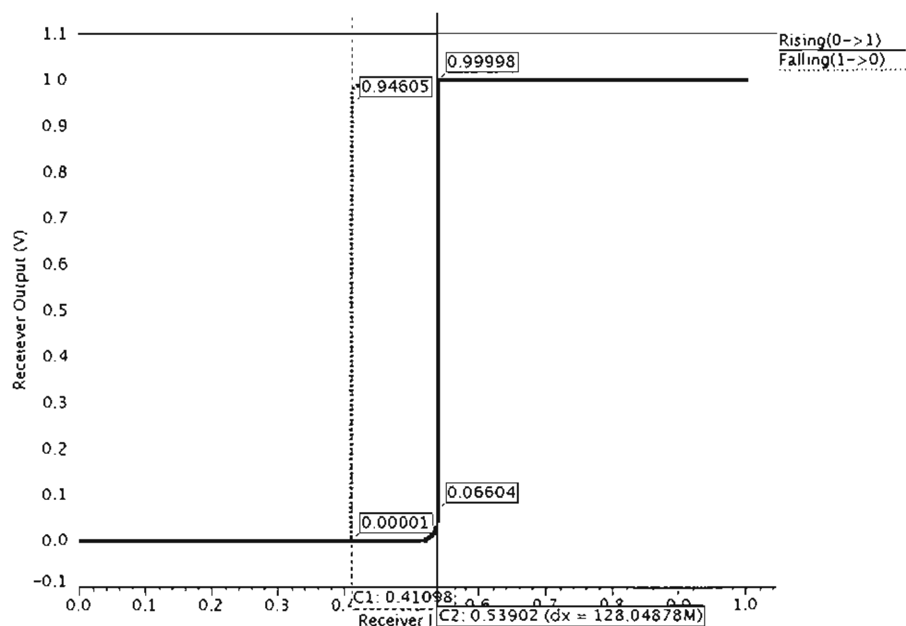

Figure 4.22. DC sweep of jam latch receiver (130 mV hysteresis) with cursors

Table 4.6. Receiver area comparisons

Receiver Type	Area [μm^2]
CMOS (large)	6.01
CMOS (small)	0.80
Dynamic Receiver (40 mV hysteresis)	7.21
Dynamic Receiver (60 mV hysteresis)	5.85
Jam Latch (120 mV hysteresis)	4.89

area of each receiver. The jam latch shows excellent use of area to obtain a large amount of hysteresis. Obviously, the CMOS inverter will be faster but without any hysteresis.

Figure 4.23 is a legend for the comparison plots found in Figure 4.24 through Figure 4.28. The receivers had similar performance characteristics that showed typical behavior for different sized inverters. All the larger receivers use extra power (see Figure 4.24), have faster rise and fall times (see Figure 4.25 and 4.26), and have larger capacitances, which reduce the amount of overshoot above V_{DD} or

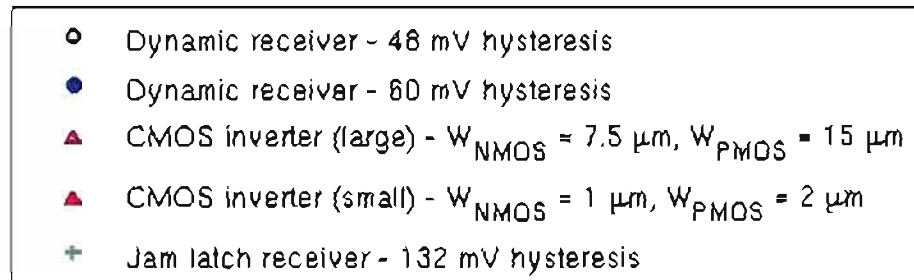

Figure 4.23. Legend for receiver comparison plots

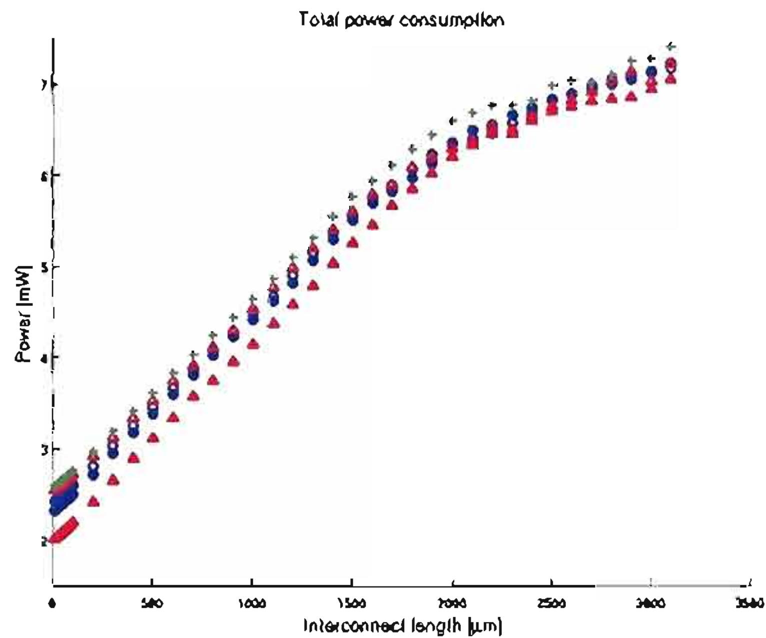

Figure 4.24. System power consumption - various receivers (10 GHz)

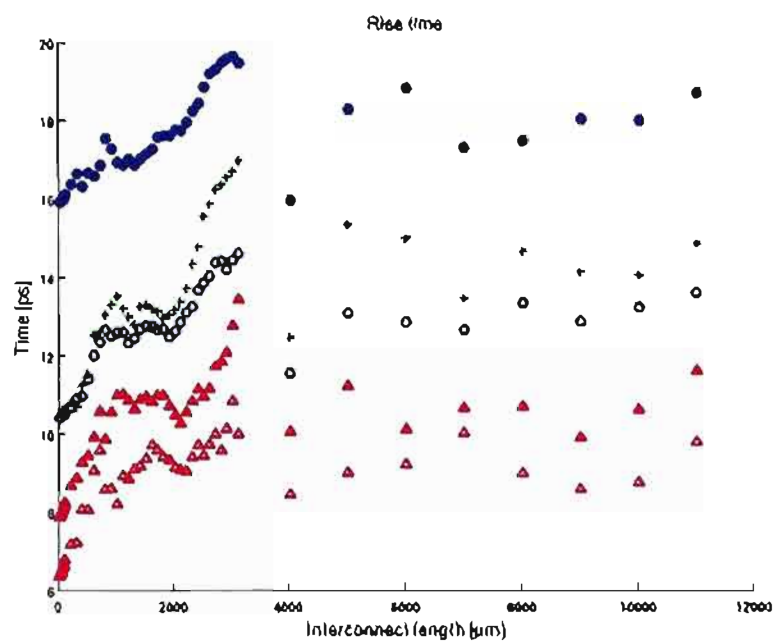

Figure 4.25. Output rise times - various receivers

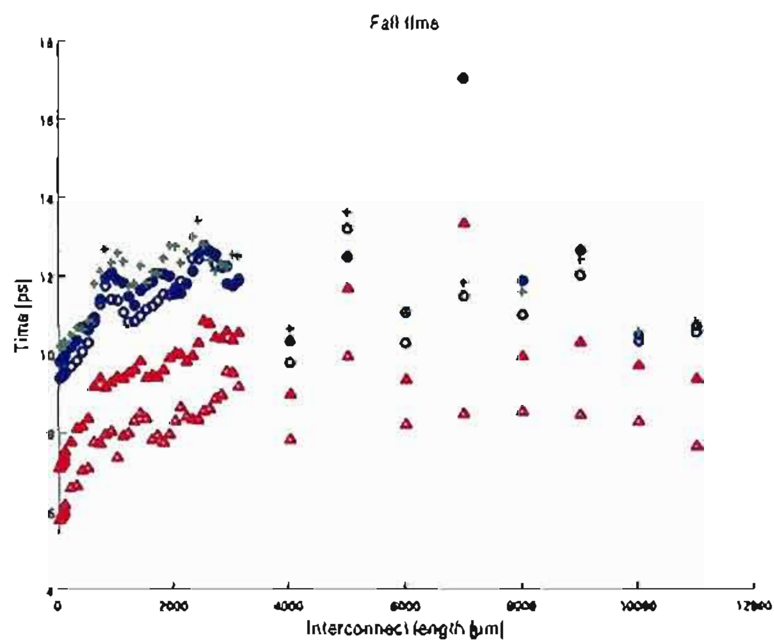

Figure 4.26. Output fall times - various receivers

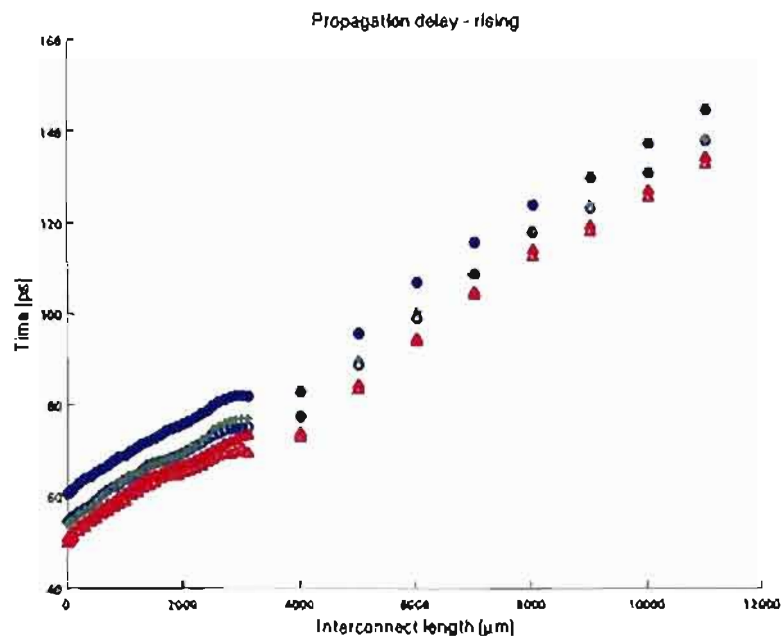

Figure 4.27. Propagation delay (rising) - various receivers

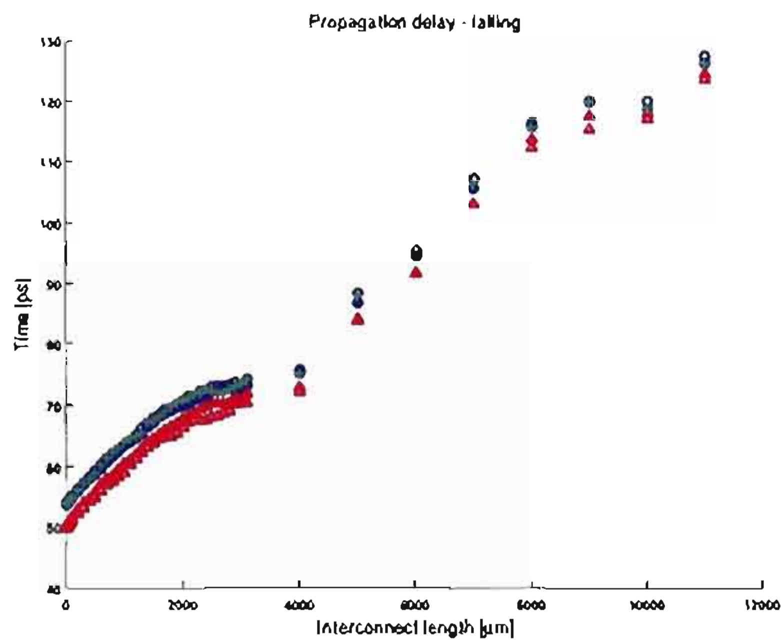

Figure 4.28. Propagation delay (falling) - various receivers

below ground (refer to Appendix B). The total propagation delay is affected by the hysteresis. The hysteresis leads to slower falling transistions and faster rising transitions than their nonhysteretic counterparts. There is also a tradeoff between hysteresis, power, and latency; more hysteresis leads to more power consumption and higher latency if everything else is equal. Based on the simulations, if no hysteresis is needed, a simple inverter is sufficient. If hysteresis is desired, the jam latch works the best. Depending on performance requirements, extra hysteresis can be added.

CHAPTER 5

TRANSMISSION LINE SIMULATIONS

In spice, there is a lossless transmission line model (T model) that contains six required arguments: four for the transmission line connections (two on each side), one for the characteristic impedance, and one for the signal delay of the transmission line in seconds per meter. An optional argument used in this study is the length of the transmission line. This argument is essential for the study since the length of the line is an independent variable being tested.

Additionally, there are several different lossy transmission line models. The W model was selected for this study because it can directly use the R, L, and C parameters generated by the transmission line synthesis program discussed in section 4.1. Initially, the lossless transmission line model with a characteristic impedance of 100Ω was used. Due to the size and material of the wires in integrated circuits, the lossy transmission line models are much more accurate. With the exception of specially marked figures in this chapter, all transmission line modeling were done with the lossy model.

The signal delay of the transmission line depends on the materials surrounding the conductors and is independent of the transmission line geometry, as explained by Bogatin [33]:

> A signal can be launched into a transmission line simply by touching the leads of a battery to the signal and return paths. The sudden voltage change creates a sudden electric and magnetic-field change. This *kink of field* will propagate through the dielectric material surrounding the transmission line at the speed of a changing electric and magnetic field, which is the speed of light in the material... [All] changing electro-

> magnetic fields are exactly the same and are described by exactly the same set of equations, Maxwell's Equations... How quickly the electric and magnetic fields can build up is what really determines the speed of the signal... [Maxwell's Equations] say that if the electric and magnetic fields ever change, the kink they make will propagate outward at a speed that depends on some constants and material properties.

Accordingly, the time delay per unit length, TD_L, is given by [33]

$$TD_L = \frac{1}{v} = \sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r} \tag{5.1}$$

where ε_0 = permittivity of free space = $8.89\times10^{-12} F/m$, ε_r = relative dielectric constant of the material = 3.9 (value for silicon dioxide used in this study), μ_0 = permeability of free space=$4\pi\times10^{-7} H/m$, and μ_r = relative permeability of the material=1 (for most materials). Therefore, if the relative permittivity of the material decreases, the electric fields can change more rapidly, causing the signal to propagate at higher speeds in the medium. Decreasing the magnetic permeability would have the same effect, but there are not many materials with different permeabilities.

Figure 5.1 through Figure 5.6 show the waveforms of lossless and lossy transmission line simulations of different lengths. The following lossless transmission line simulations include a CMOS driver, transmission line, and a dynamic receiver (refer to section 4.3 for more details). Figures 5.1, 5.3, and 5.5 each have two plots. Both plots have the input voltage which is attached to the gate of the driver. The lower subplot, the receiver input, is the node at the end of the transmission line attached to a minimum sized inverter. The upper subplot, the receiver output, is the node at the output of the minimum sized inverter. All the simulations were done in spice using the IBM CMOS10SF BSIM models.

Figures 5.2, 5.4, and 5.6 show transmission line systems with the lossy transmission line model for similar interconnect lengths as the lossless simulations. The lossy transmission lines were modeled at a much lower frequency than the lossless

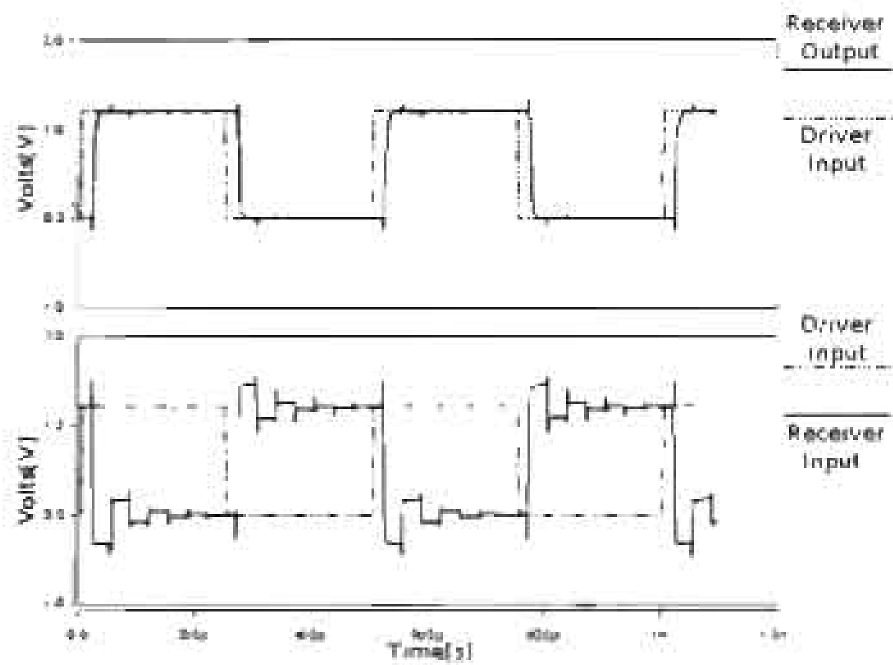

Figure 5.1 2500μm transmission line (lossless) spice simulation

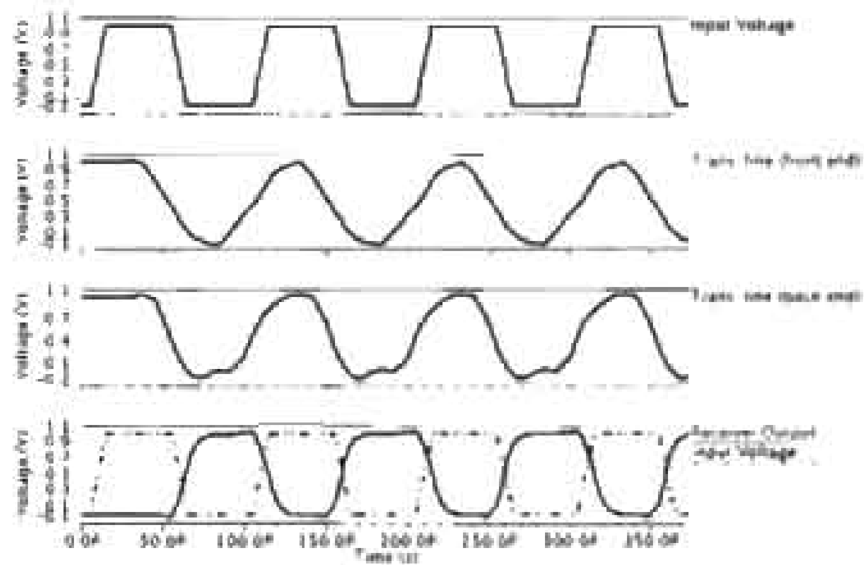

Figure 5.2 1000μm transmission line (lossy) spice simulation

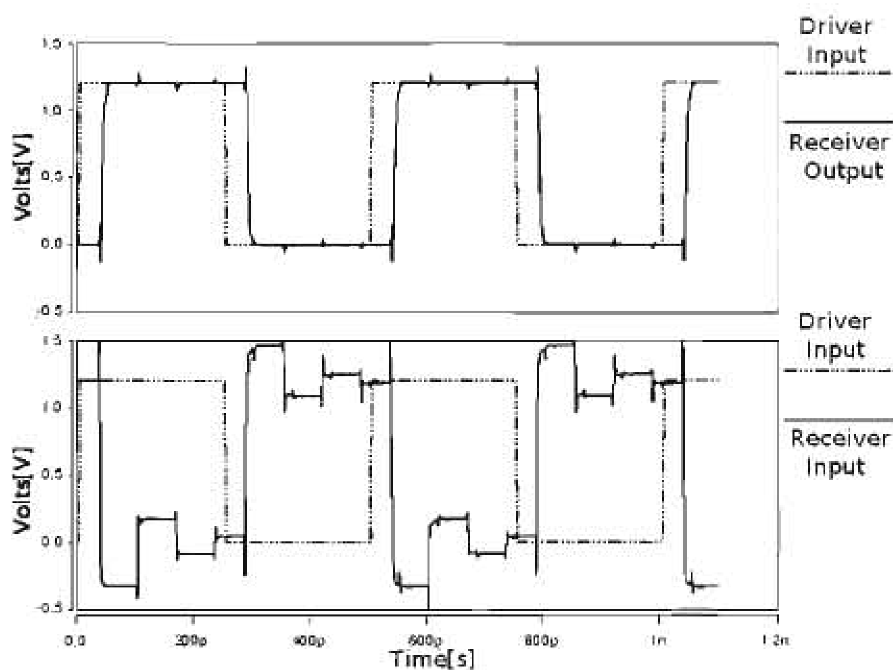

Figure 5.3. 5000μm transmission line (lossless) spice simulation

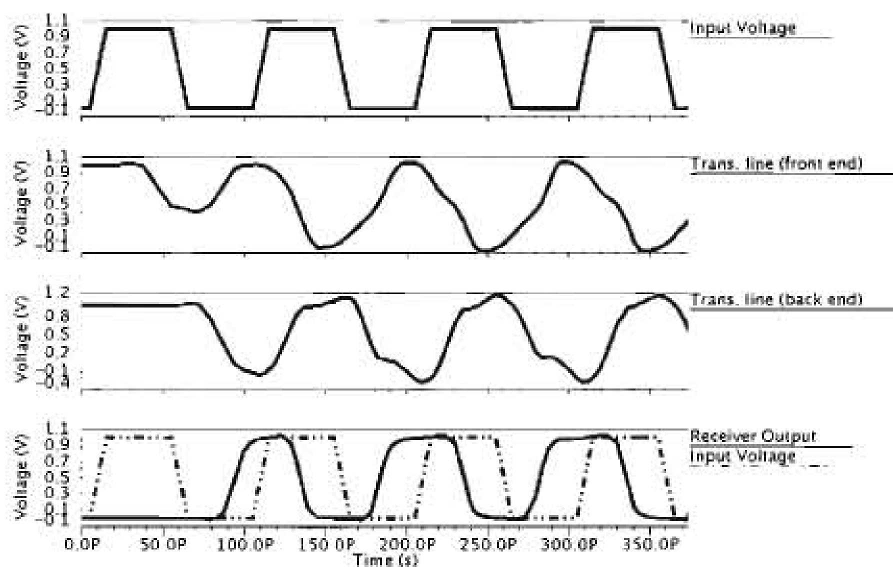

Figure 5.4. 5000μm transmission line (lossy) spice simulation

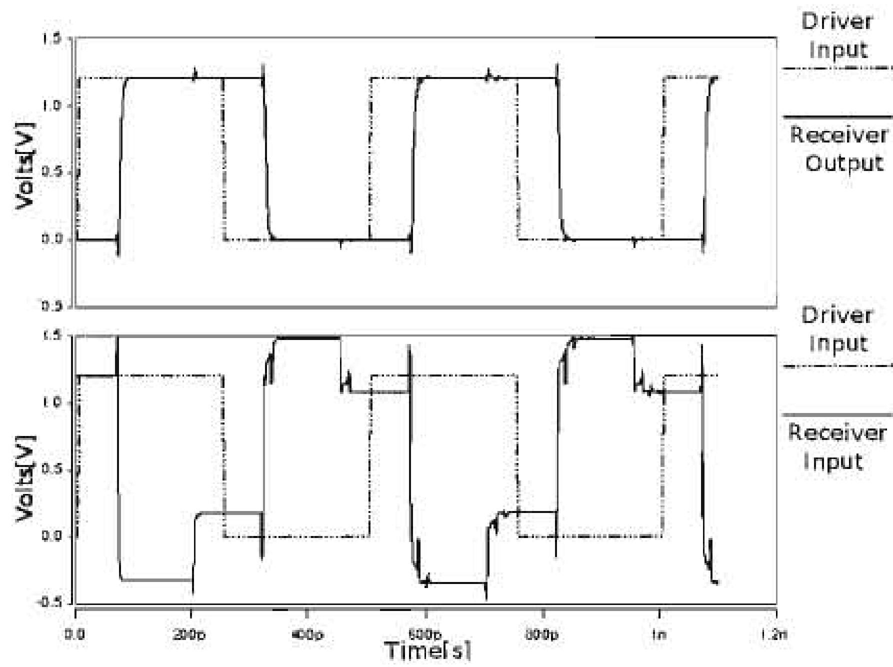

Figure 5.5. $10000\mu m$ transmission line (lossless) spice simulation

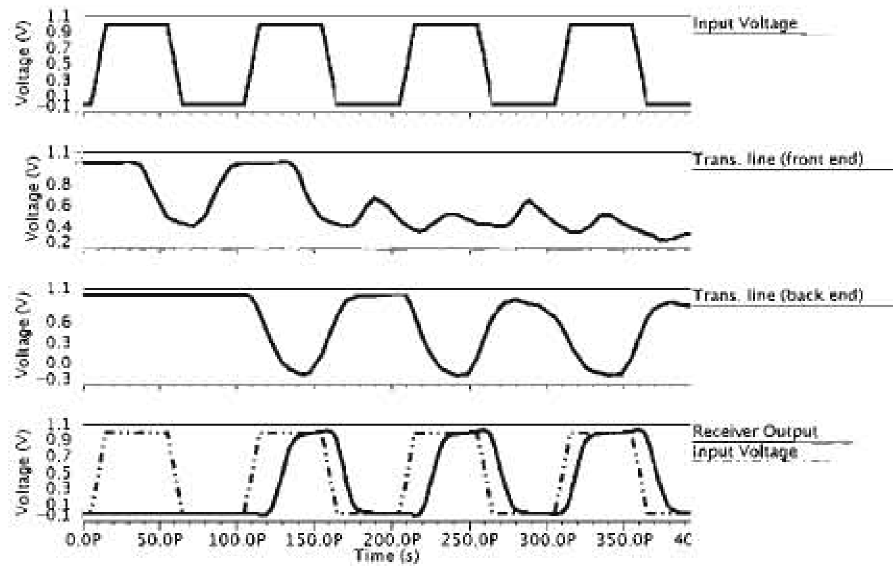

Figure 5.6. $10000\mu m$ transmission line (lossy) spice simulation

transmission lines. The lossless lines were modeled at a frequency much greater than the maximum frequency permitted by the FO4 delay for the process. Therefore, the lossy transmission lines were modeled at more realistic frequencies for the process and include the buffering circuitry connected to the driver. For lossy transmission lines, overshoot was no longer a major concern. Also, V_{DD} was changed from 1.2 V to 1.0 V in order to more accurately reflect the voltage for the process.

Furthermore, transmission line propagation requires that the rise and fall times of the driver are less than the twice the time of flight for the signal. This ensures that there is enough time for the incident wave to travel to the end of the line and for the reflected wave to return to the driver. Below this minimum transmission line length, the transmission line interconnect starts to act more like a low resistance diffusive wire with a strong driver. Assuming a rise time, τ_r, of 10 ps, the minimum transmission line length, L_{min}, the signal can travel is

$$L_{min} = \frac{\tau_r}{2\sqrt{LC}} \tag{5.2}$$

where L and C are the inductance and capacitance per unit length, respectively. This results in L_{min} of 650 μm.

5.1 Transmission Line Simulation Results

The transmission line simulation setup consisted of a buffer, a driver, a transmission line with $Z_o = 50\ \Omega$, a dynamic receiver with 40 mV hysteresis, and a load equal to 5x the size of a minimum inverter. The buffer and driver were conventional MOSFETS (neither were annular). The dynamic receiver was initially chosen and used in these simulations due to its performance and hysteresis levels. Later, the jam latch was deemed to be a better choice. Since changing the receiver only made a small difference in the overall system performance, the simulations were not repeated with the jam latch receiver (refer to section 4.3 for more information on the transmission line receiver studies).

All the transmission line simulations were done at frequencies of 1 GHz and 10 GHz. Since the transmission line parameters are length and frequency dependent, a unique transmission line was designed for every length and frequency pair. This assured the highest degree of accuracy for the simulations. Appendix A lists the values of these transmission line parameters. Both frequencies (1 GHz and 10 GHz) used the same rise and fall times of 10 ps for the initial prebuffered input. Buffering the signal provided a good way to model more realistic rise and fall times to use as inputs for the transmission line drivers.

5.1.1 Latency

The rise and fall times for all of these simulations are the amount of time required for the receiver output (which is connected to the load) to swing from 10% to 90% V_{DD}. These results are shown in Figures 5.7 through 5.10. The latency is measured at the receiver output so that the total system response is observed. The propagation delay is the amount of time required for the input voltage (before any buffering) to cause the receiver output to change. These results are shown in Figures 5.11 through 5.14. The propagation delay is dependent on the speed of the buffers, drivers, receivers, and line lengths. This delay did not change for the 1 GHz and 10 GHz case. The difference in frequency came from reducing the time the signal remained high and low.

5.1.2 Power

The power consumption was measured by finding the root mean square (rms) current over two clock cycles once the system is in a steady state and multiplying this value by V_{DD}. For the 1 GHz case, the power increased logarithmically with the length of the line (see Figure 5.15). On the other hand, the 10 GHz transmission line reaches a maximum for a length slightly less than 4000 μm, decreases, and increases again to the same maximum value (see Figure 5.16). The power consumption is periodic, behavior not observed with the 1 GHz input. The most likely cause for this effect is standing waves. These waves are caused by the superposition of the incident and reflected waves moving in opposite

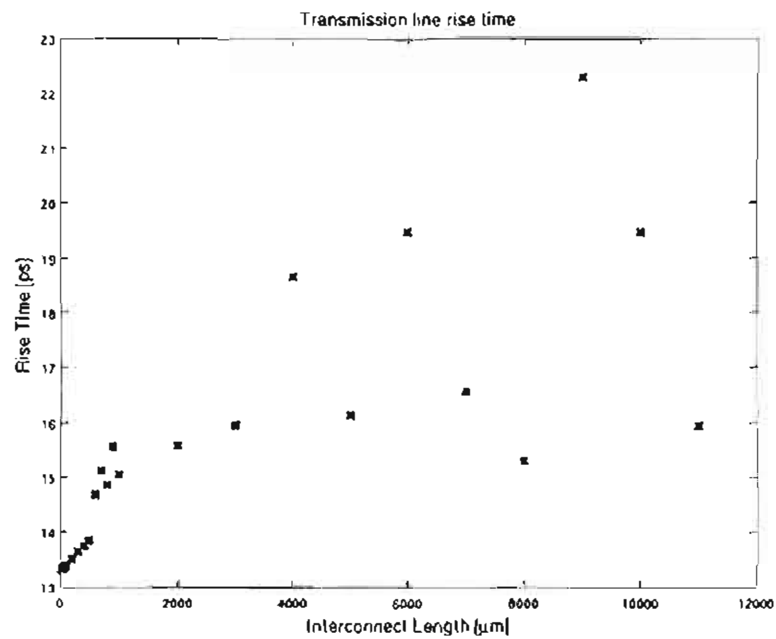

Figure 5.7. Transmission line rise times (1 GHz)

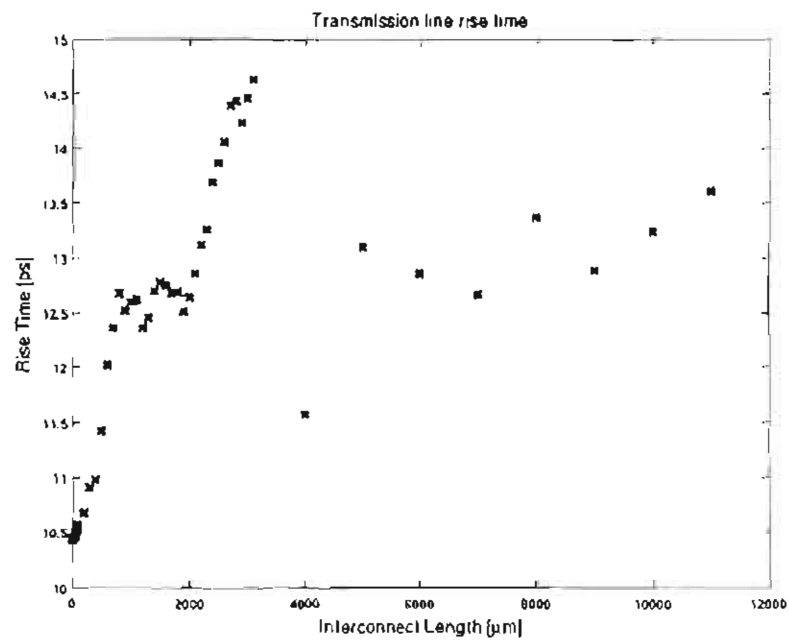

Figure 5.8. Transmission line rise times (10 GHz)

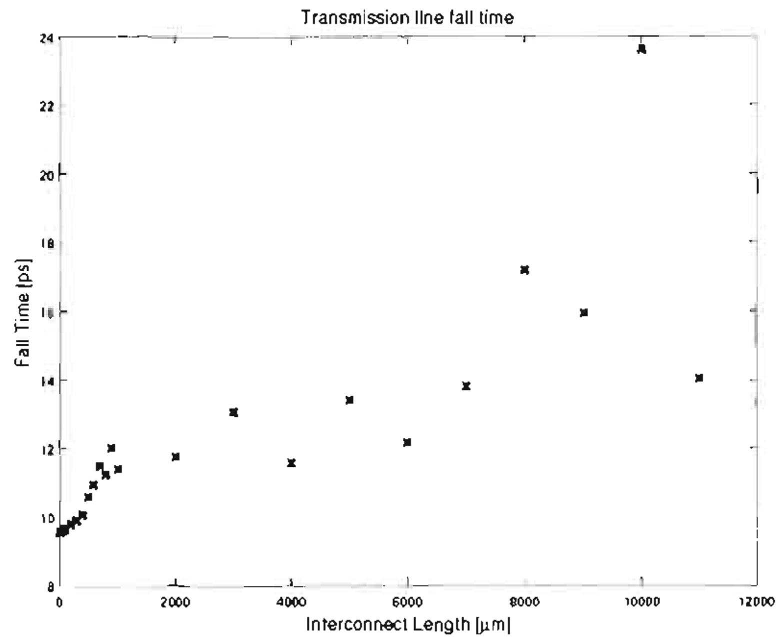

Figure 5.9. Transmission line fall times (1 GHz)

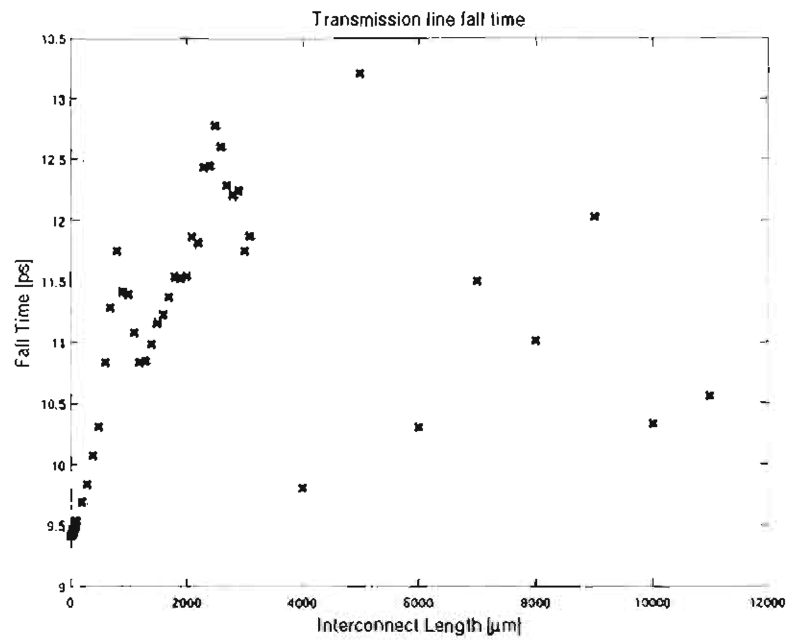

Figure 5.10. Transmission line fall times (10 GHz)

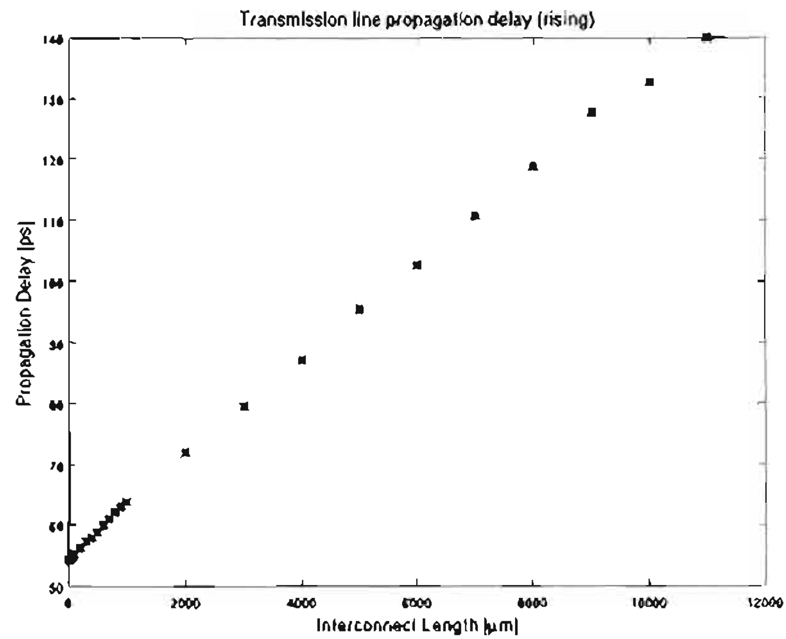

Figure 5.11. Transmission line propagation delay (rising) (1 GHz)

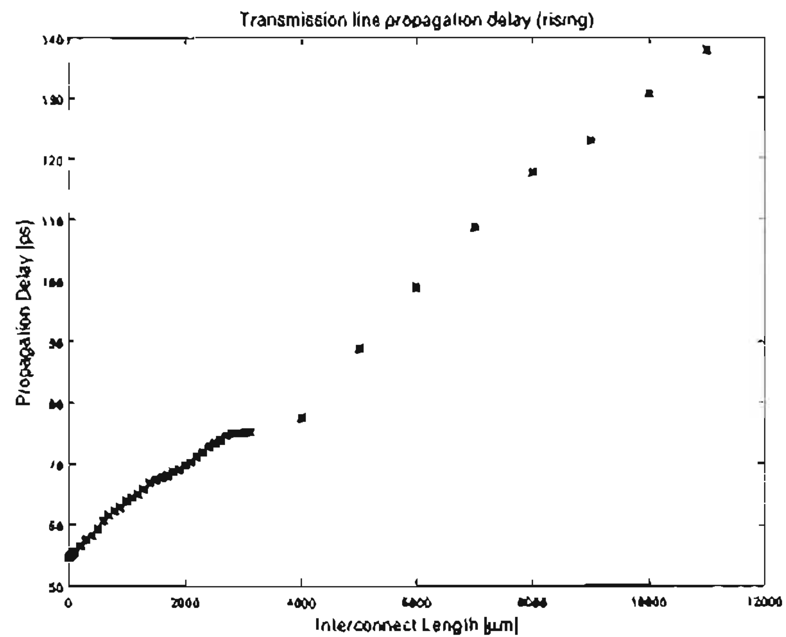

Figure 5.12. Transmission line propagation delay (rising) (10 GHz)

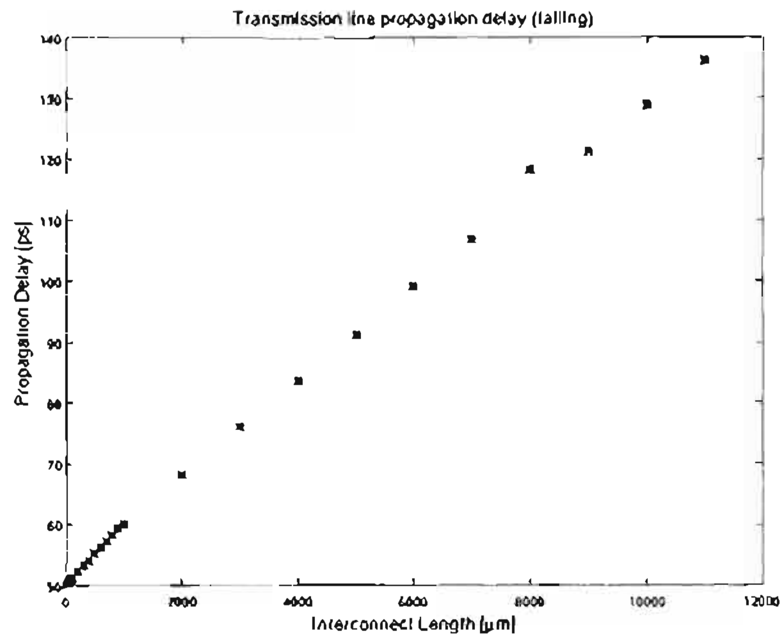

Figure 5.13. Transmission line propagation delay (falling) (1 GHz)

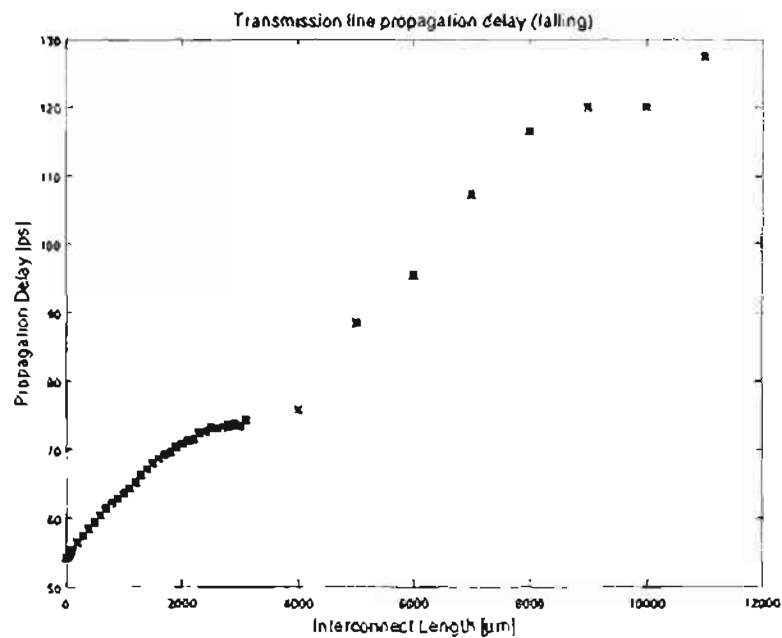

Figure 5.14. Transmission line propagation delay (falling) (10 GHz)

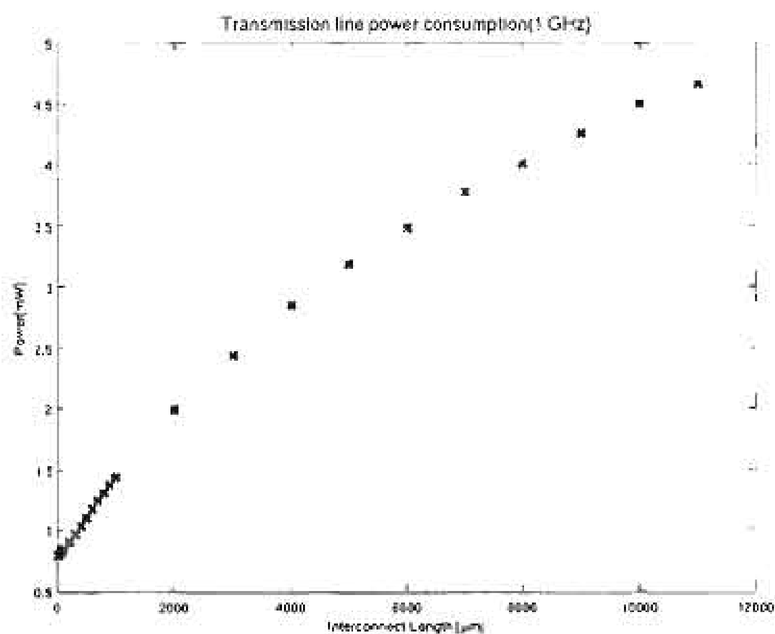

Figure 5.15. Transmission line power consumption (1 GHz)

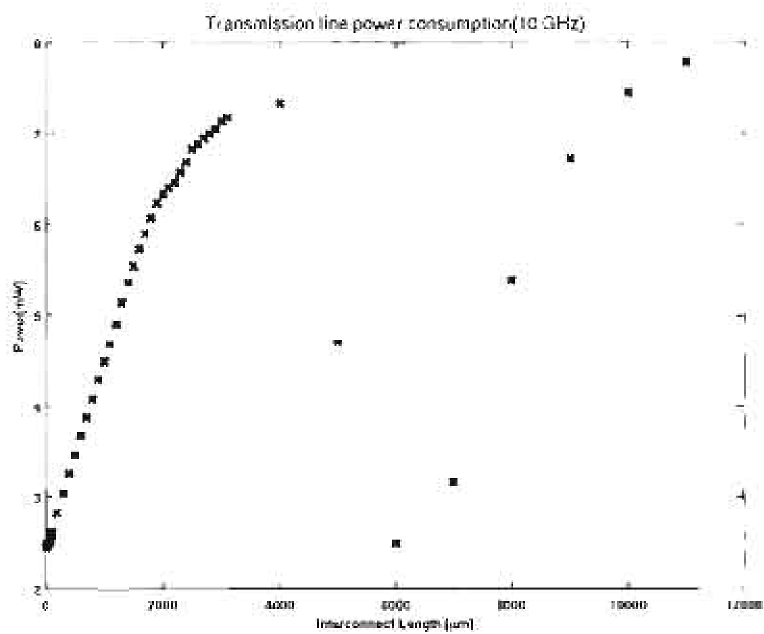

Figure 5.16. Transmission line power consumption (10 GHz)

directions. At certain places on the transmission lines, there are nodes with minimal displacement and maximal displacement. Standing wave effects become noticeable when the length of the line is of a similar magnitude as one fourth the wavelength, $\lambda/4$. For line lengths equal to odd multiples (i.e., 1, 3, 5, ..., $2n + 1$) of $\lambda/4$, there is maximal displacement at the end of the line; the driver and the transmission line attempt to force a large voltage swing at the end of the line. For line lengths equal to even (i.e., 2, 4, 6, ..., $2n$) of $\lambda/4$, there is minimal displacement at the end of the line.

The speed of light in the transmission lines is equal to [34]

$$v = \frac{1}{\sqrt{LC}} \tag{5.3}$$

where L and C are the inductance and capacitance per unit length, respectively. The ratio of L and C is set for each characteristic impedance and is independent of length. Using the parameters from Appendix A, the speed of light in a 50 Ω transmission line is

$$L = 0.387\mu H/m \tag{5.4}$$

$$C = 154.7pF/m \tag{5.5}$$

$$v = 1.292\times10^{8}m/s = 129\mu m/ps \tag{5.6}$$

The wavelength of the signal is given by

$$\lambda = \frac{v}{f} \tag{5.7}$$

For the speed of light in the medium and a frequency of 10 GHz, λ is 12,900 μm and $\lambda/4$ is 3200 μm. This value corresponds well with Figure 5.16. The figure, however, only shows data points for 3000 μm and 4000 μm. Additional data points within this range should show that the power reaches a maximum value at this

point and tapers off. Furthermore, a power minimum is expected at $\lambda/2$ at 6400 μm. The closest data point at 6000 μm shows a minimum in the power.

Although the $\lambda/4$ wavelengths affected power consumption, it also affected the amount of overshoot on the transmission line (see section 5.1.3). Therefore, the receiver must be able to tolerate the extra overshoot (which reached a maximum of 25% V_{DD}).

The 1 GHz signal did not have the same problem due to the large wavelength of the signal; its wavelength is one order of magnitude larger. The first length equal to $\lambda/4$ and a corresponding power maximum would be at 32000 μm. In practice, transmission lines this long are not feasible due to the high amount of loss.

5.1.3 Overshoot and Noise Tolerance

The lossless transmission lines are very sensitive to overshoot. Observing the waveforms (see Figure 5.1, Figure 5.3, and Figure 5.5) shows that the overshoot can be more than 25% V_{DD}. There is no resistance in the line to attenuate the signal or attenuate reflections. The more accurate lossy models do not have this same problem (see Figure 5.2, Figure 5.4, and Figure 5.6). Additionally, the waveform outputs for the lossy lines are very clean without ringing. One concern about the transmission line system is large ringing caused by reflections from impedance mismatches. This ringing can cause glitches in the output. Therefore, no ringing is a very good sign for the transmission line system. To measure the amount of overshoot at different parts of the transmission line system, the maximum and minimum voltages were measured at both ends of the transmission line, as shown in Figures 5.17 through 5.20. The maximum voltages give the overshoot above V_{DD}, and the minimum voltages give the overshoot below ground.

Similar to the diffusive wires, sending the signal through various logic gates limits the effect of steady state noise to the system. The transmission line DC sweeps showed almost exactly the same behavior, as seen in Figure 3.13.

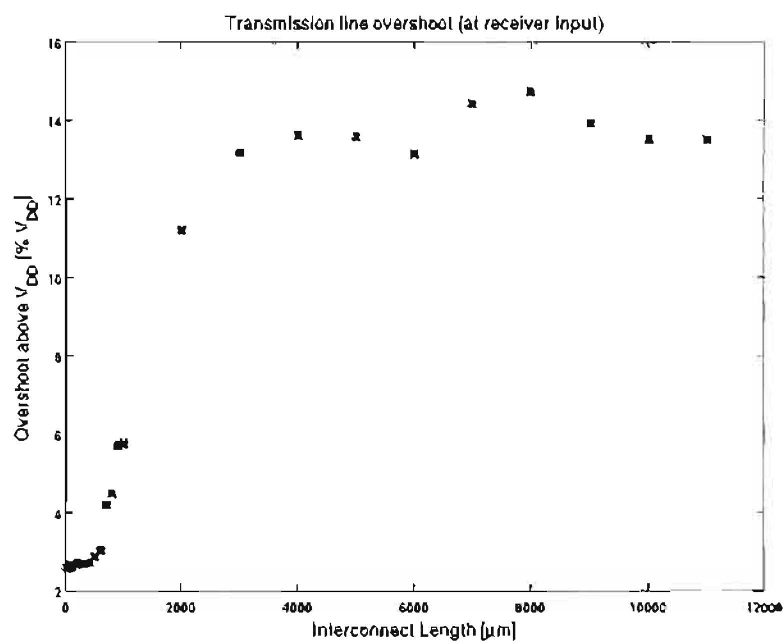

Figure 5.17. Transmission line overshoot - backend(above V_{DD}) (1 GHz)

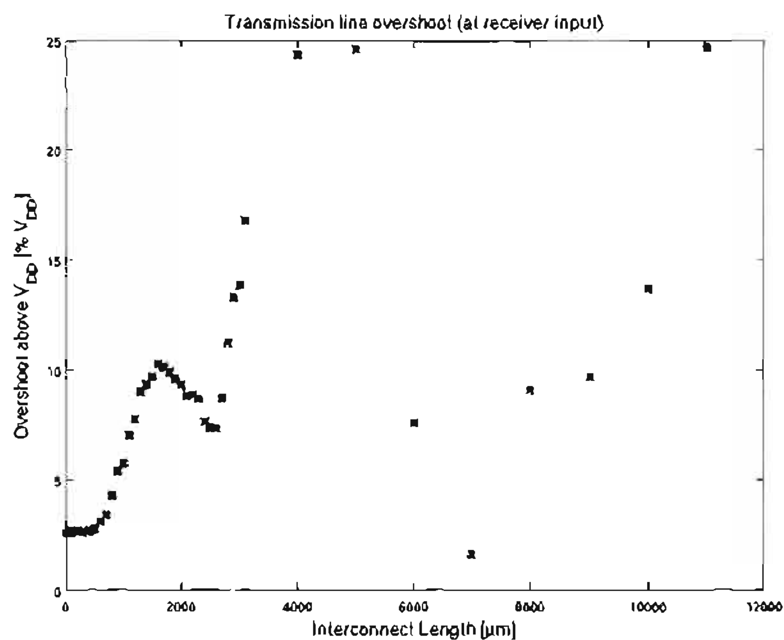

Figure 5.18. Transmission line overshoot - backend (above V_{DD}) (10 GHz)

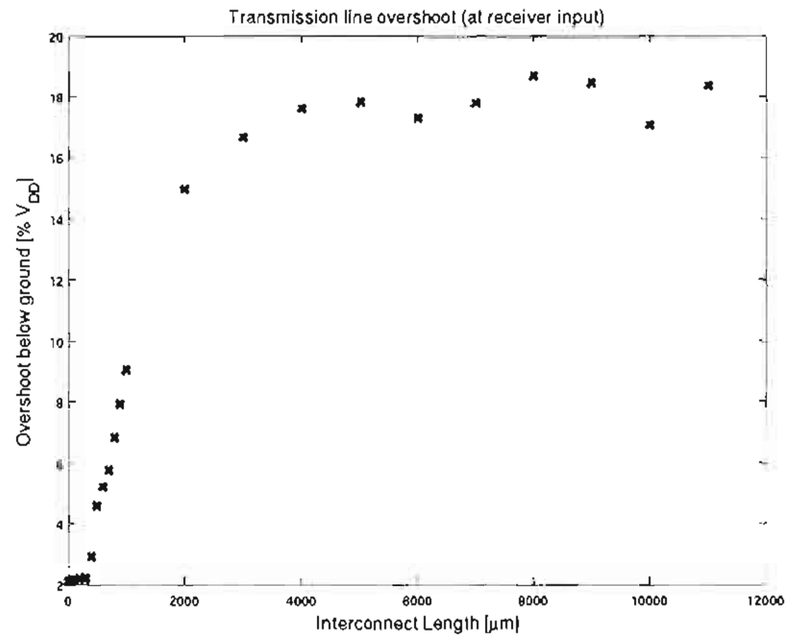

Figure 5.19. Transmission line overshoot - backend (below ground) (1 GHz)

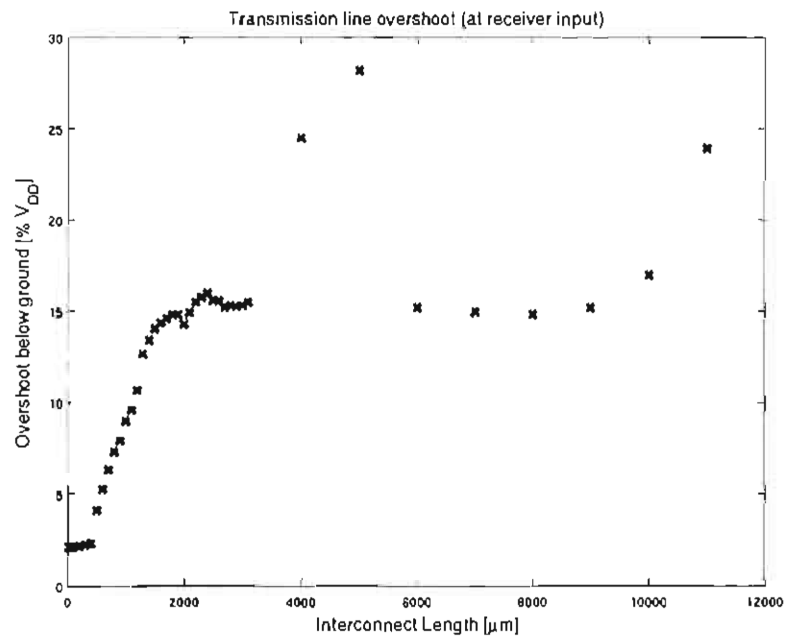

Figure 5.20. Transmission line overshoot (below ground) (10 GHz)

5.2 Area Requirements

Since transmission lines operate by sending changing electric and magnetic fields, they do not require repeaters like the diffusive wires (repeaters may be necessary, however, to change direction 90°). The spice simulations show that none of the transmission lengths tested required repeaters; they were not added into any of the transmission line simulations. As the transmission lines become longer, however, there are more problems with reflections and waiting for the reflections to affect the line output. Adding repeaters to the transmission lines would reduce the noise but would require more power and would add a small amount of delay. The silicon area for the total transmission line system consists of the buffer, the driver, the receiver, and the load. The same circuitry is used for all the transmission line systems so the silicon area is independent of the interconnect length. The silicon area is 26.31 μm^2 for all lengths. This is roughly equal to the amount of silicon necessary for a diffusive line 1000 μm long.

The metal wires and spacings for the transmission line require wider regions for the transmission lines themselves. The total width is the amount of width required for the signal wire, the two ground wires, and the two spacings between the ground and signal wires. The total width varies widely with the length of the line, frequency, and desired characteristic impedance; it can be anywhere from 1 μm to 30 μm. For most applications, one of the narrower (1 to 10 μm total widths) areas can be used. Bus signals require the two return paths and the signal path to ensure that the RLC parameters are correct; it may be possible to share return paths, but this requires further research. Forking has more stringent impedance matching requirements; it needs some wider lines (20 - 30 μm total widths) to achieve the high impedances necessary. Appendix A shows the actual values of these dimensions.

5.3 Transmission Line Forks

A transmission line fork refers to connecting a single transmission line to two perpendicular transmission lines. This creates a "T" shape at the location of the

fork. In order to minimize fork reflections and maximize the energy transmitted, the impedances must be matched on both sides of the fork. Since the two attached lines are in parallel, the combined impedance is the parallel combination of the impedances of the attached lines. Assuming identical lines, the impedance of the two lines in parallel is one half the characteristic impedance of each line. Therefore, in order to match the impedance, the attached lines must have twice the impedance of the initial line.

Lower characteristic impedances implies higher capacitance and lower inductance per unit length of the line as demonstrated by equation (4.6). The capacitance can be increased by decreasing the spacing of the line. The maximum capacitance and thus the minimum characteristic impedance is set by the design rules for minimum spacing between the metals; for the 2x thick copper layers under investigation, the minimum spacing is 0.20 μm (see layers BA, BB, BD-BG in Table 2.1). This corresponded to a minimum realizable characteristic impedance of $\sim$ 35 Ω. Even if lower impedance lines were possible, the drivers may not be able to drive them anyway. Higher characteristic impedance implies the opposite: higher inductance and less capacitance per unit length. The main way to reduce the capacitance is to increase the spacing between the signal and ground wires. In terms of modeling the transmission lines and not breaking design rules, there is not an upper bound to the characteristic impedance. For an actual integrated circuit, however, several factors limit the maximum spacing and the maximum impedance possible. First, wide spacings mean that the transmission lines will be very area expensive. The minimum pitch wires will be 0.20 μm. If a transmission line system requires 30+ μm to realize a specific impedance, there may not be enough space for it. Second, even if there is space on the metal layer of interest for the transmission line, wide spacings would make the capacitance and inductance of the transmission line more coupled to metal traces on other layers. Therefore, very wide lines require the designer to verify that other metal layers do not significantly affect the LC parameters of the line.

The range of possible impedances dictates the number times a transmission

line can be forked. More forks means that the signal can be sent to more places without repeaters. Due to the range for the metal layers, the maximum number of forks is two with the following transmission line impedances: 35 Ω, 70 Ω, and 140 Ω. For a single fork, any impedance between 35Ω and 70Ω can be used with its double. The main application of forking would be for a clock distribution network or broadcast signals to different die locations. These networks need to be able to cover an area of 1 cm^2 area. The first simulation consisted of a 10000 μm transmission line with $Z_o = 50\Omega$ connected to two transmission lines that are 5000 μm long with $Z_o = 100\Omega$. The resulting waveforms are shown in Figure 5.21. The buffer, driver, receivers, and loads were all exactly the same as for the transmission line simulations without forks. For an input frequency of 10 GHz, the output waveforms were very clean without attenuation. The internal nodes are very noisy but this does not affect the output. For two forks, there was attenuation that was independent of line length except for very short lengths ($\sim$ 100 μm legs) when the input frequency was 10 GHz. Slowing down the frequency to 8 GHz removed most of the attenuation, as shown in Figure 5.22.

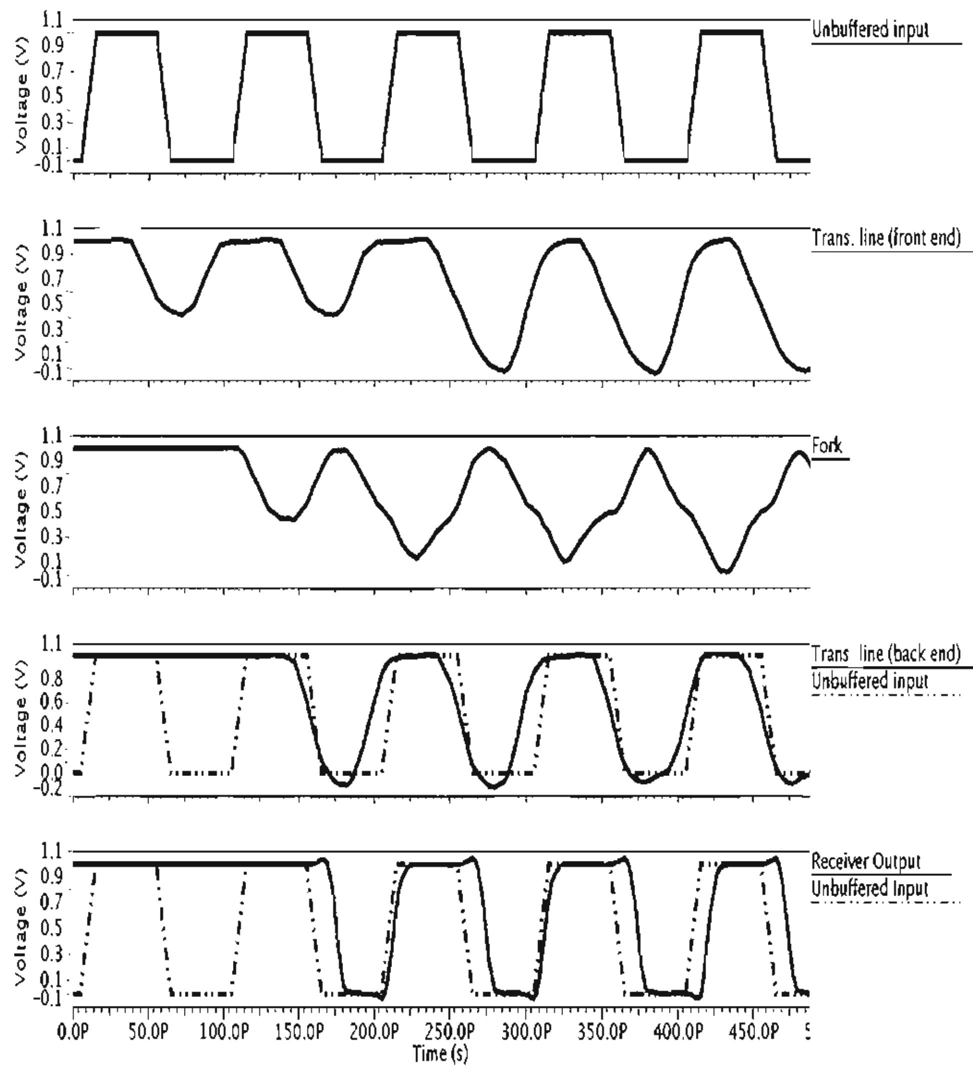

Figure 5.21. Waveforms for transmission line with single fork

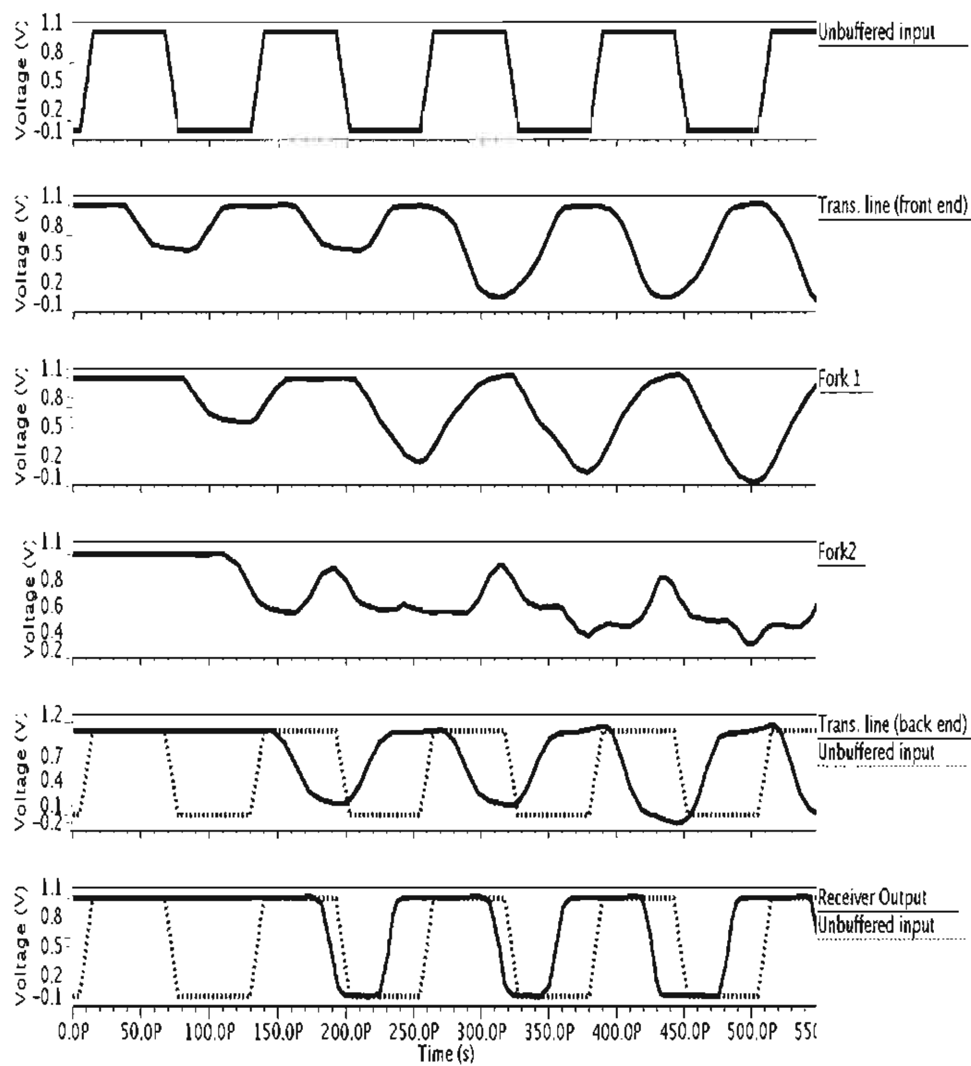

Figure 5.22. Waveforms for transmission line with two forks

CHAPTER 6

COMPARISONS: TRANSMISSION LINES VS. DIFFUSIVE WIRES

One of the main purposes of this thesis is to compare the tradeoffs between diffusive wires and transmission lines. This section reproduces data already presented. However, the results for the diffusive wires and transmission lines are placed on the same figures to permit easier comparisons.

The simulations for both the diffusive wires and the transmission lines are set up to be as equal as possible. Both sets include signal buffering that consists of two inverters connected in series. Both sets have a driver attached at the beginning of the interconnect. At this point, the diffusive wires simulations have minimum pitch wires with optimally sized and spaced repeaters. The transmission line interconnects consist of coplanar transmission lines with a characteristic impedance of 50 Ω designed for the particular frequency and length of the line. After this point, both are attached to a receiver which is attached to a load 5x the size of a minimum sized inverter for the process. The load is roughly 1/5 the size of the output stage of the jam latch receiver and 1/10 the size of the output stage of the CMOS receiver. Although the number of logic stages (not including repeaters for the diffusive wires) is the same for both sets of interconnect, the sizings are not.

Due to the frequency limits of the diffusive wires, they were only simulated at 1 GHz. The transmission lines were also tested at 1 GHz. Since they have many advantages with increasing frequency, the transmission lines were also tested at 10 GHz. Both input signals (the 1 GHz and 10 GHz) have rise and fall times equal to 10 ps.

In order to truly act as a transmission line, the transmission line length should not be less than the half the distance the signal can propagate in the medium

during the driver rise or fall time. Assuming 50 Ω transmission lines and 10 ps rise and fall times, this minimum length is 646 μm. Below this length, the signal propagation is controlled by a combination of *RC* and *RLC* effects. Therefore, very short transmission lines (below 500 μm) act more like diffusive wires with low resistance wires and a strong driver than a transmission line interconnect.

6.1 Propagation Delay

In terms of rise times, fall times, and propagation delays, the transmission lines thoroughly outperformed the diffusive wires for longer interconnects. The propagation delay is the time it takes for a switching event on the prebuffered input to switch the receiver output. Already for interconnects that are 300 μm long, the transmission lines outperform the diffusive wires, as shown in Figures 6.1 through 6.8. The length where the transmission line performance surpassed the diffusive wires was relatively constant on the frequency range of 1 GHz to 10GHz.

6.2 Power and Energy Consumption

Figures 6.9 through 6.16 compare the power and energy consumption of the diffusive wires and the transmission lines. Operating at the same frequency of 1 GHz, the transmission lines consume slightly less power for lengths greater than 400 μm (Figure 6.9) and much less power as the line length passes 5000 μm. Increasing the frequency by a factor of 10x increases the power consumption by a factor less than 10x; this can be observed by comparing Figure 6.9 to Figure 6.11.

The energy per bit was calculated to show the higher efficiency of the transmission lines at higher frequencies. For the 1 GHz transmission line simulations, both the diffusive and transmission line interconnects are operating at the same frequency. Therefore, the figures showing the energy per bit looks exactly like the power consumption figures except for changing the units on the axes. For the 10 GHz transmission lines, the power consumption is always higher than the diffusive wires except for a few dips due to standing wave reflections. The energy per bit, however, of the 10 GHz transmission line significantly outperforms the diffusive wires of almost any length (Figure 6.15). This shows the motivation behind using

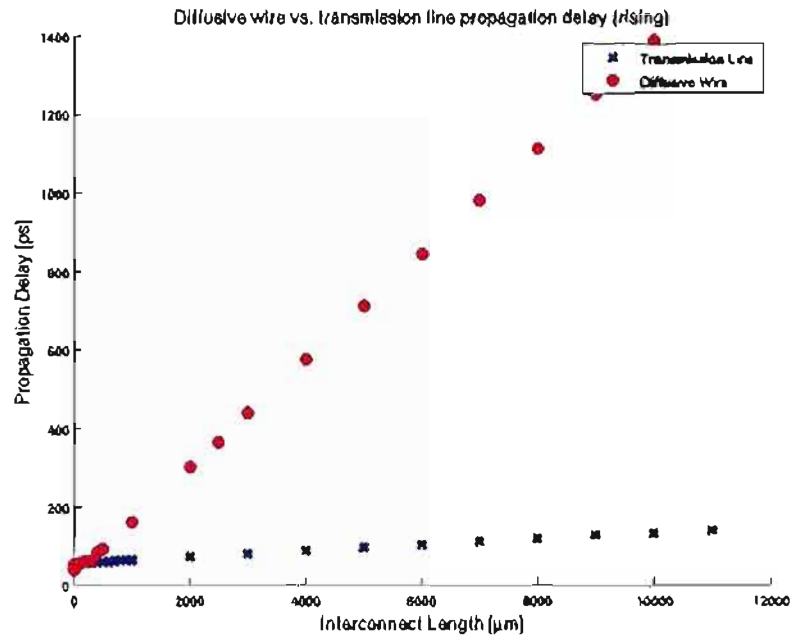

Figure 6.1. Propagation delay comparison (rising)(1 GHz)

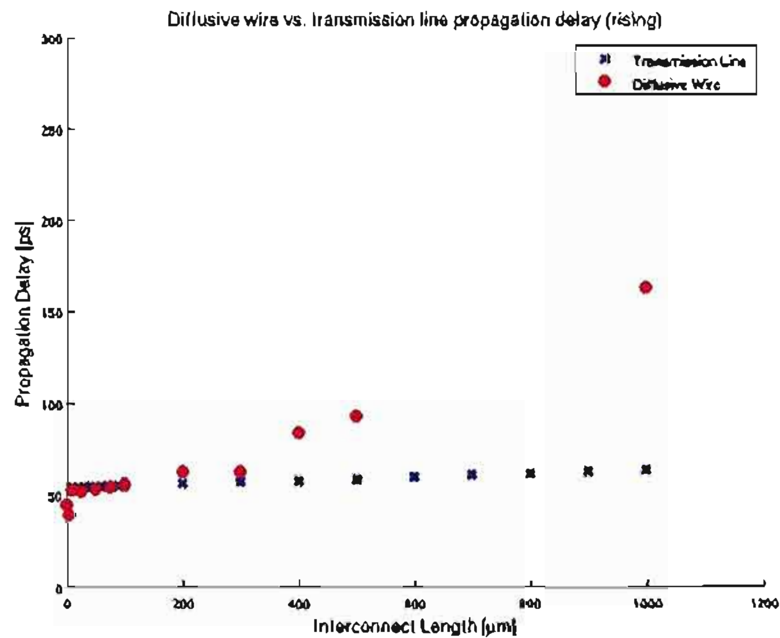

Figure 6.2. Propagation delay comparison (rising)(1 GHz)(short interconnects)

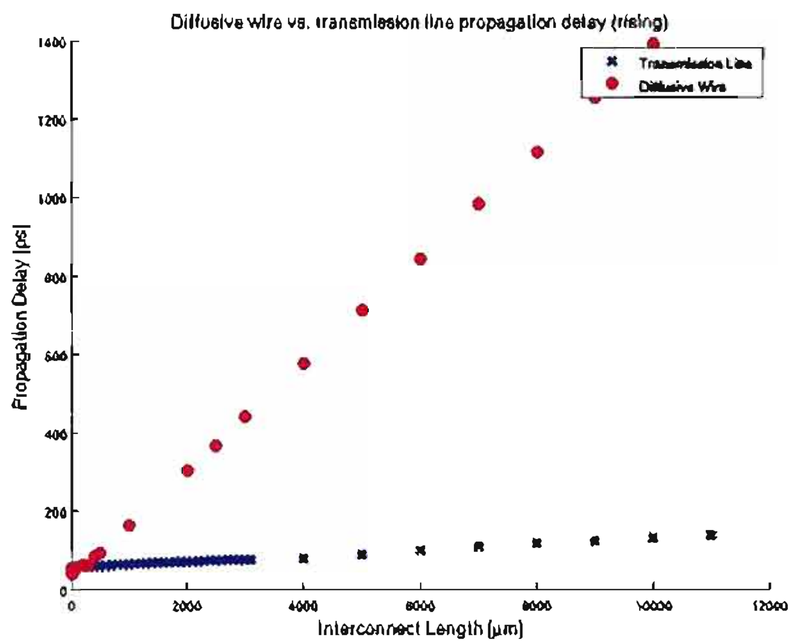

Figure 6.3. Propagation delay comparison (rising)(10 GHz)

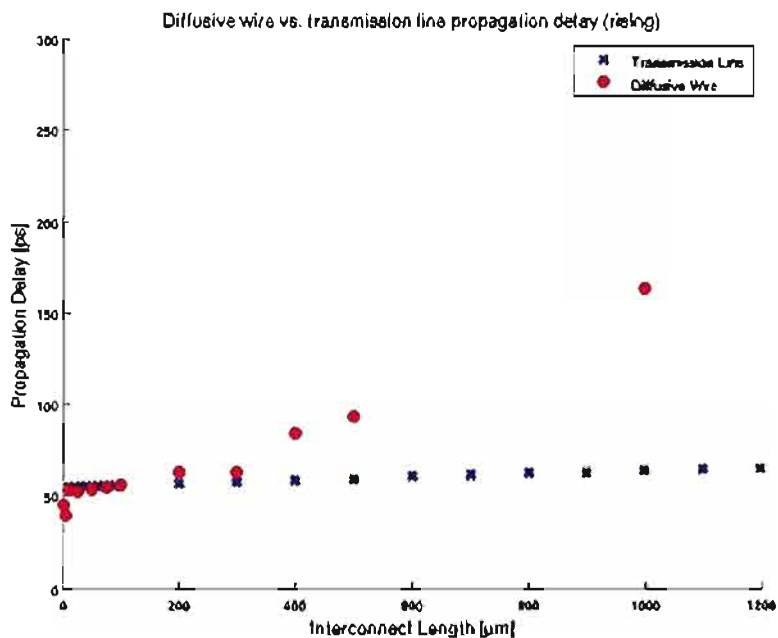

Figure 6.4. Propagation delay comparison (rising)(10 GHz)(short interconnects)

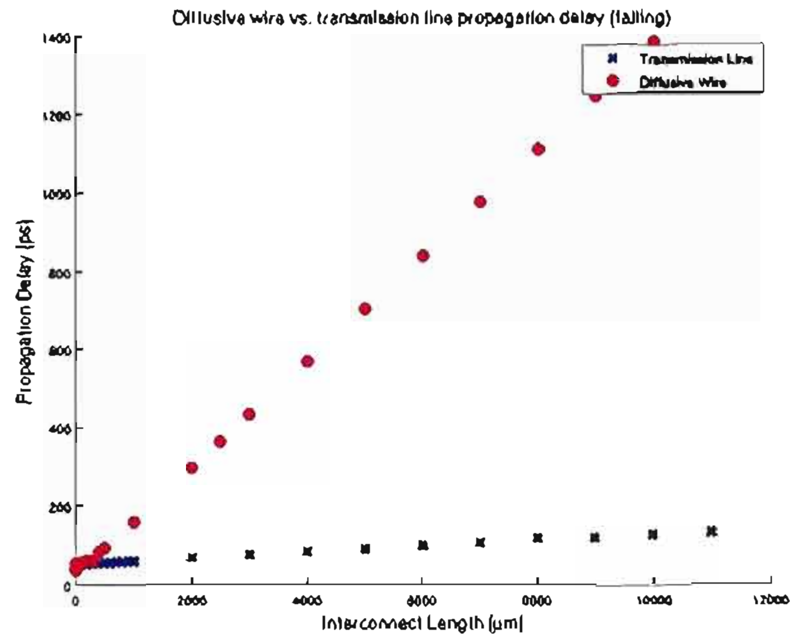

Figure 6.5. Propagation delay comparison (falling)(1 GHz)

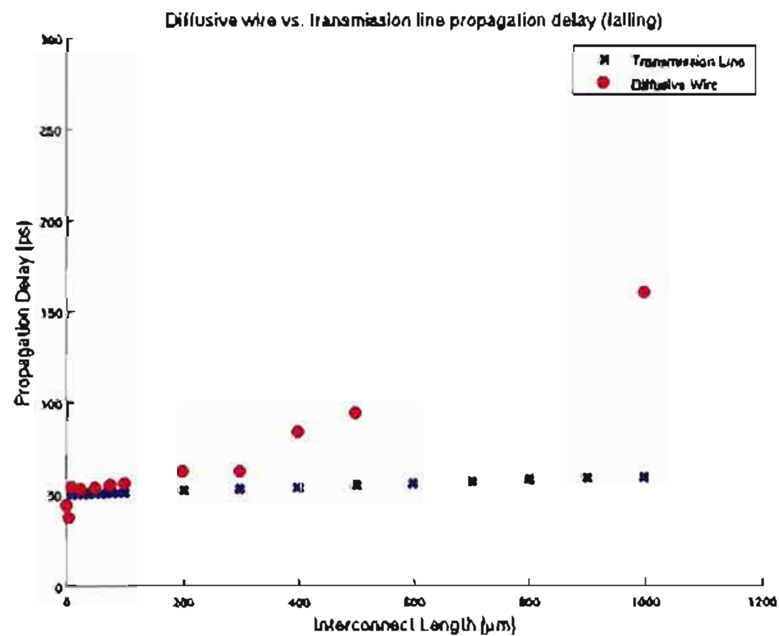

Figure 6.6. Propagation delay comparison (falling)(1 GHz)(short interconnects)

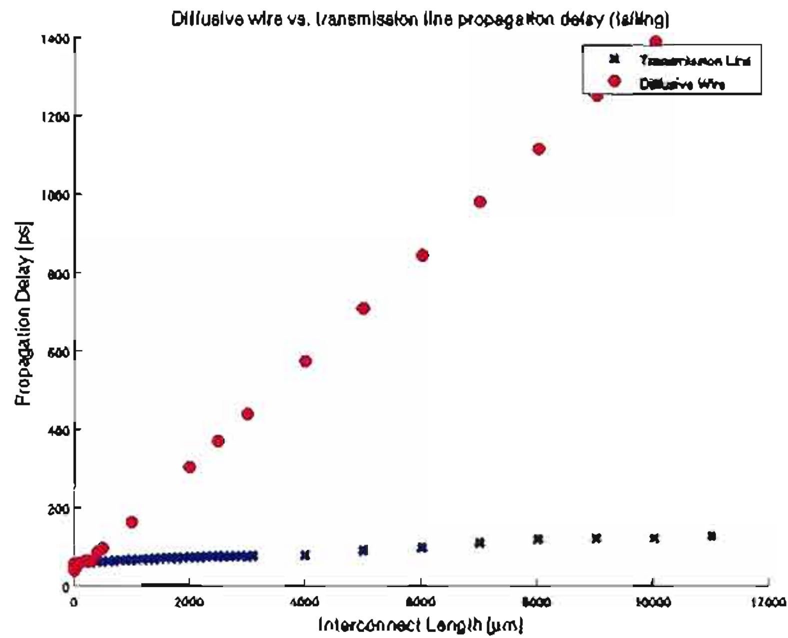

Figure 6.7. Propagation delay comparison (falling)(10 GHz)

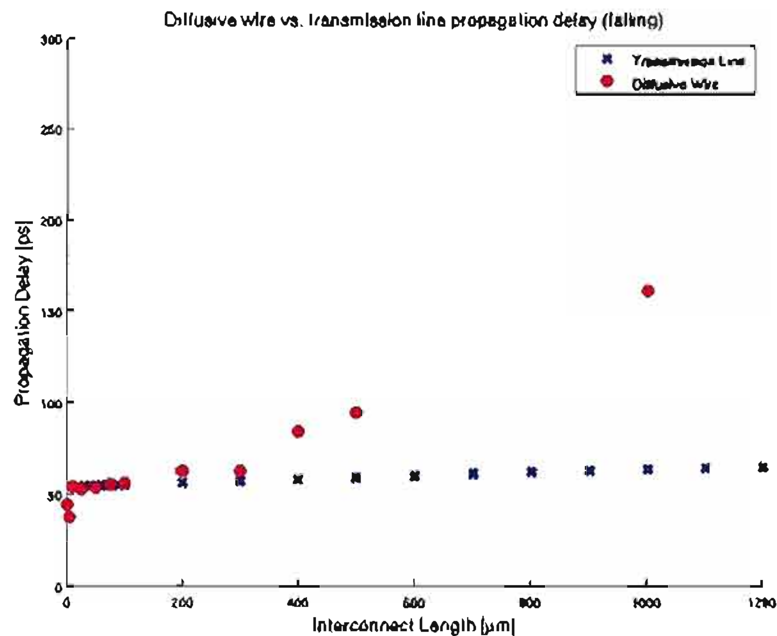

Figure 6.8. Propagation delay comparison (falling)(10 GHz)(short interconnects)

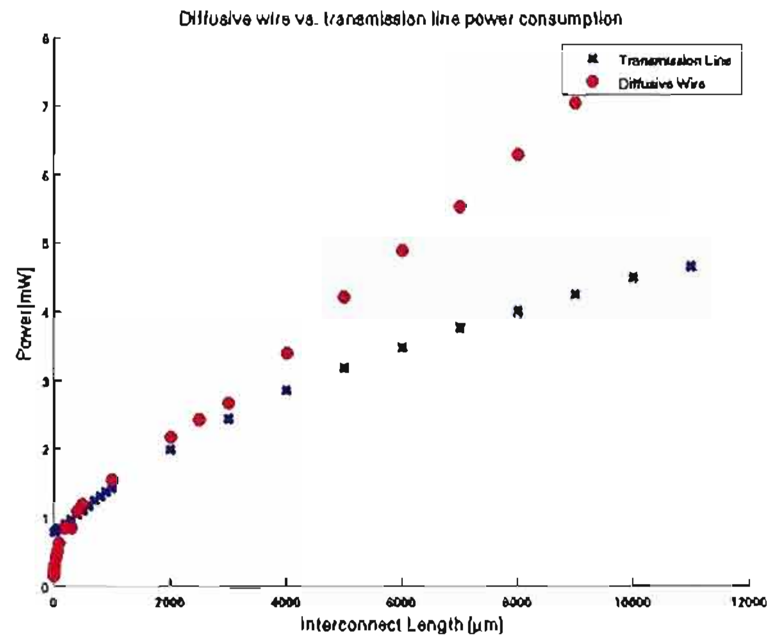

Figure 6.9. Power comparison (1 GHz - Transmission Line)

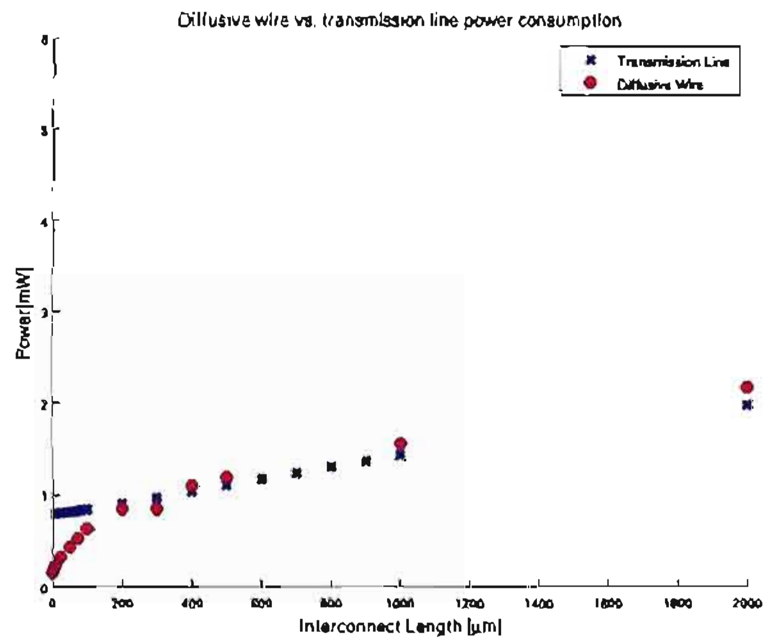

Figure 6.10. Power comparison (1 GHz - Transmission Line)(short interconnects)

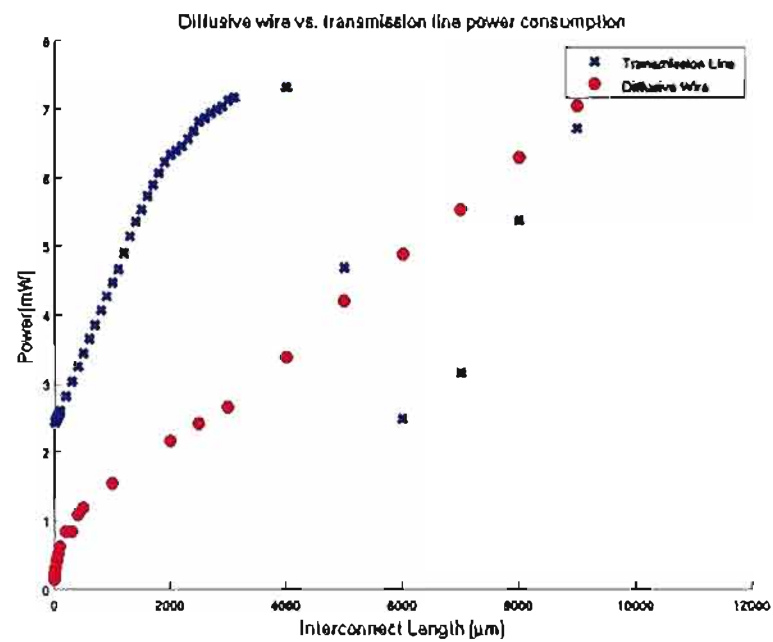

Figure 6.11. Power comparison (10 GHz - Transmission Line)

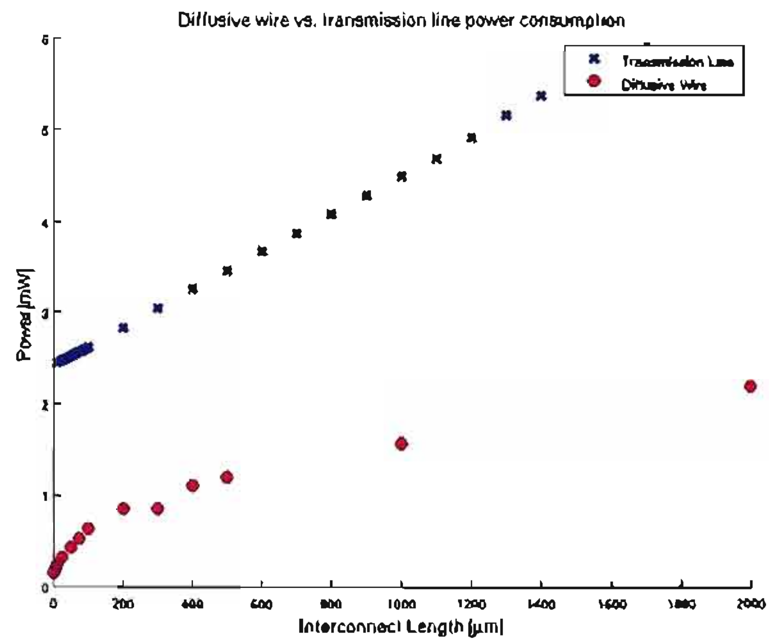

Figure 6.12. Power comparison (10 GHz - Transmission Line)(short interconnects)

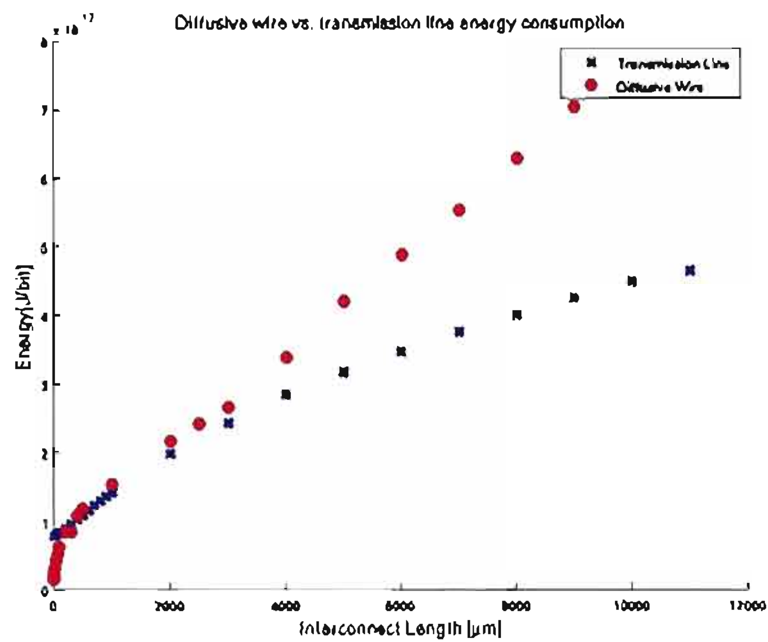

Figure 6.13. Energy comparison (1 GHz - Transmission Line)

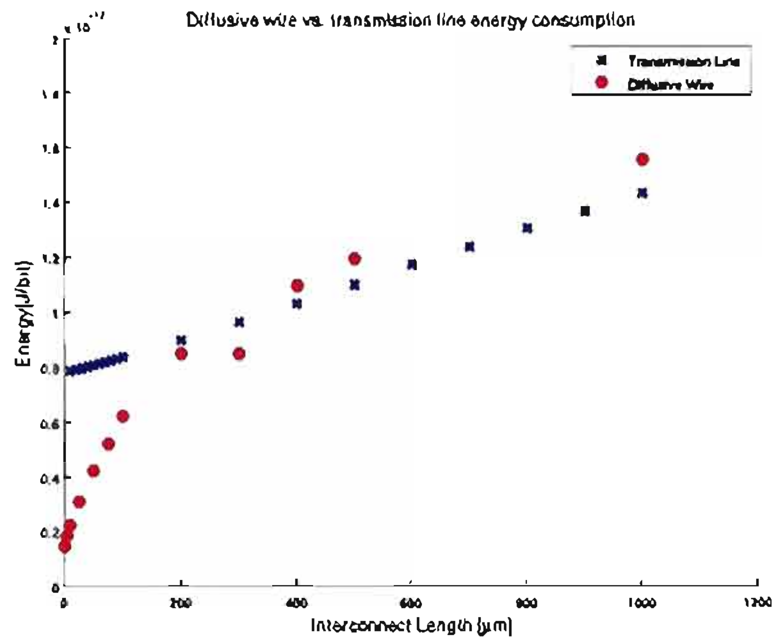

Figure 6.14. Energy comparison (1 GHz - Transmission Line)(short interconnects)

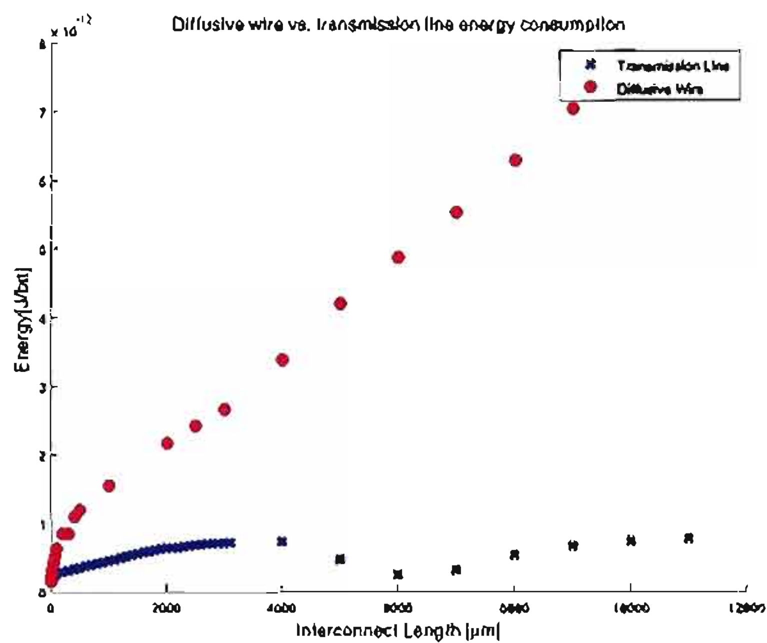

Figure 6.15. Energy comparison (10 GHz - Transmission Line)

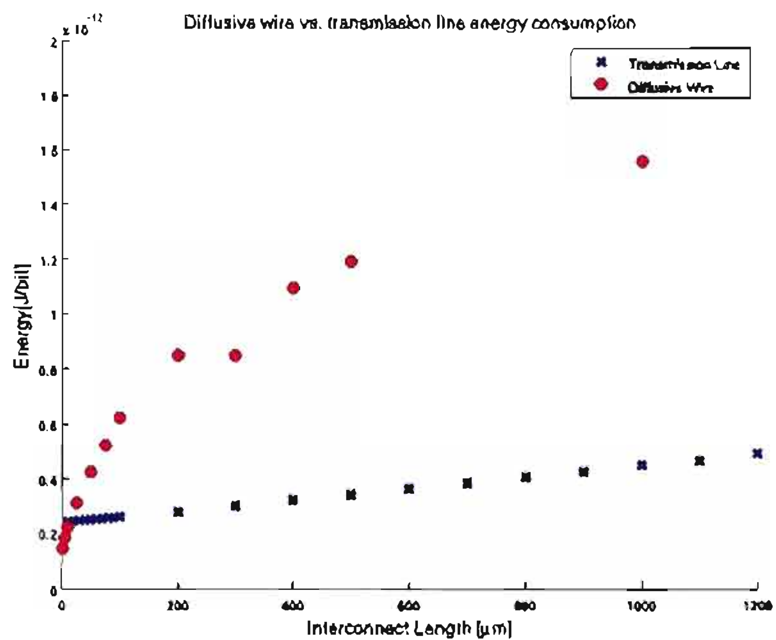

Figure 6.16. Energy comparison (10 GHz - Transmission Line)(short interconnects)

the transmission lines for a data bus; roughly a 3x increase in power yields a 10x increase in frequency (Figure 6.11). The 10 GHz transmission lines show a periodic power consumption. This is due to various line lengths corresponding to even and odd multiples of $\lambda/4$, as discussed in Chapter 5. Further power savings may be possible with the transmission lines by adjusting the frequency and line length to take advantage of these standing wave reflections. This topic requires further research.

6.3 Throughput

The transmission lines outperform the diffusive wires in terms of throughput for lengths greater than 400 μm. The diffusive wire maximum throughput was determined by increasing the frequency of the input until the output no longer reached 10%-90% of the supply voltage, V_{DD}.

The transmission line throughput was limited by the F04 delay (i.e., the time required to transmit the signal from one stage to the next one that is 4x the size). Therefore, the transmission line throughput was relatively independent of interconnect length. The maximum throughput of the transmission line systems was approximately 13 GHz. This can be compared with the diffusive wire throughputs in Figure 3.11 and Figure 3.12; the maximum diffusive wire throughput was approximately 4 GHz for interconnects length over 500 μm. The shorter diffusive wires had a higher throughput since they did not require repeaters. The transmission lines themselves were capable of transmitting signals with a higher throughput.

6.4 Area

The area comparisons need to be separated into three categories to accurately understand the advantages and drawbacks of both systems: silicon area, vias, and upper metal layer area. Silicon area and vias will be discussed jointly because they are both drawbacks of the diffusive wires. Metal layer area is only discussed for transmission lines since it is only a drawback of this system.

6.4.1 Silicon Area and Vias

As shown in Figure 3.14 and Figure 3.15, the number of repeaters and hence the total silicon area required for the diffusive wires is linearly dependent on the length of the line. Furthermore, each repeater requires a set of two vias that penetrate all of the metal layers to connect the upper metal wire to the repeater on the substrate. Vias do not require very much area but they do block signal routing on all the metal layers. Removing vias makes more metal tracks available for routing the signal.

Since the transmission lines do not use repeaters, its silicon area is about 26.3 μm^2 and is independent of length (see section 5.2). The transmission area is slightly higher because of the larger driver (NMOS width of 20 μm for the transmission line driver as opposed to an NMOS width of 12 μm for the diffusive wire driver and repeaters) and buffer sizes for the transmission lines. Once the diffusive wires require three repeaters, the transmission lines consume less silicon area than the diffusive wires. This occurs at a length of about 1500μm (Figure 3.15).

6.4.2 Upper Metal Layer Area

The diffusive wires simulated were implemented with minimum pitch wires on the top copper metal layer available in the process. The minimum pitch is 0.20 μm. In practice, the wires will be wider than this to avoid variation and reduce the wire delay. Wider wires, however, require larger repeaters and higher power consumption. Furthermore, long wires sending critical signals need to be shielded from other wires. The most common ways of doing this include increasing the space between wires and ensuring that adjacent wires do not switch in opposite directions at the same time. Therefore, the actual width required for the diffusive wires will be greater than 0.20 μm.

Since the transmission lines consist of a coplanar sandwich (Figure 4.1), the signal wire is already shielded from other signals. Therefore, they can be placed as close as the design rules permit on the same layer. For transmission lines with wide spacings, the designer must verify that the transmission line RLC parameters are not influenced by other layers. Even adjacent, parallel transmission lines will not share return paths to ensure that the RLC parameters remain constant. Further

studies may be able to combine these return paths and verify the characteristic impedances of the lines.

The total width for the transmission lines depends on a number of factors (see section 5.2). The total widths for a 10 GHz transmission line with a 50 Ω impedance for lengths of 1000μm, 5000μm, and 10000 μm are 3.37 μm, 12.2 μm, 27.1 μm, respectively (refer to Appendix A). The longer interconnects basically need wider wires to decrease the resistance per unit length of the line.

Due to the wide variety of transmission line widths possible, it is more difficult to quantitatively compare the metal area tradeoffs. For most integrated circuit designs, however, it should be noted that the lower layers are more valuable than the upper layers. That is to say, the silicon substrate and the first few metal layers are heavily occupied by devices, routing, and local interconnects. The upper metal layers are utilized far less; they are mostly used for power supplies, clock signals, and global interconnects. Therefore, although the transmission lines require more metal area, they trade silicon area and routing space for less valuable upper metal layer area.

6.5 Noise Tolerance

The lossless transmission line models operating at high frequencies were very susceptible to ringing and large voltage spikes that could cause glitching (Figure 5.1, Figure 5.3, and Figure 5.5). The lossy transmission lines did not show any ringing and very limited overshoot (Figure 5.2, Figure 5.4, and Figure 5.6). The resistance of the transmission line does an excellent job of attenuating the reflections. In practice, the signals will most likely be more noisy because the RLC parameters of the line can not be perfectly controlled due to process variation.

Due to the buffers and drivers in series, both the diffusive wires and the transmission lines filter out noise coming from the input. The diffusive wires continue this process by passing through a repeater every 500 μm whereas the transmission lines rely on consistent RLC parameters to avoid mismatch and reflections on the line.

CHAPTER 7

CONCLUSION AND RECOMMENDATIONS

As shown in Chapter 6, the transmission lines showed significant latency, power consumption, and throughput benefits over the diffusive wires. Operating at the same frequency of 1 GHz, the transmission lines had a smaller propagation delay for all interconnects over 100 μm (Figure 6.2) and consumed less power for all interconnects greater than 400 μm (Figure 6.10). The throughput for the transmission lines were limited by the throughput of the signal buffer connected to the transmission line driver; the maximum throughput was approximately 13 GHz for all interconnect lengths. The diffusive wires, on the other hand, had a maximum throughput around 13 GHz for interconnects less than 500 μm (Figure 3.11). For longer interconnects, the throughput dropped to 4 GHz for interconnect lengths of 4000 μm and greater.

The main negative tradeoff of the transmission lines is the upper metal layer area requirements. Building transmission lines requires three wires (one signal path and two return paths) that are usually wider than the minimum pitch wires. Also, to obtain the desired impedance, the transmission lines require spacings that are usually wider than the minimum wire spacings. The total system transmission line width will always be at least five times the width of the minimum pitch wire, as seen in Appendix A.

Although at first glance these area tradeoffs seem very large, a second look shows that the situation is not that bad. First, in actual systems, critical high speed interconnects will not be connected by minimum pitch wires separated by minimum spacings. The wires and their spacings will be larger than the minimum values to

minimize variation, resistance, and cross coupling capacitance. Fatter wires reduce resistance. Larger spacings reduce capacitance. Second, the diffusive wires require shielding to mitigate noise. The transmission lines are already shielded due to the return paths on either side of the signal. Third, the diffusive wires require repeaters. Each repeater requires at least two sets of vias connecting the signal metal layer to the substrate and back. These repeaters block routing space on all the intermediate metal layers. The lack of repeaters also translates to extra silicon area. Therefore, the transmission lines can actually free more lower metal layers (crucial for very short interconnects and routing) and provide more silicon space to place devices.

Furthermore, this thesis was based on the IBM metalization option offered by MOSIS for the IBM 65 nm process, which consists of 6 thin copper metal layers (1x thick), 2 thick copper metal layers (2x thick) in FTEOS (silicon dioxide-like substance), and 1 very thick aluminum layer. Thicker metal layers would decrease the necessary total transistor width. A lower k dielectric would allow the spacing to decrease while maintaining the desired characteristic impedance in addition to increasing the speed of light in the medium (see Chapter 5).

Another way to mitigate the area tradeoff is to utilize the transmission line's higher bandwidth. Since the transmission line can consistently operate at around 13 GHz, it has approximately 3 times the bandwidth than the diffusive wires for interconnects longer than 4000 μm. For a signal bus, this can translate to three diffusive wires being replaced by a single transmission line. As discussed in section 6.2, this replacement is also more energy efficient per bit transmitted. Furthermore, the transmission line bandwidth is limited by the speed of the buffers and the drivers and not the transmission lines themselves. In future processes, the bandwidth of the transmission lines will increase with the performance of the transistors. The diffusive wire system will require more repeaters. Its throughput will not increase appreciably since the RC wire delay will remain a problem.

Another unknown issue for the transmission lines is their noise tolerance and sensitivity to wires on other layers. As previously discussed, the transmission lines are shielded by other wires on the same layer due to the surrounding return paths.

If there is a transmission line that requires a large spacing, it is possible that the transmission line could become coupled to a wire on another layer. The transmission lines requiring larger spacings will require more care to avoid coupling on other layers (i.e., large metal wires cannot be placed parallel to the transmission lines on adjacent layers). Since these issues are more design specific, they were not addressed in this thesis.

7.1 Potential Applications

The results of this thesis are mainly targeted at three applications: point-to-point signaling, data buses, and clock distribution networks. Basically, any wire longer than about 400 μm and shorter than 10000 μm (or 1 cm) will have better performance with the transmission lines, as shown in Figure 7.1. Below 400 μm, diffusive wires will have roughly the same performance as the transmission lines. As the transmission lines become very long, the wires need to be very wide to reduce resistance; otherwise, the transmission line will operate in the RC regime. Additionally, the high resistance of very long transmission lines makes them difficult to drive; the output is almost always attenuated. If interconnects longer than 7500 μm are needed, alternatives such as optical interconnects become a viable solution. In summary, on-chip interconnects that do not require repeaters should be implemented with diffusive wires. Interconnects that normally require repeaters should be replaced with transmission lines. Very long or off-chip interconnects should employ an alternative interconnect. The exact lengths where a designer should switch interconnects depend on the application and design constraints. Since the transmission lines perform well at higher frequencies, wires with higher activity factors will benefit the most from transmission lines.

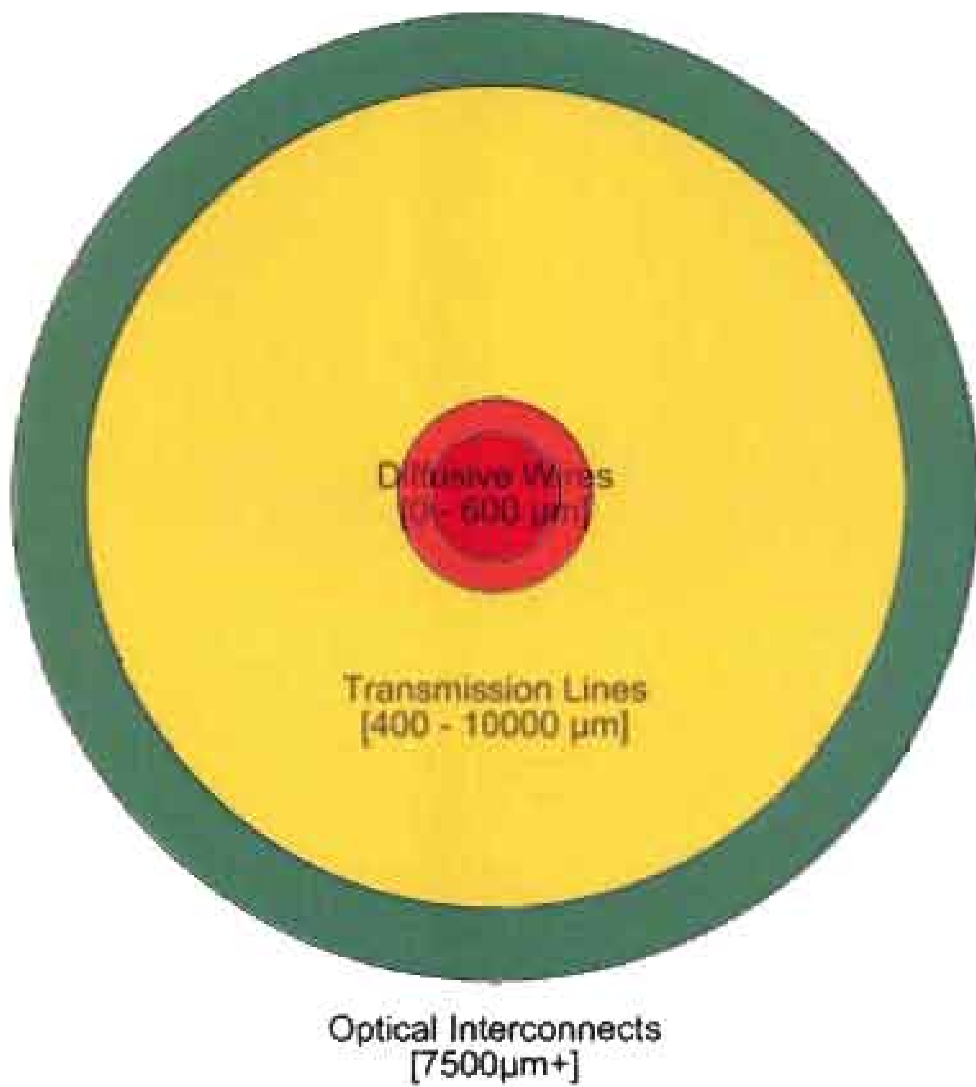

Figure 7.1: Recommended interconnects for IBM 65 nm process

The clock signal of a digital circuit has a very high activity (by definition it changes every clock cycle). For a synchronous design, the clock needs to arrive everywhere in the system at the same time with as little variation as possible. In addition to the benefits already discussed, the transmission lines would be very tolerant to variation because of the wide wires and large drivers. The transmission line can reasonably be forked two times with impedance matching; the clock signal could be sent to four places at once without any repeaters. Total wire lengths of up to 15000 μm have already been simulated successfully (refer to section 5.3).

7.2 Future Research

All the results in this thesis rely on the transmission line synthesis tool correctly determining resistance, capacitance, and inductance of the line. The impedance calculating tool (see section 4.1) has been compared to other tools widely used in academia. The next step is to build a test chip to determine if the transmission lines act as expected.

Depending on the results of the test chip, future research would include developing tools to automatically generate the transmission lines and replace diffusive wires with them. These tools could be applied to an existing integrated circuit design. An excellent study would be to implement a large integrated system with and without the transmission lines to see what system level effects and tradeoffs occur.

APPENDIX A

TRANSMISSION LINE DIMENSIONS

This appendix consists of a table listing many of the transmission line dimensions calculated with Escovar's tool (see section 4.1.3).

Table A.1: Transmission line parameters for IBM 65nm process

Frequency = 1 GHz									
	Z_o = 50 Ω, Metal Thickness = 0.35 μm								
L [μm]	W_S [μm]	W_G [μm]	S_{min} [μm]	$S(Z_o)$ [μm]	W_T [μm]	R_{tr} [Ω]	R [kΩ/m]	L [μH/m]	C [pF/m]
100	0.2	0.2	0.09	0.3304	1.26	20	369.5	0.378	151.2
100	0.4	0.2	0.06	0.3764	1.55	20	246.3	0.381	152.6
100	0.2	0.4	0.06	0.3217	1.64	20	307.9	0.388	155.2
200	0.2	0.2	0.20	0.3292	1.26	20	369.4	0.378	151.1
200	0.4	0.2	0.13	0.3743	1.55	20	246.3	0.381	152.4
200	0.2	0.4	0.15	0.3206	1.64	20	307.9	0.388	155.2
300	0.4	0.2	0.22	0.3735	1.55	20	246.3	0.381	152.3
300	0.2	0.4	0.26	0.3202	1.64	20	307.9	0.388	155.2
300	0.4	0.4	0.14	0.3734	1.95	20	184.7	0.387	154.7
400	0.4	0.2	0.34	0.373	1.55	20	246.3	0.381	152.2
400	0.4	0.4	0.21	0.373	1.95	20	184.7	0.387	154.7
500	0.4	0.4	0.30	0.3727	1.95	20	184.7	0.387	154.7
600	0.5	0.5	0.29	0.393	2.29	20	147.8	0.389	155.6
600	1	0.5	0.18	0.4824	2.96	20	98.52	0.387	155
600	0.5	1	0.20	0.3743	3.25	20	123.2	0.405	161.8
700	0.5	0.5	0.38	0.3928	2.29	20	147.7	0.389	155.6
700	1	0.5	0.23	0.482	2.96	20	98.53	0.387	155
700	0.5	1	0.26	0.3742	3.25	20	123.2	0.405	161.8
800	1	0.5	0.29	0.4817	2.96	20	98.53	0.387	154.9
800	0.5	1	0.33	0.374	3.25	20	123.2	0.405	161.8
800	1.5	0.5	0.22	0.5466	3.59	20	82.1	0.388	155

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
900	1	0.5	0.35	0.4814	2.96	20	98.52	0.387	154.9
900	1.5	0.5	0.28	0.5462	3.59	20	82.1	0.387	155
900	1	1	0.20	0.4819	3.96	20	73.89	0.395	158.1
1000	1	0.5	0.43	0.4812	2.96	20	98.52	0.387	154.9
1000	1.5	0.5	0.34	0.5458	3.59	20	82.1	0.387	155
1000	1	1	0.24	0.4817	3.96	20	73.89	0.395	158.1
2000	2	1	0.55	0.6351	5.27	20	49.26	0.388	155.4
2000	2	1.5	0.37	0.642	6.28	20	41.05	0.391	157.1
2000	3	1	0.42	0.745	6.49	20	41.05	0.387	154.9
3000	3	1.5	0.67	0.7795	7.56	20	32.84	0.387	154.9
4000	4	2	0.78	0.9144	9.83	20	24.64	0.386	154.5
4000	5	2	0.65	1.016	11	20	22.18	0.385	154.2
4000	4	3	0.48	0.9392	11.9	20	20.54	0.389	155.6
5000	4	3	0.88	0.9382	11.9	20	20.54	0.389	155.6
5000	6	2	1.04	1.104	12.2	20	20.54	0.385	153.9
5000	5	3	0.71	1.067	13.1	20	18.08	0.386	154.4
6000	6	3	0.99	1.179	14.4	20	16.43	0.384	153.7
6000	5	4	0.84	1.077	15.2	20	16.03	0.389	155.5
6000	7	3	0.86	1.279	15.6	20	15.27	0.383	153.3
7000	6	4	1.07	1.208	16.4	20	14.39	0.386	154.3
7000	5	5	1.03	1.067	17.1	20	14.8	0.393	157.1
7000	7	4	0.91	1.327	17.7	20	13.21	0.384	153.6
8000	7	5	1.02	1.345	19.7	20	11.99	0.386	154.3
8000	6	6	1.00	1.201	20.4	20	12.34	0.392	156.8
8000	7	6	0.81	1.346	21.7	20	11.17	0.388	155.3
9000	10	4	1.40	1.621	21.2	20	11.11	0.382	152.7
9000	8	6	1.00	1.479	23	20	10.29	0.386	154.3
9000	12	4	1.20	1.781	23.6	20	10.29	0.381	152.6
10000	8	6	1.39	1.478	23	20	10.29	0.386	154.3
10000	12	4	1.67	1.779	23.6	20	10.29	0.381	152.6
10000	10	6	1.07	1.72	25.4	20	9.061	0.382	153
11000	10	6	1.46	1.719	25.4	20	9.061	0.382	153
11000	12	6	1.20	1.931	27.9	20	8.243	0.381	152.3
Frequency = 5 GHz									
	Z_o = 50 Ω Metal Thickness = 0.35 μm								
2500	2.5	2	0.38	0.725	7.95	20	32.21	0.391	156.4
Frequency = 10 GHz									
	Z_o = 25 Ω Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	0.09903	0.848	20	320.2	0.224	358.1

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
100	0.5	0.2	0.05	0.1018	1.1	20	221.7	0.232	370.7
100	0.75	0.2	0.04	0.1025	1.35	20	188.9	0.238	380.8
200	0.75	0.2	0.09	0.1021	1.35	20	188.9	0.238	380.8
	Z_o = 35 Ω Metal Thickness = 0.35 μm								
100	1	0.2	0.04	0.2131	1.83	20	172.5	0.295	241.1
200	1	0.2	0.08	0.2116	1.82	20	172.6	0.295	240.9
250	0.75	0.2	0.13	0.2051	1.56	20	188.9	0.291	237.9
300	1	0.2	0.15	0.2109	1.82	20	172.5	0.295	240.8
400	1.5	0.5	0.07	0.2246	2.95	20	82.33	0.305	249.2
500	1.5	0.5	0.10	0.2243	2.95	20	82.34	0.305	249.2
600	1.5	0.5	0.14	0.224	2.95	20	82.33	0.305	249.2
700	1.5	0.5	0.18	0.2239	2.95	20	82.33	0.305	249.2
800	2	0.75	0.12	0.2365	3.97	20	57.9	0.309	252.6
900	2	0.75	0.15	0.2364	3.97	20	57.89	0.309	252.6
1000	2	0.75	0.19	0.2363	3.97	20	57.89	0.309	252.6
1000	4	0.5	0.23	0.2485	5.5	20	62.69	0.317	258.5
1000	5	0.5	0.21	0.2521	6.5	20	60.62	0.320	261.1
2000	4	1.5	0.23	0.2808	7.56	20	29.8	0.313	255.3
2000	5	1.5	0.20	0.2982	8.6	20	27.57	0.311	254.1
2000	6	1.5	0.18	0.3126	9.63	20	26.16	0.310	253.2
3000	4	4	0.23	0.2704	12.5	20	20.58	0.325	265.6
3000	5	4	0.19	0.3018	13.6	20	18.1	0.318	259.9
3000	4	5	0.21	0.2661	14.5	20	19.82	0.328	268
4000	6	5	0.29	0.3292	16.7	20	15.59	0.315	256.8
5000	10	5	0.37	0.4348	20.9	20	12.34	0.300	244.7
	Z_o = 50 Ω Metal Thickness = 0.35 μm								
100	0.5	0.5	0.00	0.3975	2.3	20	147.8	0.390	155.8
100	1	0.5	0.02	0.4924	2.98	20	98.62	0.389	155.4
100	0.5	1	0.02	0.3786	3.26	20	123.4	0.404	161.8
200	0.5	0.5	0.06	0.395	2.29	20	147.8	0.389	155.7
200	1	0.5	0.04	0.4872	2.97	20	98.6	0.388	155.2
200	0.5	1	0.04	0.3762	3.25	20	123.5	0.405	161.8
300	0.5	0.5	0.10	0.3941	2.29	20	147.8	0.389	155.7
300	1	0.5	0.06	0.4852	2.97	20	98.6	0.388	155.1
300	0.5	1	0.07	0.3754	3.25	20	123.5	0.405	161.8
400	0.5	0.5	0.16	0.3936	2.29	20	147.8	0.389	155.7
400	1	0.5	0.09	0.4841	2.97	20	98.62	0.388	155
400	0.5	1	0.10	0.3748	3.25	20	123.5	0.405	161.8

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
500	0.5	0.5	0.22	0.3932	2.29	20	147.8	0.389	155.6
500	1	0.2	0.33	0.4596	2.32	20	172.5	0.385	153.8
500	1	0.4	0.16	0.4786	2.76	20	110.9	0.386	154.5
600	1	0.2	0.45	0.459	2.32	20	172.5	0.384	153.8
600	1	0.4	0.22	0.478	2.76	20	110.9	0.386	154.5
600	1.5	0.2	0.41	0.5057	2.91	20	156.2	0.387	155
700	1	0.4	0.28	0.4776	2.76	20	110.9	0.386	154.5
700	1.5	0.4	0.23	0.538	3.38	20	94.6	0.387	154.8
800	1	0.4	0.35	0.4773	2.75	20	110.9	0.386	154.4
800	1.5	0.4	0.29	0.5375	3.37	20	94.6	0.387	154.8
900	1	0.4	0.44	0.477	2.75	20	110.9	0.386	154.4
900	1.5	0.4	0.36	0.537	3.37	20	94.6	0.387	154.7
1000	1.5	0.4	0.44	0.5366	3.37	20	94.6	0.387	154.7
1000	1.5	0.5	0.34	0.547	3.59	20	82.28	0.387	154.8
1000	2	0.5	0.30	0.5984	4.2	20	74.17	0.388	155.1
1100	1.5	0.5	0.41	0.5467	3.59	20	82.28	0.387	154.8
1100	2	0.5	0.36	0.5979	4.2	20	74.17	0.388	155
1100	1.5	1	0.21	0.5698	4.64	20	57.78	0.390	155.9
1200	1.5	0.5	0.48	0.5464	3.59	20	82.28	0.387	154.7
1200	2	0.5	0.43	0.5975	4.2	20	74.17	0.388	155
1200	1.5	1	0.25	0.5696	4.64	20	57.78	0.390	155.9
1300	2	0.5	0.50	0.5971	4.19	20	74.17	0.387	155
1300	1.5	1	0.29	0.5694	4.64	20	57.78	0.390	155.9
1300	2.5	0.5	0.46	0.6395	4.78	20	69.37	0.388	155.3
1400	2	0.5	0.58	0.5968	4.19	20	74.14	0.387	155
1400	1.5	1	0.33	0.5692	4.64	20	57.78	0.390	155.9
1400	2.5	0.5	0.54	0.639	4.78	20	69.37	0.388	155.3
1500	1.5	1	0.38	0.569	4.64	20	57.78	0.390	155.9
1500	2.5	0.5	0.63	0.6386	4.78	20	69.4	0.388	155.3
1500	2	1	0.31	0.6392	5.28	20	49.63	0.388	155.1
1600	1.5	1	0.44	0.5688	4.64	20	57.78	0.390	155.9
1600	2	1	0.35	0.639	5.28	20	49.62	0.388	155.1
1600	1.5	1.5	0.31	0.5682	5.64	20	49.76	0.395	157.9
1700	1.5	1	0.50	0.5687	4.64	20	57.78	0.390	155.9
1700	2	1	0.40	0.6388	5.28	20	49.63	0.388	155.1
1700	1.5	1.5	0.36	0.5681	5.64	20	49.76	0.395	157.9
1800	1.5	1	0.56	0.5686	4.64	20	57.78	0.390	155.9
1800	2	1	0.45	0.6386	5.28	20	49.63	0.388	155.1
1800	1.5	1.5	0.40	0.568	5.64	20	49.76	0.395	157.9
1900	2	1	0.51	0.6384	5.28	20	49.63	0.388	155
1900	1.5	1.5	0.45	0.5679	5.64	20	49.76	0.395	157.9

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
1900	2.5	1	0.44	0.6987	5.9	20	44.79	0.386	154.6
2000	2	1	0.57	0.6382	5.28	20	49.63	0.388	155
2000	1.5	1.5	0.51	0.5678	5.64	20	49.77	0.395	157.9
2000	2.5	1	0.49	0.6984	5.9	20	44.8	0.386	154.6
2100	2	1	0.63	0.6381	5.28	20	49.62	0.388	155
2100	1.5	1.5	0.56	0.5677	5.64	20	49.76	0.395	157.9
2100	2.5	1	0.55	0.6982	5.9	20	44.8	0.386	154.6
2200	2.5	1	0.61	0.698	5.9	20	44.8	0.386	154.6
2200	2	1.5	0.48	0.6501	6.3	20	41.56	0.390	156.1
2200	3	1	0.55	0.7502	6.5	20	41.6	0.386	154.4
2300	2.5	1	0.67	0.6978	5.9	20	44.78	0.386	154.6
2300	2	1.5	0.53	0.65	6.3	20	41.56	0.390	156.1
2300	3	1	0.61	0.75	6.5	20	41.6	0.386	154.3
2400	2	1.5	0.58	0.6499	6.3	20	41.56	0.390	156.1
2400	3	1	0.67	0.7498	6.5	20	41.6	0.386	154.3
2400	2.5	1.5	0.48	0.7223	6.94	20	36.7	0.388	155
2500	2	1.5	0.63	0.6498	6.3	20	41.56	0.390	156.1
2500	3	1	0.73	0.7496	6.5	20	41.6	0.386	154.3
2500	2.5	1.5	0.53	0.7221	6.94	20	36.7	0.388	155
2600	2.5	1.5	0.58	0.722	6.94	20	36.7	0.388	155
2600	3	1.5	0.51	0.7864	7.57	20	33.47	0.386	154.3
2700	2.5	1.5	0.63	0.7219	6.94	20	36.7	0.388	155
2700	3	1.5	0.55	0.7862	7.57	20	33.47	0.386	154.3
2800	2.5	1.5	0.69	0.7218	6.94	20	36.68	0.388	155
2800	3	1.5	0.60	0.7861	7.57	20	33.47	0.386	154.3
2900	3	1.5	0.65	0.7859	7.57	20	33.47	0.386	154.3
3000	3	1.5	0.71	0.7858	7.57	20	33.47	0.386	154.3
3000	3	2	0.53	0.8029	8.61	20	29.5	0.387	154.8
3000	4	1.5	0.59	0.897	8.79	20	29.51	0.384	153.5
3100	3	1.5	0.76	0.7856	7.57	20	33.48	0.386	154.3
4000	4	2	0.87	0.9304	9.86	20	25.5	0.384	153.5
4000	3	3	0.78	0.8109	10.6	20	25.8	0.390	156.2
4000	4	2.5	0.70	0.9516	10.9	20	23.17	0.384	153.7
5000	5	2.5	1.05	1.077	12.2	20	20.8	0.381	152.5
5000	5	3	0.89	1.101	13.2	20	19.27	0.381	152.5
5000	6	2.5	0.95	1.191	13.4	20	19.24	0.379	151.7
6000	5	4	1.13	1.13	15.3	20	17.48	0.382	152.7
6000	7	3	1.17	1.341	15.7	20	16.58	0.377	150.8
6000	6	4	0.99	1.274	16.5	20	15.86	0.379	151.4
7000	7	4	1.34	1.407	17.8	20	14.7	0.376	150.4
7000	6	5	1.27	1.304	18.6	20	14.86	0.378	151.4

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
7000	7	5	1.15	1.452	19.9	20	13.68	0.376	150.2
8000	7	6	1.46	1.485	22	20	13.04	0.375	150
9000	9	6	1.69	1.781	24.6	20	11.42	0.370	148.2
9000	10	6	1.60	1.921	25.8	20	10.86	0.369	147.5
9000	9	7	1.56	1.826	26.7	20	10.96	0.370	147.9
10000	11	6	2.00	2.054	27.1	20	10.39	0.367	146.9
10000	10	7	1.92	1.974	27.9	20	10.38	0.368	147.1
10000	11	7	1.84	2.12	29.2	20	9.909	0.366	146.5
11000	11	9	2.08	2.216	33.4	20	9.291	0.365	145.9
	Z_o = 70 Ω Metal Thickness = 0.35 μm								
100	1.5	1	0.01	1.471	6.44	20	57.68	0.516	105.3
200	1.5	1	0.02	1.437	6.37	20	57.7	0.514	105
300	1.5	1	0.03	1.424	6.35	20	57.7	0.513	104.8
400	1.5	1	0.04	1.417	6.33	20	57.7	0.513	104.7
500	1.5	1	0.05	1.413	6.33	20	57.68	0.513	104.6
600	1.5	1	0.07	1.409	6.32	20	57.68	0.512	104.6
700	1.5	1	0.09	1.407	6.31	20	57.69	0.512	104.5
800	1.5	1	0.12	1.405	6.31	20	57.69	0.512	104.5
900	1.5	1	0.14	1.403	6.31	20	57.69	0.512	104.5
1000	1.5	1	0.17	1.402	6.3	20	57.69	0.512	104.4
2000	1.5	1	0.70	1.395	6.29	20	57.7	0.511	104.3
3000	3	2	0.53	2.215	11.4	20	29.26	0.506	103.3
4000	3	2	1.06	2.211	11.4	20	29.27	0.506	103.3
5000	3	2	1.81	2.208	11.4	20	29.26	0.506	103.3
6000	4	3	1.64	2.803	15.6	20	21.3	0.503	102.6
7000	4	3	2.39	2.8	15.6	20	21.3	0.503	102.6
8000	5	4	2.31	3.4	19.8	20	16.99	0.500	102
8000	6	4	2.05	3.848	21.7	20	15.38	0.499	101.8
9000	5	4	3.09	3.397	19.8	20	16.99	0.500	102
9000	6	4	2.73	3.845	21.7	20	15.37	0.499	101.7
10000	6	4	3.54	3.842	21.7	20	15.37	0.498	101.7
	Z_o = 75 Ω Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	0.7852	2.22	20	320.2	0.546	97.01
100	0.25	0.4	0.05	0.8085	2.67	20	258.6	0.547	97.28
100	0.5	0.2	0.05	0.955	2.81	20	221.7	0.550	97.79
200	0.25	0.2	0.17	0.7781	2.21	20	320.2	0.544	96.79
200	0.25	0.4	0.12	0.8015	2.65	20	258.6	0.546	97.12
200	0.5	0.2	0.12	0.9425	2.78	20	221.7	0.548	97.46

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
300	0.25	0.2	0.30	0.7753	2.2	20	320.2	0.544	96.69
300	0.25	0.4	0.21	0.7989	2.65	20	258.6	0.546	97.04
300	0.5	0.2	0.20	0.9374	2.77	20	221.7	0.547	97.31
400	0.25	0.2	0.46	0.7738	2.2	20	320.2	0.544	96.62
400	0.25	0.4	0.33	0.7974	2.64	20	258.5	0.546	97
400	0.5	0.2	0.30	0.9346	2.77	20	221.7	0.547	97.22
500	0.25	0.2	0.67	0.7727	2.2	20	320.2	0.543	96.58
500	0.25	0.4	0.47	0.7964	2.64	20	258.6	0.545	96.97
500	0.5	0.2	0.43	0.9326	2.77	20	221.6	0.546	97.16
600	0.25	0.4	0.65	0.7957	2.64	20	258.7	0.545	96.94
600	0.5	0.2	0.58	0.9312	2.76	20	221.7	0.546	97.11
600	0.5	0.4	0.34	0.9767	3.25	20	160.1	0.547	97.19
700	0.5	0.2	0.76	0.9302	2.76	20	221.7	0.546	97.07
700	0.5	0.4	0.44	0.9757	3.25	20	160.1	0.547	97.16
700	0.75	0.2	0.64	1.065	3.28	20	188.9	0.547	97.28
800	0.5	0.4	0.55	0.9749	3.25	20	160.1	0.546	97.14
800	0.75	0.2	0.82	1.064	3.28	20	188.9	0.547	97.24
800	0.75	0.4	0.42	1.129	3.81	20	127.2	0.547	97.18
900	0.5	0.4	0.69	0.9742	3.25	20	160.1	0.546	97.12
900	0.75	0.2	1.03	1.062	3.27	20	188.9	0.547	97.21
900	0.75	0.4	0.51	1.128	3.81	20	127.3	0.546	97.15
1000	0.5	0.4	0.84	0.9737	3.25	20	160.1	0.546	97.1
1000	0.75	0.4	0.62	1.127	3.8	20	127.3	0.546	97.13
	Z_o = 100 Ω Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	1.598	3.85	20	320.2	0.720	71.97
100	0.25	0.4	0.05	1.688	4.43	20	258.6	0.718	71.76
100	0.5	0.2	0.05	2.014	4.93	20	221.7	0.727	72.65
200	0.25	0.2	0.17	1.57	3.79	20	320.2	0.717	71.66
200	0.25	0.4	0.12	1.659	4.37	20	258.6	0.715	71.5
200	0.5	0.2	0.12	1.964	4.83	20	221.7	0.722	72.22
300	0.25	0.2	0.30	1.558	3.77	20	320.2	0.715	71.52
300	0.25	0.4	0.21	1.647	4.34	20	258.6	0.714	71.39
300	0.5	0.2	0.20	1.944	4.79	20	221.7	0.720	72.03
400	0.25	0.2	0.46	1.552	3.75	20	320.2	0.714	71.44
400	0.25	0.4	0.33	1.641	4.33	20	258.5	0.713	71.32
400	0.5	0.2	0.30	1.933	4.77	20	221.7	0.719	71.92
500	0.25	0.2	0.67	1.546	3.74	20	320.2	0.714	71.41
500	0.25	0.4	0.47	1.637	4.32	20	258.6	0.713	71.28
500	0.5	0.2	0.43	1.926	4.75	20	221.6	0.718	71.84
600	0.25	0.2	0.95	1.543	3.74	20	320.2	0.714	71.37

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
600	0.25	0.4	0.65	1.634	4.32	20	258.7	0.712	71.24
600	0.5	0.2	0.58	1.92	4.74	20	221.7	0.718	71.78
700	0.25	0.2	1.31	1.54	3.73	20	320.1	0.713	71.34
700	0.25	0.4	0.87	1.631	4.31	20	258.6	0.712	71.22
700	0.5	0.2	0.76	1.916	4.73	20	221.7	0.717	71.73
800	0.25	0.4	1.15	1.63	4.31	20	258.6	0.712	71.19
800	0.5	0.2	0.98	1.913	4.73	20	221.6	0.717	71.7
800	0.5	0.4	0.55	2.045	5.39	20	160.1	0.715	71.52
900	0.25	0.4	1.50	1.628	4.31	20	258.7	0.712	71.17
900	0.5	0.2	1.25	1.91	4.72	20	221.7	0.717	71.66
900	0.5	0.4	0.69	2.042	5.38	20	160.1	0.715	71.5
1000	0.5	0.2	1.57	1.907	4.71	20	221.7	0.716	71.64
1000	0.5	0.4	0.84	2.04	5.38	20	160.1	0.715	71.47
1000	0.75	0.2	1.28	2.232	5.61	20	188.9	0.718	71.84
5000	3	1	3.74	5.561	16.1	20	41.38	0.711	71.11
5000	3	1.5	2.36	6.046	18.1	20	33.2	0.708	70.75
5000	4	1	3.40	6.588	19.2	20	37.38	0.713	71.26
3000	1.5	0.5	3.61	4.519	11.5	20	82.23	0.784	64.81
	Z_o = 120 Ω Metal Thickness = 0.35 μm								
100	1.5	0.2	0.03	6.425	14.7	20	156.1	0.898	62.37
200	1.5	0.2	0.07	5.921	13.7	20	156.1	0.884	61.37
300	1.5	0.2	0.13	5.741	13.4	20	156.1	0.878	60.95
400	1.5	0.2	0.20	5.643	13.2	20	156.1	0.874	60.71
500	1.5	0.2	0.30	5.58	13.1	20	156.1	0.872	60.55
600	1.5	0.2	0.41	5.535	13	20	156.1	0.870	60.43
700	1.5	0.2	0.55	5.5	12.9	20	156.1	0.869	60.34
800	1.5	0.2	0.71	5.472	12.8	20	156.1	0.868	60.26
900	1.5	0.2	0.89	5.449	12.8	20	156.1	0.867	60.2
1000	1.5	0.2	1.11	5.43	12.8	20	156.1	0.866	60.14
3000	1.5	0.5	3.61	5.967	14.4	20	82.23	0.855	59.34
8000	4.5	1	11.78	12.74	32	20	36.02	0.852	59.2
	Z_o = 125 Ω Metal Thickness = 0.35 μm								
1000	1	0.5	0.43	5.662	13.3	20	98.59	0.892	57.11
2000	1	0.5	1.73	5.575	13.2	20	98.6	0.889	56.89
3000	1	0.5	4.85	5.537	13.1	20	98.6	0.887	56.79
4000	2	1	2.69	9.047	22.1	20	49.48	0.884	56.61
4000	3	1	2.17	11.55	28.1	20	41.38	0.888	56.82
5000	2	1	4.75	9.011	22	20	49.46	0.884	56.55

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
5000	3	1	3.74	11.49	28	20	41.36	0.887	56.75
6000	2	1	7.92	8.985	22	20	49.47	0.883	56.5
6000	3	1	6.03	11.45	27.9	20	41.37	0.886	56.69
7000	3	1	9.33	11.42	27.8	20	41.37	0.885	56.65
8000	5	5	2.04	22.88	60.8	20	15.46	0.869	55.64
8000	5	10	1.66	26.8	78.6	20	13.14	0.861	55.09
8000	10	5	1.34	37.35	94.7	20	10.7	0.875	55.99
9000	5	5	2.73	22.83	60.7	20	15.47	0.869	55.61
9000	5	10	2.21	26.75	78.5	20	13.13	0.860	55.07
9000	10	5	1.81	37.23	94.5	20	10.69	0.874	55.94
10000	5	5	3.53	22.8	60.6	20	15.47	0.869	55.59
10000	5	10	2.84	26.71	78.4	20	13.14	0.860	55.05
10000	10	5	2.35	37.13	94.3	20	10.69	0.874	55.91
3000	1.5	0.5	3.61	7.824	18.1	20	82.23	0.926	54.77
	$Z_o = 140\ \Omega$ Metal Thickness = 0.35 μm								
100	1.5	1	0.01	15.76	35	20	57.62	1.044	53.28
200	1.5	1	0.02	13.6	30.7	20	57.6	1.022	52.14
300	1.5	1	0.03	12.94	29.4	20	57.63	1.013	51.71
400	1.5	1	0.04	12.61	28.7	20	57.62	1.009	51.47
500	1.5	1	0.05	12.4	28.3	20	57.62	1.006	51.31
600	1.5	1	0.07	12.26	28	20	57.63	1.003	51.2
700	1.5	1	0.09	12.15	27.8	20	57.63	1.002	51.11
800	1.5	1	0.12	12.07	27.6	20	57.62	1.000	51.04
900	1.5	1	0.14	12.01	27.5	20	57.62	0.999	50.98
1000	1.5	1	0.17	11.95	27.4	20	57.63	0.998	50.93
2000	1	1	0.99	9.324	21.6	20	74	0.989	50.47
3000	1	1	2.50	9.245	21.5	20	74	0.987	50.37
4000	1	1	5.42	9.197	21.4	20	74	0.986	50.31
5000	1.5	1.5	4.35	12.37	29.2	20	49.44	0.983	50.17
6000	1.5	1.5	7.27	12.33	29.2	20	49.45	0.983	50.13
7000	1.5	1.5	11.77	12.3	29.1	20	49.44	0.982	50.1
8000	2	2	9.15	15.44	36.9	20	37.2	0.980	50.01
9000	2	2	13.21	15.41	36.8	20	37.2	0.980	49.98
10000	3	1.5	15.43	18.55	43.1	20	33.18	0.986	50.28
Frequency = 15 GHz									
	$Z_o = 25\ \Omega$ Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	0.09903	0.848	20	320.2	0.224	358.1
100	0.5	0.2	0.05	0.1018	1.1	20	221.7	0.232	370.7

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
100	0.75	0.2	0.04	0.1026	1.36	20	189	0.238	380.4
200	0.75	0.2	0.10	0.1022	1.35	20	189.1	0.238	380.4
	Z_o = 50 Ω Metal Thickness = 0.35 μm								
2500	2.5	2	0.44	0.7381	7.98	20	33.61	0.388	155.2
	Z_o = 75 Ω Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	0.7852	2.22	20	320.2	0.546	97.01
100	0.25	0.4	0.05	0.8085	2.67	20	258.6	0.547	97.28
100	0.5	0.2	0.05	0.955	2.81	20	221.7	0.550	97.79
200	0.25	0.2	0.17	0.7781	2.21	20	320.2	0.544	96.79
200	0.25	0.4	0.12	0.8015	2.65	20	258.6	0.546	97.12
200	0.5	0.2	0.12	0.9425	2.78	20	221.7	0.548	97.46
300	0.25	0.2	0.30	0.7753	2.2	20	320.2	0.544	96.69
300	0.25	0.4	0.21	0.7989	2.65	20	258.6	0.546	97.04
300	0.5	0.2	0.20	0.9374	2.77	20	221.7	0.547	97.31
400	0.25	0.2	0.46	0.7738	2.2	20	320.2	0.544	96.62
400	0.25	0.4	0.33	0.7974	2.64	20	258.5	0.546	97
400	0.5	0.2	0.30	0.9346	2.77	20	221.7	0.547	97.22
500	0.25	0.2	0.67	0.7727	2.2	20	320.2	0.543	96.58
500	0.25	0.4	0.47	0.7964	2.64	20	258.6	0.545	96.97
500	0.5	0.2	0.43	0.9326	2.77	20	221.6	0.546	97.16
600	0.25	0.4	0.65	0.7957	2.64	20	258.7	0.545	96.94
600	0.5	0.2	0.58	0.9312	2.76	20	221.7	0.546	97.11
600	0.5	0.4	0.34	0.9767	3.25	20	160.1	0.547	97.19
700	0.5	0.2	0.76	0.9302	2.76	20	221.7	0.546	97.07
700	0.5	0.4	0.44	0.9757	3.25	20	160.1	0.547	97.16
700	0.75	0.2	0.64	1.065	3.28	20	189	0.547	97.29
800	0.5	0.4	0.55	0.9749	3.25	20	160.1	0.546	97.14
800	0.75	0.2	0.82	1.063	3.28	20	189	0.547	97.25
800	0.75	0.4	0.42	1.129	3.81	20	127.4	0.547	97.18
900	0.5	0.4	0.69	0.9742	3.25	20	160.1	0.546	97.12
900	0.75	0.2	1.03	1.062	3.27	20	189	0.547	97.21
900	0.75	0.4	0.51	1.128	3.81	20	127.3	0.546	97.15
1000	0.5	0.4	0.84	0.9737	3.25	20	160.1	0.546	97.1
1000	0.75	0.4	0.62	1.127	3.8	20	127.4	0.546	97.13
	Z_o = 100 Ω Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	1.598	3.85	20	320.2	0.720	71.97
100	0.25	0.4	0.05	1.688	4.43	20	258.6	0.718	71.76

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
100	0.5	0.2	0.05	2.014	4.93	20	221.7	0.727	72.65
200	0.25	0.2	0.17	1.57	3.79	20	320.2	0.717	71.66
200	0.25	0.4	0.12	1.659	4.37	20	258.6	0.715	71.5
200	0.5	0.2	0.12	1.964	4.83	20	221.7	0.722	72.22
300	0.25	0.2	0.30	1.558	3.77	20	320.2	0.715	71.52
300	0.25	0.4	0.21	1.647	4.34	20	258.6	0.714	71.39
300	0.5	0.2	0.20	1.944	4.79	20	221.7	0.720	72.03
400	0.25	0.2	0.46	1.552	3.75	20	320.2	0.714	71.44
400	0.25	0.4	0.33	1.641	4.33	20	258.5	0.713	71.32
400	0.5	0.2	0.30	1.933	4.77	20	221.7	0.719	71.92
500	0.25	0.2	0.67	1.546	3.74	20	320.2	0.714	71.41
500	0.25	0.4	0.47	1.637	4.32	20	258.6	0.713	71.28
500	0.5	0.2	0.43	1.926	4.75	20	221.6	0.718	71.84
600	0.25	0.2	0.95	1.543	3.74	20	320.2	0.714	71.37
600	0.25	0.4	0.65	1.634	4.32	20	258.7	0.712	71.24
600	0.5	0.2	0.58	1.92	4.74	20	221.7	0.718	71.78
700	0.25	0.2	1.31	1.54	3.73	20	320.1	0.713	71.34
700	0.25	0.4	0.87	1.631	4.31	20	258.6	0.712	71.22
700	0.5	0.2	0.76	1.916	4.73	20	221.7	0.717	71.73
800	0.25	0.4	1.15	1.63	4.31	20	258.6	0.712	71.19
800	0.5	0.2	0.98	1.913	4.73	20	221.6	0.717	71.7
800	0.5	0.4	0.55	2.045	5.39	20	160.1	0.715	71.52
900	0.25	0.4	1.50	1.628	4.31	20	258.7	0.712	71.17
900	0.5	0.2	1.25	1.91	4.72	20	221.7	0.717	71.66
900	0.5	0.4	0.69	2.042	5.38	20	160.1	0.715	71.5
1000	0.5	0.2	1.57	1.907	4.71	20	221.7	0.716	71.64
1000	0.5	0.4	0.84	2.04	5.38	20	160.1	0.715	71.47
1000	0.75	0.2	1.28	2.232	5.61	20	188.9	0.718	71.84
	Z_o = 25 Ω Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	0.09903	0.848	20	320.2	0.224	358.1
100	0.5	0.2	0.05	0.1022	1.1	20	221.8	0.231	369.8
100	0.75	0.2	0.04	0.1027	1.36	20	189.2	0.238	380.3
200	0.75	0.2	0.10	0.1023	1.35	20	189.2	0.238	380.3
	Z_o = 50 Ω Metal Thickness = 0.35 μm								
100	0.5	0.5	0.03	0.3976	2.3	20	148.1	0.390	155.8
100	1	0.5	0.02	0.4935	2.99	20	99.03	0.388	155.2
100	0.5	1	0.02	0.3808	3.26	20	124.4	0.403	161.3
200	0.5	0.5	0.06	0.3951	2.29	20	148.1	0.389	155.7
200	1	0.5	0.04	0.4881	2.98	20	99.05	0.388	155

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
200	0.5	1	0.04	0.3784	3.26	20	124.4	0.403	161.3
300	0.5	0.5	0.10	0.3942	2.29	20	148.1	0.389	155.7
300	1	0.5	0.06	0.4861	2.97	20	99.03	0.387	154.9
300	0.5	1	0.07	0.3776	3.26	20	124.4	0.403	161.3
400	0.5	0.5	0.16	0.3937	2.29	20	148.1	0.389	155.6
400	1	0.5	0.09	0.485	2.97	20	99.03	0.387	154.9
400	0.5	1	0.10	0.3771	3.25	20	124.4	0.403	161.3
500	0.5	0.4	0.25	0.3947	2.09	20	160.2	0.386	154.5
500	0.5	0.5	0.22	0.3934	2.29	20	148.1	0.389	155.6
500	1	0.2	0.33	0.46	2.32	20	172.8	0.384	153.8
600	0.5	0.5	0.30	0.3931	2.29	20	148.1	0.389	155.6
600	1	0.5	0.18	0.4837	2.97	20	99.03	0.387	154.8
600	0.5	1	0.20	0.3766	3.25	20	124.4	0.403	161.3
700	0.5	0.5	0.38	0.393	2.29	20	148.1	0.389	155.6
700	1	0.5	0.23	0.4832	2.97	20	99.03	0.387	154.8
700	0.5	1	0.27	0.3765	3.25	20	124.4	0.403	161.3
800	1	0.5	0.29	0.4829	2.97	20	99.04	0.387	154.7
800	0.5	1	0.34	0.3764	3.25	20	124.4	0.403	161.3
800	1.5	0.5	0.23	0.5498	3.6	20	82.91	0.386	154.6
900	1	0.5	0.36	0.4826	2.97	20	99.03	0.387	154.7
900	1.5	0.5	0.29	0.5494	3.6	20	82.91	0.386	154.5
900	1	1	0.21	0.4861	3.97	20	74.99	0.394	157.4
1000	1	0.5	0.43	0.4824	2.96	20	99.03	0.387	154.7
1000	1.5	0.5	0.35	0.549	3.6	20	82.91	0.386	154.5
1000	1	1	0.25	0.4859	3.97	20	74.99	0.393	157.4
2000	2	1	0.60	0.643	5.29	20	50.7	0.386	154.5
2000	1.5	1.5	0.54	0.5739	5.65	20	51.15	0.393	157.1
2000	2.5	1	0.53	0.7061	5.91	20	46.04	0.385	153.8
2500	2.5	2	0.49	0.7475	8	20	34.65	0.386	154.4
2500	3	2	0.43	0.8249	8.65	20	31.43	0.383	153.2
2500	4	2	0.37	0.9661	9.93	20	27.5	0.379	151.4
3000	2.5	2	0.73	0.747	7.99	20	34.67	0.386	154.4
3000	3.5	1.5	0.75	0.8636	8.23	20	32.92	0.381	152.4
3000	3	2	0.65	0.8242	8.65	20	31.43	0.383	153.2
3500	4	2	0.79	0.964	9.93	20	27.5	0.378	151.4
3500	3	3	0.74	0.85	10.7	20	28.22	0.383	153.2
3500	5	2	0.73	1.09	11.2	20	25.17	0.375	150.1
4000	4.5	2	1.02	1.027	10.6	20	26.2	0.377	150.7
4000	5	2	0.99	1.089	11.2	20	25.18	0.375	150.1
4000	3.5	3	0.90	0.9339	11.4	20	25.82	0.380	152
4500	5	3	0.98	1.165	13.3	20	21.57	0.373	149.3

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
4500	7	2	1.20	1.304	13.6	20	22.49	0.371	148.5
4500	4	4	0.97	1.047	14.1	20	22.58	0.376	150.5
5000	5.5	3	1.19	1.235	14	20	20.66	0.372	148.7
5000	4.5	4.5	1.11	1.148	15.8	20	20.66	0.373	149.3
10000	13	8	2.63	2.693	34.4	20	10.38	0.353	141
10000	14	8	2.58	2.838	35.7	20	10.01	0.352	140.8
10000	14	8	2.58	2.838	35.7	20	10.01	0.352	140.8
11000	16	8	3.02	3.11	38.2	20	9.4	0.351	140.4
11000	15	9	2.93	3.061	39.1	20	9.336	0.350	140.2
11000	14	10	2.91	2.979	40	20	9.436	0.350	140.1
12000	16	11	3.24	3.354	44.7	20	8.592	0.348	139.3
	$Z_o = 75\ \Omega$								
	Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	0.7852	2.22	20	320.2	0.546	97.01
100	0.25	0.4	0.05	0.8085	2.67	20	258.6	0.547	97.28
100	0.5	0.2	0.05	0.9563	2.81	20	221.8	0.550	97.74
200	0.25	0.2	0.17	0.7781	2.21	20	320.2	0.544	96.79
200	0.25	0.4	0.12	0.8015	2.65	20	258.6	0.546	97.12
200	0.5	0.2	0.12	0.9437	2.79	20	221.8	0.548	97.4
300	0.25	0.2	0.30	0.7753	2.2	20	320.2	0.544	96.69
300	0.25	0.4	0.21	0.7989	2.65	20	258.6	0.546	97.04
300	0.5	0.2	0.20	0.9387	2.78	20	221.8	0.547	97.25
400	0.25	0.2	0.46	0.7738	2.2	20	320.2	0.544	96.62
400	0.25	0.4	0.33	0.7974	2.64	20	258.5	0.546	97
400	0.5	0.2	0.30	0.9358	2.77	20	221.8	0.547	97.16
500	0.25	0.2	0.67	0.7727	2.2	20	320.2	0.543	96.58
500	0.25	0.4	0.47	0.7964	2.64	20	258.6	0.545	96.97
500	0.5	0.2	0.43	0.9339	2.77	20	221.8	0.546	97.1
600	0.25	0.4	0.65	0.7957	2.64	20	258.7	0.545	96.94
600	0.5	0.2	0.58	0.9325	2.76	20	221.8	0.546	97.05
600	0.5	0.4	0.34	0.9778	3.26	20	160.2	0.546	97.15
700	0.5	0.2	0.76	0.9314	2.76	20	221.7	0.546	97.01
700	0.5	0.4	0.44	0.9768	3.25	20	160.1	0.546	97.12
700	0.75	0.2	0.64	1.065	3.28	20	189	0.547	97.28
800	0.5	0.4	0.56	0.976	3.25	20	160.1	0.546	97.09
800	0.75	0.2	0.82	1.063	3.28	20	189	0.547	97.24
800	0.75	0.4	0.42	1.129	3.81	20	127.5	0.547	97.17
900	0.5	0.4	0.69	0.9753	3.25	20	160.2	0.546	97.07
900	0.75	0.2	1.03	1.062	3.27	20	189	0.547	97.21
900	0.75	0.4	0.51	1.128	3.81	20	127.4	0.546	97.15
1000	0.5	0.4	0.84	0.9747	3.25	20	160.2	0.546	97.06

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
1000	0.75	0.4	0.62	1.127	3.8	20	127.5	0.546	97.12
1000	1	0.5	0.43	1.294	4.59	20	98.9	0.546	97.08
2000	1.5	0.5	1.40	1.534	5.57	20	82.7	0.545	96.93
2000	1	1	1.01	1.383	5.77	20	74.55	0.545	96.83
2000	2	0.5	1.27	1.751	6.5	20	74.75	0.546	96.98
3000	2	1	1.44	1.947	7.89	20	50.27	0.542	96.29
3000	1.5	1.5	1.31	1.766	8.03	20	50.37	0.542	96.32
3000	2.5	1	1.29	2.189	8.88	20	45.53	0.541	96.19
4000	2	1.5	1.98	2.066	9.13	20	42.3	0.540	95.95
4000	3	1	2.32	2.407	9.81	20	42.42	0.540	96.06
4000	2.5	1.5	1.70	2.342	10.2	20	37.52	0.539	95.74
5000	3	1.5	2.57	2.596	11.2	20	34.36	0.537	95.55
5000	2.5	2	2.32	2.45	11.4	20	33.68	0.537	95.46
5000	3	3	1.64	2.926	14.9	20	26.8	0.533	94.83
	$Z_o = 100\ \Omega$ Metal Thickness = 0.35 μm								
100	0.25	0.2	0.08	1.598	3.85	20	320.2	0.720	71.97
100	0.25	0.4	0.05	1.688	4.43	20	258.6	0.718	71.76
100	0.5	0.2	0.05	2.016	4.93	20	221.7	0.726	72.64
200	0.25	0.2	0.17	1.57	3.79	20	320.2	0.717	71.66
200	0.25	0.4	0.12	1.659	4.37	20	258.6	0.715	71.5
200	0.5	0.2	0.12	1.965	4.83	20	221.8	0.722	72.2
300	0.25	0.2	0.30	1.558	3.77	20	320.2	0.715	71.52
300	0.25	0.4	0.21	1.647	4.34	20	258.6	0.714	71.39
300	0.5	0.2	0.20	1.946	4.79	20	221.7	0.720	72.02
400	0.25	0.2	0.46	1.552	3.75	20	320.2	0.714	71.44
400	0.25	0.4	0.33	1.641	4.33	20	258.5	0.713	71.32
400	0.5	0.2	0.30	1.934	4.77	20	221.8	0.719	71.9
500	0.25	0.2	0.67	1.546	3.74	20	320.2	0.714	71.41
500	0.25	0.4	0.47	1.637	4.32	20	258.6	0.713	71.28
500	0.5	0.2	0.43	1.927	4.75	20	221.8	0.718	71.82
600	0.25	0.2	0.95	1.543	3.74	20	320.2	0.714	71.37
600	0.25	0.4	0.65	1.634	4.32	20	258.7	0.712	71.24
600	0.5	0.2	0.58	1.921	4.74	20	221.7	0.718	71.76
700	0.25	0.2	1.31	1.54	3.73	20	320.1	0.713	71.34
700	0.25	0.4	0.87	1.631	4.31	20	258.6	0.712	71.22
700	0.5	0.2	0.76	1.917	4.73	20	221.7	0.717	71.72
800	0.25	0.4	1.15	1.63	4.31	20	258.6	0.712	71.19
800	0.5	0.2	0.98	1.914	4.73	20	221.8	0.717	71.68
800	0.5	0.4	0.56	2.047	5.39	20	160.1	0.715	71.5
900	0.25	0.4	1.50	1.628	4.31	20	258.7	0.712	71.17

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
900	0.5	0.2	1.25	1.911	4.72	20	221.8	0.716	71.65
900	0.5	0.4	0.69	2.044	5.39	20	160.2	0.715	71.47
1000	0.5	0.2	1.57	1.909	4.72	20	221.7	0.716	71.62
1000	0.5	0.4	0.84	2.042	5.38	20	160.2	0.715	71.45
1000	0.75	0.2	1.28	2.232	5.61	20	189	0.718	71.84
5000	2.5	2	2.32	5.769	18	20	33.34	0.703	70.34
Frequency = 25 GHz									
	Z_o = 50 Ω								
		Metal Thickness = 0.35 μm							
500	0.5	0.4	0.25	0.3947	2.09	20	160.2	0.386	154.5
500	1	0.2	0.33	0.4602	2.32	20	173	0.384	153.7
500	0.5	0.6	0.20	0.3895	2.48	20	140.3	0.393	157.1
2500	2.5	2	0.54	0.7577	8.02	20	35.82	0.384	153.5
	Z_o = 75 Ω								
		Metal Thickness = 0.35 μm							
5000	2.5	2	2.45	2.465	11.4	20	34.44	0.536	95.25
5000	3	3	1.80	2.953	14.9	20	27.64	0.532	94.52
	Z_o = 100 Ω								
		Metal Thickness = 0.35 μm							
5000	2.5	2	2.45	5.79	18.1	20	33.96	0.703	70.26
Frequency = 30 GHz									
	Z_o = 50 Ω								
		Metal Thickness = 0.35 μm							
100	0.5	0.2	0.05	0.3972	1.69	20	221.9	0.382	152.6
100	0.5	0.4	0.00	0.3991	2.1	20	160.6	0.387	154.8
100	1	0.2	0.04	0.4703	2.34	20	173.3	0.386	154.4
150	0.5	0.2	0.08	0.3956	1.69	20	221.9	0.381	152.5
150	0.5	0.4	0.05	0.3974	2.09	20	160.6	0.387	154.7
150	1	0.2	0.06	0.4666	2.33	20	173.3	0.386	154.2
200	0.5	0.2	0.12	0.3947	1.69	20	221.9	0.381	152.4
200	0.5	0.4	0.07	0.3966	2.09	20	160.6	0.387	154.6
200	1	0.2	0.08	0.4647	2.33	20	173.3	0.385	154.1
250	0.5	0.2	0.16	0.3941	1.69	20	221.9	0.381	152.3
250	0.5	0.4	0.09	0.396	2.09	20	160.6	0.387	154.6
250	1	0.2	0.11	0.4634	2.33	20	173.3	0.385	153.9
300	0.5	0.2	0.20	0.3936	1.69	20	221.9	0.381	152.3
300	0.5	0.4	0.12	0.3956	2.09	20	160.6	0.386	154.6
300	1	0.2	0.15	0.4625	2.33	20	173.3	0.385	153.9
350	0.5	0.2	0.25	0.3933	1.69	20	221.9	0.381	152.2
350	0.5	0.4	0.15	0.3953	2.09	20	160.6	0.386	154.6

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
350	1	0.2	0.19	0.4619	2.32	20	173.3	0.385	153.8
400	0.5	0.2	0.30	0.3931	1.69	20	221.9	0.380	152.2
400	0.5	0.4	0.18	0.3951	2.09	20	160.6	0.386	154.5
400	1	0.2	0.23	0.4613	2.32	20	173.3	0.384	153.8
450	0.5	0.2	0.36	0.3928	1.69	20	221.9	0.380	152.2
450	0.5	0.4	0.22	0.3949	2.09	20	160.6	0.386	154.5
450	1	0.2	0.28	0.4609	2.32	20	173.3	0.384	153.7
500	0.5	0.4	0.26	0.3948	2.09	20	160.6	0.386	154.5
500	1	0.2	0.33	0.4605	2.32	20	173.3	0.384	153.7
500	0.5	0.6	0.20	0.3898	2.48	20	140.6	0.393	157
600	0.5	0.4	0.34	0.3945	2.09	20	160.6	0.386	154.5
600	1	0.2	0.45	0.4599	2.32	20	173.3	0.384	153.6
600	0.5	0.6	0.27	0.3895	2.48	20	140.6	0.392	157
700	0.5	0.6	0.35	0.3894	2.48	20	140.6	0.392	157
700	1	0.4	0.29	0.479	2.76	20	111.9	0.386	154.2
700	0.5	0.8	0.30	0.3853	2.87	20	131.1	0.397	158.7
800	1	0.4	0.36	0.4786	2.76	20	111.9	0.386	154.2
800	0.5	0.8	0.38	0.3852	2.87	20	131	0.397	158.7
800	1	0.6	0.25	0.4866	3.17	20	91.66	0.388	155.1
900	1	0.4	0.44	0.4784	2.76	20	111.9	0.385	154.2
900	1	0.6	0.31	0.4864	3.17	20	91.67	0.388	155.1
900	1.5	0.4	0.38	0.5412	3.38	20	96.2	0.385	154.1
1000	1	0.5	0.44	0.483	2.97	20	99.66	0.386	154.6
1000	1	0.6	0.38	0.4862	3.17	20	91.66	0.388	155
1000	1.5	0.4	0.46	0.5408	3.38	20	96.21	0.385	154.1
2000	2	1	0.65	0.6497	5.3	20	52.3	0.384	153.8
2000	2.5	1	0.59	0.7165	5.93	20	47.77	0.382	152.8
2000	2	1.5	0.49	0.6697	6.34	20	45.09	0.385	154.1
2500	2.5	2	0.59	0.7682	8.04	20	37.03	0.381	152.6
3000	3.5	1.5	0.88	0.8866	8.27	20	34.97	0.377	150.8
3000	3	2	0.79	0.8485	8.7	20	33.73	0.378	151.3
3000	3.5	2	0.74	0.9262	9.35	20	31.47	0.375	150.2
6000	9	4	1.71	1.868	20.7	20	16.72	0.357	142.9
6000	8	5	1.63	1.823	21.6	20	16.5	0.356	142.6
6000	7	6	1.62	1.719	22.4	20	16.97	0.357	142.7
7000	9	6	2.01	2.047	25.1	20	14.86	0.354	141.5
8000	12	6	2.41	2.48	29	20	12.93	0.351	140.5
8000	14	5	2.51	2.598	29.2	20	12.9	0.352	140.8
8000	11	7	2.35	2.425	29.9	20	12.9	0.351	140.2
9000	14	7	2.76	2.853	33.7	20	11.47	0.349	139.6
9000	13	8	2.69	2.801	34.6	20	11.42	0.348	139.3

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
9000	12	9	2.67	2.712	35.4	20	11.58	0.348	139.2
10000	16	8	3.13	3.223	38.4	20	10.33	0.347	138.8
10000	15	9	3.04	3.174	39.3	20	10.26	0.347	138.6
10000	14	10	3.02	3.093	40.2	20	10.37	0.346	138.5
11000	16	11	3.41	3.472	44.9	20	9.445	0.345	137.9
11000	16	12	3.34	3.534	47.1	20	9.255	0.344	137.7
11000	15	13	3.34	3.417	47.8	20	9.427	0.344	137.6
Frequency = 35 GHz									
	Z_o = 50 Ω, Metal Thickness = 0.35 μm								
500	0.5	0.4	0.26	0.3948	2.09	20	160.8	0.386	154.5
500	1	0.2	0.33	0.4608	2.32	20	173.6	0.384	153.6
500	0.5	0.6	0.20	0.3918	2.48	20	141	0.391	156.5
2500	2.5	2	0.65	0.7786	8.06	20	38.25	0.379	151.7
	Z_o = 75 Ω, Metal Thickness = 0.35 μm								
5000	3	3	2.12	3.003	15	20	29.32	0.528	93.93
	Z_o = 100 Ω, Metal Thickness = 0.35 μm								
5000	2.5	2	2.76	5.834	18.2	20	35.32	0.701	70.08
Frequency = 40 GHz									
	Z_o = 50 Ω, Metal Thickness = 0.35 μm								
500	0.5	0.4	0.26	0.3942	2.09	20	161.2	0.387	154.6
500	1	0.2	0.33	0.4605	2.32	20	174.2	0.384	153.7
500	0.5	0.6	0.20	0.3913	2.48	20	141.6	0.392	156.6
2500	2.5	2	0.70	0.7896	8.08	20	39.6	0.377	150.8
	Z_o = 75 Ω, Metal Thickness = 0.35 μm								
5000	3	3	2.28	3.028	15.1	20	30.18	0.527	93.65
	Z_o = 100 Ω, Metal Thickness = 0.35 μm								
5000	2.5	2	2.94	5.865	18.2	20	36.14	0.700	69.96
Frequency = 45 GHz									
	Z_o = 50 Ω, Metal Thickness = 0.35 μm								
500	0.5	0.4	0.26	0.3943	2.09	20	161.5	0.386	154.6
500	1	0.2	0.34	0.461	2.32	20	174.6	0.384	153.6
500	0.5	0.6	0.21	0.3917	2.48	20	142.2	0.391	156.6
2500	2.5	2	0.76	0.7991	8.1	20	40.8	0.375	150

Table A.1 – continued from previous page

L	W_S	W_G	S_{min}	$S(Z_o)$	W_T	R_{tr}	R	L	C
Frequency = 50 GHz									
	$Z_o = 50\ \Omega$								
	Metal Thickness = 0.35 μm								
500	0.5	0.4	0.26	0.3949	2.09	20	162	0.386	154.5
500	1	0.2	0.34	0.4619	2.32	20	175.2	0.384	153.4
500	0.5	0.6	0.21	0.3921	2.48	20	142.7	0.391	156.5
2500	2.5	2	0.81	0.8079	8.12	20	41.92	0.373	149.3

APPENDIX B

ADDITIONAL TRANSMISSION LINE SIMULATION FIGURES

B.1 Transmission Line Driver and Buffer Comparisons

Figures B.1 through B.8 show the amount of overshoot for above V_{DD} and below ground for various driver and buffer setups. Section 4.2.1 describes this and other driver comparisons in more detail.

B.2 Receiver Comparisons

Figures B.9 through B.12 show the amount of overshoot for above V_{DD} and below ground for various receivers. Section 4.3.2 describes this and other receiver comparisons in more detail. Also, refer to Figure 4.23 for the receiver comparisons legend.

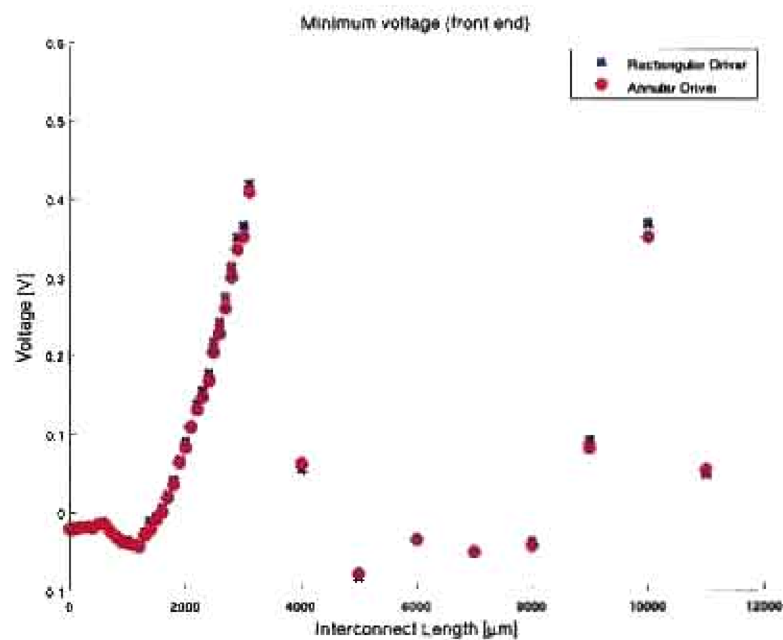

Figure B.1. Overshoot below ground at transmission line front end (conventional buffer, annular driver)

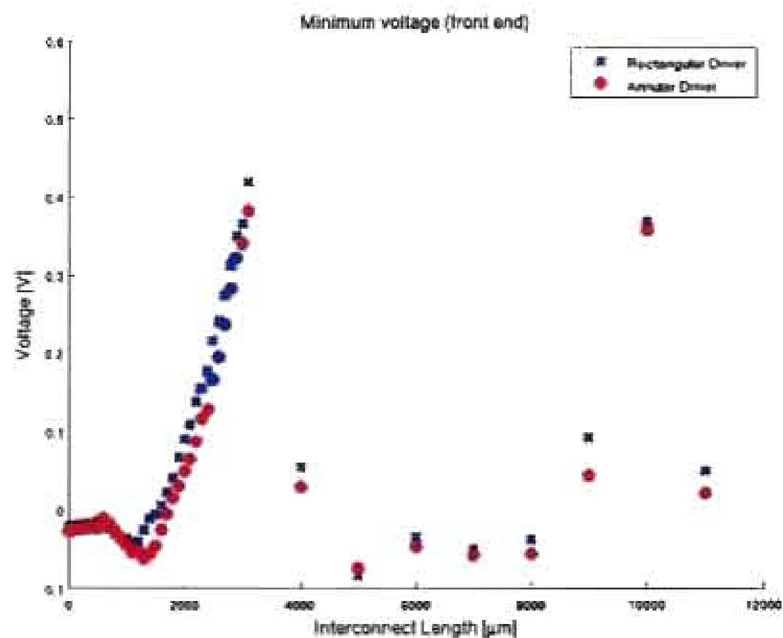

Figure B.2. Overshoot below ground at transmission line front end (annular buffer, annular driver)

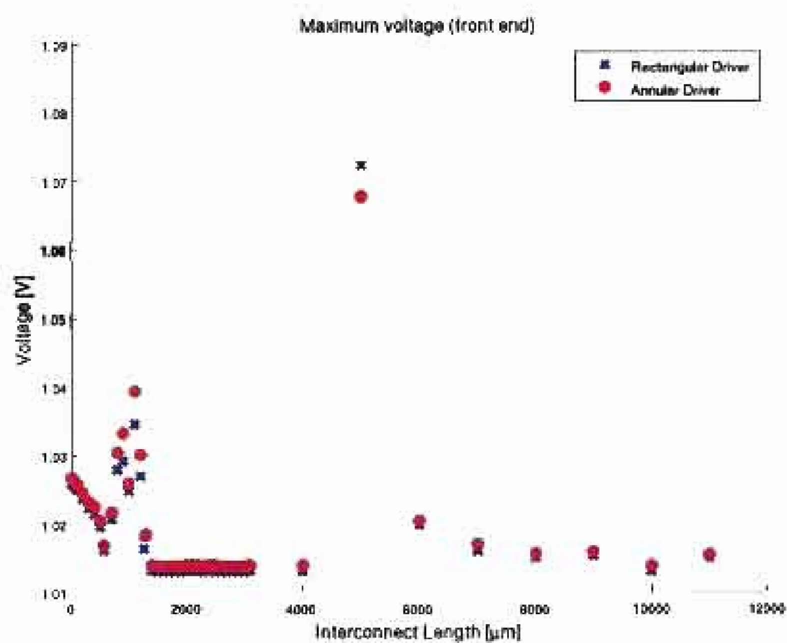

Figure B.3. Overshoot above V_{DD} at transmission line front end (conventional buffer, annular driver)

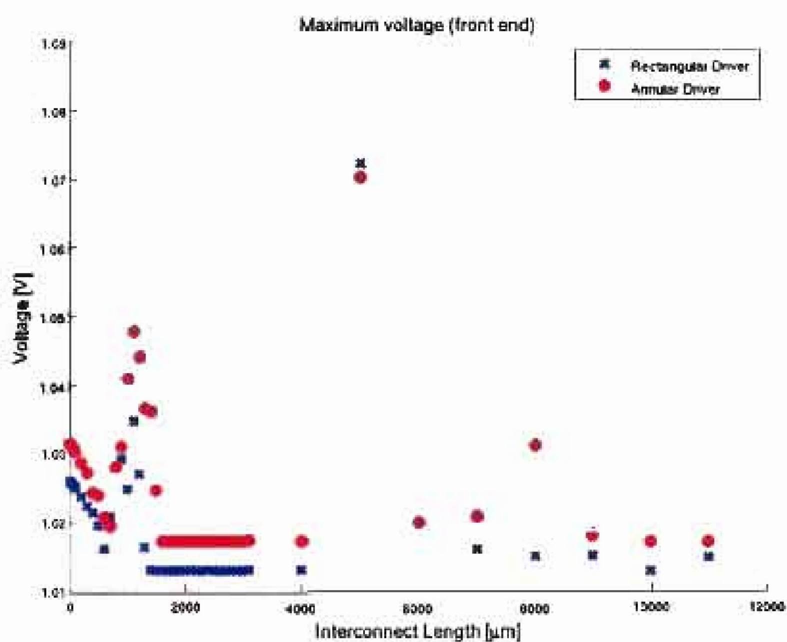

Figure B.4. Overshoot above V_{DD} at transmission line front end (annular buffer, annular driver)

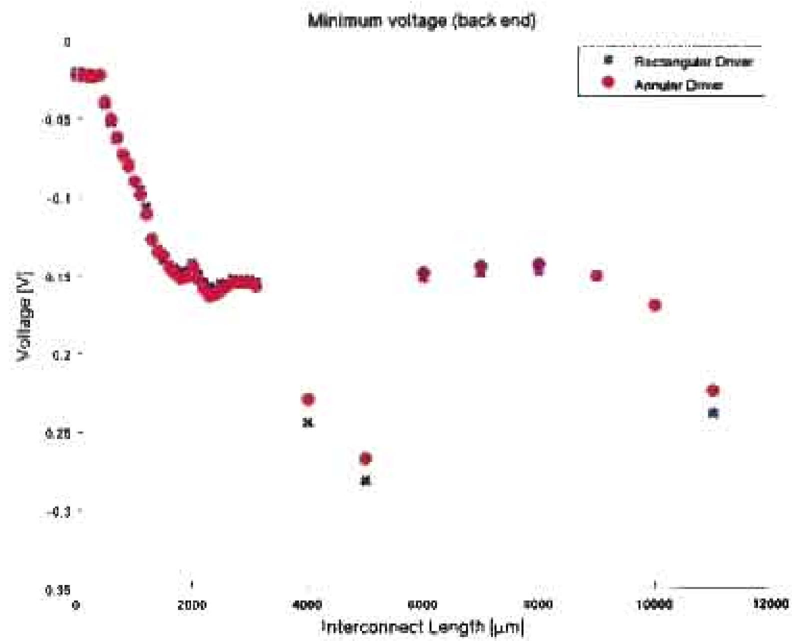

Figure B.5. Overshoot below ground at transmission line back end (conventional buffer, annular driver)

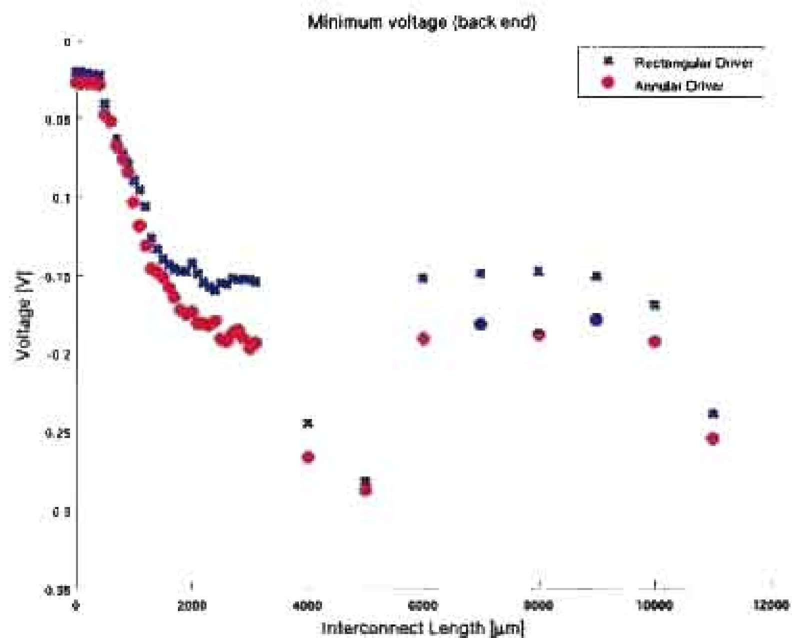

Figure B.6. Overshoot below ground at transmission line back end (annular buffer, annular driver)

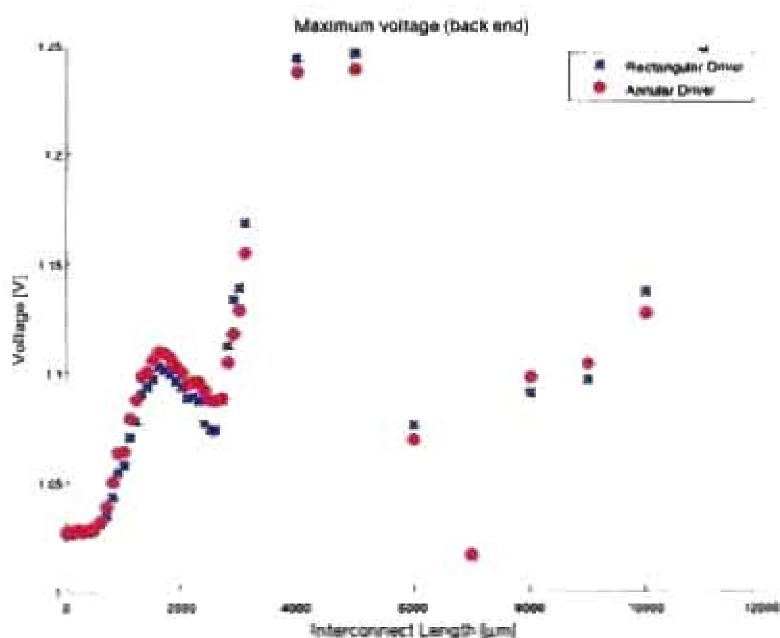

Figure B.7. Overshoot above V_{DD} at transmission line back end (conventional buffer, annular driver)

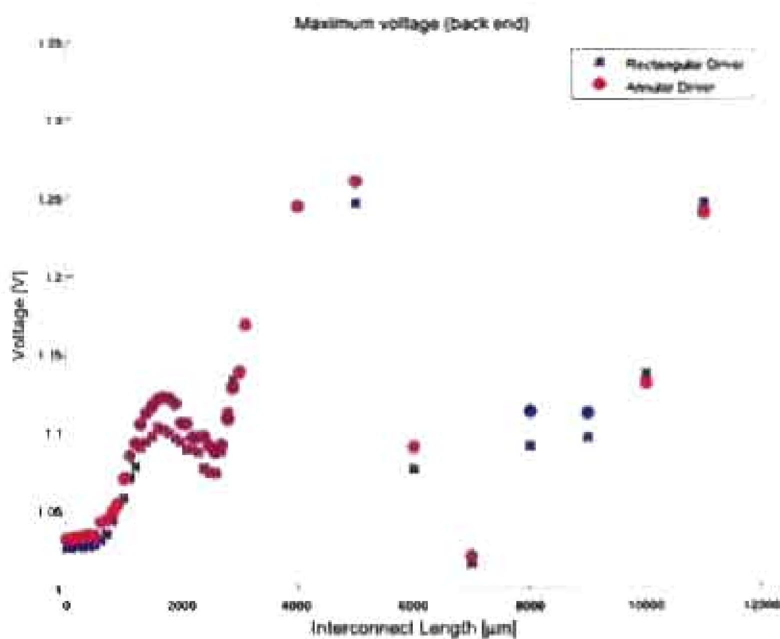

Figure B.8. Overshoot above V_{DD} at transmission line back end (annular buffer, annular driver)

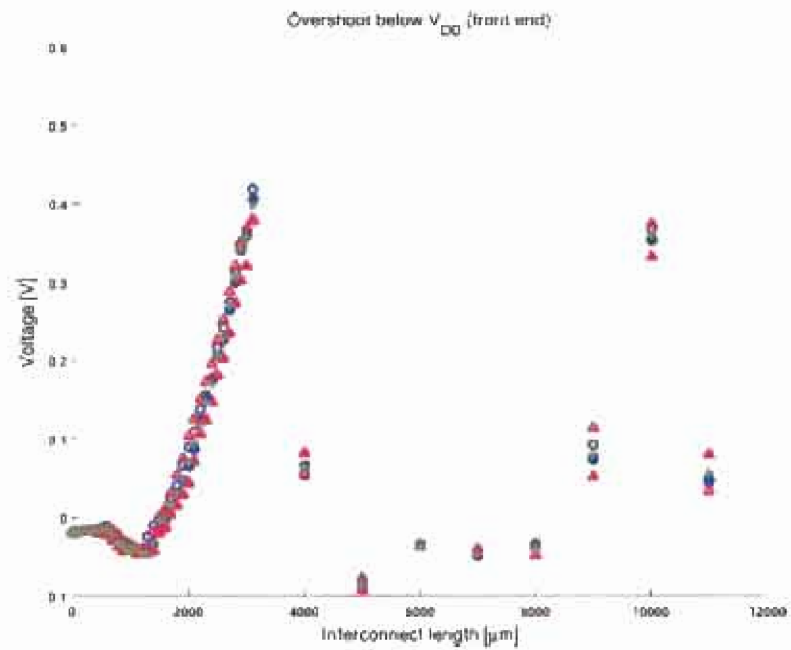

Figure B.9. Minimum voltage (front end) - various receivers

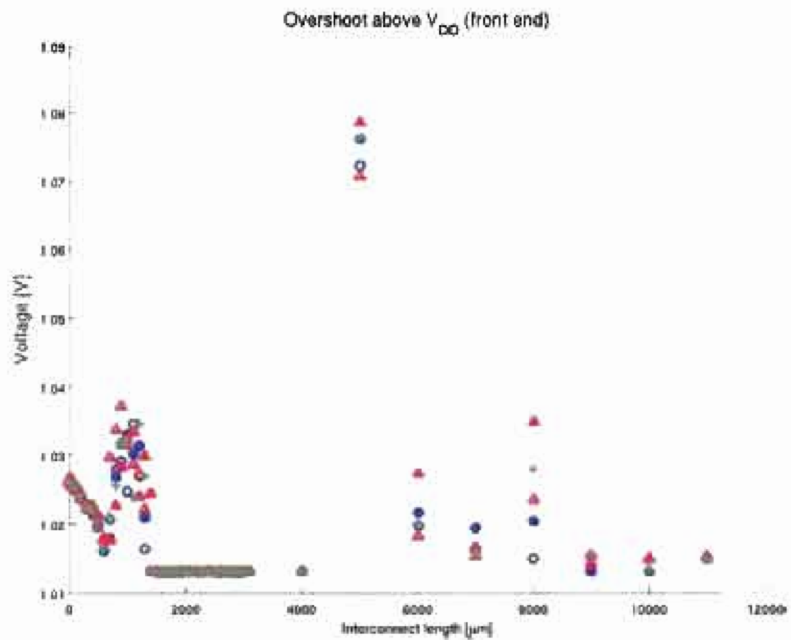

Figure B.10. Maximum voltage (front end) - various receivers

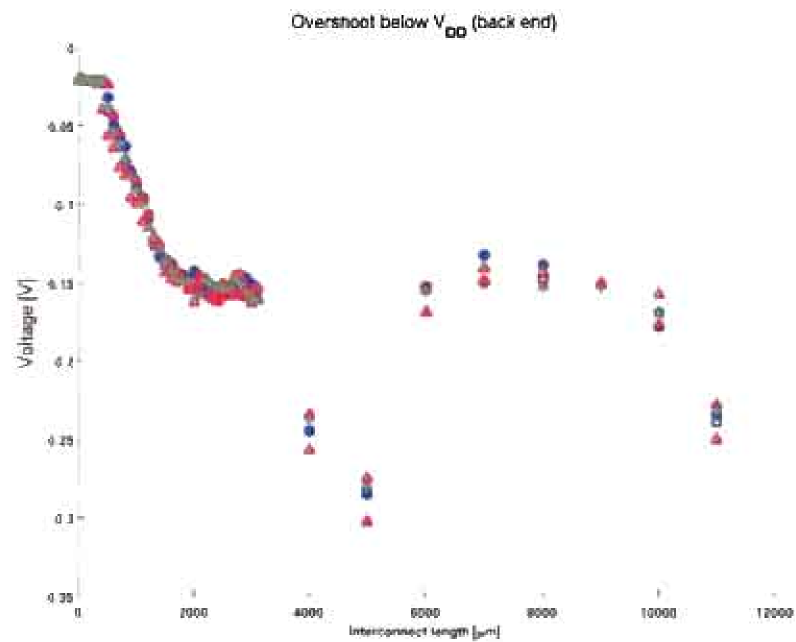

Figure B.11. Minimum voltage (back end) - various receivers

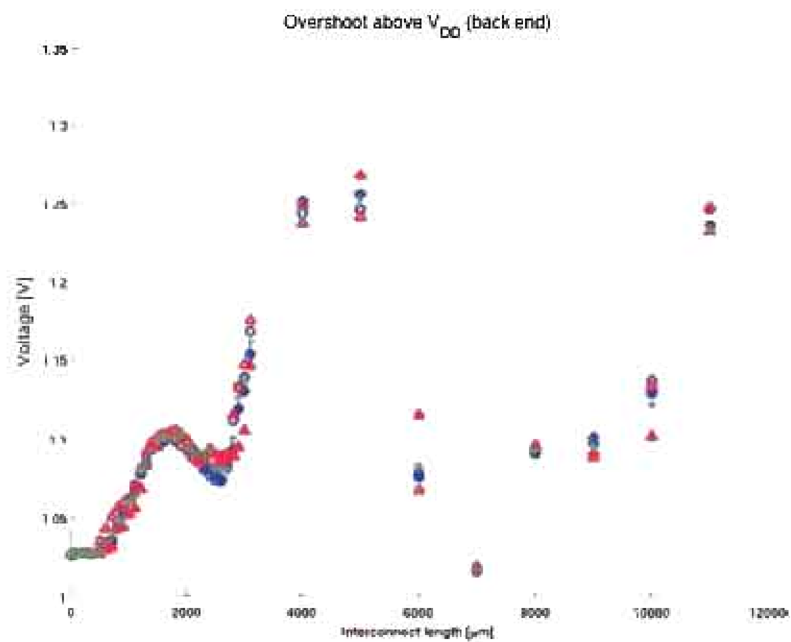

Figure B.12. Maximum voltage (back end) - various receivers

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