# FUNDAMENTAL INVESTIGATION OF HIGH TEMPERATURE OPERATION OF FIELD EFFECT TRANSISTOR DEVICES

by

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A dissertation submitted to faculty of
The University of Utah
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Department of Materials Science and Engineering

The University of Utah

December 2011

# The University of Utah Graduate School

## STATEMENT OF DISSERTATION APPROVAL

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# ABSTRACT

In this dissertation copper germanium (CuGe)-based materials were investigated as potential ohmic contacts to n-type gallium arsenide (GaAs). The CuGe-based contacts to GaAs were found to not form any reaction products with GaAs and to have low contact resistance comparable to that of nickel gold germanium (NiAuGe) ohmic contacts to GaAs. The potential for high temperature applications using CuGe ohmic contacts was investigated. A guideline for further reduction of the contact resistance has been achieved after investigating the detailed mechanism of the formation of binary CuGe contacts over a wide range of Ge concentrations. The thermal stability of CuGe contacts was significantly enhanced and improved by introducing a diffusion barrier, titanium tungsten nitride ($TiWN_x$), and a gold (Au) overlayer for high temperature applications.

Novel approaches such as epitaxial thulium phosphide (TmP) Schottky contacts and the utilization of low temperature (LT)-aluminum gallium arsenide (AlGaAs) were also investigated in this dissertation and likely will be the standard technologies for a new generation of high-temperature electronics.

Inserting a layer of aluminum arsenide (AlAs) underneath the channel of a GaAs-based MESFET was found to reduce substrate leakage currents by a factor of 30 compared with the same MESFET directly fabricated on a semi-insulating GaAs substrate. In addition to AlAs, and $Al_xGa_{1-x}As$ materials, new

materials grown at low temperatures such as LT-AlGaAs were used in heterojunction FET structures as a back wall barrier. Low drain leakage currents were achieved using AlAs and LT-AlGaAs as the back wall barriers. Some fundamental properties regarding these materials are of great interest and in need of further characterization.

Part of the work in this dissertation was devoted to the characterization of device performance for different structure designs at elevated temperatures. The suitability of GaAs-based and gallium arsenide (GaN)-based MESFET, JFET, pseudomorphic-HEMT, and modulation doped FET (MODFET) devices for high-temperature applications were investigated and addressed in terms of device performance such as transconductance, leakage current density, and current gain. Wide gap materials such as GaN have low carrier generation rate at high temperatures and, hence, high operation temperature capabilities and potential.

To my parents

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# ACKNOWLEDGMENTS

I have been fortunate to interact with many people who have influenced me greatly. One of the pleasures of finally finishing is this opportunity to thank them.

I would like to express my sincere gratitude to my advisers, Dr. L. P. Sadwick and Dr. R. J. Hwu, who regarded me as a friend rather than as a student, for their effortlessly supervisory work. They treated me as though what I thought was important. They have both wide-ranging interests and the ability to think clearly about their interests, in a highly original and probing way. The academic environment of their group is one of the most stimulating and encouraging ones.

I also give special thanks to Drs. Richard. M. Cohen, John Worlock, and Jeff Shield for being supportive in development and writing of this dissertation. It is not possible to summarize how much I owed to all my friends and colleagues in a paragraph, particularly the staff of HEDCO lab, Jack, Issue, and LaRue. This work would not be complete without their helpful discussion and valuable assistance.

I would like to dedicate this dissertation to my parents for their unconditional love and support.

# CHAPTER 1

# INTRODUCTION

## 1.1 Applications of high-temperature electronics

The best definition of “high temperature electronics” is electronics operating at temperatures in excess of those normally encountered by conventional, silicon (Si)-based semiconductors or their auxiliary components [1]. The realm of “high temperature electronics” covers a wide range of applications and has to satisfy different criteria [1].

A brief list of the applications of electronics at high temperatures is given below:

1. Intelligent sensors for application in automobile engine management system [1-3], jet engine sensors, actuators, control electronics [4], and intelligent drill heads for subterranean exploration of petroleum and minerals [5].
2. High speed computing units for jet engine testing [6].
3. Reduction of cooling loads for both military applications [7], and supersonic aircraft technology [8].
4. Spacecraft power conditioning electronics and sensors, nuclear and satellite technology [9,10].

Each of the applications has demands on reliable and accurate data acquisition and, frequently, the environment in one application is more stringent

than in the others. All the demands, on the other hand, represent many technical challenges and will require solutions for the high temperature electronic industry.

## 1.2 Physical considerations of devices at elevated temperatures

Assuming device materials can withstand short periods of time at elevated temperature, some detrimental characteristics are most notable: (1) the change in the threshold voltage, (2) the reduction in transconductance and (3) the increase in leakage currents. The most significant of these in terms of device failure is the increase in leakage currents, which can lead to a total loss of transistor-like operation [135].

In a conventional field-effect transistor (FET) with an n-type channel and a p-type gate, two leakage mechanisms, generation-recombination and diffusion, arise from two sources in the off state - both as a result of the reverse biased pn drain junction [45].

The generation-recombination term can be approximated as: [45]

$$J_{G-R} \approx \frac{qW}{2\tau} n_i \qquad (1)$$

where $W$ is the junction depletion layer width, $\tau$ is the minority carrier lifetime, $q$ is the electron charge and $n_i$ is the material intrinsic carrier concentration. Secondly, a diffusion leakage term ( for $N_A >> N_D$ ) which can be approximated as: [45]

$$J_{Diff} \approx q\sqrt{\frac{D_p}{\tau}}\frac{n_i^2}{N_D} \tag{2}$$

$$n_i = \sqrt{N_V N_C}\ \ e^{-E_g/2kT} \tag{3}$$

where $D_p$ is the hole diffusivity and $N_D$ is the donor dopant concentration, $N_V$ and $N_C$ are the effective density of states in the valence and conduction bands, respectively, $k$ is the Boltzmann constant, $T$ is the temperature and $E_g$ is the energy band gap.

From equations (1) and (2),

$$\frac{\partial J_{G-R}}{\partial T} \propto n_i \tag{4}$$

$$\frac{\partial J_{Diff}}{\partial T} \propto n_i^2 \tag{5}$$

This results generally in a low-temperature *G-R* dominated leakage and a high-temperature diffusion dominated leakage behavior. Many investigations of high temperature devices have conclusively shown that the physical situation is far more complex than the G-R-diffusion theory [131-133] predicts. One key component of the leakage is the additional conduction path developed to the substrate material which can lead to a significant contribution to the overall leakage current. Apparently, the intrinsic carrier concentration is the major temperature dependent parameter among all the leakage mechanisms.

Therefore, a reduction in intrinsic carrier concentration by increasing the energy band gap of the semiconductor material should lead to a reduction in the leakage current. Using gallium arsenide (GaAs) rather than Si, in principle, can achieve the reduction in leakage because the former has an almost 30% larger energy band gap and the leakage current is exponentially related to the energy band gap.

## 1.3 Technical challenges in high temperature electronics

The most promising technique for high temperature electronics is probably vacuum tubes, but their size, weight, and lack of large-scale integration preclude their use in many applications. Wide band-gap semiconductors have shown great potential for use in high temperature applications. However, one of the challenges is that the semiconductor materials required to produce high temperature components are in short supply and not of sufficient purity to produce high quality devices. For example, silicon-on-insulator (SOI) technology extends the useful range of silicon to above 250°C, but wafers are difficult to make and only a handful of companies manufacture them. For temperatures above 300°C, a wide band-gap semiconductor is needed. Silicon carbide (SiC), when it is formed into wafers from which components are made, is beset with a problem known as micropipes [11, 12]. The problem is most serious for components designed to handle high power, since they tend to not only be high voltage devices but also high current devices.

In the long term, the emerging technologies of SiC and diamond have the potential to provide electronic circuits operating at temperatures of 500°C and

above. Gallium nitride (GaN) technology seems to have taken off and to be a very promising candidate in terms of the maturity of material growth and processing techniques, benefiting from the manufacturing of optical components such as blue LEDs and blue lasers. In the short term, SOI and GaAs technologies are also suitable for high temperature operation and further exploration. A significant effort has been concentrated on GaAs as a high temperature material because of the relatively mature process and fabrication technology. As the ambient temperature increases, some physical considerations and fundamental obstacles have to be understood and addressed to improve the device performance at high temperatures.

## 1.4 Strategy of high temperature electronics and high temperature electronic technology (HTET)

By examining the simulated results on devices at high temperature, three general parameters can be extracted that significantly contribute to the total leakage current at high temperature in GaAs technology [45]:

1. Material band gap energy- The band gap effectively determines the intrinsic carrier densities of a given semiconductor material and, thus, also the leakage currents, assuming that the quality of the material is nearly perfect, at elevated temperatures.
2. Gate barrier height – In terms of high temperature operation, the gate barrier height for field effect transistors determines the ability of the device to suppress gate contact leakage currents.

3. Back wall barrier – This represents the height of the potential barrier (if any) between the active region and the bulk that provides a barrier to substrate leakage.

The high temperature electronic technique invented by Sadwick and Hwu et al. [89] employs a substrate bias of ~1.0 V higher than the $Vds_{max}$ (for n-channel devices) and has proven very effective for correcting the device parameters, i.e., output resistance and leakage current, at high temperature. The significance of the HTET is that higher breakdown voltage and stabilized device performance at elevated temperatures were achieved by increasing the barrier height and reverse-biasing the junction through the control of the substrate bias.

The value of having a device which functions at elevated temperatures without the need for additional arrays of techniques cannot be overemphasized. Also, it is very desirable to enhance the compatibility of integrating all kinds of circuits together. Generically, engineering the leakage currents at high temperature through a technology like HTET or a structure design involving no additional complex process steps is the ultimate goal when one is pursuing the high temperature technology using semiconductors.

## 1.5 Fundamental obstacles and associated accomplishments of this dissertation work

### 1.5.1 Ohmic contacts

The basic principle of ohmic contact formation to semiconductors is twofold : first, to reduce the width of the potential barrier which results in easier

carrier transport via, for example, tunneling; second, to reduce the barrier between the contacts and semiconductors by forming a small band-gap semiconductor that, for example, transitions to a heavily doped semiconductor/semimetallic layer immediately underneath the contact.

Ohmic contacts can be divided into two categories: alloyed ohmic contacts and nonalloyed ohmic contacts. Many types of nonalloyed contacts have been contemplated. These nonalloyed contacts include the growth of $n^{++}$Ge on GaAs by MBE which relies on the small band discontinuity between Ge and GaAs and the small barrier height of the subsequent Au contact to $n^{++}$Ge [14], the use of solid phase epitaxy of Ge [3], the use of a conductive compound such as NiSb [16], and the use of heavily doped graded InGaAs epitaxially grown on GaAs [17,18]. All of these examples rely on MBE growth, an ultrahigh vacuum material growth process tool. In addition to this, the selection of materials with the smallest lattice misfit with respect to GaAs, lower band-gap energy than that of GaAs, and high processability is part of the very challenging work in developing a new ohmic contact system.

The most common approach to fabricating ohmic contacts to GaAs is to apply an appropriate metallization scheme to the respective devices on the wafer, and then alloy the metal into GaAs. During the alloying and cooling period, one or more components of the metallic contact scheme enters into the GaAs and heavily dopes the surface layer of the GaAs or GaAs-based alloy or compound. From this point of view, silicon (Si), germanium (Ge), tin (Sn), selenium (Se), and tellurium (Te) will be suitable candidates that can be added into the contact

scheme for n-type GaAs, while zinc (Zn), cadmium (Cd), beryllium (Be), and magnesium (Mg) are used for p-type GaAs.

A simple metallization scheme, based upon the concept of solid-state epitaxy [19], involves the deposition of a transport layer, palladium (Pd), onto which a layer of amorphous Ge is then deposited without breaking vacuum. The thickness of the Ge and Pd layers are chosen such that, upon annealing, the Pd layer is completely consumed in the formation of the palladium germinide layer. The remaining Ge is then transported through the germinide to grow epitaxially on the GaAs substrate. The solid-state epitaxy (or regrowth) contacts rely on control of both kinetics and thermodynamics and are formed after driving the reaction to completion. High reliability and low contact resistance can then be both satisfied by manipulating the reaction to an optimum step [20-24]. However, substantial metallurgical interaction and electrical degradation were observed in all Pd(Ni)/Ge-based metallizations after typically 2 hours of annealing at 400°C [19-24].

Indium (In)-based ohmic contacts utilize the formation of epitaxial regrown indium gallium arsenide (InGaAs), which has a small band-gap energy, between the contact and GaAs and results in low-band-gap ohmic contacts. Tungsten (W), copper (Cu), and/or nickel (Ni) are also sometimes used as constituents in ohmic contacts to III-V semiconductor materials. Pd/In(Ge) [22], Pd/In [25], Pd/In/W [26], Ni/In/W [27-31], and Ni/Si(Ge)/In/W [32] contacts were designed to induce the regrowth of InGaAs during the contact formation, while refractory metals such as W were used to enhance the high degree of thermal stability. The Ni/In/W contacts exhibited excellent thermal stability: no change in contact resistance

was observed at 400°C after 100 hours and at 500°C after 10 hours and only a small increase in contact resistance (about $5x10^{-7}$ $\Omega cm^2$) was observed after 500°C for 100 hours. This is the best thermal stability ever achieved for In-based ohmic contacts.

In addressing Ge-based contacts, nongold contacts such as NiGe [33-35], NiGeWN [3], PdGe [30-34], and CuGe [37-39] contacts have been developed. Only NiGeWN had excellent thermal stability, but the contact resistance and the fabrication process need to be improved. The archetypal system, and, indeed, the work-horse of industry, remains the Au-Ge-based system for n-type GaAs, which has been universally adopted ever since Braslau et al. [13] introduced it in the mid 1960s. However, the Au-Ge-based contact system is thermally and electrically unstable above 300°C upon subsequent annealing [40-43].

CuGe-based materials have been investigated as ohmic contacts to n-type GaAs and have low contact resistivity compatible to that of NiAuGe contacts [13]. Their potential for high temperature applications was explored by the observation of no reaction products between contact materials and GaAs [37-39] coupled with the high peritectoid temperature point of 636°C for reaction $\varepsilon_2 + \varepsilon \rightarrow \varepsilon_1$ for Ge composition from 73.9% to 75.2% [43,45].

Based on the forgoing, the purpose of this dissertation work is twofold. The first is to obtain a guideline for further reduction of the contact resistance by investigating the detailed formation mechanism of the binary CuGe contacts with a wide range of Ge concentrations. The second purpose of this dissertation is to improve the thermal stability of CuGe contacts by introducing a diffusion barrier,

such as $TiWN_x$, and a gold (Au) overlayer for high temperature applications. It is also highly desirable to stabilize the CuGe binary contacts if the contact resistance is inevitably degraded at high temperatures. In, Ni, and molybdenum (Mo) are possible candidates to stabilize the interfaces.

Many attempts have been made to meet the most demanding requirement of a contact metallurgy for high-temperature electronics - finding a contact scheme that does not react with the semiconductor at elevated temperatures and has reliable and stable electrical and metallurgical properties. As to the question, what properties should an “ideal” contact metallization system have? Generally speaking, it should be thermally stable and environmentally robust, and microstructurally and electrically uniform.

However, the progress of adapting reliable contacts to GaAs has not yet resulted in a technology that is feasible for high temperature applications. With application demands soaring for devices and circuits capable of operating up to 400°C for GaAs and other technologies, ohmic contacts to compound semiconductors have been the major reliability issue.

### 1.5.2 Schottky contacts

Besides the criteria mentioned above, in the past two decades, Schottky barrier heights and their trends with semiconductors and metals have been the subject of both fundamental and phenomenological studies. Enhancing the barrier height to an extremely high value for reducing the drain leakage currents in a reverse biased gate-drain junction requires special care on materials selection and structure design in GaAs-based electronic devices [46,47].

Monolithic GaAs Schottky contact systems fall into two categories: aluminum (Al)-containing and Al-free. With only a few exceptions, Al-free contacts, including elemental, alloy, and compound contact materials, form Schottky barrier heights (SBHs) in the range of 0.7 ~ 0.85 eV [46,50-61], while the Al-containing ones, Al [62], W-Al [63-65], Ni-Al [66-69], Pt-Al [70], Ir-Al [71], Mo-Al [72,73], Pd-Al [74] and Ta-Al [75], form higher SBH values after annealing the contacts at temperatures between 400°C and 800°C. SBH values higher than 1.0 eV have been reported and attributed to the enhancement of the formation of $Al_xGa_{1-x}As$ below the ohmic contact during the annealing processes [66,74]. $Al_xGa_{1-x}As$ has a larger bandgap energy than GaAs and, consequently, in general, a larger Schottky barrier height (SBH) than that of GaAs.

As the growth of $Al_xGa_{1-x}As$ alloys improves, it has become essential to thoroughly characterize these materials because epitaxial growth is superior to metallization, including in the formation of contacts, as far as control, reproducibility and uniformity are concerned. If a solid relationship between Al-composition and SBH can be built up empirically or theoretically, not only can the device performance be engineered, but also, more importantly, the uniformity of SBH values can be improved. For example, the barrier heights of gate metal/semiconductor systems are not presumably controlled by metallization parameters alone but also by growth parameters [75]. Many attempts have focused on the surface states of AlGaAs materials and the results on Schottky contacts/AlGaAs were shown to be processing dependent rather than conclusively related to Al compositions [75-88].

It is well known that the barrier heights of the metal to GaAs systems are limited to a range of 0.7 to 0.9 eV because the Fermi energy is pinned at an energy near one-third of the band-gap energy as measured from the valence band edge. This range of barrier heights is not large enough for high temperature applications and limits the operation temperatures to about 200°C for GaAs technology. Among all field effect transistors, except junction field effect transistors (JFETs), metal Schottky contacts to semiconductor are integral parts in many devices such as modulation doped field effect transistors (MODFETs) and metal emitter semiconductor field effect transistors (MESFETs). Even with an SBH value as high as 1.0 eV, GaAs MESFETs will have a gate-limited leakage current density of $2x10^{-5}$ A/μm at 300°C [91], thus limiting the applications to lower temperatures. The prediction of device performance is based on simulations using analytical models modified with empirical results to agree with the observed measurement results [91].

However, unlike GaAs, $Al_xGa_{1-x}As$ surfaces are very reactive, especially at high aluminum concentrations and, hence, place some stringent requirements on metal/semiconductor systems employing $Al_xGa_{1-x}As$. Among the possible detrimental effects, DX centers [116], oxidation, and material quality play important roles and should be taken into consideration in device structure design [88]. The effects of the Al content on the SBH in $Al_xGa_{1-x}As$ materials are of great importance if the SBH is to be higher than 1.2 eV.

Novel approaches such as epitaxial Schottky contacts and the utilization of LT-AlGaAs open up new possibilities and likely will be the standard

technologies for the next generation of high-temperature electronics for the following reasons:

1. The fabrication of metal contacts on semiconductors is becoming the foremost issue in VLSI fabrication, because they are, to date, the major size and speed limiting factors. For example, the growth by molecular beam epitaxy of Al/$Al_xGa_{1-x}As$ Schottky barriers can produce nearly ideal interfaces which have been instrumental in clarifying and elucidating the role of the band structure of $Al_xGa_{1-x}As$ in the transport mechanism [77,88]. These structures are ideal test beds for the various theories on Schottky barriers. An important question associated with this approach is the thermal stability of the metal/semiconductor interface.
2. Grain boundaries serve as a sink of atoms and fast diffusion paths allowing reactions, contamination and electromigration to take place [90]. There is no doubt that current transport through these defects will be much easier than in the monocrystalline materials. Therefore, contacts should be ultimately monocrystalline and epitaxial.
3. LT-GaAs and AlGaAs buffer layers are commonly used to reduce backgating and output conductance and increase breakdown voltage, as well as in high speed detectors [109-115]. The resistivity of LT-AlGaAs following proper annealing after growth is in the range of $1x10^{11}$ ~ $1x10^{12}$ Ωcm [103] at room temperature, which is remarkably higher than that of semi-insulating GaAs, typically, around ~ $1x10^{8}$ Ωcm. This insulator-like behavior provides for the possibility of metal-insulator-semiconductor field effect transistor (MISFET) structures. Analogous to MOSFETs, the gate

leakage current normally is not a concern as long as the quality of insulator is assured. However, the surface states on GaAs presumably limit the performance of the MISFET [85,117]. To date, there is no report on the mechanism of carrier transport for the metal/LT-AlGaAs interface.

### 1.5.3 Back wall barriers

Thermal currents at elevated temperatures were first characterized by Sadwick and found not to be influenced or controlled by the gate bias, contributing significantly to the drain leakage current for MESFET devices at high temperatures [118]. Since demonstrated by Lee et al. [119], the back wall barrier has become the standard approach for eliminating substrate leakage in terms of its efficiency and convenience. Inserting a layer of AlAs underneath the channel was found to reduce substrate leakage currents by a factor of thirty, compared with the same MESFET fabricated on a semi-insulating GaAs substrate. The concept of semiconductor-on-insulator (SOI) can be implemented on GaAs using wide-gap materials such as AlAs and AlGaAs since they are lattice matched to the GaAs substrate [126,127]. New materials grown at low temperatures, such as LT-AlGaAs, are attractive for their high resistivities at room temperature after appropriate annealing procedures. Reported resistivity values for LT-AlGaAs grown at 300°C is in the range of $10^{11}$ Ωcm to $10^{12}$ Ωcm after annealing [103]. Calculated resistivity at 400°C shows lower conductivity for this material compared with that of AlAs materials. It should be noted that such work and efforts are still in the early stages for adopting LT-AlGaAs into high temperature

devices. Some fundamental properties regarding these materials are still of great interest and in need of further characterization.

### 1.5.4 Structure design

The suitability of MESFET, JFET, HEMT), and heterojunction bipolar transistor (HBT) devices for high-temperature applications have been reviewed [119-128] in terms of device performance such as transconductance, leakage current density, and current gain. The utilization of heterojunctions has become inevitable according to the reported results [131,134]. Regardless of the criticisms of being potentially high cost, low yield, and less technology-competitive, the methodology of introducing heterojunctions into device design has been shown to be feasible and promising. Part of the work in this dissertation is devoted to the characterization of device performance for different structure designs at elevated temperatures. The performance of different devices will be compared and some conclusions will be made and presented as the guideline for GaAs high temperature electronics.

### 1.5.5 Process design

Process design certainly plays an important role in accounting for the success of device applications. Leakage currents across the surface of GaAs become severe at temperature higher than 250°C [129]. Mesa isolation technology needs to be modified since a quasiplanar structure is easy to accomplish. Attempts for developing a new technique that is capable of avoiding extra leakage current such as implantation in device isolation should be

addressed. Implementations of this technology result in no contact to areas outside the active region and were found to be an ideal structure for the measurement of substrate and gate leakage at high temperatures.

## 1.6 References


1. R. B. Brown, F. L. Terry, and K. Wu, IEDM Tech. Digest (1987) 274.

2. F. S. Shoucair, J. Microelectron. 22 (1991) 39.

3. D. E. Cusack, W. M. Glasheen, and H. R. Steglich, 2nd HiTEC, Charlotte, NC, 1994, p. III-17.

4. S. Przybylko, 26th Joint Propulsion Conference, 1990, p.1.

5. A. F. Veneruso, 1st Int. HiTEC, Albuquerque, 1991.

6. W. C. Nieberding and A.J. Powell, IEEE Trans. Ind. Electron. IE29 (1982) 103.

7. W. G. Taschek, 1st Int. HiTE, Albuquerque, 1991.

8. D. W. Christenson, 1st Int. HiTEC, Albuquerque, 1991.

9. A. N. Hammoud, 1st Int. HiTEC, Albuquerque, 1991.

10. R. F. Jurgens, IEEE Trans. Ind. Electron. IE29 (1982) p. 107.

11. J. A. Powell, D. J. Larkin, L. Zhou, and P. Pirouz, Third Int. HiTEC, Albuquerque, NM, 1996, p. II-3,.

12. C. H. Wu, C. Jacob, X. J. Ning, S. Nishino, and P. Pirouz, J. Cryst. Growth 158 (1996) 480.

13. N. Braslau, J. B.Gunn, and J. L.Staples, Solid State Electron. 10 (1967) 38.

14. R. Stall, C. E. C. Wood, K. Board, and L. F. Eastman, Electron. Lett. 15 (1979) 800.

15. E. D. Marshall, B. Zhang, L. C. Wang, P. F. Jiao, W. X. Chen, T. Sawada, S. S. Lau, K. L. Kavanagh, and T. F. Kuech, J. Appl. Phys. 67 (1990) 3136.

16. R. Dutta, A. Lahav, M. Robbins, and V. G. Lambrecht, J. Appl. Phys. 67 (1990) 3136.

17. T. Nitton, H. Ito, O. Nakajima, and T. Ishibashi, Japan Appl. Phys. Lett. 25 (1986) L865.

18. J. M. Woodall, J. L. Freeout, G. D. Pettit, T. N. Jacson, and P. Kirchner, J. Vac. Sci. Tech. 19 (1981) 636.

19. E. D. Marshall, W. X. Chen, C. S. Wu, S. S. Lau, and T. F. Kuech, Appl. Phys. Lett. 47 (1985) 298.

20. E. D. Marshall, S. S. Lau, C. J. Palmstrom, T. Sands, C. L. Schwartz, S. A. Schwartz, J. P. Harbison, and L. T. Florez, Mater. Res. Soc, Symp. Proc. 148 (1989) 163.

21. C. J. Palmstrom, S. A. Schwartz, E. Yablonovitch, J. P. Harbison, C. L. Schwartz, L. T. Florez, T. J. Gmitter, E. D. Marshall, and S. S. Lau, J. Appl. Phys. 67 (1990) 334.

22. L. C. Wang, X. Z. Wang, S. S. Lau, T. Sands, W. K. Chan, and T. F. Kuech, Appl. Phys. Lett. 56 (1990). 2129.

23. C. C. Han, X. Z. Wang, I. C. Wang, E. D. Marshall, S. S. Lau, S. A. Schwartz, C. J. Palmstrom, J. P. Harbison, L. T. Florez, R. M. Potemski, M. Tischler, and T. F. Kuech, J. Appl. Phys. 68 (1990) 5714.

24. J. S. Kwak, H. N. Kim, H. K. Baik, J. L. Lee, D. W. Shin, C. G. Park, H. Kim, and K. E. Pyun, J. Appl. Phys. 80(7) (1996) 3904.

25. L. C. Wang, X. Z. Wang, N. S. Hsu, S. S. Lau, S. D. Lin, T. Sands, S. A. Schwartz, D. L. Plumton, and T. F. Kuech, J. Appl. Phys. 69(8) (1991) 4364.

26. K. Fricke, H. L. Hartnagel, G. Schutz, G. Schweeger, and J. Wurfl, Second HiTEC, Charlotte, NC, 1994, p. P-197.

27. M. Murakai, W. H. Price, J. H. Greiner, J. D. Feder, and C. C. Park, J. Appl. Phys. 65(9) (1989) 3546.

28. M. Murakami, H. J. Kim. AY. C. Shih, AW. H. Price, and C. C. Park, Appl. Surf. Sci. 41/42 (1989) 195.

29. M. Murakami, Material Science Report 5 (1990) 273.

30. M. C. Hugon, B. Agius, F. Varnicere, C. Dubon-Chevallier, J. F. Bresse, and M. Froment, Appl. Phys. Lett. 58(24) (1991) 2773.

31. M. C. Hugon, B. Agius, F. Varnicere, and M. Froment, J. Appl. Phys. 72(8) (1992) 3570.

32. M. Murakami, W. H. Price, M. Norcott, and P. E. Hallali, J. Appl. Phys. 68(5) (1990) 2648.

33. K. Ohta and M. Ogawa, Ext. Abs., Japan Soc. Appl. Phys. 35(2) (1974) 263.

34. W. T. Anderson, Jr, A. Christo, and J. E.Davey, IEEE J. Solid State Circuit. SC-13 (1978) 430.

35. K. Tanahashi, H. J. Takata, A. Otsuki, and M. Murakami, J. Appl. Phys. 72 (1992) 4183.

36. E. Kolawa, W. Flick, C. W. Nieh, J. M. Molarius, M. A. Nicolet, L. J. Tandon, J. H. Madok, and F. C. T. So, IEEE Trans. Electron. Device 36 (1989) 1223.

37. M. O. Aboelfotoh, C. L. Lin, and J. M. Woodall, Appl. Phys. Lett. 65 (1994) 3245.

38. S. Oktyabrsky, M. O. Aboelfotoh, and J. M. Woodall, J. Electron. Mater. 25(11) (1996) 1662.

39. S. Oktyabrsky, M. O. Aboelfotoh, and J. Narayan, J. Electron. Mater. 25(11) (1996) 1673.

40. T. S. Kuan, P. E. Batson, T. N. Jackson, H. Rupprecht, and E. L. Wilkie, J. Appl. Phys. 54(12) (1883) 6952.

41. A. Iliadis and K. E. Singer, Solid State Commun. 49(1) (1984) 99.

42. Y. C. Shih, M. Murakami, E. L. Wilkie, and A. C. Callegari, J. Appl. Phys. 62(2) (1987) 582.

43. E. Zanoni, A. Callegari, F. Fantini, H. L. Hartnagel, F. Magistrali, A. Paccagnella, and M. Vanzi, Quality and Liability Engineering International, vol.6 (1990) 29.

44. E. Haug, N. Hedgecock, and W. Buckel, Z. Phys. B22 (1975) 237.

45. S. M. Sze etc., Physics of Semiconductor Devices, 2nd ed., Wiley, New York, 1981.

46. C. D. Wilson, A. G. O'Neill, S. M. Baier, and J. C. Nohava, IEEE Trans. Electron. Device (1996) 201.

47. E. H. Rhoderick and R. H. Williams, Metal-Semiconductor Contacts, 2nd ed., OUP, New York, 1988.

48. W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, Phys. Rev. Lett. (1981) 2342.

49. C. R. Crowell, J. C. Sarace, and S. M. Sze, Trans. Met. Soc. AIME, (1965) 233.

50. J. O. McCaldin, T. C. McGill, and C. A. Mead, J. Vac, Sci. Tech. 13 (1976) 802.

51. A. M. Goodman, J. Appl. Phys. 34 (1963) 329.

52. J. Wurfl, B. Janke, K. H. Rooch, and S. Thierbach, 22nd ISCS, Cheju Island, Korea, 1995, p. 54.

53. U. Merkel, E. Nebauer, and M. Mai, Thin Solid Films (1992) 217.

54. J. Wurfl, J. K. Singh, and H. L. Hartnagel, IEEE Reliab. Phys. 28th Annual Proc. 1990, p. 87.

55. K. Fricke et al., IEEE Electron. Device Lett. EDL-10 (1989) 577.

56. T. Sand, Mater. Sci. Eng. B1 (1989) 289.

57. A. G. Lahav, C. S. Wu, and F. A. Baiocchi, J. Vac. Sci. Tech. B6 (1988) 1785.

58. D. V. Morgan and J. Wood, Appl. Surf. Sci. 38 (1989) 517.

59. T. E. Haynes, W. K.Chu, C. C. Han, S. S. Lau, and S. T. Picraus, Appl. Phys. Lett. 53 (1988) 2200.

60. K. M. Yu, J. M. Jaklevic, E. E. Haller, S. K. Cheung, and S. P. Kwok, J. Appl. Phys. 64 (1988) 1284.

61. W. P. Kang and Y. Gurbuz, J. Appl. Phys. 75 (12) (1994) 8175.

62. C. P. Chen, Y. A. Chang, J. W. Huang, and T. F. Kuech, Appl. Phys. Lett. 64(11) (1994) 1413.

63. H. Nakamura, Y. Sano, T. Nonaka, T. Ishida, and K. Kaminishi, IEEE GaAs IC Symp. Tech. Digest, (1983) 134.

64. S. P. Kwok, J. Vac. Sci. Tech. B4 (1986) 1383.

65. Y. Sekino, T. Kimura, K. Inokuchi, Y. Sano, and M. Sakuta, Jpn. J. Appl. Phys. 27 (1988) L2183.

66. C. P. Chen, Y. A. Chang, and T. F. Kuech, J. Appl. Phys. 77(9) (1995) 4777.

67. C. P. Chen, Y. A. Chang, and T. F. Kuech, J. Appl. Phys. 77(9) (1995) 1915.

68. S. A. Chambers, J. Vac. Sci. Tech. B7 (1989) 737.

69. C. P. Chen, Y. A. Chang, and T. F. Keuch, Appl. Phys. Lett. 64 (1994) 3485.

70. T. Sand, W. K. Chan, C. C. Chang, E. W. Chase, and V. K. Keramidas, Appl. Phys. Lett. 52 (1988)1388.

71. T. Lalinsky, D. Gregusova, Z. Mozolava, J. Breza, and P. Vogricic, Appl. Phys. Lett. 64(14) (1994) 1818.

72. T. S. Huang, J. G. Peng, and C. C. Lin, Appl. Phys. Lett. 61 (1992) 3017.

73. T. S. Huang, J. G. Peng, and C. C. Lin, J. Vac. Sci. Tech. B11 (1993) 756.

74. T. S. Huang and J. G. Pang, J. Appl. Phys., 78(9) (1995) 5739.

75. T. S. Huang and S. M. Jean, J. Appl. Phys. 75(11) (1994) 7519.

76. J. M. Woodall, P. D. Kirchner, J. L. Freeouf, D.T. McInturff, M. R. Melloch, and F. H. Pollak, Philos. Trans. R. Soc. A 344 (1673) (1993) 521.

77. K. Okamoto, C. E. C. Wood, and L. F. Eastman, Appl. Phys. Lett. 38 (8) (1981) 1116.

78. K. Steiner, H. Mikami, K. Nishihori, M. Nagaoka, and N, Uchitomi, J. Vac. & Tech. B9 (3) (1991) 1601.

79. C. Ghezzi, E. Gombia, and R. Mosca, J. Appl. Phys. 70 (1) (1991) 215.

80. J. H. Baek, M. Shur, R. R. Daniels, D. K. Arch, J. K. Abrokwah, and O. N. Tufte, IEEE Electron. Device Lett. EDL-7(9) (1986) 519.

81. T. J. Miller and M. I. Nathan, Appl. Phys. Lett. 61(19) (1992) 2332.

82. M. Eizenberg, M. Heiblum, M. I. Nathan, N. Braslau, and P. M. Mooney, J. Appl. Phys. 61(41) (1987) 1516.

83. C. Meva'a, X. Letartre, P. Rojo-Romeo, and P. Viktorovitch, Solid State Electron. 41(6) (1997) 857.

84. S. Tiwari and D. J. Frank, Appl. Phys. Lett. 60(5) (1992) 630.

85. M. S. Daw and D. L. Smith, Appl. Phys. Lett. 36(8) (1980) 690.

86. R. E. Allen and J. D. Dow, Phys. Rev. B 25(2) (1982) 1423.

87. J. Tersoff, Phys. Rev. B 32(10) (1985) 6968.

88. M. Missous, W. S. Truscott, and K. E. Singer, J. Appl. Phys. 68(5) (1990) 2239.

89. R. Narasimhan, L. P. Sadwick, and Ruey J. Hwu, IEEE Trans. Electron. Device 46 (1999) 24.

90. L. P. Sadwick, P. P. Lee, M. Patel, M. Nikols, R. J. Hwu, J. E. Shield, D. C. Streit, D. Brehmer, K. McCormick, S.J. Allen, and R.W. Gedridge, J. Cryst. Growth (1996) 4843.

91. F. W. Smith, A. R. Calawa, L. -L. Chen, M. J. Manfra, and L. J. Mahoney, IEEE Electron. Device Lett. 9 (1988) 77.

92. K. Xie, Z. C. Huang, and C. R. Wie, J. Electron. Mater. 20(7) (1991) 553.

93. G. N. Maracas, K. Shiralagi, R. Ramamurti, and R. W. Carpenter, J. Electron. Mater. 22(12) (1993) 1375.

94. Kai Zhang and D. L. Miller, J. Electron. Mater. 22(12) (1993) 1433.

95. C. E. Stutz, D. C. Look, E. N.Taylor, J. R. Sizelove, and P. W. Yu, J. Electron. Mater. 24(1) (1995) 31.

96. B. Tadayon, M. E. Twigg, M. Fatemi, M. Y. Frenkel, A. Giordana, and D. S. Katzer, J. Electron. Mater. 2 (11) (1995) 1753.

97. P. Arifin, E. M. Glodys, and T. L. Transley, Mater. Sci. and Eng. B35 (1995) 330.

98. S. Shiobara, K. Sasaki, and H. Hasegawa, Solid State Electron. 38(9) (1995) 1685.

99. M. Lagadas, Z. Hatzopoulos, N. Kornilios, M. Androulidaki, A. Christou, and P. Panayotatos, Mater. Sci. and Eng. B44 (1997) 355.

100. M. Missous and S. O'Hagan, J. Cryst. Growth 175/176 (1997) 197.

101. A. K. Verma, J. S. Smith, H. Fujioka, and E. R. Weber, J. Appl. Phys. 77(9) (1995) 4452.

102. R. A. Kiehl, M. Yamakuchi, T. Ohshima, M. Saito, and N. Yokoyama, Appl. Phys. Lett. 69 (10) (1996) 1441.

103. A. K. Verma, J. Tu, and J. S. Smith, Appl. Phys. Lett. 68 (5) (1996) 699.

104. P. Kordos, M. Marso, A. Forster, J. Darma, J. Betko, and G. Nimtz, Appl. Phys. Lett. 71 (8) (1997) 1118.

105. R. V. V. V.J. Rao, T. C. Chong, W. S. Lau, L. S. Tan, C. Geng, and N. Lim, Electron. Lett. 34 (1998) 2066.

106. J. A. Carlin, S. A. Ringel, R. N. Sacks, and K. S. Yap, J. Vac. Sci. Technol. B 16(3) (1998) 1372.

107. H. Reese, Y. J. Chiu, and E. Hu, Appl. Phys. Lett. 73 (1998) 2624.

108. L. He, Solid State Electron. 41(12) (1997) 1881.

109. R. Zhao, W. S. Lau, T. C. Chong and M. F. Li, Japan. J. Appl. Phys. 35 (1996) 22.

110. R. H. Blick, M. L. Roukes, W. Wegscheider, and M. Bichler, Phys. B 249-251 (1998) 784.

111. J. Novak, M. Morvic, J. Betko, A. Forster, and P. Kordos, Mater. Sci. & Eng. B40 (1996) 58.

112. F. W. Smith, Ph.D Thesis, MIT, 1990.

113. D. C. Look, D. C. Walters, M. O. Manazreh, J. R. Sizelove, C. E. Stutz, and K. R. Evans, Phys. Rev. B42 (1990) 3578.

114. A. C. Warren, J. M. Woodall, J. L. Freeouf, D. Grischowsky, D. T. McInturff, M. R. Meloch, and N. Otsuka, Appl. Phys. Lett. 57 (1990). 1331.

115. A. C. Campbell, G. E. Crook, T. J. Rogers, and B. G. Streetman, J. Vac. Sci. Tech. B8 (1990) 305.

116. C. Ghezzi, E. Gombia, and R. Mosca, J. Appl. Phys. 70(1) (1991) 215.

117. L. G. Meiners, Thin Solid Films 56 (1979) 201.

118. L. P. Sadwick, Appl. Phys. Lett. 64(1) (1994) 79.

119. R. Lee, G. Trombley, B. Johnson, R. Reston, C. Havasy, and M. Mah, Second Hi-TEC, Charlotte, NC, 1994, p. V-3.

120. S. Baier, J. Nohava, R. Jeter, R. Carlson, and S. Hanka, Second Hi-TEC, Charlotte, NC, 1994, p. V-21.

121. N. A. Papanicolaou, W. T. Anderson, D. S. Katzer, S. H. Jones, and J. R. Jones, Second Hi-TEC, Charlotte, NC, 1994, p. V-9.

122. J. Wurfl, B. Janke, K. H. Rooch, and S. Thierbach, Second Hi-TEC, Charlotte, NC, 1994, p. V-33.

123. J. C. Zopler, V. M. Heitala, A. Ga. Baca, M. S. Housel, and M. E. Sherwin, Third Hi-TEC, Albuquerque, NM, 1996, p. IV-9.

124. Y. Gobert and G. Salmer, IEEE Trans. Electron. Device 39 (1992) 1571.

125. H. Wong, C. Liang, and N. W. Cheung, IEEE Trans. Electron. Device 41 (1994) 299.

126. C. Ito, T. Jenkins, G. Trombley, R. Lee, R. Reston, C. Havasy, B. Johnson, and C. Eppers, IEEE Electron. Device Lett. 17 (1996) 16.

127. R. Lee, G. Trombley, B. Johnson, R. Reston, M. Mah, C. Havasy, and C. Ito, IEEE Electron. Device Lett. 16 (1995) 265.

128. K. Fricke, V. Krozer, and M. Schubler, Third Hi-TEC, Albuquerque, NM, 1996, p. IV-15.

129. J. Wurfl and B. Janke, Mater. Sci. & Eng. 46 (1997) 52.

130. F. P. McCluskey, R. Grzybowski, and T. Podlesak, HiTEC CRC Press, Boca Raton, FL, 1997.

131. C. D. Wilson, A. G. O'Neil, S. M. Bair, and J. C. Nohava, IEEE Trans. Electron. Devices (1996) 201.

132. T. Cunnigham. E. Fossum, and S. Baier, IEEE Electron. Device Lett. 35 (1992) 570.

133. T. E. Zipperian, R.J. Chaffin, and L. R. Dawson, IEEE Trans. Ind. Electron. (1982) 129.

134. C. D. Wilson and A. G. O'Neill, Trans. 2nd HiTEC, Charlotte, NC, 1994, p. V-15.

135. C. D. Wilson and A. G. O'Neill, First European Conference Proc. on HiTEC, 1993, III.4.

# CHAPTER 2

# EXPERIMENTAL

In Chapter 2 of this dissertation, the various techniques, instrumentation and equipment utilized in this dissertation are introduced and, in some cases, a brief discussion of the theory of operation and some practical considerations for these techniques, instrumentation and equipment are presented below with references provided for further, more in-depth reading for the interested reader.

## 2.1 X-ray diffraction analysis

Several X-ray techniques are used to characterize semiconductors and thin-films, including X-ray diffraction [5], rocking-curve [6], and grazing incidence scattering (GIS) [7, 8].

A Philips X-ray diffratometer (PW 1710, Philips) with Cu $K_\alpha$ radiation at 1.5406 Å operated at 40 KV and 20 mA was used for the standard $\theta$-$2\theta$ scan. A typical scan rate was ~0.05°/sec. A second Philips X-ray diffratometer was used for the GIS and rocking curve analysis at an operation voltage and current of 40 KV and 30 mA, respectively. A typical glancing angle was 2~3° with a span of 1°. The rocking curves were obtained exclusively by rotating the crystal about an angle corresponding to the GaAs (004) reflection. A Bede SCIENTIFIC™ Model

D1 double X-ray diffratometer was used for the rocking curve analysis on multi-layer structures at an operation voltage and current of 40 KV and 30 mA, respectively. The associated software for the diffratometer can be used to simulate the thickness, composition, and interface roughness for all ternary compound semiconductors according to the measured rocking curves.

## 2.2 X-ray photoelectron spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) is a widely used method of determining the chemical composition of a surface [16]. In the XPS technique, X-rays impinge upon a sample and ionize atoms, releasing core-level photoelectrons. The photoelectrons are collected and analyzed by the XPS instrument to produce a spectrum of emission intensity versus electron binding energy. The X-ray photoelectron spectroscopy system used for surface analysis for this dissertation was a Fisons (now VG Scientific) 220I-XL imaging multi-technique surface analysis system, including a monochromatic high-flux micro-focused Al X-ray source for high-resolution, high-sensitivity work; a magnetic immersion lens for high collection efficiency and stable charge compensation; and a unique detector system for spectral and imaging data acquisition. The XPS is equipped with an argon (Ar) sputtering gun that was used to remove the top few atomic layers of the thin films since the thin films are usually contaminated by either oxidation or human handling (i.e., organics, oil, etc.). A sputtering rate of 50 Å/min was used to obtain depth analysis of the thin films investigated in this dissertation.

## 2.3 Thermal analysis – differential scanning calorimetry (DSC)

The technique of differential scanning calorimetry (DSC) involves recording the energy necessary to establish a zero temperature difference between a substance and a reference material against either time or temperature as the two specimens are subjected to an identical temperature program regime. The ordinate value at any time or temperature is related to the difference in heat flow between a standard sample and an unknown sample under test. The difference in heat is related to the kinetics of the process. Integration of the area under the heat flow curve yields the enthalpy change associated with the thermal event of interest [9, 10].

## 2.4 Photoluminescence (PL) measurements

A customized photoluminescence (PL) system [1] consisting of an Ar-laser as the excitation light source, an optical lens systems, and photodetectors, which have the ability to monitor emitted wavelengths from 400 nm to 1.5 $\mu$m, was used for investigating impurities and crystal quality of semiconductors such as gallium arsenide (GaAs), aluminum gallium arsenide (AlGaAs), low temperature (LT)-AlGaAs, and indium gallium arsenide (InGaAs) for the work performed in this dissertation. Room temperature and low temperature (~10K) measurements were performed on a stage that was chilled by a cryo-pump under a vacuum of $2x10^{-6}$ Torr. The photoluminescence response of the samples due to excitation by the 488 nm line of the $Ar^{+}$ laser was measured. The laser beam was chopped and focused onto the sample with a spot size of approximately 0.25 $mm^2$. The PL emission was fed into a Spex Model 1870 monochromator and detected by a

Hamamatzu R1104 head-on photomultiplier tube using standard lock-in amplification techniques. The excitation intensity used for the samples reported in this dissertation was 10 mW. Details of the experimental setup can be found in Ref.1.

## 2.5 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) images show critical information about surface features with unprecedented clarity [13]. The AFM can examine any rigid surface, either in air or with the specimen immersed in a liquid. "Minor" (and major) differences between "smooth" surfaces show up dramatically. The AFM can resolve very tiny features down to atomic dimensions that were previously hard to observe or not observed at all.

A tiny stylus gently contacts the specimen. As the XYZ translator scans either the specimen or the stylus horizontally in a raster pattern (XY), the stylus rides up and down the surface's hills and valleys. The deflection of the stylus is registered by the laser/photodiode sensor and the XYZ translator adjusts stylus or specimen (depending on the microscope) up or down (Z) to restore the stylus to its original position. The computer stores the vertical position at each point and assembles the image.

All images were taken under the "Tapping" mode [14, 15] using a Digital Instruments atomic force microscope. Scan rates of one to two lines per second were used and data were taken at 512 points/line and 512 lines per scan area.

## 2.6 Current-voltage measurements

All the current-voltage (I-V) measurements [11, 12] were conducted using a test system comprised of a HP 4145B parameter analyzer, a Micromanipulator HSM hot stage and chuck controller, and an IBM personal computer (PC) compatible computer. The data were acquired via an IEEE 488 HPIB data bus and stored electronically for further analysis. Low temperature measurements were performed by first chilling the chuck using liquid nitrogen until the temperature was stabilized at 77K. The vacuum chuck was slowly heated up and data were taken accordingly. It typically took around 1 hour for the temperature of the vacuum chuck to go from 77K to room temperature.

## 2.7 Capacitance-voltage measurements

The capacitance-voltage (C-V) characteristics [11, 12] were obtained with an EG&G PAR 410/4108 capacitance bridge also controlled by a PC. If the slope of the $C^{-2}$ vs. V plot obtained is linear, one can obtain an independent measurement of barrier height using the method of least squares fit, from the intercept of the voltage axis $V_{int}$ through the use of the following relationship [2]

$$\phi_b = V_{\text{int}} + \phi_o + kT/q \qquad (6)$$

where $\phi_o = (kT/q)ln(N_c/n)$ can be determined from the donor density which, in turn, can be calculated from the slope of the $C^{-2}$ vs. V plot. The density of states in the conduction band of $Al_xGa_{1-x}As$ can be found in Ref.3.

## 2.8 Hall measurements

The free electron (or hole) concentrations and mobilities were measured at room temperature using the Hall effect measurement technique with Van der Pauw geometry [4]. Ohmic contacts were formed using pure indium (99.999%) or In/Sn [for n-type samples] or In/Zn (3% Zn) [for p-type samples] dots alloyed in a Lindberg furnace for 10 min at 300°C in $N_2$. The principle of and a details of the Hall effect technique and measurement can be found in Ref.4.

## 2.9 Wet etching of GaAs and $Al_xGa_{1-x}As$ compounds

$H_3PO_4$ : $H_2O_2$ :Methanol in a 3:1:1 ratio was used as a mesa isolation etch throughout the entire processing. This etching solution is isotropic and not a selective etchant for GaAs and $Al_xGa_{1-x}As$ compounds. The etching rate is a function of temperature; for example, the etching rate is 3500 Å /min at 5°C and ~1.1μm/min at 17°C.

## 2.10 Annealing

Forming gas (in a ratio of $H_2$:$N_2$ = 3:7) was used for the thermal annealing process. After annealing, the samples were quenched by “dropping” them onto aluminum foil after the samples had been capped with a nitride protective layer. For samples without capping, cooling at the edge of the tube furnace for 2 min was found to be sufficient and did not cause any additional oxidation of the contacts.

## 2.11 References


1. I. H. Ho, Localized Structure in III-V Alloys, Ph.D. Dissertation, University of Utah, Chapter 5, 1997.

2. E. H. Rhoderick and R. H. Williams, Metal Semiconductor Contacts, 2nd ed., OUP, New York, 1988.

3. M. Missous, W. S. Truscott, and K. E. Singer, J. Appl. Phys. 68(5) (1990) 2239.

4. L. J. van der Pauw, Philips Research Report 13, Chapter 4, 1958, p. 1.

5. B. D. Cullity, Elements of X-ray Diffraction, 2nd edition, Addison Wesley, London, 1978.

6. J. Chaudhuri and F. Hashmi, Advances in X-ray Analysis, Vol. 39, Plenum Pub., Corp., New York, 1997, p. 637.

7. W. H. Zachariasen, Theory of X-ray Diffraction in Crystals, John Wiley and Sons, London, 1945.

8. B. E. Warren, X-ray Diffraction, Dover Publications, Inc., New York, 1990.

9. B. Wunderlich, Thermal Analysis, Academic Press, New York, 1990.

10. J. A. Dean, The Analytical Chemistry Handbook, McGraw Hill, New York, 1995.

11. S. M. Sze, Physics of Semiconductor Devices, 2nd ed., Wiley, New York, 1981.

12. E. H. Nicollian and J. R. Brew, MOS (Metal Oxide Semiconductor) Physics and Technologies, Wiley, New York, 1982.

13. J. C. Vickerman, Surface Analysis - The Principal Techniques, John Wiley and Sons, New York, 1997.

14. R. V. Lapshin, Rev. Sci. Inst. 69(9) (1998) pp. 3268–3276.

15. Q. Zhong, D. Inniss, K. Kjoller, and V. Elings, Surf. Sci. Lett. 290 (1993) L688.

16. D. W. Turner and M. I. Al Jobory, J. Chem. Phys. 37 (1962) 3007.

# CHAPTER 3

# THERMALLY STABLE CuGe-BASED OHMIC CONTACTS TO N-TYPE GaAs AND TiWN DIFFUSION BARRIERS

## 3.1 Specific contact resistance (SCR) of CuGe-based ohmic contacts to n-GaAs

### 3.1.1 Effect of annealing conditions on specific contact resistance

Specific Contact Resistance (SCR) is the reciprocal derivative of current density respect to voltage. When evaluated at zero bias, this specific contact resistance is an important figure of merit for ohmic contacts [48]. To characterize specific contact resistance, the transmission line method (TLM) is typically used [51]. The TLM measurement technique uses a series of contacts each with different spacings. Typical contact lengths and widths (W) are 200$\mu$m. As can be seen in Fig.1, the I-V characteristics measured at room temperature between adjacent contacts deposited on n-type GaAs (n = $4.05 \times 10^{17} cm^{-3}$) spaced 20 $\mu$m apart produce linear results after 20 min annealing at temperatures from 400°C to 480°C in forming gas.

The resistivity of $Cu_3Ge$ ohmic contacts decreased as the annealing temperature increased for a fixed annealing time of 20 min. The lowest contact resistance was obtained from samples annealed at 400°C. The planar interface

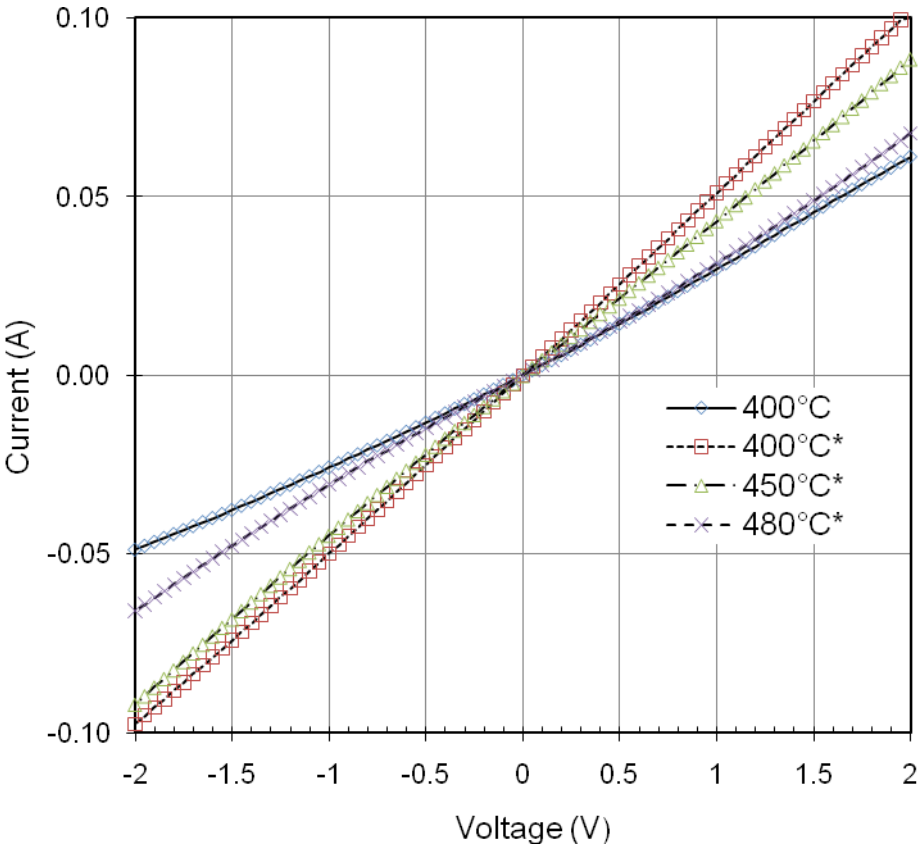



Fig.1. Current-voltage characteristics at room temperature for $Cu_3Ge$ ohmic contacts to n-type GaAs having a doping density of $4x10^{17}cm^{-3}$. Annealing conditions were 20 min in forming gas at the different temperatures listed in this figure.

between the contacts and substrate, along with the higher diffusion coefficient of Ge at 400°C, are thought to be responsible for the lower contact resistance among all of the annealing temperatures tested; this is discussed in Section 3.2.4 of this dissertation. In Fig. 2, a dramatic change in conductivity of the $Cu_3Ge$ contacts after annealing at 400°C for 20 min was observed; this result is indicative of the results obtained, in general, if the contacts were not immediately annealed after deposition. This change is an indication of how strongly this contact material tends to oxidize. Oxidation of the contacts is problematic in terms of the practical usefulness of these contacts.

Annealing in a nitrogen ambient and in vacuum were found to have similar results compared to annealing in forming gas in terms of specific contact resistance, for CuGe-based ohmic contacts to n-type GaAs.

The I -V characteristics of Cu/Ge based ohmic contacts to n-type GaAs (n = $4.05 \times 10^{17}$ $cm^{-3}$) varied with annealing time as shown in Fig. 2. At 400°C, if the annealing time was less than 10 min, the Cu/Ge contacts to n-type GaAs appeared to have rectifying I-V characteristics. The insert in Fig. 2 shows the normalized specific contact resistance, with respect to that of contacts annealed for 30 min, as a function of annealing time at 400°C for $Cu_3Ge$ ohmic contacts to n-type GaAs. The valley at which the lowest resistance was achieved corresponded to an annealing time of 30 min. Increases in annealing time for longer than 30 min were found to have little effect on specific contact resistance for $Cu_3Ge$ contacts to n-type GaAs.

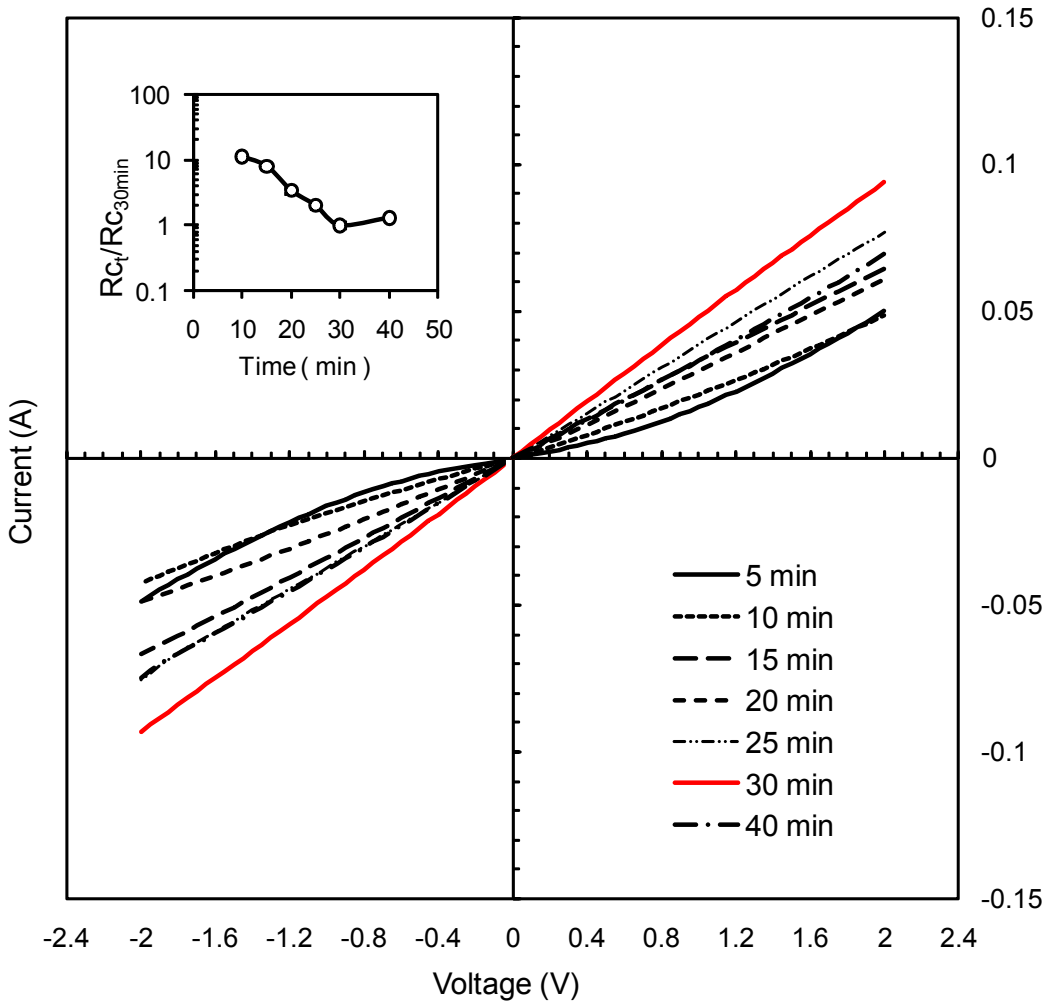



Fig. 2. Room temperature current-voltage characteristics of $Cu_3Ge$ ohmic contacts to n-type GaAs (n = $4.05 \times 10^{17}$ $cm^{-3}$ ) after annealing at 400°C for times ranging from 5 min to 40 min. The specific contact resistance versus annealing time is also shown in the insert.

Figs. 3(a) to (d) are AFM images of the surface morphology of CuGe-based contacts to GaAs for (a) as-deposited;(b) annealed at 400°C for 30 min; (c) annealed at 450°C for 30 min; and (d) annealed at 480°C for 30 min. The root mean square roughness of samples (a) to (d) is 10Å, 50Å, 55Å, and 54Å, respectively. Such smooth surfaces are much better than that of AuGeNi and InGeW contacts [1-13], which normally have root mean square (RMS) values ranging from 100 to 500 Å, typical values for ohmic contacts to n-GaAs. The perturbation at the contact-substrate interface is considerably smaller and is responsible for the smooth surface of this contact system on GaAs.

### 3.1.2 Effect of Ge compositions on specific cntact resistance (SCR)

Fig. 4 shows the specific contact resistance of Cu/Ge contacts to n-type GaAs as a function of Ge composition as determined by the transmission line meaurement (TLM) technique. Two n-type GaAs doping levels, $1.0x10^{17}$ $cm^{-3}$ and $4.05x10^{17}$ $cm^{-3}$, were used to verify the effect. The values of specific contact resistance (SCR) of the CuGe-based contacts to n-type GaAs depend on the doping densities of the semiconductor, as well as the Ge composition in the binary alloys.

For n-type GaAs with a doping concentration of $1.0x10^{17}$ $cm^{-3}$, as shown in the upper curve in Fig. 4, as the Ge composition increased from 15 % to 25 %, the specific contact resistance was found to decrease from $1.5x10^{-5}$ $\Omega cm^2$ to $9.3x10^{-6}$ $\Omega cm^2$, respectively.

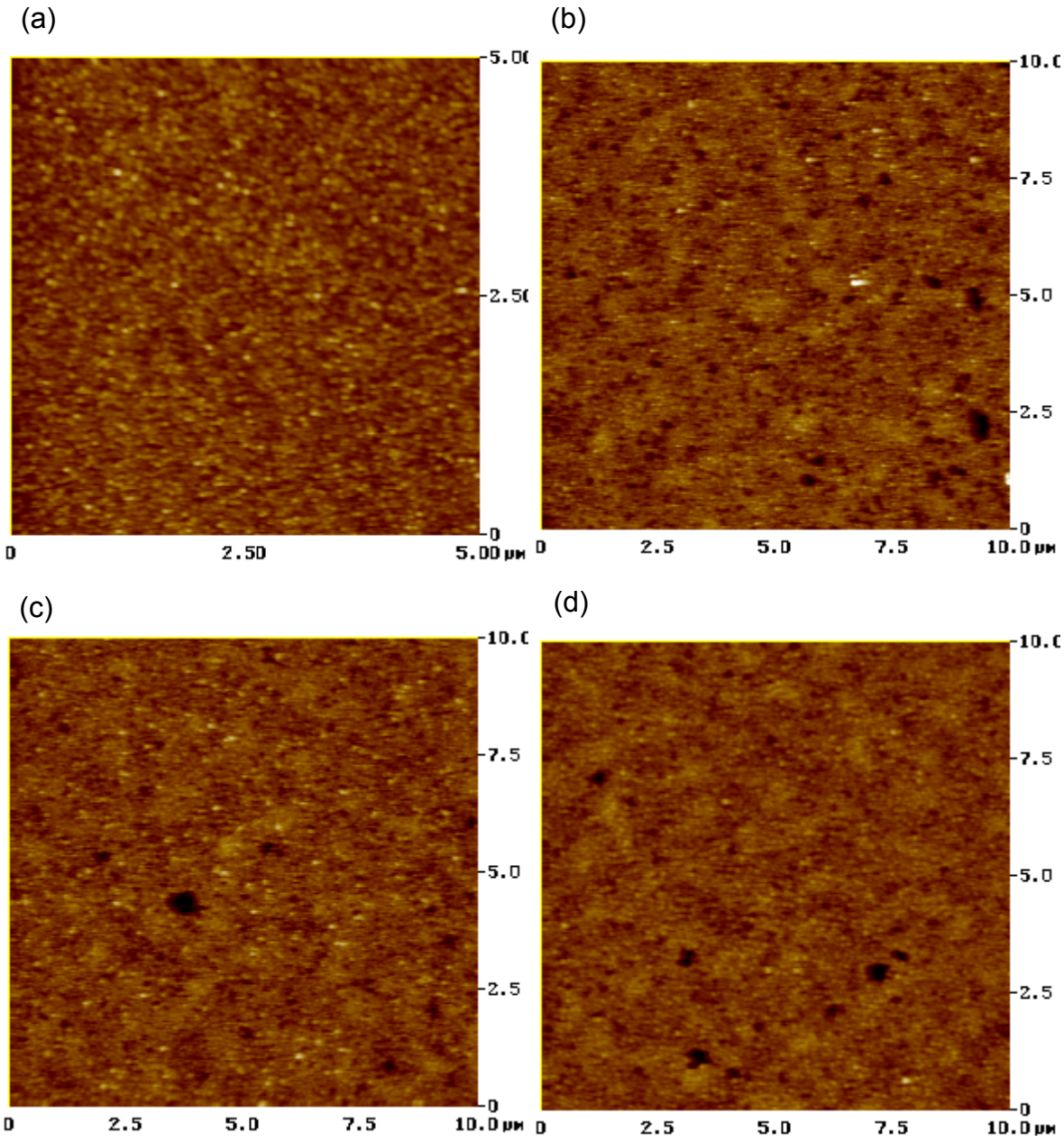



Fig. 3. AFM micrographs for (a) as-deposited Ge/Cu/n-GaAs, and after annealing for 30 min at (b) 400°C, (c) 450°C, and (d) 480°C in forming gas ambient.

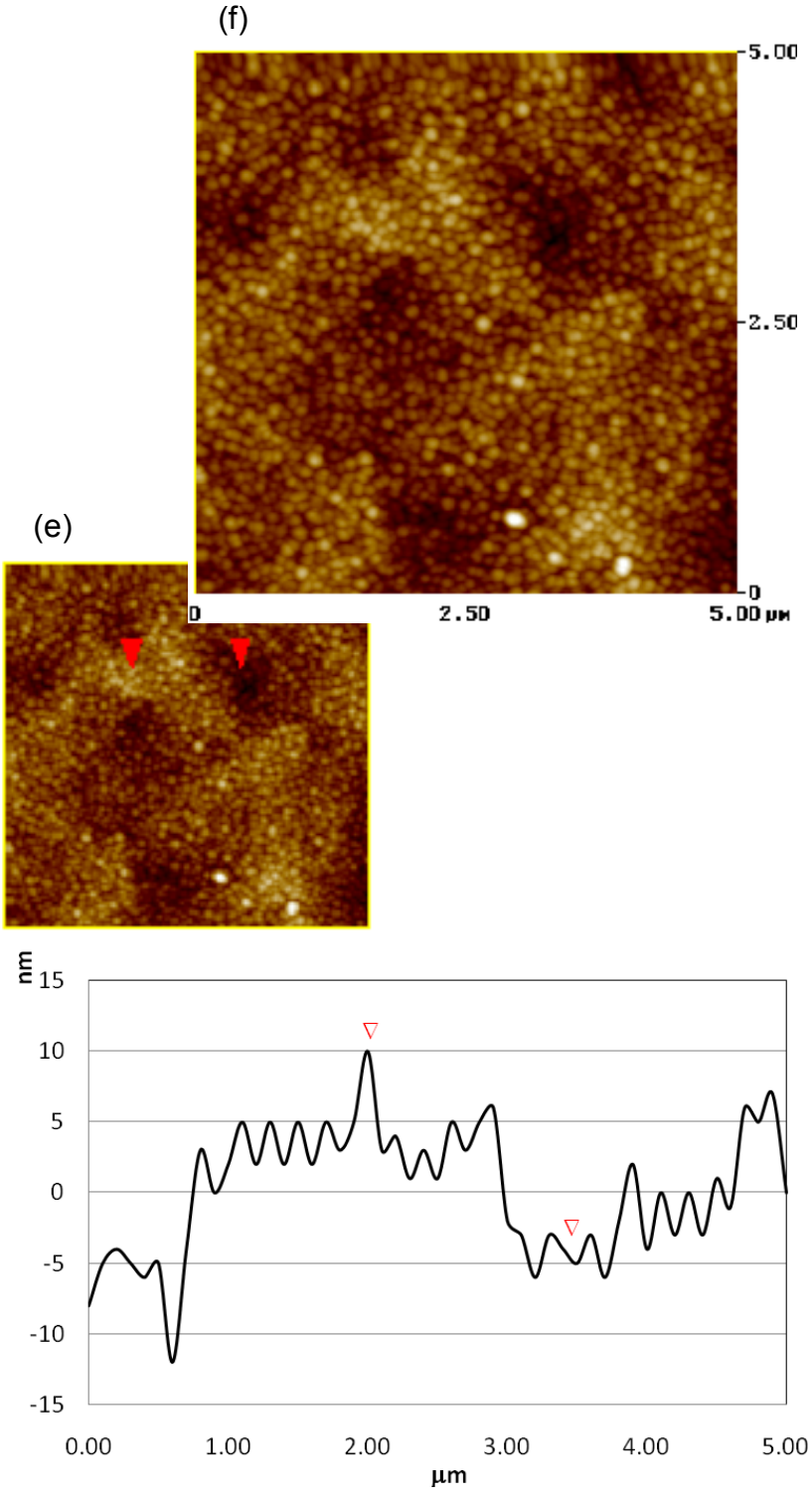



Fig.3. continued (e) Cross-section analysis and (f) roughness analysis for Cu/Ge contacts to n-type GaAs (n = $4.05 \times 10^{17}$ $cm^{-3}$ ) after annealing at 400°C for 25 minutes.

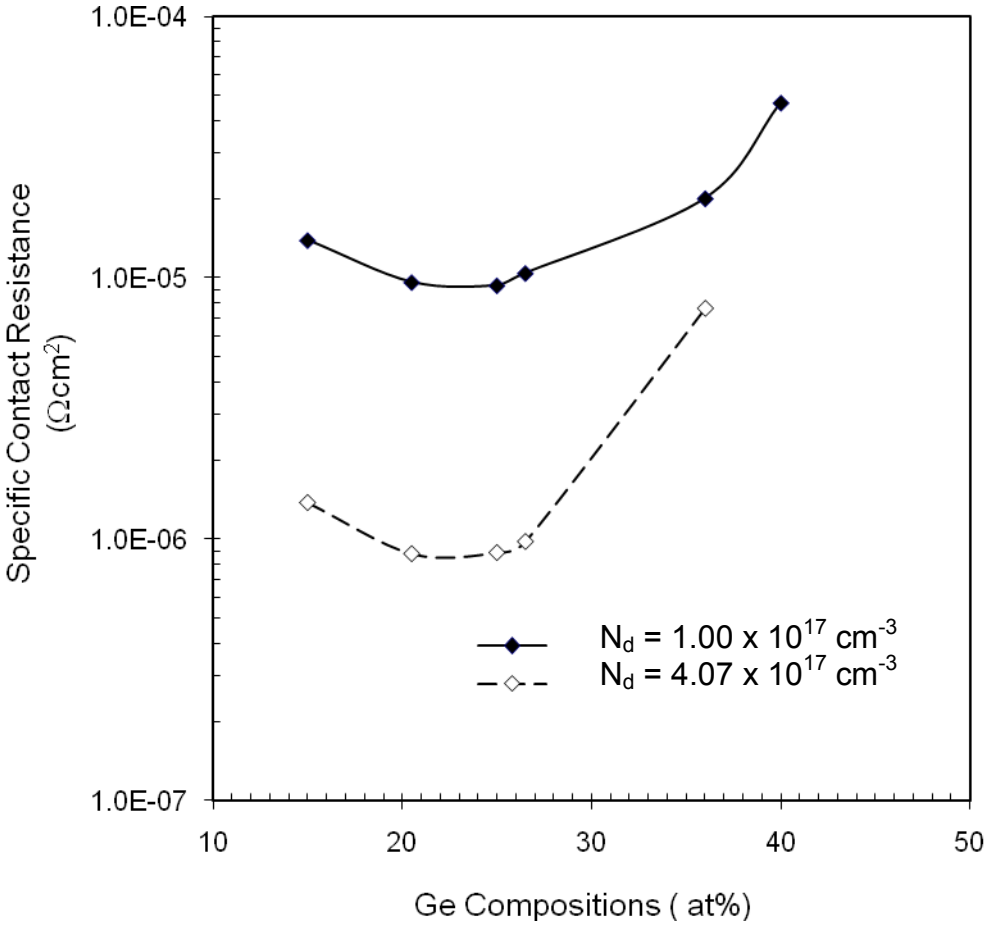



Fig. 4. Specific contact resistance (SCR) as a function of Ge composition for the CuGe-based ohmic contacts as determined by transmission line method (TLM) measurements.

The SCR was found to increase from $9.3x10^{-6}$ $\Omega cm^2$ to $4.5x10^{-5}$ $\Omega cm^2$ as the Ge composition increased from 25 at % to 40 at %, respectively. Thermodynamics data indicated that low Ge composition favored the formation of $Cu_3As$ and hexagonal $Cu_5Ge$ phases which have higher resistance than that of $Cu_3Ge$ [14,15]. Ge deficient layers (average composition $Cu_5Ge$) reveal the formation of a nonuniform intermediate layer of hexagonal $Cu_3As$ phase which grows epitaxially on Ga {111} planes of GaAs [17]. In this case, the Ga that is released diffuses out and dissolves in the alloyed layer thus stabilizing the phase, which is formed in the structures with an average Ge concentration as low as 5 at % [17].

Along with the effect of free copper [52], which acts as a double acceptor for GaAs, higher specific contact resistance for Ge compositions higher than 25 % can be explained as follows. To explain why the lowest specific contact resistance occurred at a Ge composition of 25 at %, a possible reason, from Woodall's observation on the interfaces of Cu/Ge to n-type GaAs, is that the planar interface is responsible for a better specific contact resistance when the Ge composition was around 25 at % [17].

It is well known that copper introduces electrically active centers in GaAs producing, for example, double compensation [18]. These levels in n-type GaAs exhibit thermal activation energies measured from the valence band at 0.15 eV and 0.45 eV, respectively [14,18]. Since copper tends to occupy a substitutional gallium site [52,53], $Cu_{Ga}$, it would be expected to act as a double acceptor. Therefore, it is necessary for a precise control in composition and annealing conditions to prevent free copper from further diffusion into GaAs. The SCR of

the ohmic contacts shown in Fig. 4 was apparently influenced by the Ge content. Different results have been found by Woodall et al. [15] where only a slight change in SCR was observed as the Ge composition was varied from 15 at % to 30 at %. The increase in SCR at high Ge composition ( i.e., >30 at % ) can be explained by the fact that the contact area of $\varepsilon_1$-$Cu_3Ge$ and $\varsigma$-CuGe to GaAs was reduced due to an increase in proportion of epitaxial Ge grains despite their small interfacial energy barrier to the substrate [19 - 24].

Unique properties of the contact layers, namely low specific contact resistivity, high thermal stability, interface sharpness, and high contact layer uniformity are related to the formation of an ordered orthorhombic $Cu_3Ge$ phase. In the alloyed layer with Ge concentrations >25 at %, there were no phases due to chemical reactions with GaAs in the interface region found, thus demonstrating the chemical inertness of the $Cu_3Ge$ ordered phase with respect to GaAs at temperatures up to 450°C. This results in sharp interfaces and uniform chemical composition, the characteristics needed for superior contacts.

### 3.1.3 Specific contact resistance (SCR) of $Cu_3Ge$ to n-type GaAs as a function of doping density

In this dissertation, $Cu_3Ge$ was deposited and annealed on n-type GaAs with doping concentrations ranging from $1.0x10^{17}$ $cm^{-3}$ to ~ $6.0x10^{18}$ $cm^{-3}$. Hall effect measurements were performed for each sample and the measured sheet resistances were used to test against the slopes determined from the TLM measurements.

The values of sheet resistances determined from these two different measurements agree well with each other as can be seen from Table 1. As seen in Fig. 5, the measured SCR is inversely proportional to increases in the doping concentration in the range of $2.0x10^{17}$ $cm^{-3}$ to ~ $6.0x10^{18}$ $cm^{-3}$. For n-GaAs with a doping density below $2.0x10^{17}$ $cm^{-3}$, the relationship between SCR and $exp(N_d^{-1/2})$ is no longer linear. The straight line shows the $exp(N_d^{-1/2})$ relationship between the SCR and carrier concentration, n, which, at room temperature is very nearly equal to the n-type net doping concentration, $N_d$.

Table 1. Properties of n-type and p-type GaAs as determined by TLM and Hall effect measurements in this dissertation work.

| Sample Number | Doping concentration($cm^{-3}$) | Mobility ($cm^2$/vsec) | Sheet Resistance by Hall(Ω/□) | Sheet Resistance by TLM(Ω/□) |
|---|---|---|---|---|
| CG1 | $5.35x10^{15}$ | 6200 | $2.7x10^{-1}$ | $1.9x10^{-1}$ |
| CG2 | $9x10^{16}$ | 4520 | $1.9x10^{-2}$ | $1.7x10^{-2}$ |
| CG3 | $2.07x10^{17}$ | 4000 | $9.0x10^{-3}$ | $7.5x10^{-3}$ |
| CG4 | $4.07x10^{17}$ | 3300 | $4.7x10^{-3}$ | $4.0x10^{-3}$ |
| CG5 | $8.09x10^{17}$ | 2610 | $2.4x10^{-3}$ | $2.0x10^{-3}$ |
| CG6 | $3.0x10^{18}$ | 1620 | $8.5x10^{-4}$ | $7.2x10^{-4}$ |
| CG7 | $6.0x10^{18}$ | 1100 | $5.8x10^{-4}$ | $4.4x10^{-4}$ |
| CG8 | $6.68x10^{18}$ | __^ | __^ | $7.3x10^{-4}$ |
| CG9* | $8.96x10^{18}$ | 60 | $8.0x10^{-3}$ | $8.4x10^{-3}$ |
| CG10* | $2.38x10^{19}$ | ~20 | $4.2x10^{-3}$ | $4.6x10^{-3}$ |

* p-type GaAs; _^ psuedomorphic-HEMT structure

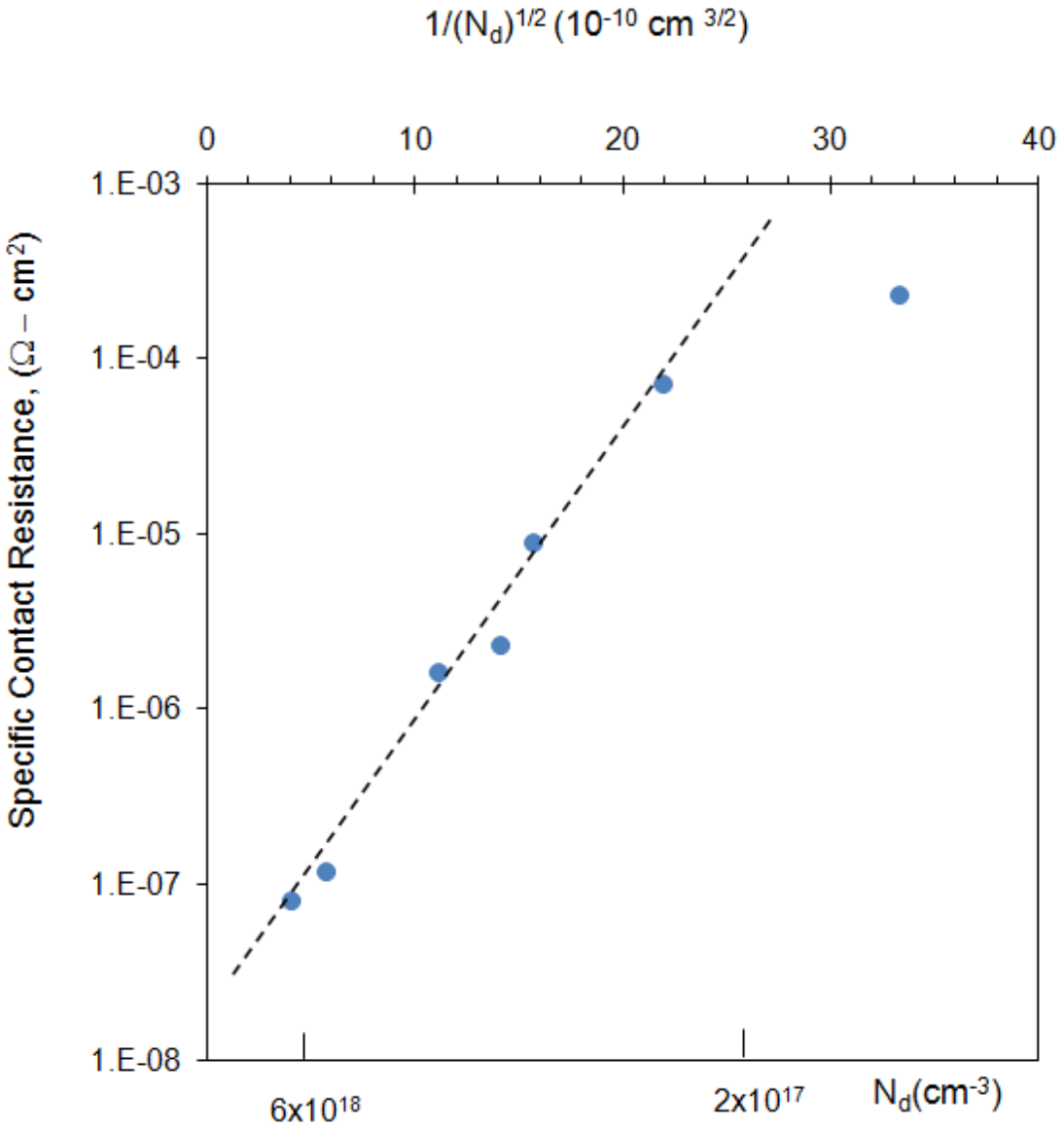



Fig. 5. Measured SCR of $Cu_3Ge$ to n-type GaAs as a function of carrier concentration in GaAs.

This is similar to what has been observed in alloyed contacts where the alloyed contacts tend to have an $N^{-1/2}$ dependence on doping density [25]. The ohmic behavior associated with the tunneling occurs at a doping level $N_d$ of about $3x10^{18}cm^{-3}$, where the characteristic tunneling energy becomes comparable with the thermal energy, *kT*. Also, for doping levels heavier than $3x10^{18}$ $cm^{-3}$, an $exp(N_d^{-1/2})$ dependence of contact resistance was observed as was predicted by theory [48]. For lighter doping, it was found that the contact resistance is independent of $N_d$. When doping concentrations were lower than $2.0x10^{17}$ $cm^{-3}$, the linearity was no longer maintained and the measured SCR was much lower than the value extrapolated by the linear function at the high doping region [25]. The turning point might be direct evidence of the mechanism for ohmic behavior for the following reason: it supports the theory that current transport by tunneling is through a heavily doped $n^+$ layer, which is most likely formed by Ge diffusion into the n-GaAs, because current flow is indeed enhanced for doping densities lower than $3x10^{18}$ $cm^{-3}$. Moreover, it predicts that ohmic behavior will be forbidden for the same material to p-type GaAs with doping concentrations less than $2.0x10^{17}$ $cm^{-3}$ which has been investigated by Woodall et al. [14, 54]. A SCR of $5 \times 10^{-6}$ $\Omega\,cm^2$ has been achieved on p-type GaAs with doping concentration of $7.0x10^{18}$ $cm^{-3}$ [54].

As can be seen from Table 1, the sheet resistance of n-type GaAs determined by TLM measurements agrees well with the Hall measurement results performed on the same samples, respectively, in this dissertation work. The ohmic behavior exhibited on epitaxial p-type GaAs can be attributed to tunneling since doping levels on the two samples were fairly high, with one

doped to $8.98 \times 10^{18}$ $cm^{-3}$ and the other, $2.38 \times 10^{19}$ $cm^{-3}$, respectively. The psuedomorphic HEMT contains three doped layers: a heavily doped GaAs capping layer, a delta doping layer in AlGaAs, and a uniformly doped AlGaAs layer. Hall effect measurements were not performed because extracted data such as sheet resistance represent a complicated combination of these three layers which cannot readily be used to elucidate pertinent data for any of the three single layers. Only the sheet resistance obtained by TLM was recorded as current only flows in the heavily doped GaAs capping layer in the TLM measurement.

### 3.1.4 Ternary (In, Ni, Au) CuGe contacts to n-type GaAs

Attempts to reduce the contact resistance of binary CuGe-based ohmic contacts to n-type GaAs and to enhance their thermal stability by adding In, Ni, and Au were performed in this dissertation study. Rapid thermal annealing (RTA) [55] was used with the forming gas ($N_2/H_2$ ratio of 7/3) for all annealing processes in this dissertation work.

Adding Au into CuGe was found to change the ohmic behavior of CuGe-based contacts to a rectifying one. Fig. 6 shows the I-V characteristics of CuGe-based contacts with and without Au. At the same annealing condition where the binary CuGe contacts had shown linear current-voltage behavior, all Au-containing CuGe contacts formed weak Schottky contacts to n-type GaAs. Changing the layer sequence of Cu, Ge and Au was found to have no influence on this phenomenon.

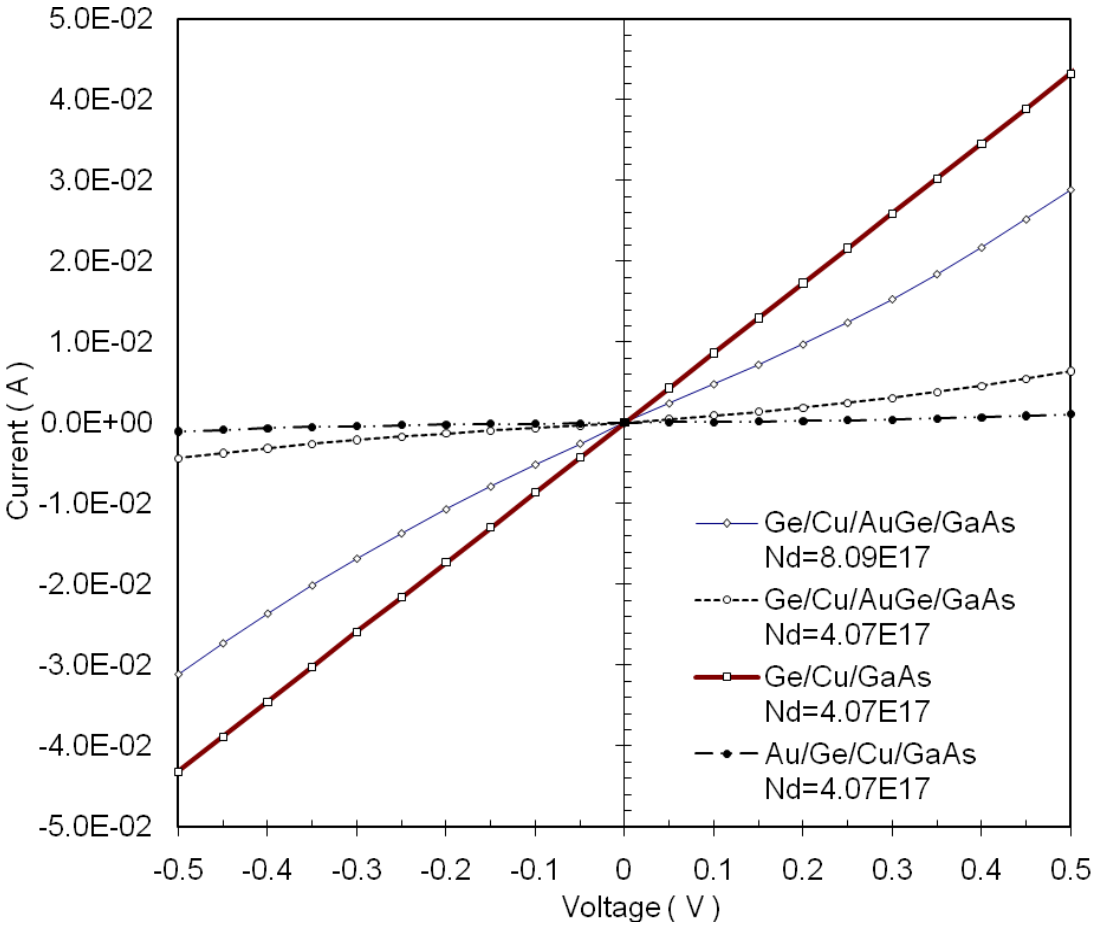



Fig. 6. Current-voltage characteristics of $Cu_3Ge$ to n-type GaAs at room temperature with and without the addition of of gold to this contact system.

Neither the ohmic behavior nor the optimum annealing condition of CuGe-based contacts changed with the addition of In and Ni. However, the specific contact resistance was found to increase when In and Ni were added to the CuGe binary system as can be seen in Fig. 7. The annealing time for the data shown in Fig. 7 was 90 sec in the forming gas. The thermal stability of these ternary alloys will be discussed in Section 3.4.3.

The results from the annealing of Au-CuGe system are of great importance when the operation temperature is increased to 400°C. Thus, if Au is chosen as an overlayer, it must be separated from the CuGe-based contacts by diffusion barrier(s). The observed I-V characteristics can be explained by the change in primary reactions. Originally, reactions are constrained because of the limited reagents in the Cu-Ge binary system.

The additional Au and Ge have a eutectic point at ~365°C and can thus easily play a major and dominant role in the reactions between Cu and Ge at annealing temperatures higher than 400°C. Moreover, ternary Cu-Ge-Au alloys are favored in the temperatures range from 400°C to 600°C, see Fig. 8 [49], so that Ge tends to incorporate into the ternary alloy rather than at the interface. Consequently, no heavily doped layer is formed at the metal/semiconductor interface and this inhibits the ohmic behavior for this contact system.

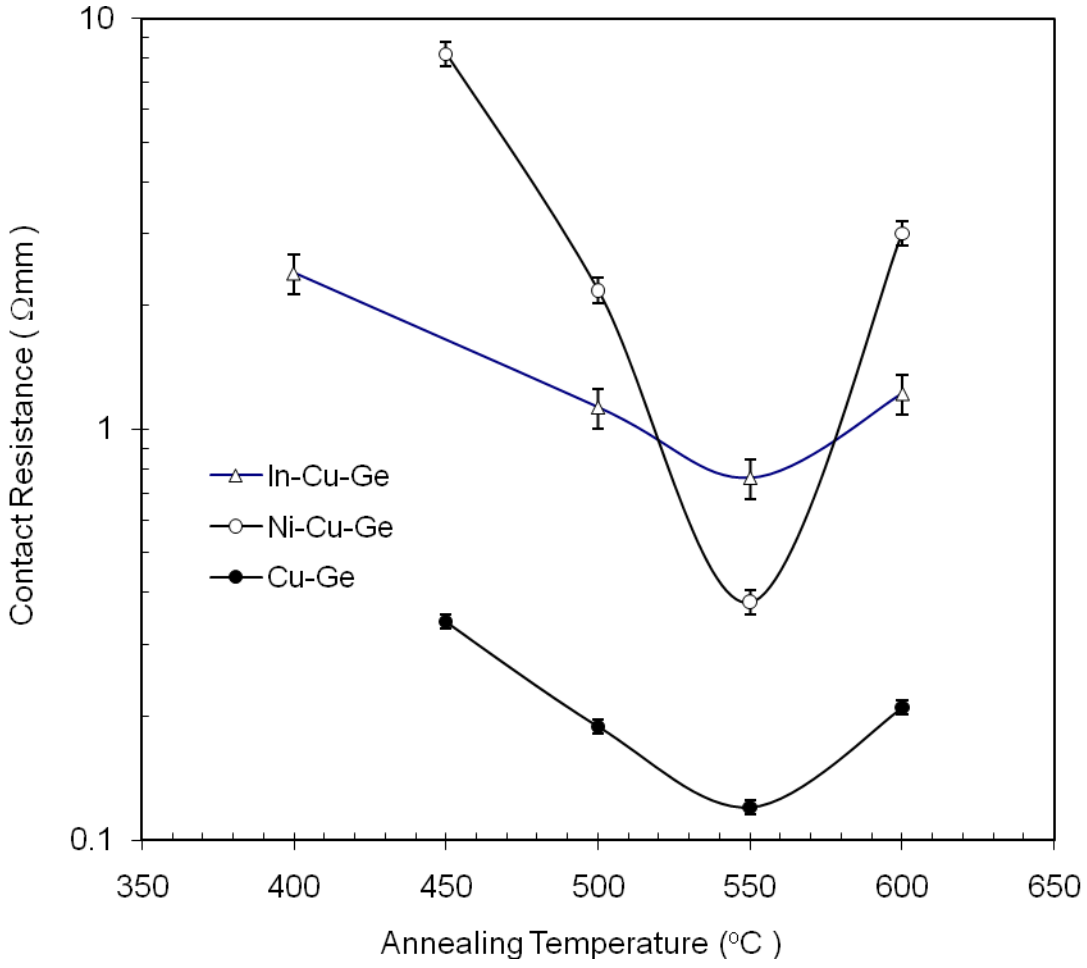



Fig. 7. A comparison between the contact resistance of binary CuGe-based contacts and that of ternary Ni(In)CuGe contacts to n-type GaAs with a doping concentration of $4x10^{17}cm^{-3}$.

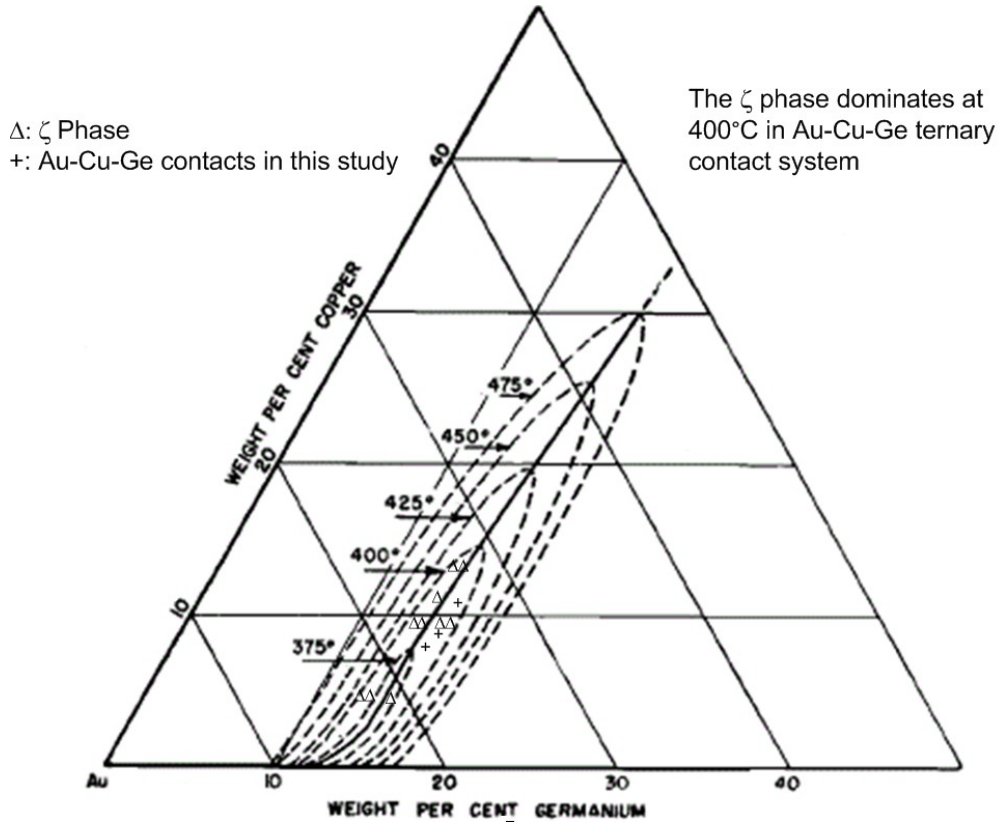



Fig. 8. The ζ phase at 400°C in Au-Cu-Ge ternary contact system (Adapted from [49] ).

### 3.1.5 CuGe-based contacts to other III-V compound semiconductors: GaInP, GaN, and AlGaAs

It is well known that forming ohmic contacts to semiconductors with a wider energy band-gap becomes more difficult compared to narrower band-gap materials [1, 2, 48, 57, 58]. In this dissertation work, three wide-bandgap materials were studied: GaInP, GaN, and AlGaAs. All three of the wide-gap materials used in this section were Si-doped with basic specifications as

tabulated in Table 2. It was not surprising that $Cu_3Ge$ formed ohmic contacts for all three n-type materials.

Thus, this contact scheme essentially appears to be a universal ohmic contact to any n-type semiconductor regardless of the band-gap energy. So far, this behavior can be explained by Ge atoms always occupying the group-III sites in the n-type semiconductors which forms a heavily doped n+ layer thus favoring tunneling.

## 3.2 Carrier transport mechanism and diffusion behavior of polycrystalline-Cu/ amorphous-Ge contacts to GaAs

### 3.2.1 XRD Analysis and I-V Characteristics

Further examinations of Cu-Ge/GaAs contact system before and after heat treatment by X-ray diffraction (XRD) are shown in Fig. 9. The as-deposited, e-beam evaporated Cu on GaAs appears to be polycrystalline, whereas as-

Table 2. Specifications for the three wide-gap semiconductors used in this dissertation work to test the formation of $Cu_3Ge$ ohmic contacts.

| Material | Growth Technique | Band-gap Energy (eV) | $N_d(cm^{-3})$ | Mobility($cm^2$/Vs) | $\rho_c(\Omega cm^2)$ |
|---|---|---|---|---|---|
| GaN | MOCVD | 3.36 | $1.0x10^{18}$ | 100 | $6.7x10^{-4}$ |
| AlGaAs | MBE | 1.79 | $2.57x10^{17}$ | 1875 | $1.3x10^{-4}$ |
| GaInP | MOCVD | 1.90 | $\sim 6.0x10^{16}$ | 3000 | $\sim 1.0x10^{-2}$ |

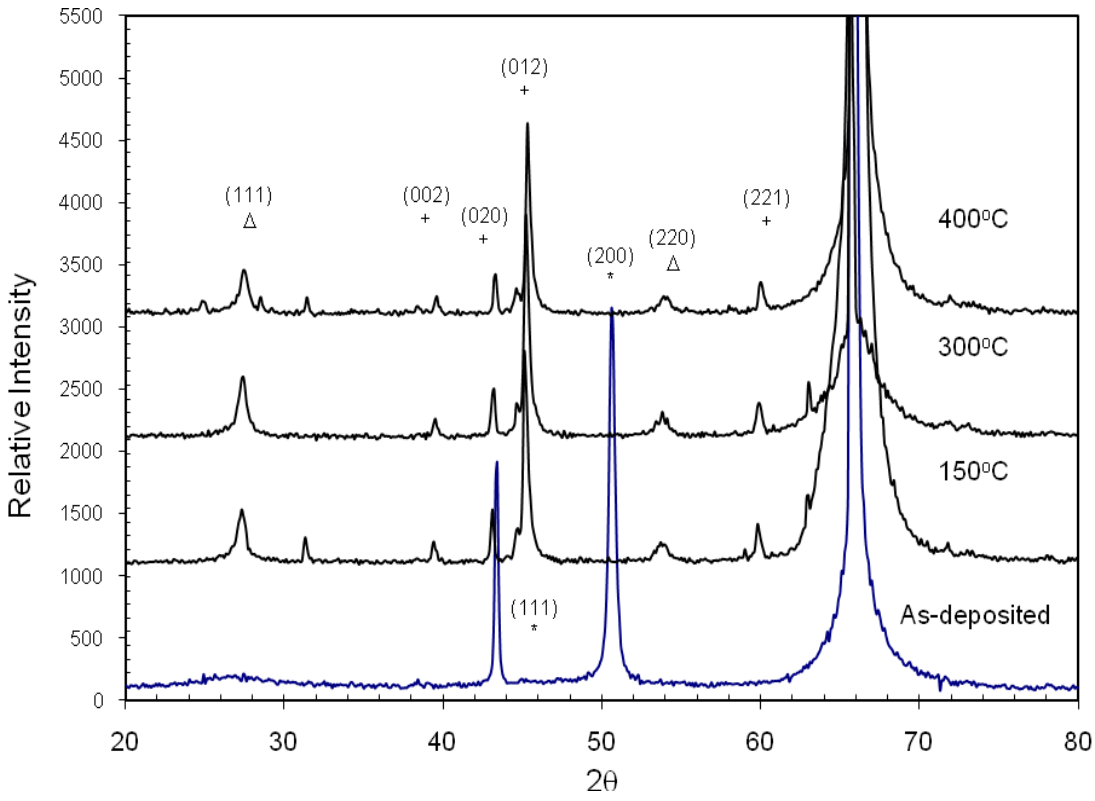



Fig. 9. XRD profiles for Ge(78 nm)/Cu(122 nm)/n-type GaAs after 30 minutes annealing in the forming gas. ( + --- $Cu_3Ge$; * --- Cu; Δ --- Ge )

deposited, e-beam evaporated Ge appears to be amorphous (no peaks observed) on GaAs. It was found that after annealing at 150°C for 30 minutes under forming gas ($H_2$:$N_2$ = 3:7), the strongest peak, the (200) of Cu, was no longer detected by XRD, whereas the (012) peak of $Cu_3Ge$ appeared at $2\theta$ = 45.345° and crystallized Ge peaks were observed at a position of $2\theta$ = 53.73° indicating that the formation of $Cu_3Ge$ was nearly complete. The crystal structure of $Cu_3Ge$ determined by XRD is orthorhombic with lattice constants $a_o$ = 5.031Å, $b_o$ = 4.204 Å, and $c_o$ = 4.555 Å.

TLM measurements showed no sign of ohmic behavior after a 150 hr annealing at 150°C for CuGe-based contacts to n-type GaAs with doping concentrations of $4.07 \times 10^{17}$ $cm^{-3}$. Thus, the formation of $Cu_3Ge$ could not, alone, be directly responsible for the ohmic behavior. Essentially, the Ge has to overcome the barrier between itself and GaAs and then be activated at higher temperatures to reside on Ga-sites to achieve the observed linear current-voltage characteristic.

The XRD data of the CuGe-based contacts after being annealed at 300°C for 30 min were similar to that observed at 150°C except the magnitude of peaks from the $Cu_3Ge$ were slightly higher than that at 150°C due to more reaction products being formed at higher temperatures. This increase in peak intensity was more profound for samples annealed at 400°C with no other peaks than those for $Cu_3Ge$ detected by XRD.

Fig.10 shows the XRD profiles for Ge(78 nm)/Cu(122 nm)/n-type GaAs after 10 min, 20 min, and 30 min annealing times, respectively, at 400ºC in the

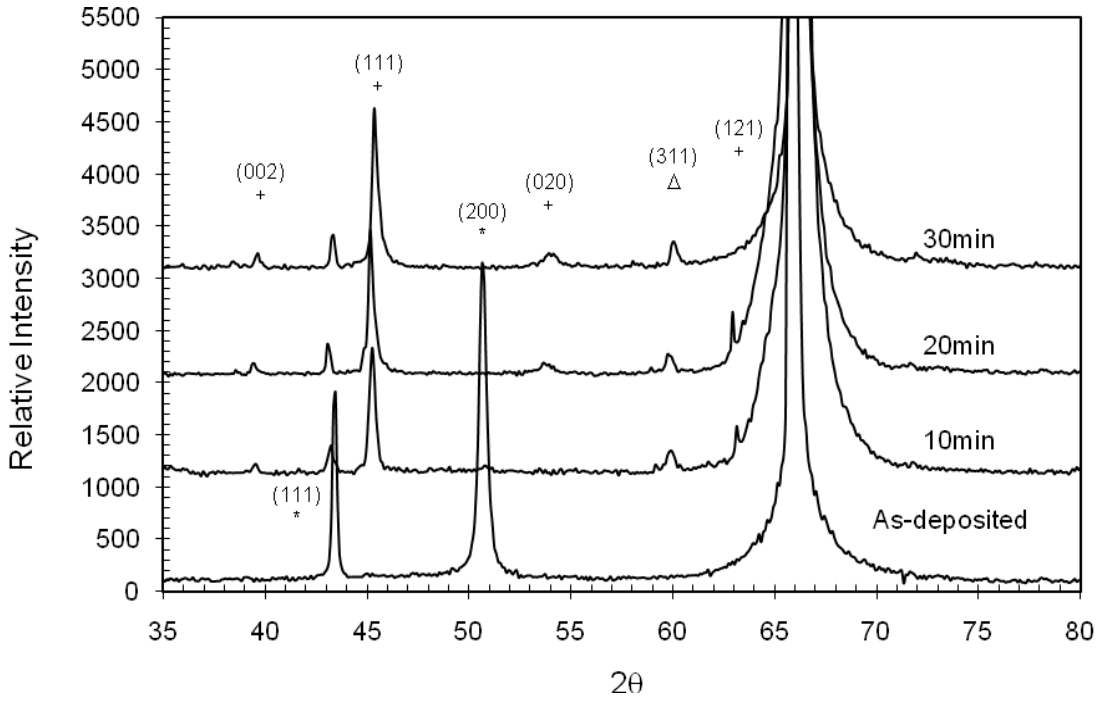



Fig.10. XRD profiles for Ge(78 nm)/Cu(122 nm)/n-type GaAs after 10 min, 20 min, and 30 min annealing at 400°C in the forming gas. ( + --- $Cu_3Ge$; * --- Cu; Δ --- Ge )

forming gas. The orthorohmbic phase and the crystalline Ge phase appear after 10 minutes annealing with no detectable Cu content at this stage. The recrystallization of Ge was observed at 300°C and 400°C according to the XRD patterns in Fig. 10, and the AFM images shown in Figs. 3(e) and (f).

An experiment was performed using 78 nm Ge on top of 122 nm Cu deposited on a n-type GaAs ($N_d = 4.07x10^{17}\ cm^{-3}$) sample covered with $Si_3N_4$

grown at 150°C for the nonmetal areas. TiWN (200 nm) and Au (200 nm) were then sputtered through the etched widows right on top of each contact pad. The sample was then placed on a hot chuck and its temperature was ramped up from room temperature to 150°C in about 20 min. When temperature was stabilized, I-V measurements were performed between two contact pads. The temperature was then increased by 10°C and allowed to be stabilized for 5 min before another set of I-V measurements were taken. This process continued until 300°C was reached.

The I-V characteristics versus annealing temperature are shown in Fig. 11. The first linear I-V curve was observed at 300°C' and when the temperature was immediately brought down to 250°C, the I-V characteristic remained linear and the contact resistance was found to decrease with time up to 120 hr and remain constant after that. The ohmic behavior can be related to the thermal voltage at 300°C, which is 50 meV; if the Ge layer is deposited first, because the Schottky barrier height of Ge to n-type GaAs (Si-doped to $4.07 \times 10^{17}$ $cm^{-3}$) was measured to be approximately 0.06 eV [14], the thermal voltage is very close in value to the Schottky barrier height. In the case where Cu directly contacts to GaAs, carrier transport may be through a mechanism that is different from what has been mentioned previously. However, the SCR of Cu/Ge to n-type GaAs has no relation to the sequence of layer deposition, but the Cu and Ge compositions and the annealing temperatures play significant roles for achieving a low SCR.

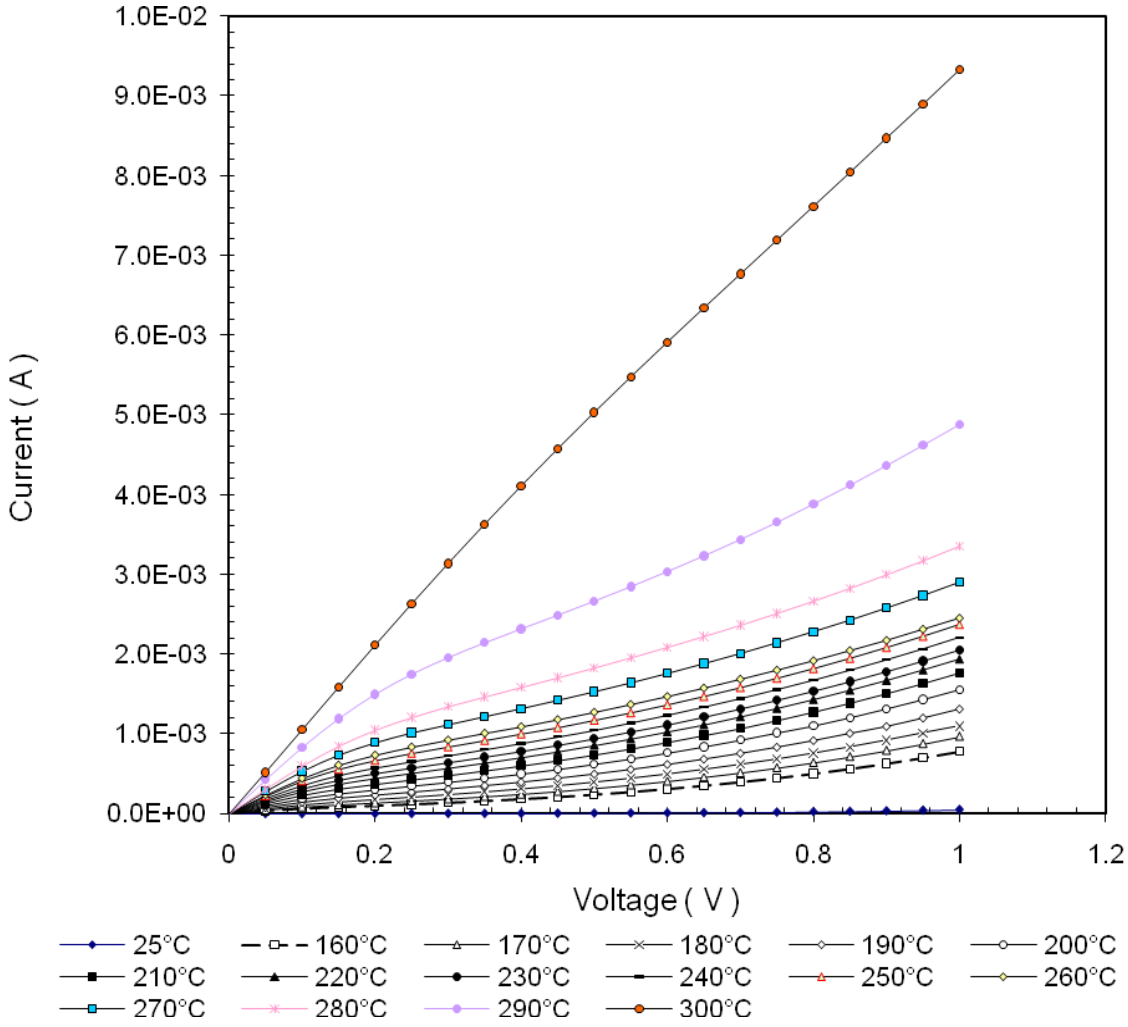



Fig. 11. Current-voltage characteristics at temperatures between 150°C and 300°C for an as-deposited Cu/Ge contact to n-type GaAs.

Microstructure studies on the Cu/Ge ohmic contact system to n-type GaAs revealed an epitaxially grown Ge layer between $Cu_3Ge$ and GaAs interface [14, 15]. XRD results in this dissertation work show that only Ge and $Cu_3Ge$ are detected for Cu/Ge ohmic contacts to n-type GaAs after annealing at 300°C for 30 mins. The results support the carrier transport mechanism being what is shown in Fig. 5 where only tunneling could lead to linear relationship between

the SCR and to $exp(N_d^{-1/2})$. To investigate the current transport mechanism of CuGe contacts, the $R_c$ values were measured at temperatures in the range of –190°C to 150°C for $Cu_3Ge$ and conventional AuGeNi contacts. The relation between the contact resistance and temperature for these contacts is shown in Fig.12. Both types of contacts provided almost the same $R_c$ values of ~ 0.1 Ωmm at room temperature. The essentially unchanged contact resistance over the temperature range investigated in this dissertation indicates that the mechanism of current transport is primarily tunneling, which is relatively temperature independent.

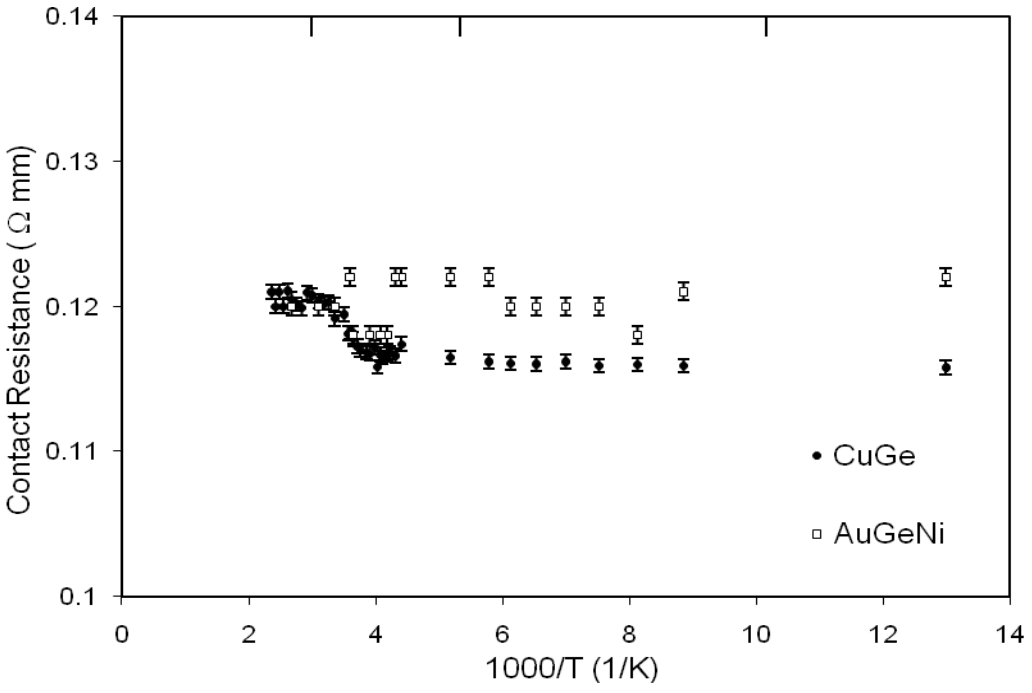



Fig. 12. Contact resistance of CuGe-based and AuGeNi ohmic contacts for temperatures between -190°C and 150°C.

A proposed band diagram at the $Cu_3Ge/n^{++}GaAs/n^{+}GaAs$ interfaces is shown in Fig.13. There are two energy barriers that limit the electron transport through these interfaces; one is the energy barrier ($\phi_b$) between the metal and the heavily doped $n^{++}GaAs$, and the other is the energy barrier ($\phi_o$) between the $n^{++}GaAs$ and $n^{+}GaAs$ layers. If the $R_c$ value is limited by the electron transport through the barrier at the metal/$n^{++}GaAs$ interface, then the $R_c$ value is dominated by the field emission mechanism [26,27] and is relatively insensitive to temperature. Therefore, if this is actually the case, the transport through the barrier at the $n^{++}GaAs/n^{+}GaAs$ interface should be temperature dependent. Together, with results shown in Fig.12, the current transport is controlled by the barrier between $Cu_3Ge$ /$n^{++}$ GaAs, $\Phi_b$. The observed $R_c$-temperature relation suggests a relatively low $\phi_o$ value for the $n^{++}GaAs/n^{+}GaAs$ interface. According to models proposed by Lonnum and Johannessen [26] and Linhard [27], the junction depth, which controls the main current transport, is believed to be nearly equal to the $R_p$ value, where $R_p$ is the junction depth for which the energy barrier $\phi_o$ is a minimum according to the doping concentration at the $n^{++}GaAs$ layer. Secondary ion mass spectrometry (SIMS) profiling has shown that the depth of the junction is in the range of ~60 nm; hence, the doping concentration in the heavily doped region is in the range of $5\sim6x10^{19}$ $cm^{-3}$, according to Linhard's model.

In case Ge exists between the $Cu_3Ge$ and $n^{++}GaAs$ layers, the effective barrier of $\phi_b$ will not increase too much since the conduction band discontinuity between GaAs and Ge is reported to be only 0.06eV, meaning that the voltage

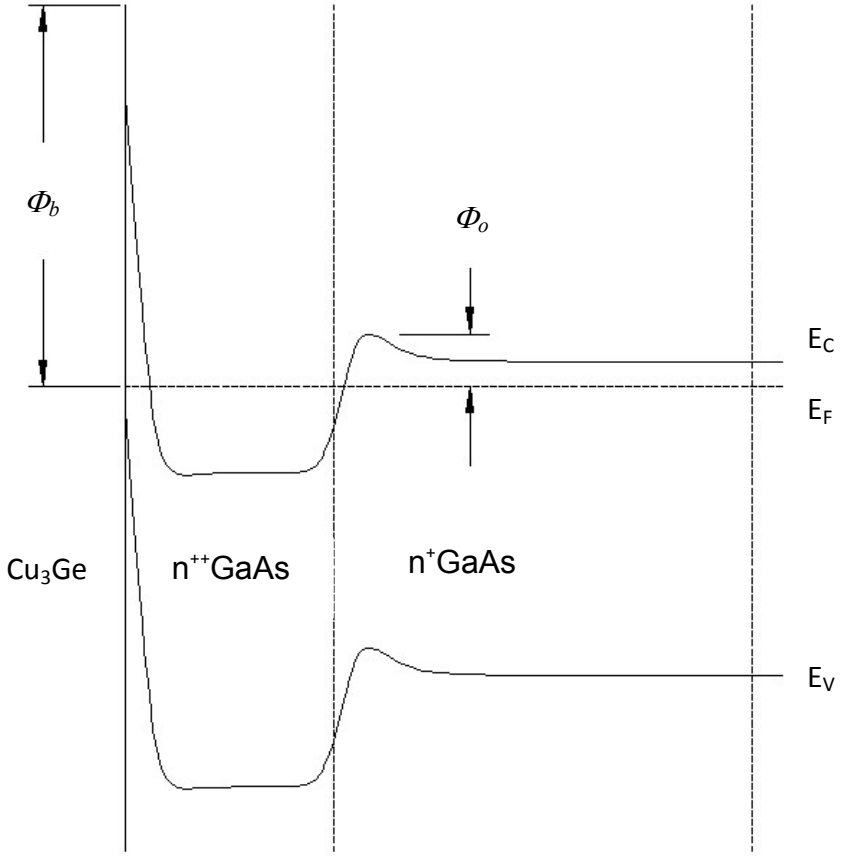



Fig. 13. A proposed schematic band diagram for the CuGe/n-type GaAs interfaces after annealing. $\Phi_b$ and $\Phi_o$ are the barriers between $Cu_3Ge/n^{++}GaAs$ and $n^{++}GaAs/n^{+}GaAs$, respectively.

drop at the GaAs/Ge interface is essentially negligible. Current transport is then limited by the energy barriers at the $Cu_3Ge$/n+Ge ($\phi_b$) and the $n^{++}GaAs/n^{+}GaAs$ interfaces. For a deep junction where $\phi_b$, the Schottky barrier between $Cu_3Ge$ and $n^{++}GaAs$ is relatively high, as in the $Cu_3Ge$/GaAs system, the contact conduction is dominated by field emission to transport current through the metal/heavily doped GaAs(Ge) interface. In this case, the tunneling probability is

relatively independent of temperature.

### 3.2.2 Differential scanning calorimetry (DSC) analysis

The objective of this part was to identify the reactions observed using X-ray analysis. Thermal analysis is of high sensitivity and can be used in thin-film studies as long as the mass of the thin film can be accurately measured. Six pairs of Poly-Cu(122 nm)/$\alpha$-Ge(78 nm) were deposited on semiinsulating GaAs using electron-beam evaporation and cleaved into 5.12 mm x 4.82 mm rectangles for the DSC analysis. The temperature ramp rate was set to 10°C/min and a standard procedure recommended by the manufacturer was followed [61]. Fig. 14 shows the relation between heat flow, which is the difference in the amount of heat required to increase the temperature of a sample and reference, and the temperature. A valley at a temperature of 232°C represents an exothermic reaction. It is very surprising that the reaction identified by XRD at low temperatures did not appear in the DSC profile. Thus, the exothermic reaction is related to either the phase transformation or decomposition of $Cu_3Ge$. Possible phase evolutions have been given in Ref. [49] where $Cu_3Ge(\varepsilon_1)$ and $Cu_5Ge(\varsigma)$ are two phases which are highly favored in the temperature and composition range.

Integration of the area under the heat flow curve yields the enthalpy change associated with the thermal event of interest [62, 63]. A value of 95 Kcal/gram was obtained for the heat flow curve given in Fig. 14. Such a low enthalpy indicates a fast reaction between Cu and Ge, which is in agreement

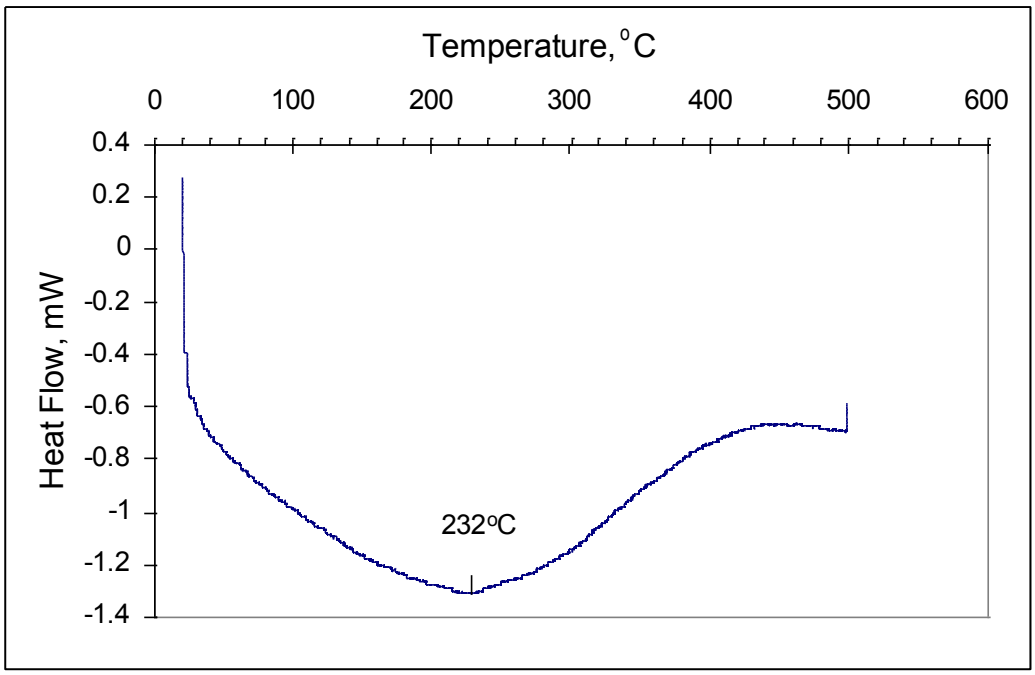



Fig. 14. DSC analysis for Cu/Ge contacts on semi-insulating GaAs.

with XRD analysis and the van der Pauw measurements in Section 3.2.3. However, the exotherm did not appear as sharp as in the transition for melting or decomposition reactions. It is possible that the enthalpy of reaction might have been overestimated due to the ambiguity of the ends of the reaction.

### 3.2.3 Kinetics of thin-film reactions of Cu/$\alpha$-Ge bilayers on semiinsulating GaAs

#### 3.2.3.1 Van der Pauw measurement

It has been found that $Cu_3Ge$ exhibits unexpectedly low electrical resistivities at room temperature and is believed to be the only phase formed in the thin-film reactions between Cu and Ge [16,17]. Unlike the silicides, which

have been widely studied [70,71], the literature on copper germanides is very limited [28], especially on GaAs substrates. The thin-film reaction kinetics has not been systematically investigated. However because of its importance on the reliability issue when subjected to high temperature, such an investigation is needed. Therefore, in this section, a detailed characterization of the diffusion behavior, phase formation, and kinetics of thin-film reactions between polycrystalline Cu ( Poly-Cu ) and amorphous Ge ( $\alpha$-Ge ) films is presented as a function of annealing conditions.

Fig. 15 shows the variation of resistance, R, of a 550 nm Ge on 440 nm Cu thin film contact on a semiinsulating GaAs wafer annealed under temperature, T, that was increased at rates *dT/dt* of 0.2, 1.0, and 5.0 °C/min, respectively. The similarity of these curves suggests the same basic reaction path for all heating rates studied in this dissertation. The basic behavior can be summarized as follows: From room temperature to ~100°C, the resistance increases linearly with temperature, T, from ~0.0077 $\Omega$ to ~0.01 $\Omega$ and then increases rapidly as the first reaction occurred. At temperatures between 100°C and 180°C, the normalized total resistance was exponentially proportional to temperature and dependent on the temperature ramp rates. The resistance first reached a peak value and then dropped to a minimum within 10°C at temperatures between 130°C and 180°C, depending on the ramp rate. Finally, the resistance increased further in the temperature range from 180°C to 230°C, but not as rapid an increase as took place for the first reaction. The second region of resistance increase is also dependent on the temperature ramp rate. The second region of

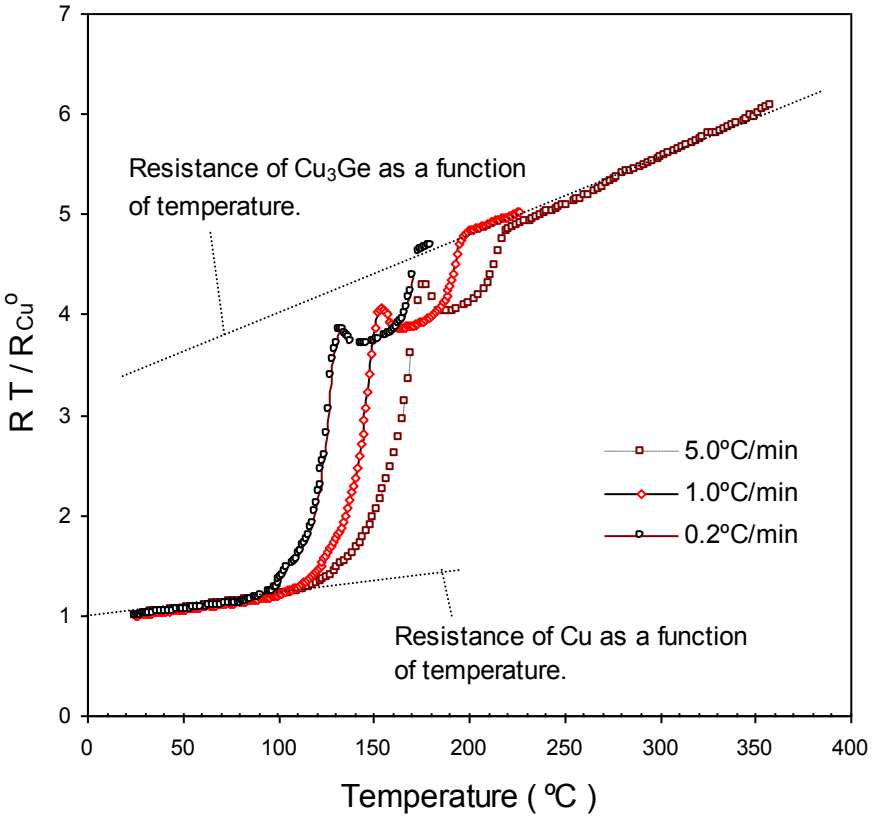



Fig. 15. Normalized total resistance of Cu/Ge contacts on semiinsulating GaAs at temperatures between room temperature and 370°C. The heating rates used in the measurements are 0.2°C/min, 1.0°C/min, and 5.0°C/min, respectively. $R_{Cu}^{o}$ , copper resistance at 0°C, equals to 0.0077 Ω.

resistance increase was followed by a linear resistance change to ~370°C. As mentioned in section 3.2.1, the XRD analysis for samples heated to 150°C, 210°C, and 300°C, respectively, showed no extra phases other than $Cu_3Ge$ and crystallized Ge. Thus, the first region of all curves in Fig. 15 can be denoted as and considered to be the formation of $Cu_3Ge$. However, there still is not enough evidence to say what the second reaction is. The second region of all curves in Fig. 15 actually occurred with a decrease in the total resistance of the thin-film, and the reaction was almost independent of heating rate. It is worth noting that, in Fig. 15, all transition points from which the resistance started to decrease fell below the extended second linear region, indicating that they represented departure from the completion of the formation of the $Cu_3Ge$ phase. It is still unknown at this time why the second reaction was complete within 40°C regardless of the initial starting temperature.

3.2.3.2. Reaction kinetics analysis

To quantify the above results, the R(T) data in Fig.15 were modeled using a three-layer parallel resistor model [28]. The Ge, $Cu_3Ge$, and Cu layers were assumed to be simple resistors with the resistance of each phase scaling linearly with the layer thickness. The Ge layer was not found to contribute significantly to electrical conduction in the structure, and hence, a two-layer parallel resistor model effectively sufficed for this modeling effort.

Fig. 16 shows a detailed R(T) result for a sample heated from room temperature to 375°C at a heating rate of 1°C/min. The thickness of Cu and Ge

were 380 nm and 780 nm, respectively. Before the reaction, the majority of the current was conducted through the Cu thin film; the initial linear resistance increase is due to the temperature variation of the resistance of the Cu thin film.

The same argument applies to the second linear resistance change after the reaction, which provides an indication of the temperature coefficient for the resistance of the $Cu_3Ge$ thin-film. Thus, the first part of the model accounts for the linear resistance of the initial and final phases of the $Cu_3Ge$ thin-film behavior.

Assuming a standard parallel-resistor equivalent circuit [28],

$$R(T)^{-1} = \left( R_{Cu}^{0} + T\frac{dR_{Cu}}{dT} \right)^{-1} [1 - x(T)] + \left( R_{CG}^{0} + T\frac{dR_{CG}}{dT} \right) x(T) \qquad (6)$$

where *x(T)* is the normalized germanide thickness, the room-temperature resistances and the rate of change of resistance with temperature for Cu and $Cu_3Ge$ layers are $R_{Cu}^{o}$ and $dR_{Cu}/dT$ and $R_{CG}^{o}$ and $dR_{CG}/dT$, respectively.

From the fitting of the curves shown in Fig.15, the following values were obtained:

$R_{Cu}^{o}$ = 0.0077 Ω at 0°C, $dR_{Cu}/dT$ = 2.67x10-5 Ω/°C, $R_{CG}^{o}$ = 0.0273 Ω at 0°C, and $dR_{CG}/dT$ = 1.2x10-4 Ω/°C, in good agreement with previous measurements for Cu and $Cu_3Ge$ [28] .

An assumption, based on the observation of planar interfaces [17], was made that the nucleation rate was high for all the temperatures considered and there were no nucleation-limiting regions. Thus, a standard equation for the germanide thickness *x(T)* was used to described the reaction [28].

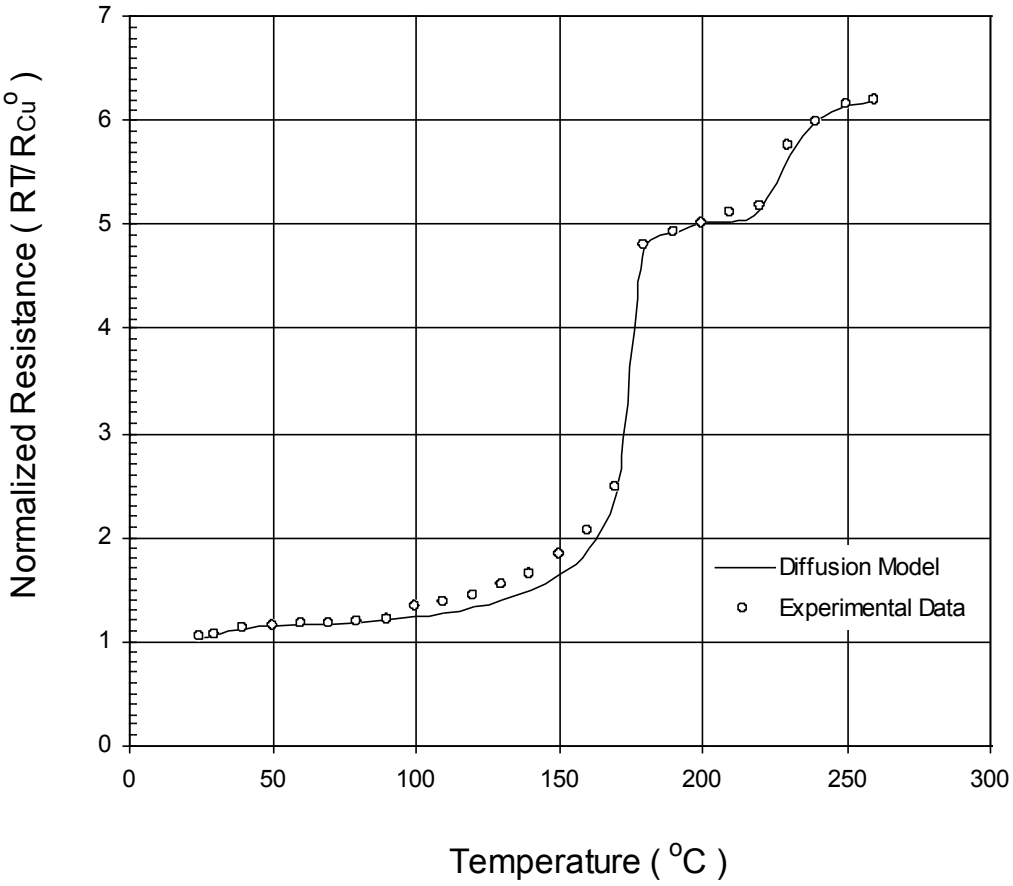



Fig. 16. Comparison of the normalized experimentally measured resistance of Cu/Ge contacts to n-type GaAs using the van der Pauw measurement technique to simulated results from the diffusion model. The experimental data are taken at a heating rate of 1.0°C/min. Note the excellent agreement between the experimental measurements and the simulated results.

$$\frac{dx(T)}{dt} = \frac{D(C/N)k_s}{D + k_s x(T)} \qquad (7)$$

where $D$ is the diffusivity of the moving species and is presumed to be of the general form $D_o e^{-Q/kT}$ , where $D_o$ is a constant, $k$ is Boltzmann's constant, and $Q$ is the diffusion activation energy; $C$ and $N$ denote the concentration of the reactant and the number of product species per unit volume, respectively; $k_s$ is the reaction rate constant; and $t$ is the heating time.

If it is assumed that the reaction is diffusion rate limited, then

Eq.(7) can be simplified by assuming $k_s x(T) >> D$ to give

$$dx^2(T) = 2D(C/N)\, dt = 2D\, dt \qquad (8)$$

Because there were no data to make a quantitative estimate of $C/N$, it was taken as unity for the current calculations in this dissertation. The only effect that a nonunity value of $C/N$ will have, assuming that $C/N$ is not temperature dependent in the range of temperatures investigated in this this dissertation, is to introduce a multiplicative factor in Eq. (8) if $C/N$ is not unity. From Eq. (8),

$$x^2(T) = \int_{273}^{T} 2D_0 e^{-Q/kT} \left(\frac{dt}{dT}\right) dT = \frac{2D_0}{r} \int_{273}^{T} e^{-Q/kT}\, dT \qquad (9)$$

Similar equations were developed for the reaction-rate-limited case [$D >> k_s$]

Equation (9) was numerically integrated using the **MATHEMATICA™** software package to yield *x(T)*. This was then substituted into Eq. (6) to fit the portion of curve in which the reaction occurred. The complete fit for the 1.0 °C/min heating rate curve is shown in Fig. 16 as the solid line. Changes in $D_o$ were found to translate the fitted curve along the temperature axis while changes in *Q* changed the shape of the curve.

The diffusion-limited model was found to fit the first reaction very well but not the second one. The model was modified to incorporate a reaction rate limited mechanism for curve fitting. According to the data shown in Fig. 15, there appears to be a new phase formed during the reactions that is different from $Cu_3Ge$. The resistance and the resistance change rate with temperature of the new phase $R_X^o$ and $dR_X/dT$, respectively, used in the calculations were 0.0303 Ω and 2.67x10-5 Ω/°C, respectively. A value for the reaction rate constant of $1.0x10^{-10}$ cm/sec was found to yield better results in terms of fitting the second part of the reactions. Possible reactions which could account for the rate-limited process could be the mixing of $Cu_3Ge$ with Ge or a phase transformation of $Cu_3Ge$ from one phase to another as has been observed by Woodall et al. [14,15].

The diffusion rate was found to have an average activation energy of 0.89 ± 0.02 eV and a preexponential factor $D_o = 3.0 \pm 0.5 \times 10^{-3}$ cm$^2$/s, although the $D_o$ value may have been affected by errors in the *C/N* = 1 assumption. The activation energy of 0.89 eV/atom is ~0.04 eV higher than that reported by Wang [28] in their work on the same material on silicon dioxide. The difference might

result from the larger grain sizes in this work. This result suggests that Cu and Ge atoms in $Cu_3Ge$ were transported primarily through the grain boundaries, based on the activation energy being less than 1.0 eV.

### 3.2.4 Secondary ion mass-spectroscopy (SIMS) analysis and Boltzmann-Matano method

Secondary ion mass spectroscopy (SIMS) is a technique used in materials science and surface science to analyze the composition of solid surfaces and thin films by sputtering the surface of the specimen with a focused primary ion beam and collecting and analyzing ejected secondary ions. These secondary ions are measured with a mass spectrometer to determine the elemental, isotopic, or molecular composition of the surface. SIMS is the most sensitive surface analysis technique, being able to detect elements present in the parts per billion range [56].

The time of flight (TOF) mass analyzer separates the ions in a field-free drift path according to their kinetic energy. The TOF technique requires pulsed secondary ion generation using either a pulsed primary ion gun or a pulsed secondary ion extraction. It is the only analyzer type able to detect all generated secondary ions simultaneously, and is the standard analyzer for static SIMS instruments.

Fig.17 is a partial SIMS depth profile for a sample of CuGe on n-GaAs that received thermal treatments at 400°C for 30 min. The interdiffusion coefficient of Cu and Ge in GaAs can be extracted from the depth profile by the

Boltzmann-Matano method [29]. Fick's second law can be formulated into an ordinary-differential equation as given by:

$$\tilde{D} = -\frac{1}{2t}\frac{1}{(dc/dx)}\int_{c_1}^{c} x\,dc \qquad (14)$$

where $D$ is the interdifffusion coefficient of the Cu(Ge) component, t is time, ($dc/dx$) is the slope of the depth profile at concentration $c$, and $c_1$ is the initial concentration of the component at t = 0. Concentration $c$ is defined as the concentration at the Boltzmann-Matano interface that the plane from which the integration of the areas under the concentration-distance curve from $C_1$ and to $C_2$ (concentration after diffusion has taken place for a time t) are equal.

The interdiffusion coefficients of Cu and Ge in GaAs at 400°C were calculated to be $5\times10^{-15}$ $cm^2$/sec and $1.55\times10^{-14}$ $cm^2$/sec, respectively. Adding Cu into Ge was found to enhance the diffusion of Ge into GaAs compared with a published value of the diffusion coefficient for Ge at 400°C ($6\times10^{-21}$ $cm^2$/sec) [15].

This behavior of the Ge impurity in the presence of Cu gives very strong evidence that the most probable mechanism for ohmic contact creation is a formation of a highly Ge-doped n+layer at the $Cu_3Ge$/n-GaAs interface.

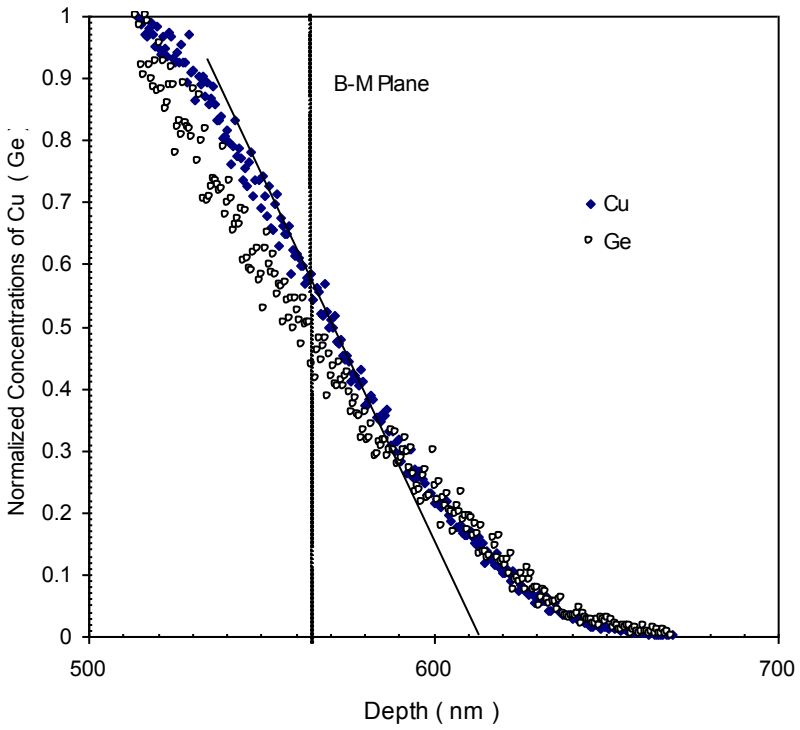



Fig. 17. A plot of the normalized concentrations of Cu and Ge versus depth. The Boltzman-Matano method was used to determine the interdiffusion coefficient of Cu and Ge in $Cu_3Ge$. The concentration-distance curve is measured by TOF-SIMS from samples of CuGe on n-GaAs after annealing at 400°C for 30 min.

## 3.3 TiWN diffusion barrier for CuGe-based ohmic contacts

### 3.3.1 General introduction of thin films

The intrinsic stress of thin films prepared by physical vapor deposition techniques is known to vary with preparation and deposition conditions. Numerous reports have, for example, indicated that sputtering at low gas pressures results in compressively stressed films, while high gas pressures

produce tensile films [30-32]. It is generally believed that changes in arrival energies and the numeric ratio of gas atoms reflected by the target and atoms sputtered from the target play a dominant role in the evolution of film structure accounting for these stresses [33]. At low pressure, the arrival energies of atoms of both groups are only slightly modified by collisions as they move from the target to the substrate. As a result, energetic atoms from both groups bombard the uppermost layers of the film causing densification through atomic rearrangement and compressive film stress. At high pressures, collisions reduce such bombardment and the associated particle energy and increase the oblique angles of incidence for sputtered atoms arriving at the surface of the growing film causing atomic shadowing [34]. This combination of effects results in films with a microstructure that is columnar and has voided growth boundaries. Such films are associated with in-plane tensile stresses resulting from attractive forces between columns [34]. The total void volume, distribution, and connectivity are also thought to affect a number of other film properties [34,35].

### 3.3.2 Electrical and physical properties of RF-sputtered TiWN films

Diffusion barriers are often used for protecting metal interconnection or contact materials especially at high temperatures; however finding a way to produce void-free and dense films becomes an even more demanding challenge since a contact degradation mechanism known as “hillocks” is routinely observed in films with poor protection layers. The origin of the hillock formation is the compressive stress, and the main mass transport mechanism for hillock

formation is the grain boundary diffusion for thin films with a columnar structure [72-74].

Particularly, for high temperature operation, which requires thermally stable, chemically inert, and electrically enhanced contacts to assure reliable functionality, it is very important to introduce additional barrier(s) to stabilize the contact materials.

Titanium tungsten nitride (TiWN) has been reported as a Schottky contact to n-type GaAs with a high degree of thermal stability [42-47]. More often, it is used to protect Au-Ge-based ohmic contacts and some other interconnection metals. For Cu-Ge-based ohmic contacts to n-type GaAs, up to this date, the author of this dissertation has been a member in the only research group to report on the ability to maintain the low resistance contacts over long periods of high temperature exposure at temperatures up to 400°C.

It is worthwhile to address the importance of controlling the film properties for high temperature devices. As an example, high contact resistance to the drain and source of FETs effectively results in low transconductance and high pinch-off voltage, and, hence, poor high-frequency performance. The emphasis of this section is on the effect of the preparation and process conditions of the diffusion barriers on the thermal stability of the ohmic contacts barriers. Special interest is given to the crystal structure, mechanical properties, and electrical properties of sputtered TiWN films in this dissertation work.

To study these relations experimentally a series of $TiWN_x$ layers were RF-magnetron sputtered at various nitrogen and argon pressures and at a fixed target to substrate distance.

The characterization of film properties is summarized as follows. Film thickness was measured using a Sloan Dektak - IIA surface profiler and film resistivity was obtained using four-point measurements. X-ray diffraction is a very powerful technique to monitor film structural properties. The film compositions were measured by XPS in which a characteristic x-ray from an aluminum target was used as the light source and the binding energies of atoms were measured.

A SEM and an AFM were used to measure both the surface morphology and grain size. The grain size obtained by X-ray diffraction and AFM were compared. Stresses were measured and investigated using a Sloan Dektak - II A surface profiler. The intrinsic stress was determined by the traced strain on the samples before and after thin film deposition. The calculation of intrinsic stress will be separately discussed in Section 3.3.3.

All parameters of the sample preparation are tabulated in Table 3. Films were prepared with a wide range of nitrogen concentrations, from 10% to 40%, and powers, from 100 W to 400 W, as seen from Table 3.

The as-deposited $Ti_{0.3}W_{0.7}$ was found to be polycrystalline with a face-centered cubic (F.C.C) structure and a lattice constant of 3.16 Å based on XRD results as shown in Fig. 18. W and TiW have different phases and their properties change depending on all of the parameters involved in the deposition and processing [36-38].

Reported phase-preparation conditions and relationships have shown that the argon (Ar) partial pressure plays the most important role in determining the phase for as-deposited W films [36]. The results are profoundly useful in the Ti-W-N system, but this ternary system has much more complexity than pure W

Table 3. Parameters and properties of RF-sputtered TiW and TiWN films.

| Material | RF Power (W) | DC Bias (V) | Argon Pressure (mTorr) | Nitrogen +Argon Pressure (mTorr) | Deposition Rate (Å/min) | Grain size(Å) | RMS Roughness (Å) | Resistivity (Ωcm) |
|---|---|---|---|---|---|---|---|---|
| TiW | 150 | -186 | 3.6 | 3.6 | 100 | | 10-15 | 8.0E-5 |
| TIWN | 150 | -198 | 3.6 | 4.3 | 76 | 350-360 | 10-15 | 4.4E-4 |
| TIWN | 150 | -207 | 3.6 | 5.4 | 67.5 | 360-390 | 10-15 | 1.2E-3 |
| TIWN | 150 | -225 | 3.6 | 10.0 | 50 | 400-410 | 10-15 | 3.14E-3 |
| TIWN | 300 | -288 | 3.6 | 4.3 | 125 | 350-360 | 10-15 | 3.9E-4 |
| TIWN | 400 | -366 | 3.6 | 4.3 | 170 | 350-360 | 10-15 | 1.65E-4 |
| TIWN | 150 | -170 | 3.6 | 6.5 | 60 | 350-360 | 10-15 | 1.8E-3 |
| TIWN | 300 | -257 | 3.6 | 6.5 | 105 | 350-360 | 10-15 | 1.6E-3 |
| TIWN | 400 | -331 | 3.6 | 6.5 | 135 | 350-360 | 10-15 | 5.0E-4 |

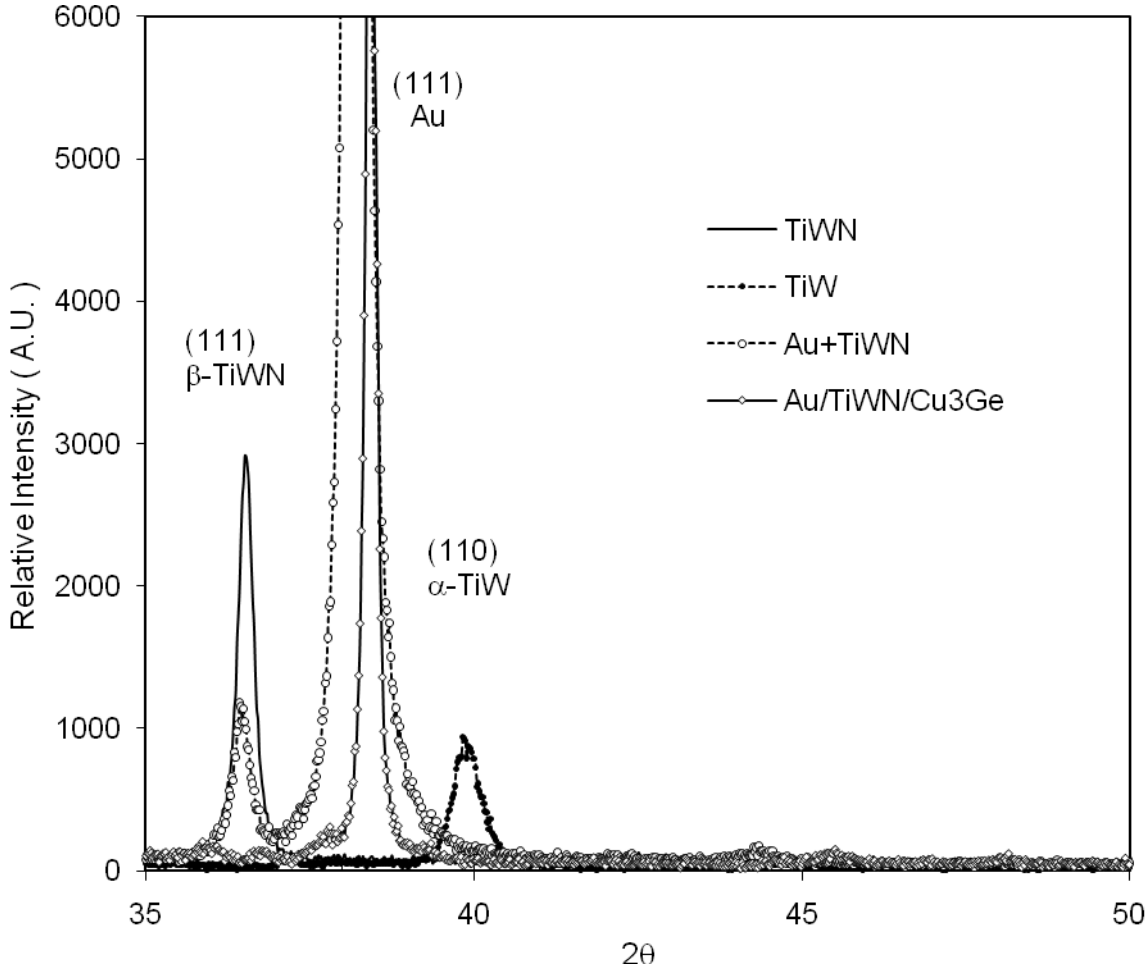



Fig. 18. XRD profiles for RF sputtered TiW and TiWN thin films deposited on GaAs and $Cu_3Ge$/GaAs materials.

primarily because of the incorporation of oxygen and nitrogen in the Ti-W-N system. For TiW-nitrides, the $\alpha$-phase is considered to be more stable than the $\beta$-phase and, hence, is favored when high temperature operation is the goal.

In the Au/TiWN/Ge/Cu/n-GaAs multijunction systems, it has been shown that Ohmic to Schottky transitions can occur if there is a failure to stabilize the stoichiometry between Cu and Ge [54]. Also, nonreacted Cu and Ge will cause either higher contact resistance or excessive diffusion. The other issue regarding the Au overlayer for bonding, which is essential for adapting CuGe-based contacts to integrated circuits, is to prevent intermixing of Cu-Ge and Au by using a TiWN layer as a diffusion barrier.

The resistivity of the RF-sputtered films as a function of $N_2$ percentage is plotted in Fig. 19 on a log scale for two RF-power levels, 150 W and 400 W, respectively. One of the interesting features in Fig. 19 shows the exponential relationship between the resistivity and $N_2$ gas composition in the sputtering environment.

Fig. 20 shows a linear increase in deposition rate with respect to the RF-power for 10% $N_2$ and 25% $N_2$ gas compositions, respectively. For all samples sputtered, the argon pressure was kept constant at 3.6 mTorr. Changing the $N_2$ percentage from 10% to 30% results in a decrease of 33.3% in the deposition rate for films prepared at a power of 150 W, and 28% for those prepared at 400 W. Increasing the gas pressure during sputtering is known to increase the oblique angle of incident of sputtered atoms arriving at the surface of the growing film causing atomic shadowing [34,35]. A decrease in deposition rate with gas pressure is then expected if this argument holds true.

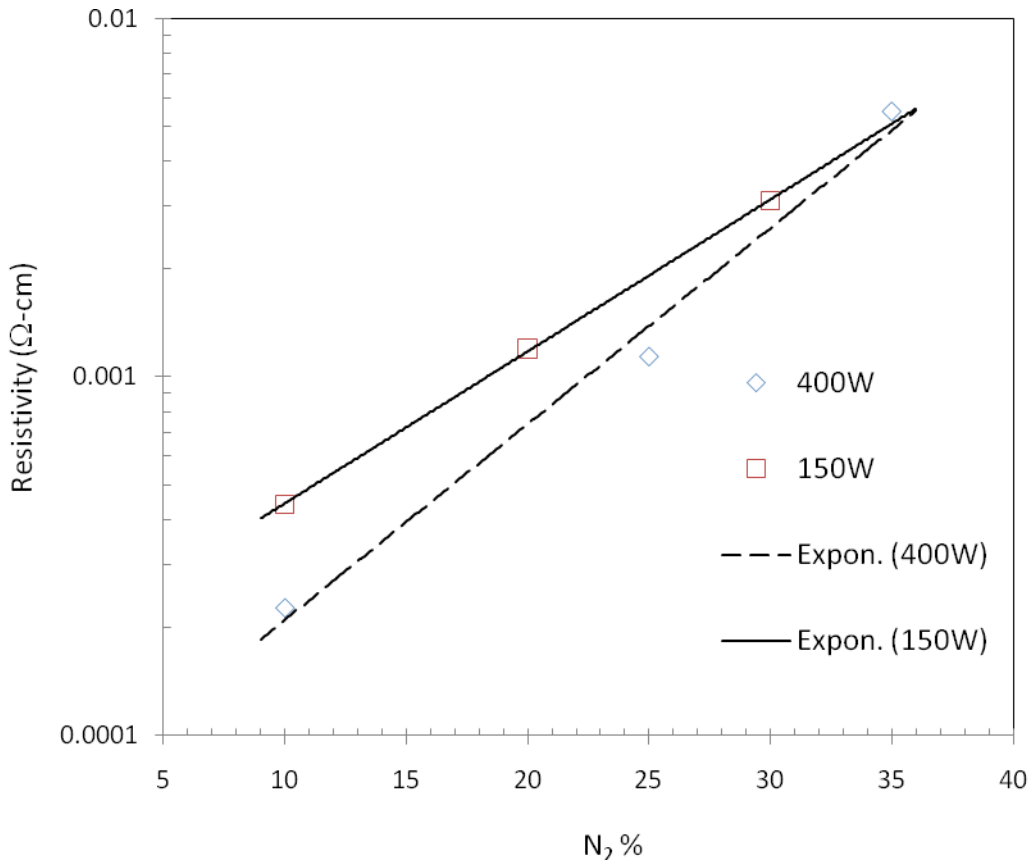



Fig. 19. Resistivities of RF-sputtered TiWN thin films as a function of nitrogen gas composition during sputtering and RF sputtering power level.

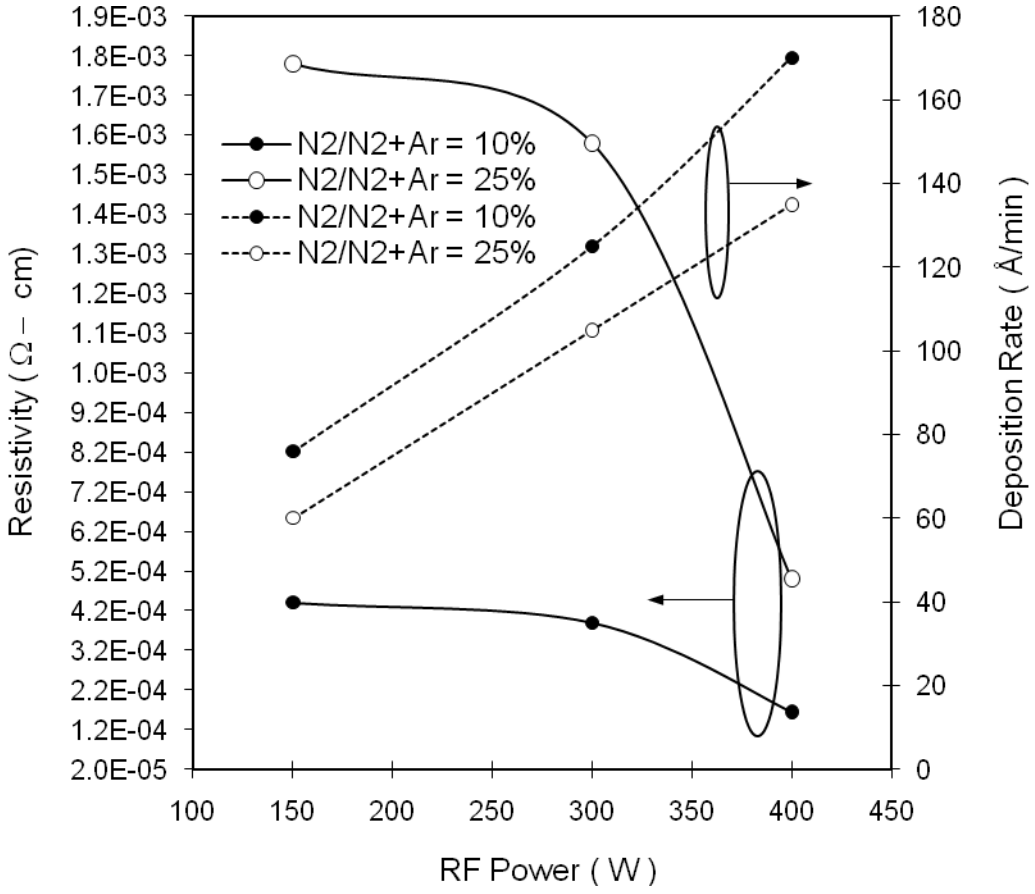



Fig. 20. Deposition rates and resistivities of RF magnetron sputtered TiWN thin films as a function of RF sputtering power at different nitrogen gas compositions.

Also, changes in film resistivity at increased power levels are less profound and become significant only when the RF-power was increased to 400 W. For both $N_2$ sputtering composition levels, the trend remained the same and only changed in magnitude. The density of atoms deposited on the anode from the target increases when sputtering power increases due to an increased rate of bombardment of the target by the Ar plasma. Surface conductivity of the deposited materials is thus improved. When the $N_2$ composition is increased, the deposition rate decreases due to collisions of source atoms with the the sputter gases, which is caused by the shortened mean free path between the sputter gases and the sputtered material. The amount of nitrogen incorporated into the film deposited at 400 W may be higher than that deposited at 100 W and this may explain why the difference in resistivity disappears at higher nitrogen concentrations.

Because film resistivity strongly depends upon the crystalline structure and impurities, to interpret what was experimentally observed, it is necessary to perform further characterization measurements and determine the factors that are responsible for this behavior and, if possible, to do so without any ambiguities.

The XRD analysis of TiWN films prepared at 150 W for different nitrogen concentrations is shown in Fig. 18. Features shown in Fig.18 include: 1 Phase evolution from $\alpha$ to $\beta$ when the nitrogen concentration was increased from 10% to 20%; 2 Peak broadening due to fine grains that were observed for all four peaks; and 3 Preferred orientations in the [110] planes for the $\alpha$-phase and [111] for the $\beta$-phase in all TiWN films were observed. The crystal structure

accompanying the change in lattice constant may also result in an increase of deposition rate if the structure changes from, for example, body centered cubic (B.C.C.) to F.C.C. For nitrogen-incorporated TiW films without preferred orientations, the density in atoms per cubic centimeter reduces from $6.338 \times 10^{22}$ to $5.10 \times 10^{22}$ when the crystal structure changes from B.C.C. to F.C.C. [64]. This results in a slight increase in thickness if the same amount of atoms arrive at the substrate surface. Therefore, some other factors which result in the decrease of the deposition rate associated with the nitrogen content need to be understood. First, an increase of the nitrogen partial pressure in an argon gas ambient with constant argon pressure will have an inevitable increase in the probability of interaction between these two respective gas species, hence, decelerating the velocity of argon ions which controls the sputtering rate. Second, a negative DC bias will attract argon ions; some of these argon ions might not be able to reach the target, but, instead, may hit the substrate. In RF sputtering deposition, the DC bias determines the intensity of the sputtering gas bombardment on the substrate surface during one half of the cycle and the deposition rate is known to decrease at higher bias voltage [65]. Thus, the lower rate at high nitrogen concentration can be explained since high nitrogen content results in high DC bias as can be seen in Table 3. The films were analyzed using X-ray Photoelectron Spectroscopy (XPS). All three TiWN films have similar XPS spectra as can be seen in Figs. 21 (a) and (b). From Fig. 21 (a), the lower line and upper line represent XPS spectrum for samples prepared at 150 W /-198 V DC bias that was not Ar ion beam etched and one that received 10 minutes of Ar ion beam etching, respectively.

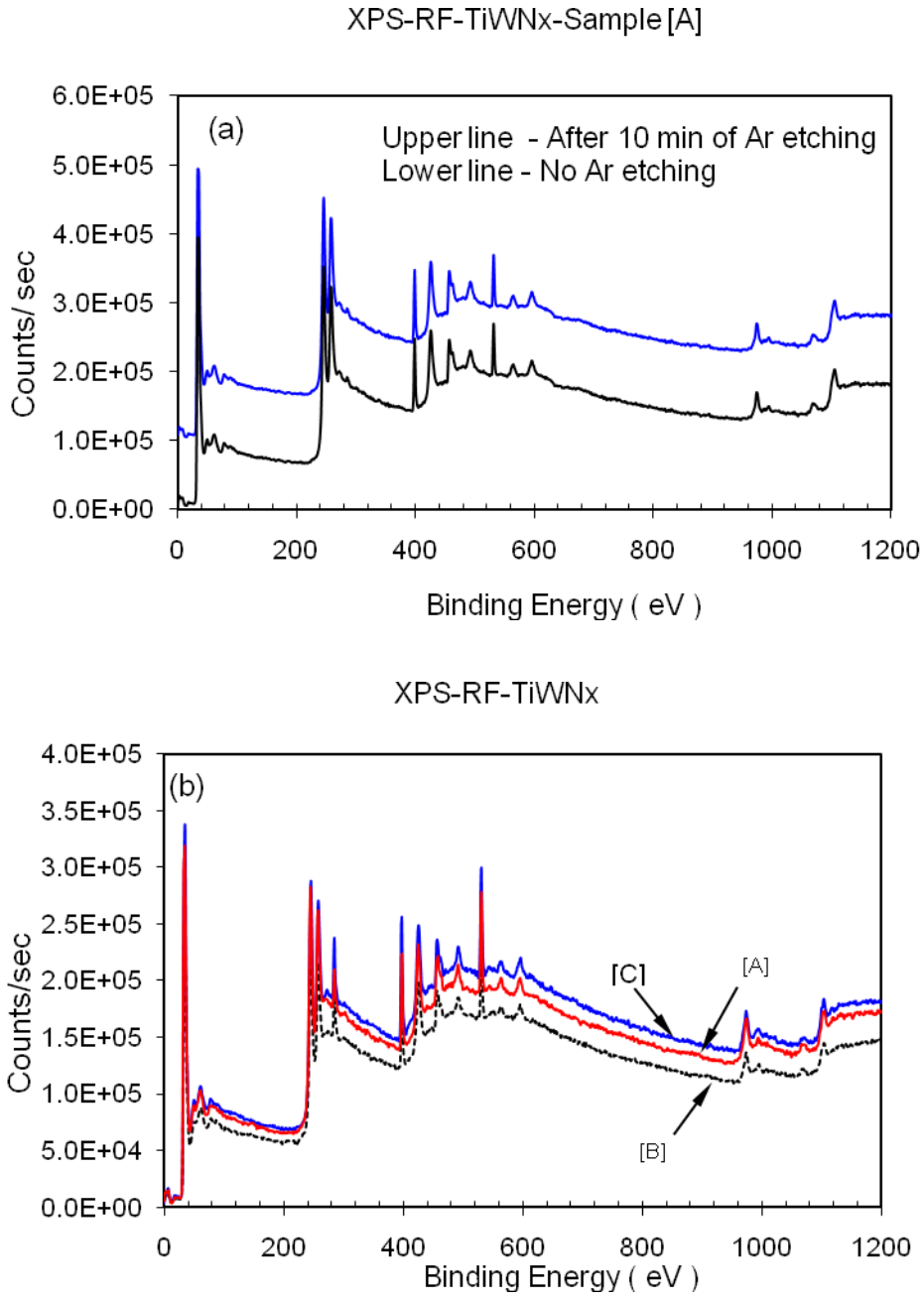



Fig. 21. XPS spectra for RF sputter deposited TiWN thin films prepared (a) at 150 W /-198 V DC bias [A] and (b) at 150 W/-198 V DC bias [A], at 150 W/-207 V DC bias [B], and at 150 W/-225 V DC bias [C].

The two curves are identical except for the difference in vertical shift, which is intentionally done for separating two curves. These two curves show the chemical states of each element on the surface and in the etched surface are the same. Figs. 22(a) and (b) show the XPS signals versus binding energy plots for Ti and W, respectively, in TiWN films. Ti appears as a nitride instead of an oxide, while W tends to be a pure form with a slight amount of oxygen and nitrogen binding. It will be shown in this dissertation that, because of this tiny amount of oxygen and nitrogen, the thermal stability of TiWN films is better than that of TiW films.

Using the XPS quantitative analysis of all monitored elements, together with the measured properties in Table 3, a relationship between chemical composition and nitrogen concentration for TiWN thin films prepared under various conditions is depicted in Fig. 23. The incorporation of nitrogen increases as the nitrogen concentration increases while the Ti/W ratio was found to be unchanged and independent of the amount of nitrogen incorporation. Oxygen in TiWN films could be from the exposure to air before being loaded into the XPS chamber. All spectra were taken on samples that first received a 10 min argon ion etching to remove the surface oxide. However, it was found that the oxygen level still was about 5% even after 20 min of etching in argon plasma. Thus, this percentage (5%) of oxygen is thought to be incorporated during the deposition. Such an increase in the nitrogen content of the thin films with respect to the nitrogen gas concentration during sputtering can be realized as a higher incorporation probability at high pressures compared to low pressures [65].

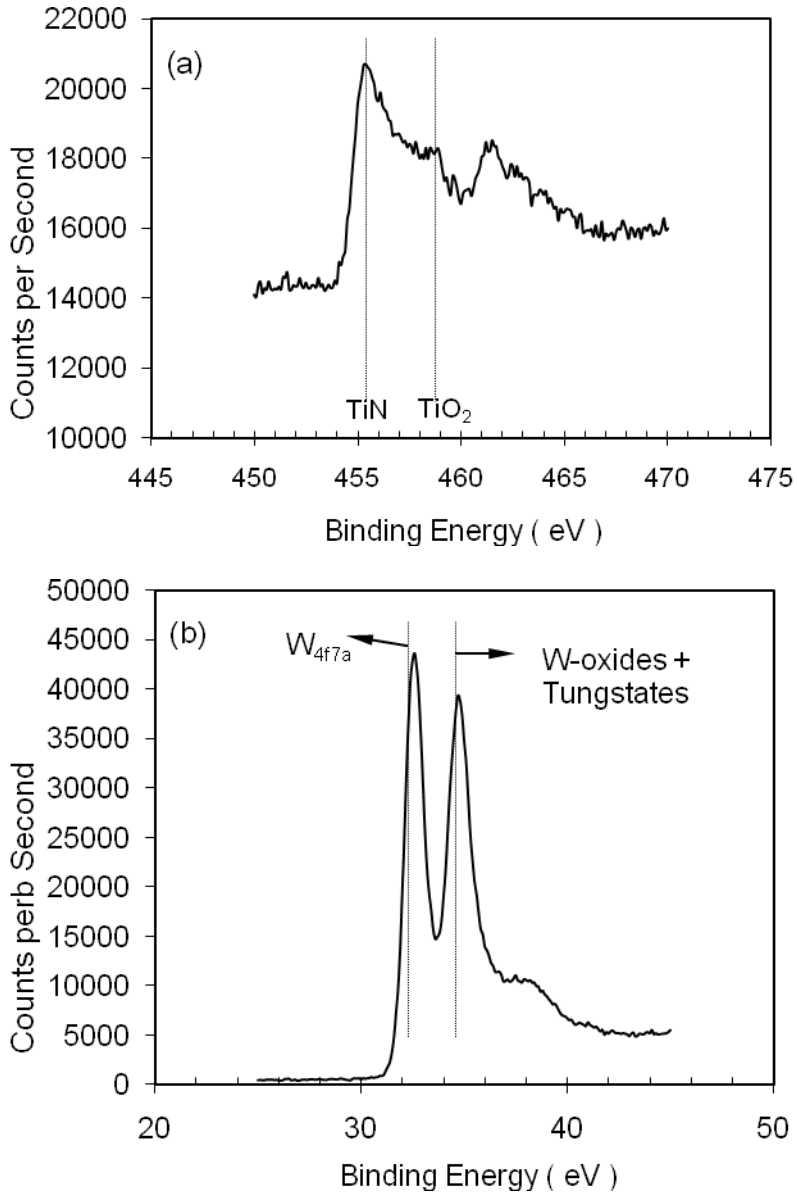



Fig. 22. XPS profiles of Ti and W in example sputtered TiWN films used in this dissertation. Ti appears to bind with nitrogen, while W binds to oxygen, as well as nitrogen, and forms tungsten oxides and tungsten nitrides, respectively.

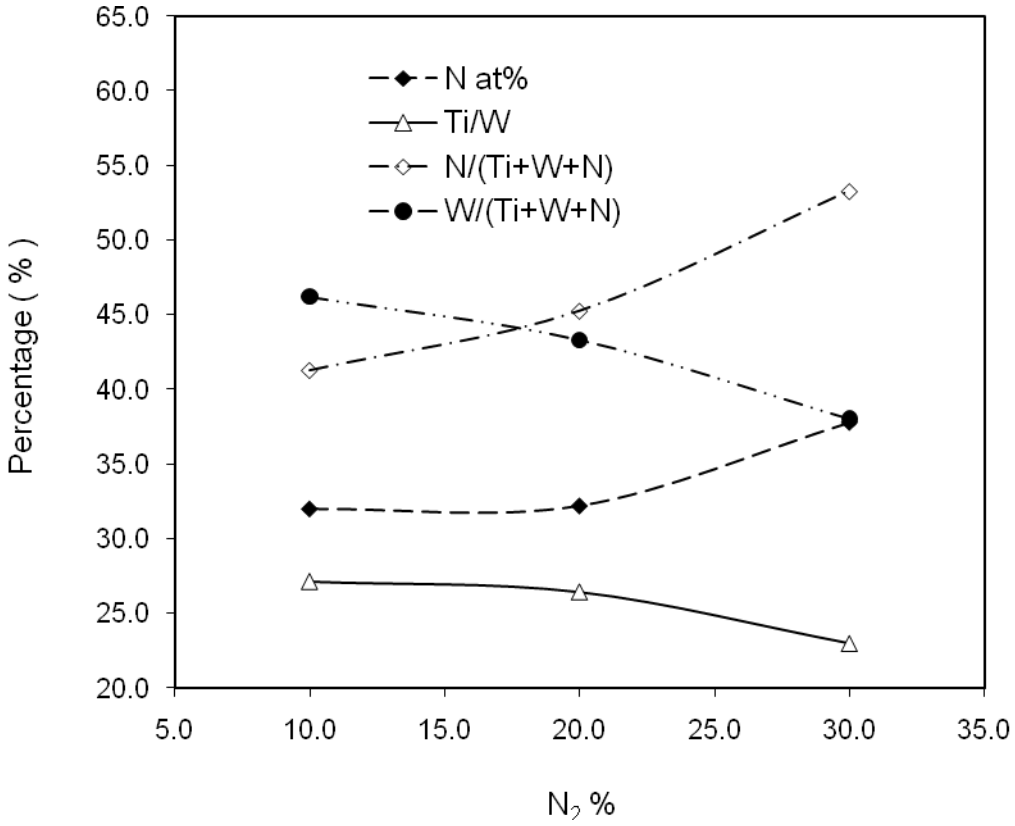



Fig. 23. Results of XPS analysis for RF-sputtered TiWN thin films.

The tungsten oxides degrade the quality of the thin films. Using low Ar sputtering pressure, both the sputtered atoms from the target and reflected gases are more energetic due to having a longer mean free path; hence, a reduced travel distance from target to substrate can further decrease the incorporation of nitrogen into TiW films [37,38] if a low nitrogen composition in the films is desired.

### 3.3.3 Modeling of intrinsic stress of TiWN on semiinsulating GaAs

The intrinsic stress for as-deposited TiWN films on semi-insulating GaAs was also studied in this dissertation. It should be pointed out that the stress calculated in this dissertation is actually the “stress change” before and after deposition. Film stress values were obtained through the equation [34]

$$\sigma = Ed^2\Delta(1/R)/6(1-\nu)t \qquad (11)$$

where $E$, $d$, $R$, $t$, and $v$ are the substrate’s Young’s modulus, thickness, radius of curvature, film thickness, and Poisson’s ratio, respectively [34,35]. Values used for the calculation are 75 GPa, 450 μm, and 0.3, for the GaAs substrate’s, Young’s modulus, thickness, and Poisson’s ratio, respectively. As mentioned before, the change $\Delta(1/R)$ in the radius of curvature of the GaAs bars (20mm x 10 mm x 0.45mm) from before to after deposition is used to calculate the change in stress. The thickness of each film, t, was obtained by measuring the deposition step in the film at an area of the GaAs substrate that was masked during deposition on the corresponding GaAs substrate using a Sloan Dektak II-a surface profiler. The stress for the sputtered TiWN films deposited directly onto GaAs substrates and on CuGe deposited on GaAs substrates with respect to the sputtering gas pressure is shown in Fig. 24 (a). For the entire range of gas pressure, from 3.6 mTorr to 10 mTorr, the as-deposited TiWN films on GaAs and on CuGe/GaAs were found to have compressive stress. The compressive stress was inversely proportional to the nitrogen pressure as seen in Fig. 24 (b).

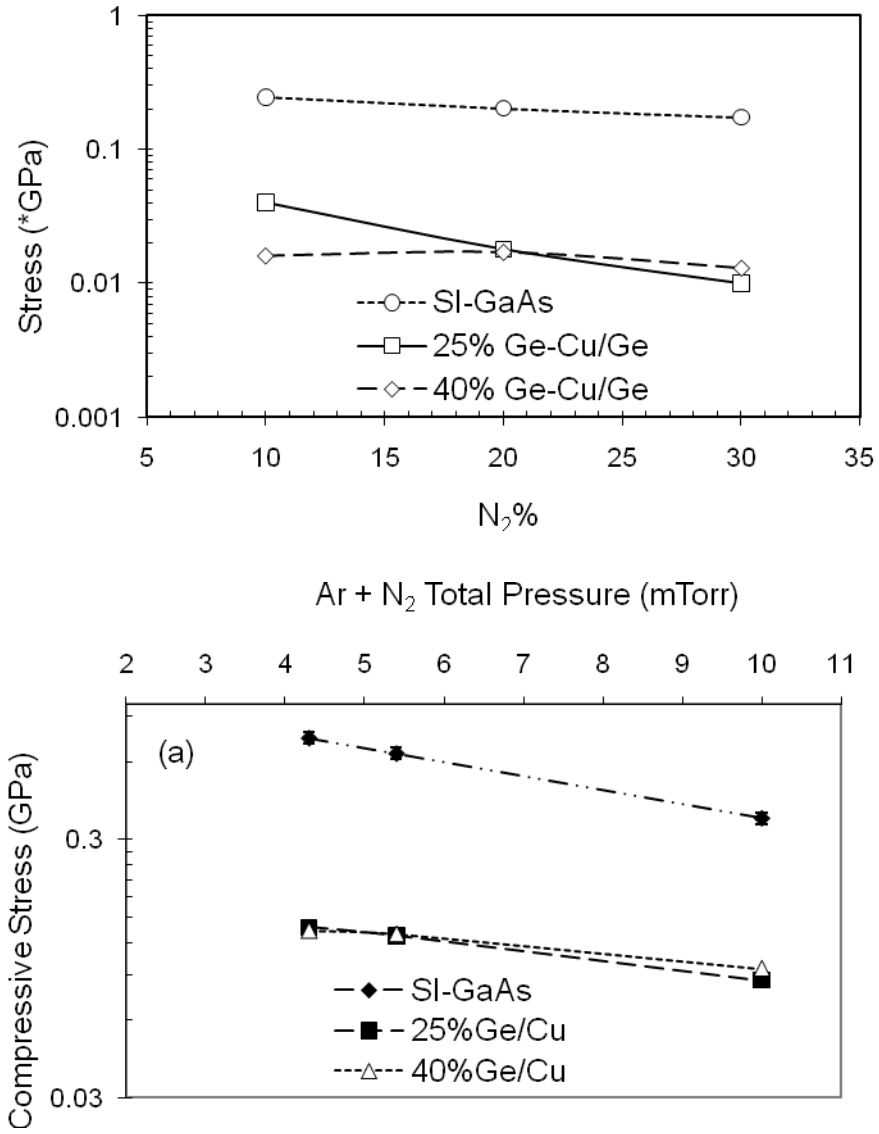



Fig. 24. Stress levels of RF-sputter deposited TiWN thin films as a function of (a) argon and nitrogen total pressure at a fixed value of argon pressure and (b) nitrogen percentage at a fixed Ar pressure of 3.6 mTorr on semi-insulating GaAs, 25%Ge-CuGe, and 40%Ge-CuGe samples.

The transition from compressive stress to tensile stress was estimated by extrapolating to zero stress assuming a linear relationship. This transition was found to be around 15 mTorr for TiWN on GaAs and 19 mTorr for TiWN on CuGe/GaAs. The tensile CuGe on GaAs was found to be tunable by adjusting the TiWN thickness and process parameters such as the nitrogen compositions and the gas flow rates. The importance of this tunability is to assure the proper stress on the film to prevent peeling or delaminating during thermal processes. For example, CuGe deposited on GaAs has tensile stress and the substrate will deform in a convex manner, indicating that the films are prone to peeling-off. The measured film stress is thought to also be associated with the grain size.

The microstructure of TiWN deposited on epi-ready GaAs substrates that were studied in this dissertation was found to be an intricate mixture of small crystallites, 30 nm to 41 nm in size, of β-W and nitrides, such as TiN, $W_2N$, and $Ti_2N$ [40,41]. Figs. 25(a)-(d) are typical AFM micrographs of TiWN on GaAs substrates obtained for this dissertation. Preliminary cross section TEM-results indicated that each column might consist of a single crystal of β-W matrix with nitride precipitates, which could be called a grain [41]. In this dissertation study, it was assumed that the microstructural features observed in AFM are grains.

A simple model, similar to a model used for stress changes during grain growth [39] could possibly explain this observation. If it is assumed that, for the same thickness, the same numbers of atoms are deposited on all samples and the smaller grained material will have a more compressive stress as the volume per atom in the grain boundary is greater than that in the lattice [39,41]. The stress in the film can be formulated as:

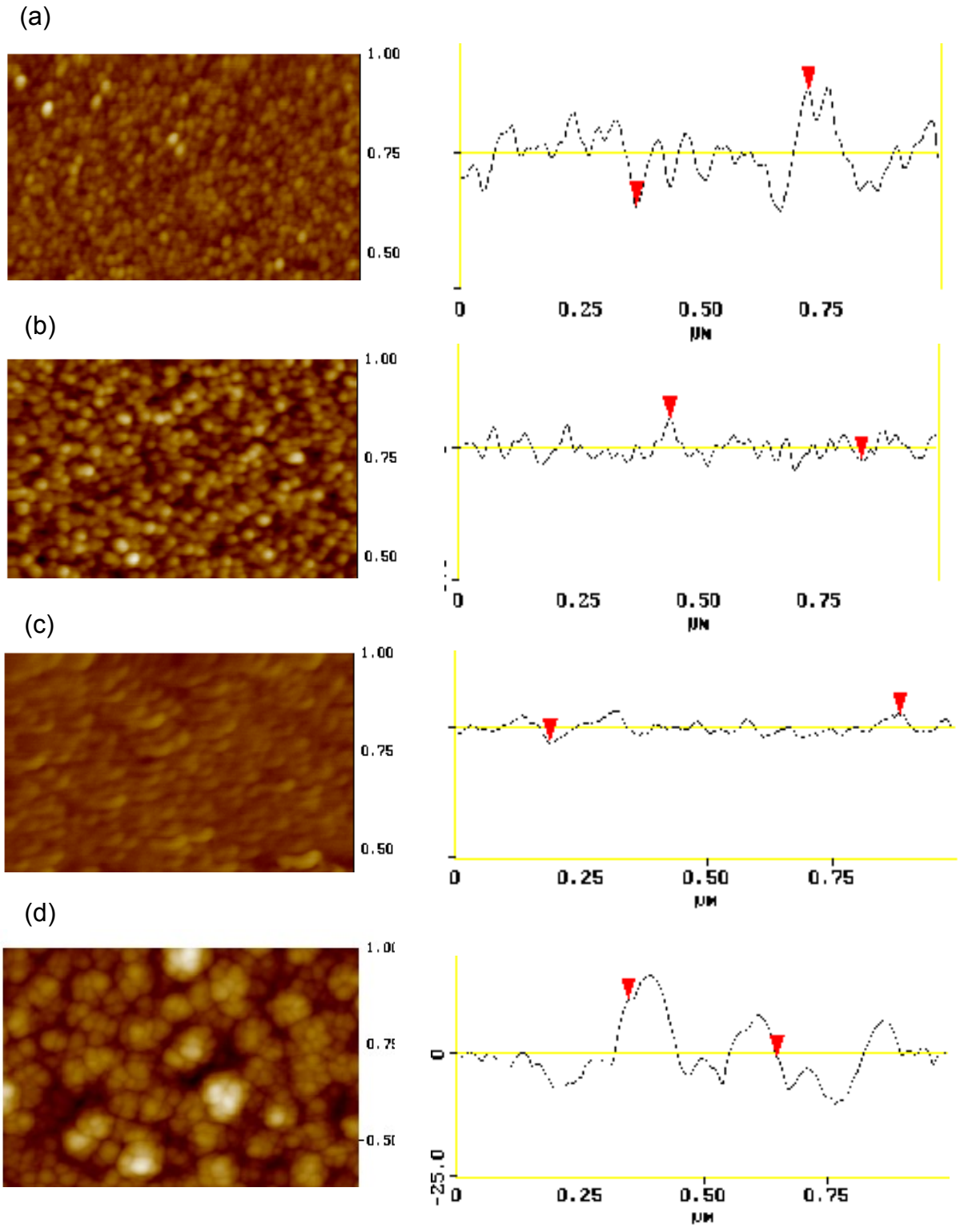



Fig. 25. AFM micrographs for RF-sputtered TiWN thin films deposited on semi-insulating GaAs [(a) – (c)] and CuGe (d) at power of 150 W and DC bias of (a) -198V, (b) -207V, (c) -225V, and (d) -198V, respectively. The cross section profiles for grain size analysis are also shown on the right hand side of images.

$$\sigma = \sigma_o + B\varepsilon \qquad (12)$$

with $\sigma_o$ the deposition stress for a single crystal, $B = E/(1-v)$ the biaxial modulus, $E$ the Young's modulus, $v$ the Poisson's ratio and $\varepsilon$ the dilatation strain in any in-plane direction due to the excess volume of the grain boundaries. For columnar grains $\varepsilon$ is equal to [39]:

$$\varepsilon = -e/2 = -(4\Delta a/d)*1/2 = -2\Delta a/d \qquad (13)$$

with $e$ is the volumetric transformation strain associated with the creation of grain boundaries, $\Delta a$ the excess volume per unit area of grain boundary, which is expected to be on the order of the atomic diameter, and close to the grain size.

Fig. 26 shows the stress in the TiWN layers as a function of the inverse of the TiWN grain size. The slope of the stress versus the inverse of the grain size yields the value of $-2B\Delta a$. Assigning a value of 75 GPa for the biaxial modulus, a slope of $-3\times10^{-8}$ GPa*m results in a $\Delta a$ value of 2Å, which is somewhat less than half the atomic diameter of TiWN. The stress for a single crystal from the extrapolated stress versus $1/d$ yields a tensile stress of 0.17 GPa. It is possible, because the larger grain size would have a smaller $\Delta a$ value, that this would result in less excess grain boundary volume and a more tensile stress. Alternately, the TiWN layers can have different microstructures apart from the grain size resulting in different stresses in the thin films.

If the deposition stresses are rather large, the possibility of severe plastic deformation should be considered. The Hall-Petch relation [68,69] predicts a linear decrease of yield stress with the inverse of the square root of the grain size. Although $\sigma$ versus $d^{-1/2}$ yields a better linear fit than $\sigma$ versus 1/d, the

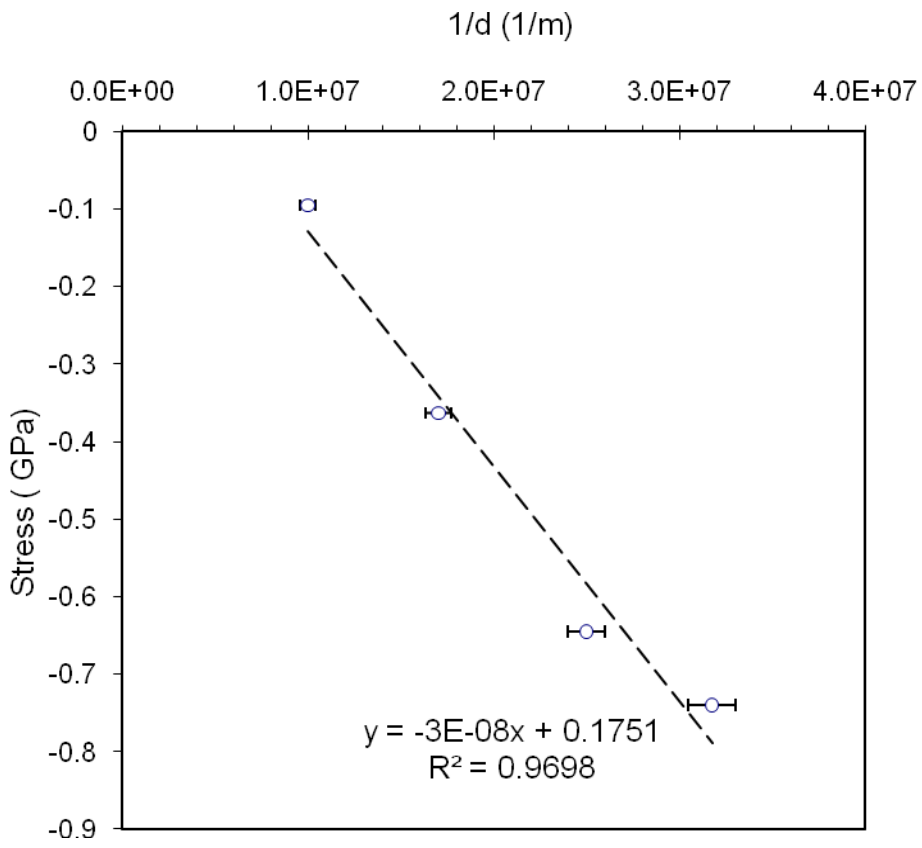



Fig. 26. Film stress as a function of grain size for RF-sputtered TiWN thin films.

extrapolated compressive yield stress for a single crystal from this fit is a tensile stress of about 0.17 GPa which is similar to the result to the stress obtained from the extrapolated stress versus $1/d$ method. The temperature during the sputtering must be high to explain this discrepancy in terms of thermal stress as the change in stress with temperature for TiWN on GaAs is about 1.3 MPa/°C [38].

## 3.4 Thermal stability of CuGe-based ohmic contacts with diffusion barriers

Unprotected $Cu_3Ge$ contacts become insulating after a long time exposure to untreated air, implying that special protection layer(s) must be used if Cu-Ge based materials are chosen for use as contacts to III-V semicondutor materials. In addition, the I-V characteristics changed rapidly from linear (ohmic) to Schottky behavior as temperature increased from room temperature to about 300°C for unprotected $Cu_3Ge$. Therefore, potential thermal diffusion barriers were investigated in this dissertation as discussed in the following sections.

### 3.4.1 With TiW as the diffusion barrier

Figs. 27 (a) and (b) are AFM microphotographs that show the morphology of a Cu/Ge/GaAs sample covered with a TiW layer after annealing this structure at 400°C for 30 min. It should be noted that the color of TiW changed from yellow to milky white after annealing indicating the poor protection properties and capabilities of TiW as a protection barrier layer for CuGe. With a TiW layer, hillocks were found almost everywhere on the sample surface. Specific contact resistance for a TiW cover layer on CuGe to n-type GaAs was found to increase from $1.5x10^{-6}$ $\Omega cm^2$ to ~$10^{-3}$ $\Omega cm^2$ after 14-hr of annealing at 400°C as can be seen in Fig. 28. Therefore, it can be concluded that TiW failed to protect CuGe-based ohmic contacts to n-type GaAs at 400°C. A SIMS depth profile, shown in Fig. 29, for this sample demonstrates a severe intermixing between the contact material and the TiW protection/diffusion layer which resulted in both poor morphology and degraded contact resistance.

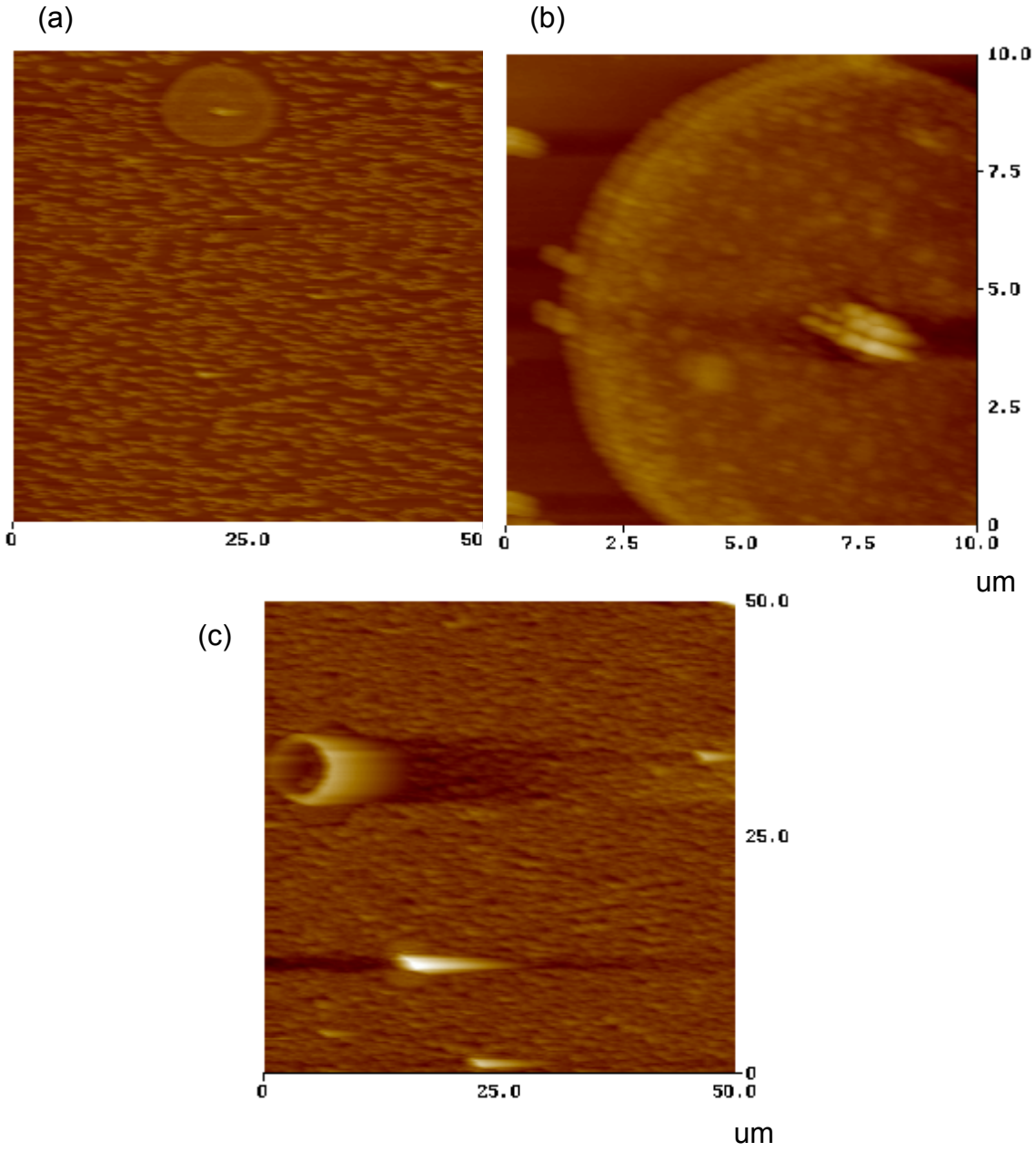



Fig. 27. AFM micrographs showing morphologies of TiW-covered Cu/Ge contacts to n-type GaAs after annealing at 400°C for 30 min: (a) “Hillock” and clusters are seen in the AFM micrographs, (b) an enlarged AFM micrograph near a “Hillock,” and (c) perturbations and “Hillock” can be clearly seen.

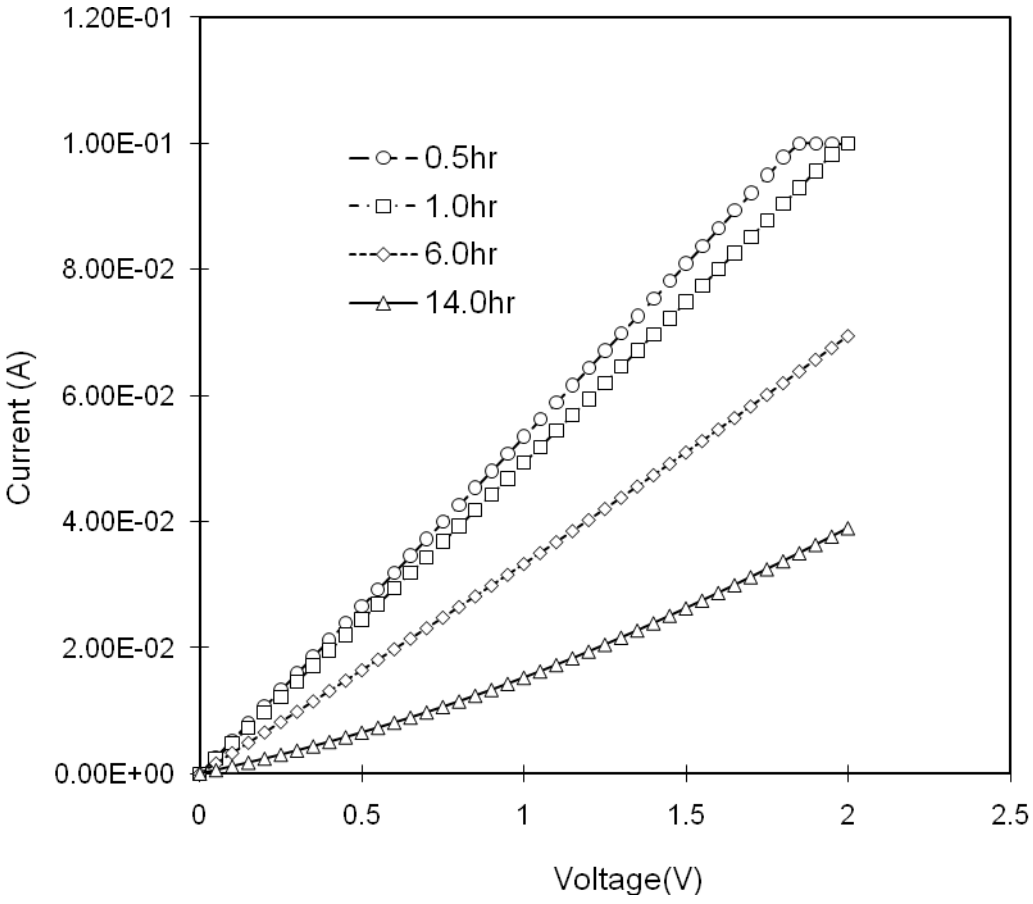



Fig. 28. Current-voltage characteristics after annealed at 400°C for TiW-covered $Cu_3Ge$ ohmic contacts to n-type GaAs.

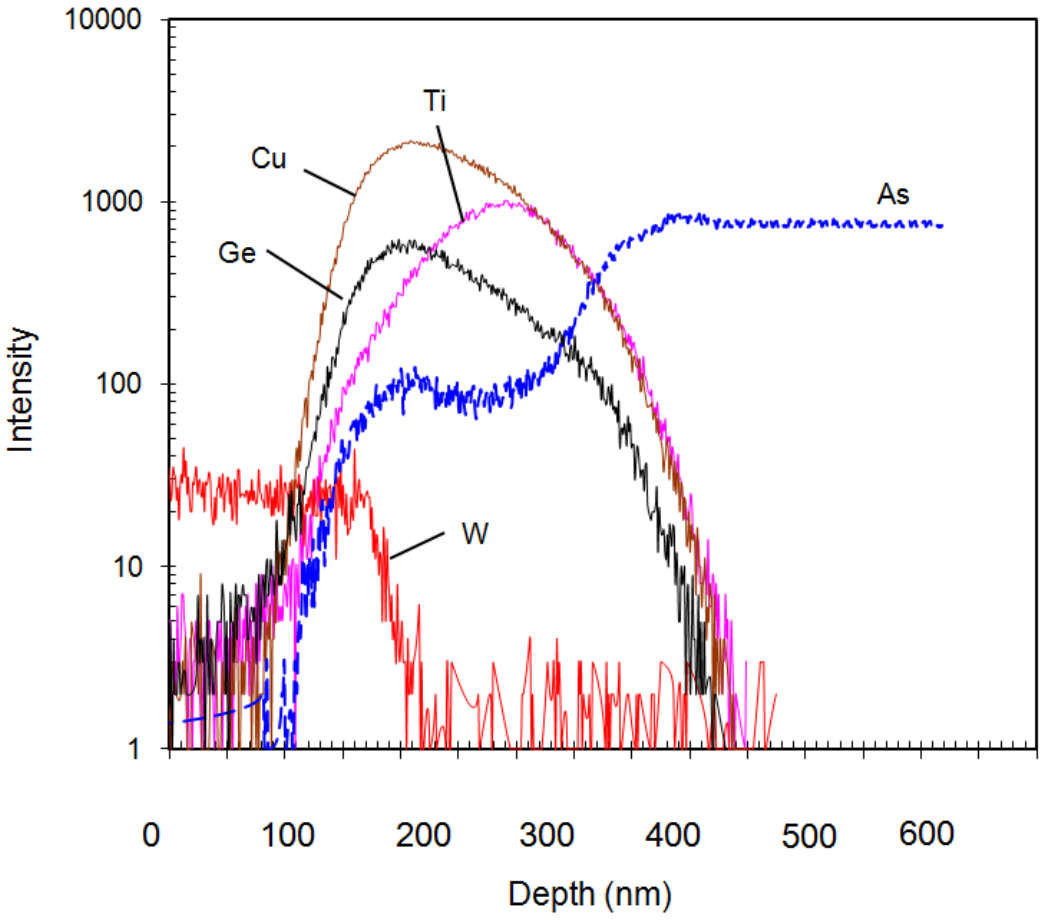



Fig. 29. TOF-SIMS depth profile for CuGe-based ohmic contacts covered with TiW and Au layers after annealing at 400°C for 30 min.

In this dissertation work, it was routinely observed that chunks of atoms clustered on the surface of the Cu and Ge layers having a size of a few micrometers formed if the CuGe films were evaporated at a rate higher than 5Å/sec. These types of defects should be avoided in order for the diffusion barrier layers to completely cover the areas where the protection is needed.

### 3.4.2 With TiWN as the diffusion barrier

As has been shown, typical grain sizes of RF-sputtered TiWN films range from 30 to 60 nm. All TiWN films prepared for this annealing test as part of this dissertation were targeted to be between 150 nm to 200 nm in thickness to avoid possible discontinuities in the film due to the insufficient film thickness. The same contact scheme approach in Section 3.4.1 that was used for TiW was also used with TiWN replacing TiW as a possible diffusion barrier. After a 400°C/30 min annealing in nitrogen atmosphere there was no observed change in surface morphology, as can be seen in Fig. 30 (a), or an observed change in the contact resistance compared to an as-annealed CuGe contact with a SiN passivation layer under the same annealing conditions. For this contact scheme, to simplify processing steps, a diffusion barrier layer should probably be deposited with the photoresist left on and used for masking and processing of the ohmic contacts; however, such a barrier layer needs to be able to sustain the post thermal treatment, which is typically 400°C for this dissertation work, at which the lowest contact resistance of CuGe contact was obtained. The SIMS depth profiles for TiWN covered CuGe contacts to n-type GaAs before and after annealing are shown in Figs. 31 (a) and In Fig. 31(b). Only the redistribution of Ge and Cu com-

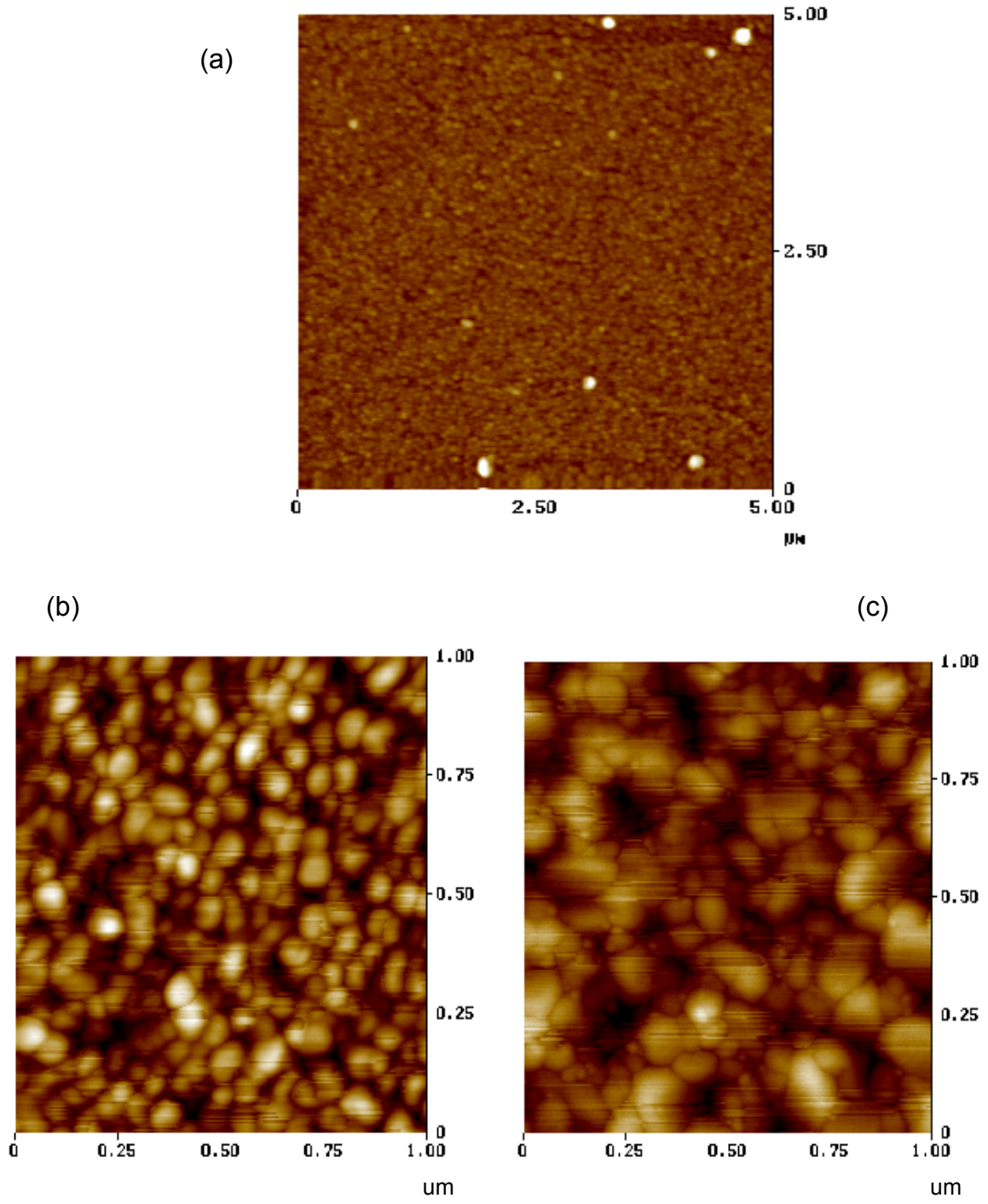



Fig. 30 AFM micrograph for (a) RF sputtered TiWN covered CuGe-based contacts on n-type GaAs and (b) Au/TiWN covered CuGe-based contacts on n-type GaAs after an annealing at 400°C for 30 min, respectively. Prolonged annealing times caused the coarsening of the polycrystalline gold overlayer as shown in (c) where the same sample was annealed at 400°C for 2 hrs.

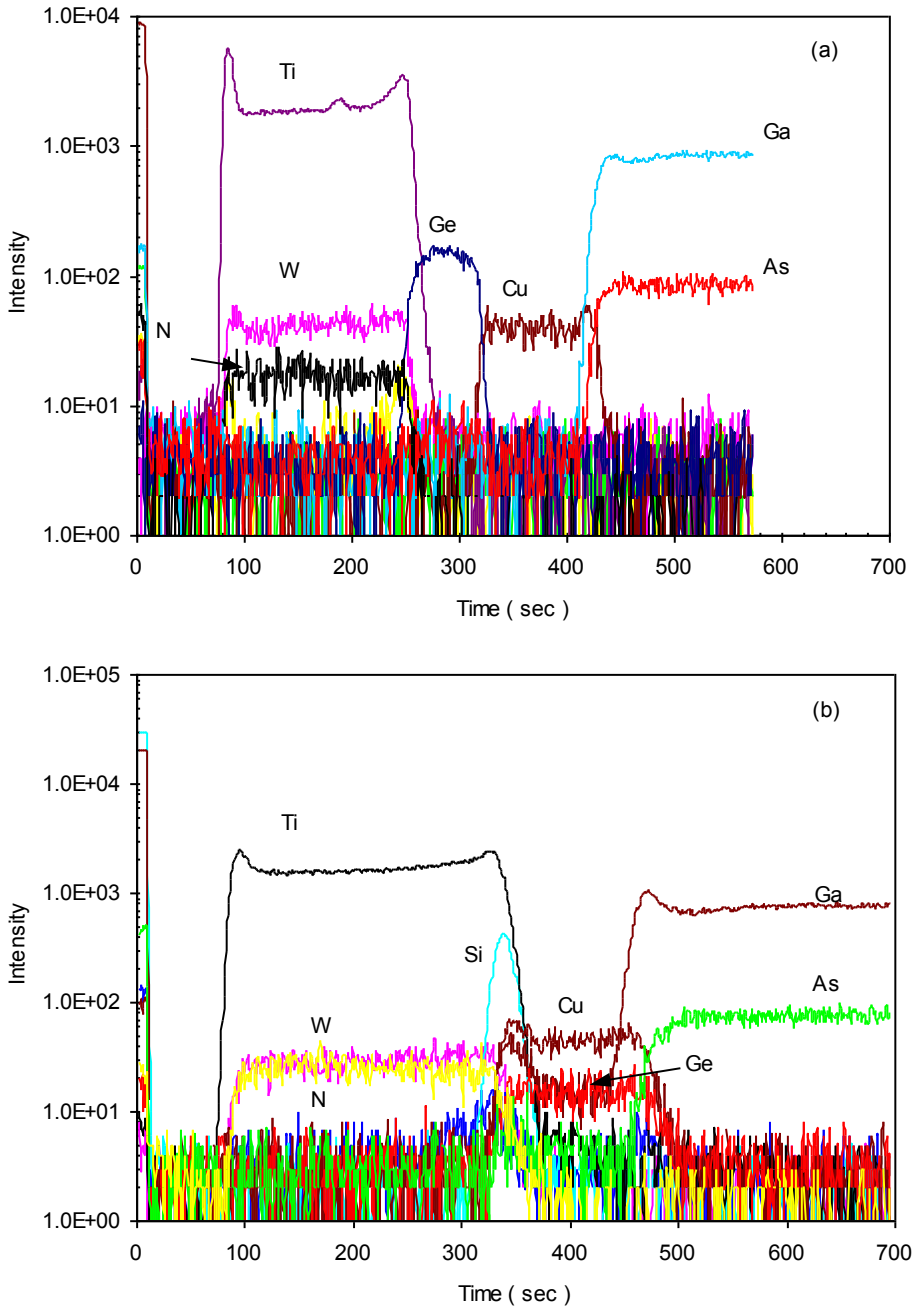



Fig. 31. TOF-SIMS profiles for Au/TiWN - protected CuGe-based ohmic contacts to n-type GaAs (a) as – deposited and (b) after annealing at 400°C for 14 hrs.

positions was observed. The relatively unchanged W and Ti-composition profile in the TiWN layer strongly indicates that both titanium and tungsten are bonded to nitrogen or oxygen which might be the responsible mechanism for the improved properties in terms of less intermixing with Cu and Ge. TiWN has been studied and shown to have a columnar structure with nitride precipitates “stuffed” within the grain [33]. Due to such closely spaced precipitates, the diffusion of Cu and Ge can be effectively blocked if the precipitates are separated by a distance that is less than the atomic diameter of Cu and Ge, which is 3.615 Å and 5.658 Å, respectively.

### 3.4.2 With Au overlayer and TiWN as a diffusion barrier

It is of great importance to have an Au over layer on TiWN covered CuGe ohmic contacts to n-type GaAs because of the concern and need for wire bonding the ohmic contacts in order to package the final structures, devices, and circuits and be able to make electrical contact to the structures, devices and circuits. The practical concern remains the same to keep the process as simple as possible when the Au layer is added. A 2000 Å-thick Au layer was sputtered on top of TiWN prior to the annealing. Samples received the same heat treatment protocol as that for the previous TiWN covered samples discussed above. It was found that there was no noticeable change in surface color or morphology under optical microscope and AFM examinations (see Figs. 30(b) and (c)) Only the coarsening of Au layer was observed by AFM. SIMS depth profiling of this sample is shown in Fig. 31 in which it can be seen that Au was contained (and is away from the CuGe contact region) and only penetrated about 200 Å during the

14-hr annealing process. This lack of significant interaction can be attributed to the “stuffed” TiWN barrier layer which effectively blocks the out-diffusion of Cu to the surface. As long as there is no reaction between Au and TiWN, TiWN is a capable diffusion blocker for Au because Au has an atomic diameter of 4.07 Å, just slightly larger than that for Cu.

A contact configuration as shown in Fig. 32 (a) will suffer from the oxidation of the contact through lateral diffusion and also potentially the decomposition of GaAs at high temperatures. A better way to do the high temperature test is to cover and mask the nonalloyed area with dielectric materials, such as silicon dioxide ($SiO_2$), silicon nitride ($Si_3N_4$), and aluminum oxide ($Al_2O_3$) etc, as shown in Fig. 32 (b).

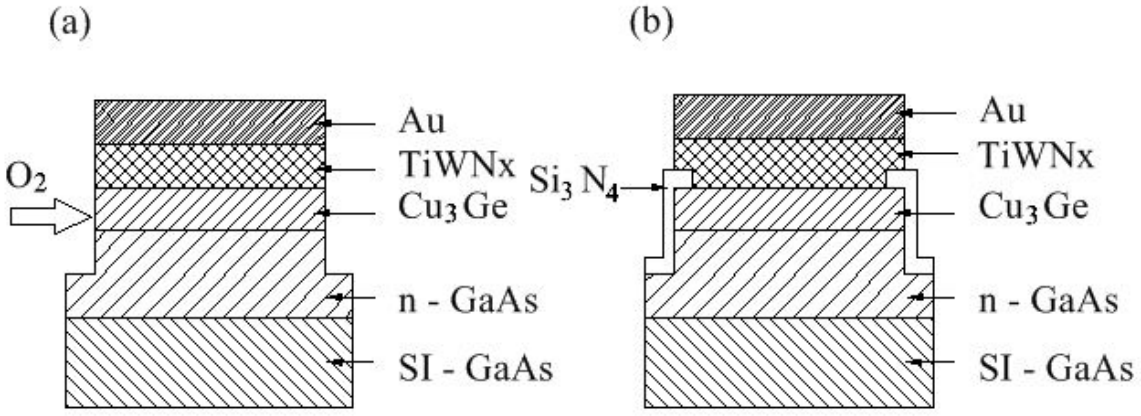



Fig. 32. Potential structural and processing configurations of the n-type ohmic contacts to be used on the devices for high-temperature testing. In (a), oxygen will penetrate laterally and cause the deterioration of contact resistance for $Cu_3Ge$ to n-type GaAs, while in (b), the oxidation was prohibited by a thin PECVD deposited $Si_3N_4$ layer.

The average specific contact resistance as a function of the annealing time at various temperatures is shown in Fig. 33. For temperatures below 400°C, the specific contact resistance of CuGe to n-type GaAs with a doping concentration of $5x10^{17}$ $cm^{-3}$ remained unchanged after a 150 hrs soaking at a temperature of 350°C on top of a thermal hot temperature chuck under untreated air ambient environment with an Au/TiWN protection barrier and a cover/mask layer. At an aging temperature of 400°C, the same temperature as for the alloying process, a very slow degradation in specific contact resistance was observed for $Cu_3Ge$ ohmic contacts to n-type GaAs. Since no phase transformation was revealed by X-ray analysis for the samples which had undergone the aging test at 400ºC for 150 hrs, a possible mechanism that accounts for the SCR degradation was that Cu diffused into GaAs and created a highly compensated layer which is less conductive than $Cu_3Ge$. The degradation rate was measured as $0.05 \pm 0.01x10^{-6}$ $\Omega cm^2$/hr at 400°C and close to being proportional to $t^{1/2}$. The increase in specific contact resistance after 2000 hrs of operation should be $1\ x10^{-4}$ $\Omega cm^2$. This increase in specific contact resistance is equivalent to an increase of 1 Ω in the source resistance for contacts having dimensions of 100 μm x 100 μm.

This low degradation rate in contact resistance has a relationship with respect to the diffusion coefficient of Cu and Ge from the $Cu_3Ge$ to the GaAs. The interdiffusion coefficient of Cu and Ge can be extracted from SIMS depth profiles using the Boltzmann-Matano method [67]. The interdiffusion coefficients of Cu and Ge in GaAs at 400°C were calculated to be $5x10^{-15}$ $cm^2$/sec and $1.55x10^{-14}$ $cm^2$/sec, respectively. Adding Cu into Ge was found to enhance the

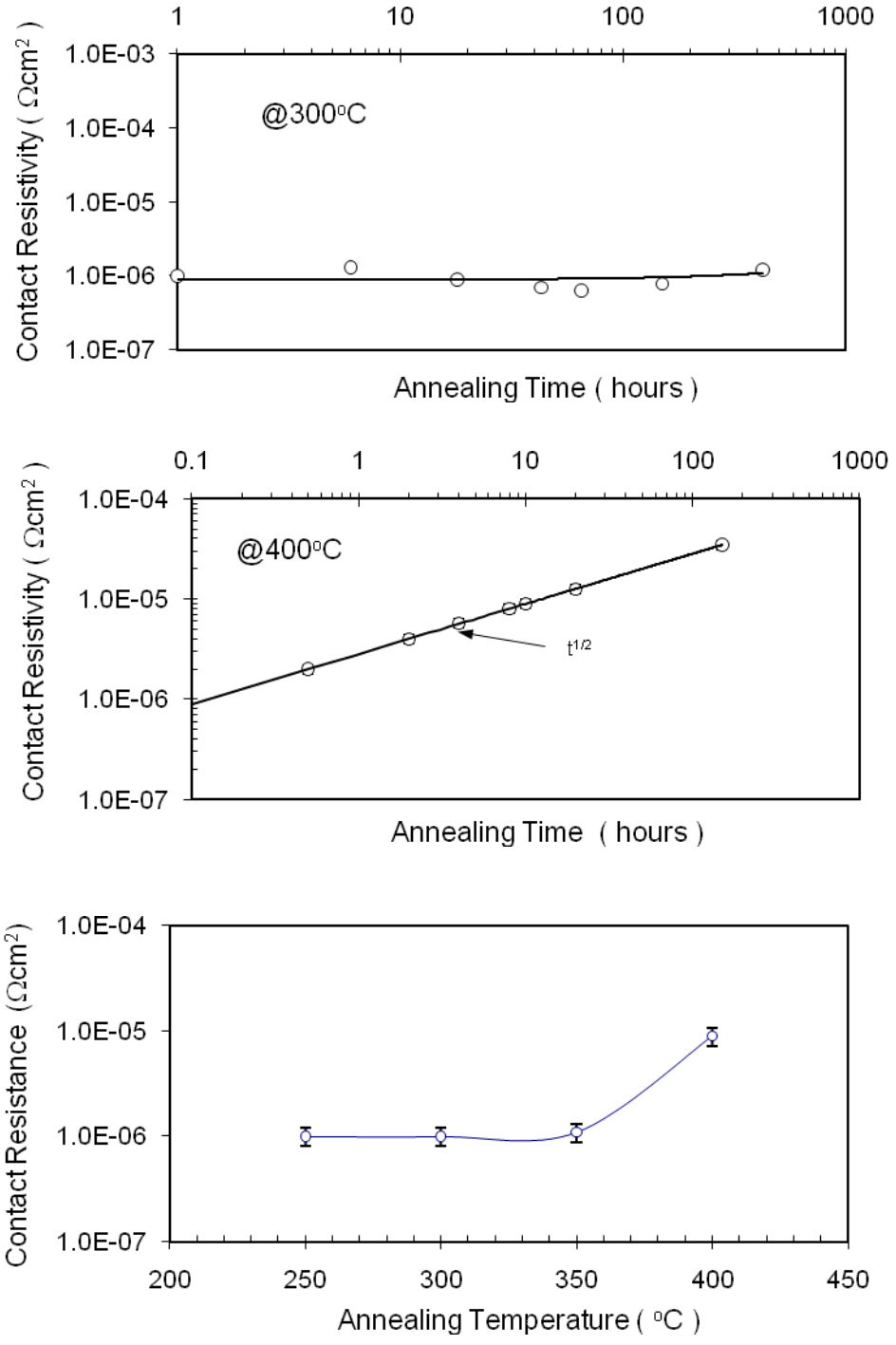



Fig. 33. Thermal stability of $Cu_3Ge$ with $TiWN_x$/Au capping layers at (a) 300°C, (b) 400°C, and (c) temperatures between 250°C and 400°C.

diffusion of Ge into GaAs based on a comparison of listed value of the diffusion coefficient for Ge at 400°C ($6x10^{-21}$ $cm^2$/sec) [66]. This enhanced diffusion behavior of Ge in the presence of Cu gives very strong evidence that the most probable mechanism for ohmic contact creation is the formation of highly Ge-doped $n^+$GaAs layer at the interface as stated earlier in this dissertation.

The Ge appears to be the faster species at 400°C which aids in preventing the compensation effect of Cu, as Cu is a double-acceptor to GaAs, from occurring. This apparent situation might explain why there is a wide range of annealing times for which this contact scheme maintained relatively low contact resistance to n-type GaAs. As Ge diffuses away from the heavily doped region and further into the GaAs, an increase in specific contact resistance will be observed because the tunneling probability decreases as the doping concentration is lowered and the effective tunneling distance is increased. The thermal stability of CuGe-based ohmic contacts to n-GaAs is controlled by the enhanced Ge diffusion due to the presence of Cu in the films.

The TiWN barrier and Au overlayer scheme was applied to the ternary alloy ohmic contacts InCuGe and NiCuGe. Aging tests at 400°C resulted in a linear relationship between specific contact resistance and aging time for both of these ternary alloys to n-type GaAs. The diffusion of Ge in these systems is thought not to be enhanced by the addition of In and Ni [6-9]. For either In or Ni to form the respective ternary CuGe ohmic contacts, the addition of one of these elements may result in phase evolution or reaction products that contribute to such a high degradation rate.

## 3.5 Conclusion

In conclusion, CuGe-based ohmic contacts deposited under appropriate deposition procedures and precise composition control have low resistivity competitive to that of AuGeNi contacts to n-type GaAs. The RF-sputtered TiWN thin films with certain levels of nitrogen incorporation are effective diffusion barriers preventing intermixing between Au and $Cu_3Ge$. The degradation rate of specific contact resistance of $Cu_3Ge$ to n-type GaAs with a TiWN barrier and Au overlayer is close to $t^{1/2}$, where t is the time measured in seconds, at 400°C and negligible at temperatures lower than 350°C.

The properties of $Cu_3Ge$ ohmic contacts to n-type GaAs have demonstrated that these contacts can be suitable candidates as ohmic contacts in GaAs-based electronic devices for high-frequency, high-power, and high-temperature applications.

## 3.6 References

1. N. Braslau, J. B. Gunn, and J. L. Staples, Solid State Electron. 10 (1967) 38.

2. T. S. Kuan, P. E. Batson, T. N. Jackson, H. Rupprecht, and E. L. Wilkie, J. Appl. Phys. 54(12) (1983) 6952.

3. A. Iliadis and K. E. Singer, Solid State Commun. 49(1) (1984) 99.

4. Y. C. Shih, M. Murakami, E. L. Wilkie, and A. C. Callegari, J. Appl. Phys. 62(2) (1987) 582.

5. R J. Del Alamo, J. A., and T. Mizutani, Solid State Electron. 31 (1988) 1635.

6. M. Murakai, W. H. Price, J. H. Greiner, J. D. Feder, and C. C. Park, J. Appl. Phys. 65(9) (1989) 3546.

7. M. Murakami, H. J. Kim. Y. C. Shih, AW. H. Price, and C. C. Park, Appl. Surf. Sci. 41/42 (1989) 195.

8. M. Murakami, Mater. Sci. Rep. 5 (1990) 273.

9. M. C. Hugon, B. Agius, F. Varnicere, C. Dubon-Chevallier, J. F. Bresse, and M. Froment, Appl. Phys. Lett. 58(24) (1991) 2773.

10. M. C. Hugon, B. Agius, F. Varnicere, and M. Froment, J. Appl. Phys. 72(8) (1992) 3570.

11. M. Murakami, W. H.Price, M. Norcott, and P. E. Hallali, J. Appl. Phys. 68(5) (1990) 2648.

12. B. Kovács, L. Dávid, Zs. Kincses, I. Mojzes, B. Pécz, Vo Van Tuyen, Gy . Vincze, L. Dobos, Proc. of NATO Advanced Res. Workshop on Multichip Modules with Integrated Sensors ed. by W. K. Jones and G. Harsányi, Kluwer Academic Publishers, Dordrecht, Netherland,1996, pp. 289-300.

13. L. Dávid, B. Kovács, I. Mojzes, B. Pécz, J. Lábár and L. Dobos, In Extended Abstracts of JVC-7 (7th Joint Vacuum Conference of Hungary, Austria, Croatia and Slovenia) ed. by S. Bohátka et al., Debrecen, Hungary, 1997, pp. 255-256.

14. M. O. Aboelfotoh, C. L. Lin, and J. M. Woodall, Appl. Phys. Lett. 65 (1994) p. 3245.

15. S. Oktyabrsky, M. O. Aboelfotoh, and J. M. Woodall, J. Electron. Mater. 25(11) (1996) 1662.

16. P. Nath, K. L. Chopra, Thin Solid Films 58(2) (1979) 339.

17. S. Oktyabrsky, M. O. Aboelfotoh, and J. Narayan, J. Electron. Mater. 25(11) (1996).1673.

18. M. E. Lin, Z. Ma, F. Y. Huang, Z. F. Fang, L. H. Allen, and H. Morkoc, Appl. Phys. Lett. 64 (1994) 1003.

19. E. D. Marshall, W. X. Che, C. S. Wu, S. S. Lau, and T. F. Kuech, Appl. Phys. Lett. 47 (1985) 298.

20. E. D. Marshall, S. S. Lau, C. J. Palmstrom, T. Sands, C. L. Schwartz, S. A. Schwartz, J. P. Harbison, and L. T. Florez, Mater. Res. Soc, Symp. Proc. 148 (1989) 163.

21. C. J. Palmstrom, S. A. Schwartz, E. Yablonovitch, J. P.Harbison, C. L. Schwartz, L. T. Florez, T. J. Gmitter, E. D. Marshall, and S. S. Lau, J. Appl. Phys. 67 (1990) 334.

22. L. C. Wang, X. Z. Wang, S. S. Lau, T. Sands, W. K. Chan, and T. F. Kuech, Appl. Phys. Lett. 56 (1990) 2129.

23. C. C. Han, X. Z. Wang, l. C. Wang, E. D. Marshall, S. S. Lau, S. A. Schwartz, C. J. Palmstrom, J. P. Harbison, L. T. Florez, R. M. Potemski, M. Tischler, and T. F. Kuech, J. Appl. Phys. 68 (1990) 5714.

24. J. S. Kwak, H. N. Kim, H. K. Baik, J. L. Lee, D. W. Shin, C. G. Park, H. Kim, and K. E. Pyun, J. Appl. Phys. 80(7) (1996) 3904.

25. N. Braslau, Interfaces and Contacts, Mater. Res. Soc. Symp. Proc. 18 (1983) 393.

26. F. Lonnum and J. S. Johannessen, Electron. Lett. 22 (1986) 632.

27. J. Linhard, M. Scharff, and Schiott, Mat. Frs. Medd. Dan. Vidensk. Selsk, 33 (1963) 1.

28. Z. Wang, G. Ramanath, L. H. Allen, and A. Rockett, J. Appl. Phys. 82(7) (1997) 3281.

29. D. R. Poirier and G. H. Geiger, Transport Phenomena in Metallurgy, Addison-Wesley Pub. Co. London, 1982, p. 482.

30. J. E. Harper, J. Cuomo, R. J. Gambino, and H. R. Kaufman, Nucl. Instr. and Meth. In Phys. Res. B 7/8 (1985) 886.

31. H. Windischmann, J. Appl. Phys. 62 (1987) 1800.

32. B. Window, F. Sharples, and N. Savvides, J. Vac. Sci. Technol. A, 6 (1988) 2333.

33. A. Witvrouw, W. De Bosscher, B. Deweerdt, R. Verbeeck, F. Loosen, Ph. Roussel, and K. Maex, Mat. Res. Soc. Symp. 308 (1993) 51.

34. S. M. Rossnagel, P. Gilstrap, and R. Rujkorakarn, J. Vac. Sci. Technol. 21 (1982) 1045.

35. P. A. Flinn, D. S. Gardner, and W. D. Nix, IEEE Trans. on Electron. Devices ED-34 (1987) 689.

36. Iton Wang, Mat. Res. Soc. Symp. Proc. 130 (1988) 341.

37. J. E. Baker, R. J. Blattner, S. Nadel, and C. A. Evans. Jr., Thin Solid Films 69 (1980) 53.

38. R. S. Nowicki, J. M. Harris, M. A. Nicolet, and I. V. Mitchell, Thin Solid Films 53 (1978) 195.

39. M. F. Doemer and W. D. Nix, CRC Critical Review in Solid-State and Materials Science 14 (1988) 225.

40. A. G. Dirks, R. A. M. Wolters, and A. J. Neilissen, Thin Solid Films 193/194 (1990) 201.

41. A. G. Dirks, R. A. M. Wolters, and A. E. M. De Veirman, Mater. Res. Soc. Symp. Proc. 260 (1992) 787.

42. M. Werner, R. Job, A. denisenko, A. Zaitsev, W. R. Fahrner, C. Johnson, P. R. Chalker, and I. M. Buckley-Golder, Diamon and Related Materials, 5(6-8) (1996) 723.

43. D. G.Teer and K. C. Laing, CEP Consultants Ltd. Edingburgh, UK, 1991, p. 202.

44. T. Fukada, M. Hasegawa, T. Mori, Y. Toyoda, and T. Mikami, J. of The Vacuum Society of Japan, 38(11) (1995) p. 955.

45. T. Hauzer. T. Trinh, D. B. Lewis, J. S. Brooks, and W. D. Munz, Surf. and Coat. Tech. 76(1-3) (1995) 159.

46. Kun-Chuan Lin, Edward Y. Chang, Sheng-Ping Wang, Yeong-Lin Lai and Chun-Yen Chang, Jpn. J. Appl. Phys. 33(8A) (1994) 4546.

47. T. Hurkmans, T. Trinh, D. B. Lewis, J. S. Brooks, and T. Mikami, Surface and Coating Technology 76(1-3) (1995) 159.

48. S. M. Sze, Physics of Semiconductor Devices, 2nd ed., Wiley, New York, 1981.

49. R. I. Jaffee and B. W.Gonser, Trans. Amer. Inst. Min. Met. Eng. 166 (1946) 436.

50. H. W. King, T. B. Massalski, and L. L. Issacs, Acta Metall. 11(12) (1963) 1355.

51. H. H. Berger, Sold State Electron. 15 (1972) 145.

52. W. J. Moore, R. L. Henry, S. B. Saban, and J. S. Blackmore, Phys. Rev. B 46 (1992) 7229 – 7231.

53. J. C. Burgiel and H. J. Braun, J. Appl. Phys. 40 (1969) 2583.

54. M. O. Aboelfotoh, M. A. Borek, and J. Narayan, Appl. Phys. Lett. 75 (1999) 3953.

55. A. Kamgar, “Rapid Thermal Processing of Silicon“ in Submicron Integrated Circuits, R. K. Watts. Wiley Interscience, New York, 1989.

56. A. Benninghoven, Analysis of sub-monolayers on silver by secondary ion emission. Physica Status Solidi 34 (1969) 169–171.

57. H. Goronkin, S. Tehrani, T. Remmel, P. L. Fejes, K. J. Johnston, IEEE Trans. on Electron. Devices 36(2) (1989) 281-288.

58. J. A. D. Alamo and T. Mizutani, Solid State Electron. 31(11) (1988) 1635-1639.

59. D. E. Cusack, W. M. Glasheen, and H. R. Steglich, 2nd HiTEC, Charlotte, NC, 1994, p. III-17.

60. R. Stall, C. E.C. Wood, K. Board, and L. F. Eastman, Electron. Lett. 15 (1979) 800.

61. NETZSCH Instruments, Inc., Differential Scanning Calorimetry (DSC), Paoli, PA, 19301 USA.

62. B. Wunderlich, Thermal Analysis, Academic Press. New York, 1990, pp. 137–140.

63. J. A. Dean, The Analytical Chemistry Handbook, McGraw Hill, New York, 1995, pp. 15.1–15.5.

64. R. S. Norwiki et al, Thin Solid Films 53 (1978) 195.

65. S. K. Ghandhi, VLSI Fabrication Principles Silicon and Gallium Arsenide, 2nd ed. John Wiley & Sons, Inc., New York, 1994.

66. K. Sarma, R. Darby, K. Rose, O. Aina, W. Katz, and N. Lewis, J. Appl. Phys. 56 (1984) 2703.

67. M. E. Glicksman, Diffusion in Solids: Field Theory, Solid-State Principles and Applications, Wiley, New York, 2000.

68. E. O. Hall, Proc. Phys. Soc., Ser. B, 64 (1951) 747-753.

69. N. J. Petch, J. Iron and Steel Institute (1953) 25–28.

70. R. Dahan, J. Pelleg and L. Zevin, J. Appl. Phys. 67(6) (1990) 2885–2889.

71. P. Gas and F. M. d' Heurle, Appl. Surf. Sci. 73 (1993) 153.

72. S. K. Lahiri and O. C. Wells, Appl. Phys. Lett. 15 (1969) 234.

73. W. B. Pennebaker, J. Appl. Phys. 40 (1969) 394.

74. E. Iwamura, T. Ohnishi, and K. Yoshikawa, Thin Solid Films 270 (1995) 450.

# CHAPTER 4

# LEAKAGE CURRENT AT ELEVATED TEMPERATURES AND SCHOTTKY CONTACTS TO $Al_XGa_{1-X}As$ MATERIALS

## 4.1 Introduction

Among field effect transistors, except JFETs, metal Schottky contacts to compound III-V semiconductors are integral parts in many devices such as modulation doped field effect transistors (MODFETs) and MESFETs. The barrier heights of the metal/semiconductor interface in metal/GaAs systems are limited to a range from 0.7 eV to 0.85 eV [1] due to the numerous surface states at the GaAs interface which cause the "pinning" of the Fermi level at about 1/3 of the bandgap ($E_g$) above the valence band edge [1]. According to our calculations [22], even with a SBH value as high as 1.0 eV, GaAs MESFETs will have a gate-limited leakage current density of $2x10^{-5}$ A/$\mu$m at 300°C, thus limiting applications to temperatures in this range.

Monolithic GaAs/metal Schottky contact systems can be categorized into Al-containing and Al-free types of metallizations. With only a few exceptions, Al-free contacts, including elemental, alloy, and compound contact materials, form Schottky barrier heights (SBH) in the range of 0.7 to 0.85 eV [1-7], while some of the Al-containing ones form higher SBH values after annealing [8-20]. SBH

values higher than 1.0 eV have been reported and the enhanced SBH has been attributed to the formation of $Al_xGa_{1-x}As$ during the annealing process [8,20]. As the growth of $Al_xGa_{1-x}As$ alloys improves, it has become essential to thoroughly characterize these materials because the epitaxial growth is superior to metallization from the control and precision standpoint of view. If a solid relationship between Al-composition and SBH can be built up empirically or theoretically, not only can the device performance be better engineered, but also, more importantly, it potentially improves the uniformity of SBH values, which is of great importance in circuit design. However, unlike GaAs, $Al_xGa_{1-x}As$ surfaces are very reactive, especially at high aluminum concentrations and hence place some stringent requirements on metal/semiconductor pairs employing $Al_xGa_{1-x}As$.

In this dissertation a systematic study was performed by choosing elemental platinum (Pt) and TiWN alloys as Schottky metals to n-type AlGaAs with the Al composition content varying from zero to 30%. AlGaAs epilayers were grown by MBE with Si used as the n-type dopant. Sample specifications are tabulated in Table 4 with all pertinent parameters and characterization techniques also shown in Table 4. Deep level transient spectroscopy (DLTS) for n-type AlGaAs resulted in capricious energy levels for the deep traps [63,64] thus, in Table 4, the results are not listed.In Table 4, the Al compositions of $Al_xGa_{1-x}As$ were determined by the 18K-PL results of $Al_xGa_{1-x}As$ (x= 0.165 and 0.30, respectively). Fig. 34 shows the PL spectra of $Al_xGa_{1-x}As$ (x= 0.165 and 0.30, respectively) taken at 18K, in which transitions at 1734.1 meV and 1820.0 meV, respectively, can be translated into 16.5% and 28.5%, respectively, Al compositions [54] in close agreement to the desired and specified values.

Table 4. Material properties of n-type $Al_xGa_{1-x}As$ materials used for Schottky contact tests

| | GaAs | $Al_{0.165}Ga_{0.835}As$ | $Al_{0.3}Ga_{0.7}As$ |
|---|---|---|---|
| $N_d(x10^{17}cm^{-3})$ | 2.38 | 4.89 | 1.83 |
| Hall Mobility,$\mu_n$ ($cm^2/Vs$) | 3280 | 1886 | 1106.5 |
| Epi-layer Thickness ($\mu m$) | 0.6 | 0.9 | 1.07 |
| Al content by RCXRD( % ) | 0 | 16.5 | 30.0 |
| Al content by PL( % ) | 0 | 16.5 | 28.5 |

Current-voltage (I-V), activation energy (A/E), and capacitance-voltage (C-V) measurements were used to characterize the Schottky barrier heights. Despite the possible errors caused by the DX-centers potentially introducing positive/negative charges, the C-V measurement results is an accepted reference and, effectively, a standard and has been proven to be a powerful and accurate technique for characterizing the SBH in metal/semiconductor systems [39].

## 4.2 Theoretical calculations of gate current as a function of Schottky barrier height (SBH) in MESFET devices at high temperatures

Typical doping concentrations of the channel in III-V FET devices fall into the range from $1x10^{17}$ $cm^{-3}$ to $5x10^{17}$ $cm^{-3}$. At this doping range, the reverse

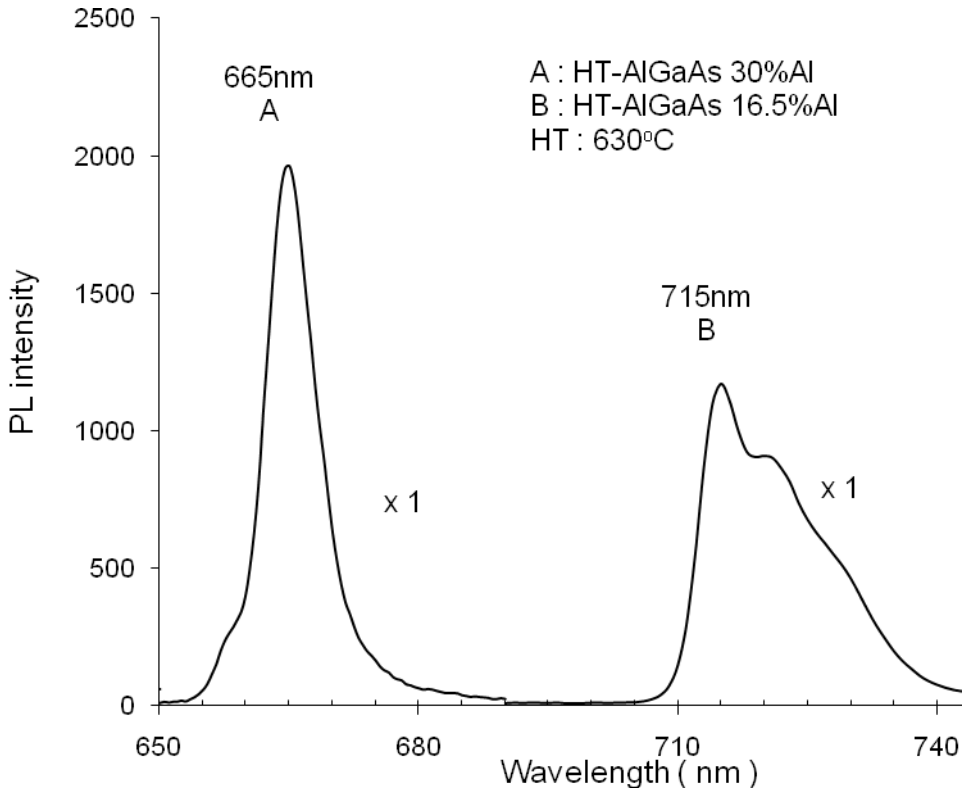



Fig. 34. 18K photoluminescence spectra for $Al_xGa_{1-x}As$ materials grown at 630°C with A) x = 30% of Al and B) x = 16.5% of Al, respectively. Please note that HT, high temperature, refers to a normal growth temperature of 630°C which is considerably higher than 300°C and 350°C, the so called LT, low temperature, used in the dissertation for growing LT-AlGaAs materials.

leakage current of a Schottky diode is dominated by the tunneling through the lowered energy barrier between the metal/semiconductor interfaces due to image forces [1]. The reverse saturation current density of a Schottky diode is given by:

$$J_R \approx J_S \qquad (for V > 3kT/q)$$

$$= A^{**} T^2 \exp(-\frac{q\phi_{B0}}{kT}) \exp(\frac{q\sqrt{q\mathrm{E}/4\pi\varepsilon_s}}{kT}) \tag{14}$$

$$\mathrm{E} = \sqrt{\frac{2qN_D}{\varepsilon_s}(V + V_{bi} - \frac{kT}{q})}$$

where $A^{**}$ is the Richardson constant, $\phi_{Bo}$ is the Schottky barrier height at zero bias, $E$ is the external field applied to the Schottky junction, $V_{bi}$ is the built-in potential, $T$ is the absolute temperature, and $\varepsilon_s$ is the permittivity of the semiconductor. The reverse current of a Schottky diode is analogous to the gate-drain current under reverse bias. The electric field between the gate and drain electrodes is stronger compared to that of the gate-source and the drain-source because the gate and drain are typically biased under opposite polarity voltages (i.e., the gate to source voltage is negative and the drain to source voltage is positive. The calculated current densities (current/channel width in the unit of A/μm) as a function of Schottky barrier height are plotted for different temperatures in Fig. 35. In the calculations for Fig. 35, a 2 μm long x 100 μm wide gate was used. The maximum leakage current densities are limited to the saturation current densities for a given contact area. For a gate barrier height of 1.0 eV, the gate to source leakage current densities at Vgs = -1.0 V and Vds =

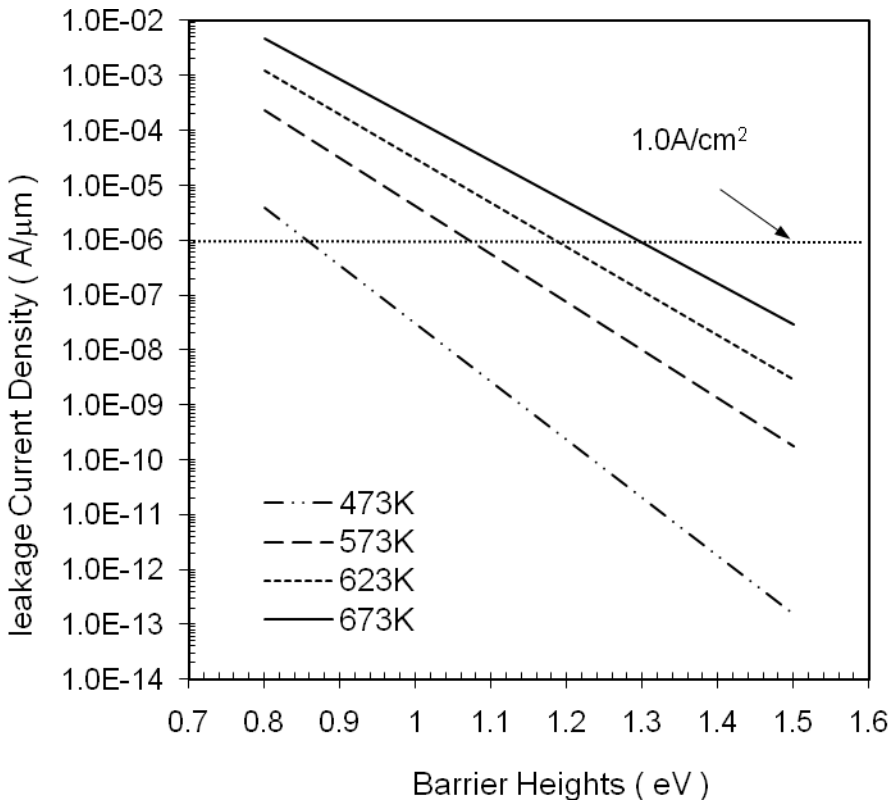



Fig. 35. Current densities, in A/μm, as a function of Schottky barrier height for temperatures between 200°C and 400°C for a 2 μm long and 100 μm gate biased at $V_{gs}$= -1.0 V and $V_{ds}$= 2.0 V.

2.0 V will be $4.2 \times 10^{-6}$, $3.0 \times 10^{-5}$, and $1.6 \times 10^{-4}$ A/μm at 300°C, 350°C, and 400°C, respectively. If the value of leakage current density is limited to a range of 1 A/cm$^2$ (equivalent to $1.0 \times 10^{-6}$ A/μm for unit gate width) for device operation, then a gate barrier of 1.0 eV can only be used to temperatures around 300°C.

Therefore, it is necessary to improve the Schottky barrier to the values higher than 1.0 eV for more reliable operation at high temperatures.

In device operation, the actual leakage current is somewhat higher than what is predicted from the theory due to both the small features and the concentrated electric field at the edges which increases the probability of carrier tunneling through the barrier and the tunneling is, thus, significantly enhanced [1, 22]. In addition, any imperfections of the semiconductor crystal are assumed negligible. Stated in other words, the interfacial states are neglected for the calculation. This neglecting of the interface states needs to be adjusted when heterojunctions are used. As long as the materials in the entire structure are lattice matched to the substrate, it is assumed in this dissertation that the interfacial states are small in number and that thermionic emission is always the dominant carrier transport mechanism for a reverse biased Schottky junction.

## 4.3 Theoretical calculations of substrate leakage currents in FET devices at high temperatures

For a conventional FET type device, the leakage currents arise from two sources in the off state as a result of the reversed biased pn drain junction: generation-recombination and diffusion [23]. Repeating the calculation in Chapter 2 of reference 1 with all parameters appropriately set for GaAs with a doping concentration of 2.0 x 10 $^{17}$ cm$^{-3}$ allows one to generate a plot of generation-recombination and diffusion leakage currents as a function of temperature as shown in Fig. 36. The size of of the transistor used for the data shown in Fig. 36 had a gate of 2 $\mu$m x 100 $\mu$m and was biased at $V_{gs}$= -1.0 V and $V_{ds}$= 2.0 V. A generation-recombination dominated leakage current at temperatures lower than 350°C and a diffusion dominated leakage current at higher temperatures are

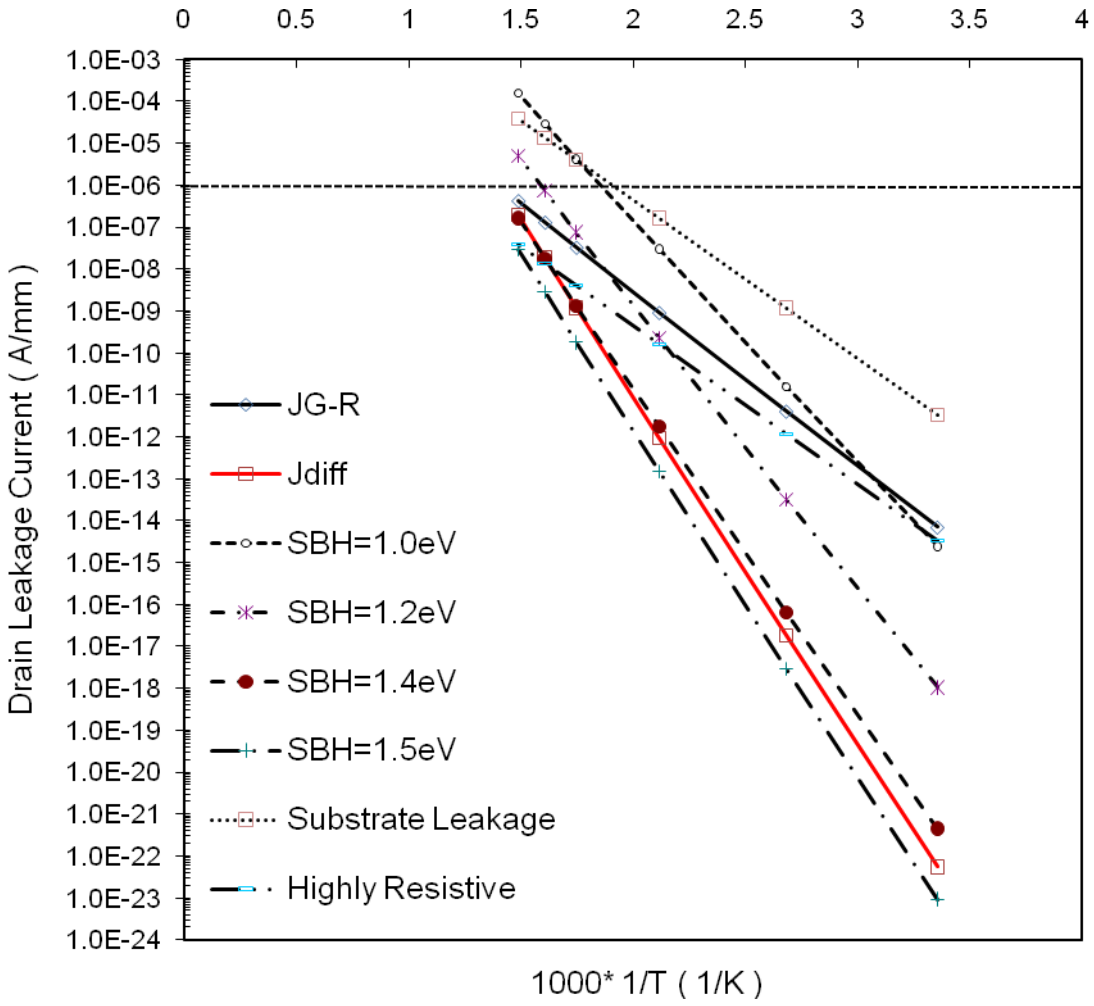



Fig. 36. Drain leakage current densities as a function of temperature under various dominate mechanisms. The dominant mechanisms are (i) G-R and diffusion current at a reverse biased pn junction, (ii) gate leakage current under reverse bias, and (iii) substrate leakage current represented by rectangles, triangles, and circles, respectively.

clearly visible. Fig. 36 also shows gate – leakage – current - limited drain leakage current densities for Schottky Barrier Heights of 1.0eV, 1.2eV, 1.4eV, and 1.5eV, respectively. The information contained in Fig. 36 suggests that gate leakage current surpasses substrate leakage at 400°C for a GaAs transistors having SBH less than 1.2 eV and without back wall barrier or highly resistive layers underneath the active channel. However, by studying and reviewing many real devices, the leakage levels in these real devices are typically much higher than the corresponding calculated ones due to additional leakage paths in these devices. Taking a depleted channel of a FET as an example, above a certain temperature, the background carrier concentration increases exponentially with temperature thus leading to a conduction path for drift leakage currents between the gate, source and drain. Furthermore, the substrate can significantly contribute to the overall leakage simply by its enhanced conductivity at high temperatures. The total leakage current accounting for all leakage paths is then calculated and superimposed onto the previous generation-recombination and diffusion leakage currents. To show the effect of back wall potential barrier on the leakage current, a potential barrier of 250 meV was used when calculating the substrate leakage currents. The results of these calculations are shown in Fig. 37. The thermal activated substrate conductivity was assumed to be due to the EL2 defect which has an activation energy of 0.75 eV [21]. Comparing this substrate leakage current with the gate leakage current at 400°C, it was found that the substrate leakage current surpasses the gate leakage current for SBH values higher than 1.0 eV.

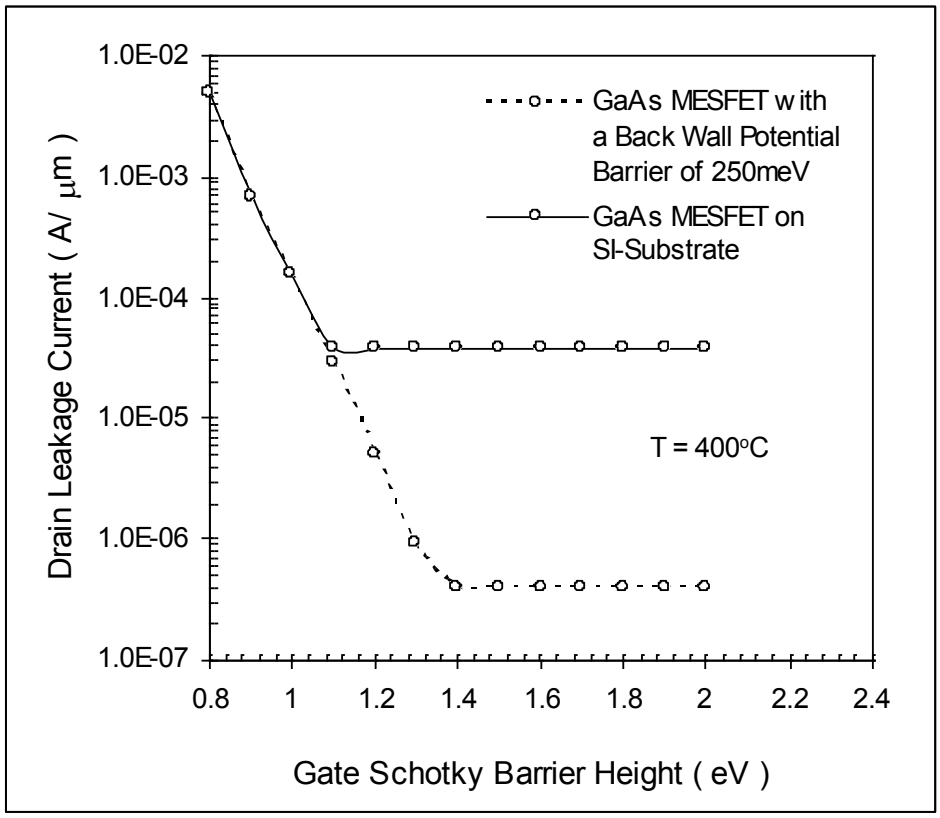



Fig. 37. Total drain current density at 400°C for typical GaAs MESFETs with and without back wall barriers.

Therefore, the advantage of the improved SBH vanishes due to the high substrate leakage currents. This implies that changing the choice of substrate to a wider band-gap material underneath the channel is needed to reduce the substrate leakage current so as to more fully utilize the high SBH values. The total drain leakage current could be reduced to $4.0 \times 10^{-7}$ A/μm if the Schottky barrier height is increased to approximately 1.4 eV.

The relative contributions of energy band-gap, barrier height and back wall barrier height to the overall leakage at 400°C can be produced and deduced from

the simulation of a generic device with the three parameters varied to indicate trends in the high temperature leakage currents. In this dissertation work, the simulated energy band gap values range from 1.1 eV (the band gap energy of Si) at x = 0 to 1.4 eV (the band gap energy of GaAs) at x = 1.0; the barrier height ranges from 0.6 eV to 1.4 eV and the back wall barrier height ranges from 0 meV to 250 meV, respectively. The Si-MOSFET devices represent a high gate barrier, a relatively low energy band-gap, and no back wall. For a Si-MOSFET this leads to a substrate limited leakage current density of $3.85 \times 10^{-5}$ A/μm. In contrast, the GaAs-MESFET has a higher energy band-gap than Si, a low gate barrier and no back wall. For a GaAs-MESFET, this leads to a gate limited drain leakage current density of about $4.82 \times 10^{-2}$ A/μm at 400°C. From Fig. 38, the GaAs-MESFET can be operable, say with 1 A/cm$^2$ of leakage current, if a SBH value of 1.30 eV and a 50% (~125 meV) of back wall barrier height are possible. However, the drain leakage current will be 5% of the maximum drain current, which is equivalent to an on/off current ratio of 20 at 400°C.

## 4.4 Schottky contacts to n-type GaAs

Results demonstrated in this section consist of a mixture of elemental, compound, and alloy Schottky contacts to n-type GaAs. Barrier heights are determined by I-V measurements and are shown in the inset along with the I-V characteristics in Fig. 39.

After annealing in an $N_2$ atmosphere, platinum (Pt), $TiWN_x$, TiW, NiAl, and $Ni_2Al_3$ Schottky contacts to n-type GaAs had ideality factors ranging from 1.02 to 1.10 at room temperature, indicating that the current flow is dominated by

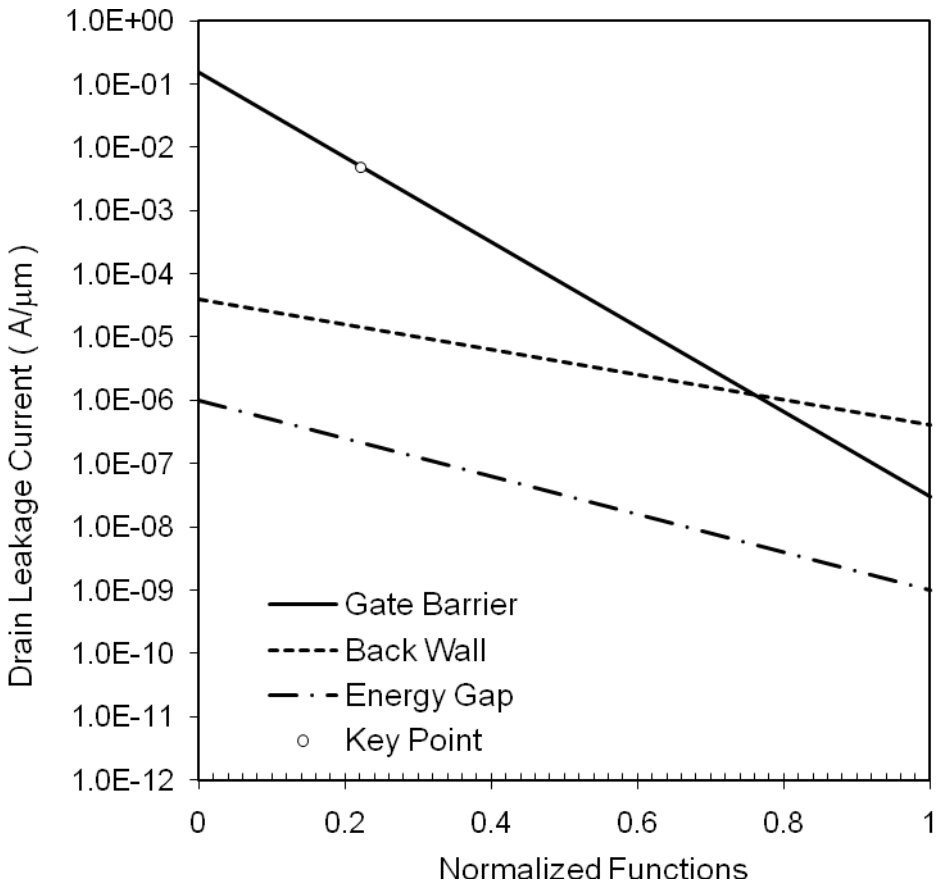



Fig.38 Drain leakage current density at 400°C as function of normalized parameters. The energy gap ranges from 1.1 eV (the band gap energy of Si) at x = 0 to 1.4 eV (the band gap energy of GaAs) at x = 1.0, while the gate barrier ranges from 0.6 eV to 1.4 eV and the back wall potential from 0 meV to 250 meV.

Schottky emission which is temperature dependent. Among the materials studied, the barrier heights of TiW and $TiWN_x$ materials were found to have the lowest barrier heights. Increasing the nitrogen content during the sputtering leads to a monotonic decrease in barrier height for $N_2/(N_2+Ar)$ ratios from zero percent to 25% of 0.63 eV to 0.59 eV, respectively. These results agree with the observations that, in $TiWN_x$ to n-type GaAs contact systems, too much nitrogen

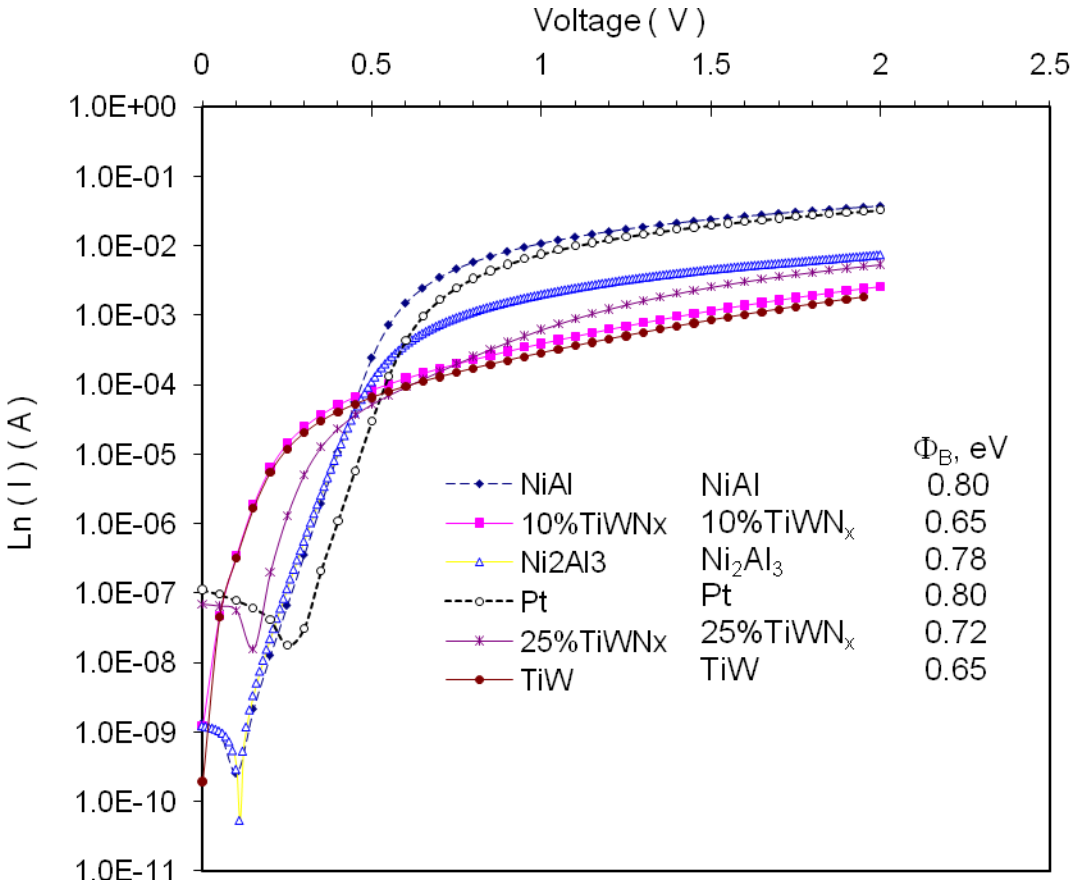



Fig. 39. Current-voltage characteristics for several Schottky contacts to n-type GaAs.

incorporation leads to the formation of GaAsN which has a lower bandgap energy than that of GaAs, while insufficient nitrogen incorporation frees the Ti and downgrades the thermal stability of this contact system [25]. Typical Schottky barrier heights for metal/n-type GaAs were limited to 0.8 eV for all the materials tested. The thermal stability of these Schottky materials was carried out on a thermal hot stage maintained at 300°C for various length of times. Degradation of contacts was detected by the forward-bias current-voltage (I-V) characteristics in terms of barrier heights and ideality factors for $TiWN_x$, NiAl, and $Ni_2Al_3$. The ideality factors were improved after annealing at 300°C for 60-hr which could possibly be attributed to the significant reduction or elimination of defects and (planar interfaces) between the respective metal and semiconductor [26]. Barrier heights of $TiWN_x$, NiAl, and $Ni_2Al_3$ to n-type GaAs were measured in a range of $0.65 \pm 0.03$ eV, $0.80 \pm 0.02$ eV, and $0.78 \pm 0.02$ eV, respectively.

TiW material oxidized during the annealing process thus requiring an overlayer such as Au to protect the TiW material during annealing. However, the barrier height remained unchanged with the presence of Au but values as low as 0.65 eV were measured after annealing. The low barrier heights for $TiWN_x$ and TiW materials could be related to sample preparation since sputtering is a high-energy process and the plasma of the sputtering process may introduce damage to the semiconductor surface [40-44].

Results from I-V measurements for the Schottky diodes made by these materials and protected $Cu_3Ge$ ohmic contacts showed that the diodes were no longer rectifying at 300°C as seen in Fig. 40. Although NiAl has the highest barrier height among the tested materials, it still behaves like a “soft Schottky”

contact at 300°C. This indicates the reduction of barrier height at high temperatures is sometimes an intrinsic property that rules out the usage of certain materials [54].

For example, materials that form a variety of reaction compounds with the semiconductors and materials that have high diffusivity in the semiconductors are subject to changes in barrier height and the current transfer mechanism. On the contrary, some materials, such as Ni/Al to n-GaAs, are more rectifying at higher temperatures or remain nearly unchanged [54].

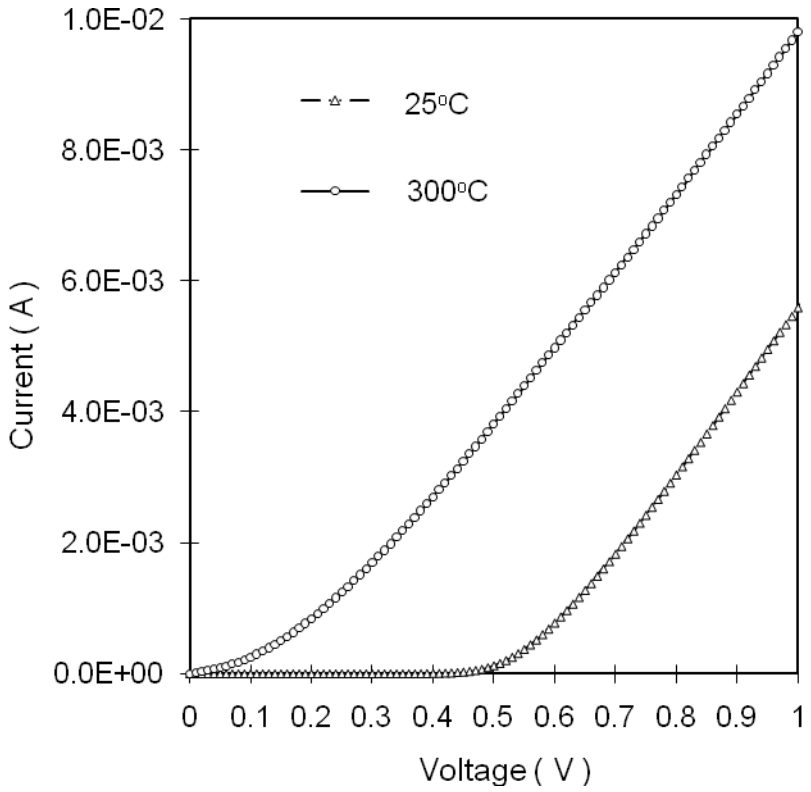



Fig. 40. I-V characteristics under forward bias at 25°C and at 300°C for NiAl-based Schottky contacts to n-type GaAs after annealing at 300°C for 3-hr.

The reverse-bias I-V characteristics were a different story. Along with the improved conductivity of the thin films after annealing, higher current flow in the diode was also measured. Figs. 41(a) to (d) show the I-V curves of the reverse-biased Schottky diodes made using TiW, NiAl, and $Ni_2Al_3$, respectively as the contact materials. In Fig. 41(a), (b), and (c), a significant increase of leakage current was measured. The early breakdown is a consequence of intermixing of contact materials and GaAs through the unstabilized interface. To the author's knowledge, none of these three contacts have been reported to be stable at 300°C. Surprisingly, $TiWN_x$ showed very stable Schottky behavior even after a 423 hours annealing at 300°C as seen in Fig. 41(d). Leakage currents measured on a number of devices were very similar and never exceeded $10^{-7}$ A for a gate area of $4x10^{-4}$ $cm^2$. $TiWN_x$ materials have shown good thermal stability as potential high temperature Schottky contacts [40-44]. However, the barrier heights apparently have not achieved the 1.0 eV mark at 300°C operation for $TiWN_x$ Schottky contacts to GaAs.

## 4.5 Schottky contacts to n-type $Al_xGa_{1-x}As$, $x \leq 0.30$

### 4.5.1 Platinum Schottky contacts

I-V measurements, activation energy measurements, and C-V measurements for Pt Schottky contacts to $Al_xGa_{1-x}As$ are shown in Figs. 42(a) and (b). Essential parameters extracted from the analysis are also tabulated in discussion section.

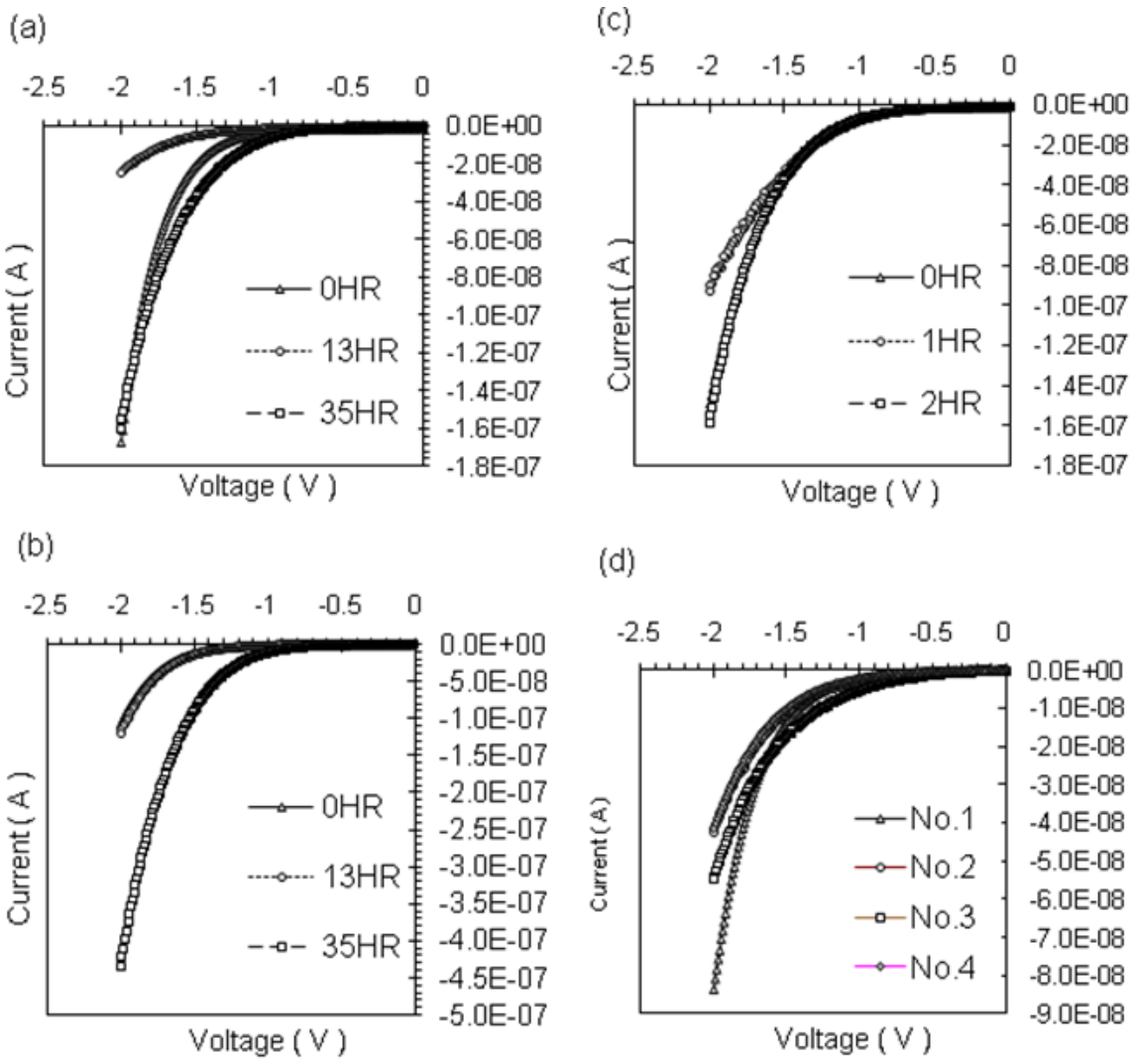



Fig. 41. Current-voltage characteristics under reverse bias conditions for four different Schottky contacts after annealing at 300°C for 423-hr (a) TiW, (b)NiAl, (c) $Ni_2Al_3$, and (d) TiWN.

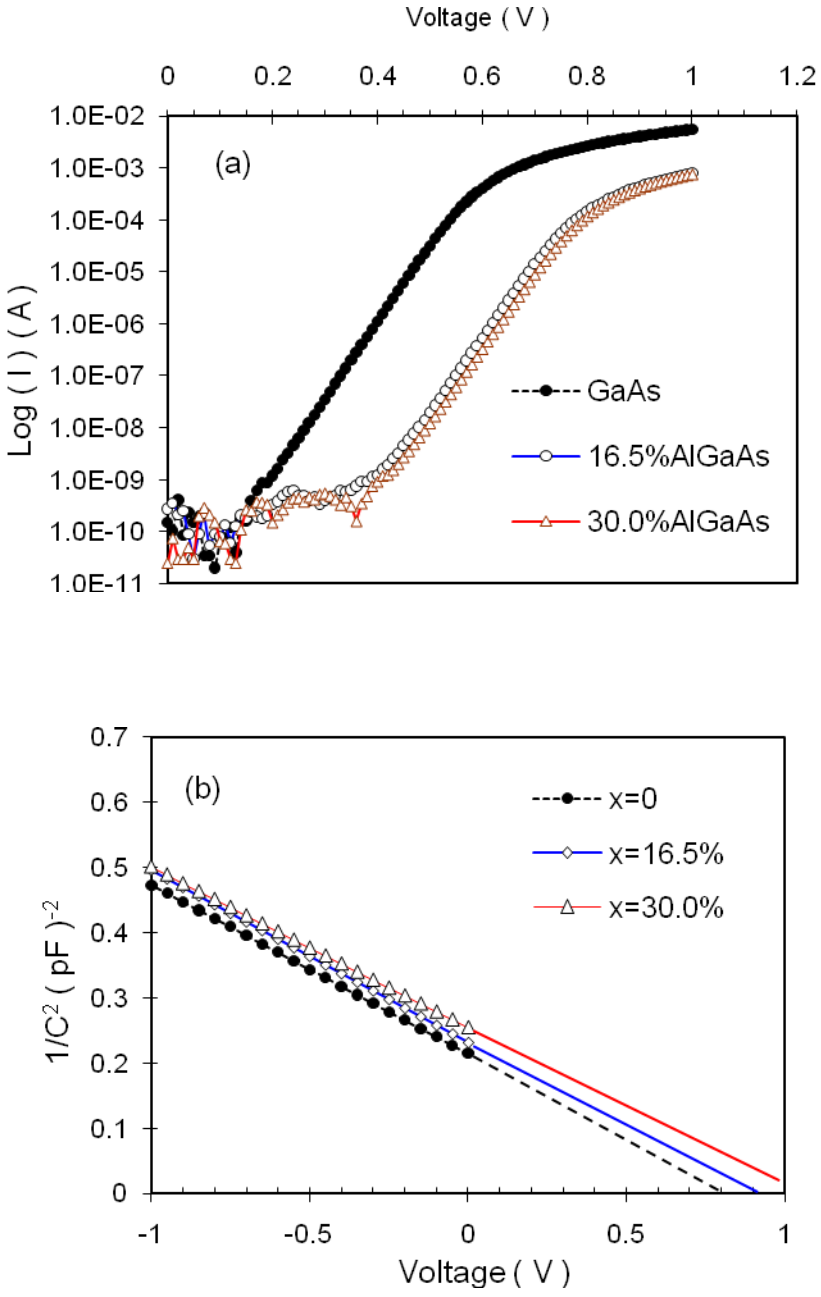



Fig. 42. Characteristics of Pt Schottky contacts to n-type $Al_xGa_{1-x}As$ materials for x = 0 to 0.30 from (a) I-V and (b) C-V measurements.

Increases in Al composition of the $Al_xGa_{1-x}As$ layer resulted in a monotonic increase in barrier height for Pt/n-type AlGaAs Schottky diodes. The results of activation energy measurements followed closely to that of I-V measurements, while C-V measurements gave slightly higher barrier heights. With Al compositions of AlGaAs of zero, 16.5%, and 30.0%, the Schottky barrier heights to platinum were of 0.8 eV, 0.92 eV, and 1.06 eV, respectively, based on I-V measurements. The wet etching prior to the metal deposition did not result in much deviation of the ideality factors from unity since all the measured ideality factors were equal to or less than 1.08. An interesting, normally overlooked, issue concerns the value of the Richardson constants in AlGaAs materials and will be discussed later in Section 4.5.4 of this dissertation. The proper values can be extracted from the activation energy measurements if the contact area is carefully measured [1].

### 4.5.2 10%$TiWN_x$ Schottky contacts

Figs. 43(a) to (c) show the results of I-V measurements, activation energy measurements, and C-V measurements, respectively, for 10% $TiWN_x$ Schottky contacts to $Al_xGa_{1-x}As$. The nitrogen compositions determined by XPS were about 18 at %. Ten percent nitrogen concentration represents the processing condition where the $N_2$ to $N_2$+Ar flow rate ratio was kept at 10%. Such a high percentage of $N_2$ helps to stabilize the $\beta$-phase $TiWN_x$ and most of the nitrogen atoms were found to bond with titanium and tungsten, to oxygen. Barrier heights were found for this material to be 0.675 eV to GaAs, 0.90 eV to 16.5% AlGaAs, and 1.10 eV to 30.0% AlGaAs. Again, a monotonic increase of the SBH as a

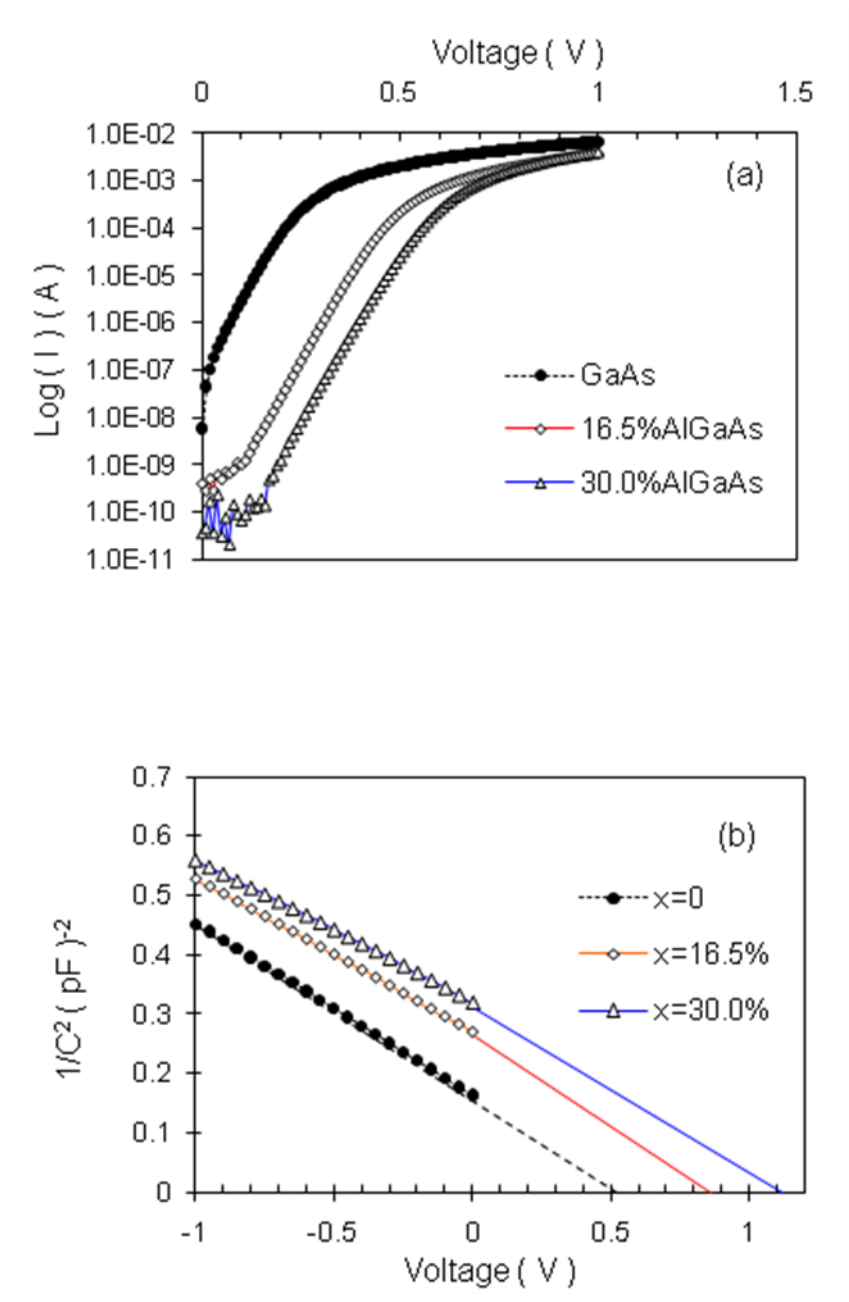



Fig. 43. Characteristics of 10% $TiWN_x$ Schottky contacts to n-type $Al_xGa_{1-x}As$ materials for x = 0 to 0.30 from (a) I-V and (b) C-V measurements.

function of increased Al compositions was observed in $TiWN_x$ Schottky contacts in this dissertation.

### 4.5.3 25%$TiWN_x$ Schottky contacts

Figs. 44(a) and (b) show the results of I-V and C-V measurements, respectively, for 25% $TiWN_x$ (i.e., x = 0.25) Schottky contacts to $Al_xGa_{1-x}As$ . The trend of the barrier height with respect to the Al composition was similar to what was observed in the previous section in terms of the bandgap energy dependence of the semiconductor to the Schottky contact. Barrier heights for 25% $TiWN_x$ were found to be 0.59 eV to GaAs, 0.81 eV to 16.5% AlGaAs, and 0.95 eV to 30.0% AlGaAs, based on the I-V measurements.

Fig. 45 shows the results of activation energy measurements for TiWN Schottky contacts to n-type AlGaAs at temperatures between room temperature to 150°C. High linearity between saturation current and reciprocal temperature was preserved in this temperature range. Again, the barrier height was found to increase as the Al composition of the AlGaAs materials increased. All ideality factors measured were fairly close to unity indicating that the dominant mechanism of carrier transport is thermionic emission. The barrier heights of 25% $TiWN_x$ to 16.5% and 30.0% AlGaAs, respectively, were found to be 0.968 eV and 0.993 eV, respectively. For 10% $TiWN_x$ Schottky contacts to n-type AlGaAs, measured SBHs were 0.808eV and 1.075eV for x = 16.5% and 30.0%, respectively, $Al_xGa_{1-x}As$ as can be seen from Fig. 45.

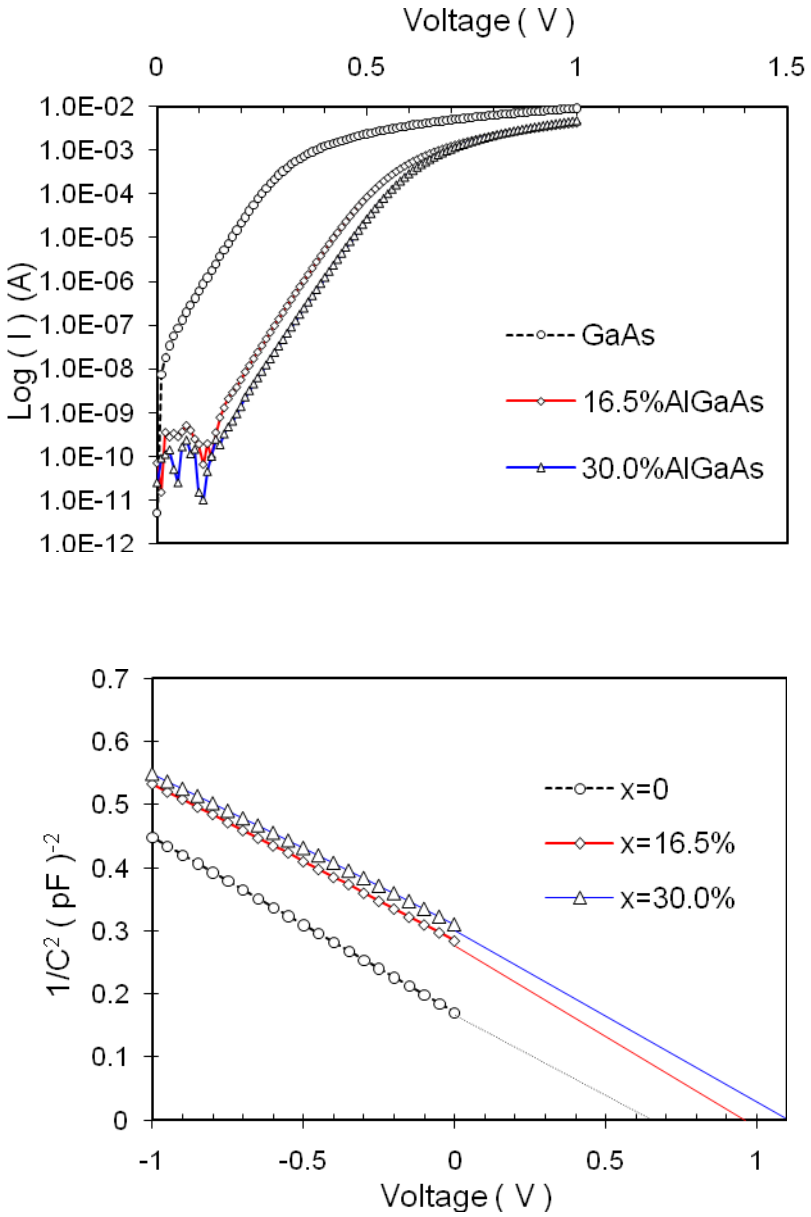



Fig. 44. Characteristics of 25% TiWN Schottky contacts to n-type $Al_xGa_{1-x}As$ materials for x = 0 to 0.30 (a) I-V and (b) C-V measurements.

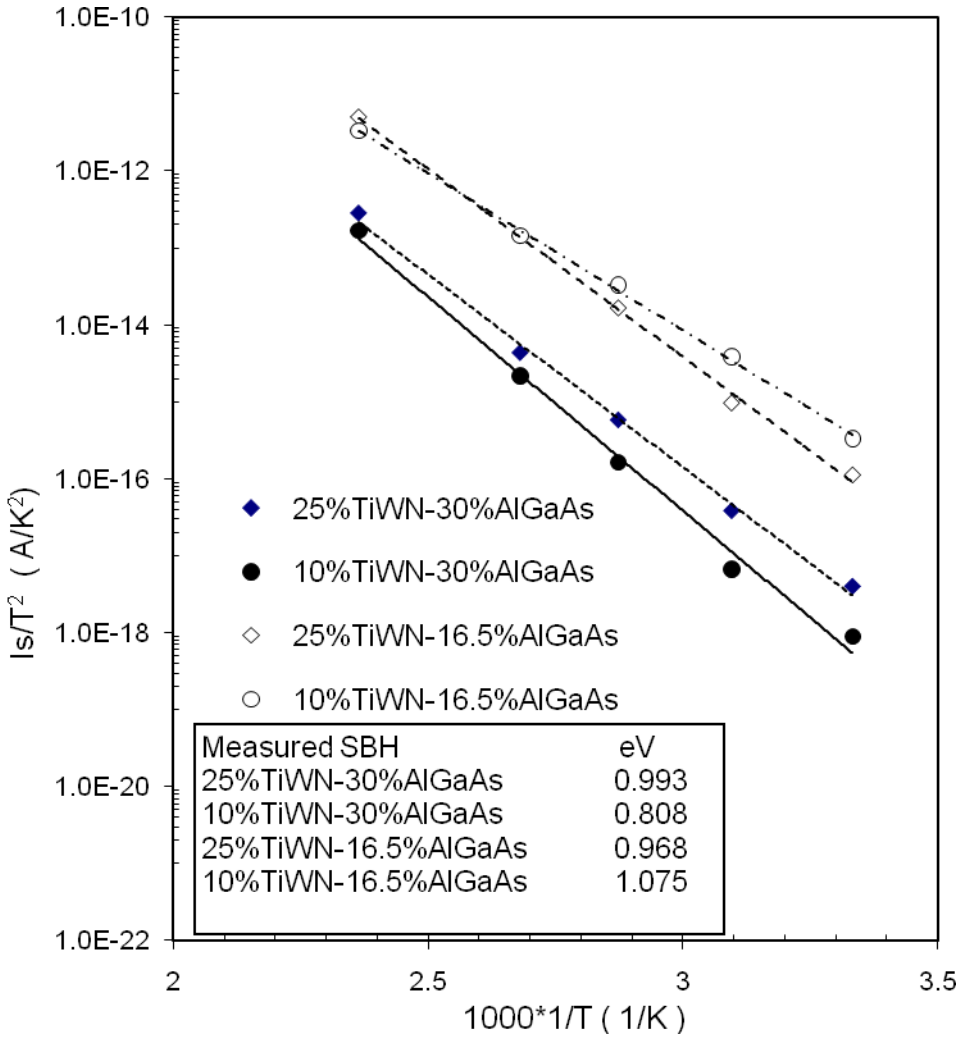



Fig. 45. Activation energy measurements for TiWN Schottky contacts to n-type AlGaAs at temperatures from room temperature to 150°C.

### 4.5.4 Discussion

Early attempts to predict the effective Schottky barrier height for metal/semiconductors, particularly in GaAs and AlGaAs materials, failed to reach a general agreement with the empirical observations [45,46]. Three rules most frequently cited and prominent in the literature are the anti-site model by Allen and Dow [37], the anion vacancies model by Dow and Smith [36], and metal induced gap states (MIGS) by Tersoff [38]. These three rules were all proposed to deal with the pinning position of the Fermi-level in the AlGaAs system due to surface states.

a). Barrier height of metals to n-type GaAs :

The measured barrier heights as a function of electronegativity of metals deposited on Si and GaAs are plotted in Fig. 46 [1]. A weak, but observable, linear function in the Si Schottky system has been developed and attributed to Si being a covalent semiconductor. On the contrary, the randomly distributed barrier heights make the quantitative analysis difficult for metals to GaAs but the average barrier height is close to 0.8 eV, almost independent of the electronegativity of metals. The group consists of Cu and the precious metals Ag, Au, Pd and Pt, which have a mean barrier height of 0.97 ± 0.04 eV to n-type AlGaAs measured from actual diodes. Recent reports on the Schottky contacts to GaAs reconfirmed that there exists no linear relationship between Schottky barrier height and metal work function as would be suggested by the Schottky-Mott theory [45].

Similar predicted results were obtained if the metal work function was replaced by the Pauling or Miedema electronegativities [46]. The relationship

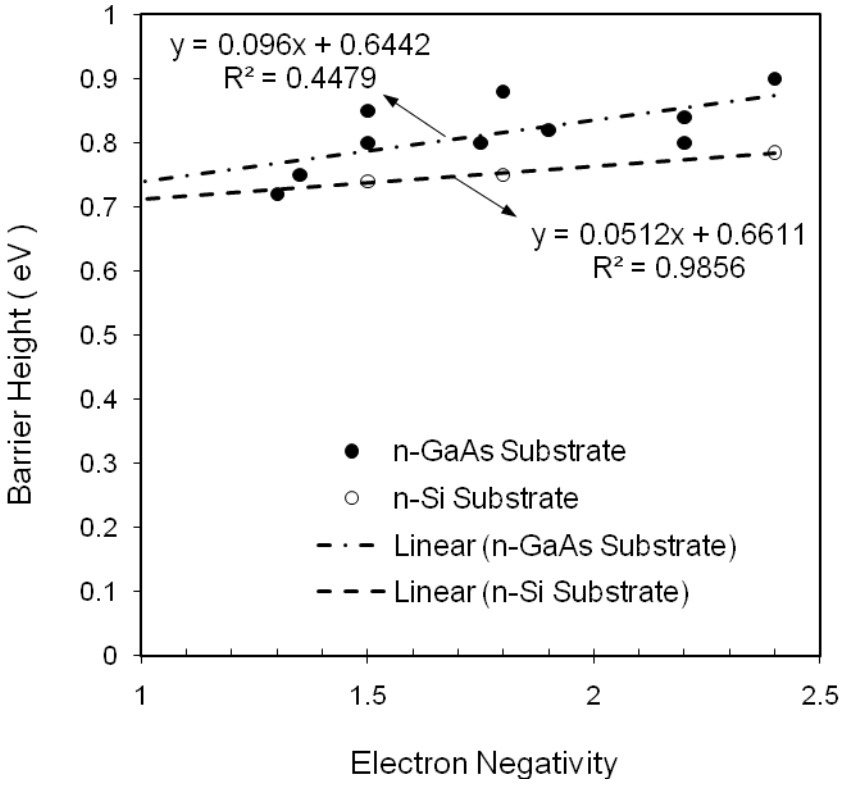



Fig. 46. Measured barrier heights as a function of electronegativity of selected metals deposited on n-Si and n-GaAs. (Adapted from [1])

between the Schottky barrier heights and Pauling's electronegativities of the contact metals suggests that the interfacial chemistry plays a crucial role during Schottky barrier formation [46]. The pinning strength defined as the change in the barrier height with respect to the change in electronegativity of metals was found to be ~0.1 eV, which is a considerably large value and indicative of the strong effect pinning has among all semiconductors [1].

b). Barrier height of metals to n-type $Al_xGa_{1-x}As$, x = 0 to 0.3:

The experimental results of the Schottky barrier heights and ideality factors determined by I-V, activation energy, and C-V measurements for metals to n-type AlGaAs are summarized in Table 5.

The calculated $E_g$-$\Phi_{bn}$ (equivalent to the barrier height to p-AlGaAs assuming the same pinning levels exist for both n-type and p-type AlGaAs and also summing the barrier heights to p-AlGaAs and to n-AlGaAs for the same Schottky contact should result in the bandgap energy of AlGaAs) of Pt to n-type AlGaAs as a function of Al composition based on the three models previously mentioned are shown in Fig. 47. For the region of Al content less than 30%, all three models predict an increase in barrier height for Pt contacts to n-type AlGaAs. Basically, the predictions from the anti-site model and anion vacancy rule show larger increases in barrier height than the MIGS model predicts. Fig. 48 shows the measured $E_g$-$\Phi_{bn}$ versus aluminum composition for $TiWN_x$ and Pt contacts with the predicted pinning levels from all three models shown for comparison. The quantitative fit to the MIGS model is excellent for the Pt contacts. The maximum error is 0.02 eV. In view of uncertainties in the measured barrier heights and the known band-gap values of AlGaAs alloys, the fit is excellent.

The results for these two types of $TiWN_x$ contacts indicate that these contacts obey the MIGS model rather than the anion vacancy model. The maximum error is 0.045 eV and the average deviation from the theoretical curve is about 0.025 eV. Again, in view of uncertainties in the measured barrier heights and the known band-gap values of AlGaAs alloys, the fit is excellent. The same

Table 5. Experimental results for the Schottky barrier heights and ideality factors determined by I-V, activation energy (A/E), and C-V measurements.

| | | | GaAs | $Al_xGa_{1-x}As$ X = 0.165 | $Al_xGa_{1-x}As$ X = 0.30 |
|---|---|---|---|---|---|
| Pt | $\Phi_B$ (eV) | I-V | 0.86 | 1.01 | 1.10 |
| | | C-V | 0.8 | 0.88 | 1.0 |
| | Ideality Factor | | 1.15 | 1.20 | 1.20 |
| 10% TiWN | $\Phi_B$ (eV) | I-V | 0.63 | 0.86 | 0.94 |
| | | A/E | -- | 0.81 | 1.08 |
| | | C-V | 0.66 | 0.83 | 0.99 |
| | Ideality Factor | | 1.08 | 1.06 | 1.04 |
| 25% TiWN | $\Phi_B$ (eV) | I-V | 0.59 | 0.81 | 0.95 |
| | | A/E | -- | 0.97 | 1.00 |
| | | C-V | 0.61 | 0.90 | 1.05 |
| | Ideality Factor | | 1.00 | 1.10 | 1.01 |

trend was also observed in lanthanum hexaboride ($LaB_6$) but is not shown in the figures.

The results are striking in that the pinning position of Fermi-level can be described by a simple model requiring that the Fermi-level resides in the middle of the energy bandgap.

The physics of this gap center was illustrated by Tersoff [38] in which the barrier height of metal to p-type semiconductor, $\Phi_{bp}$, is

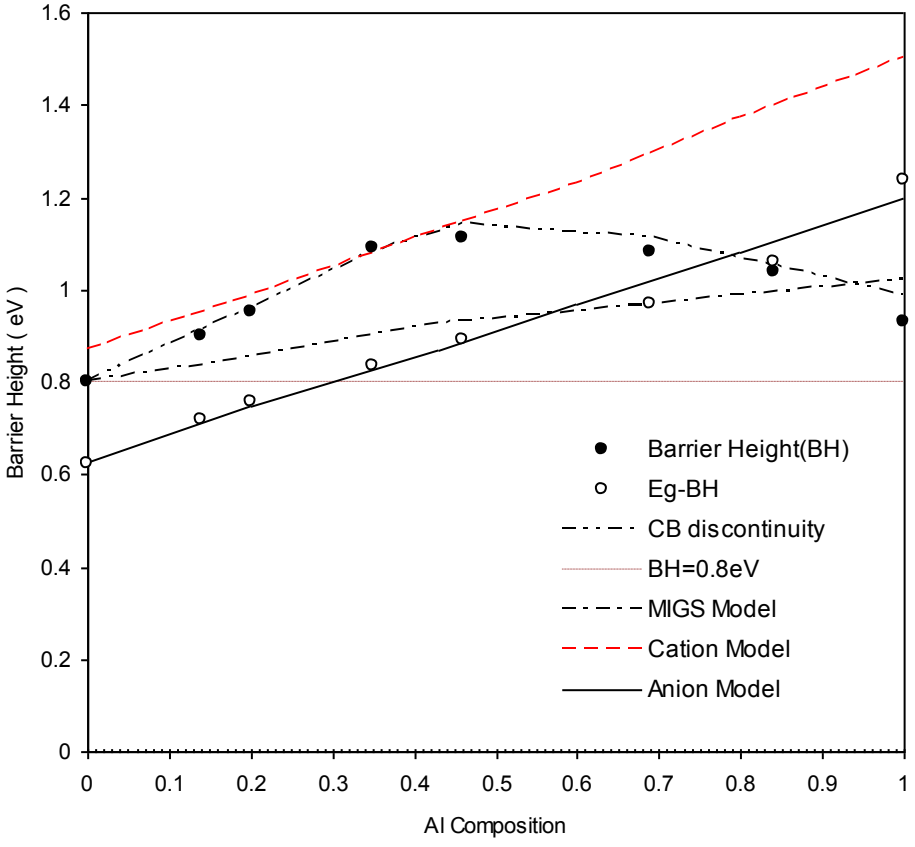



Fig. 47. Calculated barrier heights as a function of Al composition for Pt Schottky contacts to n-type AlGaAs with Al content ranging from zero to 100%.

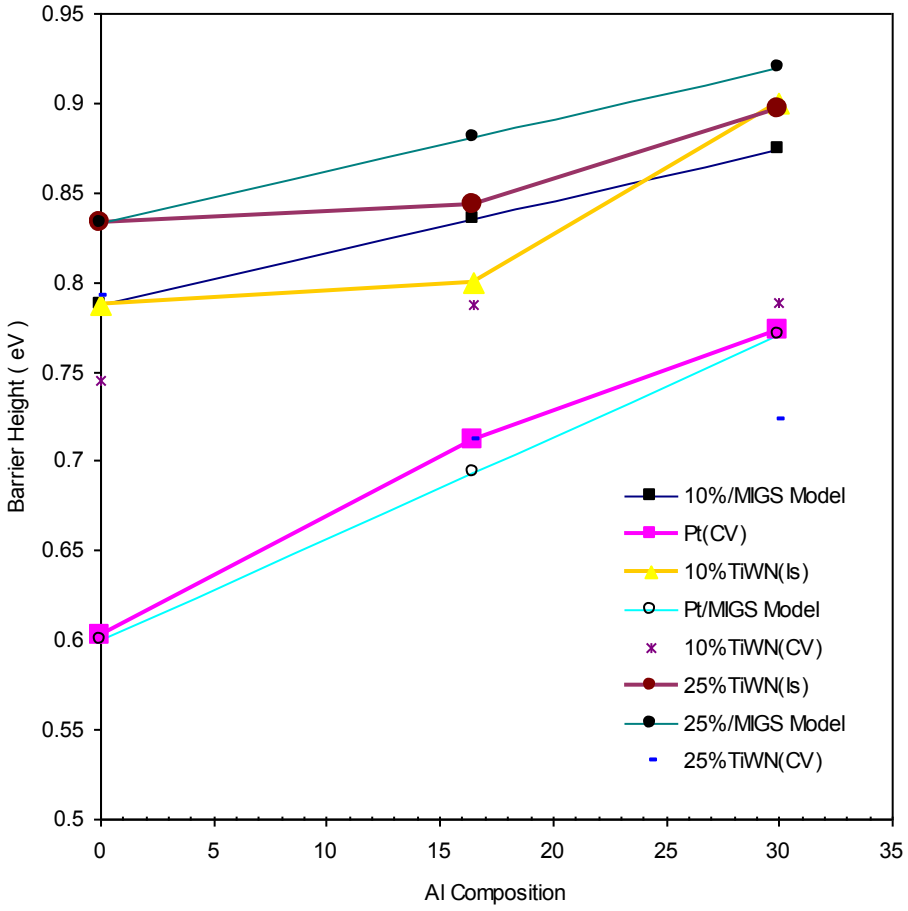



Fig. 48. Measured Schottky barrier heights of TiWN and Pt contacts to n-type AlGaAs as a function of Al composition. The values predicted by the MIGS model are also plotted for comparison.

$$\phi_{bp} = \frac{1}{2}\left[E_g^i - \frac{\Delta}{3}\right] + \delta_m \qquad (15)$$

where $E_c$ is the indirect conduction minimum, i.e., excluding $T$, $E_g^i$ is the minimum

$$E_g^i \equiv E_c - E_v \qquad (16)$$

indirect gap, $\Delta$ is the spin-orbit splitting in the valence band, and $\delta_m$ is a constant depending on contact materials. Quantitatively, given any large subset of data, one could determine $\delta_m$ and predict the remaining data to within 0.1 eV.

However, other deposition techniques produce different trends that require a different model than the MIGS model to obtain a better fit [39]. Therefore, the potential of detailed theoretical analysis to predict specific quantitative correlations has not yet been universally established. Qualitatively, the trend shows that a monotonic increase in the barrier height of metals as the Al composition in AlGaAs increases and this will be beneficial for high-temperature applications since the leakage due to the gate will be dramatically reduced as the SBH increases.

## 4.6 Polycrystalline and monocrystalline Schottky contacts to n-type $Al_xGa_{1-x}As$, x = 0.3

Owing to the versatility of modern growth techniques, epitaxial Schottky contacts and semiconductors can be grown in the same system as part of a sequence process/growth run. Known to be a time-consuming process step [39], the gate metallization needs to be carefully examined in terms of methods to

reduce the process time and increase the throughput. The epitaxial growth of a contact metal right after semiconductor growth, among other things, also eliminates a long waiting time prior to the deposition. It can be expected that a lower density of surface states will result by such in-situ postgrowth processing steps. Therefore, if one is able to define the features of a gate contact that meets the target value, contacts prepared in this way should have better performance in terms of better ideality factor, thermal stability, and lower leakage currents at reverse biases [21,39].

Thermally stable rare earth compounds have been developed for high speed, high power, and high temperature applications [47]. In this section, thulium phosphide (TmP) grown by MBE on AlGaAs epilayers is characterized. High quality TmP epilayers are consistently obtained for growth temperatures ranging from 500 to 600°C with growth rates between 0.5 and 0.7 μm/hr. The properties, especially leakage currents at high temperature, are of great interest since attempts to improve the barrier heights to values higher than 1.2 eV have not had much success yet. An alternative way to eliminate the leakage path through grain boundaries in conventional deposited Schottky materials is by making or replacing them with monocrystalline materials.

Fig. 49 shows the result of room temperature activation energy measurements for sputtered contacts of Pt, $LaB_6$, 25% TiWN, and 35% TiWN, along with epitaxial TmP contact to n-type $Al_xGa_{1-x}As$, with x = 0.3, at room temperature. TmP formed the highest SBH of the five contacts, followed by $LaB_6$, Pt, and then the two types of TiWN contacts.

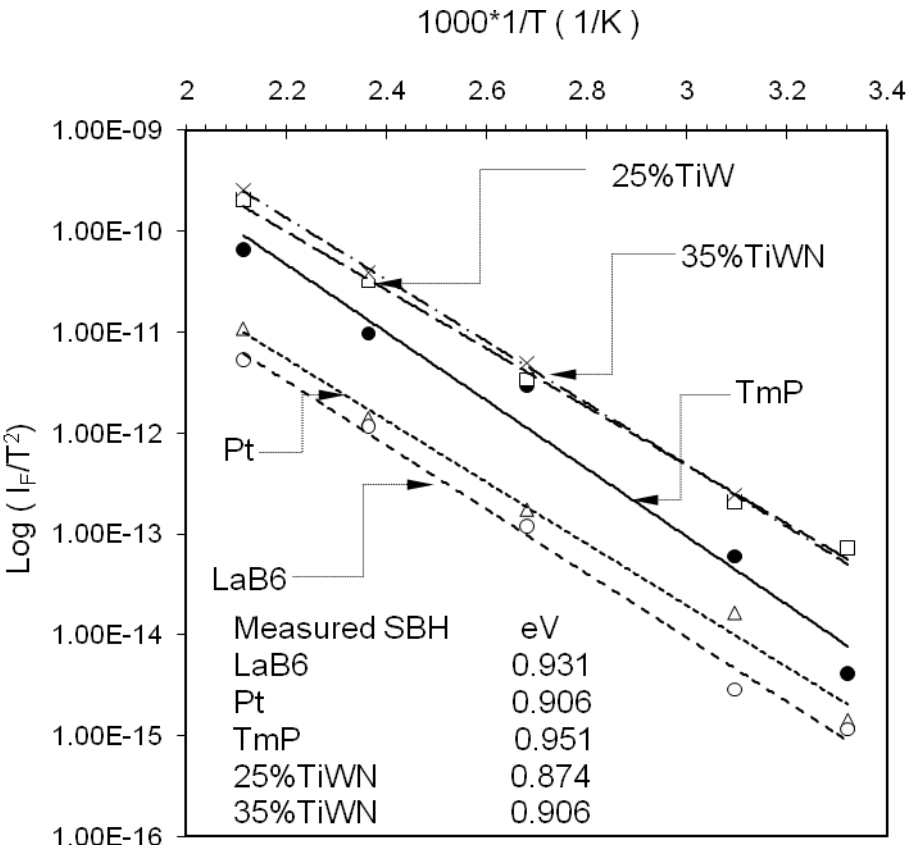



Fig. 49. Results of room temperature activation energy measurements for several Schottky contacts including polycrystalline and single crystal TmP to n-type AlGaAs with an Al composition of 30.0%.

Fig. 50 shows the room temperature C-V characteristics of Schottky diodes made by deposited $LaB_6$, DC-sputtered 25% TiWN, DC-sputtered 35% TiWN contacts, and epitaxial TmP contacts.

C-V measurements show that the SBH of TmP is lower than that of $LaB_6$ but higher than that of TiWN. The results did not favor the utilization of epitaxial Schottky contacts in terms of barrier height for high temperature applications.

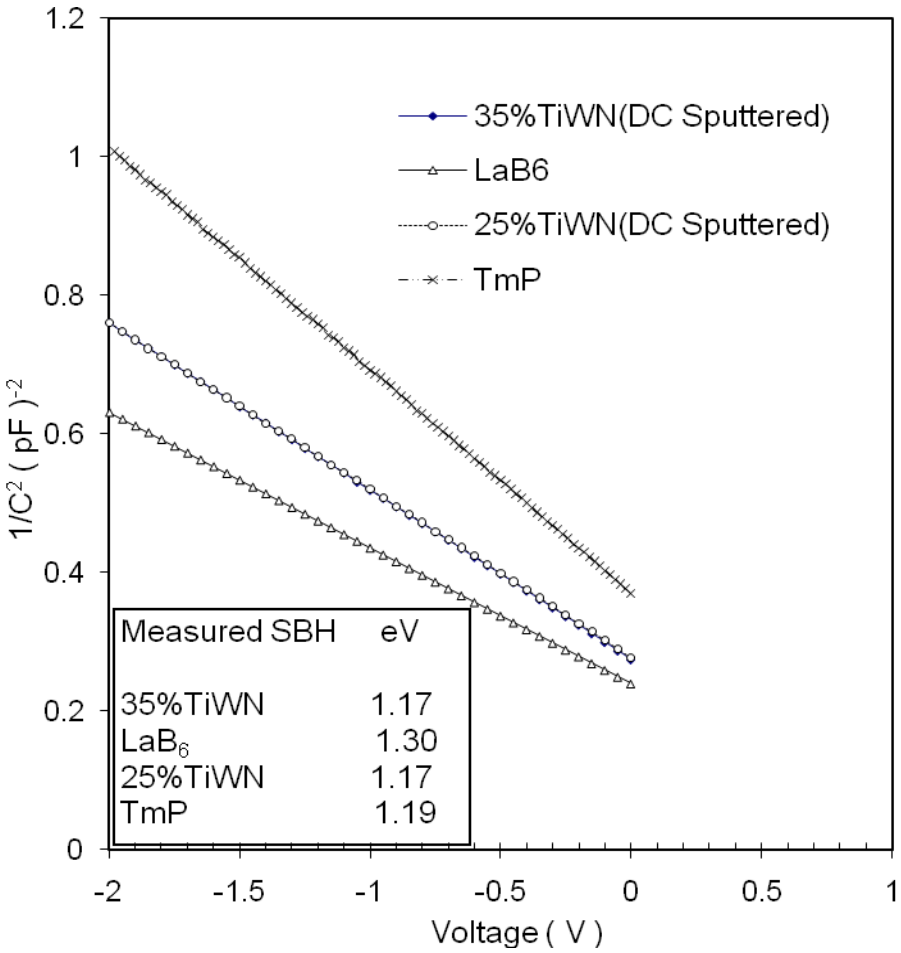



Fig. 50. C-V characteristics of several Schottky contacts to n-type AlGaAs with an Al composition of 30%. The TmP contacts are single crystal with all the others being polycrystalline.

A high resolution XRD analysis result is shown in Fig. 51(a) where the GaAs (004) and AlAs (004) peaks appear at 66.20° and 66.30°, respectively. Fig. 51(b) shows the X-ray pattern of TmP grown on n-AlGaAs in which only sharp (002) and (004) peaks were observed. The peak at a $2\theta$ of 32.35° represents the diffraction from the (002) planes of TmP, while the (004) peaks of both materials appear separately, 67.35° for TmP, 66.20° for GaAs, respectively. According to

XRD analysis, TmP was found to have an NaCl structure and a lattice constant of 5.573 Å, thus having only a -0.15% mismatch to AlGaAs. AFM measurements of the surface roughness also showed a smooth and flat surface with an RMS roughness of 3 to 4 Å, just within a monolayer fluctuation in a 50 x 50 $\mu m^2$ scanned area. Based on the X-ray diffraction results, it is believed that TmP has been epitaxially grown on AlGaAs for first time that we are aware of [55].

Fig. 52(a) shows I-V characteristics of a TmP Schottky contact to n-type AlGaAs as a function of temperature. As seen in Fig. 52(a), under forward bias, the turn on voltage decreases as the temperature increases. From the measured I-V characteristics, the SBH can be extracted using the following equation [1]:

$$I = A A^* T^2 \, Exp\,( -\phi_b / kT ) \, Exp\,( qV/nkT ) \qquad (17)$$

where $A^*$ is Richardson constant, $k$ is the Boltzmann constant, $A$ is the contact area, $T$ is the absolute temperature in Kelvin, n is the ideality factor, and $\phi_b$ is the Schottky barrier height. The value of the Richardson constant used in this study is 90 $Acm^{-2}K^{-2}$ [8]. The Schottky barrier height and ideality factor at room temperature calculated by Equation (1) are 1.07 eV and 1.18 eV, respectively.

C-V measurements resulted in a Schottky barrier height of 1.19 eV as shown in Fig. 52(b). From the $1/C^2$ vs. V plot for this SBH, the Schottky barrier height was obtained directly from the intercept of the voltage axis plus the thermal voltage, $kT/q$ which is 25.9 meV at room temperature.

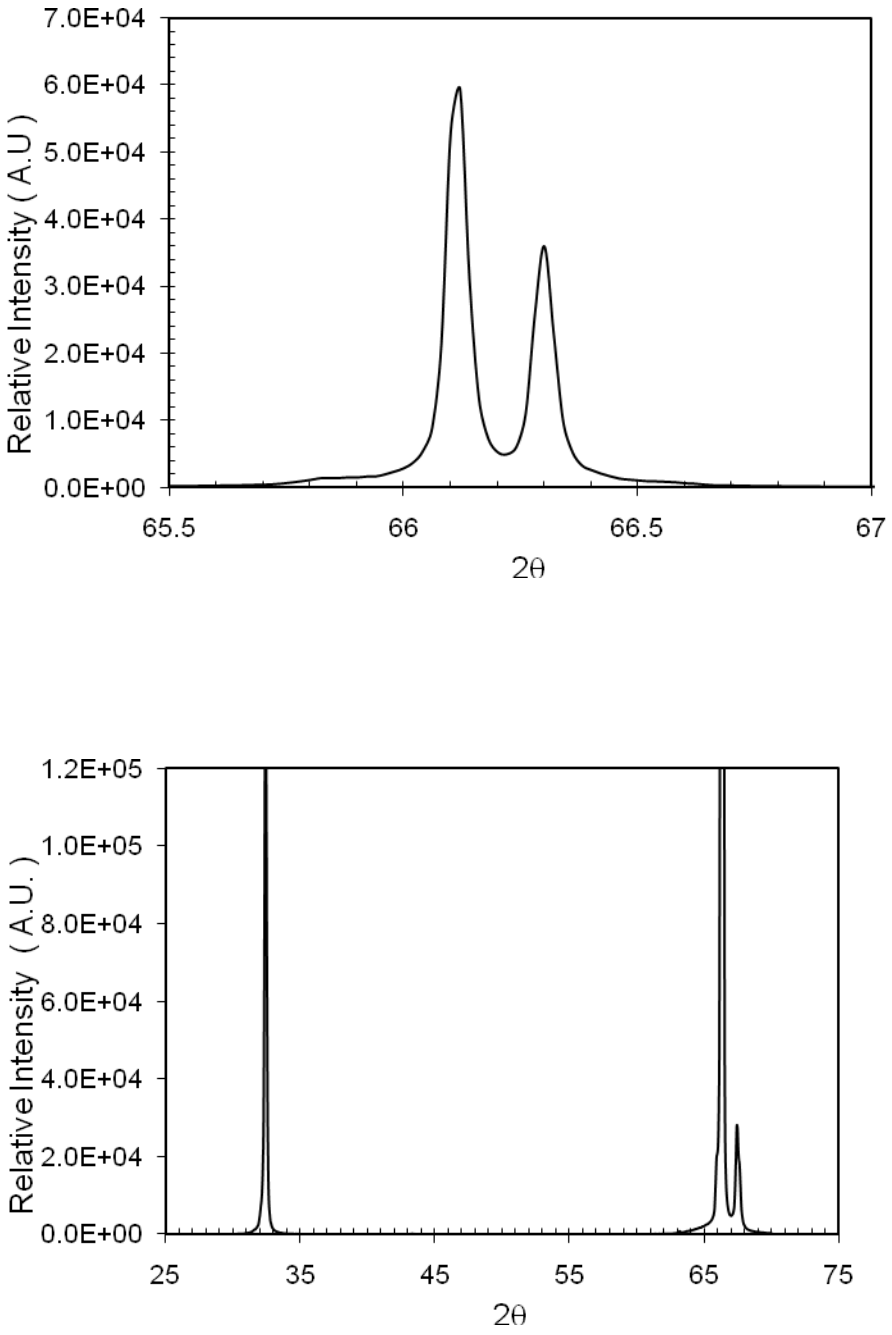



Fig. 51. XRD spectra for TmP on n-type AlGaAs with an Al composition of 30% from (a) high resolution XRD results showing the AlAs and the GaAs (004) peaks; (b) showing the TmP (002) and (004) peaks, as well as the (004) peak of AlGaAs.

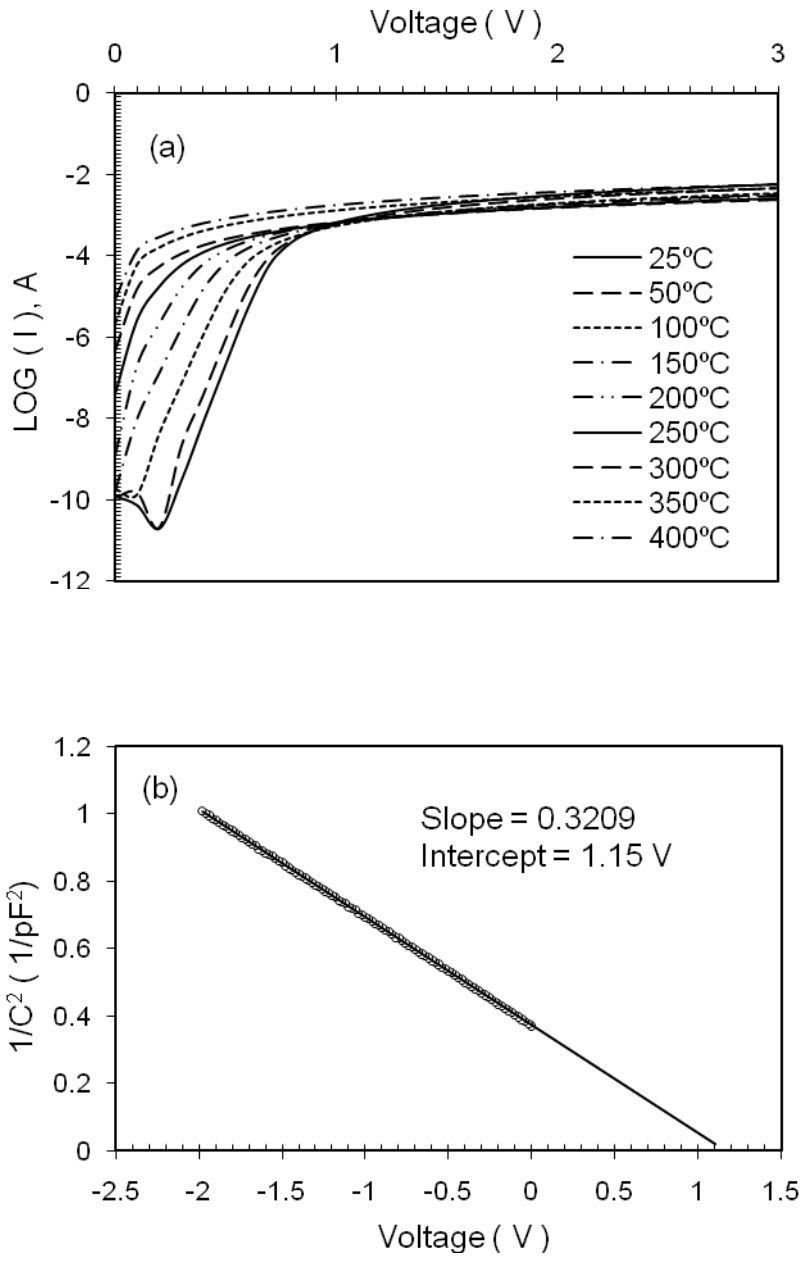



Fig.52. Characteristics of a TmP Schottky contact to n-type AlGaAs from (a) Current-voltage as a function of temperature, and (b) Room temperature capacitance-voltage measurements.

The depth of Fermi level below the conduction band, $V_n$, and the intrinsic barrier height resulting from the static dipole layer, $\Delta\phi$, were 76 meV and 35 meV, respectively. These values were used in determining the barrier height. The doping density extracted from C-V measurements was $2.0 \times 10^{17}$ $cm^{-3}$, in good agreement with the Hall measurement result. Additionally, the measured band gap energy fits the Al composition very well, indicating that DX centers that commonly existed in doped AlGaAs appeared to be negligible in the AlGaAs epilayers due, possibly, to the ultrahigh vacuum growth environment. On the other hand, the ability to decompose the native oxide on AlGaAs and epitaxially grow TmP on top of the AlGaAs is believed to greatly reduce or eliminate surface states and contribute to such a high Schottky barrier height.

As the temperature was ramped up from room temperature to 400°C, the leakage current from a 210 μm x 210 μm TmP/GaAs contact area increased from less than 10 pA to 0.52 mA, respectively. From a Log (I) versus reverse bias plot for TmP/AlGaAs shown in Fig. 53, an almost 6 orders increase in magnitude is observed over this temperature range. It is worth noting that, even at 400°C, the leakage current density was as low as $1.2 \times 10^{-9}$ $A/\mu m^2$, considerably lower compared to the results in the literature for other material systems [22,23]. The Schottky barrier heights and ideality factors at different temperatures were determined and the results plotted versus temperature in Fig. 54. As can be seen in Fig. 54, as the temperature increased from 25°C to 400°C, the SBH remained constant at 1.08 ± 0.02 eV up to 350°C, then increased slightly to 1.12 eV at 400°C. However, due to the uncertainty in the determination from the I-V

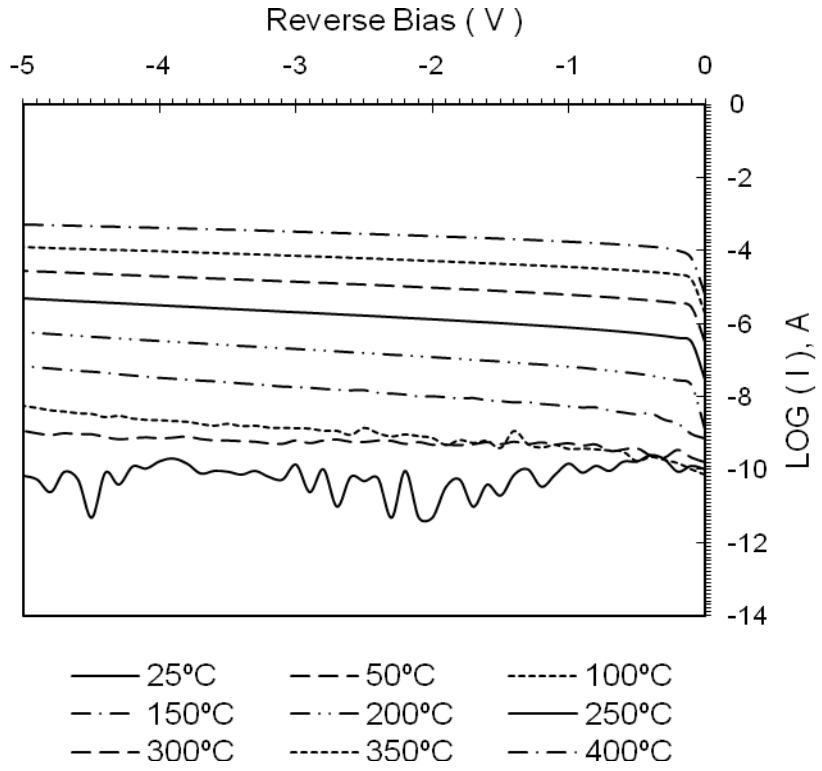



Fig. 53. Current-voltage characteristics of TmP Schottky contacts to n-type AlGaAs under reverse bias at temperatures between 25°C and 400°C.

measurements, this may not be a valid increase. The activation energy associated with the Schottky barrier height as a function of temperature was too high to be calculated in this work. The ideality factor decreased from 1.16 at 28ºC to 1.03 at 200°C most likely due to the higher probability of tunneling electrons overcoming the barrier, indicating that the current is dominated by thermionic emission [1]. For temperatures higher than 200°C, an increase in the ideality factor is thought to be associated with the relatively high doping density in the AlGaAs layer, $1.8 \times 10^{17}$ $cm^{-3}$ in this case. The DX trap centers in n-type AlGaAs can be problematic when the Al composition is greater than 20% [48-52].

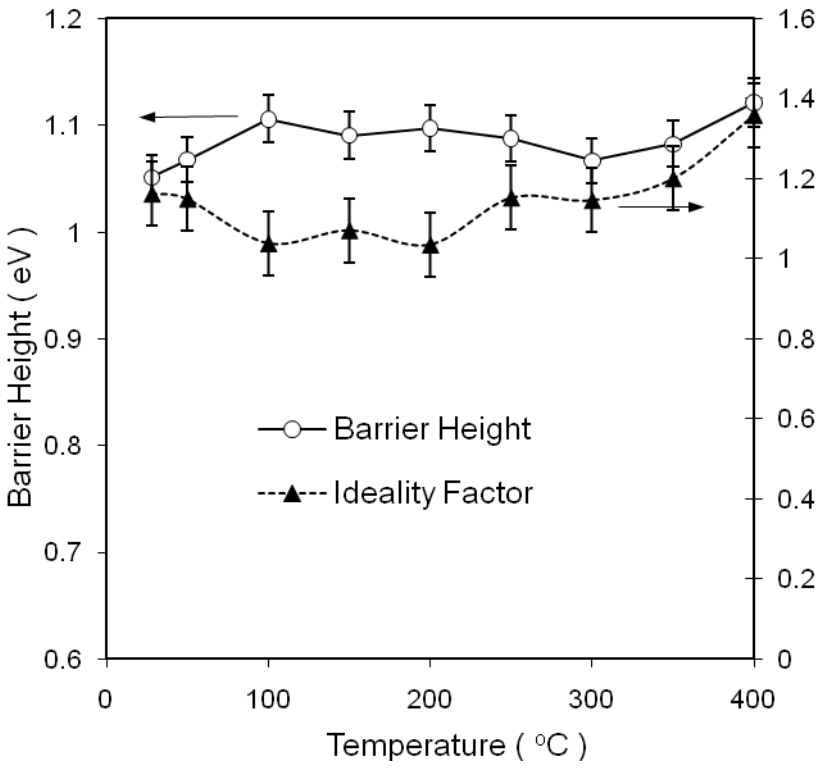



Fig. 54. Schottky barrier heights and ideality factors of TmP Schottky contacts to n-type AlGaAs at temperatures between 25°C and 400°C.

At high temperature, electrons and holes no longer remain in the traps but emit into their respective bands when sufficient thermal energy is supplied. This carrier transfer mechanism through defect-assisted tunneling might explain why the ideality factor was higher than unity at high temperatures.

The stable SBH observed over a wide range of temperatures was in contrast to the results reported for deposited contacts where a strong dependence on temperature as well as oxide thickness was observed [53]. The absence of an oxide at the interface may be responsible for the insensitivity to temperature of the TmP Schottky contact system.

Figs. 55(a) to 57(a) demonstrate the results for the high temperature behavior of Pt and $TiWN_x$ contacts. The extracted SBH and ideality factors as a function of annealing temperature are shown in Figs. 55(b) to 57(b), respectively. As the temperature increases, the turn on voltage of the Schottky barrier (SB) diodes decreases as a consequence of more energetic carriers overcoming the Schottky barrier at higher temperatures than at lower temperatures.

The I-V measurements resulted in a slight increase in barrier heights for Pt, 25% TiWN, and 35% TiWN contact materials as the device temperature increased. Measured temperature coefficient of SBH for Pt, 25% TiWN, and 35% TiWN contact materials are 0.3, 0.14, and 0.16 meV/K, respectively. If the Fermi level pinning is due to MIGS [38], then the temperature dependence of SBH is governed by the temperature dependence of the band gap. In this case the value of temperature coefficient of SBH should be equal to 0.2 meV/K [62].

The ideality factors for all three contacts show a trend of decreasing in magnitude at higher temperatures because thermionic emission tends to take over as the dominant current transport mechanism [1,46]. It is worth pointing out that, for all the Schottky diodes made with deposited contacts, the reverse leakage currents were higher than that for epitaxial TmP at 400°C. Thus, the advantage of using epitaxial Schottky in high temperature applications has been established and confirmed. Fig. 58 (a) and (b) show the high degree of thermal stability of the TmP Schottky to n-type AlGaAs system at 400°C. In Fig. 58 (a), the SBH and ideality factors measured at 25°C were found to be unchanged after annealing at 400°C for 150-hr.

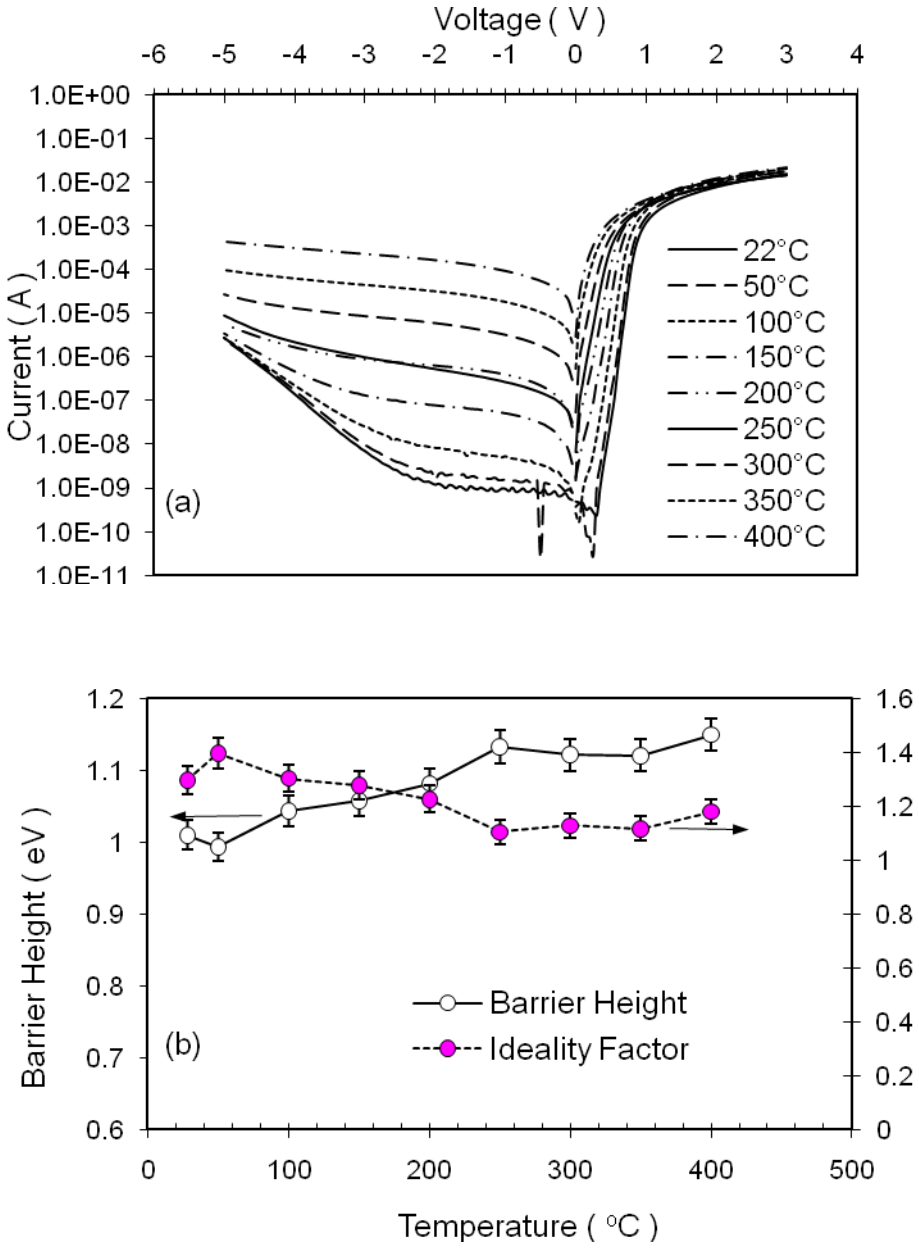



Fig. 55. Temperature behavior of Pt Schottky contacts to n-type AlGaAs demonstrated by (a) Current-voltage characteristics at temperatures between 22°C and 400°C, and (b) extracted Schottky barrier heights and ideality factors as a function of temperature.

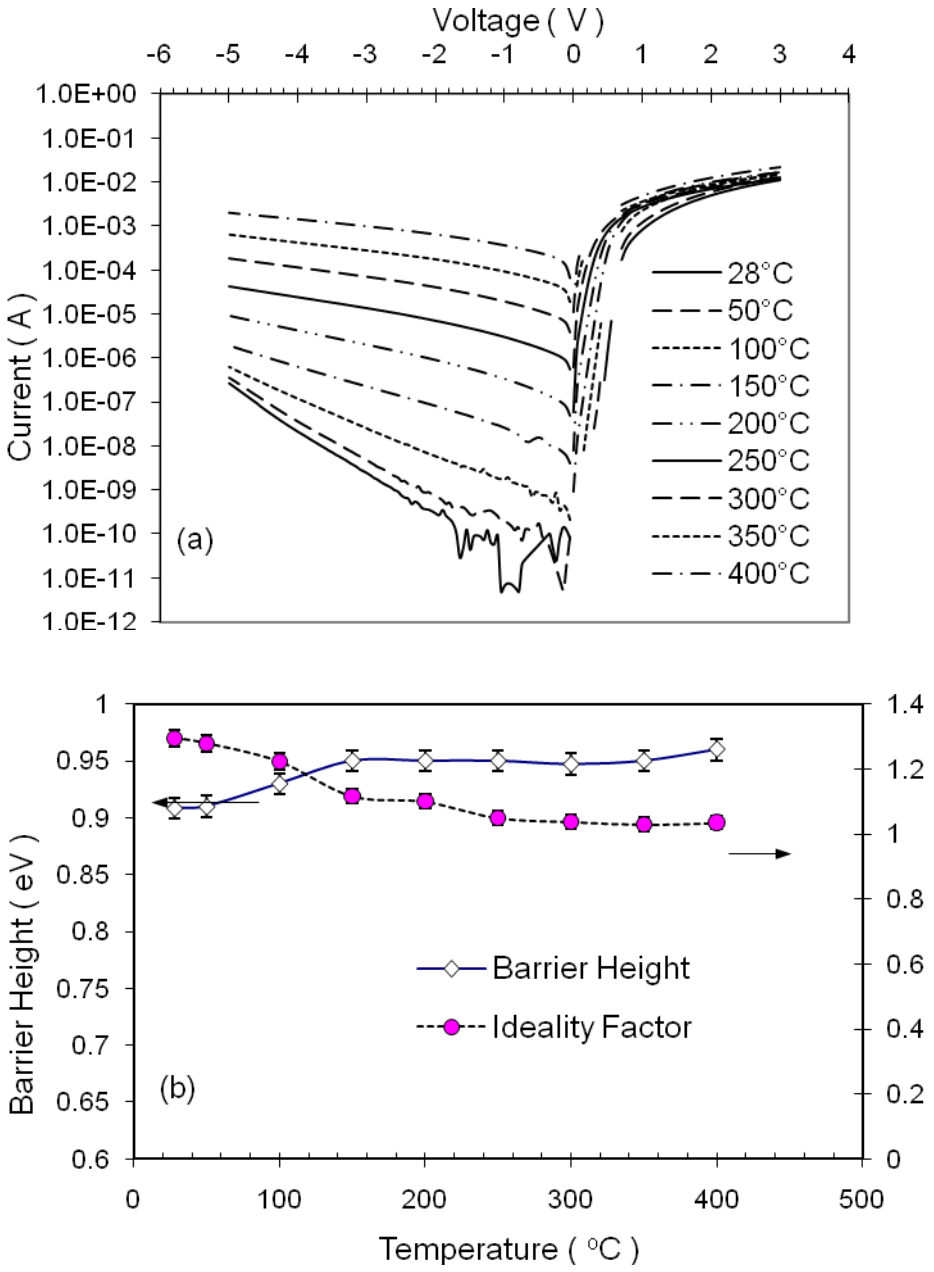



Fig. 56. Temperature behavior of 25% TiWN Schottky contacts to n-type AlGaAs demonstrated by (a) Current-voltage characteristics at temperatures between 28°C and 400°C, and (b) extracted Schottky barrier heights and ideality factors as a function of temperature.

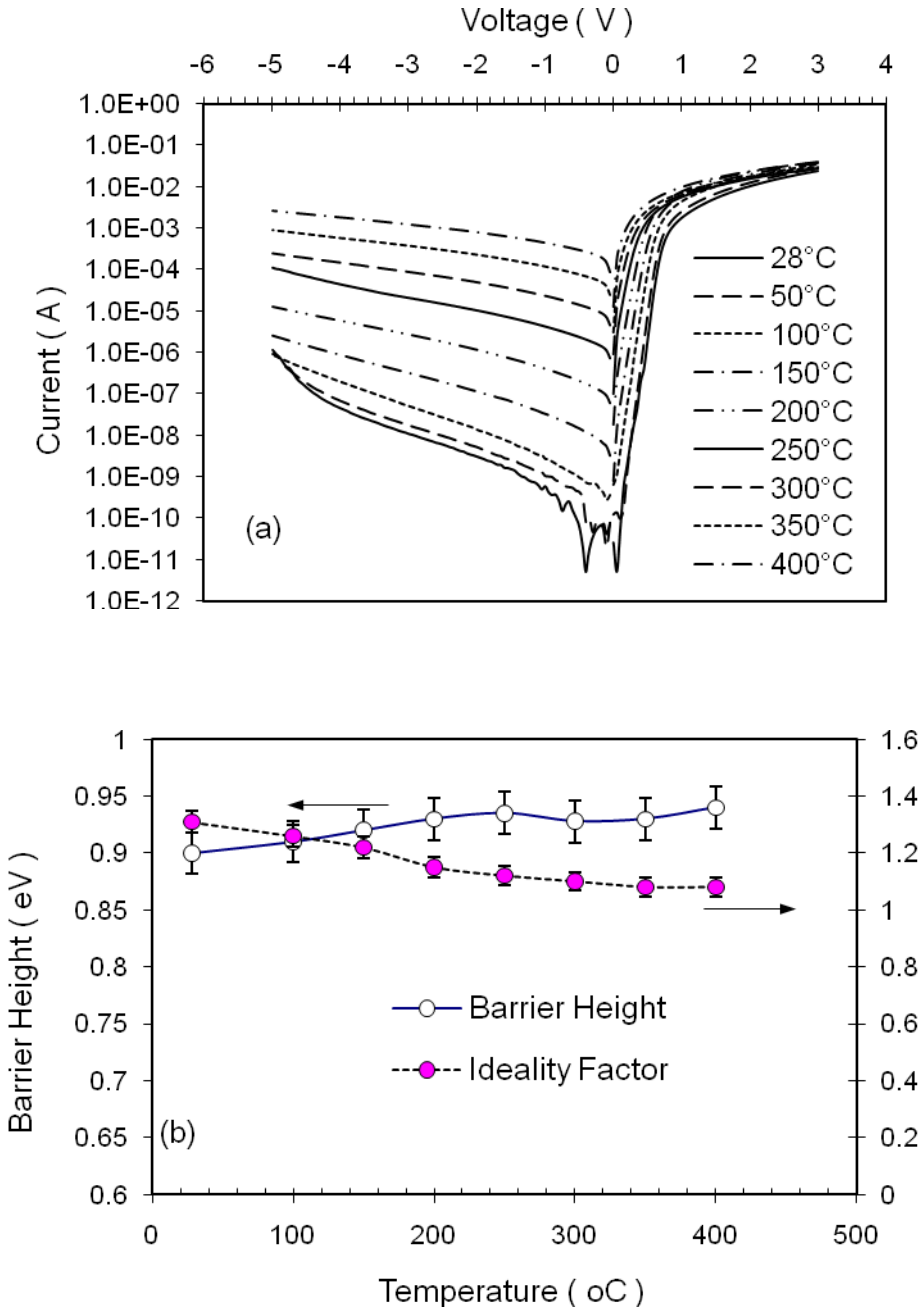



Fig. 57. Temperature behavior of 35% TiWN Schottky contacts to n-type AlGaAs demonstrated by (a) Current-voltage characteristics at temperatures between 28°C and 400°C, and (b) extracted Schottky barrier heights and ideality factors as a function of temperature.

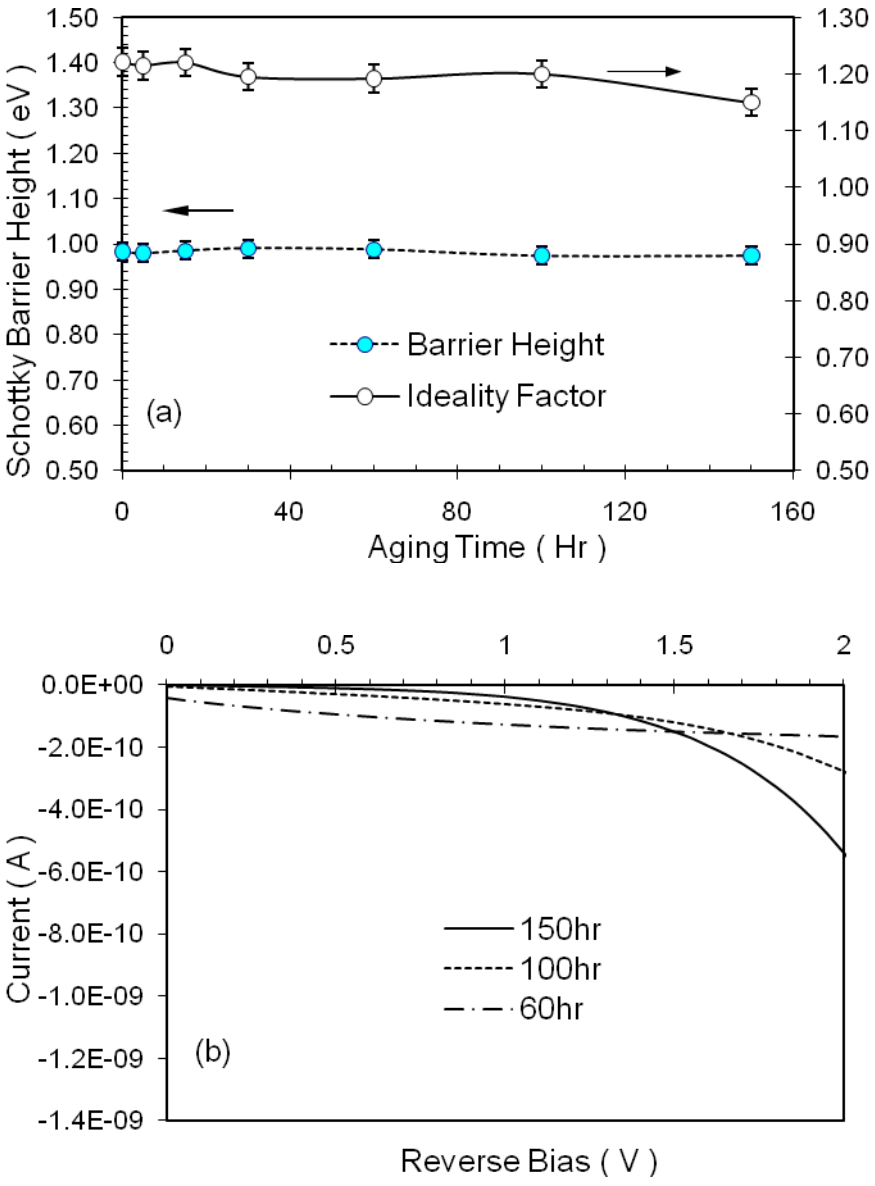



Fig. 58. Temperature behavior of TmP to n-type AlGaAs demonstrated by (a) Schottky barrier heights and ideality factors contacts as a function of annealing time at 400°C, and (b) reverse-biased diode current-voltage characteristics after annealing at 400°C for 60-hr, 100-hr, and 150-hr.

In Fig. 58 (b), the reverse leakage currents measured at 25°C at –2 V were found to be less than $6x10^{-10}$ A.

Fig. 59 is the time-of-flight (TOF)-SIMS depth profile for TmP/n-type AlGaAs contacts after a 400°C/150-hr annealing in untreated air ambient. The relatively high oxygen and impurity levels in the TmP layer probably are from the source materials that are typically 99.999% pure or less in the purity for all available sources.

No sign of oxygen traps or accumulation at the interfaces or AlGaAs epi-layers were observed in the depth profile. In fact, the oxygen concentration decreased at TmP/AlGaAs interface as can be seen in Fig. 59. For deposited contacts, the native oxide at the metal-AlGaAs interface is difficult to avoid especially for practical production contacts and devices.

The formation of wide bandgap materials such as GaP ($E_g$ = 2.26eV) during the TmP growth may be responsible for such a high barrier height although such formation is not observable or distinguishable in Fig. 59. The high barrier height may be attributed to the reduction of the effective doping density of n-AlGaAs during the growth if the Tm atoms tend to reside on group-III sites and act as acceptors in AlGaAs. Such a low leakage current density for epitaxial TmP Schottky contacts to n-type AlGaAs is an expected result indicating the excellent performance potential for use in FET devices at high temperatures.

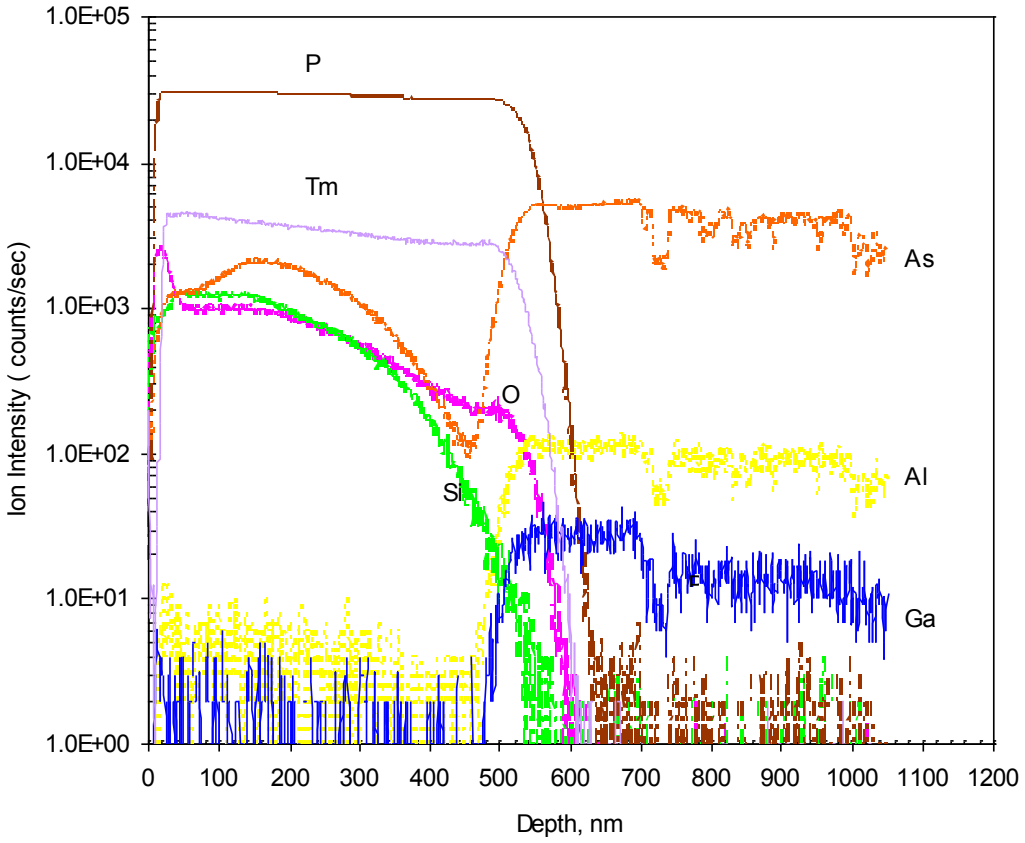



Fig. 59. TOF-SIMS depth profile of TmP grown on n-type AlGaAs by MBE.

## 4.7 $TiWN_x$ Schottky contacts to undoped LT-AlGaAs and AlAs materials

LT-AlGaAs layers were grown at 300°C and 350°C on top of a channel layer and sandwiched by two high temperature (HT)-AlAs layers using MBE. Both the AlAs and AlGaAs epilayers were intentionally not doped for the initial interest in the fabrication of MISFET devices. $TiWN_x$ contacts were deposited with the same procedures described in section 4.5.3, followed by annealing in a $N_2$ ambient at 350°C for 10 min. $Cu_3Ge$ ohmic contacts were first etched in

windows through AlAs and LT-AlGaAs layers and then deposited right on top of the n-GaAs channel layer. Metallization was carried out at 400°C for 15 min in forming gas.

Figs. 60 (a) and (b) show the current-voltage characteristics, along with the I-V characteristics of the ohmic contact, for TiWN contacts to LT-AlGaAs grown at 300°C and 350°C, respectively. Fairly good conduction was found for diodes under forward bias, while extremely low leakage currents, approaching the lower limit of the measurement equipment, were observed under reverse bias for both growth temperature cases.

Typical leakage currents were in the range of 10 pA to 100 pA at room temperature. The forward I-V curves in the low field region did not follow the Schottky diode equation or other models for tunneling junctions.

$TiWN_x$ Schottky contacts to undoped LT-AlGaAs grown at 300°C and to AlAs barriers which is grown beneath the LT-AlGaAs had almost identical I-V characteristics. A slight difference in the I-V curves was found between the $TiWN_x$/LT-AlGaAs(350°C) and the $TiWN_x$/AlAs systems, with the latter having a higher current than the former one at forward voltages higher than 1.5 V. The interface roughness scattering [61] is thought to play an important role as the quality of AlAs grown on top of LT-AlGaAs will not be as perfect as the AlGaAs epitaxial layer. Fig. 61(a) shows the current/voltage$^2$ versus 1/voltage characteristics, known as a Fowler-Nordheim (F-N) plot [59], for $TiWN_x$ Schottky contacts to undoped LT-AlGaAs and AlAs materials. Fowler – Nordheim tunneling has been studied extensively in metal-oxide-semiconductor (MOS) structures

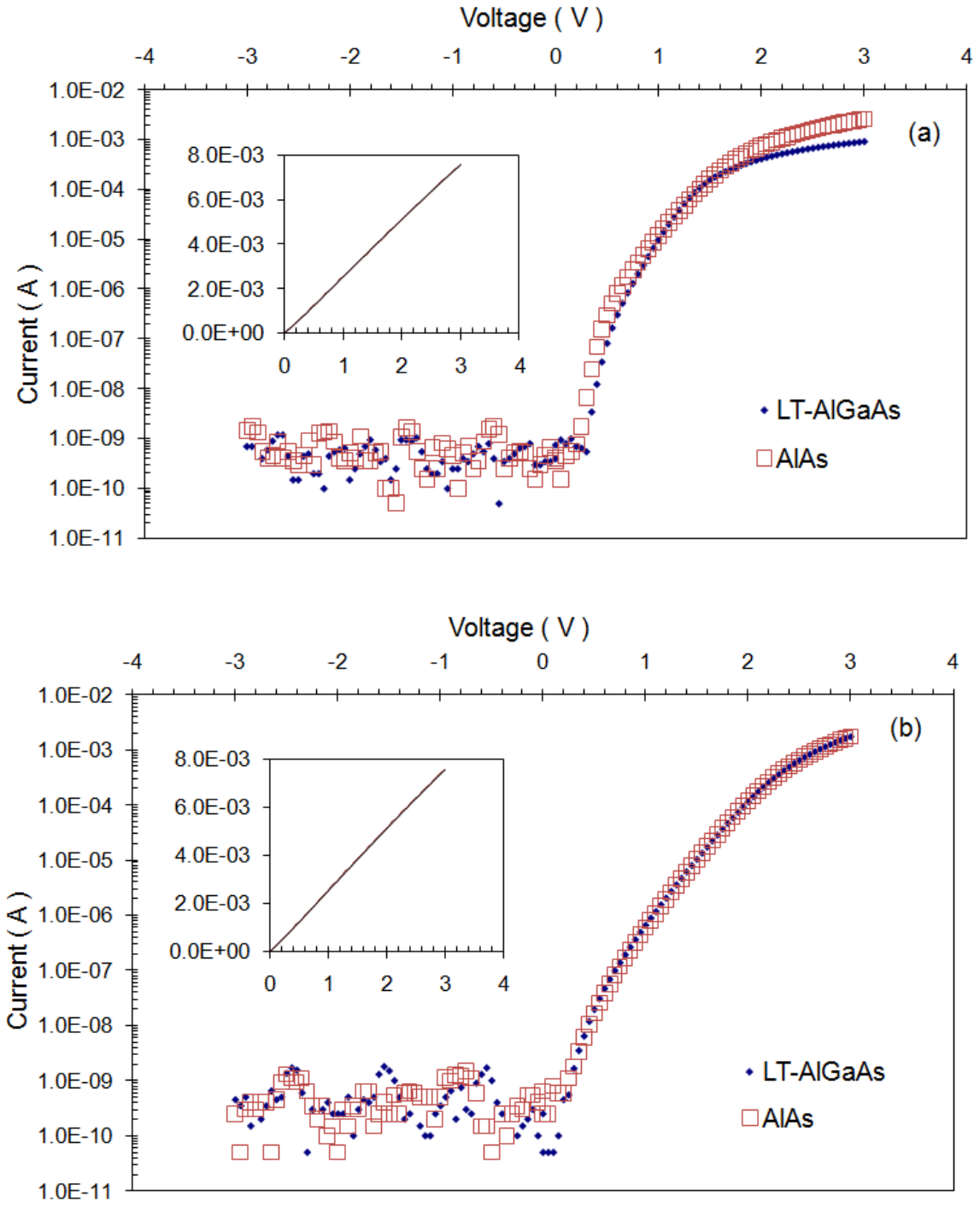



Fig. 60. Current-voltage characteristics of TiWN Schottky contacts deposited on LT-AlGaAs with an Al composition of 30% grown at (a) 350°C and (b) 300°C. The insert shows the I-V curve resulting from electrical connections between two ohmic contacts.

where it has been shown to be the dominant current mechanism, especially for thick oxides [59].

At voltages higher than 1.0 V, region A in Fig, 61, the current transport through $TiWN_x$ Schottky contacts to LT-AlGaAs grown at 300°C and 350°C was found to be dominated by the F-N mechanism because of the good linear fit obtained in this region. However, the current flowing in the $TiWN_x$ contacts to LT-AlGaAs grown at 350°C was approximately 2 orders of magnitude higher than that of the $TiWN_x$ contacts to LT-AlGaAs grown at 300°C. This difference of ~ 2 orders of magnitude can be attributed to the high resistivity of LT-AlGaAs grown at 300°C which is approximately 2 times higher than the resistivity of LT-AlGaAs grown at 350°C.

Fig. 61(b) shows the Log (I) versus voltage$^{1/2}$ characteristics, known as a Frenkel-Poole (F-P) plot [60], for $TiWN_x$ Schottky contacts to AlAs and LT-AlGaAs. Frenkel-Poole emission was used to define the conduction process in insulators when carrier transport is due to field–enhanced thermal excitation of trapped electrons into the conduction band. In the F-P plot, a linear fit is shown for $TiWN_x$ Schottky contacts to AlAs and LT-AlGaAs grown at 300°C for the voltage range from 0.5 V to 2.0 V. However, for $TiWN_x$ Schottky contacts to AlAs and LT-AlGaAs grown at 350°C, it is hard to define a linear region where the F-P mechanism dominates. LT-AlGaAs grown at 300°C is expected to have more defects (or traps) than AlGaAs grown at 350°C; thus, these results directly support a mechanism involving the thermal excitation of electrons from traps into the conduction band of the insulator [57].

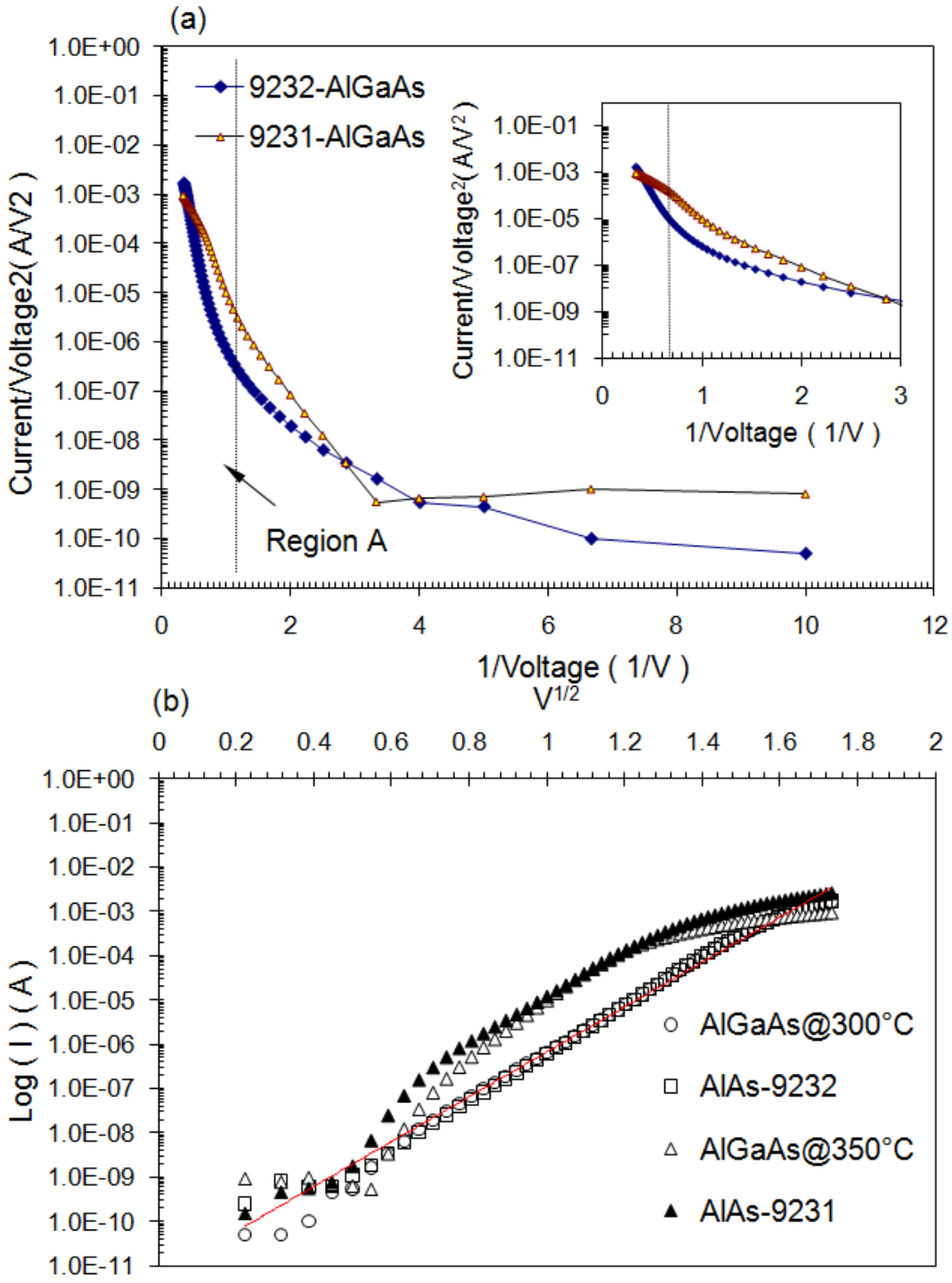



Fig. 61. Determination of the current mechanism for TiWN contacts to LT-AlGaAs and TiWN contacts to AlAs grown at normal growth temperatures between 600°C and 630°C on top of LT-AlGaAs using (a) Fowler-Nordheim and (b) Frenkel-Poole plots.

## 4.8 Conclusion

In MESFET devices, reverse leakage currents of the gate Schottky diode are dominated by tunneling through the lowered energy barrier, due to image forces, between the metal/semiconductor interfaces. The Schottky barrier heights can be enhanced by increasing the Al composition in the gate contact layers due to the increase in band gap energies. For deposited contacts, the MIGS model appears to be suitable and can be used to predict the barrier of metal/ $Al_xGa_{1-x}As$ interfaces.

The low-power consumption operation at elevated temperatures cannot be achieved without the engineering of the buffer layers in GaAs-technology known as the “back-wall barrier.” Together with the “gate barrier engineering,” a reliable operation at 400°C for GaAs-based electronics is feasible. Grain boundaries serve as the sink of atoms and fast diffusion paths allowing reactions, contamination and electromigration to take place [47].There is no doubt that current transport through these defects will be much easier than that in the monocrystalline materials. Thus, to reduce or eliminate these easy current transports through defects, the contacts should be ultimately monocrystalline and epitaxial. Thulium phosphide (TmP) has demonstrated excellent performance as a promising Schottky contact for high-temperature operations. Other rare-earth compounds, i.e., arsinides and phosphides, having material properties similar to that of TmP, will be potential candidates for high-temperature applications.

## 4.9 References


1. S. M. Sze, Physics of Semiconductor Devices, 2nd ed., Wiley, New York, 1981.

2. E. H. Rhoderick amd R. H. Williams, Metal-Semiconductor Contacts, 2nd ed., OUP, New York, 1988.

3. W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, Phys. Rev. Lett. (1981) 2342.

4. C. R. Crowell, J. C. Sarace, and S. M. Sze, Trans. Met. Soc., AIME (1965) 233.

5. J. O. McCaldin, T. C. McGill, and C. A. Mead, J. Vac. Sci. Technol. 13 (1976) 802.

6. A. M. Goodman, J. Appl. Phys. 34 (1963) 329.

7. J. Wurfl, J. K. Singh, and H. L. Hartnagel, IEEE Reliab. Phys. 28th Annual Proc. 1990, p. 87.

8. C. P. Chen, Y. A. Chang, J. W. Huang, and T. F. Kuech, Appl. Phys. Lett. 64(11) (1994) 1413.

9. H. Nakamura, Y. Sano, T. Nonaka, T. Ishida, and K. Kaminishi, IEEE GaAs IC Symp. Tech. Digest, 1983, p. 134.

10. S. P. Kwok, J. Vac. Sci. Technol. B4 (1986) 1383.

11. Y. Sekino, T. Kimura, K. Inokuchi, Y. Sano, and M. Sakuta, Jpn. J. Appl. Phys. 27 (1988) L2183.

12. C. P. Chen, Y. A. Chang, and T. F. Kuech, J. Appl. Phys. 77(9) (1995) 4777.

13. C. P. Chen, Y. A. Chang, and T. F. Kuech, J. Appl. Phys. 77(9) (1995) 1915.

14. S. A. Chambers, J. Vac. Sci. Technol. B7 (1989) 737.

15. C. P. Chen, Y. A. Chang, and T.F. Keuch, Appl. Phys. Lett. 64 (1994) 3485.

16. T. Sand, W. K. Chan, C. C. Chang, E. W. Chase, and V. K. Keramidas, Appl. Phys. Lett. 52 (1988) 1388.

17. T. Lalinsky, D. Gregusova, Z. Mozolava, J. Breza, and P. Vogricic, Appl. Phys. Lett. 64(14) (1994) 1818.

18. T. S. Huang, J. G. Peng, and C. C. Lin, Appl. Phys. Lett. 61 (1992) 3017.

19. T. S. Huang, J. G. Peng, and C. C. Lin, J. Vac. Sci. Technol. B11 (1993) 756.

20. T. S. Huang and J. G. Pang, J. Appl. Phys. 78(9) (1995) 5739.

21. L. P. Sadwick, Appl. Phys. Lett. 64(1) (1994) 79.

22. C. D. Wilson, A. G. O'Neill, S. M. Baier, and J. C. Nohava, IEEE Trans. Electron. Devices (1996) 201.

23. C. D. Wilson and A. G. O'Neill, Trans. 2nd HiTEC, Charlotte, NC, 1994, p. V-15.

24. J. M. Woodall, P. D. Kirchner, J. L. Freeouf, D. T. McInturff, M. R. Melloch, and F. H. Pollak, Philos. Trans. Royal Soci. A. 344(1673) (1993) 521.

25. H. Chen, L. P. Sadwick, M. Sokolich, K. L. Wang, R. D. Larson, and T. Y. Chi, J. Vac. Sci. Technol. B7(5) (1989) 1096.

26. L. C. Zhang, S. K. Cheung, C. L. Liang, and N. W. Cheung, Appl. Phys. Lett. 50 (1987) 445.

27. K. Okamoto, C. E. C. Wood, and L. F. Eastman, Appl. Phys. Lett. 38(8) (1981) 1116.

28. K. Steiner, H. Mikami, K. Nishihori, M. Nagaoka, and N, Uchitomi, J. Vac, Sci. Technol. B 9(3) (1991) 1601.

29. C. Ghezzi, E. Gombia, and R. Mosca, J. Appl. Phys. 70(1) (1991) 215.

30. J. H. Baek, M. Shur, R. R. Daniels, D. K. Arch, J. K. Abrokwah, and O. N. Tufte, IEEE Electron. Device Lett. Vol.EDL-7, 9 (1986) 519.

31. T. J. Miller and M. I. Nathan, Appl. Phys. Lett. 61(19) (1992) 2332.

32. M. Eizenberg, M. Heiblum, M. I. Nathan, N. Braslau, and P. M. Mooney, J. Appl. Phys. 61(41) (1987) 1516.

33. C. Meva'a, X. Letartre, P. Rojo-Romeo, and P. Viktorovitch, Solid State Electron. 41(6) (1997) 857.

34. S. Tiwari and D. J. Frank, Appl. Phys. Lett. 60(5) (1992) 630.

35. R. Narasimhan, L. P. Sadwick, and R. J. Hwu, IEEE Trans. of Electron. Devices 46 (1999) 24.

36. M. S. Daw and D. L. Smith, Appl. Phys. Lett. 36(8) (1980) 690.

37. R. E. Allen and J. D. Dow, Phys. Rev. B 25(2) (1982) 1423.

38. J. Tersoff, Phys. Rev. B 32(10) (1985) 6968.

39. M. Missous, W. S. Truscott, and K. E. Singer, J. Appl. Phys. 68(5) (1990) 2239.

40. M. Werner, R. Job, A. Denisenko, A. Zaitsev, WR. Fahrner, C. Johnson, P. R. Chalker, and I. M. Buckley-Golder, Diamond and Related Materials 5(6-8) (1996) p. 723.

41. D. G. Teer and K. C. Laing, CEP Consultants Ltd. Edingburgh, UK, 1991, p. 202.

42. T. Fukada, M. Hasegawa, T. Mori, Y. Toyoda, and T. Mikami, Jpn. J. Vac. Soc. 38(11) (1995) 955.

43. T. Hauzer, D. B. Lewis, J. S. Brooks, and W. D. Munz, Surf. And Coat. Technol. 76(1-3) (1995) 159.

44. Kun-Chuan Lin, Edward. Chang, Sheng-Ping Wang, Yeong-Lin Lai and Chun-Yen Chang, Jpn. J. Appl. Phys. 33 (1994) 4546.

45. G. Myburg, F. D. Auret, W. E. Meyer; C. W. Louw, M.J. van Staden, Thin Solid Films 325(1-2) (1998) 181.

46. G. Myburg, F. D. Auret, W. E. Meyer, H. Burger, Thin Solid Films 249(1) (1994) 95.

47. L. P. Sadwick, P. P. Lee, M. Patel, M. Nickols, R. J. Hwu, J. E. Shield, D. C. Streit, D. Brehmer, K. McCormick, S.J. Allen, and R.W. Gedridge, J. Cryst. Growth (1996) 4843.

48. G. S. Gargill; A. Segmuller, T. N. Theis, Mater. Chem. Phys. 42(2) (1995) 138.

49. S. Ghosh and V. Kumar, Solid State Commun. 98(2) (1996) 195.

50. S. Ghosh and V. Kumar, Solid State Commun. 104(12) (1997) 781.

51. Y. B. Jia, H. G. Grimmeiss, Solid State Commun. 101(10) (1997) 771.

52. M. Baj, L. H. Dmowski, J. Phys. Chem. Solids, 56(3-4) (1995) 589.

53. V. Krozer, M. Ruppert, J. M. Miao, W. Y. Lee, and M. Schubler, Proc. 2nd Int. HiTEC, Charlotte (1994) IV9.

54. C. Canali, F. Magistrali, M. Sangalli, C. Tedesco, and F. Marchetti, Proc. 29th Int. Relia. Phys. (1991) 206.

55. S. Yoshida, S. Misawa, S. Gonda, J. Appl. Phys. 53 (1982) 6844.

56. J. S. Lin, Ph. D. Thesis, in press.

57. J. Frenkel, Phys. Rev. 54 (1938) 647.

58. E. Geissberge, R. A. Sader, M. L. Balzan, and J. W. Crittes, J. Vac. Sci. Technol. B5(6) (1987) 1701.

59. R. H. Fowler and Dr. L. Nordheim, Electron Emission in Intense Electric Fields, Proc. Royal Soc. London, 119 (1928) 173–181.

60. J. Frenkel, Technol. Phys. USSR, 5 (1938) 685.

61. P. Roblin, R. C. Potter, and A. Fathimulla, J. Appl. Phys. 79(5) (1996) 2502–2508.

62. H. W. Hubers and H. P. Roser, J. Appl. Phys. 84 **(**1998) 5326.

63. R. Brunwin B. Hamilton, P. Jordan and A.R. Peaker, Electron. Lett. 15 (1979) 34.

64. B. Hamilton et al., J. Appl. Phys. vol. 50 (1979) 637.

# CHAPTER 5

# HIGH TEMPERATURE ELECTRONIC DEVICES

## 5.1 Device configuration

Ion implantation has proved to be a successful method to achieve high resistivity layers for various fabrication steps in III-V semiconductor device technology [1]. High energy ion bombardment with light ions — hydrogen (H), helium (He), beryllium (Be), boron (B), nitrogen (N), and oxygen (O) — is a very attractive method to obtain interdevice electrical isolation for GaAs-based integrated circuits. The drawback accompanying such a high-energy process is that implantation-induced deep level defects can not be completely bleached and eliminated [2,3]. These defects are believed to be mobile at 520K [4,5] and will be potential leakage paths due to the imperfections that they cause inside the crystal.

By appropriate selection of implant species, typical room temperature leakage currents between ohmic contacts isolated by proton (H) bombardment are in the $10^{-9}$A range. When characterizing the high temperature performance of gate contacts, the leakage from and between contact pads might be greater than that flowing through the gates inside the active region if the contact pads are not isolated.

In this dissertation, a novel approach for device isolation to eliminate almost any and all additional electrical contact and connection to the substrate was developed to overcome the deficiency of proton bombardment approach. It is a hybrid technique that combines both mesa isolation and dielectric isolation using PECVD $Si_3N_4$ as the insulation layer and Cr or Ti/Au as the adhesion layers. Figs. 62(a) and (b) show the photographs of a device fabricated by the technique mentioned above with (a) before and (b) after gate metallization. The device processing starts from a wet etching for mesa isolation, followed by deposition of $Si_3N_4$ using PECVD at 300°C. The dielectric strength in terms of the leakage current of the $Si_3N_4$ grown at 300°C was characterized and found to be around 4 nA/μm at 10V at 400°C, indicating that the film quality was good and the leakage current was quite negligible for high temperature applications.

The adhesion layers, either Ti/Au or chromium (Cr), having a thickness of 3000Å, were deposited using sputtering. Prior to the metallization, contact windows were opened using carbon tetraflouride ($CF_4$) plasma etching at a power level of 50 W for which photolithography patterning of the device structures to create the contact window locations had been performed prior to the plasma etching. Next, ohmic contacts consisting of Cu and Ge layers were sequentially deposited using e-beam evaporation. The mesa isolation region was left typically 30-50 μm wider than the contact width for positioning the gates inside the spacing between the drain and source. Without the extra spacing, it is very difficult to develop a 2 μm gate having a trench depth of more than 1.5 μm. It should be noted that gate adhesion metal runs from the insulating layer down

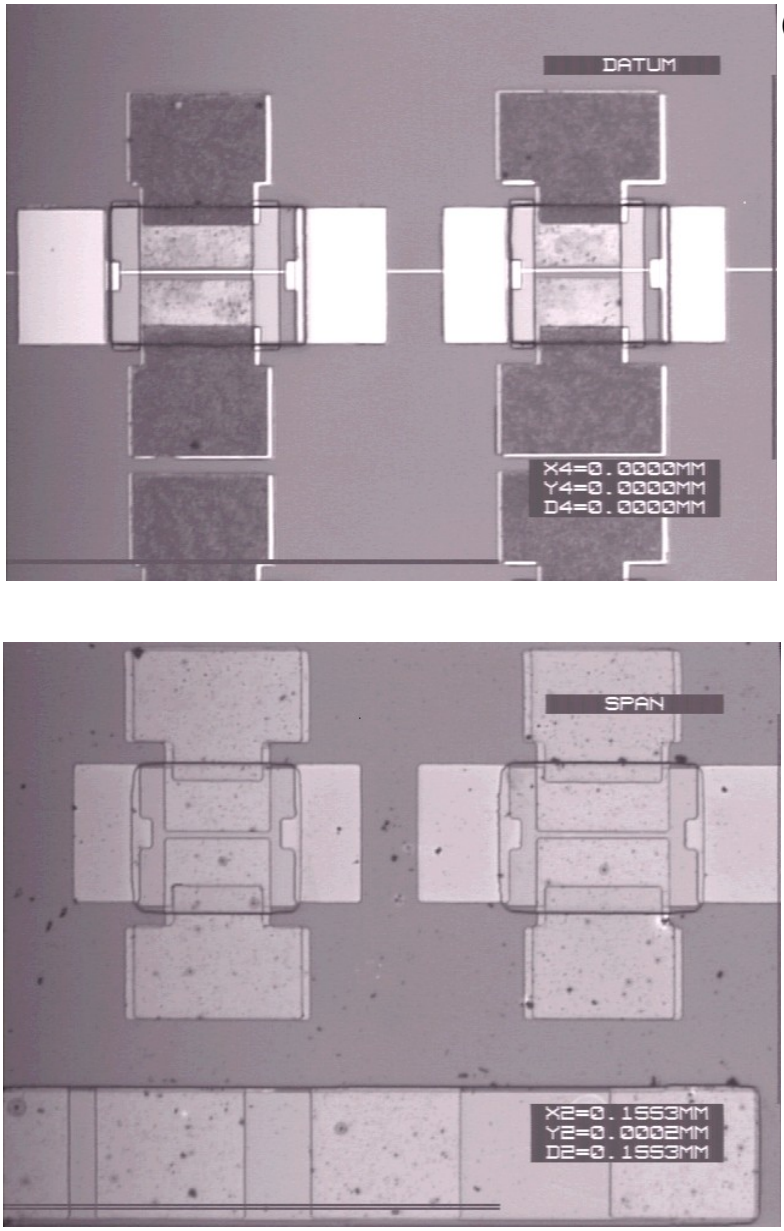



Fig. 62. Photographs of the heterojunction MESFETs; (a) before and (b) after the gate metal deposition. The TLM patterns are also shown on the bottom of photograph (a).

to the mesa which most likely forms a Schottky contact to the top semiconductor surface. Current flows directly between gate adhesion metals and the ohmic contacts. The device surface thus has an unguarded region that needs to be well defined. A second wet etching was conducted to remove the unguarded region on the mesa. The two etch windows that run across the length of mesa were defined by photoresist and then the semiconductor materials were wet etched to the same depth as that of the mesa isolation.

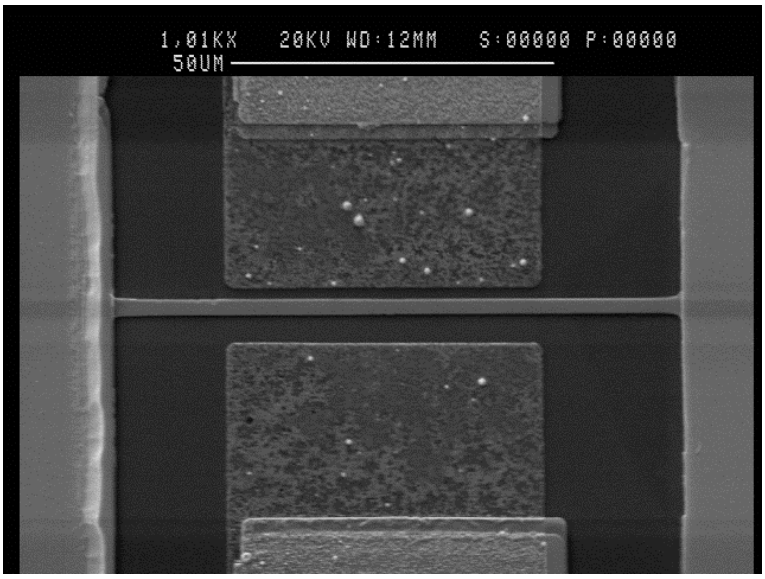
Figs. 63 (a) and (b) show the photographs near the center of active region before and after the second etching, respectively. It is clear that the gates now are suspended between the trench and adhesion layers after the trench etching. The performance of the device due to this wet etching process is quite different than without the wet ecthing process. The $I_d$-$V_{ds}$ characteristics at 300°C for representative GaAs-MESFETs are shown in Fig. 64(a) and (b), while the gate current $I_g$-$V_{ds}$ characteristics are shown in Fig. 65(a) and (b). The early voltage breakdown seen in Fig. 64(a) in devices without the second etching is corrected by the deep trench etch which eliminates the gate leakage path to the substrate as evidenced by the I-V characteristics shown in Fig. 64(b). The leakage and pinch-off characteristic are poor in devices without the second etching.

## 5.2 Heterojunction MESFET and JFET

### 5.2.1 Structure design

The structures of heterojunction MESFET and JFET used in this dissertation work are listed in Table 6 and show the sequence of MOCVD epitaxy

(a)




(b)

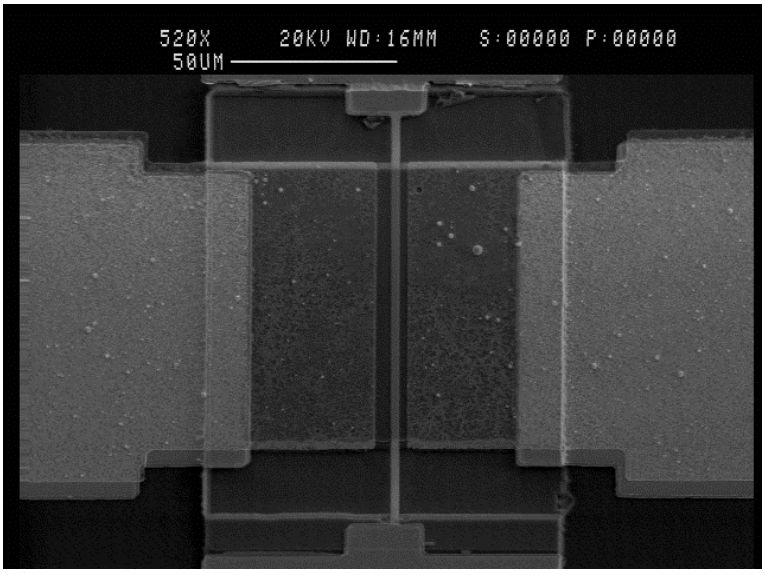



Fig. 63. Photographs for a heterojunction MESFET shown near the active region of the device; (a) before and (b) after the trench etching.

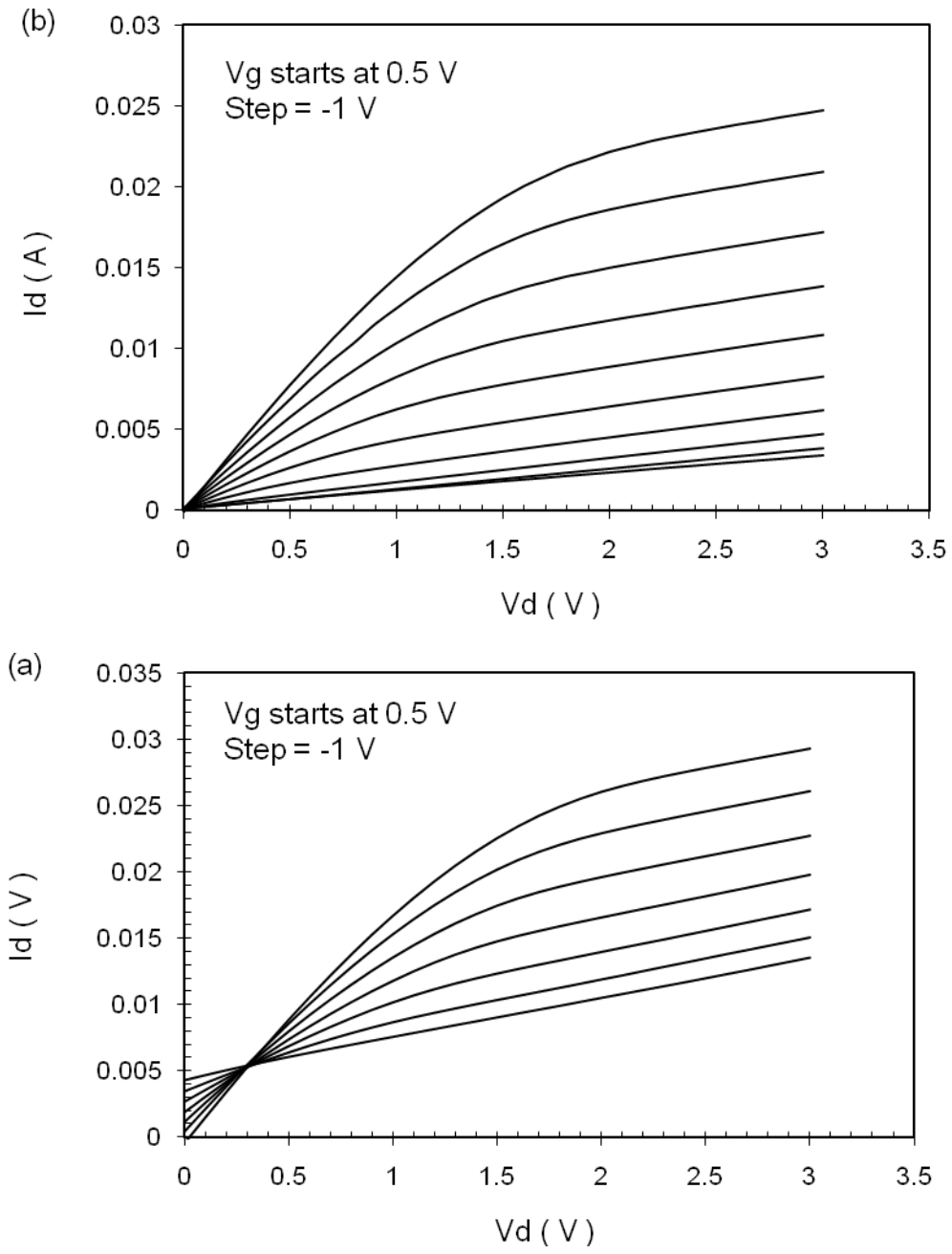



Fig. 64. $I_d$ -$V_{ds}$ characteristics at 300°C for a representative GaAs-MESFET with (a) shallow trench separation and (b) deep trench separation.

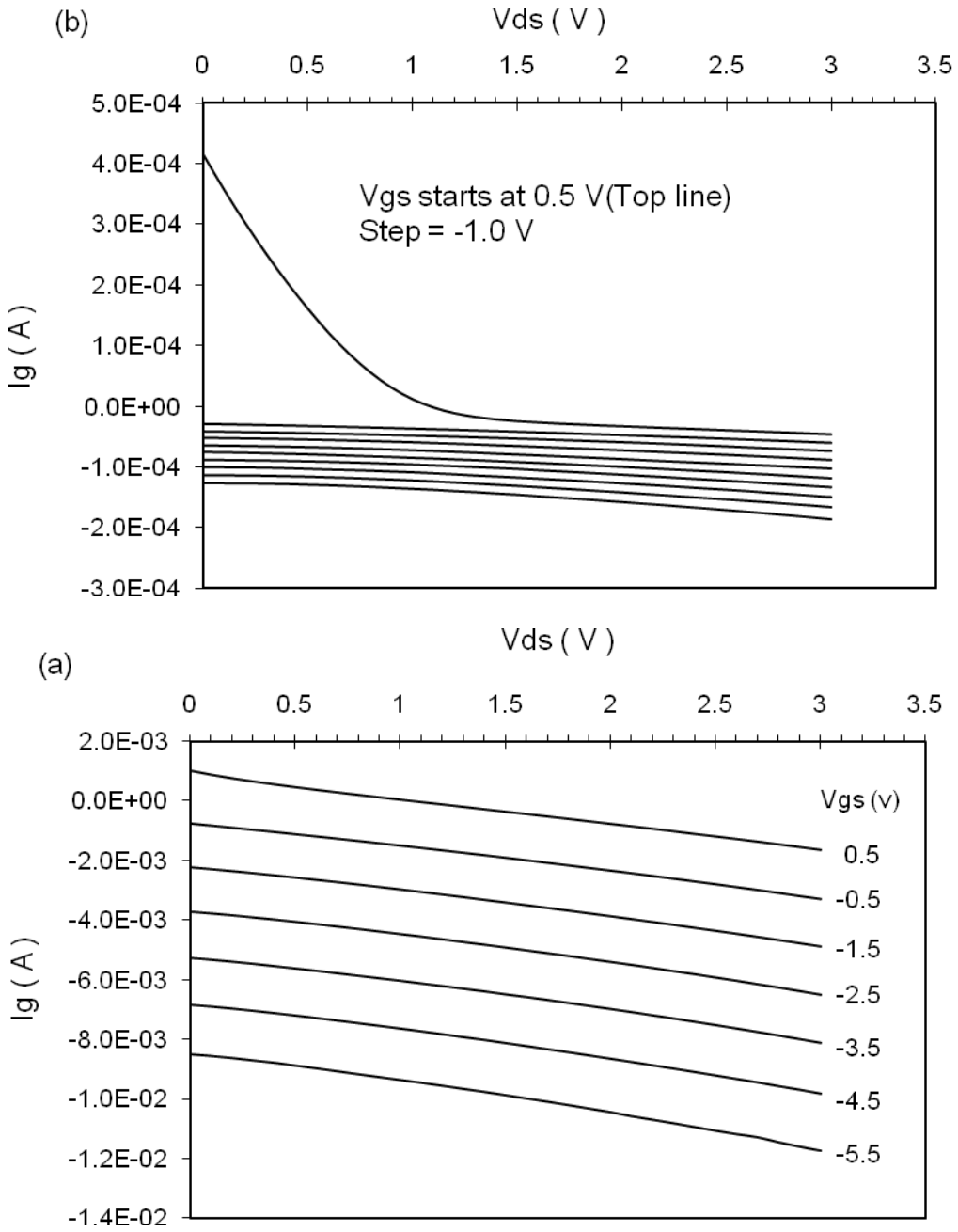


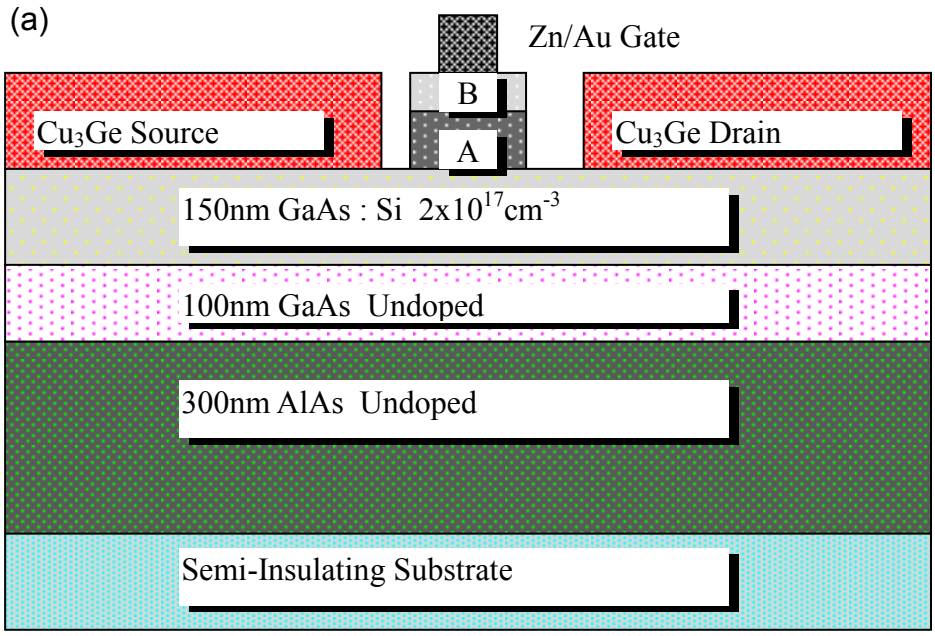

Fig. 65. $I_g$ -$V_{ds}$ characteristics at 300°C for a representative GaAs-MESFET with (a) shallow trench separation and (b) deep trench separation.

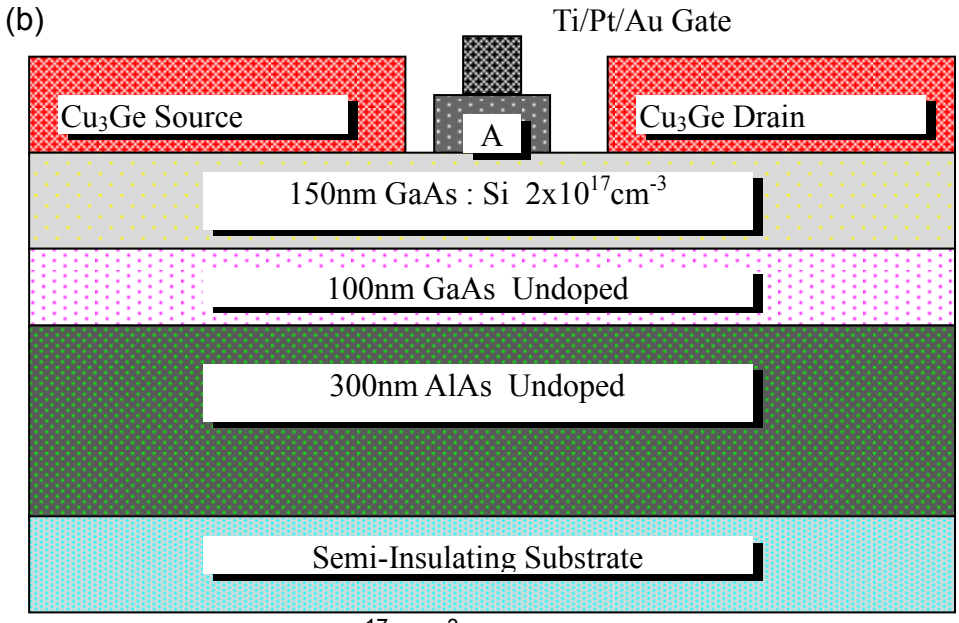
Table 6. Profile of heterojunction field effect transistor structures with an AlAs buffer layer.

| | | | |
|---|---|---|---|
| *iGaAs* | 10nm | | |
| *pAlGaAs* | 50nm | C : $2x10^{18}cm^{-3}$ | 30% Al |
| *nAlGaAs* | 100nm | Si : $4x10^{17}cm^{-3}$ | 30% Al |
| *nGaAs* | 150nm | Si : $2x10^{17}cm^{-3}$ | |
| *iGaAs* | 100nm | | |
| *iAlAs* | 300nm | | |
| *iGaAs* | 200nm | | Buffer |
| *S.I. GaAs* | 300μm | | Substrate |

growth. Carbon was chosen as the p-type dopant because of its exceptional low diffusivity compared to other doping elements [6].

The device reliability may be improved if there is less intermixing between dopants and contact materials. For JFETs, the Zn/Au ohmic contacts with a thickness of 5 nm/150 nm were deposited onto p-type AlGaAs by sputtering. Annealing of this ohmic contact was carried out in a furnace under forming gas environment, together with the Cu/Ge ohmic contacts. The contact resistance was measured to be of the order of 0.5 Ωmm by TLM for Zn/Au to p-type AlGaAs. For MESFETs, the Schottky gate contacts were deposited onto the n-type AlGaAs using sputtering. Fig. 66 shows the side-view of an as-finished heterojunction JFET and MESFET after completion of the process steps mentioned above.




A. 100nm AlGaAs : Si $3x10^{17}$ $cm^{-3}$

B. 50nm AlGaAs : Zn $3x10^{18}$ $cm^{-3}$

Fig. 66. The side-view of a heterojunction (a) JFET and (b) MESFET.

The JFET should have less reverse leakage current than that of the MESFET due to the higher built-in potential pn semiconductor junction gate barrier compared with the barrier height of the Schottky metal semiconductor junction of the MESFET. The purpose of the AlAs epilayer is to reduce the substrate leakage current. The undoped GaAs epilayer inserted in between the AlAs and the channel layer is found to improve the pinch-off characteristics at elevated temperatures [7].

For comparison, a layer of n-type GaAs with a thickness of 100 nm and a doping density of $2.3 \times 10^{17}$ $cm^{-3}$ was grown on a semi-insulating (SI) GaAs substrate. All processing steps were kept the same as those that had been applied to the HFET structure.

### 5.2.2 Device performance

#### 5.2.2.1 Monolithic GaAs MESFET

Fig. 67 shows the $I_d$ versus $V_{ds}$ characteristics at room temperature, 200°C, and 300°C, respectively, for a representative MESFET using $Cu_3Ge$ as the ohmic contacts and TiPtAu as the gate contacts. The device showed severe degradation of the pinch-off characteristics. The drain current on-off ratios at $V_{ds}$ = 5V, defined as the drain current at zero gate voltage divided by drain current at pinch-off (which is –4V in this case), decreased from $3 \times 10^5$ at room temperature to 30 at 200°C, and then to ~ 5 at 300°C. The gate diode had a weak ability for carrier modulation at high temperatures because its Schottky barrier height is only 0.85 eV as characterized and measured from forward voltage I-V curves. The increased conductivity of the semi-insulating substrate at high temperatures

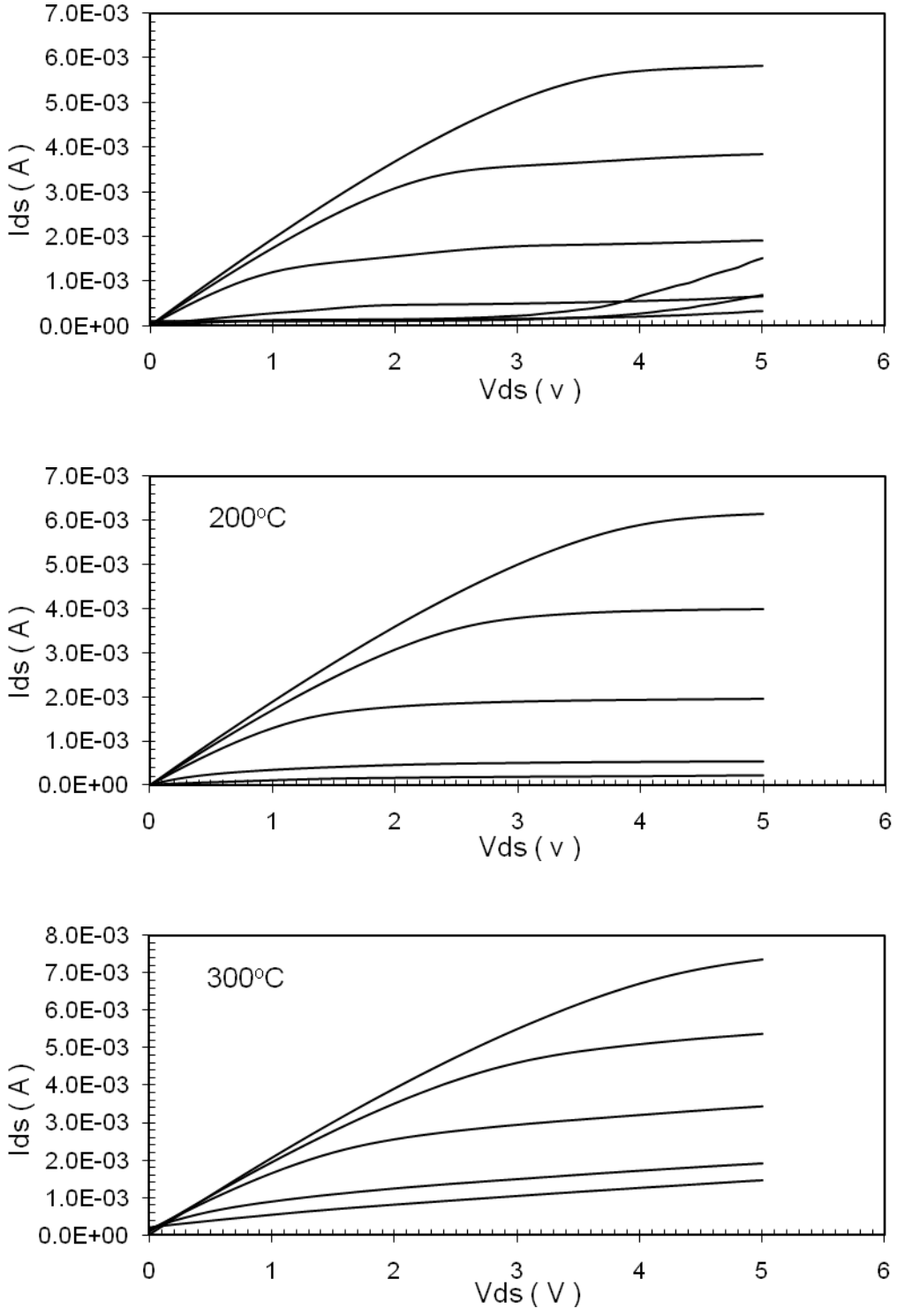



Fig. 67. $I_d$- $V_{ds}$ characteristics for a representative GaAs-MESFET at 39°C, 200°C, and 300°C. The MESFET devices measured were 2 μm long and 100 μm-wide with the gate bias stepped from zero volts with a step size of -1.0 V.

also accounts for the high leakage currents and poor performance [3,8]. The total drain leakage at 300°C is 1.46 mA for a 2 μm long and 100 μm wide gate length device at $V_{ds}$ = 5 V and $V_{gs}$ = -4 V. The $I_{ds}$ and $I_{gs}$ versus $V_{ds}$ characteristics are shown together in Fig. 68, from which a gate current of 667 μA was measured, which is almost half of the total drain leakage current. Clearly this gate leakage current is one of the key components contributing to the total drain leakage current.

The measured gate current under reverse bias at 300°C is ~two times that predicted by the Schottky diode equation [11]. This discrepancy can be ascribed to the barrier lowering effect caused by the highly concentrated field intensity at the edge of the gate as compared to the uniform field assumed in the calculations [11]. The drain leakage density at 300°C for a 2 μm long and 100 μm wide device is $1.5 \times 10^{-5}$ A/μm while the theory predicts a value of $1.0 \times 10^{-5}$ A/μm. Different substrates appear to have various deep level traps which contribute to the current transport at high temperatures [3]. Thus, the value of the activation energy, 0.75 eV, used in the calculations is an indication that the current transport in the substrate used in this study is possibly dominated by EL2 trap centers [3]. The resistivity of substrate used in the calculation was $6 \times 10^{9}$ Ωcm; as the buffer layer grown by MBE might be of a higher quality compared with the semi-insulating substrate in terms of being higher resistivity so there is a possibility of the leakage current density being reduced accordingly.

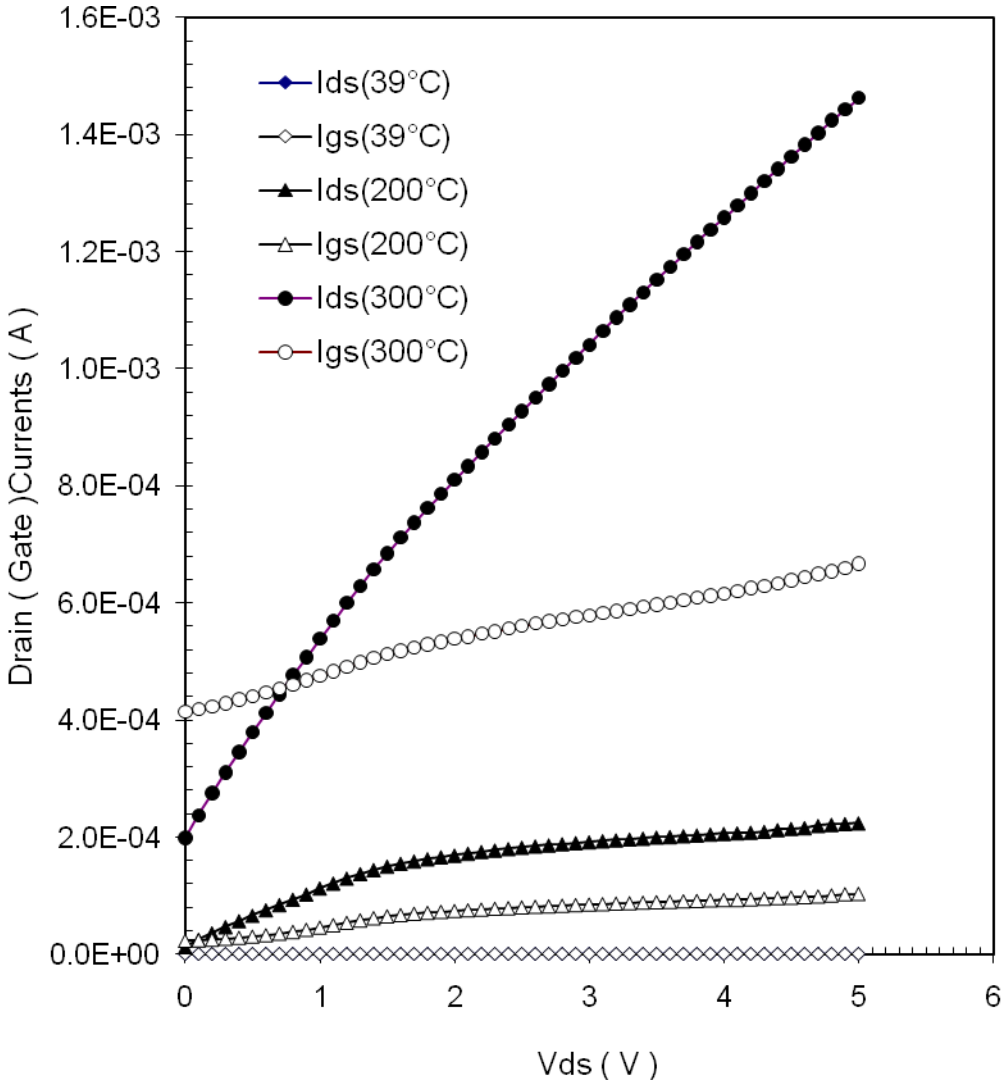



Fig. 68. Drain current, $I_{ds}$-$V_{ds}$ and gate current, $I_{gs}$-$V_{ds}$ characteristics for a representative GaAs-MESFET at 39°C, 200°C, and 300°C. The MESFET devices measured were 2 μm long and 100 μm-wide with $V_{ds}$ = 5 V and $V_{gs}$ = -4 V.

5.2.2.2 Heterojunction MESFET and JFET

Figs. 69 (a) and (b) show the $I_d$ versus $V_{gs}$ characteristics of JFETs and MESFETs between 30°C and 400°C. At room temperature, the drain current on/off ratio of the MESFET is ~ $5x10^5$ while for the JFET it is ~ $1x10^4$. At 400°C, the ratio degraded to ~ 10 for the JFET for the on current at $V_{gs}$= +1.0 V and ~15 for the MESFET for the on current value at $V_{gs}$= +0.5 V. As the temperature increased, the total drain leakage current, which consists of gate leakage and substrate leakage currents, increased exponentially. The relatively poor on/off ratio at low temperatures might be caused by the interface scattering at the AlAs/i-GaAs and i-GaAs/n-GaAs interfaces where I stands for intrinsic (i.e., no) doping. The pinch-off voltage depends on channel doping concentration and thickness. Characteristics such as the fully open channel current, $I_F$, pinch-off voltage, $V_p$, drain current, $I_{ds}$, and transconductance, $g_m$ , as a function of gate-source are given, respectively, by [9]

$$I_F = q\nu_{sat}\omega_g N_D t \tag{18}$$

$$V_p = \frac{qN_D t^2}{2\varepsilon} \tag{19}$$

$$I_{ds} = I_F\left[1-\left(\frac{V_{gs}}{V_p}\right)^{1/2}\right] \tag{20}$$

$$g_m \equiv \frac{\partial I_d}{\partial V_G} = \frac{I_F}{2\sqrt{V_p V_{gs}}} \tag{21}$$

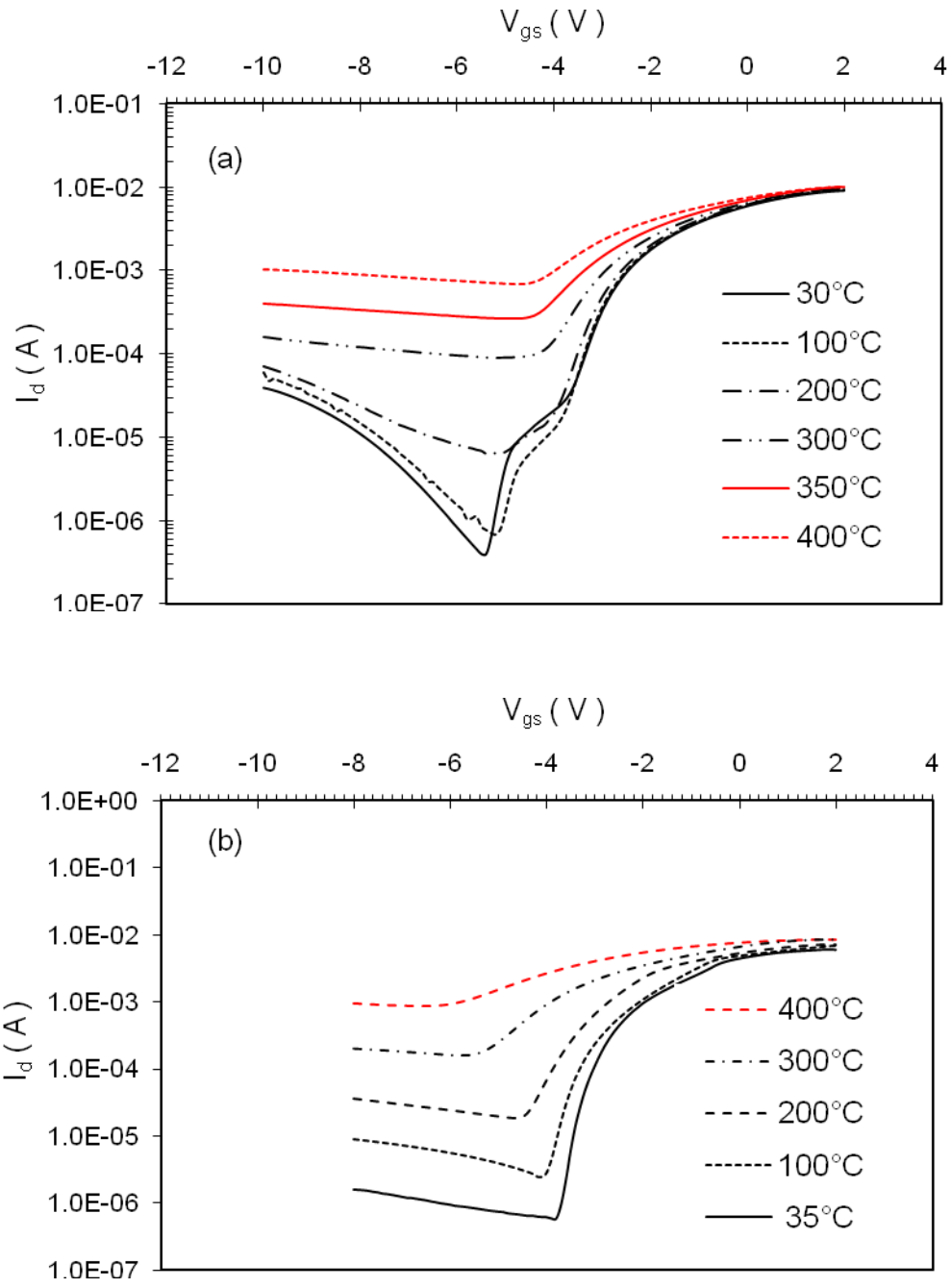



Fig. 69. $I_d$ -$V_{gs}$ characteristics at temperatures between 30°C and 400°C for (a) a heterojunction MESFET and (b) a heterojunction JFET.

where $\nu_{sat}$ is the saturated electron drift velocity and $\omega_g$ is the gate width. In this structure, $N_d$ and $t$ were 2.5x10$^{17}$ cm$^{-3}$ and 150 nm, respectively. The saturated electron drift velocity is $\nu_{sat}$ ~ *7 x 10$^6$ cm/sec,* $V_p$ was calculated as 3.9 V at room temperature by the formula (19).

The threshold voltages determined as the zero current intercepts of the $I_d^{1/2}$ versus $V_{gs}$ characteristics were found to increase from –3.6 V at 35°C for both devices to -6.5 V for the JFET, and -5.4 V for the MESFET, respectively, at 400°C as shown in Fig. 70.

Figs. 71(a) and (b) show the temperature dependence of the gate diode characteristics between room temperature and 400°C for the heterojunction MESFET and JFET, respectively. At room temperature, the JFET had a gate turn-on voltage (defined as 1 mA/mm of gate current or 0.1mA for these 2 μm long and 100 μm wide devices) of 0.75 V with the turn-on voltage (also defined in the same way as the JFET above) of the MESFET being 0.93 V. At 400°C, the gate turn-on voltage of the JFET was 0.34 V while the MESFET had a turn-on voltage of 0.35 V. At 400°C, to obtain a gate current of 1.0 mA, the JFET and MESFET required a forward bias of ~ 0.7 V. The gate diode characteristics in the reverse-bias region showed early breakdown for the MESFET and slightly better behavior for the JFET due to the differences between the Schottky barrier and p-n junction gates, respectively.

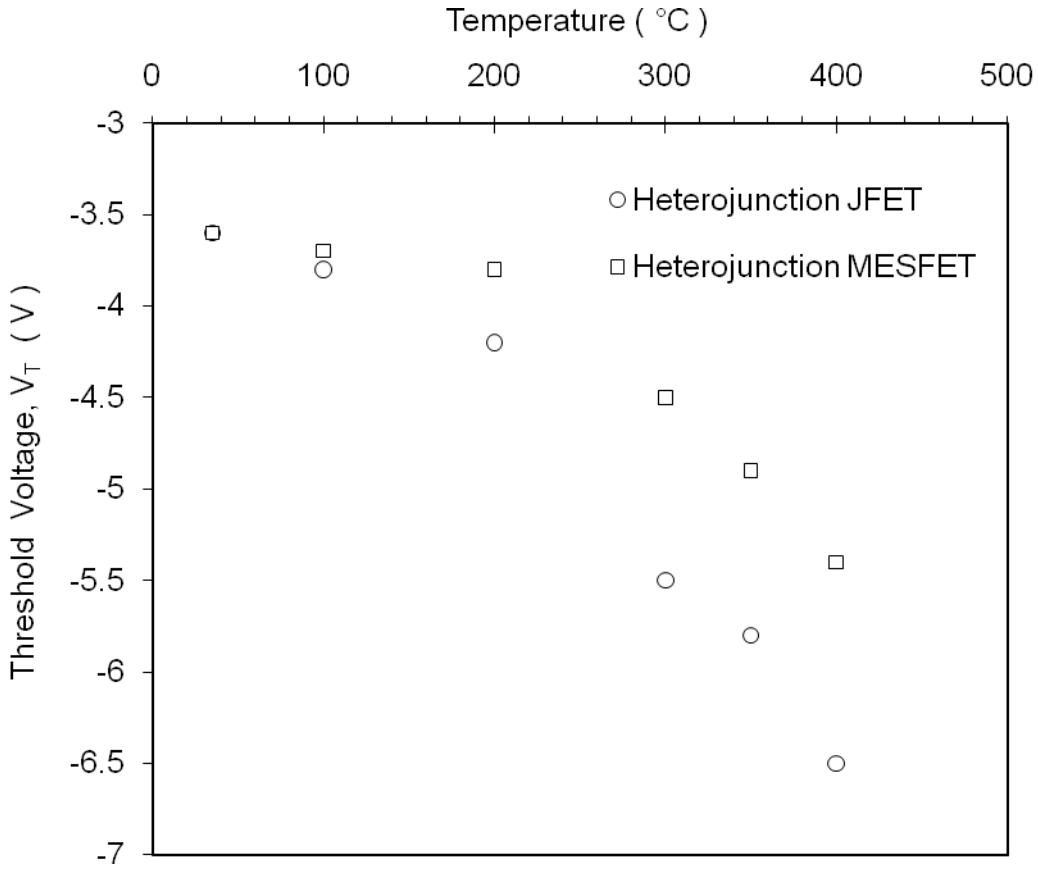



Fig. 70. Threshold voltages for a representative heterojunction MESFET and a representative JFET at temperatures between 30°C and 400°C.

The transconductance, $g_m$, of the JFET and the MESFET as a function of temperature is shown in Fig. 72(a) and (b), respectively. The peak $g_m$ value was 120 mS/mm for MESFET at room temperature while it was ~95 mS/mm for the JFET at room temperature. At 400°C, the gate leakage became severe for both the MESFET and the JFET, and, therefore, poor charge modulation occurred. Thus, a decrease in transconductance was observed in both devices. This result

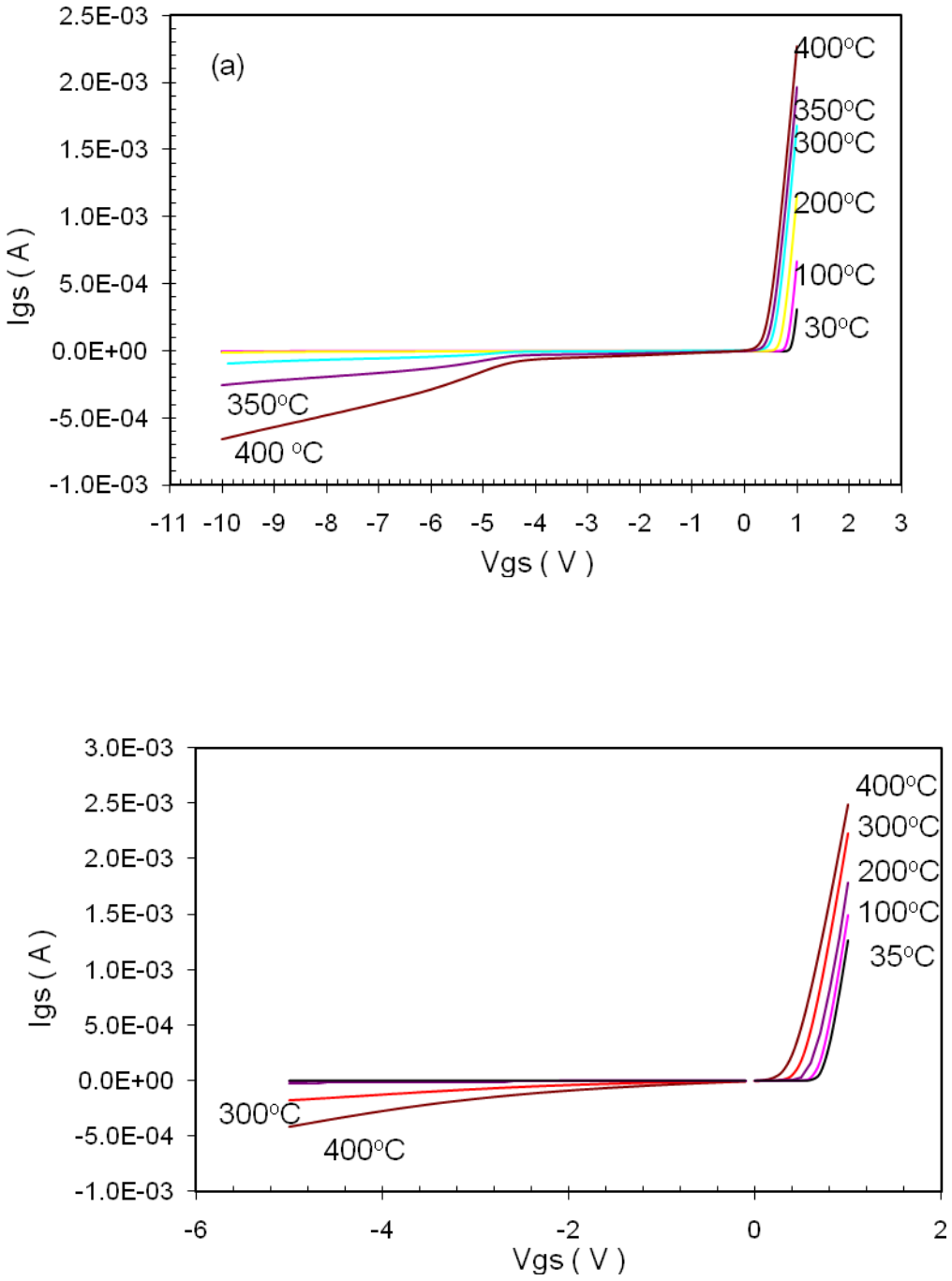



Fig. 71. Temperature dependence of the gate diode characteristics from room temperature to 400°C for (a) a heterojunction MESFET and (b) a heterojunction JFET.

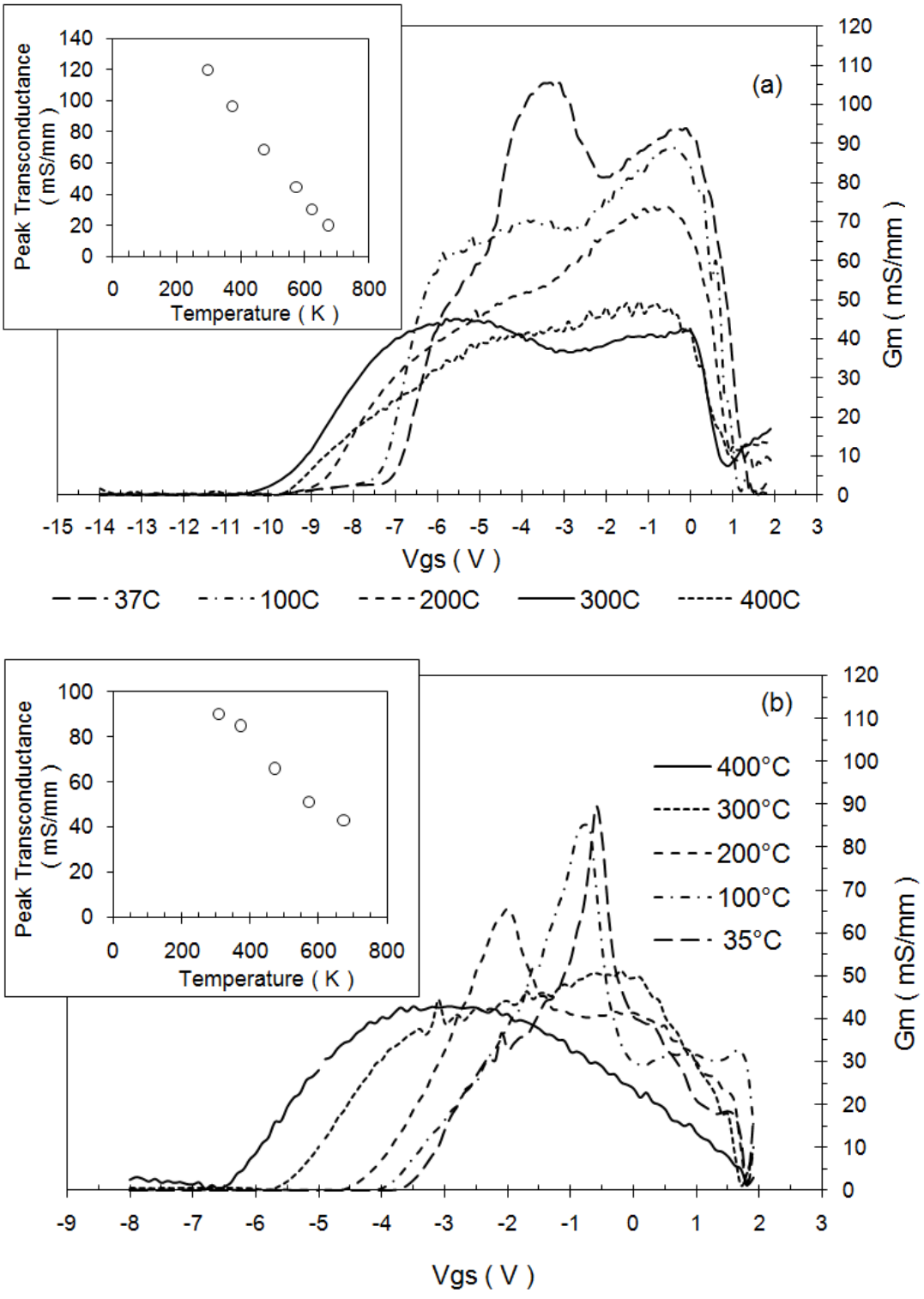



Fig. 72. The transconductance as a function of gate bias for (a) the heterojuction MESFET and (b) the heterojunction JFET at temperatures from room temperature to 400°C.

is in agreement with the gate diode characteristics in which the gate leakage current of the MESFET is slightly larger than that of the JFET and becomes significant at temperatures above 350°C. The gate and drain leakage currents, in general, cannot be modulated or directly controlled by the gate and/or drain voltages, thus leading to a reduction in the controllable charge modulation at high temperatures.

### 5.2.3 Comparison between monolithic GaAs FETs and heterojunction FETs

#### 5.2.3.1 Effect of Schottky barrier height on leakage current

The temperature dependence of the $I_d$ versus $V_{ds}$ characteristics for a representative heterojunction MESFET with gate dimensions of 2 x 100 $\mu m^2$ at 300°C, 350°C, and 400°C, are shown in Figs. 73(a), 74(a), and 75(a), respectively. Along with the $I_d$-$V_{ds}$ plots, the $I_{ds}/I_{gs}$ versus $V_{ds}$ characteristics at the pinch-off condition are shown shown in Figs. 73(b), 74(b), and 75(b), respectively. Comparing these results with GaAs MESFETs, the gate currents were dramatically reduced in heterojunction MESFETs because the gate barrier height measured by the forward I-V characteristic is 1.1 eV, which is 0.3 eV higher than that of the GaAs MESFET. The measured gate current density for the GaAs MESFET is 6.8 $\mu A/\mu m$ at 300°C, while it is 8 $\mu A/\mu m$ at 400°C for heterojunction MESFET. The effect of gate leakage current on drain leakage has been discussed in Chapter 4 where the gate current density at 400°C predicted by the Schottky emission current model is 1.2 $\mu A/\mu m$. The difference between the

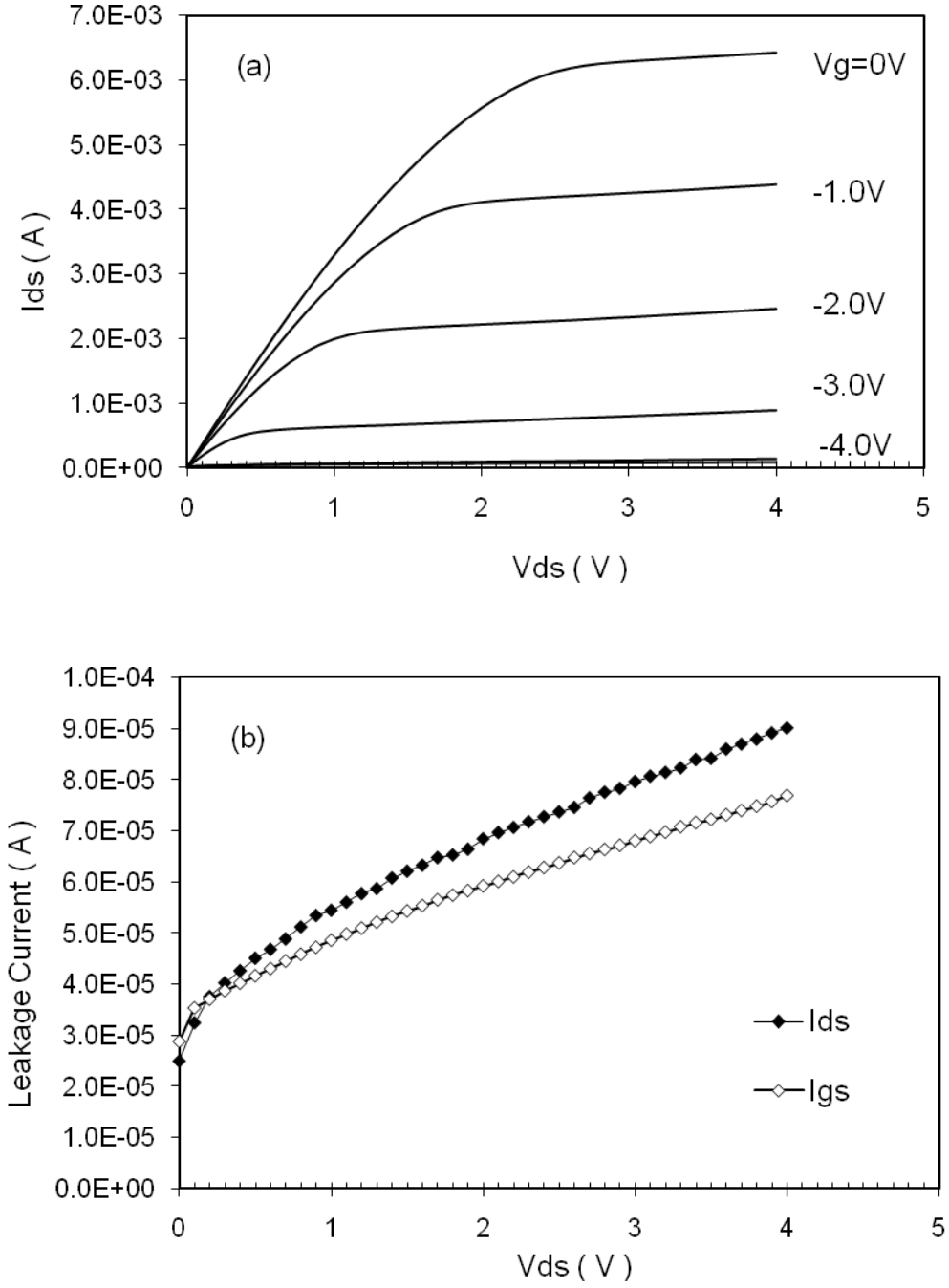



Fig. 73. Characteristics for a representative heterojunction MESFET at 300°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) Drain and gate currents at the pinch-off condition, which is equivalent to a gate voltage of -4.0 V.

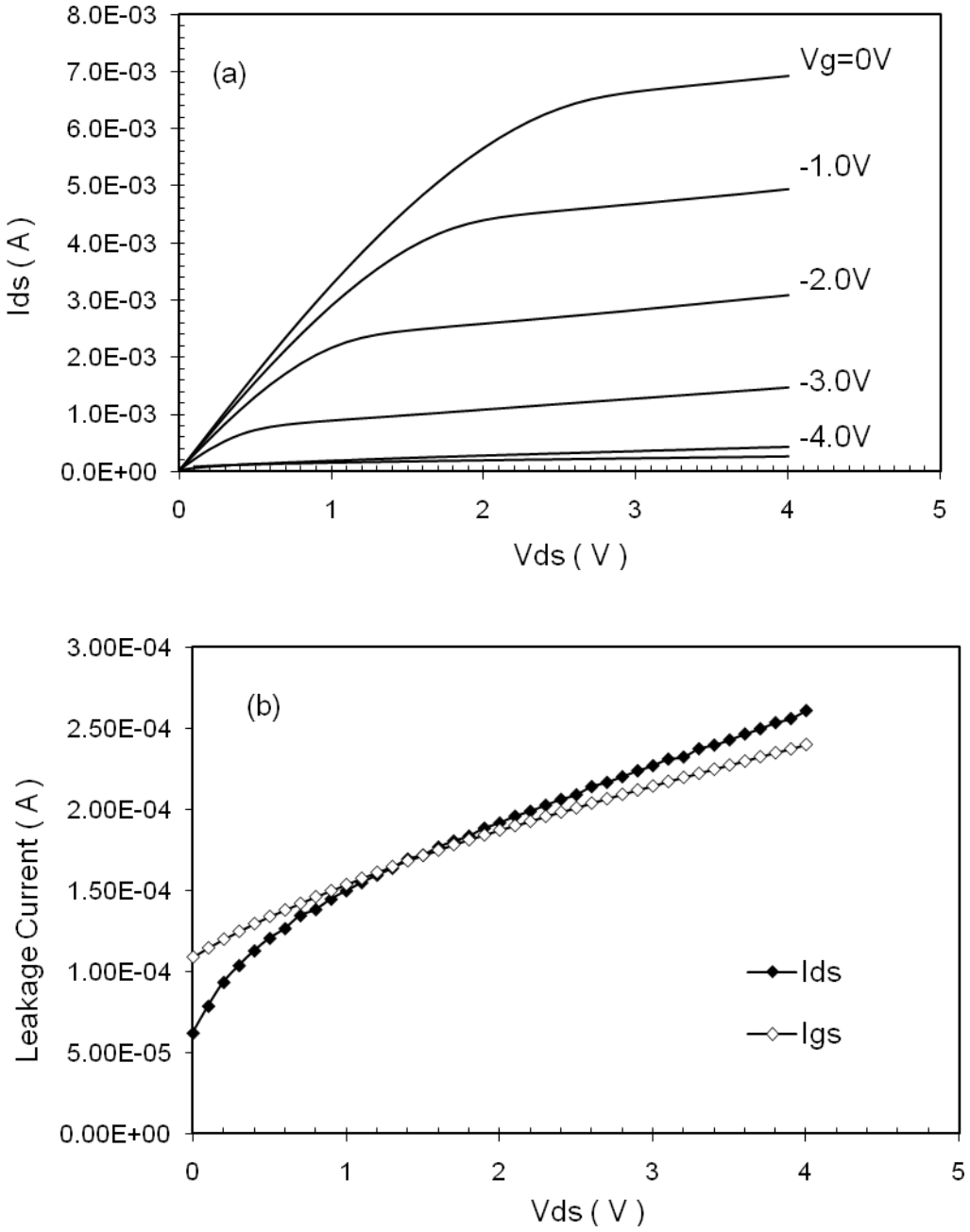



Fig. 74. Characteristics for a representative heterojunction MESFET at 350°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) Drain and gate currents at the pinch-off condition, which is equivalent to a gate voltage of -5.0 V.

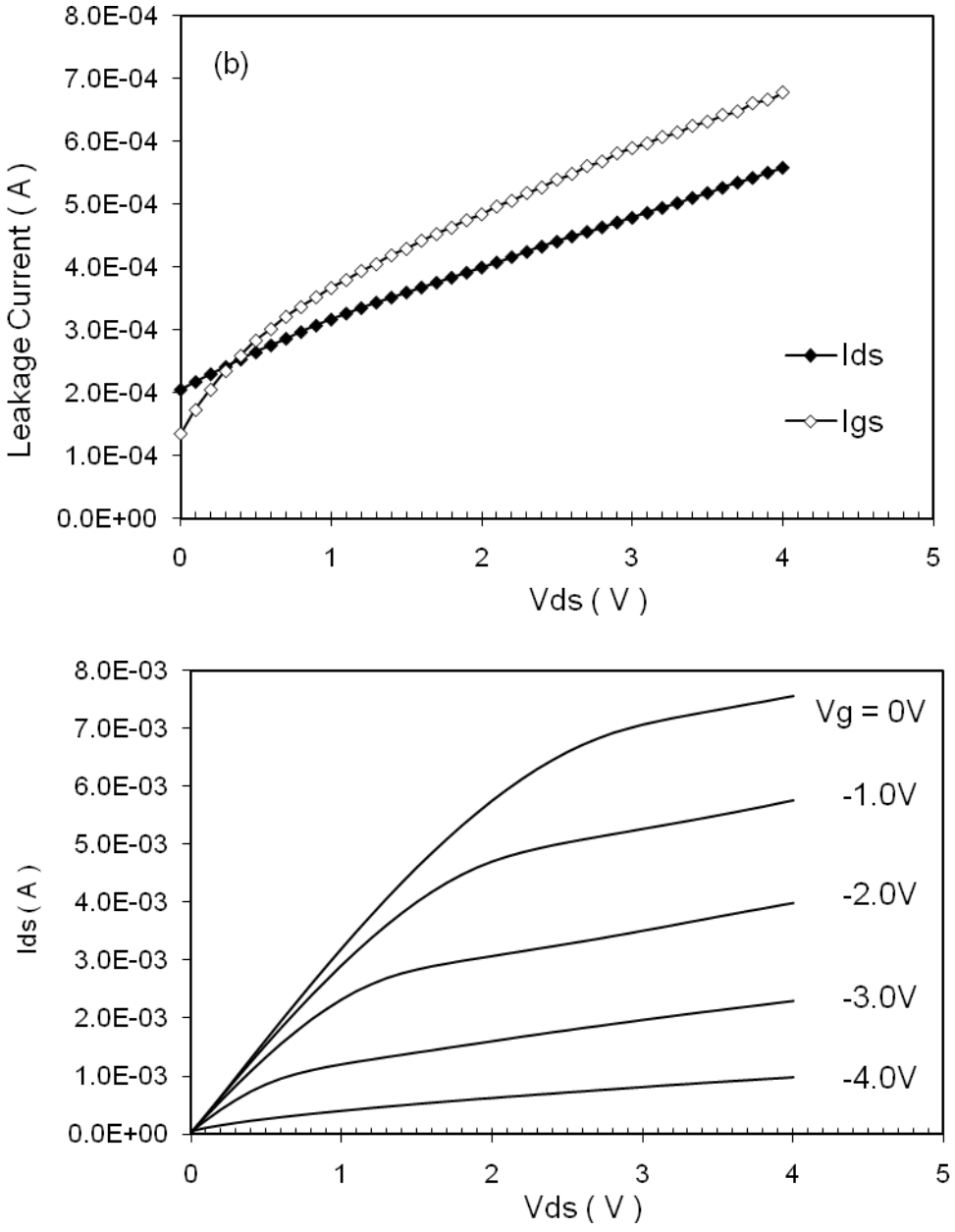



Fig. 75. Characteristics for a representative heterojunction MESFET at 400°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) Drain and gate currents at the pinch-off condition, which is equivalent to a gate voltage of -5.0 V.

measured and predicted values is ascribed to the barrier lowering due to the concentrated field at the periphery of gate contact [3].

5.2.3.2 Effect of back-wall barrier on leakage currents

In GaAs MESFETs, without back-wall barriers, the subthreshold drain leakage current at 300°C has been shown to be dominated by the gate leakage current. The substrate leakage becomes the dominant component of drain leakage currents at 350°C as confirmed by the high temperature tests but not shown in the figures. The drain leakage currents of heterojunction MESFETs, on the other hand, were found to be gate-leakage-dominated including at 400°C. The conduction band offset between GaAs and AlAs is ~0.25 eV [10], and according to Fig. 39, the gate leakage currents will always dominate the total drain leakage currents for barrier heights less than 1.158 eV. The subthreshold drain leakage current density at 400°C is 5.6 μA/μm, which closely follows the value of 4.0 μA/μm predicted by the model. Again, the emphasis on the increase in the Schottky barrier height in MESFET devices is extremely important for eliminating gate to drain leakage currents at elevated temperatures.

5.2.3.3 MESFET and JFET

Figs. 76(a), 77(a), and 78(a) show the temperature dependence of the $I_d$ versus $V_{ds}$ characteristics for a representative heterojunction JFET at 300°C, 350°C, and 400°C, respectively. Along with the $I_d$-$V_{ds}$ plots, the $I_{ds}/I_{gs}$ versus $V_{ds}$ characteristics at pinch-off conditions are shown in Figs. 76(b), 77(b), and 78(b),

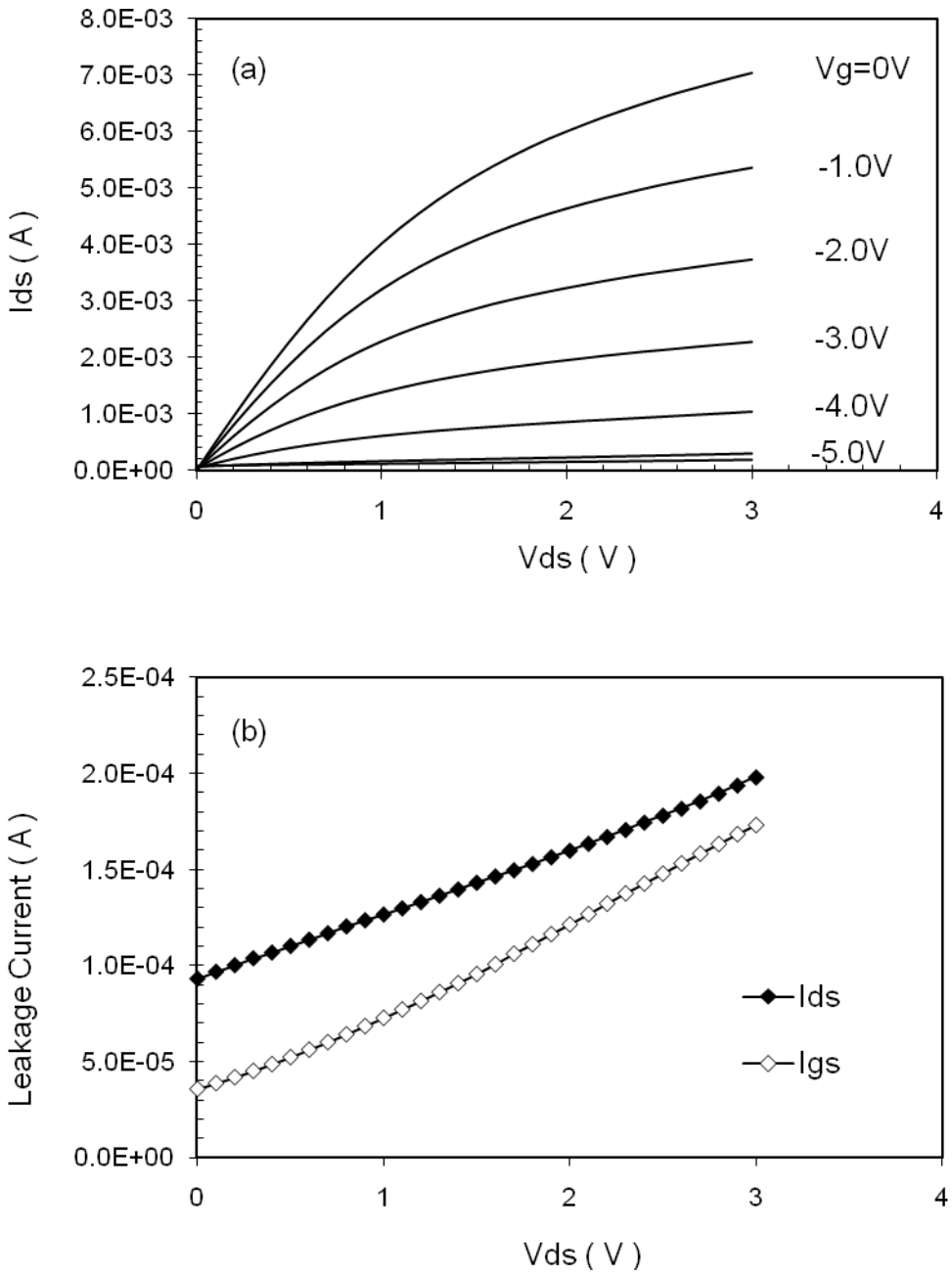



Fig. 76. Characteristics for a representative heterojunction JFET at 300°C demonstrated by (a) $I_d$ -$V_{ds}$, and (b) Drain and gate currents at the pinch-off condition, which is equivalent to a gate voltage of -5.0 V.

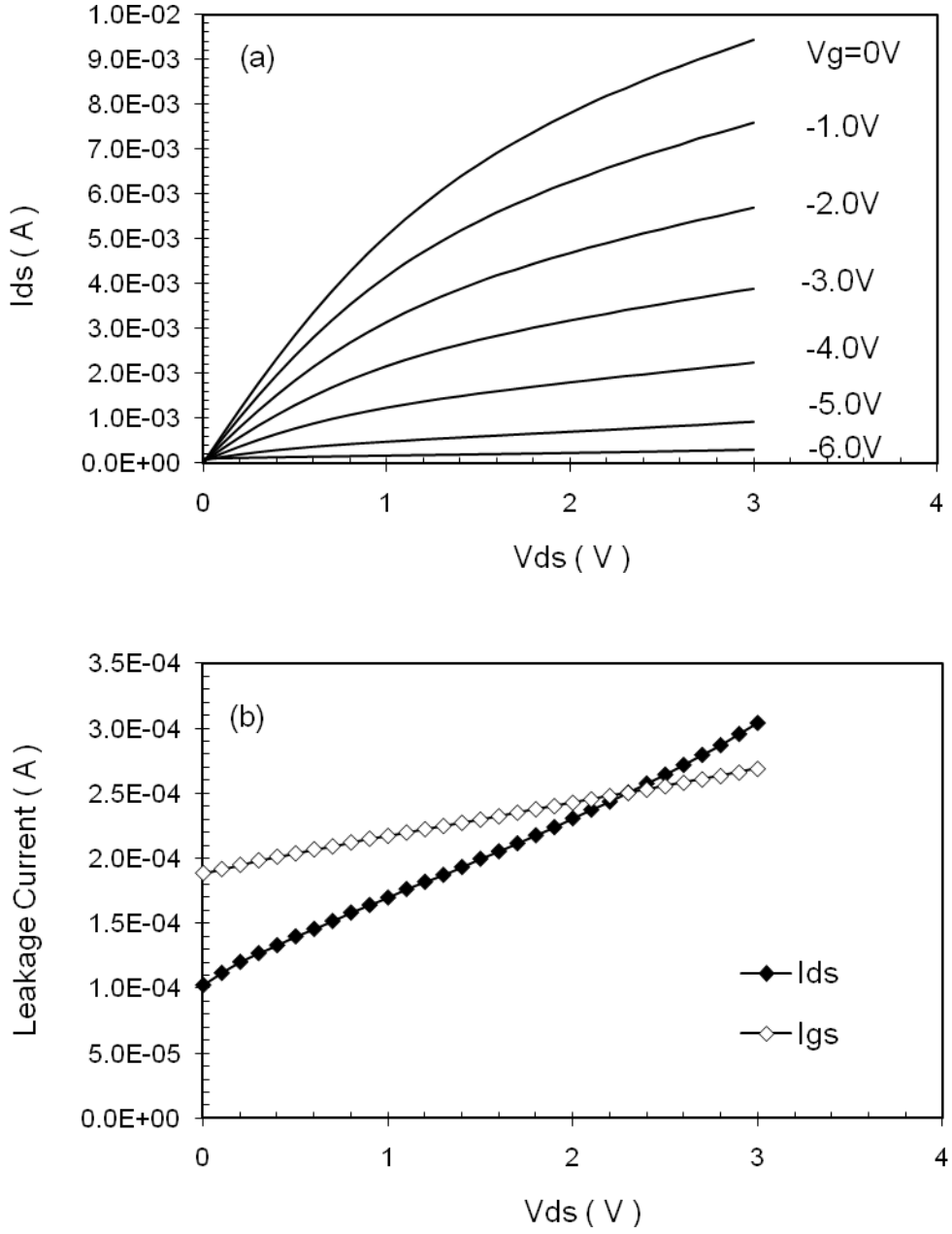



Fig. 77. Characteristics for a representative heterojunction JFET at 350°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) Drain and gate currents at the pinch-off condition, which is equivalent to a gate voltage of -6.0 V.

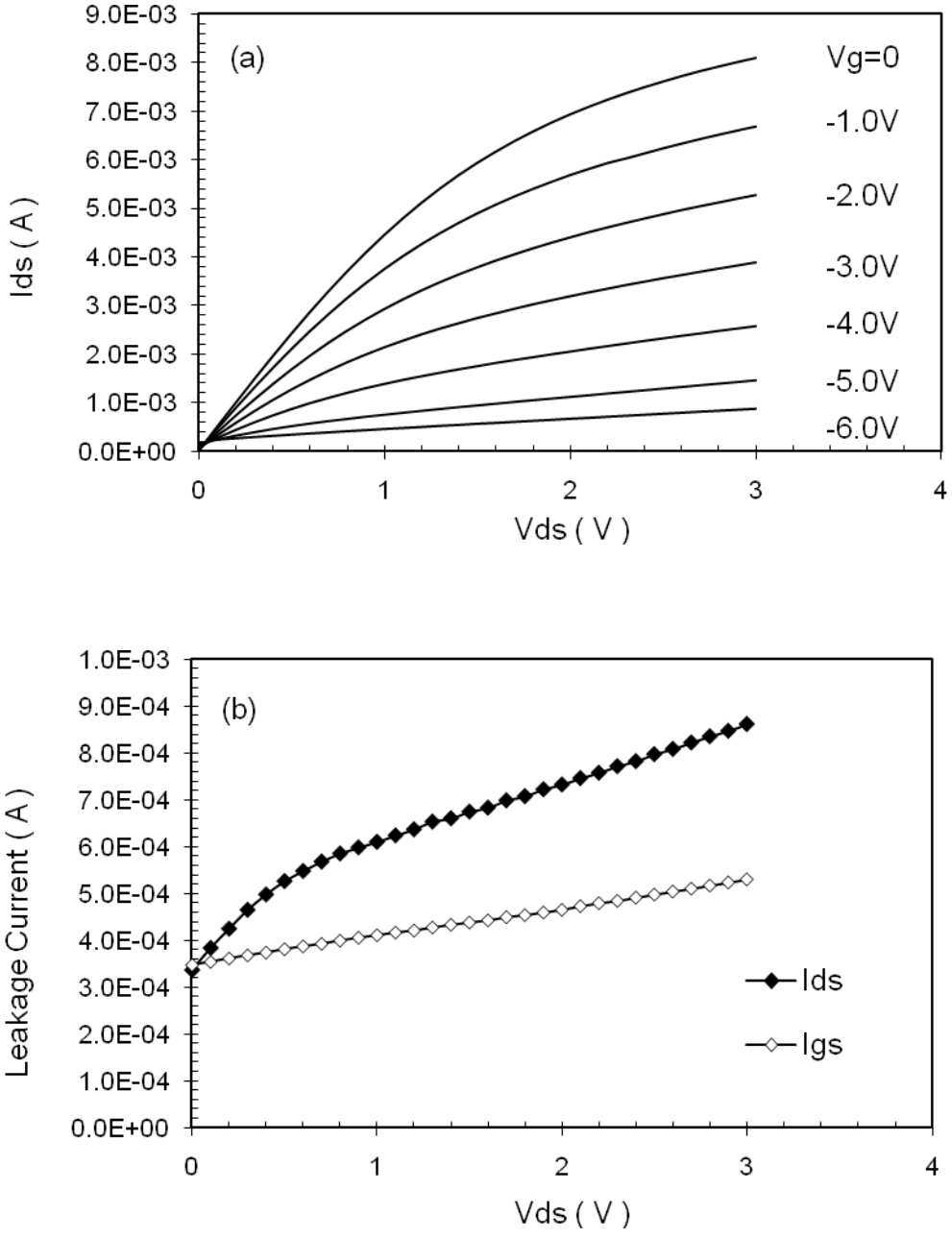



Fig. 78. Characteristics for a representative heterojunction JFET at 400°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) Drain and gate currents at the pinch-off condition, which is equivalent to a gate voltage of -6.0 V.

respectively. Unlike the case for the MESFETs, the gate leakage currents in JFETs at temperatures above 300°C are lower than those of drain leakage currents due to the higher built-in potential of the pn JFET gates compared with the Schotky barrier MESFET gates.

Stated another way, the p-n junction underneath the gate contact metal for JFETs is less conductive at high temperatures than the Schottky barrier junction underneath the gate contact metal for MESFETs. Table 7 shows that, for temperatures between 300°C and 400°C, the MESFETs have better pinch-off characteristics than the JFETs do. This situation with respect to the pinch-off characteristics can be understood by examining the structure design in Section 5.2. The built-in potential of the AlGaAs p-n junction is ~ 0.75 eV corresponding to the turn-on voltage of the gate diode. This value is apparently too low compared to the theoretical value, ~1.4 eV, for the doping concentrations given in Table 7 [11]. The lack of a sharp transition in thickness or doping concentration, or higher doping level than the nominal value at the interface [11], are thought to be responsible for such a low built-in potential. The peak transconductance of the JFET is inferior to the peak transconductance of the MESFET because of the excess capacitance associated with the JFET since gm has a inverse dependence on capacitance [53].

In Fig. 79, the $g_m$ of the MESFET appears to degrade faster than that of the JFET as the temperature increases from room temperature to 400°C. From the gate leakage in Table 7, it is reasonable to attribute the difference to the lower gate leakage currents, and therefore, better charge modulation, of the pn

Table 7. Gate leakage currents and drain leakage currents at temperatures of 300°C, 350°C, and 400°C for a representative heterojunction MESFET and JFET, respectively.

| | MESFET | | JFET | |
|---|---|---|---|---|
| | $I_g$ ( x$10^{-6}$ A ) | $Id_{sub}$( x$10^{-6}$ A ) | $I_g$( x$10^{-6}$ A ) | $Id_{sub}$( x$10^{-6}$ A ) |
| 300°C | 76.8 | 90 | 173 | 151 |
| 350°C | 240 | 261 | 269 | 303 |
| 400°C | 677 | 558 | 531 | 862 |

junction gate JFET compared to the Schottky barrier gate MESFET at high temperatures.

### 5.2.4 Summary

It is important that the pad metals have to be isolated from the substrate by a dielectric layer otherwise an additional leakage path through the pads at high temperatures will occur. Cr, Ti, and Pt have good adhesion when contacted to $Si_3N_4$ and CuGe-based ohmic contacts and thus can be used to prevent the delamination of the pad metals. The viability of heterojunction MESFET and JFET devices operating at 400°C have been demonstrated in this dissertation. Two key factors contributing to the reduction of drain leakage currents were the

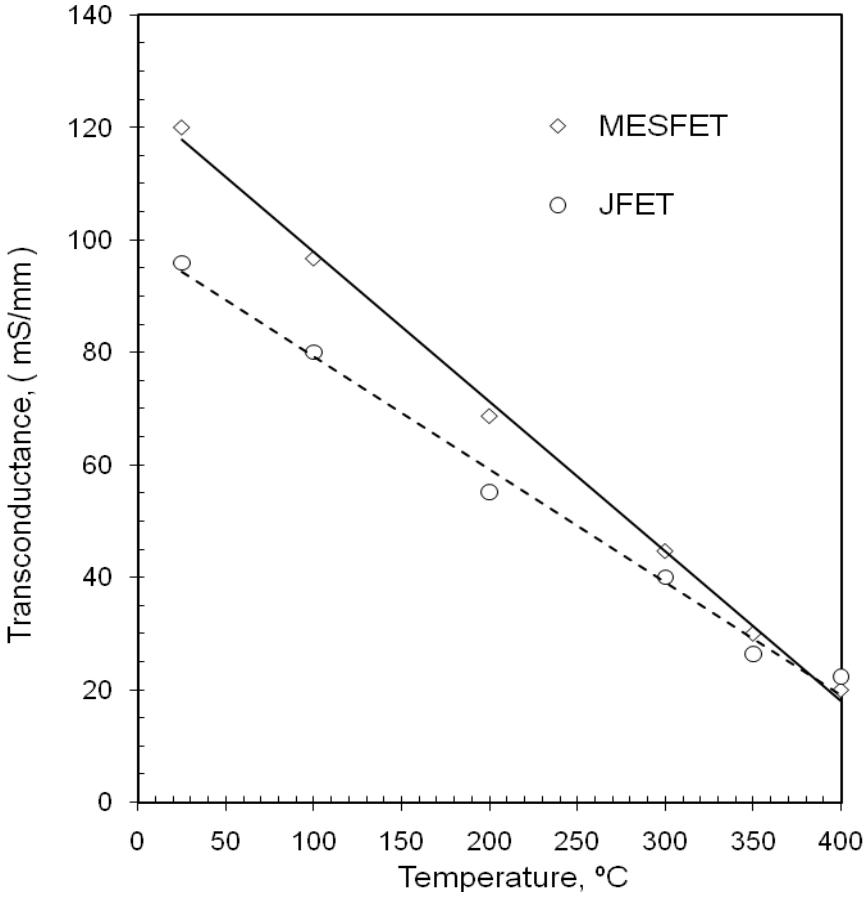



Fig. 79. Peak transconductance of a representative heterojunction MESFET and JFET at temperatures from 25°C to 400°C.

use of a high resistivity, undoped AlAs buffer layer and a wide band-gap AlGaAs material as the gate contacting layer.

Structure design in MESFET and JFET technologies for high-temperature applications needs to include the back-wall barriers such as undoped AlAs and AlGaAs, etc., which are necessary, otherwise, device performance will severely degrade at elevated temperatures, not only because of gate leakage but also because of the substrate leakage.

## 5.3 Pseudomorphic-high electron mobility transistors (p-HEMTs)

### 5.3.1 Introduction

When two semiconductor materials with different band-gaps are joined together to form a heterojunction, discontinuities in both the conduction- and valence-band edges occur at the heterointerface [52]. As shown in Fig. 80, the conduction band diagram of a GaAs-based pseudomorphic-HEMT (p-HEMT), the wide band-gap material, for example, AlGaAs, is doped n-type. The added donor charges bend the band edges and create a triangular potential well [53] in the conduction-band edge of the lower band-gap material, for example, InGaAs. Electrons accumulate in this well and form a sheet of charge analogous to the inversion layer in metal-oxide-semiconductor (MOS) structure. Due to the narrow potential energy well, the carrier energies are quantized perpendicular to the interface while free movement parallel to the interface is maintained [1]. The thickness of the channel is typically only 10 nm, which is much smaller than the de Brogile wavelength of the electrons in this material [1]. The channel of the hetero-FET (HFET) is referred to as a two-dimensional electron gas (2DEG) due to the quantized nature of the allowed energy levels in the channel [53]. In addition, by proper and judicious design, the physical separation of the electrons from the dopant impurities reduces the impurity scattering and, therefore,

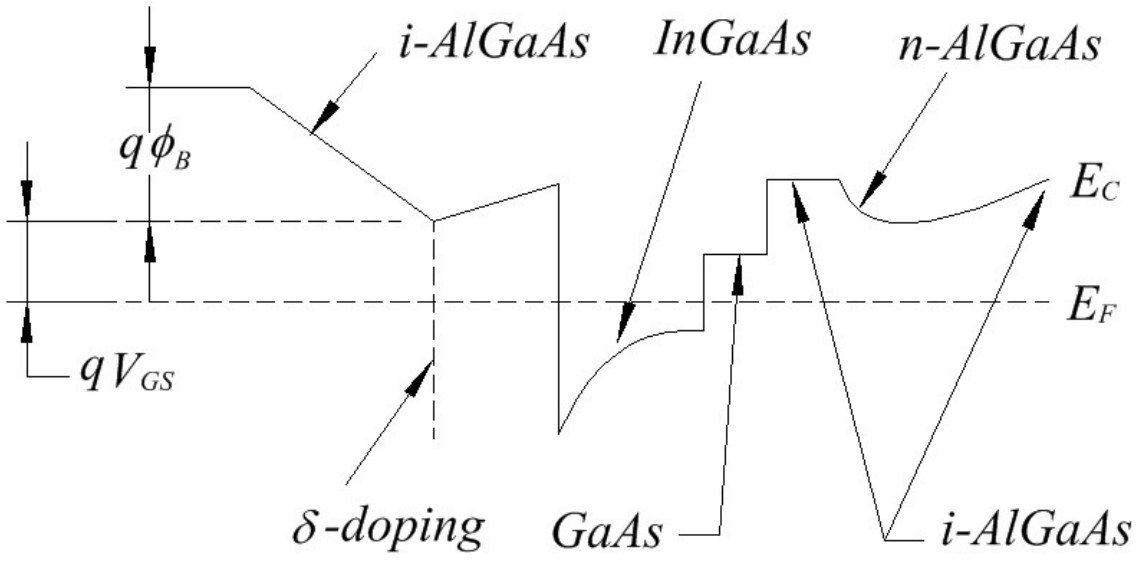



Fig. 80. Conduction band profile for a δ-doped p-HEMT with backside doping layer. Delta-doping, also referred to as pulse, atomic layer or spike doping, consists of growth interruption, and the incorporation of a doping layer of density > 1 x $10^{13}$ $cm^{-2}$ [44,45].

enhances the mobility as well as the effective velocity of electrons under the influence of an electric field [1].

The charge control in the HFET is defined as the behavior of the charge in the device as a function of an externally applied field from the gate electrode. The relationship of the sheet charge $n_s$ to the applied voltage $V_g$ is given by [12]

$$n_s = \frac{\varepsilon}{q(d_d + d_i + \Delta d)}(V_g - V_{th}) \qquad (22)$$

where $d_d$ is the AlGaAs donor-layer thickness and $d_i$ is the AlGaAs spacer-layer thickness.

The threshold voltage for a planar doped HFET structure is given by [12]

$$V_{th} = \phi_b - \Delta E_c - \frac{qN_d d_d^{\,2}}{\varepsilon} \tag{23}$$

where $\phi_b$ is the metal barrier height, $\Delta E_c$ is conduction-band discontinuity between AlGaAs and InGaAs, $d_d$ is the distance between the metal gate and the doped plane and $N_d$ is the surface concentration of donors in doped plane. The values of $\phi_b$, $\Delta E_c$, $d_d$, and $N_d$ for this particular p-HEMT (or HFET) structure are 1.0 eV, 0.2 eV, 50 nm, and 3.49 x $10^{12}$ $cm^{-2}$, respectively.

The suitability for high-temperature operation of a p-HEMT device has not been explored except in one report [42]. The near room temperature properties of a low band-gap InGaAs channel layer have been investigated [13]. The high-gain and high-speed nature of an InGaAs channel p-HEMT draws most of the interest [13].

### 5.3.2 Structure design

The p-HEMT typically consists of n-GaAs contact layer, n-AlGaAs carrier supply layer, i-AlGaAs spacer, i-InGaAs channel layer, i-GaAs insert layer, i-AlGaAs backside spacer, n-AlGaAs backside doping layer, and i-AlGaAs buffer layers. The Al composition was kept to less than 25% to avoid the effect from DX centers which are deep-level defects that can trap carriers and are detrimental for high frequency operation.

Detailed layer structure, including layer sequence, thickness, doping concentration, and composition are listed in Table 8.

In MBE grown layers, after growing a thin undoped spacer, the Si flux is turned on for monolayer coverage [14]. It is possible to make ~90% activation of the Si doping at growth temperatures around 630°C [14]. The breakdown voltages are higher because the gate is on the undoped AlGaAs and located away from the donors.

For high-temperature operation, the p-HEMT structure is favored for several reasons:

(i). The $n^+$ GaAs layer reduces the contact resistance.

(ii). The gate ohmic metal will contact to the undoped AlGaAs layer thus the barrier height should be increased compared to the gate ohmic metal contacting the GaAs.

(iii). The back-wall barriers consisting of up to 25% of undoped AlGaAs materials are grown underneath the channel.

### 5.3.3 Device performance

Fig. 81 shows the rocking curve XRD spectra of the measured and modeled results of the GaAs-pHEMT with the same profile listed in Table 8. The simulated layer thickness and composition of some of the significant layers are given in the last column in Table 8. The Al and In compositions are also verified using photoreflectance characterization [47] in which the resulting spectra correspond to transitions in the materials thus yielding the band-gap energies and the compositions. For the same composition range as the XRD data, a value

Table 8. Detailed structure of a p-HEMT for high-temperature operation

| *Material* | ss | Doping Level | Composition | Simulated RC-XRD data |
|---|---|---|---|---|
| *N+GaAs* | 50nm | Si : $6x10^{18}cm^{-3}$ | | 48.52nm |
| *iAlGaAs* | 50nm | undoped | 25% Al | 50.18nm/26.9% Al |
| *Delt dope* | | | | |
| *iAlGaAs* | 2nm | undoped | 25% Al | |
| *iInGaAs* | 14nm | undoped | 20% In | 13.03nm/20.85% In |
| *iGaAs* | 2.5nm | undoped | | 2.17nm |
| *iAlGaAs* | 3nm | undoped | 25% Al | |
| *nAlGaAs* | 2.5nm | Si : $6x10^{18}cm^{-3}$ | 25% Al | 47.38nm/26.9% Al |
| *iAlGaAs* | 30nm | undoped | 25% Al | |
| *iAlGaAs* | 30nm | undoped | 0~25% Al | |
| *iGaAs* | 300nm | undoped | | |
| *S.I. GaAs* | 400μm | | Substrate | |

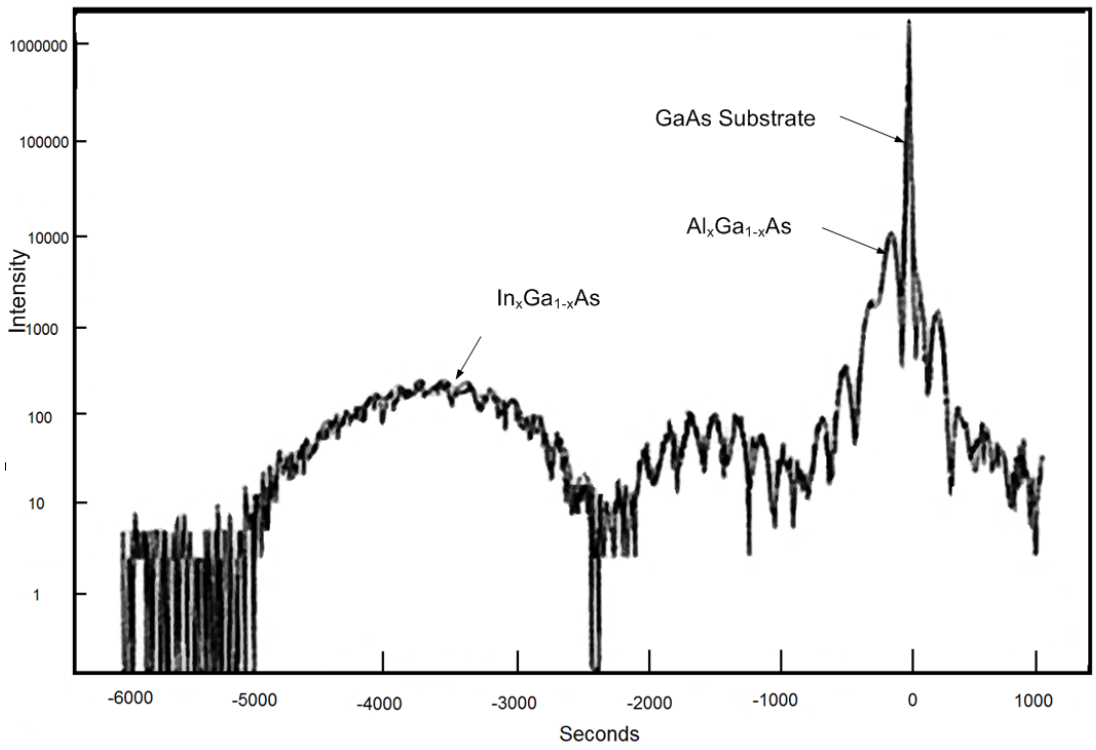



Fig. 81. Rocking-curve XRD results for a p-HEMT structure. The sharp peak on the diffraction spectrum comes from the GaAs substrate. The broad peak next to the sharp peak is from the AlGaAs, while the other broad peak on the left is the InGaAs peak that is well defined and separated from the GaAs peak.

of 25 ± 2% was obtained for aluminum in AlGaAs, while a value of 20 ± 1% for indium in InGaAs was obtained using photoreflectance characterization, respectively.

Fig. 82 shows the transconductance and $I_{ds}$ as a function of gate voltage at room temperature. A peak transconductance of 350 mS/mm at $V_{ds}$ = 1.0 V was achieved using $Cu_3Ge$ ohmic contacts to a p-HEMT having a 2-μm gate length. A typical $g_m$ for 0.1 μm technology using AuGeNi ohmic contacts is ~700 mS/mm [15] for p-HEMTs fabricated with the same structure.

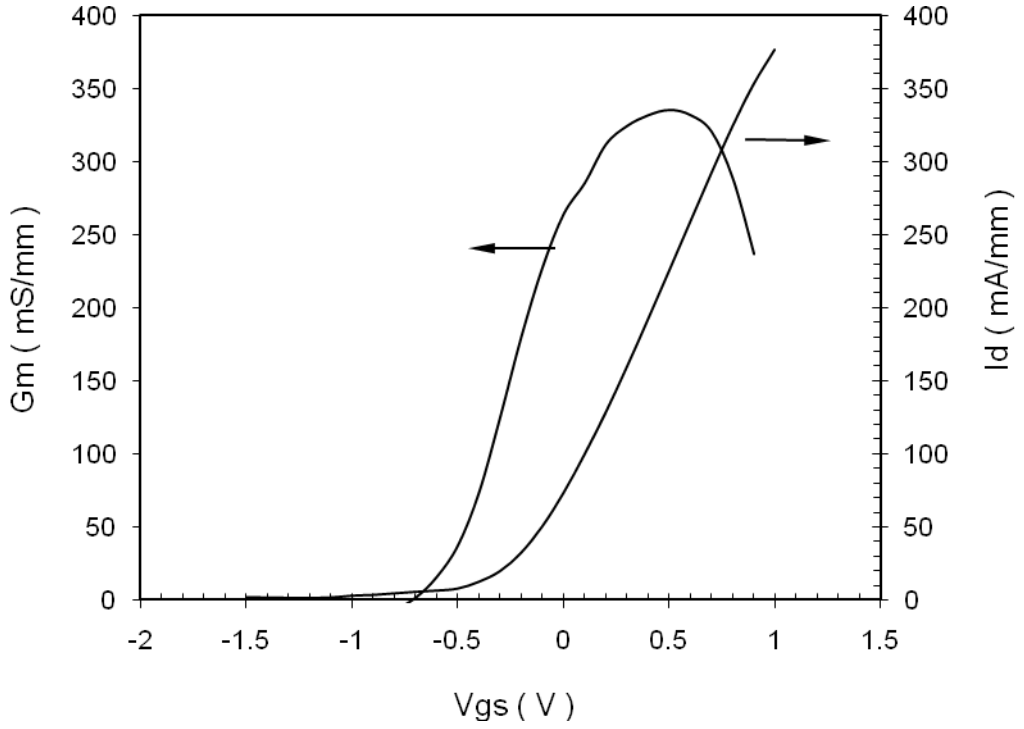



Fig. 82. Transconductance and drain current versus gate voltage data obtained in this dissertation work for a representative pseudomorphic-HEMT at room temperature.

The peak transconductance corresponds to the onset of the parallel conduction in the carrier supply layer, and drops beyond this point [48]. The backside uniform doping in the AlGaAs layer, which lies below the channel, gives a wider transconductance curve, ranging from –0.5 V to ~ 1.0 V gate voltage, compared to that obtained from single-plane doping structures which tend to have a narrow transconductance curve [16].

Some of the devices with shorter drain-source spacing have peak $g_m$ values as high as 400 mS/mm, but the pinch-off characteristics are not as hard

as compared with the devices shown in Fig. 82. The TiPtAu Schottky contacts to undoped $Al_{0.25}Ga_{0.75}As$ have a barrier height of ~ 1.0 eV as determined from forward I-V curves. Thus, the high temperature behavior in terms of leakage current will be presumably gate leakage dominated for temperatures higher than approximately 350°C. However, the TiPtAu contacts are unstable at temperature above 250°C [54,55]. Thus a different gate metallization scheme is needed.

The $I_d$ versus $V_{ds}$ characteristics for a 100 μm-wide device at room temperature, 200°C, 300°C, and 400°C are shown in Figs. 83 (a), (b), (c), and (d). A decrease in peak saturation current is the consequence of the mobility of electrons in the InGaAs channel decreasing with respect to the increase in temperature. Also, the devices had poor pinch-off characteristics at temperatures higher than 300°C.

Fig. 84 shows the transconductance-gate voltage characteristics at temperatures between 25°C to 400°C. The extracted peak transconductances at temperatures between room temperature and 400°C are also shown in the insert. The transconductance decreased about 38% when the temperature increased from 25°C to 200°C. The slow transition between 200°C and 300°C is caused by the additional thermally generated current underneath the channel. The total drain current, which was expected to decrease due to the mobility change at high temperatures, did not decrease much as can be seen in Figs. 83 (b) and (c) because the electrons were able to overcome the back barrier and drop into the channel thus contributing a leakage current to the total drain current. At temperatures higher than 300°C, electrons can no longer be well confined in the

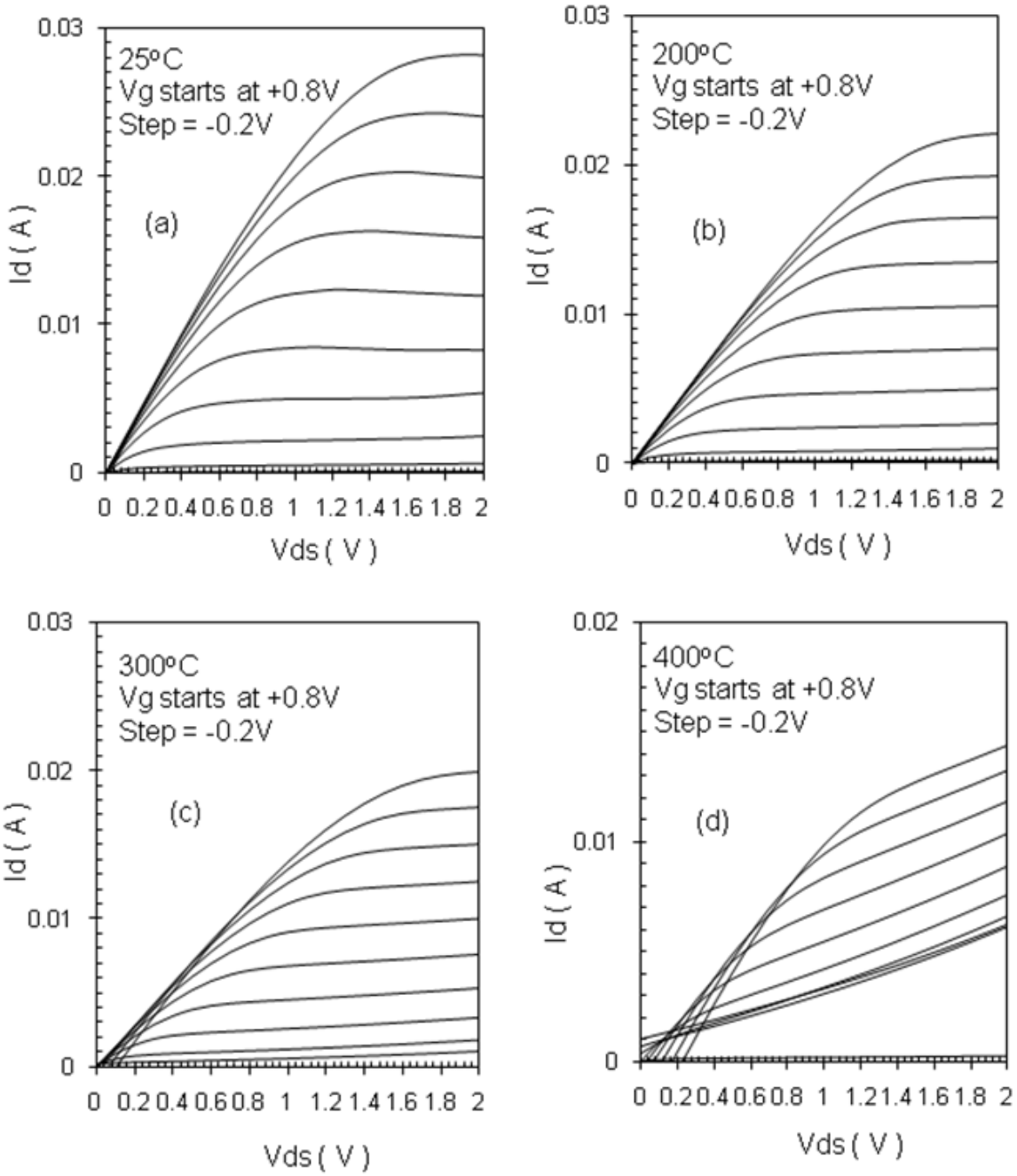



Fig. 83. $I_d$-$V_{ds}$ characteristics of a representative p-HEMT at (a) 25°C, (b) 200°C, (c) 300°C, and (d) 400°C.

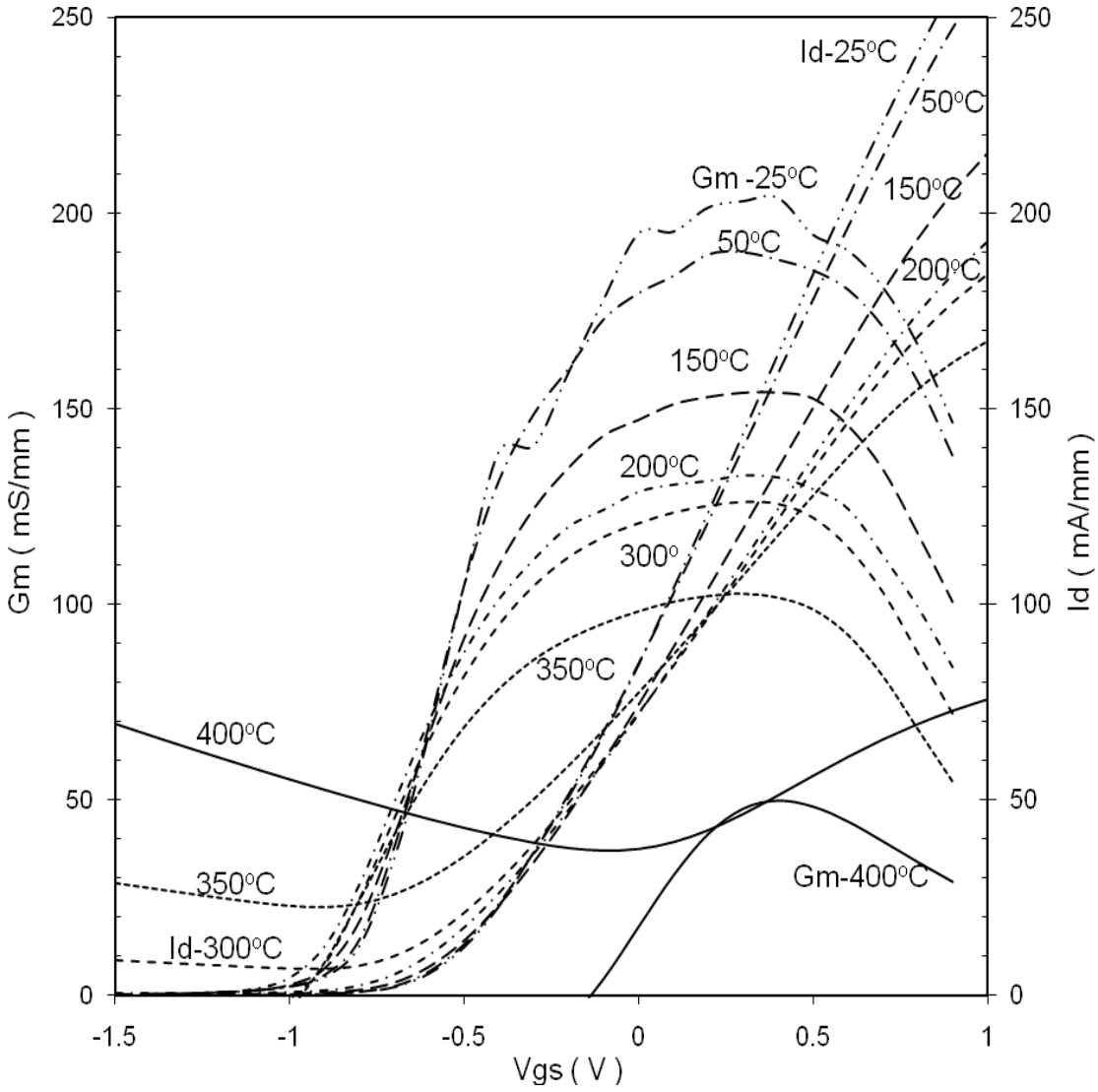



Fig. 84. Transconductance of a representative p-HEMT as function of gate voltage at temperatures from 25°C and 400°C.

channel, which together with the increased parallel conduction in the carrier supply layer, results in the transconductance degrading faster than $T^{-1}$.

The drain leakage currents were found to be exceptionally high and almost as leaky as the monolithic GaAs MESFET without the back-wall barrier. The measured gate current density was slightly lower than the expected value of $1.57 \times 10^{-4}$ A/μm.

The undoped AlGaAs layer may be responsible for the reduction in gate leakage current density due to the lack of DX centers. Under these conditions at high temperature, the device has lost the ability to effectively modulate the carriers because of the parallel conduction in the carrier supply layer. Increasing the separation between the doping plane and gate contact and lowering the doping density might help to improve this characteristic; however the tradeoff is between the transconductance and the breakdown voltage – attempts to raise the transconductance will, most probably, result in a decrease in the breakdown voltage.

### 5.3.4 Leakage current density in pseudomorphic-HEMT

For distinguishing the dominant leakage current source, the $I_d$ and $I_g$ versus drain voltage characteristics at 300°C, 350°C, and 400°C are plotted together and shown in Fig. 85. The maximum drain leakage currents at $V_{ds}$= 1.5 V and $V_{gs}$= -0.8 V at 300°C, 350°C, and 400°C are 1.01 mA, 3.08 mA, and 6.66 mA, respectively, while the corresponding gate reverse leakage currents are 856 μA, 2.93 mA, and 6.85 mA, respectively (see Table 9). It is very clear that the

Table 9. Subthreshold characteristics of a p-HEMT at 300°C, 350°C, and 400°C.

| Temperature | $I_d$ at $V_{gs}$ = -0.8V | $I_g$ at $V_{ds}$ = 1.5V |
|---|---|---|
| 300°C | 1.01mA | 856μA |
| 350°C | 3.08mA | 2.93mA |
| 400°C | 6.66mA | 6.85mA |

leakage current dominates the reverse gate current at high temperatures due to the relatively low Schottky barrier height of the TiPtAu gate and possible reactions taking place between the TiPtAu and the semiconductor at high temperatures. As can be seen from Fig. 85(a), the gate leakage current is the dominant current, including for the drain leakage current contribution, at high temperatures of 300°C and above. To address the strategy of structure design for p-HEMTs for high-temperature operation, a few of the layers for the profile in Table 8 need to be changed and modified:

1. The backside doping used to broaden the transconductance-Vgs curve has to be removed because it provides an additional leakage path to the channel at high temperatures.

2. Incorporation of a high Al-containing layer underneath the channel layer, most likely under the backside spacer to reduce the transport of thermally generated leakage current. This is analogous to the concept of semiconductor-on-insulator for eliminating substrate leakage currents.

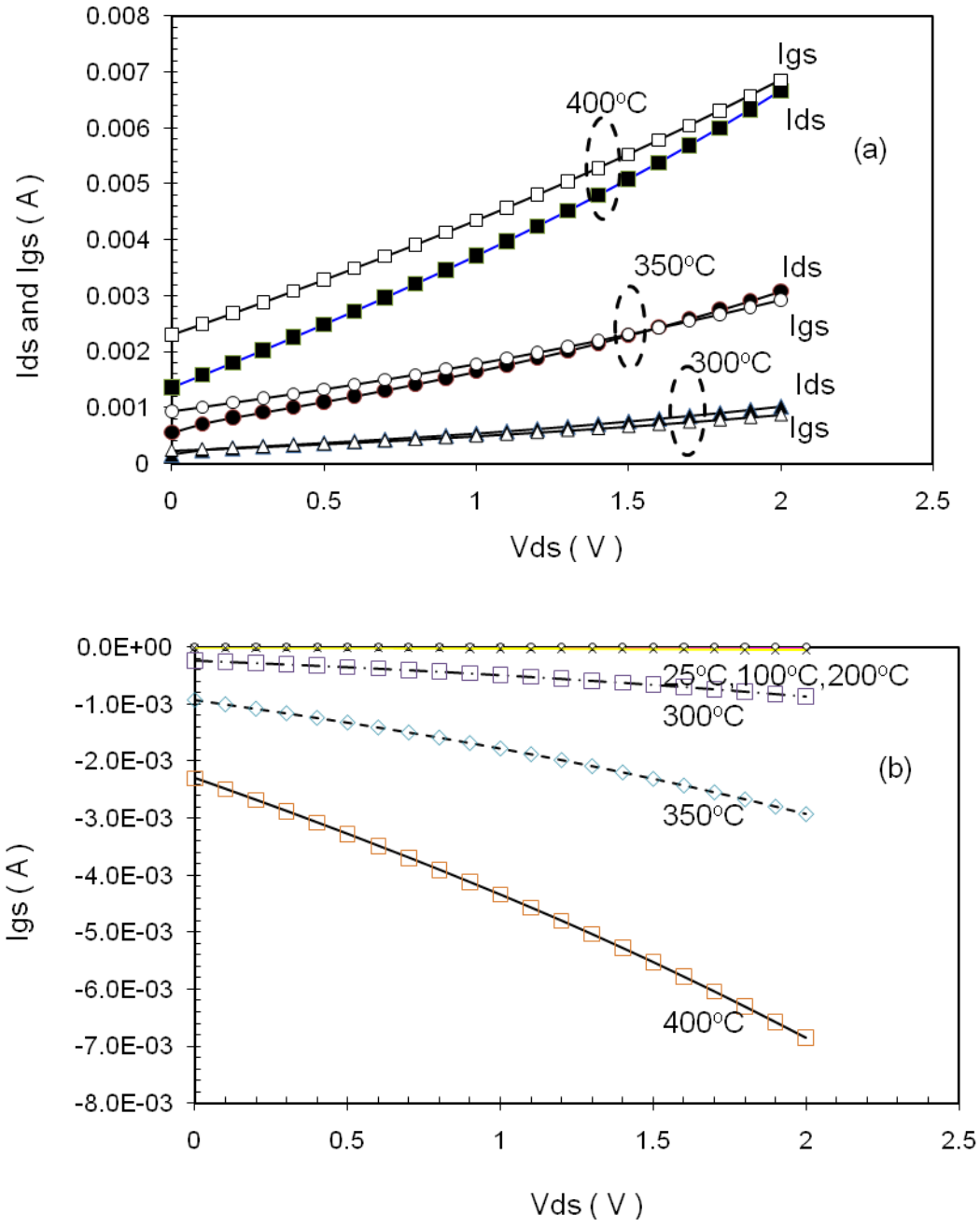



Fig. 85. Temperature dependent leakage currents for a representative p-HEMT at elevated temperatures demonstrated by (a) Gate and drain leakage currents measured at the pinch-off point, which is equivalent to a gate voltage of -1.0 V, and (b) $I_{gs}$-$V_{ds}$ characteristics at a gate voltage of -1.0 V at temperatures from 25°C to 400°C.

3. Increasing the separation between the doping plane and gate contact and lowering the doping density might help to improve the breakdown characteristic but the tradeoff is a lower transconductance in return for higher breakdown voltage.

Fundamentally, the confinement of carriers changes with position along the channel [11] of a HEMT. Fig. 86 shows the variation of the conduction band edge along the channel at positions (a) near the source end and (b) near the drain end at room temperature. The carrier confinement is generally better near the source end than the drain end because of the varying electrical field in the channel of the device. Such a carrier confinement will be reduced even more at high temperature due to the band-gap lowering as the band gap energy decreases with increasing temperature [46]. Up to this date, there is no solution to prevent the parallel conduction in the carrier supply layer without sacrificing the device performance such as transconductance, output power, etc.

### 5.3.5 Summary

The performance of p-HEMTs is superior to any other device in terms of the transconductance. For high-temperature applications, p-HEMTs become leaky at high temperature because of the parallel conduction and buffer design. The gate diode performs better when contacted to the undoped AlGaAs layer, which is beneficial in designing a structure for high temperature operation.

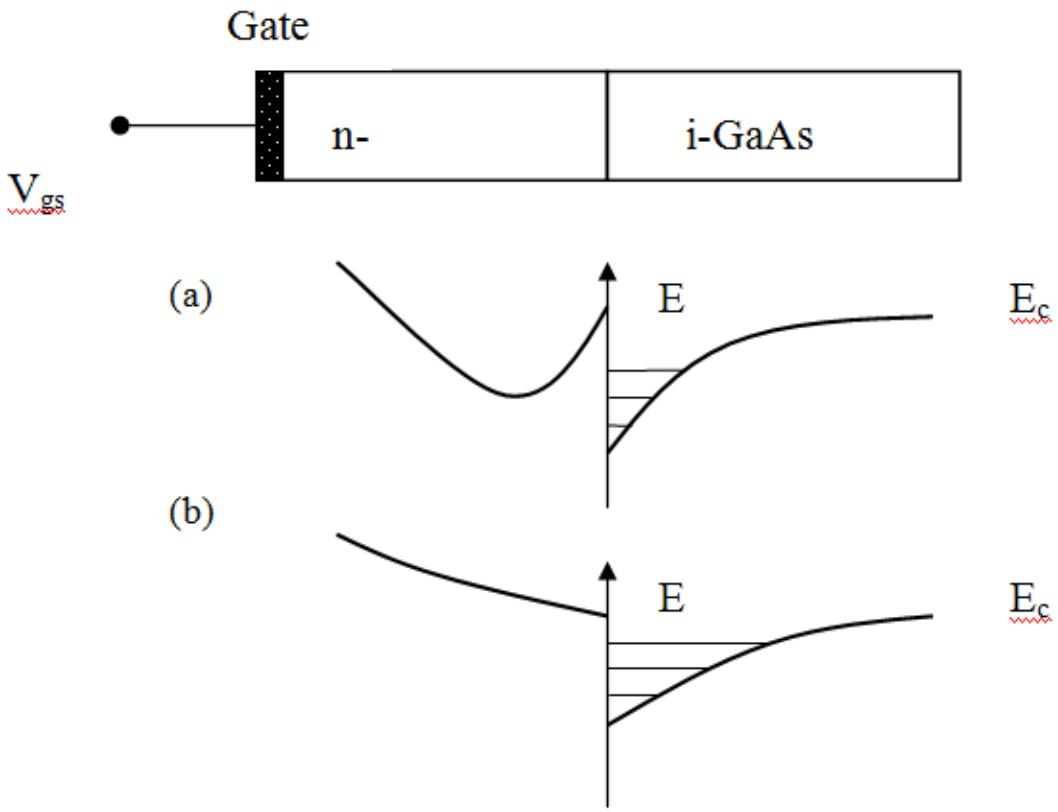



Fig. 86. Variation of conduction band edge along the channel of the device [11]:

(a) near source end - good confinement and

(b) near drain end – reduced confinement

## 5.4 Heterojunction MESFET fabricated with $Al_{0.3}Ga_{0.7}As$ gate contact layer and buffer layer grown at low temperatures (LT)

### 5.4.1 Characterization of LT- $Al_{0.3}Ga_{0.7}As$ materials

Fig. 87 shows the X-ray analysis results for $Al_{0.3}Ga_{0.7}As$ grown at 300°C and 350°C in which both samples have experienced in-situ annealing at 630°C

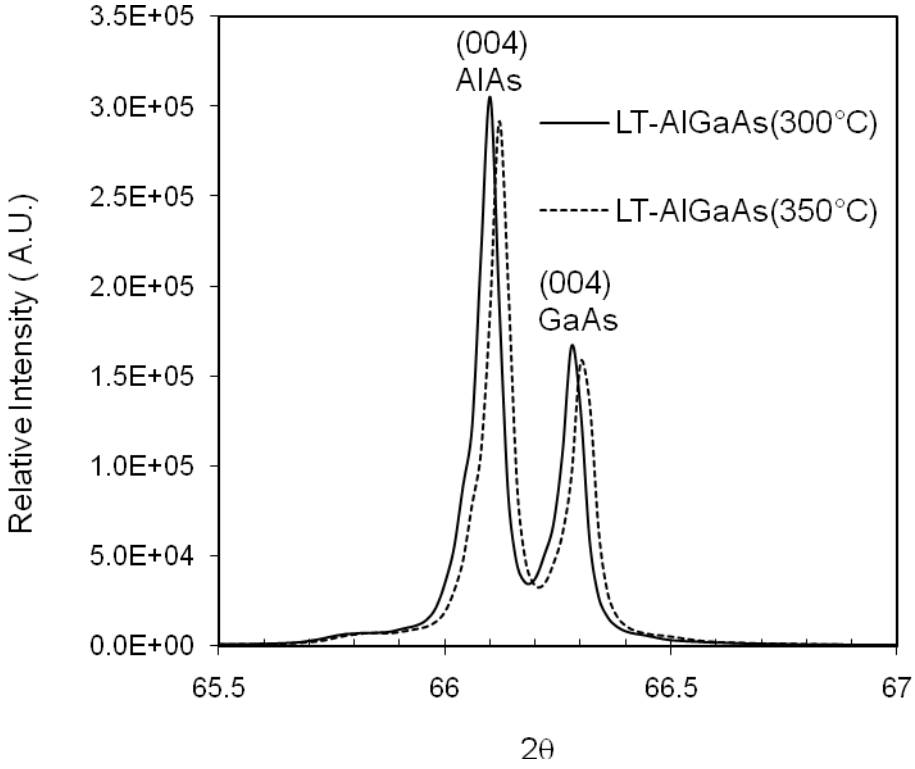



Fig. 87. XRD patterns for LT-AlGaAs materials grown at 350°C and 300°C. Only the (004) peaks of AlAs and GaAs from K1$\alpha$ radiation were collected.

for 15 min. From this point on, the sample designation E9231 will be used for the wafer with the LT-AlGaAs grown at 350°C and the sample designation E9232 for the wafer grown at 300°C. At the step size of 0.001 degree per second, the AlAs (004) peaks are also observed in the graph. No arsenic (As)-precipitate related peaks were detected for either wafer. This indicates the high level of growth quality because, if such peaks existed, the As precipitate related peaks are under the resolution limit of the XRD spectrum. The (004) peak of $Al_{0.3}Ga_{0.7}As$ grown at

300°C shifts 0.0175° towards a smaller angle with respect to that grown at 350°C which also may be within the growth reproducibility/uniformity tolerances.

The X-ray spectra for the 350°C-grown and the 300°C-grown $Al_{0.3}Ga_{0.7}As$ samples are, in almost every respect, identical as can be seen from Fig. 87. If there are any discrepancies, these discrepancies may be from the compositional differences between two samples since the run-to-run uniformity is ~ 2%.

Fig. 88 shows 18K- photoluminescence (PL) spectrum of the $Al_{0.3}Ga_{0.7}As$ grown at 300°C ( line A ) and grown at 630°C ( line B ). For comparison, the spectrum of $Al_xGa_{1-x}As$ ( x = 0.165 ) grown at 630°C is shown as line C. The center energy of the emission from the LT- $Al_{0.3}Ga_{0.7}As$ is at 1974.3 meV and the FWHM is found to be 23 meV. This is an indication that the $Al_{0.3}Ga_{0.7}As$ is of good quality and can be grown at temperatures as low as 300°C. This also explains the peak shift in the XRD analysis in Fig. 87.

The difference in lattice constants of the two LT- $Al_{0.3}Ga_{0.7}As$ samples is found to be 0.025% due to the difference in Al composition. The Ga and Al incorporation at both regular and low growth temperatures was 100% because the desorption rate of both atoms was negligible within this temperature range.

The atomic compositions of Al and Ga should be the same for HT- and LT-$Al_{0.3}Ga_{0.7}As$. Therefore, most likely, there is an appreciable shift in the stoichiometry or inhomogeneous high Al-containing AlGaAs in the LT-AlGaAs that affected the optical properties and caused a blue-shift in the PL spectrum. The samples were etched down until the LT-$Al_{0.3}Ga_{0.7}As$ was exposed and surface morphology analysis using AFM could be performed. Figs. 89(a) to (d) show that

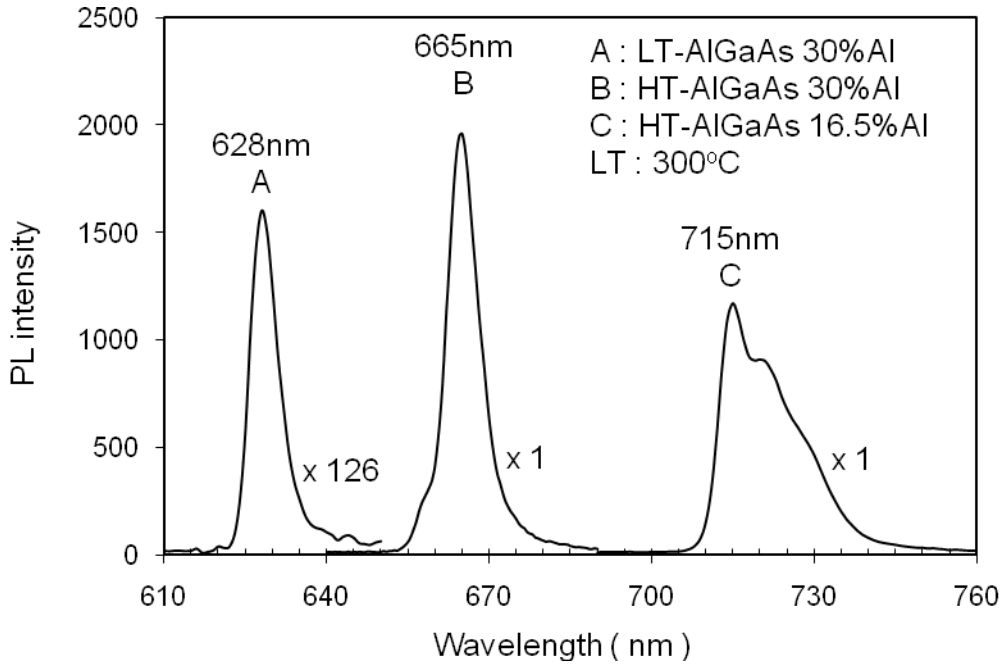



Fig. 88. 18K-PL spectrum of $Al_xGa_{1-x}As$ (x = 0.3) grown at 300°C ( line A ) and 630°C ( line B ). For comparison, the spectrum of $Al_xGa_{1-x}As$ ( x = 0.165 ) grown at 630°C is shown as line C.

the LT- $Al_{0.3}Ga_{0.7}As$ has precipitates with an average size of 0.5μm and agglomerated as bands (of small islands). EDX mapping analysis shows a high As concentration in the region of precipitates. The observation is similar to what has been seen by Smith et al. [17,18] and is one of the mechanisms responsible for the high resistance after annealing [17-27].

### 5.4.2 Structure design

The two LT-$Al_{0.3}Ga_{0.7}As$ layers used in this dissertation work had a two-fold purpose. The LT layer (lower) under the n-type GaAs channel layer serves

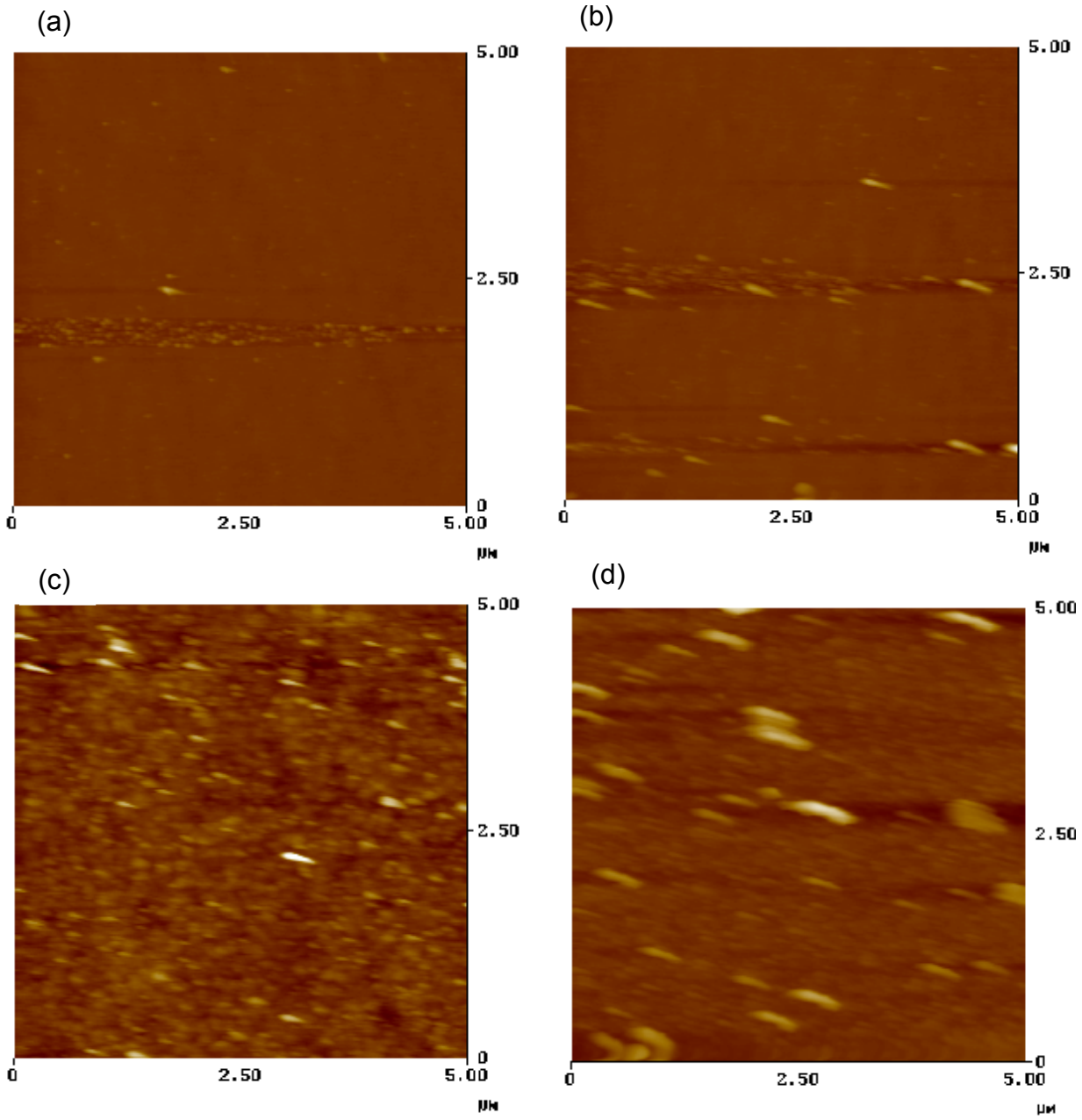



Fig. 89. AFM photographs for (a) GaAs capping layer, (b) upper LT-AlGaAs, (c) n-GaAs channel layer, and (d) Lower LT-AlGaAs in a MESFET structure consisting of LT-AlGaAs and AlAs materials. Upper refers to the layer grown above the channel, while lower is used for the layer below the channel.

as backside barrier, and the LT layer (upper) on top of channel layer was used to improve the gate diode performance because of its high resistance and, thus, low leakage current at high temperatures. Two growth temperatures, 300°C and 350°C were used in an attempt to study the effects of the LT-AlGaAs. Table 10 lists the layer sequence for this heterojunction MESFET using LT-AlGaAs. The AlAs barrier layers prevent the out-diffusion of As from the LT-AlGaAs so that the high temperature performance properties of the channel and the gate are assured. In other words, the high temperature reliability is improved.

Table 10. The detailed profile of the heterojunction MESFET using LT-AlGaAs as gate contacting and buffer layers. AlAs layers were used as diffusion barriers.

| Material | Composition | Doping Level | Thickness |
|---|---|---|---|
| iGaAs | | Unintentional doped | 10nm |
| AlAs | | | 10nm |
| LT-AlGaAs | 30% Al | | 100nm |
| AlAs | | | 10nm |
| nGaAs | | $N_d=3x10^{17}$ $cm^{-3}$ | 100nm |
| iGaAs | | Unintentional doped | 3nm |
| AlAs | | | 20nm |
| LT-AlGaAs | 30% Al | | 200nm |
| iGaAs | | Unintentional doped | 50nm |
| GaAs Substrate | | Semi-insulating | 450μm |

### 5.4.3 Device performance

Figs. 90(a) and (b) show the $I_d$ versus $V_{gs}$ characteristics at temperatures from 25°C and 400°C for devices made on wafers E9231 and E9232. The pinch-off characteristics at 25°C and at higher temperatures for devices made on E9232 were always better than those on E9231. For example, the current on/off ratio at 25°C was improved dramatically from ~$4x10^4$ to ~$3x10^7$ when the growth temperature of LT-AlGaAs was lowered from 350°C to 300°C. However, no significant improvement of the device performance in terms of drain current on/off ratio at 400°C was found for devices made on either E9231 or E9232. The ratio was found to be ~6 at 400°C for both devices. A detailed analysis of the current on/off ratio at high temperature will be given in Section 5.5. The pinch-off voltages of these devices were found to be higher than that calculated by Eq. 23 because of the IR drops on the gate diode.

Figs. 91 and 92 show I-V characteristics of the gate diodes at temperatures from 25°C and 400°C for devices fabricated on wafers E9231 and E9232, respectively. Diodes fabricated on wafers E9231 and E9232 have similar performance. From the linear I-V plot, the turn-on voltage at each temperature (defined as 1 mA/mm of gate current or 0.1 mA for these 2 x 100 $\mu m^2$ devices) can be extracted. Table 11 lists the respective turn-on voltage at temperatures between 25°C to 400°C for devices on both wafers. The high-temperature behavior of TiPtAu gate metal to LT-AlGaAs grown at 300°C and 350°C is quite similar to each other so the turn-on voltages are almost identical in both cases. However, since the AlGaAs grown at 300°C has higher resistance than that

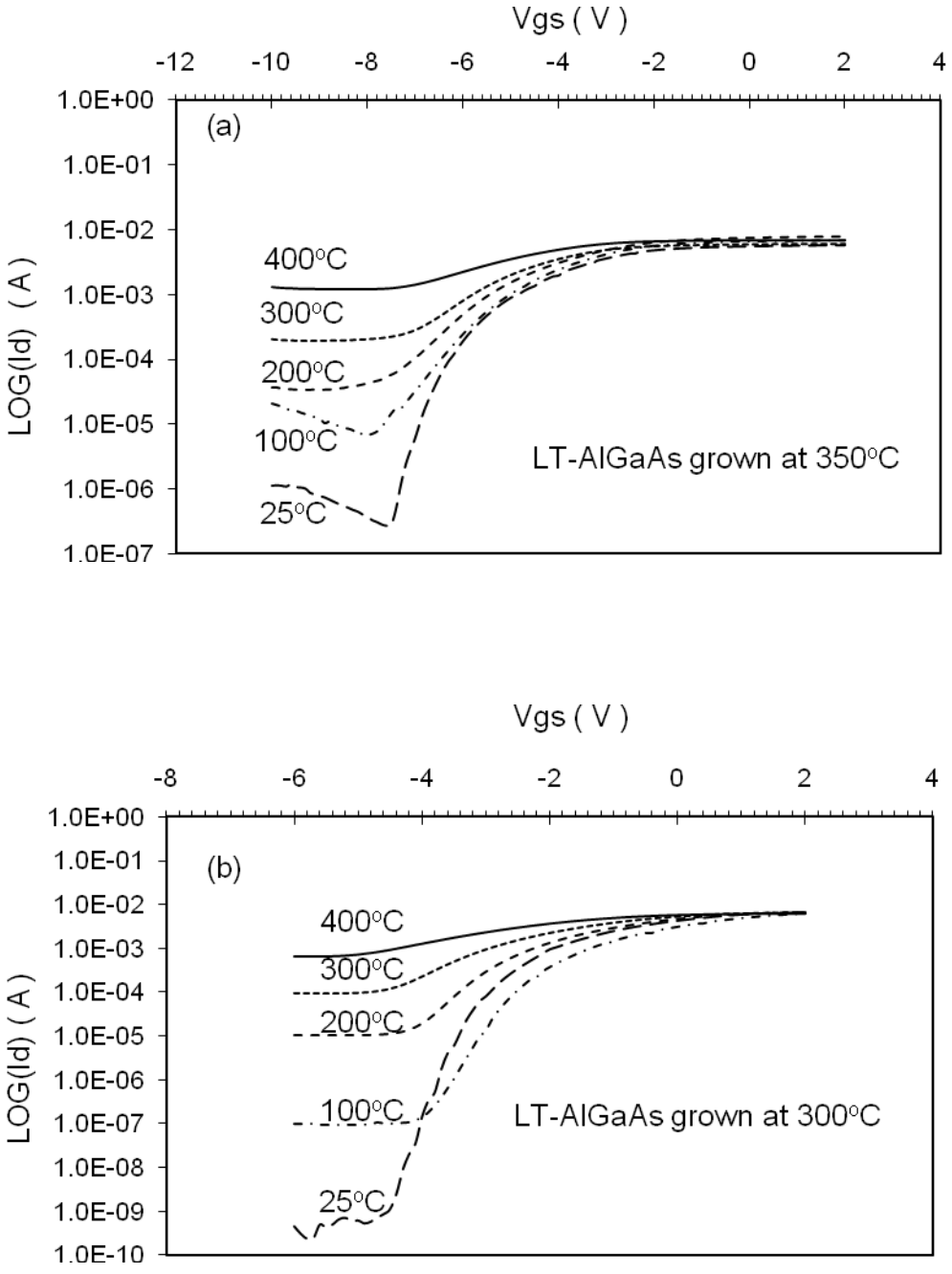



Fig. 90. $I_d$-$V_{gs}$ characteristics at temperatures from 25°C to 400°C for MESFET fabricated with LT-AlGaAs grown at (a) 350°C and (b) 300°C.

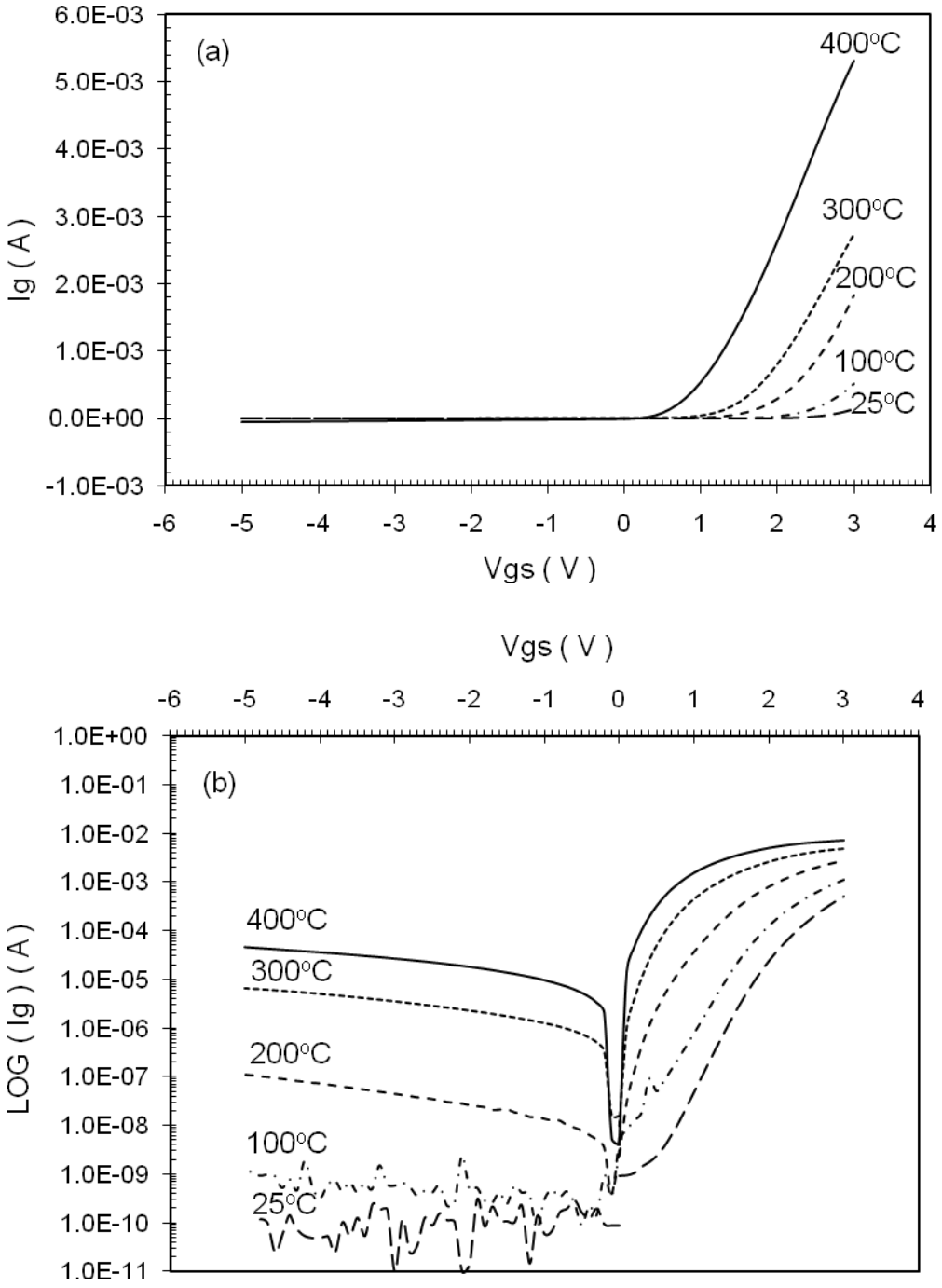



Fig. 91. Current-voltage characteristics at temperatures between 25°C to 400°C in (a) linear and (b) log scale of a representative gate diode fabricated on LT-AlGaAs grown at 350°C.

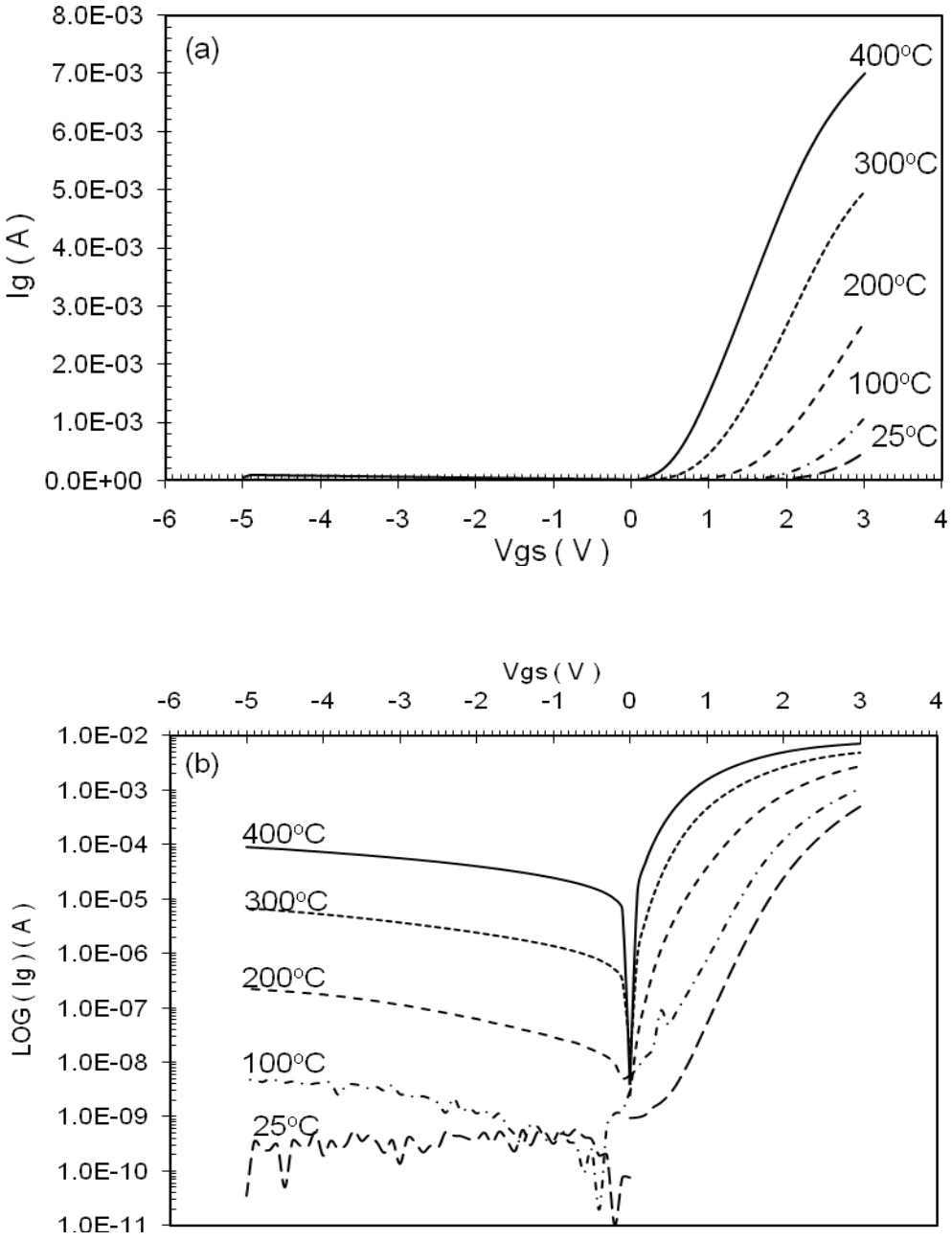



Fig. 92. Current-voltage characteristics at temperatures from 25°C to 400°C in (a) linear and (b) log scale of a representative gate diode fabricated on LT-AlGaAs grown at 300°C.

Table 11. Gate turn-on voltages and reverse currents at temperatures from 25°C to 400°C for TiPtAu gate to LT- $Al_{0.3}Ga_{0.7}As$ grown at 300°C and 350°C.

| Temperature | E9231( Avg. ρ = 673.9Ω/□ ) | | E9232( Avg. ρ = 1340.1Ω/□ ) | |
|---|---|---|---|---|
| | Turn-on Voltage, V | Reverse Current* | Turn-on Voltage, V | Reverse Current* |
| 25°C | 2.4V | 190pA | 2.4 V | 35pA |
| 100°C | 1.95V | 4.7nA | 2.0 V | 1.15nA |
| 200°C | 1.25 V | 230nA | 1.3 V | 113nA |
| 300°C | 0.6 V | 68.4 μA | 0.6 V | 67.0 μA |
| 400°C | 0.3 V | 89.0 μA | 0.3 V | 45.4 μA |

* Measured at –5.0V

grown at 350°C, as can be seen from the average sheet resistivity specified in the first row in Table 11, the reverse leakage current measured at – 5.0 volts for the gate diodes on wafer E9232 is always less than the reverse leakage current measured on wafer E9231.

Originally, if the resistivity of LT-AlGaAs epilayer is sufficient to achieve true metal-insulator-semiconductor (MIS) like gate characteristics, the structure usedin this dissertation provides a certain possibility for realizng a MIS field effect transistor (MISFET) using LT-AlGaAs as the gate insulator. The characteristics of the gate “diode” have to be determined in order to verify the carrier transport mechanism. There are potentially several mechanisms that can dominate the carrier transport in metal-insulator-semiconductor systems. Besides the Schottky emission, which has been mentioned in Chapter 4, Frenkel-Poole (FP) [28] and Fowler-Nordheim (FN) [29] mechanisms are commonly seen in insula-

tor/semiconductor interfaces. To aid in identifying each mechanism, the current-voltage characteristics at constant temperature can be plotted as current/voltage$^2$ versus 1/V for FN and Log (I) versus $V^{1/2}$ for FP. If there appears to be a linear fit in the form of a Log (I) versus $V^{1/2}$ plot, the current transport is mainly through the Frenkel-Poole mechanism. If the linear fit is better for the current/voltage$^2$ versus 1/V plot, the Fowler-Nordheim mechanism dominates. For thermionic emission, the mechanism can be verified using thermal activation measurements of the saturation currents as a function of temperature.

Figs. 93(a) and (b) show the I-V characteristics, current/voltage$^2$ versus 1/V and (b) Log (I) versus $V^{1/2}$, for diodes made from TiPtAu/LT-$Al_{0.3}Ga_{0.7}As$ grown at 350°C and grown at 300°C, respectively. In Fig. 93(a), diodes made from TiPtAu/LT-$Al_{0.3}Ga_{0.7}As$ grown at 350°C had a linear part, region A, at the high-field region, indicating the FN mechanism. This linear region extended to a voltage of 0.5 V and showed a change in slope at the lower field region. The FN mechanism seems to be favored because the thickness of LT-AlGaAs was relatively thick (100 nm) so that it was necessary to apply high voltages to the system to reduce the barrier width to a sufficiently small value in order to observe the Fowler-Nordheim type of tunneling effect [29].

The FN plot also shows that diodes made by TiPtAu/LT-$Al_{0.3}Ga_{0.7}As$ grown at 300°C had a small linear part of the curve for voltages higher than 2V. The FN mechanism appears to not be the dominant current transport mechanism for the diodes made from TiPtAu/LT-$Al_{0.3}Ga_{0.7}As$ grown at 300°C. The FP plot, the Log (I) versus $V^{1/2}$ plot, for diodes made by TiPtAu/LT- $Al_{0.3}Ga_{0.7}As$ grown at 350°C and

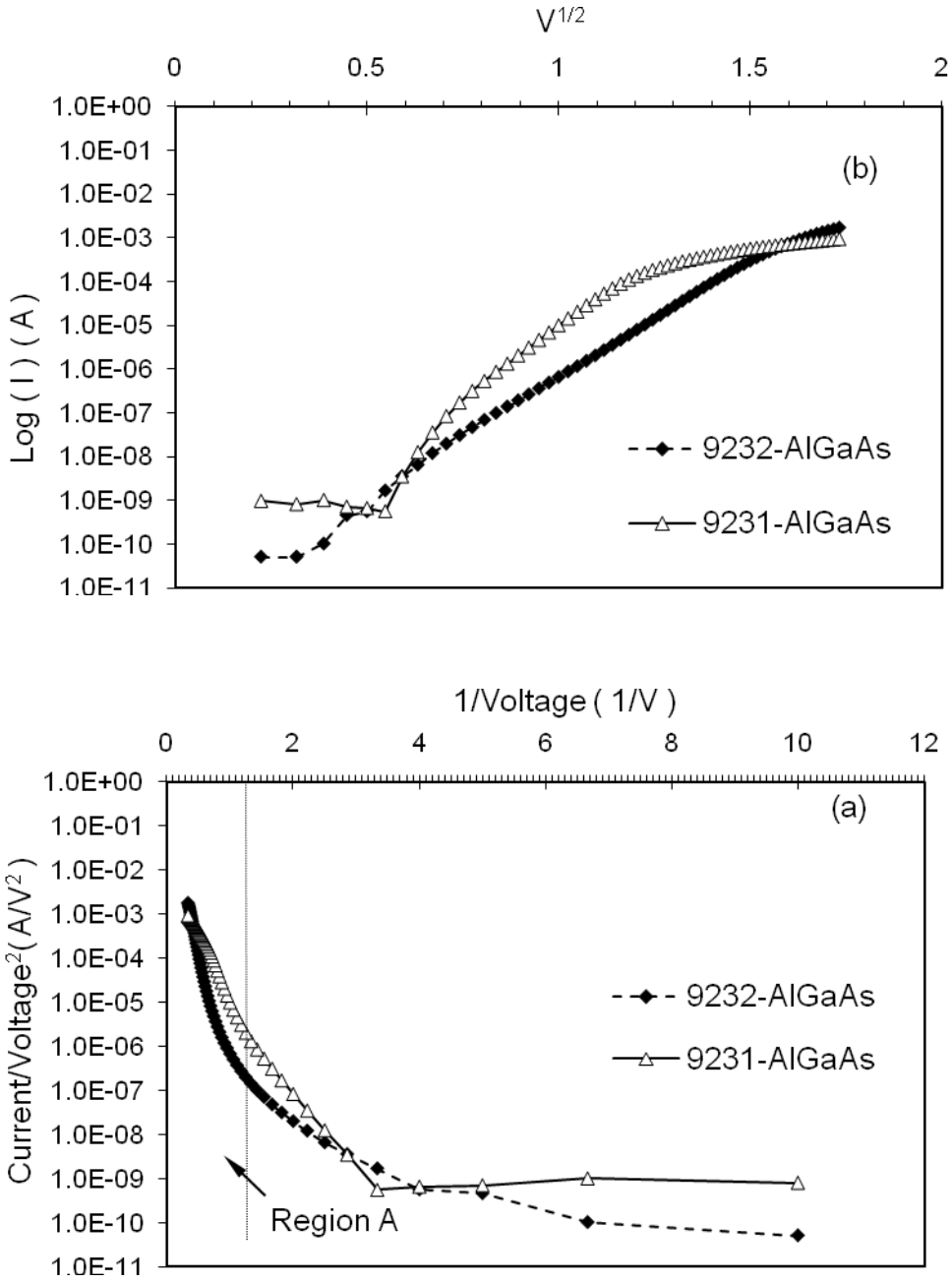



Fig. 93. Determination of carrier transport mechanisms for TiPtAu contacts to LT-AlGaAs materials grown at 300°C and 350°C, respectively, using (a) Fowler-Nordheim and (b) Frenkel-Poole plots.

grown at 300°C, respectively, are shown in Fig. 93(b). It was difficult to say if curve for the LT- $Al_{0.3}Ga_{0.7}As$ grown at 300°C fits the equation well. However the curve did fit quite well for $Al_{0.3}Ga_{0.7}As$ grown at 350°C for the voltage range from 0.5 V to 2.0 V. This fit supports a mechanism involving the thermal excitation of electrons from traps into the conduction band of the insulator [28].

Fig. 94 shows the saturation currents versus the reciprocal temperature plot of diodes made from TiPtAu gate metal to LT-AlGaAs grown at 350°C and

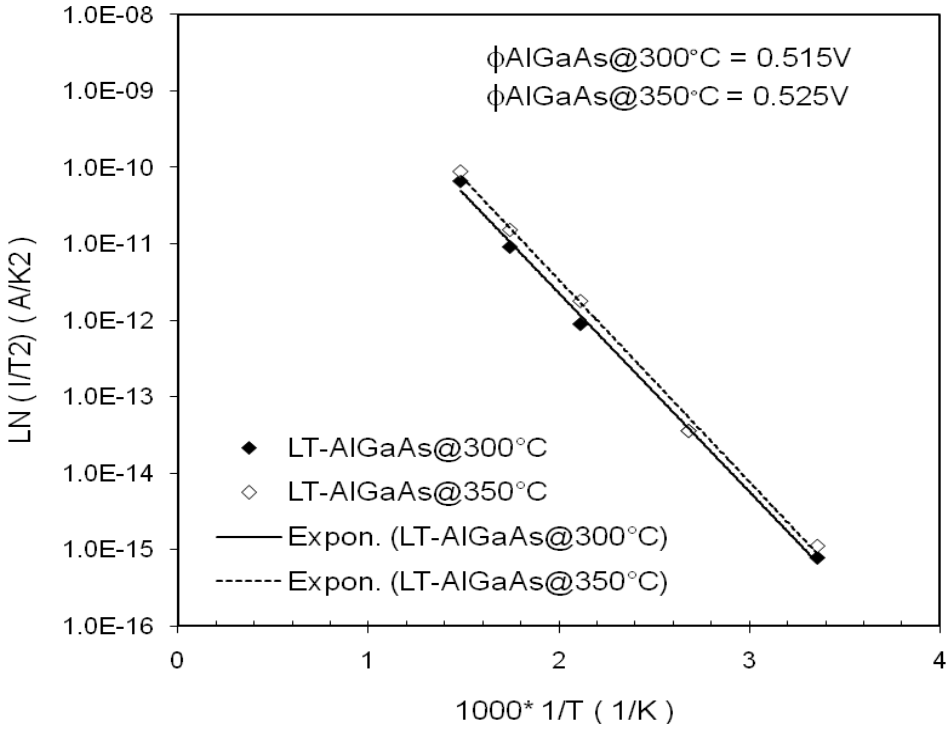



Fig. 94. Activation energy measurements for the saturation current of TiPtAu Schottky contacts to LT-AlGaAs materials grown at 300°C and 350°C, respectively.

300°C, respectively. The excellent linear relationship in both cases indicates that the gate currents were mainly dominated by thermionic emission so that the devices here behave as MESFETs instead of MISFETs.

### 5.4.4 Comparison between monolithic GaAs FETs and HFETs

#### 5.4.4.1 Reduction in gate leakage currents

There are two effective ways which have been proven to reduce gate leakage currents at high temperatures in this study: First, applying wide band-gap materials such AlGaAs to replace GaAs. Second, the use of p-AlGaAs on top of n-AlGaAs to make JFET structures.

Figs. 95 and 96 show the $I_d/I_g$ versus $V_{ds}$ curves at 300°C and 400°C, respectively, for MESFETs fabricated with LT-AlGaAs grown at 350°C having a gate length of 2 μm. Even at 400°C, the gate leakage current density, $9x10^{-7}$ A/μm at $V_{ds}$= 3 V and $V_{gs}$= -7 V, was extremely low. According to the calculations in Chapter 4, a calculated barrier height of 1.33 eV is needed to make the gate leakage current density reach such a small value. However, many attempts to precisely characterize the barrier height of the Schottky diodes failed to give a number close to 1.33 eV. From the Log (I) vs. V plot, values greater than 2.0 eV were obtained, but the ideality factors were much greater than unity. If the turn-on voltage is defined as the voltage to give a 1mA/mm current, then the typical value for the turn-on voltage is around 2.4 V for these MESFETs. The $1/C^2$ versus voltage characteristics resulted in a much higher built-in potential and, thus, barrier height for the gate diode. Because, in the low field region, the linearity in

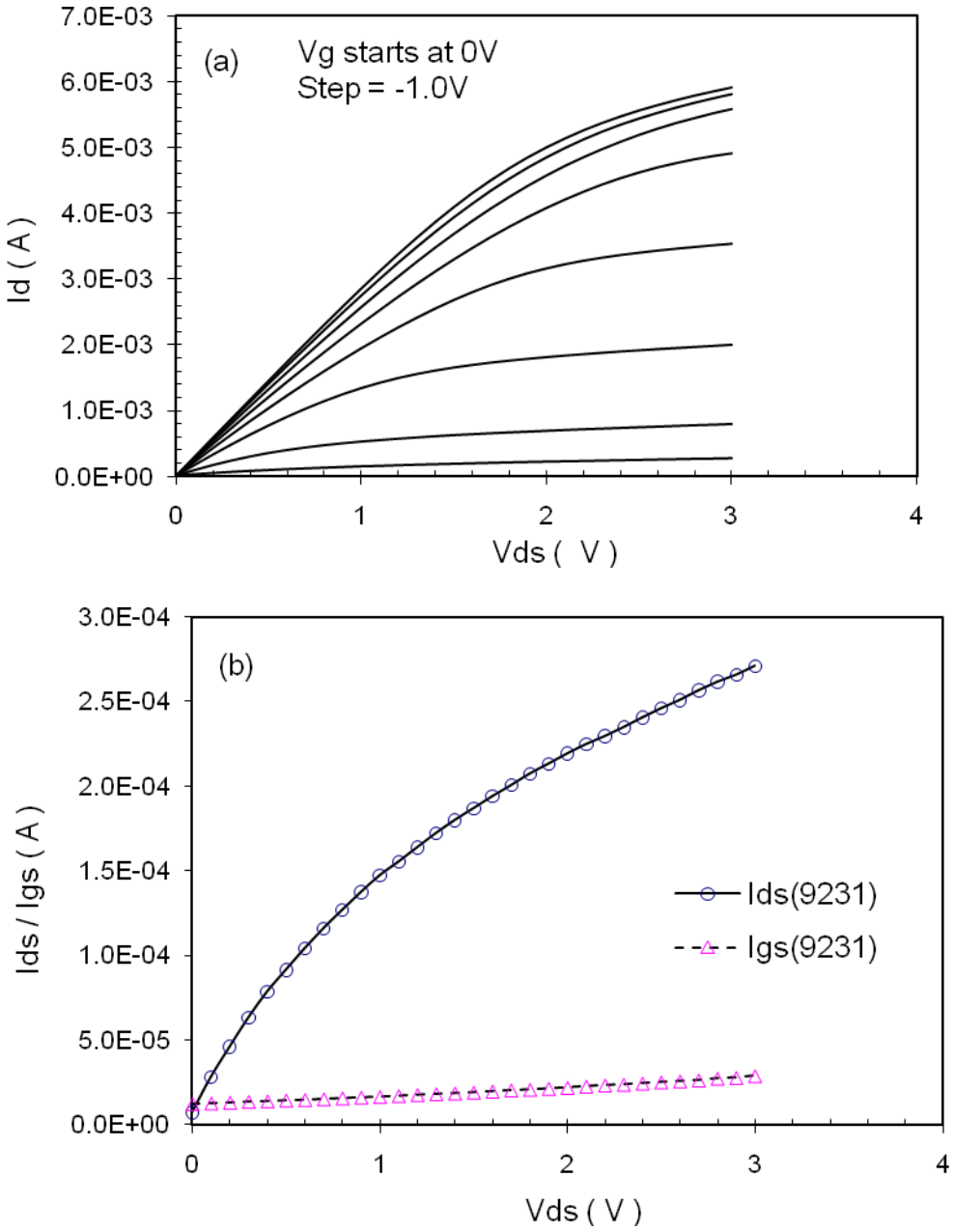



Fig. 95. Current-voltage characteristics at 300°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) drain and gate leakage currents at pinch-off at an equivalent gate voltage of -7.0 V, for a representative MESFET fabricated with LT-AlGaAs grown at 350°C.

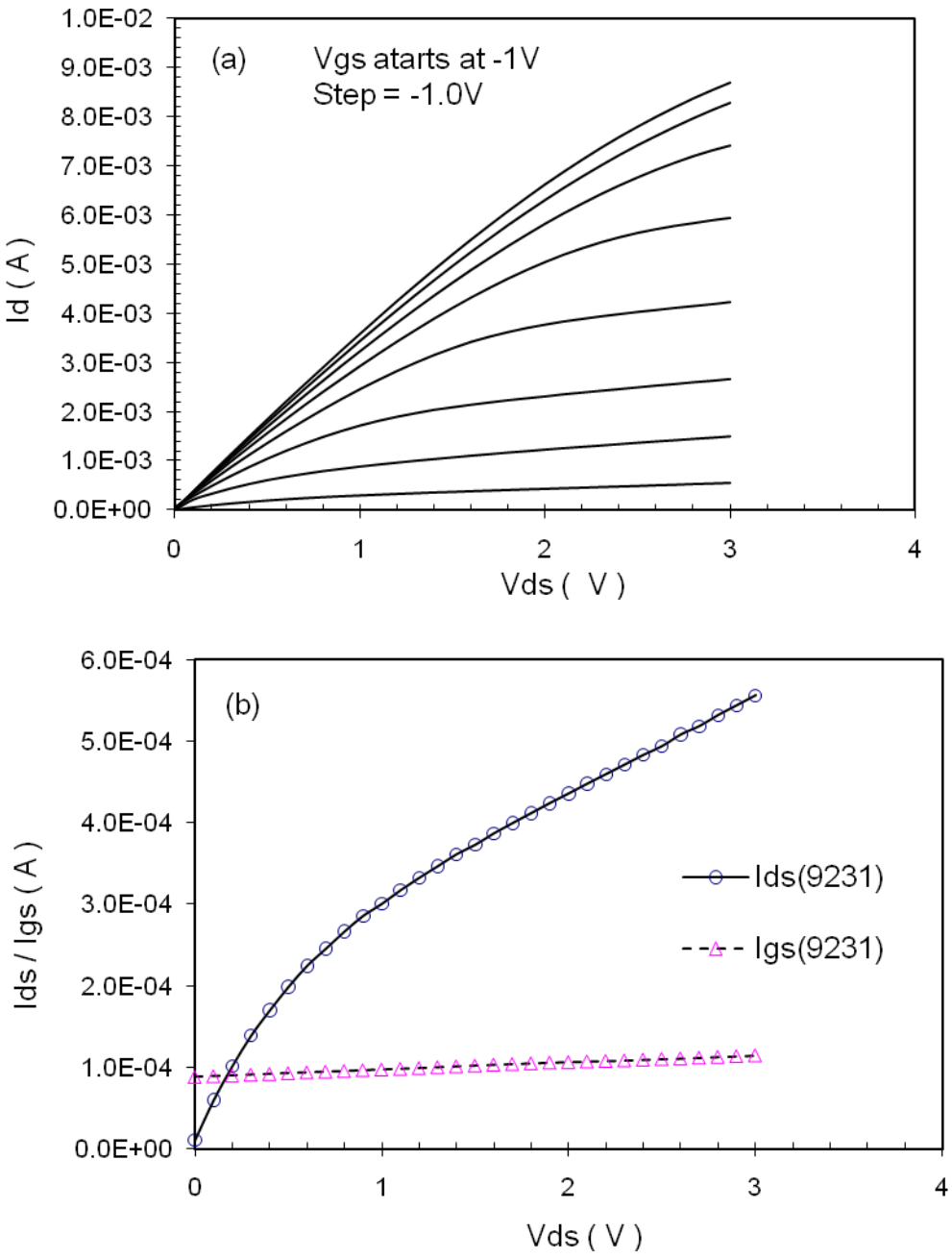



Fig. 96. Current-voltages characteristics at 400°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) drain and gate leakage currents at pinch-off at an equivalent gate voltage of -8.0 V, for a representative MESFET fabricated with LT-AlGaAs grown at 350°C.

the $1/C^2$ versus voltage plot does not fit very well, it is difficult to make a precise determination of the barrier height. This lack of a good fit is believed to be associated with the defect states in low-temperature grown AlGaAs. It is further believed that the barrier height for metal contacts to LT-AlGaAs is so high because of extremely low saturation current measured from the gate diode at room temperature, that, even with the existence of defect states, the total leakage current remains low.

MESFETs fabricated with LT-AlGaAs grown at 300°C had similar results as can be seen in Figs. 97 and 98 which show the $I_d/I_g$ versus $V_{ds}$ curves at 300°C and 400°C, respectively. The major difference between the two LT-AlGaAs cases was the gate leakage currents at temperatures from 25°C and 400°C.

The leakage currents were always higher in the devices fabricated with the LT-AlGaAs grown at 350°C due to the lower resistivity compared with the leakage currents for the LT-AlGaAs grown at 300°C.

The total drain leakage currents for MESFETs fabricated with LT-AlGaAs grown at 300°C were found to be higher than those fabricated with LT-AlGaAs grown at 350°C; this result makes sense and is quite reasonable due to higher defects for materials grown at lower temperature. The effect of interface roughness scattering on pinch-off characteristics has been noticed as the gate pinch-off voltage changed from -7.0 V for devices fabricated with LT-AlGaAs grown at 300°C to –8.0 V for devices fabricated with LT-AlGaAs grown at 350°C. In reviewing the profile in Table 10, an AlAs layer grown under normal conditions inserted between the n-GaAs channel layer and LT-AlGaAs buffer layer is

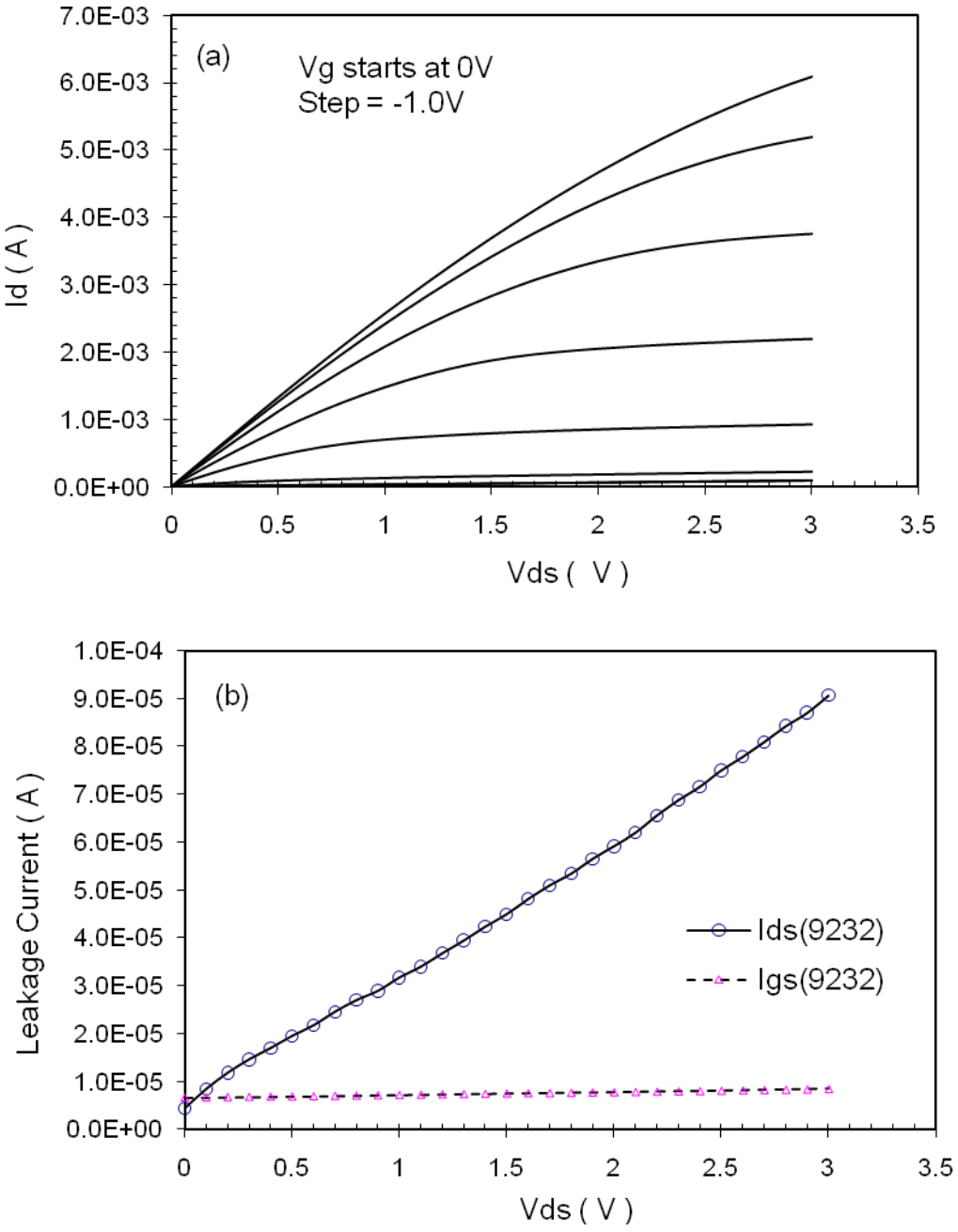



Fig. 97. Current-voltages characteristics at 300°C demonstrated by (a) $I_d$-$V_{ds}$, and (b) drain and gate leakage currents at pinch-off, at an equivalent gate voltage of -6.0 V, for a representative MESFET fabricated with LT-AlGaAs grown at 300°C as the gate contacting and buffer layers.

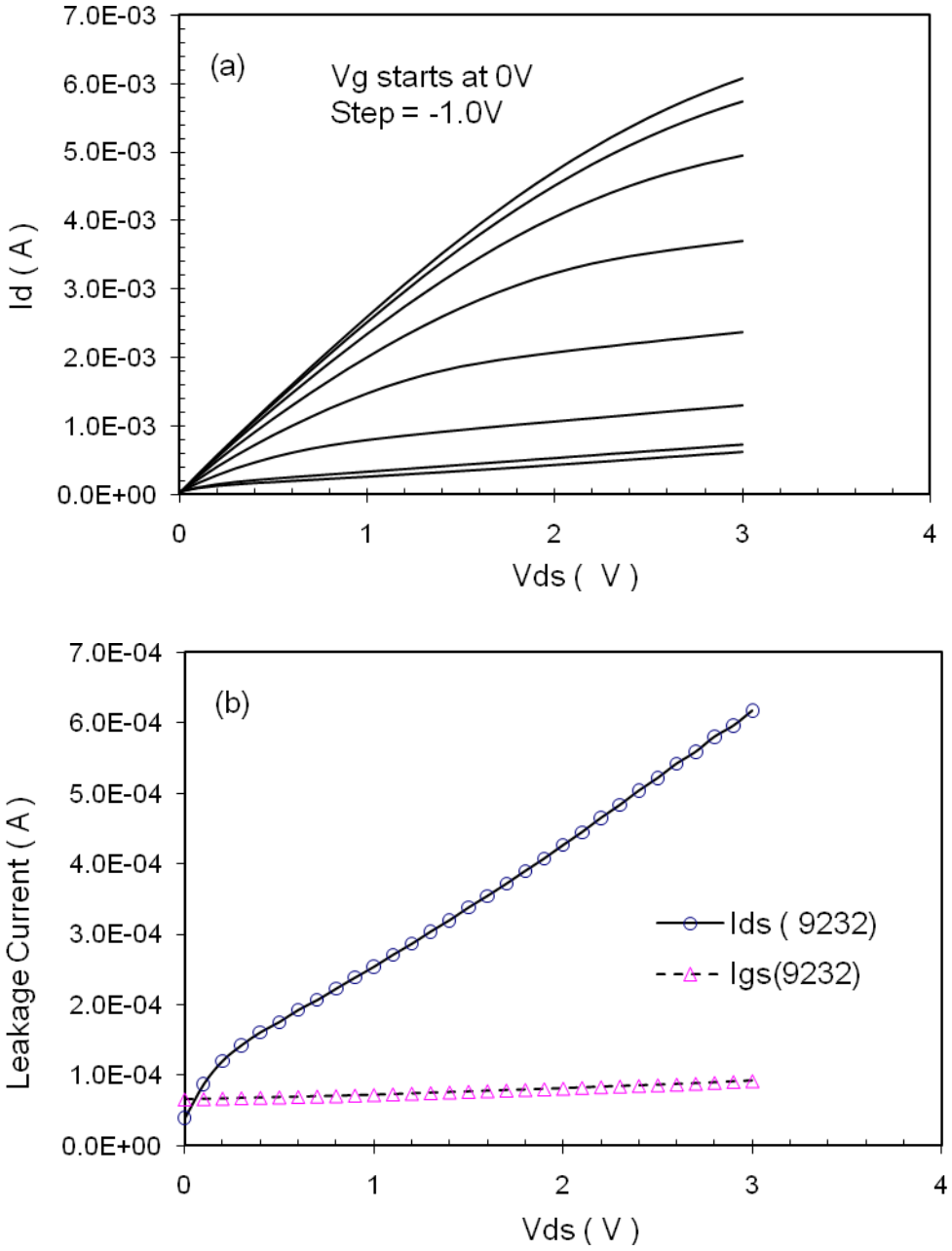



Fig. 98. Current-voltages characteristics at 400°C demonstrated by (a) $I_d$-$V_{ds}$ characteristics, and (b) drain and gate leakage currents at pinch-off, at an equivalent gate voltage of -7.0 V, for a representative MESFET fabricated with LT-AlGaAs grown at 300°C as the gate contacting and buffer layers.

thought to prevent point defects in LT-material from propagating to the channel [30]. Therefore the interface scattering plays a less significant role in affecting the device characteristics at high temperatures. However, based on I-V characterization results, it is necessary to optimize the material properties of AlAs and LT-material such as the thickness of AlAs, the growth temperature of LT-AlGaAs, and the composition of LT-material to further reduce the leakage currents. Contrary to the conductivity of LT-AlGaAs that has been shown to be lower at lower growth temperatures, interface scattering may be very severe in the devices with LT-AlGaAs grown at 300°C due to the relatively poor crystal quality [46]. Table 12 lists the gate leakage and drain leakage currents for all of the structures studied in this dissertation. The width of the devices was 100 μm and the gate length was 2 μm for all devices in this dissertation work.

Table 12. Comparison between gate and drain leakage currents in different structures at elevated temperatures.

| | Gate Contact Layer | Buffer Layer |
|---|---|---|
| | Gate Leakage Current, $I_g$ ( x$10^{-6}$ A ) | Drain Leakage Current, $Id_{sub}$( x$10^{-6}$ A ) |
| GaAs MESFET | n-GaAs | SI-GaAs |
| | 667* | 1460* |
| Heterojunction MESFET | n-$Al_{0.3}Ga_{0.7}As$ | AlAs |
| | 677 | 558 |
| Heterojunction HJFET | p-$Al_{0.3}Ga_{0.7}As$/ n-$Al_{0.3}Ga_{0.7}As$ | AlAs |
| | 531 | 862 |
| HMESFET-E9231 | LT- $Al_{0.3}Ga_{0.7}As$ @350°C | LT- $Al_{0.3}Ga_{0.7}As$ @350°C |
| | 114 | 560 |
| HMESFET-E9232 | LT- $Al_{0.3}Ga_{0.7}As$ @ 300°C | LT- $Al_{0.3}Ga_{0.7}As$ @ 300°C |
| | 92.1 | 617 |

*Measured at 300°C, all others, measured at 400°C.

Using wide band-gap materials such as AlGaAs grown at normal temperatures, instead of GaAs, as the gate contact layers, was found to reduce gate leakage currents of the heterojunction MESFETs at 300°C by a factor of 8. The gate leakage in heterojunction MESFETs investigated in this dissertation at 400°C is slightly higher than that of monolithic GaAs MESFETs at 300°C. This difference is attributed to the improved barrier height in heterojunction MESFET.

The gate current can be further reduced when the high-temperature HT-AlGaAs is replaced by LT-AlGaAs. A reduction factor greater than seven was achieved if the LT-AlGaAs was grown at 300°C, while it was ~ six for the LT-AlGaAs grown at 350°C. The high resistance of the LT-AlGaAs materials after annealing appears to have been responsible for such low gate leakage currents.

The smaller gate leakage current in the heterojunction JFET as compared with that in the heterojunction MESFET device is ascribed to the higher built-in potential of the gate pn junction for the heterojunction JFET structure. The performance of heterojunction JFETs in this study was not significantly improved because the built-in potential was much lower than the target value. This lower than expected built-in potential may possibly be due to the defects at the n-AlGaAs/p-AlGaAs interface resulting from the MOCVD growth. However, the carrier modulation in the heterojunction JFET is not as efficient as that in the heterojunction MESFET due to the additional gate capacitance (~400 pF for the heterojunction JFET versus 27 pF for the heterojunction MESFET).

5.4.4.2 Reduction in subthreshold drain leakage currents

The subthreshold drain leakage currents consist of substrate and gate leakage currents and the transition where one is dominant over the other depends on the barrier height and back-wall barrier layers, respectively. If 50% of the gate current contributes to the total drain leakage current, then, AlAs is a better buffer layer than LT-AlGaAs for the MESFET structure [7]. Semi-insulating GaAs is, at best, only fair at supporting device and circuit operation at temperatures higher than 250°C since the substrate becomes fairly conductive rather than insulating at higher temperatures.

If the conductance of a buffer layer as a function of temperature can be characterized separately, along with the gate leakage current, one can compare the total drain leakage current and evaluate whether the structure design results in any extra leakage currents in gated devices. The next section deals with the buffer conductance of Al-containing AlGaAs buffers.

## 5.5 Leakage currents on Al-containing AlGaAs buffers

A pictorial cross section of the devices used in the measurements of the buffer conductance is shown in Fig. 99. After the formation of the ohmic contacts, the devices were etched down to the buffer layer using wet etching in a chemical solution described in Chapter 2 Section 2.9. The CuGe-based ohmic contacts served as the mask during the etching process. Devices were 100 μm wide and had a drain-to-source spacing of 6 μm. The transconductance in units of mS/mm was calculated by measuring the total current and dividing by the voltage-width product for a given fixed gate length.

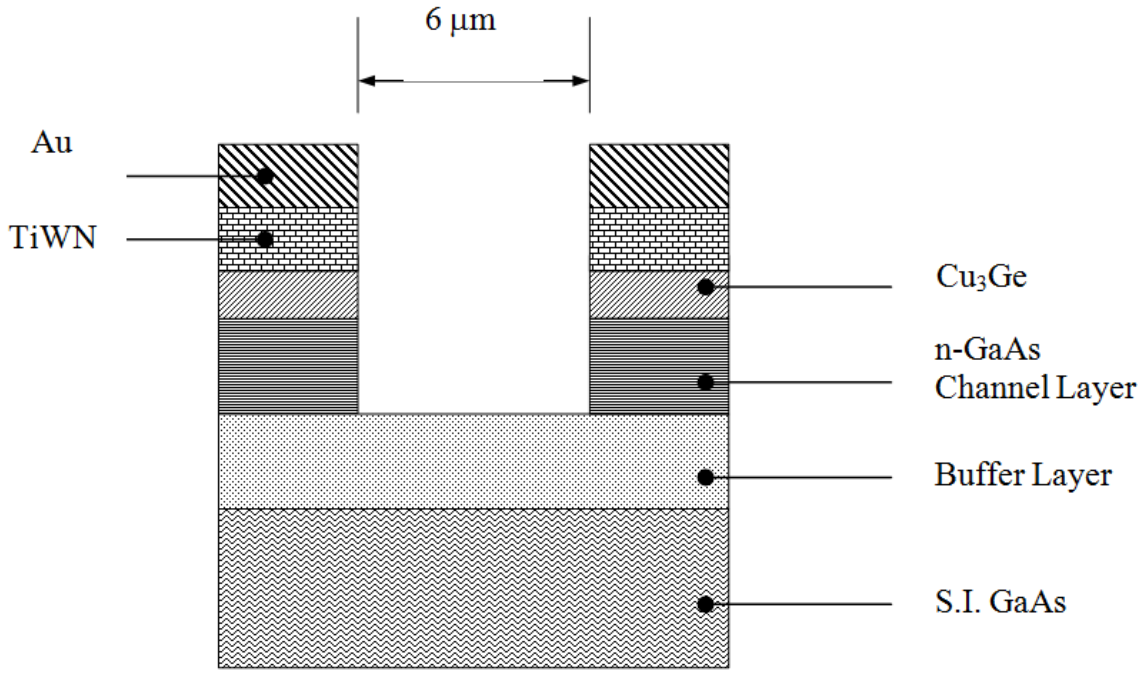



Fig. 99. Schematic representation of devices used for leakage current measurements. $Cu_3Ge$ contacts were used as the ohmic contacts to n-GaAs channel layer.

Fig. 100 shows the buffer conductance in log scale at temperatures from 25°C and 400°C for Al-containing buffers. The conductance of AlGaAs buffer is almost 50 times that of AlAs buffer at 400°C. With the only exception being the hopping of conductance in LT-AlGaAs and AlAs materials, the conductance of all buffers obeys an exponential relationship with respect to $T^{-1}$. The insert in Figure 100 shows an enlarged plot of the circled region in Fig. 100; hopping of conductance for AlAs and $Al_{0.3}Ga_{0.7}As$ materials grown at low temperatures can be seen at high temperatures.

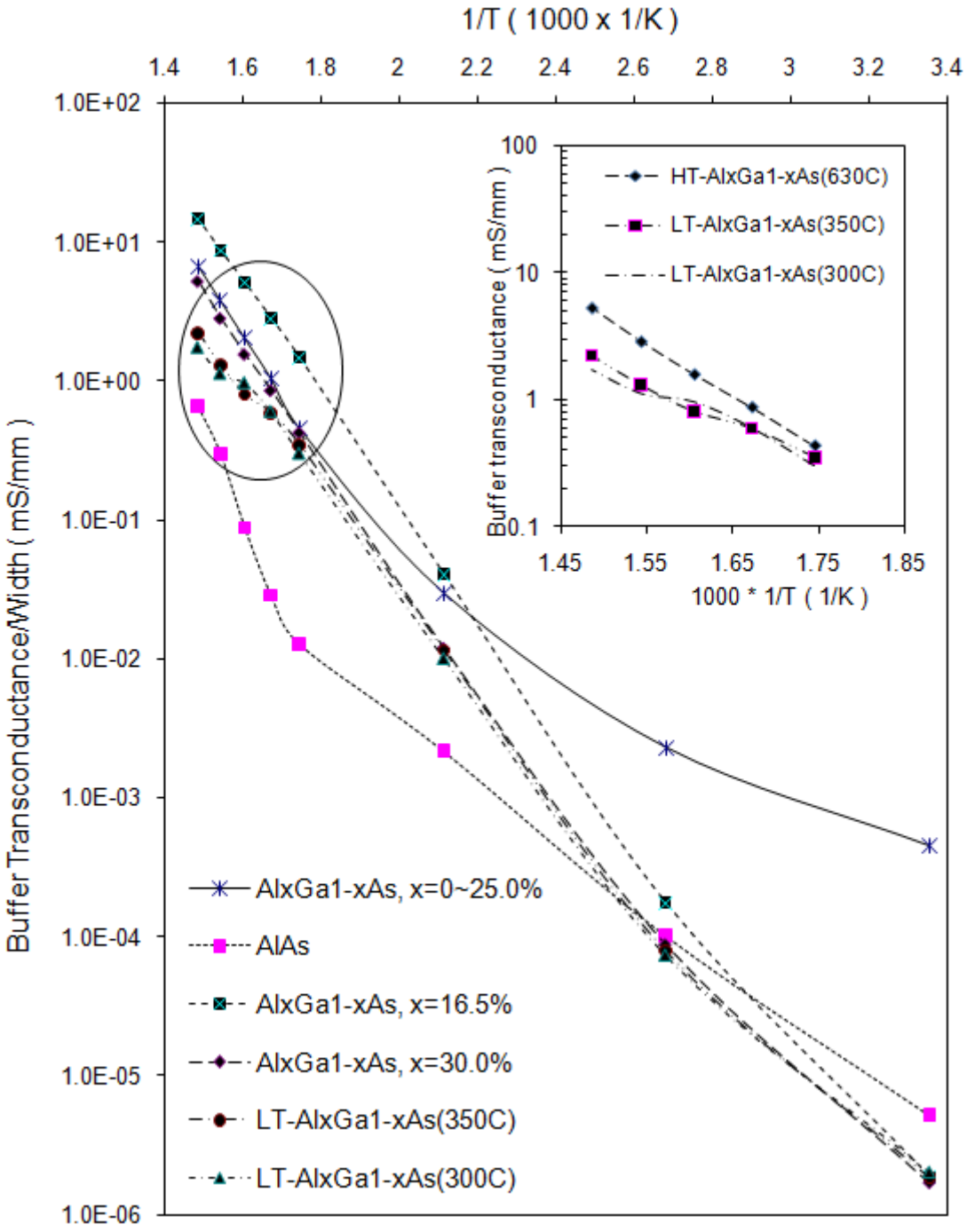



Fig. 100. Buffer transconductance in units of mS/mm at temperatures from 25°C and 400°C for several Al-containing semiconductors. The insert shows an enlarged plot for LT-AlGaAs buffers at temperatures from 300°C to 400°C.

Graded AlGaAs buffer (x = 0 to 25%) have the highest conductance in the temperature range between 25°C to ~ 200°C. However in the range between 300°C to 400°C, the graded AlGaAs buffer conductance falls in between the 30% and 16.5% Al buffers.

It is believed that the diffusion leakage current of AlGaAs at temperatures between 300°C to 400°C is dominant over the drift leakage current [50]. The activation energy, taken from the slope of conductance versus 1/T curve shown in Fig. 100, for each buffer material, along with the calculated band-gap energies, are tabulated in Table 13.

Comparing the $E_g/2$ of each buffer material with the activation energy extracted from the conductance versus $T^{-1}$ curves, there is a good agreement between the two values as the largest discrepancy between the two sets is only

Table 13. Summary of band-gap energies and activation energies for various Al-containing buffers.

| AlxGa1-xAs | Band-gap Energy by Theory [41], eV | | Activation Energy, eV |
|---|---|---|---|
| | $E_g$, eV | $E_g/2$, eV | |
| x=16.5 % | 1.54 | 0.77 | 0.765 |
| x=0~25 % | 1.608 | 0.804 | 0.866 |
| x=30.0 % | 1.647 | 0.824 | 0.835 |
| x=30.0 % [A] | 1.647 | 0.824 | 0.773 |
| x=30.0 % [B] | 1.647 | 0.824 | 0.767 |
| x=100.0 % | 2.16 | 1.08 | 1.312 |

A Grown at 350°C

B Grown at 300°C

50 meV. An intrinsic material property which is exponentially proportional to the reciprocal temperature is the intrinsic-carrier density of the buffer materials [50]. This result supports the proposal for the use of wide band-gap materials as the substrate of choice for high temperature electronics.

One of the significant accomplishments in this dissertation is the direct measurement of the substrate leakage in the sense of real device usage. The results indicate that if AlAs is used as the buffer, the substrate leakage current density at 400°C is as low as ~$7x10^{-7}$ A/μm at a forward bias of 1 V for a drain-source spacing of 6 μm. For the LT-AlGaAs buffer grown at 300°C, the calculated substrate current density at 400°C is ~ $5.2x10^{-6}$ μA/μm at $V_{ds}$= 3 V, while the total drain leakage current density measured in the real device is $6.2x10^{-6}$ μA/μm at 400°C; clearly the majority of the leakage current is from the substrate.

The hopping of the conductance in LT-AlGaAs buffers at temperatures between 300°C and 400°C is thought to reflect the carrier generation across the band-gap via the deep level states [51]. In a similar manner, the steep increase in conductance in the AlAs buffer is thought to be defect-state-related [51].

## 5.6 GaN-based MESFETs and MODFETs

### 5.6.1 Introduction

GaN-based materials are attractive for high-temperature electronics because of the low thermal generation rates and high breakdown fields inherent in wide band-gap semiconductors. High peak and saturation velocity ($V_p$ = $3.1x10^7$ cm/s, $V_s$ = $2.5x10^7$ cm/s, respectively) [31], chemical inertness, and a

fairly high thermal conductivity make GaN a very strong potential material for field effect transistors (FET) operating at elevated temperatures. The III-V nitrides certainly offer the additional advantage of heterojunction device design. Through heterojunction design, two-dimensional electron gas (2-DEG) structures have been demonstrated [32, 33, 37, 43].

### 5.6.2 Device fabrication

GaN-based MESFET and MODFET structures were grown on sapphire substrates using MBE. The cross sections of these two device structures are illustrated in Fig. 101. All of the structures had a buffer layer consisting of a 20 nm aluminum nitride (AlN) layer on a sapphire substrate, followed by a 3 μm unintentionally-doped (i) GaN layer. The active layers were then grown on this undoped 3 μm-thick GaN layer. The MESFET consisted of a 100 nm thick, $1x10^{17}cm^{-3}$ Si-doped channel thinned from an originally 2 μm layer and without a heavily doped ($n^{++}$) capping layer. The MODFET had a 20 nm thick, Si-doped AlGaN epilayer with an Al composition of 30 % and a 1 μm thick, undoped GaN channel layer. The sheet carrier concentration and Hall mobility were measured as $1.3x10^{12}$ $cm^{-2}$ and 960 cm/Vsec, respectively. All of the FETs were fabricated with a source-drain spacing of 6 μm. The gate length was 2 μm and the width varied from 100 μm to 200 μm. The wafer was first covered with a 300 nm-thick, sputtered Ti layer to act as a mask prior to patterning of the device via photolithography. Processing steps are similar to those that have been described for GaAs-based devices [56].

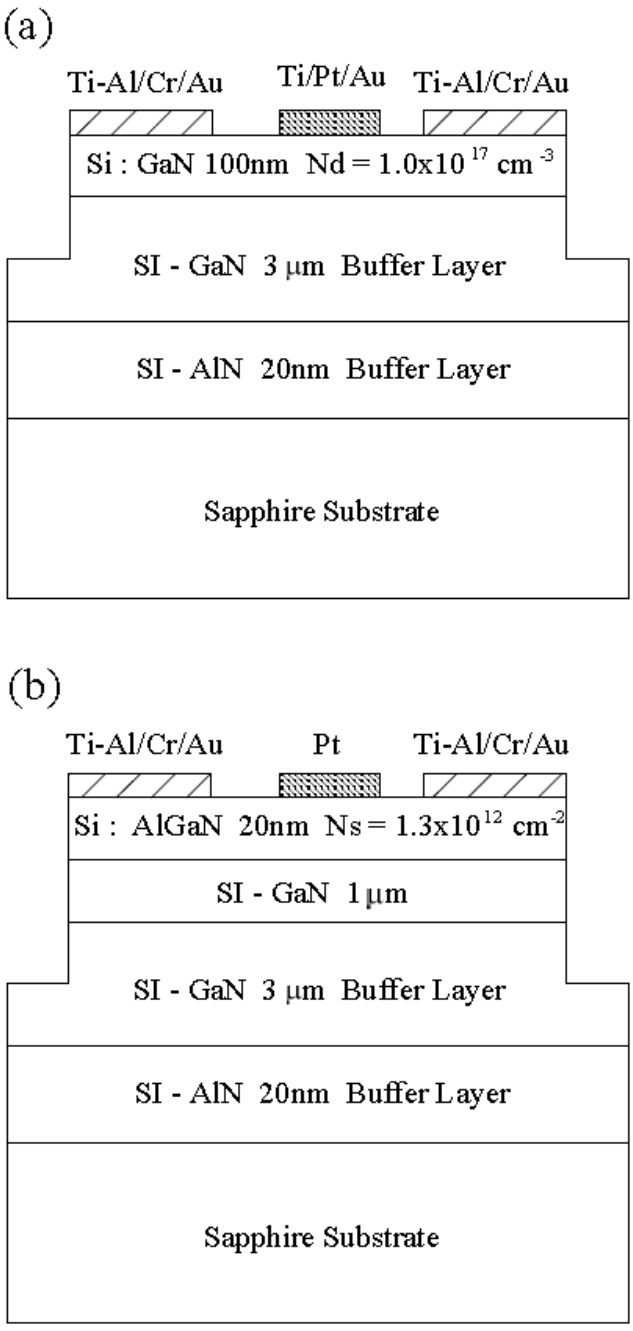



Fig. 101. Cross-sectional views of (a) Si-doped MESFET and (b) AlGaN/GaN MODFET.

The major difference in processing between the GaN-based devices and GaAs-based devices is that the wet etching was ruled out in the case of GaN-based devices. The trench etching for device isolation was carried out by reactive ion etching (RIE) using a chlorine (Cl) based plasma. The final depth of the mesa is close to 2 μm. The Ti mask is then removed in HF solution and the contact windows were exposed. The wafer was plasma etched for 30 sec in $CF_4$ and Ar plasma. Then the Ti-Al ohmic contacts were deposited using e-beam evaporation.

Fig. 102 shows a plot of the specific contact resistance versus annealing time. The annealing condition was optimized and found to be 600°C for 5 min for TiAl to n-type GaN with a doping density of $1.0x10^{17}cm^{-3}$. As can be seen from

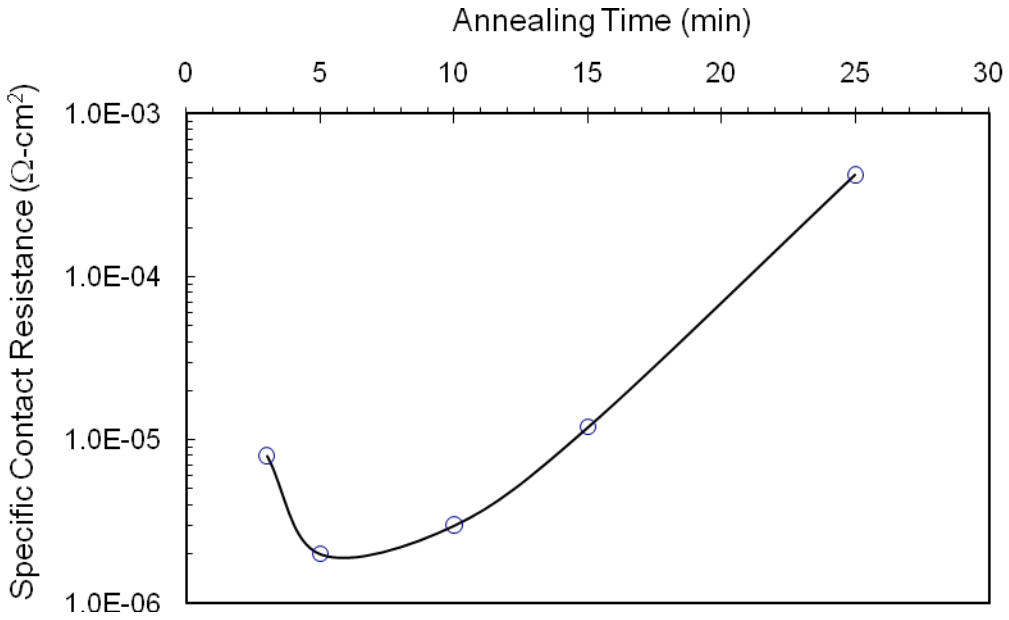



Fig. 102. Specific contact resistance of TiAl ohmic contacts to n-type GaN as a function of annealing time at 600°C in $N_2$ ambient.

Fig. 102, the minimum contact resistance is attained for annealing times on the order of 5 min.

TiAl is thermally stable at temperatures up to 400°C if protected with TiWN or Cr/Au. Fig. 103 shows the excellent performance of this ohmic contact scheme at 400°C for up to 150 hrs. Fig. 104 shows the optical photographs for the as-fabricated devices in which the gate dimension was 2 μm. The devices are covered with $Si_3N_4$ except for the bright rectangular windows on which Cr and Au layers are sequentially deposited by sputtering for the electrical probing. The contact resistance of TiAl to n-type AlGaN was much higher than the contact resistance of TiAl is to n-GaN.

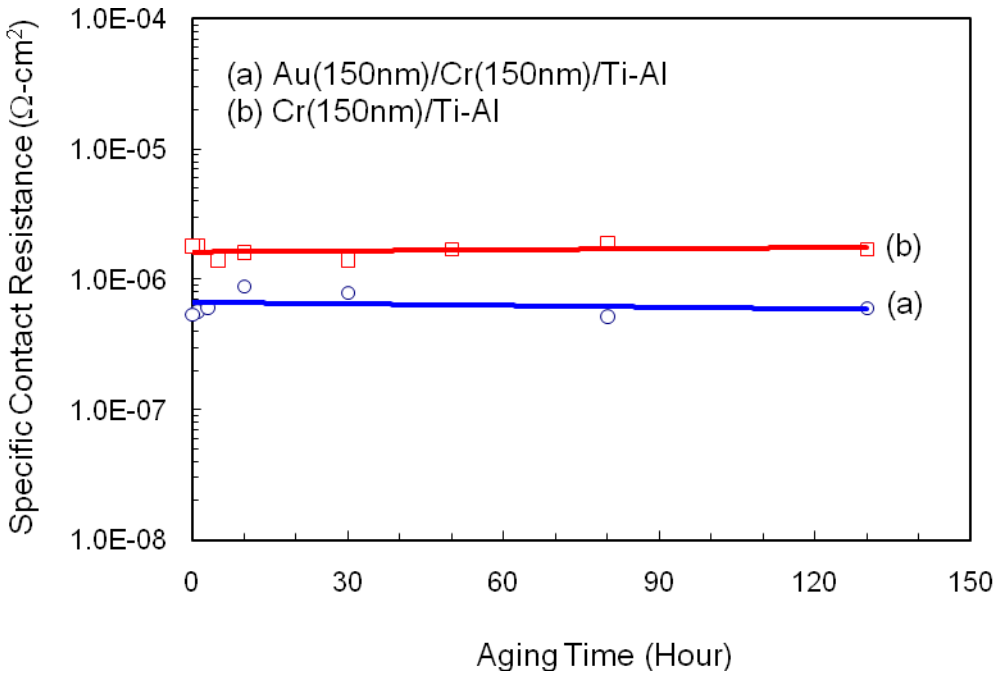



Fig. 103. Results of aging tests at 400°C for TiAl ohmic contacts to n-type GaN protected by a Cr diffusion barrier and an Au over layer.

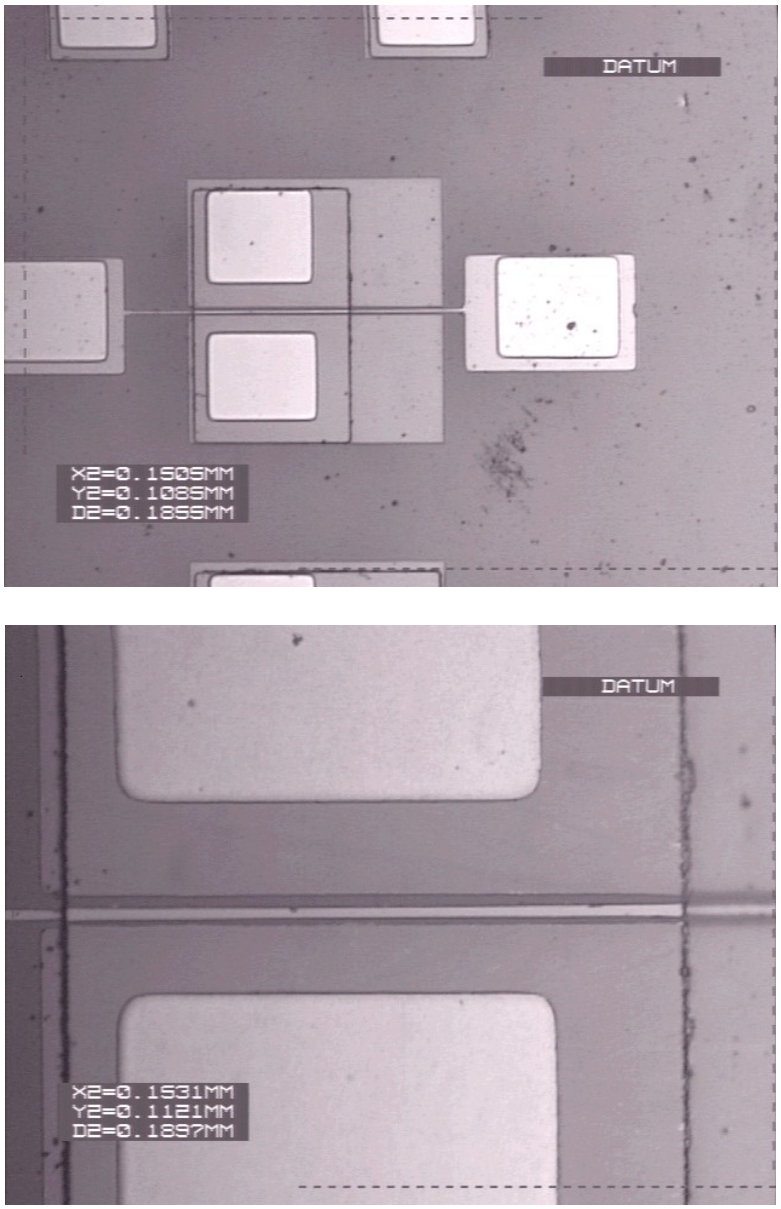



Fig. 104. Photographs of an (a) as-fabricated AlGaN/GaN MODFET with TiAl ohmic contacts and Pt Schottky contacts, and (b) an enlargement of circled area in (a).

The specific contact resistance was approximately two orders of magnitude higher for the case of n-AlGaN than for n- GaN, but the contact resistance of TiAl to n-type AlGaN was still lower than $1.0x10^{-4}$ $\Omega cm^2$. Further studies to improve the contact resistance are necessary for increasing the output power of the AlGaN/GaN devices.

The I-V characteristics of Pt, Au, and W Schottky contacts to n-type AlGaN are shown in Fig. 105. The forward I-V characteristics are exponential over 7 decades of current with ideality factors ranging from 1.05 to 1.15. The reverse leakage current densities at –90 V were 0.12 μA/mm, 0.60 μA/mm, and 5.38 μA/mm, for Pt, Au, and W, respectively. The measured barrier heights in this dissertation for Pt, Au, and W were 0.97 eV, 0.86 eV, and 0.63 eV, respectively. These results reflect the dependence of the barrier height on metal work function because Pt has the largest work function of 5.65 eV, followed by that of Au, 5.1 eV, than that of W, 4.55 eV [34-36]. However, the quantitative relation between the magnitude of barrier and metal work function does not give satisfactory results. For example, Pt and Au contacts to n-type AlGaN have a difference of only 0.11 eV in the barrier heights, whereas there is 0.55 eV difference in the work functions between Pt and Au.

It appears that there may not be an advantage of using a wide band-gap semiconductor, such as AlGaN, to improve the barrier height in GaN-based materials as has been shown to be very effective in GaAs-based materials. For example, the Schottky barrier height of Pt to n-type GaN is also close to 1.0 ~ 1.1 eV [37] which is similar in magnitude to the SBH to AlGaN.

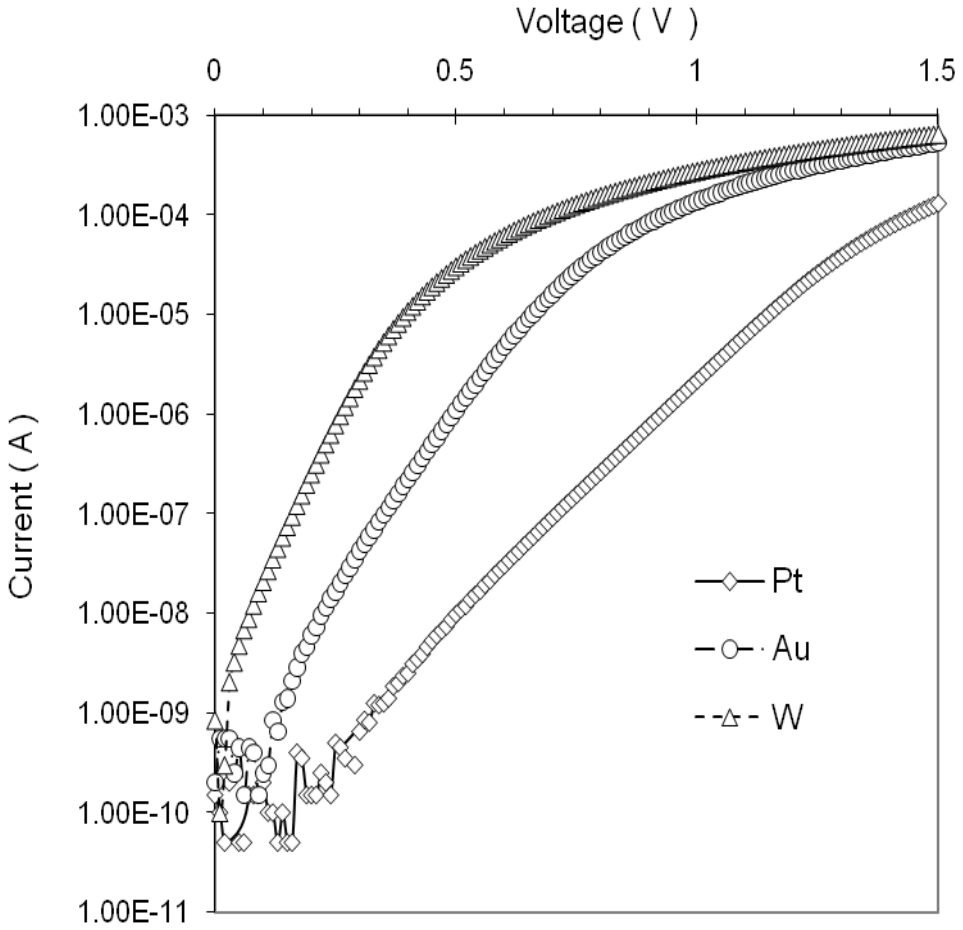



Fig. 105. Current-voltage characteristics for Pt, Au, and W Schottky contacts to n-type AlGaN with an Al composition of 30.0%.

From a leakage current point of view, the $Si_3N_4$/GaN MISFET might be able to reduce most of the gate leakage currents but the devices tend to have extremely high pinch-off voltages and low transconductance [38]. A more accurate picture of the Schottky barrier height dependence on material band-gap or band-gap discontinuity will emerge as GaN-based technology matures.

### 5.6.3 Device characterization

#### 5.6.3.1 GaN MESFET

Fig. 106(a) shows the $I_d$ versus $V_{gs}$ characteristics of a GaN MESFET at temperatures from 28°C to 400°C. The on/off current ratio at 400°C was only 5 because of the severe leakage currents from the Pt/n-GaN gate diode and the undoped GaN buffer layer. The device was completely pinched-off at –9 V gate bias at 25°C. The transconductance, which is not shown in the figure, remained relatively constant at 10 mS/mm from 25°C to 400°C without noticeable degradation. The I-V characteristics of the gate diode as a function of temperature are shown in Fig. 106(b). From Fig. 106(b), the poor performance of the gate Schottky diode can be seen. The reverse current at 400°C and at a gate bias of –10 V was as large as 1.4 mA. The weak rectifying property of the gate diode is believed to be due to the defects in the doped-GaN layer, which is close to the buffer layer.

It is well known that the threading dislocations may have a high density in or near the channel of a GaN-based device and that this high threading dislocation density may provide leakage paths at elevated temperatures [38].

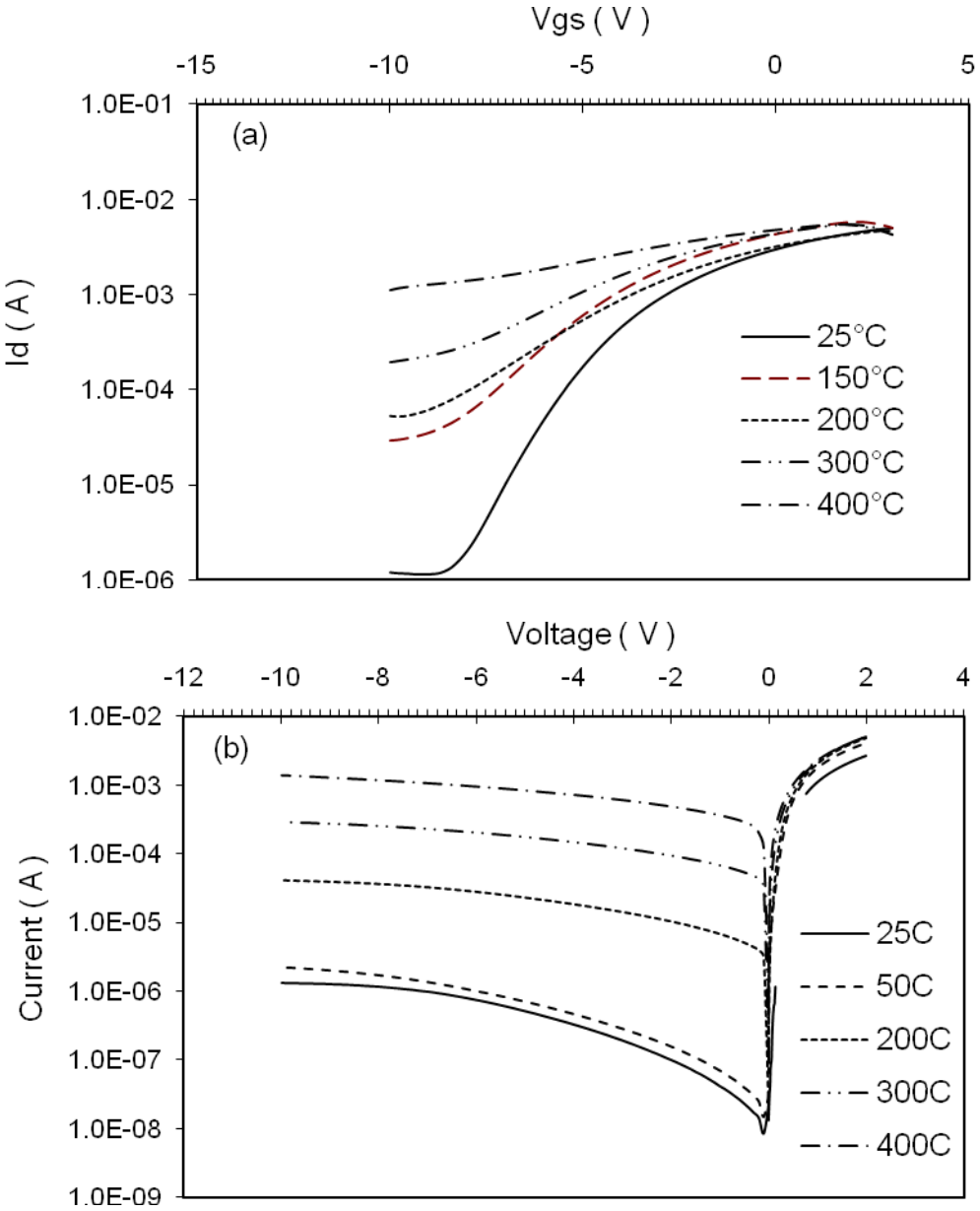



Fig. 106. Current-voltage characteristics for a representative GaN-MESFET of at temperatures from 25°C to 400°C demonstrated by (a) Drain currents as a function of gate voltage and (b) Current-voltage of the Pt/n-GaN Schottky diode.

It is worth pointing out that the GaN structure analyzed in this part of the dissertation was grown a number of years ago and the material properties for GaN-based semiconductors were not as good compared to those of currently grown GaN-based semiconductors and that these older GaN-based structures have considerably more defects.

Fig. 107(a) shows the $I_d$-$V_{ds}$ characteristics as a function of $V_{gs}$ at 300°C for GaN-MESFET fabricated with Pt as the gate and TiAl as the ohmic contacts. These devices were operational, but the pinch-off was not complete with a total drain leakage current of ~500 μA at $V_{gs}$= -7 V. Fig. 107(b) shows the $I_d$ vs $V_{ds}$ characteristics at $V_{gs}$= -7 V. At $V_{ds}$ = 10 V, the total drain leakage was 550 μA, while the gate leakage current was 335 μA.

The gate leakage currents prevented complete channel pinch-off at 400°C as shown in Fig. 108(a). At this temperature, the gate current surpassed the drain leakage current and became the dominant leakage source, as can be seen from Fig. 108 (b).

5.6.3.2 GaN modulated doped field effect transistor (MODFET)

Fig. 109 shows the $I_d$-$V_{ds}$ characteristics at 35°C for a MODFET having dimensions of 2 x 200 $\mu m^2$. The current when the channel was fully open was 33 mA and the breakdown voltage was ~70 V (not shown in the figure). A maximum dc power of 2.8 W/mm was achieved.

Self-heating was observed in this type of device as reflected by the decrease in drain current with respect to increased drain voltage.

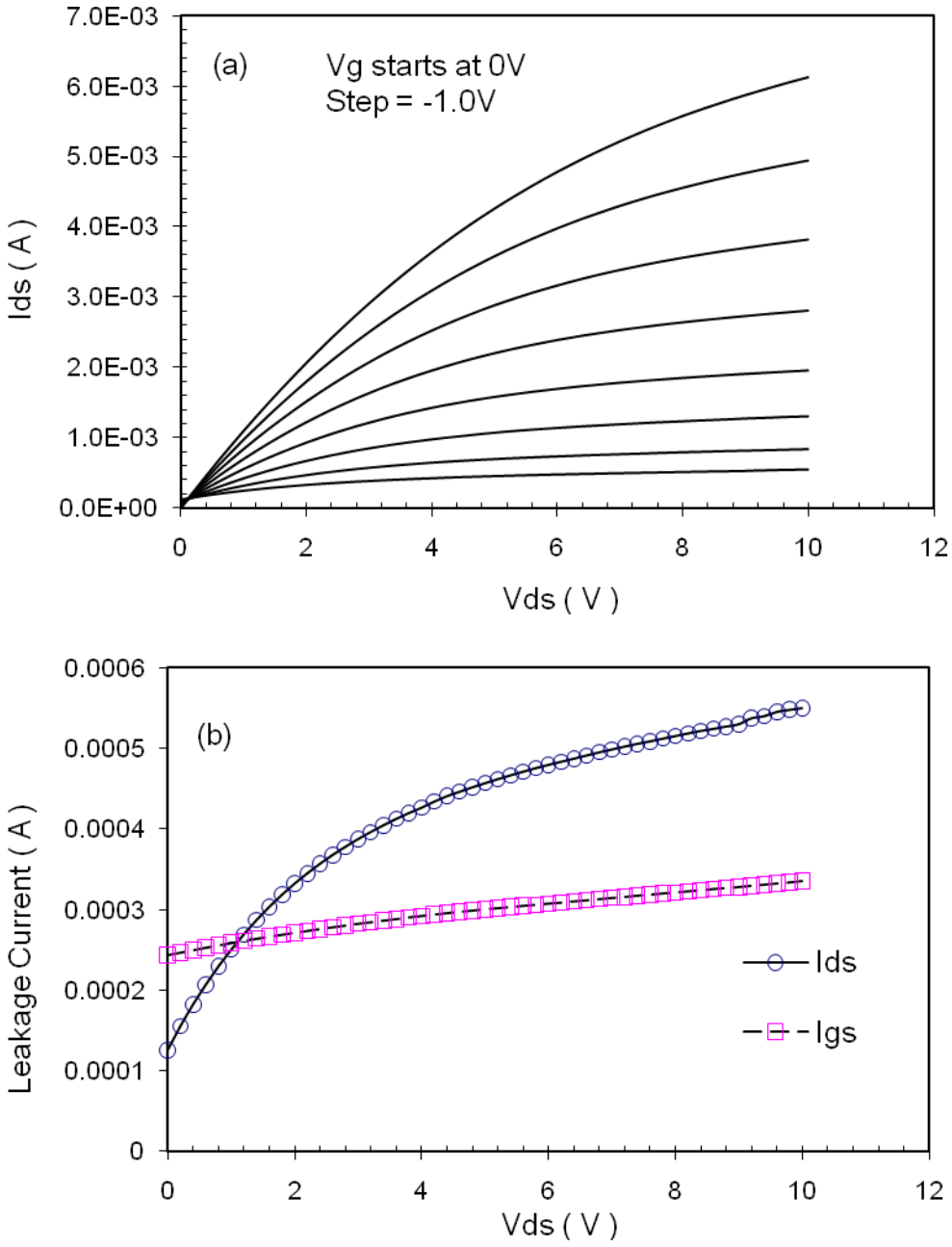



Fig. 107. Current-voltage characteristics at 300°C for a representative GaN-MESFET fabricated with Pt as the gate and TiAl as the ohmic contacts:

(a) $I_d$-$V_{ds}$ characteristics; (b) Drain and gate leakage currents at pinch-off, which occurred at a gate voltage of -7.0 V.

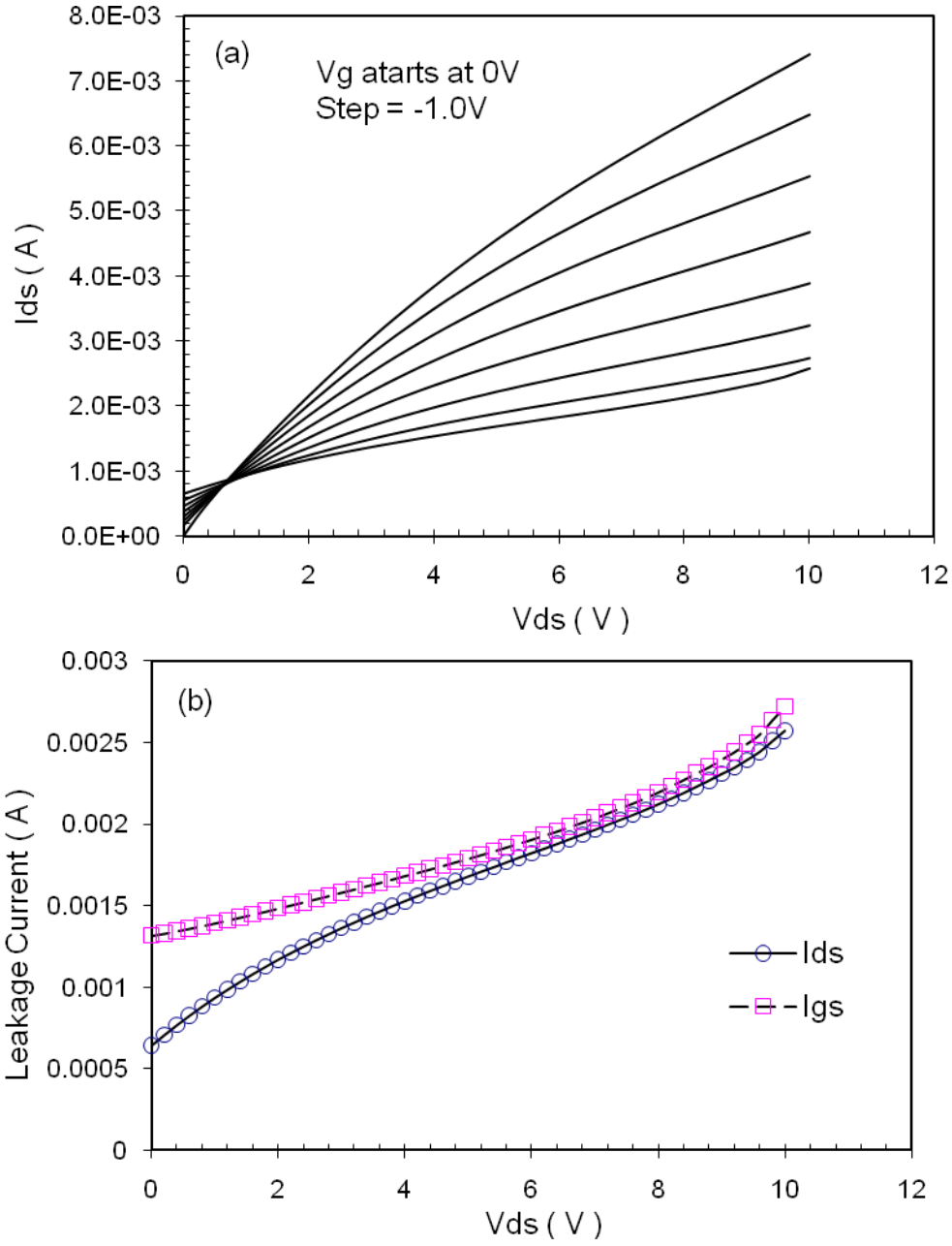



Fig. 108. Current-voltage characteristics at 400°C for a representative GaN-MESFET fabricated with Pt as the gate and TiAl as the ohmic contacts:

(a) $I_d$-$V_{ds}$ characteristics; (b) Drain and gate leakage currents at pinch-off, which occurred at a gate voltage of -7.0 V. Note that at $V_{ds}$ voltages at or above 6 V, $I_{ds}$ and $I_{gs}$ are almost equal to each other.

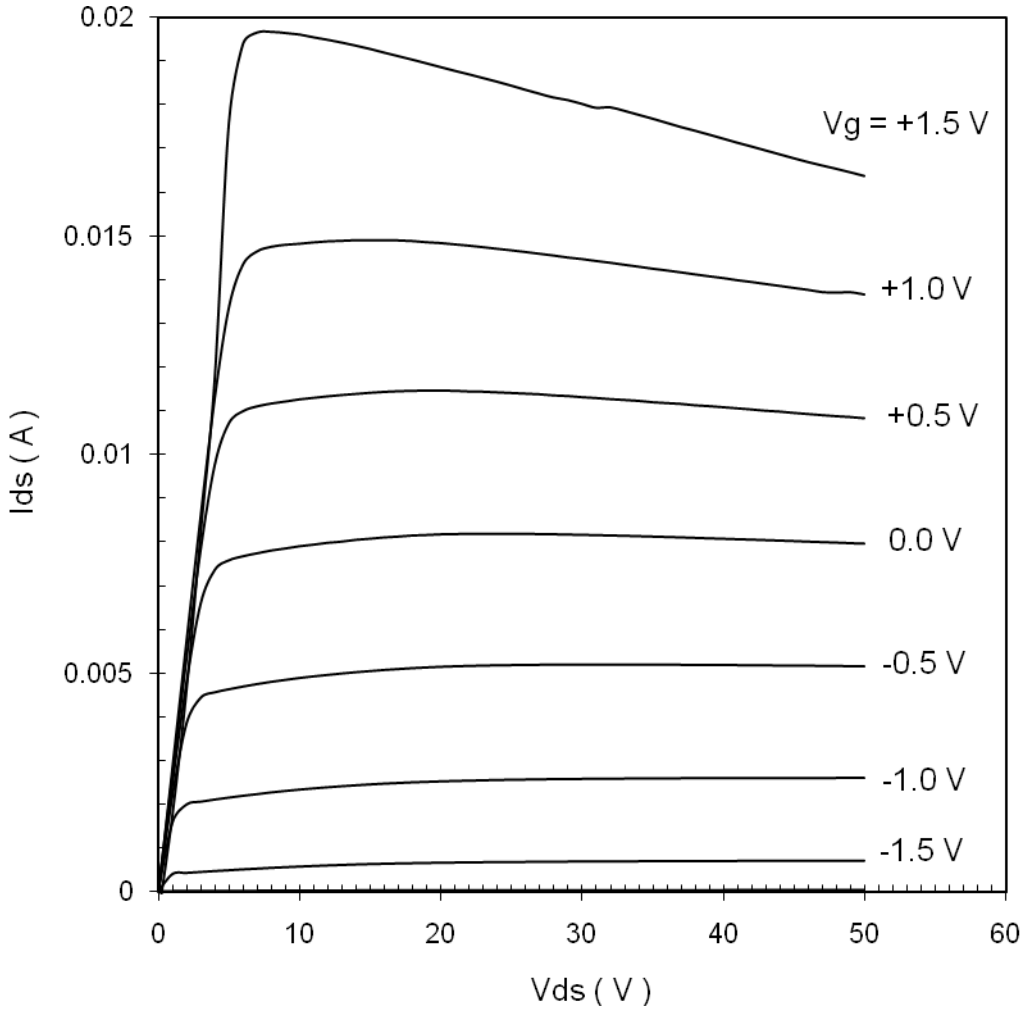



Fig. 109. $I_d$-$V_{ds}$ characteristics at 35°C for a representative AlGaN/GaN MODFET with dimensions of 2 μm x 200 μm. Note that self-heating is evident for positive $V_{gs}$ values.

Another reason for such behavior is, at higher fields, the electron mobility of the 2DEG is reduced, due to the scattering of electrons into lower-mobility subbands [32,33].

Fig. 110 shows the $I_d$ versus $V_{gs}$ characteristics for a 2 μm x 100 μm of a represenative AlGaN/GaN MODFET device at temperatures between 35°C and 400°C. Despite the low on/off current ratio at 35°C of ~1150 for these devices, a relatively superior on/off current ratio of ~70 at 400°C was obtained for these devices while still having good pinch-off characteristics at 400°C.

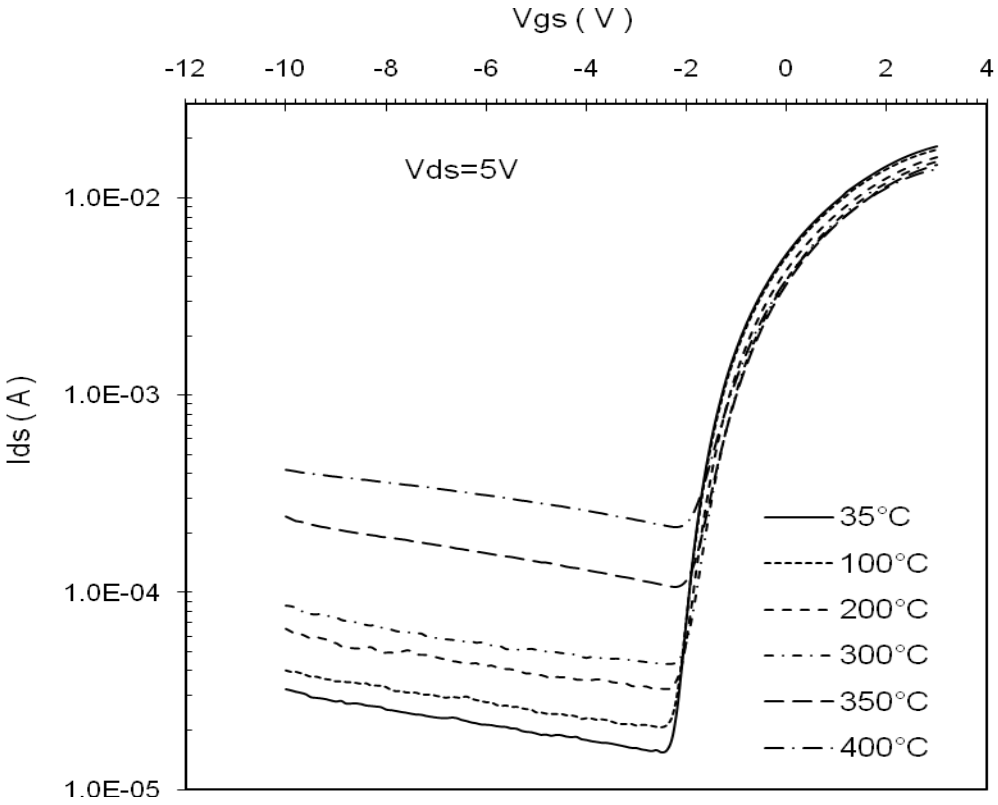



Fig. 110. Drain currents as a function of gate voltage for a representative AlGaN/GaN MODFET at temperatures from 35°C to 400°C. The drain to source voltage was set at 5.0 V.

The total drain leakage currents at pinch-off (i.e., $V_{gs}$ = -2 V, $V_{ds}$ = 5V) were 48 μA, 110 μA, and 225 μA, at temperatures of 300°C, 350°C, and 400°C, respectively. Using GaN as a buffer layer for AlGaN/GaN-based devices, the total drain leakage at 400°C was reduced by a factor of 2 compared with using AlAs as a buffer for AlGaAs/GaAs-based devices due to the higher band-gap of GaN in GaN-based devices over AlAs in GaAs-based devices.

For these AlGaN/GaN MODFET devices, the transconductance gradually decreased with temperature up to 350°C, followed by a steeper drop between 350°C and 400°C, as can be seen in Fig. 111. The peak transconductance was 47 mS/mm near room temperature, and dropped by 12% of its initial value to 41.4 mS/mm at 350°C. The decrease in transconductance with temperature can be explained by the temperature dependence of electron mobility. However, instead of 1/T dependence as in GaAs [11,39], it was found that the electron mobility in GaN was relatively insensitive to temperatures above 300 K.

The large conduction band discontinuity [32, 33, 37, 43 ] in this material system plays an important role in terms of better electron confinement and, thus, potentially less degradation in transconductance. The band-gap energy of $Al_{0.3}Ga_{0.7}N$ at 300 K is 4.03 eV [11], while the corresponding band-gap energy is 3.348 eV for Wurtzite GaN [11]. Therefore, the conduction band offset of $Al_{0.3}Ga_{0.7}N$/GaN is expected to be higher than that of the $Al_{0.3}Ga_{0.7}As$/GaAs system [11]. Another apparently unique property of this structure is the fixed pinch-off voltage in the temperature range from 35°C to 400°C.

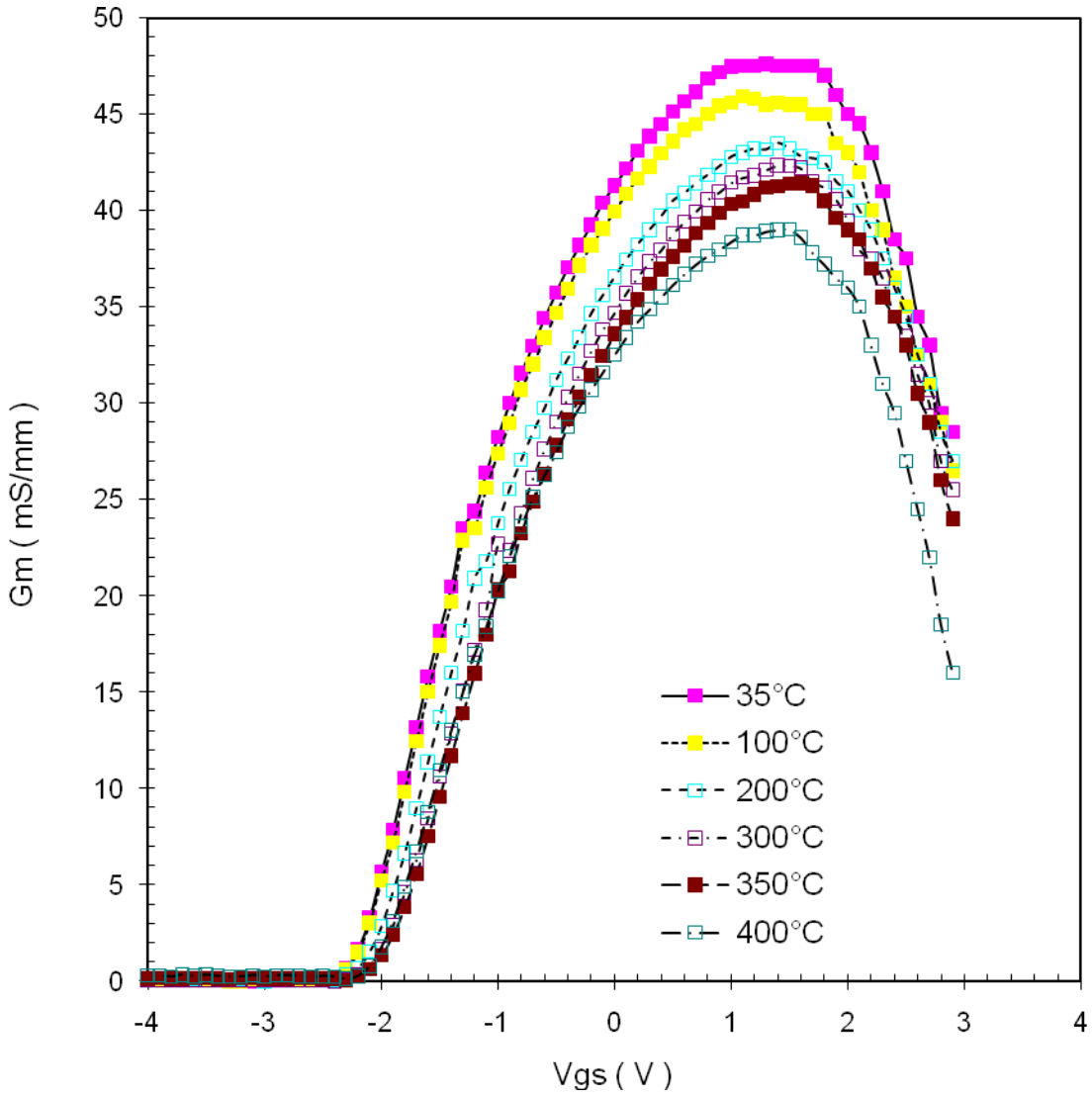



Fig. 111. Transconductance as a function of gate voltage for a representative AlGaN/GaN MODFET at temperatures from 35°C to 400°C.

This fixed pinch-off voltage is attributed in this dissertation to a lower value of the thermally generated substrate leakage currents at high temperatures, and, hence, there is stronger gate bias modulation of the channel carriers when there are fewer thermally generated carriers and the channel is not dominated by thermally generated carriers.

The elevated temperature characteristics of representative MODFETs are shown in Figs. 112, 113, and 114 for temperatures of 300°C, 350°C, and 400°C, respectively. The current ratios of gate leakage to total drain leakage for $V_{ds}$ = 5V and $V_{gs}$= -2V at 300°C, 350°C, and 400°C are 22.4 μA/48 μA, 133 μA/110 μA, and 271 μA/225 μA, respectively. The fact that the gate current became the dominant leakage source is not surprising because the barrier height characterized from forward I-V curves for the gate diode at 35°C was ~1.0 eV. A 1 eV SBH is not sufficient to eliminate gate leakage at temperatures higher than 350°C as has been shown for all of the GaAs-based devices studied in this dissertation.

Comparing these elevated temperature characteristics with that of GaAs-based high temperature devices, it can be concluded that a larger conduction band discontinuity and a higher band-gap in the buffer layer can improve the high temperature performance in a HEMT or MODFET structure. The barrier height is the key point for achieving high power, high temperature applications for HEMT and MODFET structures. For GaN-based HEMT and MODFET structures, the barrier height may be improved by choosing metals having a large work function.

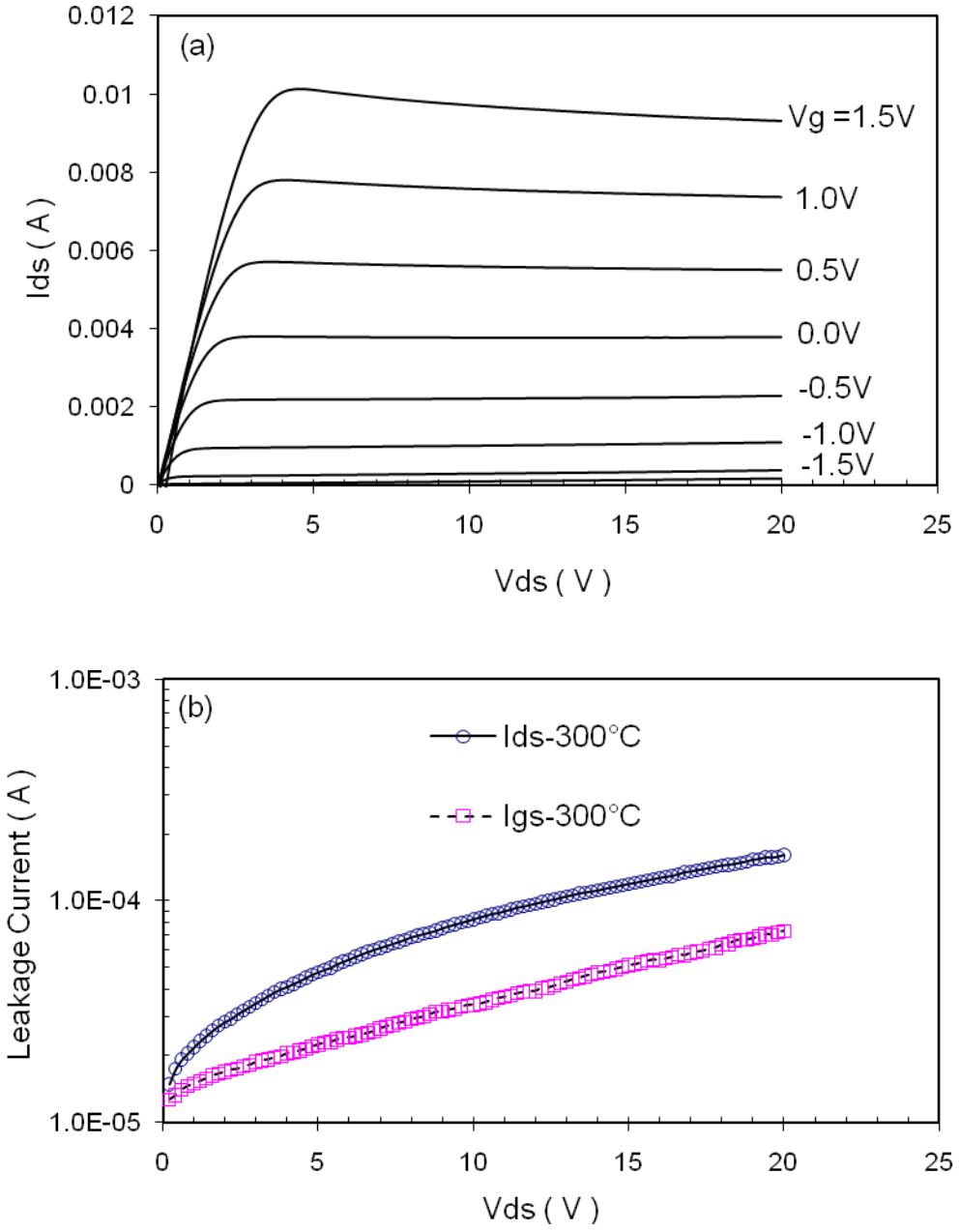



Fig. 112. Current-voltage characteristics at 300°C for a representative AlGaN/ GaN MODFET fabricated with Pt as the gate and TiAl as the ohmic contacts: (a) $I_d$-$V_{ds}$ characteristics; (b) Drain and gate leakage currents at pinch-off, which corresponds to a gate voltage of -2.0 V.

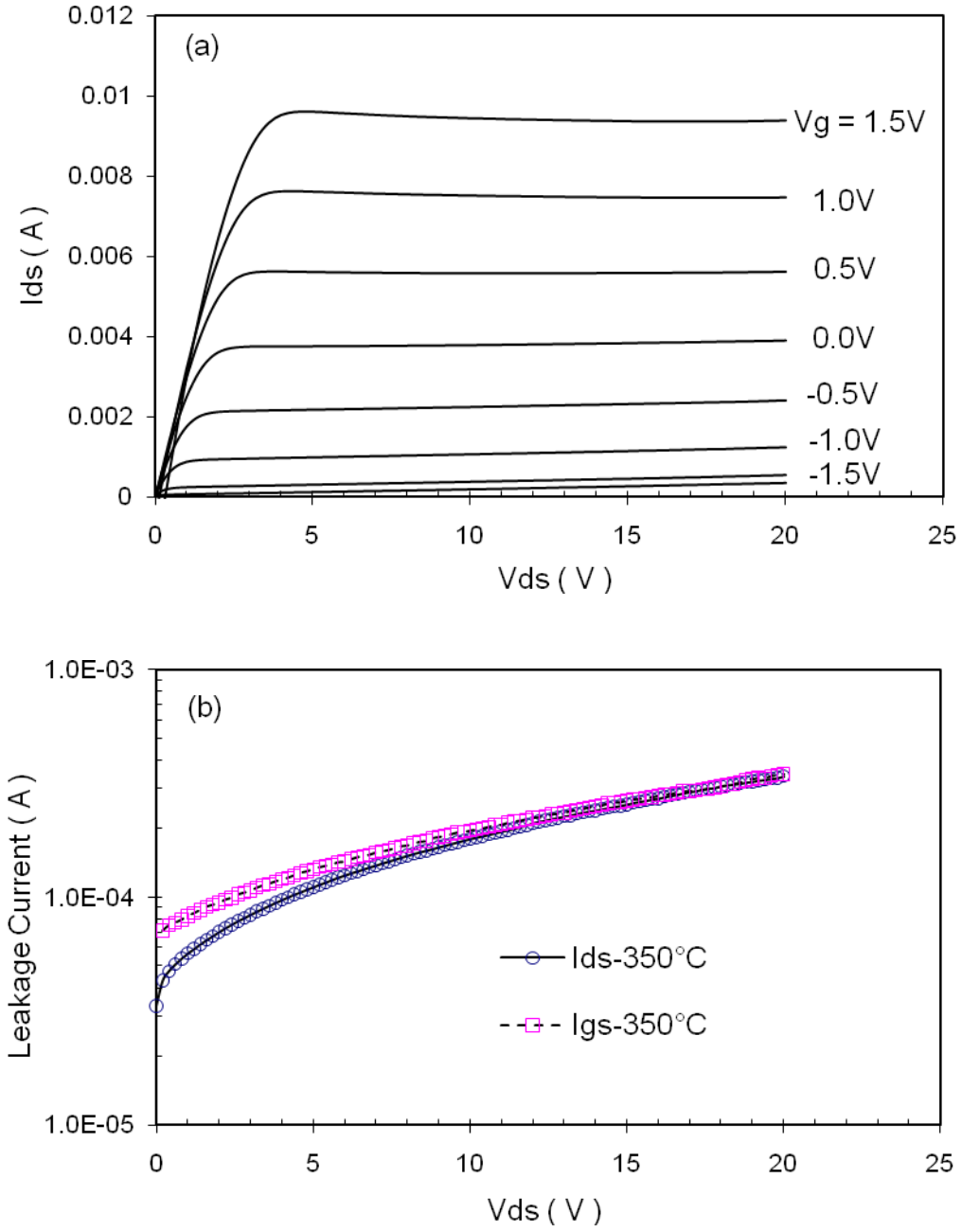



Fig. 113. Current-voltage characteristics at 350°C for a representative AlGaN/ GaN MODFET fabricated with Pt as the gate and TiAl as the ohmic contacts: (a) $I_d$-$V_{ds}$ characteristics; (b) Drain and gate leakage currents at pinch-off, which corresponds to a gate voltage of -2.0 V.

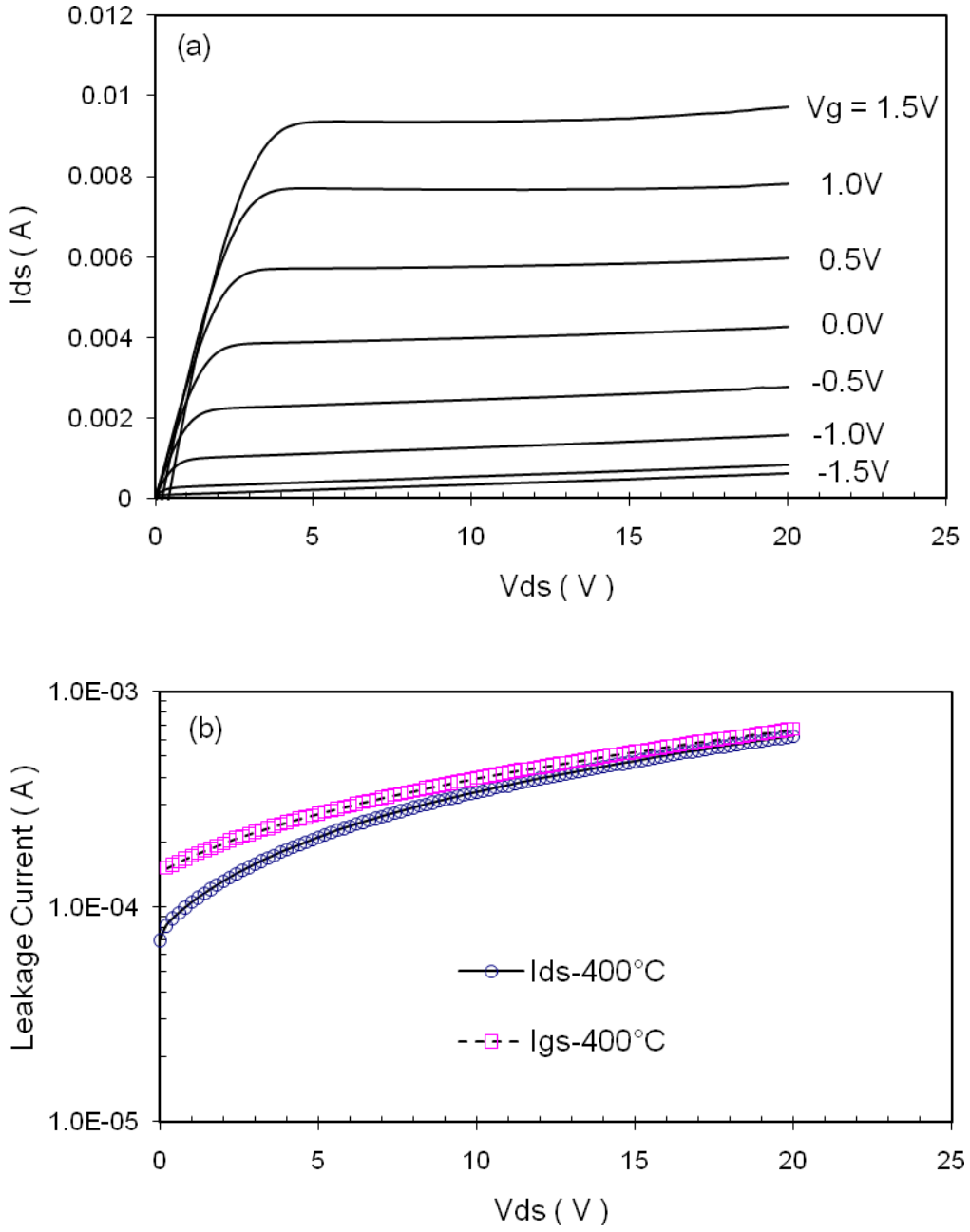



Fig. 114. Current-voltage characteristics at 400°C for a representative AlGaN/ GaN MODFET fabricated with Pt as the gate and TiAl as the ohmic contacts: (a) $I_d$-$V_{ds}$ characteristics; (b) Drain and gate leakage currents at pinch-off, which corresponds to a gate voltage of -2.0 V.

Note, that at high Vds voltages, the drain and gate currents are essentially identical for these AlGaN/GaN MODFETs at 350°C indicating substantial leakage currents are present especially gate leakage currents which contribute to the drain leakage as well. However, as mentioned before in this dissertation, a more accurate picture of the Schottky barrier height dependence on material band-gap or band-gap discontinuity needs to be explored.

## 5.7 Conclusion

The performance of GaAs-based high temperature electronic devices is presumably determined by the structure design. Through appropriate structure design, one can manipulate the leakage currents from the substrate, gate, and reverse-biased junctions to achieve low-power, low leakage operation at elevated temperatures. For example, the gate leakage currents at 400°C in a heterojunction MESFET is equivalent to that of a GaAs MESFET device without an AlGaAs epilayer at 300°C if a thin layer of AlGaAs is placed on top of n-GaAs to be contacted to the gate. The performance of the heterojunction JFET structure (i.e., inserting a p-AlGaAs layer on top of the n-AlGaAs layer) is found to be equally impressive in terms of reduced leakage currents and improved device performance. Further reduction in gate thermal leakage current is possible by applying LT-AlGaAs to replace the AlGaAs materials grown at normal temperatures.

A satisfactory low-leakage current device will not be realized without a back-wall barrier in the structure design because the substrate becomes semi-conducting rather than semi-insulating at high temperatures. LT-AlGaAs and high

Al-content AlGaAs are found to be very effective as a back-wall barrier and in reducing substrate leakage currents.

Using wide band-gap semiconductors such as GaN on sapphire, silicon carbide or other wide band-gap materials reduces the substrate leakage current at elevated temperatures. For this potential to be realized, defect levels must be reduced. Improvements in semi-insulating buffers, stable ohmic contacts, and Schottky barrier heights are needed to optimize the high temperature operation.

## References


1. S. J. Pearton, Mater. Sci. Rep. 4 (1990) 313.
2. S. A. Goodman, F. K. Koschnick, Ch. Weber, J.- M. Spaeth, and F. D. Auret, Solid State Commun. (1999) 593.
3. L. P. Sadwick, Appl. Phys. Lett. 64(1) (1994) 79.
4. J.- M. Spaeth, K. Krambrock, Adv. Solid State Phys. 33 (1993) 11.
5. D. Pons, J. Phys., C 18 (1985) 3839.
6. N. Kobayashi, T. Makimoto, and Y. Horikoshi, Appl. Phys. Lett. 50 (1987) 1435.
7. R. Lee, G. Trombley, B. Johnson, R. Reston, C. Havasy, M. Mah, and C. Ito, Proc. 2nd HiTEC, 1994, p. V-3.
8. P. Schmid, K. M. Lipka, J. Ibbetson, N. Nguyen,U. Mishra, L. Pond, C. Weitzel, E. Kohn, IEEE Electron Device Lett. 19 (1998) 225.
9. J. L. B. Walker, High-Power GaAs FET Amplifiers, Artech House, Inc., Norwood, MA, 1993.
10. J. Hill and P. H. Ladbrooke, Electron. Lett. 22 (1986) 218.
11. S. M. Sze, Physics of Semiconductor Devices, 2nd ed., Wiley, New York, 1981.
12. S. Tiwari, IEEE Trans. Electron. Dev. ED-31 (1984) 879.

13. R. L. Ross, S. P. Svensson, and P. Lugli, Pseudomorphic HEMT Technology and Applications, Kluwer Academic Publishers, Norwell, MA, 1996, p. 20.

14. K. L. Tan, R. M. Dia, D. C. Striet, L. K. Shaw, A. C. Han, M. D. Sholley, P. H. Liu, T. Q. Trinh, T. Lin, and H. C. Yen., Electron. Device Lett. EDL-12 (1991) 23.

15. K. L. Tan, R. M. Dia, D. C. Striet, T. Lin, T. Q. Trinh, A. C. Han, P. H. Liu, , P.- M. D. Chow, and H. C. Yen, IEEE Electron. Device Lett. 11 (1990) 585.

16. R. L. Ross, S. P. Svensson, and P. Lugli, Pseudomorphic HEMT Technology and Applications, Kluwer Academic Publishers, Norwell, MA, 1996, p. 157.

17. F. W. Smith, A. R. Calawa, L.- L. Chen, M. J. Manfra, and L. J. Mahoney, IEEE Electron. Device Lett. 9 (1988) 77.

18. F. W. Smith, Ph.D Thesis, MIT, 1990.

19. R. A. Kiehl, M. Yamakuchi, T. Ohshima, M. Saito, and N. Yokoyama, Appl. Phys. Lett. 69 (10) (1996) 1441.

20. K. Verma, J. Tu, and J. S. Smith, Appl. Phys. Lett. 68 (5) (1996) 699.

21. P. Kordos, M. Marso, A. Forster, J. Darma, J. Betko, and G. Nimtz, Appl. Phys. Lett. 71 (8) (1997) 1118.

22. J. A. Carlin, S. A. Ringel, R. N. Sacks, and K. S. Yap, J. Vac.Sci. Technol. B 16(3) (1998) 1372.

23. H. Reese, Y. J. Chiu, and E. Hu, Appl. Phys.Lett. 73 (1998) 2624.

24. L. He, Solid-State Electronics 41(12) (1997) 1881.

25. R. Zhao, W. S. Lau, T. C. Chong and M. F. Li, Japan. J. Appl. Phys. 35 (1996) 22.

26. R. H. Blick, M. L. Roukes, W. Wegscheider, and M. Bichler, Physica B 249-251 (1998) 784.

27. J. Novak, M. Morvic, J. Betko, A. Forster, and P. Kordos, Mater. Sci. and Eng. B40 (1996) 58.

28. J. Frenkel, Phys. Rev. 54 (1938) 647.

29. R. H. Fowler and L. W. Nordheim, Proc. Roy. Soc. A119 (1928) 173.

30. M. N. Chang, K. C. Hsieh, T. E. Nee, and J. I. Chyi, J. Appl. Phys. 86(5) (1999) 2442.

31. U. V. Bhapkar and M. S. Shur, J. Appl. Phys. 82 (1997) 1649.

32. D. Bykhovski, B. L. Gelmont, and M. S. Shur, J. Appl. Phys. 81 (1997) 6332.

33. P. M. Asbeck, E. T. Yu, S. S. Lau, G. J. Sullivan, J. Van Hove, and J. Redwing, Electron. Lett. 33 (1997) 1230.

34. S. E. Mohney and S. S .Lau, GaN and Related Materials II, Edited by S. J. Pearton, Gordon and Breach, New York, 1998.

35. Q. Z. Liu, L. S. Yu, K. V. Smith, F. Deng, C. W. Tu, P. M. Asbeck, E. T. Yu, and S. S Lau, Proc. of the ECS Symp. On GaN and Related Materials, Paris 97 (1998) 34.

36. T. Ping, Q. Chang, J. W. Yang, M. A. Khan, and I. Adesida, J. Electron. Mater. 27 (1998) 261.

37. S. N. Mohammad, Z. F. Fan, W. Kim, O. Aktas, A. E. Botchkarev, A. Salvadar, and H. Morkoc, Electron. Lett. 32 (1996) 598.

38. S. C. Binari, K. Doverspike, G. Kelner, H. B. Dietrich, and A. E. Wickenden, Solid State Electron. 41(2) (1997) 177.

39. F. S. Shoucair, P. K. Ojala, IEEE Trans. Electron. Devices 39(7) (1992) 1551.

40. Y. Koide, H. Itoh, M. R. H. Khan, K. Hiramatu, N. Sawaki, I. Akasaki , J. Appl. Phys. 61 (1987) 4540.

41. B. Chen and A. Sher, Semiconductor Alloys, Plenum Press, New York, 1995, p. 260.

42. R. Narasimhan, L. P.Sadwick, and R. J.Hwu, IEEE Trans. Electron. Devices 46 (1999) 24.

43. W. Yao, J. Cao, and X. Lei, J. Funct. Mater. and Devices 5 (1999) 213.

44. E.F. Schubert, A. Fischer, and K. Ploog, IEEE Trans. Electron. Devices ED-33 (1986) 625.

45. M. Hueshen, N. Moll, E. Gowen, and J. Miller, IEDM Tech. Dig. (1984) 348.

46. E. M. Conwell. Properties of Silicon and Germanium, Part II, Proc. IRE, 46 (1958) 1281.

47. F.H. Pollak and H. Shen, Mater. Sci. and Eng. R10 (1993) 275.

48. T.J. Drummond, R. Fischer, S. L. Su, W. G. Lyons, H. Morkoc, K. Lee. And M. S. Shur, Appl. Phys. Lett. 62 (1983) 262.

49. K. Verma, J. Tu, and J. S. Smith, Appl. Phys. Lett. 68 (5) (1996) 699.

50. D. Wilson and A. G. O'Neill, First European Conference Proc. HiTEC, Paper 1993, III.4.

51. Ghezzi, E. Gombia, and R. Mosca, J. Appl. Phys. 70(1) (1991) 215.

52. J. V. Dilorenzo, R. Dingle, M. D. Feuer, A. C. Gossard, R. H. Hendel, J. C. M. Wang, A. Kastalsky, R. A. Kiehl, and P. O'Connor, IEDM Tech. Dig. (1982) 578.

53. S. M. Sze, High – Speed Semiconductor Devices, Wiley, New York, 1990.

54. J. L. Lee, J. K. Mun, and B. T. Lee, J. Appl. Phys. 82(10) (1997) 5011–5016.

55. K. Sehgal, R. Gulati, A. A. Naik, Seema Vinayak, D. S. Rawal, and H. S. Sharma, Mater. Sci. and Eng., B 48(3) (1997) 229–233.

56. S. K. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, Wiley, New York, 1994.

# CHAPTER 6

# CONCLUSIONS AND FUTURE WORK

## 6.1 Conclusions

In conclusion, CuGe-based ohmic contacts deposited under appropriate deposition procedures and precise composition control have low resistivity competitive to that of AuGeNi contacts to n-type GaAs. RF-sputtered TiWN, with certain levels of nitrogen incorporation, are effective diffusion barriers preventing intermixing between Au and $Cu_3Ge$. The degradation rate of the specific contact resistance of $Cu_3Ge$ to n-type GaAs with a TiWN barrier and Au overlayer is close to $t^{1/2}$ at 400°C and negligible at temperatures lower than 350°C.

The properties of $Cu_3Ge$ ohmic contacts to n-type GaAs have demonstrated that they will be suitable candidates as ohmic contacts in GaAs-based electronic devices for high frequency, high power, and high temperature applications.

In MESFET devices, reverse leakage currents of the gate Schottky diode are dominated by the tunneling through the lowered energy barrier between the metal/semiconductor interfaces due to image forces and the effects of elevated temperatures including the exponential dependence of the thermally generated carriers on temperature and the reduction in SBH with increased temperature. The Schottky barrier heights for GaAs-based devices can be enhanced by increasing the Al composition of the AlGaAs layer in the gate contact layers due

to the larger bandgap of AlGaAs compared to GaAs and the large conduction band discontinuity. For deposited contacts, the MIGS model appears to be suitable for the work performed in this dissertation and can be used to predict the barrier height of metal/$Al_xGa_{1-x}As$ interfaces.

The low-power consumption operations at elevated temperatures cannot be achieved without the careful engineering of the buffer layers in GaAs-technology – the so-called “back-wall barrier.” Together with “gate barrier engineering,” reliable operations at 400°C for GaAs-based electronics are feasible.

Grain boundaries serve as the sink of atoms and fast diffusion paths allowing reactions, contamination and electromigration to take place. There is no doubt that current transport through these defects will be much easier than that in the monocrystalline materials. Thus, the contacts should be ultimately monocrystalline and epitaxial. Thulium phosphide (TmP) has demonstrated excellent performance as a promising Schottky contact for high-temperature operations. Other rare-earth compounds, i.e., the rare earth arsenides and phosphides, having material properties similar to that of TmP, are potential candidates for high temperature applications

The performance of GaAs-based high temperature electronic devices is presumably determined by the structure design. Through appropriate structure design, one can manipulate the leakage currents from the gate, reverse-biased junctions, and substrate to achieve low power, low leakage operation at elevated temperatures. There are two effective approaches for reducing the gate leakage currents for GaAs FETs, heterojunction MESFETs and JFETs, namely increased

Schottky barrier heights and built-in potentials, respectively. Further reduction in gate current is achieved by applying LT-AlGaAs to replace the AlGaAs materials for GaAs-based devices grown at normal temperatures.

The generation-recombination current dominates the diffusion current as the major component of substrate leakage for GaAs FETs grown on GaAs substrates at temperatures around or lower than ~ 350°C. LT-AlGaAs and high Al-content AlGaAs such as AlAs are found to be very effective in reducing substrate leakage current at all temperatures investigated in this dissertation.

Using wide band-gap semiconductors such as GaN grown on wide band-gap substrates reduces the substrate leakage current at elevated temperatures. Devices that take advantage of and exploit the higher conduction band discontinuity between GaN and AlGaN and, thus, the higher electron-confinement, show high stability in transconductance in the temperature range from or below room temperature up to ~ 400°C. Ti-Al ohmic contacts protected by Cr and Au overlayers can be used for high temperature applications. However, improvements in semi-insulating buffers, stable ohmic contacts, and Schottky barrier heights are needed to optimize the high temperature operation.

## 6.2 Future work

Thermally stable ohmic contacts to n-type GaAs with no degradation at temperatures higher than 400°C, for example, NiIn(Ge)W/$WN_x$/Au ohmic contacts to n-type GaAs have shown impressive performance and can be promising candidates in terms of low specific contact resistance and excellent thermal stability.

Future research efforts should pursue Schottky contact materials with barrier heights higher than 1.3 eV to both GaN- and GaAs-based semiconductors. This research should also include investigations of single crystalline Schottky contacts to reduce leakage current at high temperatures. Rare earth compounds are promising candidates and have shown an ability to satisfy both requirements and need to be explored further in the future.

The simulation of device performance using commercial software packages can greatly aid and expand upon the preliminary success that was realized in this dissertation study and will help the optimization on device structure design. The high temperature performance can be dramatically improved as many mistakes, both in design or processing, can be detected, understood, further simulated and corrected.

The design of the buffer and gate contacting layers in GaN-based electronic devices, especially the characterization on the Schottky behavior of metal/$Al_xGa_{1-x}N$ interfaces at elevated temperatures, needs to be systematically performed. While a strong dependence of SBH on metal work function is noted, the measured barrier heights show a large amount of variation for metals with similar work functions. This suggests that sample preparation and material quality need to be improved. It is important to match the coefficient of thermal expansion and the lattice constant between Schottky metals and $Al_xGa_{1-x}N$ in order to obtain stress-free or nearly stress-free interfaces and, thus, more stable Schottky contacts. It is also worth noting that Schottky contacts should ultimately be single crystalline. Pd, Ni, Rh, Re, and Te are potential candidates due to their high work function. The lattice mismatch between Ti ( or Zr ) diboride and AlGaN

is less than 0.6% which makes these diborides potential candidate single crystalline Schottky contacts to AlGaN.