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# QUANTIFYING COMPONENT DEGRADATION AND LEVEL OF AGING IN POWER CONVERTERS USING SPREAD SPECTRUM TIME DOMAIN REFLECTOMETRY

by

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A dissertation submitted to the faculty of
The University of Utah
in partial fulfillment of the requirements for the degree of

Master of Science

Department of Electrical and Computing Engineering

The University of Utah

August 2013

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The University of Utah Graduate School

# STATEMENT OF THESIS APPROVAL

The following faculty members served as the supervisory committee chair and members for the thesis of Most Sultana Nasrin.

Dates at right indicate the members' approval of the thesis.

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# ABSTRACT

Power converters are frequently exposed to electrical stresses such as over voltage, over current and switching impulses during their regular operations. These stresses may not result in immediate failure of a power converter. However, over longer periods they cause gradual degradation of critical components inside the converter, which ultimately leads to a complete failure of the converter. Failure of a power converter might disrupt the operation of the entire system, occasionally causing catastrophic outcomes. Estimating a converter's state of health and predicting the remaining life involves extensive research in semiconductor device physics and circuit theory, and is both important and challenging.

There is always a dire need to determine the level of aging in power converters so that an approximate time to failure could be predicted. A reflectometry technique was applied to power converters to identify failure and aging associated to critical components inside a power converter. In addition, mechanisms for gradual shift in measurable electrical parameters of power converter components over long durations have been studied under the scope of the project. While there exist several other techniques for predicting reliability and aging of power converters, they are limited to characterizing isolated components only. Whereas using the proposed technique, estimating the component degradation in energized circuits is possible. Spread spectrum time domain reflectometry (SSTDR) has been commercially used for detecting aircraft wiring faults during the last decade, however, it

was never applied to components in a power converter. During the preliminary stage of this project SSTDR was applied to a DC-DC converter circuit, and several key parameters such as MOSFETs ON resistance was extracted to characterize MOSFET aging. Later on, this technique was applied to different other components in an H-bridge AC-AC converter for failure rate estimation and reliability analysis. The MTTF (mean time to failure) was calculated based on the SSTDR generated data.

The conducted research has initiated other SSTDR based prognostics and state of health measurement methods applicable to PV panels, electric machines and batteries.

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# ACKNOWLEDGEMENTS

It would never be possible to finish my dissertation without the guidance of my committee members, help from group members, and support from my family and husband.

I would like to express my deepest gratitude to my advisor, Dr. Faisal Khan, for his excellent guidance, caring, patience, and providing me with an excellent research environment. I would like to thank Dr. Cynthia Furse, who provided me continuous support to carry on my research on SSTDR application in power electronic circuits. I would also like to thank Dr. Marc Bodson for guiding my research for the past two years.

Special thanks goes to my group mates, Mohammed Khorshed Alam and Abusaleh Imtiaz who were always willing to help and give their best suggestions.

I would also like to thank my parents, sister, and brother. They were always encouraging me with their best wishes. Last, but most importantly, I would like to especially thank to my husband, Mahatasin Azad, for his love and support during my M.S. He was always cheering me up and made it possible to finish my research.

# CHAPTER 1

# INTRODUCTION

Power converter circuits have a wide range of applications, and ceaseless operation of these converters is imperative in most cases. These converters are frequently exposed to electrical stresses, such as over voltage, over current and switching impulses during their regular operations. These stresses may not result in immediate failure of the converter, however, over longer periods they cause gradual degradation of critical components inside the converter, which ultimately leads to failure of the converter. Failure of a power converter might disrupt the operation of the whole system, occasionally causing catastrophic outcomes. Therefore, reliability prediction of the converters is vital. Estimating a converter's state of health and predicting the remaining life involves extensive research in semiconductor device physics and circuit theory, and is both important and challenging. A failure survey of various components in a power converter is shown in Figure 1.1[1], and it distinctly shows that electrolytic capacitors and semiconductor switches are two critical aging-affected components in power converter circuits. Photographs of damaged metal oxide semiconductor field effect transistors (MOSFETs) and electrolytic capacitor are given in Figure 1.2. Component parameters, such as, ON-resistance and switching characteristics of MOSFETs/insulated gate bipolar transistors (IGBTs), and equivalent series resistance (ESR) of capacitors, degrade over time, and the

accumulated aging eventually affects several operating characteristics of the component such as output voltage ripple, switching loss, conduction loss [2], [3], [4]. Therefore, the state of health of the entire power converter could be obtained by studying the component level aging. However, the aggregated effect of aging associated to any component is difficult to calculate because of complex interconnections between multiple components in a converter circuit.

Several existing online methods are based on identification of individual component degradation and some real time techniques are based on identification of the overall system's performance. The techniques based on individual device degradation are particularly suitable to locate degradation in any specific type of component i.e., electrolytic capacitors or MOSFETs or IGBTs, and at least two measurements are required to collect – voltage and current. On the other hand, the methods intended to predict the overall circuit's degradation are unable to locate the aged components. Therefore, there is a categorical need to develop a real time method that can identify the aged components as well as predict the overall system performance based on the aged devices. The aim of this project is to identify the origin of component-level degradation, level of aging, and thus predict the overall system's reliability using mathematical analysis based on obtained experimental data.

## 1.1 Origin of component degradation

Predicting the converter's state of health and the remaining life are extremely challenging tasks and involve extensive research both in semiconductor device physics and circuit theory. Two of the most failure prone components in a power converter are

semiconductor switches and electrolytic capacitors. In order to conduct a failure study and predict the remaining life of the component and hence the power converter, the origin of component failure needed to be studied first. Therefore, the origin of these failures and previous work on identification of the measurable quantities induced by degradation of these components are described in the following sections.

### 1.1.1 Origin of degradation in electrolytic capacitors

The performance of the electrolytic capacitor is affected by nonrated values of operating parameters such as voltage, current, frequency, and temperature. The primary failure mechanism of the electrolytic capacitor is the evaporation of the electrolyte solution. During operation, the evaporation of the solution is accelerated by one or multiple of these phenomena, the ripple current, over voltage, and temperature elevation [5]. As the electrolyte solution dries up, the effective contact area between the electrodes decreases. This results in a decrease in capacitance and increase in equivalent series resistance (ESR) [6]; which further increases the temperature losses. This temperature losses again contribute to accelerating degradation of ESR and eventually leads to complete failure of the capacitor.

Mathematical relationship between volumetric loss of electrolyte solution and rise of ESR is given by, $ESR = ESR_0/v^2$ [6], where $v$ ($= V/V_0$) denotes the normalized volume of electrolyte solution. According to [7], a capacitance is considered to reach its end of life if the value of capacitance is decreased by 10% or more from its initial value. This happens when a capacitor loses 30% to 40% of its electrolyte, i.e., when ESR increases by a factor of 2 to 3 [8]. Reference [9] presented the degradation of capacitance due to thermal and

electrical overstresses. According to this analysis, capacitance decreases due to thermal overstress and ESR increases due to electrical overstress. Reference [5], [8] - [11] presented several methods of health monitoring of electrolytic capacitors depending on the value of ESR. Therefore, it is evident that by measuring capacitive impedance change we can measure the aging level of electrolytic capacitors.

### 1.1.2 Origin of degradation in power semiconductor devices

Failure of semiconductor devices can be categorized into two groups: (a) chip related failure, and (b) packaging related failure [12]. The reasons for chip related failures are electrical overstress, electrostatic discharge, latch up, charge effects and radiation effects [12]. The combined effect of high voltage and high current constitutes electrical overstress. Overheating can be crucial under high voltage conditions and may cause secondary breakdowns. Abrupt losses of gate oxide in MOS devices occur due to such breakdowns. In this continuation, drain current decreases and gate leakage current increases after the breakdown [1]. The gate terminal of MOSFETs can also be affected by electrostatic discharge (ESD). The effect of electrical stress at the gate area was studied in [13] [14] by applying a high voltage at the gate terminal. It was also found that threshold voltage increases with aging, and any increment in the threshold voltage directly results in an increment in switching time causing additional switching loss. Usually, threshold voltage deviates from the typical value because of degradation in the gate oxide region and/or degradation at the oxide-channel interface. The rate of this degradation depends on the thickness of the gate oxide. If a very high positive voltage is applied at the gate terminal or a very high negative voltage is applied at the drain terminal of an N-channel MOSFET, hot

carriers are generated in the silicon substrate. Due to the very high kinetic energy of these carriers, they can move around or get trapped in the oxide region or at the oxide-channel interface.

Threshold voltage ($V_{th}$) shifts as a result of the applied stress (positive voltage) at the gate terminal of an N-channel MOSFET. However, the amount of shift in threshold voltage ($\Delta V_{th}$) gradually decreases when over-voltage stress is applied repeatedly [15]. As a result of repetitive application of positive voltage stress, increased numbers of acceptor ions move towards the surface and create a nonlinear energy distribution. This is the reason for nonlinearity in $\Delta V_{th}$. This shift in threshold voltage is negative when a negative stress is applied at the gate terminal. In an N-channel MOSFET, when threshold voltage is increased over cumulative stress, the gate to source capacitance ($C_{gs}$) decreases, and the gate to drain capacitance ($C_{gd}$) increases [15]. Rapid increase in applied drain-source voltage of a MOSFET or the collector-emitter voltage of an IGBT may cause an undesirable triggering of the parasitic elements (the formed BJT in MOSFET structure and the auxiliary thyristor in IGBT). In this regard, reference [2] presented an accelerated aging procedure by applying both high power and constant thermal stress. The drain current was allowed to increase with sufficient thermal stress, and the device failed to turn off at some point in spite of a zero gate voltage. Moreover, a sudden increase in package temperature indicates thermal runway of the device. This phenomenon indicates the loss of gate control, and the ON resistance ($R_{DS\ (ON)}$) exhibits a sudden drop due to elevated drain current. Therefore, higher $R_{DS\ (ON)}$ is consistent with aging and a sudden drop in the value of $R_{DS\ (ON)}$ is an indicator of the loss of gate control.

In power MOSFETs, both carrier injection and ionic contamination induce undesired change in threshold voltage, leakage current and transconductance, which eventually leads to device failure. The power semiconductor switches in space environments suffer from significant charge build up within the oxide and insulators due to the radiation effects, and this induced charge is responsible for any shift in the threshold voltage [16]. Oxide-trapped charge is positive for both P- and N- channel transistors. However, interface-trapped charge is negative for an N-channel transistor, which causes positive shift in $V_{th}$; whereas interface-trapped charge is positive for a P-channel transistor, which causes negative shift in $V_{th}$. Any shift in the $V_{th}$ increases the leakage current, which ultimately leads to device failure.

The packaging related failures arises from the difference in coefficients of thermal expansion (CTE) among various material constituents of the chip and the package. Packaging failures are of mainly two types, bond failures and die-solder layer failure. Bond failure is predominantly caused by any crack growth at the bond wire/chip interface due to the difference of CTEs of Si and Al [17]. Bond wire lift-off can be electrically detected by measuring the collector-emitter saturation voltage ($V_{CE,sat}$) of IGBT [18]-[20], and this failure can be detected from a 5% increment in $V_{CE,sat}$ [21]. For a MOSFET, $R_{DS\ (ON)}$ increases due to the degradation at metallization and at the contact area of bonding wire metallization [22]. Reference [23] also concluded that $R_{DS\ (ON)}$ increases due to thermal aging. Intermetallic growth and Kirkendall voids formation at the bond-pad interface at higher temperature were studied here. Figure 1.3 and Figure 1.4 provide the graphical presentation of crack and void formations and failure in bonding inside a power MOSFET.

According to [24], $R_{DS\ (ON)}$ is found to be the most significant aging factor in power

MOSFETs. Die-solder layer failures are related to the formation of initial solder microstructures, substrate metallization, intermetallic compounds, and cracks. These voids increase the thermal impedance, resulting in higher temperature fluctuations within the semiconductor device. The thermal impedance can be determined from the junction temperature of the device, and reference [25] described a technique that uses $R_{DS\ (ON)}$ of the device to determine the junction temperature. Die solder degradation has been studied in references [26] [27] by applying thermal stress to the device, and $R_{DS\ (ON)}$ increased due to the degradation. Therefore, the variation in $R_{DS\ (ON)}$ is considered a precursor to failure due to its dependence on junction temperature. Variation in $R_{DS\ (ON)}$ is related to the formation of cracks and voids in the source metal layer according to reference [28].

In summary, the aging factors associated with MOSFETs are i) ON-resistance, ii) threshold voltage and iii) various MOSFET capacitances. However, from the existing literature study, it can be concluded that the $R_{DS\ (ON)}$ is the most significant aging factor in MOS devices and the novelty in any measurement technique lies in how accurately and conveniently this $R_{DS\ (ON)}$ can be measured, especially when the device is energized.

Multiple MOSFETs connected in parallel have become a prevalent trend these days. Nonuniform degradation among parallel MOSFETs is found in [29] due to high current stress. Variation in current distribution was observed in parallel MOSFETs as well. This imbalance is further aggravated by (i) increased $R_{DS\ (ON)}$ during thermal stress, (ii) increased effect of conductance path mismatch during current stress and (iii) increased effect of thermal path difference during thermal stress. In addition to power MOSFETs, several studies focused on leading failure parameters for discrete IGBTs under thermal degradation caused by power cycling overstress. Collector-emitter voltage was identified

as a health indicator in [30]. In [31], the maximum peak of the collector-emitter ringing during turn-off transient was identified as the degradation variable. In [32], the switching turn-off time was recognized as a failure precursor; and switching ringing was used in [33] to characterize degradation. Reference [34] explains how threshold voltage, transconductance, and collector-emitter ON voltage ($V_{CE\ (ON)}$) could be used to identify aging. Therefore, the equivalent impedance $R_{CE}$ will be impacted due to the variation in $V_{CE\ (ON)}$ under any specific operating condition.

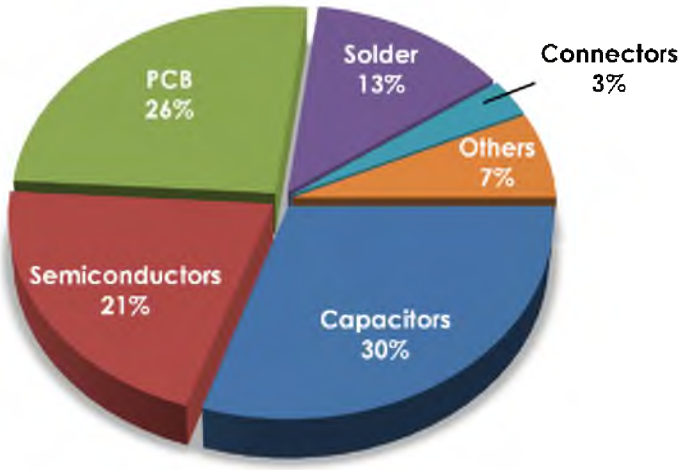
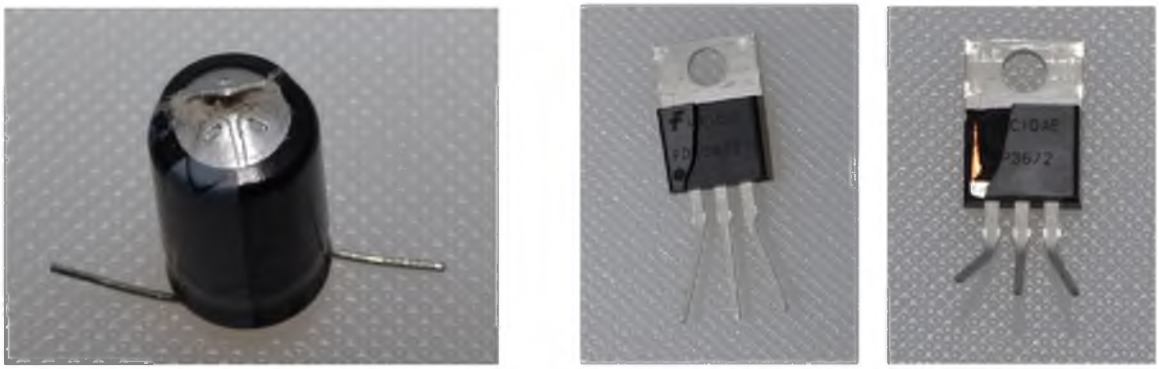



Figure 1.1: A failure survey of different components responsible for converter failure (adapted from [1]).



(a) (b)

Figure 1.2: (a) Damaged electrolytic capacitor (failed at high voltage); (b) damaged MOSFET (failure caused by high voltage applied across drain and source).

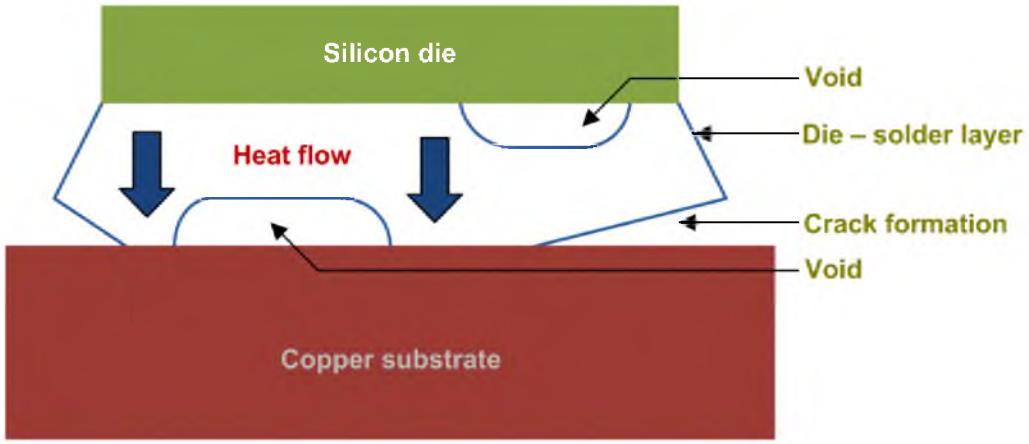



Figure 1.3: The origination of cracks and voids in a power MOSFET due to aging.

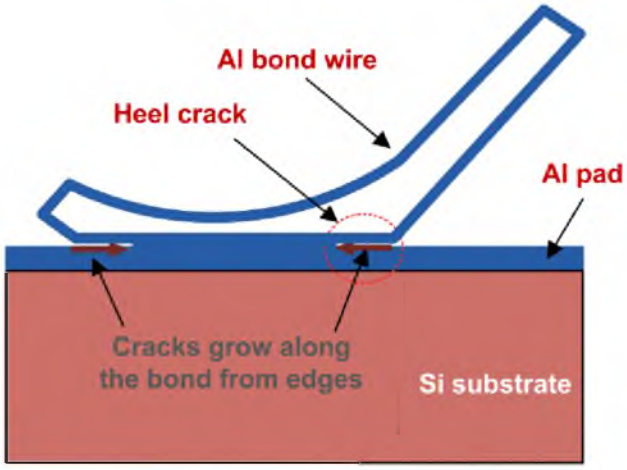



Figure 1.4: Wire bonding failure in semiconductor devices.

# CHAPTER 2

# EFFECT OF AGING ON MEASURABLE PARAMETERS

Device characterization was performed to observe the changes in parameters of electrolytic capacitors, power MOSFETs and IGBTs. Multiple devices were aged in a controlled environment using both temperature stress and power stress. The characterization test details are given in Table 2.1. The detailed aging procedure of capacitors, MOSFETs, IGBTs and shift in their measurable parameters are described in the following sections. The temperature chamber used to apply temperature stress is shown in Figure 2.1.

## 2.1 Characterization of electrolytic capacitors

Three SEK102M010ST aluminum electrolytic capacitors were aged using temperature stress in a simple parallel RC circuit, and the circuit diagram used to take measurements is shown in Figure 2.2. Capacitors C2, C3, and C4 were aged at 150°C, 160°C, and 170°C, respectively, and each of them were stressed for 1 hour. The change in capacitance and ESR were measured using an LCR meter at 60 Hz after they reached room temperature. The variations are given in Table 2.2 and Figure 2.3 and it is apparent that the ESR and the capacitances change due to thermal aging, and that capacitor ripple voltage increased due to the variation in ESR and self-capacitance.

## 2.2 Characterization of power MOSFETs

### 2.2.1 Single MOSFET circuit

Multiple power MOSFETs were aged using power and temperature stress in a controlled environment. 1 V DC voltage ($V_{DS}$) was applied across the drain-source terminals of FDP 3672 N-channel power MOSFET to apply power stress, and the MOSFETs were placed in a controlled temperature chamber at 110°C using a Delta 9059 environment chamber. Experimental setup used for quantifying the accelerated aging of the MOSFETs is shown in Figure 2.4(a). The gate-source voltage was 12 V and $R_{Lim}$ was removed ($R_{Lim}$ = 0) during the accelerated aging procedure. Due to the high power dissipation (~8W) in each MOSFET, the case temperature reached 170°C within 10 minutes which was stabilized between 160°C~170°C during this accelerated aging process. The above procedure was applied to four different MOSFETs M2, M3, M4 and M5, and their initial $R_{DS\,(ON)}$ were approximately equal (33 ~ 34 mΩ). M1 was used as the reference MOSFET as zero stress was applied to it. These stressed MOSFETs were cooled down to room temperature after accelerated aging, and the $R_{DS\,(ON)}$ were measured using the setup shown in Figure 2.4(b). The gate voltage was set to 5 V and the value $R_{Lim}$ was selected as 5 Ω while taking the measurements of $R_{DS\,(ON)}$. A noticeable permanent increment in $R_{DS\,(ON)}$ was obtained after aging, and the change in $R_{DS\,(ON)}$ was in the range of 2 ~ 10 mΩ for these MOSFETs under test. Calculated $R_{DS\,(ON)}$ for M1 ~ M5 are shown in Table 2.3 and the variation in $R_{DS\,(ON)}$ with aging duration is shown in Figure 2.5.

### 2.2.2 Multiple MOSFET circuit: detecting sample variation

Multiple power MOSFETs were aged using both power and thermal overstress in a controlled environment. The main objective of this test was to identify the sample variation from device to device by applying similar stress to a group of MOSFETs. Three groups of MOSFETs were selected with four devices in each group with similar characteristics ($R_{DS\ (ON)}$). No stress was applied to one group, one group was aged by moderate power stress, and the third group was aged by extreme power stress. Schematics of the test setup of this group test are shown in Figure 2.6.

The value of current sense resistor ($R_{sense}$) was 0.05 Ω. Power dissipation across each device was calculated, and $R_{pot}$ was initially adjusted to ensure equal power stress across each of these four MOSFETs. The applied voltage was 1.46 V DC for moderately accelerated aging of one group of FDP 3672 N-channel power MOSFETs. The power dissipation across each MOSFET was ~ 9.417 W, and the surface temperature was stabilized at $200^0$C during the period of aging. The devices were aged at $110^0$C ambient temperature inside the thermal chamber for 150 minutes. These devices were cooled down to the room temperature after accelerated aging, and $R_{DS\ (ON)}$ were calculated while the MOSFET was connected in a dc-dc converter circuit (test setup of Figure 2.4(b)). It was found that all four MOSFETs in a group had similar rise in $R_{DS\ (ON)}$ as a result of aging, and the rate of increment was ~25%. These values of $R_{DS\ (ON)}$ before and after aging are given in Table 2.4.

A 1.66 V DC voltage was applied for extremely accelerated aging of one group of MOSFETs and the power dissipation was ~12.35 W across each of the devices. The surface temperature was ~$245^0$C during this extremely accelerated aging procedure, while the

ambient temperature was $110^0$C. The drain current of the devices dropped to zero after 90 minutes of aging because of the complete failure of one MOSFET in the group. The failure related to a single MOSFET caused a sudden imbalance in current through the remaining MOSFETs. Therefore, thermal impedance of the devices increased significantly which led the devices to act like an open circuit and finally drain current of all MOSFET's reached zero. $R_{DS\,(ON)}$ of these devices were calculated after gradually bringing the devices to room temperature and a large increment in $R_{DS\,(ON)}$ of one MOSFET (M16) was observed. $R_{DS\,(ON)}$ of M15 was increased only about 2 mΩ and this is not practical after applying extreme stress. Group 3 MOSFETs were aged for only 90 minutes and M15 was not affected so much for this short duration. All MOSFETs might not be aged similarly under extreme stress states for a short duration. This could be due to the manufacturing issues of the MOSFETs. The variations in $R_{DS\,(ON)}$ before and after aging are given in Table 2.4.

## 2.3 Characterization of IGBTs

### 2.3.1 Single IGBT circuit

Three IRGI4090PbF trench IGBTs were stressed in a controlled environment as shown in Figure 2.7 (a). A 1V DC voltage was applied between the collector and emitter of the IGBTs, and due to the high power dissipation (~8.5W) across them, the surface temperature increased to 150°C within 10 minutes. These IGBTs were placed in a controlled temperature chamber at 110°C. The above procedure was applied to three different IGBTs for different time durations. The devices were cooled down to room temperature, and the characteristics were recorded. It was found that the collector to emitter voltage ($V_{CE}$) of IGBTs G2, G3, and G4 significantly increased due to this accelerated aging. Due to the

change in $V_{CE}$, the equivalent impedances of these IGBTs were also affected at particular operating conditions. While taking these measurements, the gate voltage was 15V, series resistance ($R_{Lim}$) was 4Ω and $V_{in}$ was 12V (Figure 2.7(b)). Measured $V_{CE}$ and equivalent resistance ($R_{CE}$) for both aged and new IGBTs have been provided in Table 2.5 and Figure 2.8.

### 2.3.2 Multiple IGBT circuit: detecting sample variation

Similar to power MOSFETs, several IGBTs were aged using both power and thermal overstress in a controlled environment. The main objective of this test was to identify the sample variation from device to device by applying similar stress to a group of devices. Three groups of IGBTs were selected with four devices in each group with similar characteristics (collector-emitter ON voltage). No stress was applied to a group, one group was aged by moderate power stress, and the third group was aged by extreme power stress. Schematics of the test setup of this group test are shown in Figure 2.6. The value of current sense resistor ($R_{sense}$) was 0.05 Ω. Power dissipation across each device was calculated, and $R_{pot}$ was initially adjusted to ensure equal power stress across each of these four IGBTs.

A group of N-channel 6A 1200V IGBTs were moderately aged by applying a 2.15V DC between the collector and emitter. The operating conditions of these IGBTs were matched by adjusting $R_{pot}$. The power dissipation of each IGBT was ~8.85 W, and the surface temperature reached $200^0$C with an ambient temperature of $110^0$C. The devices were aged for 150 minutes and characteristics were measured when the devices reached room temperature. It was found that $V_{CE}$ decreased with higher aging. However, $V_{CE}$

increased with aging of IRGI4090PbF trench IGBTs described earlier. Therefore, the change of $V_{CE}$ may be positive or negative for different devices.

Similar to power MOSFETs, one group of IGBT was aged using extreme power stress (~13.38 W). A 2.25V DC voltage was applied during this extreme accelerated aging procedure and surface temperature reached close to $250^0$C while the ambient temperature was $110^0$C. Three IGBTs of this group failed to operate and the collector current dropped to zero after 80 minutes of aging, and one IGBT showed higher $V_{CE}$ after aging. The variation in $V_{CE}$ of these two groups as a function of aging has been summarized in Table 2.6. Due to the change in $V_{CE}$, the equivalent resistance ($R_{CE}$) of the aged IGBTs also changed.


Figure 2.1: The photograph of the environment test chamber (DELTA 9059) used in this project.

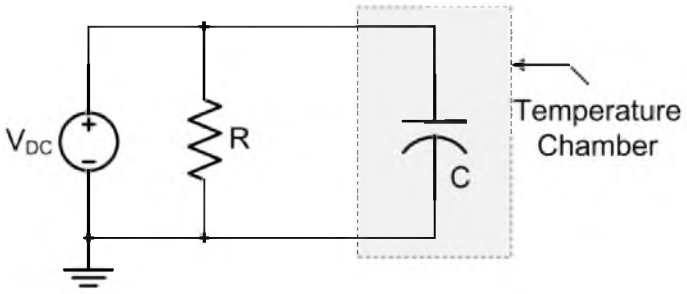



Figure 2.2: Schematic of the test setup to characterize electrolytic capacitors.

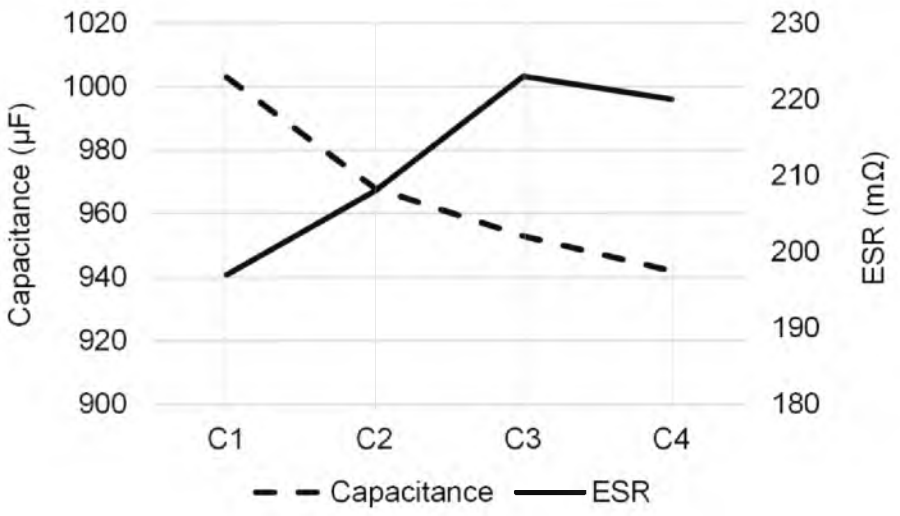



Figure 2.3: Variation in ESR and capacitance of electrolytic capacitors under thermal stress.

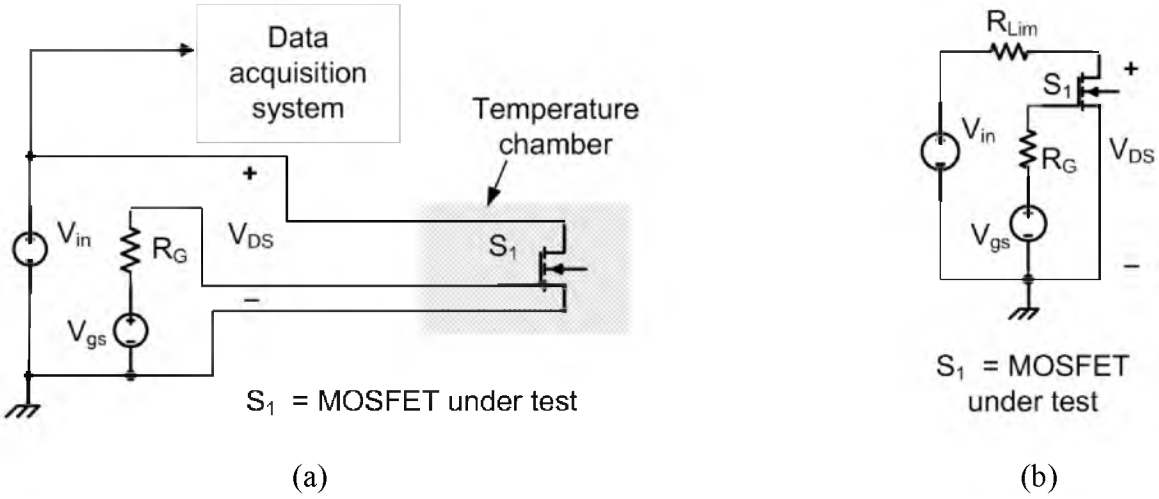



Figure 2.4: (a) Experimental setup used for quantifying the accelerated aging of the MOSFETs; (b) experimental setup used to measure $R_{DS\,(ON)}$.

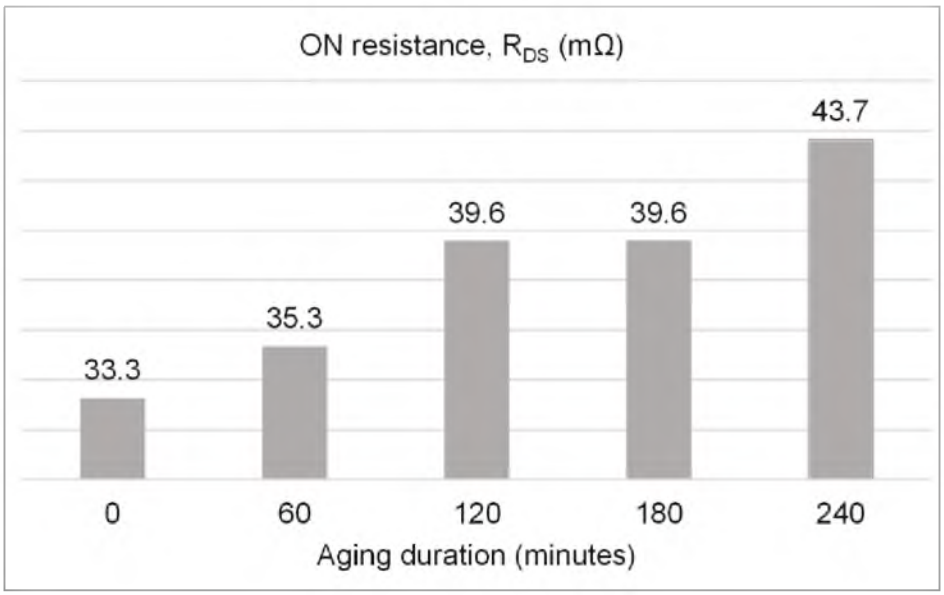



Figure 2.5: Measured $R_{DS\,(ON)}$ for different MOSFETs (M1 – M5) as a function of aging duration.

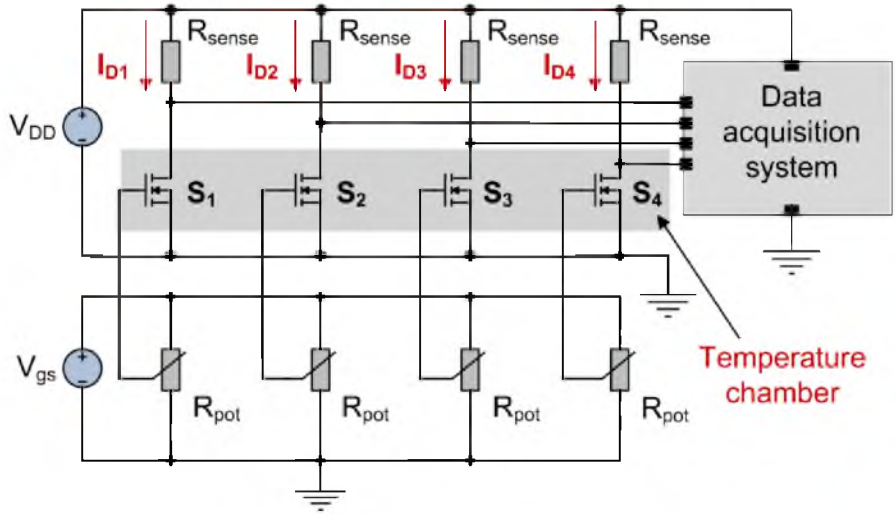
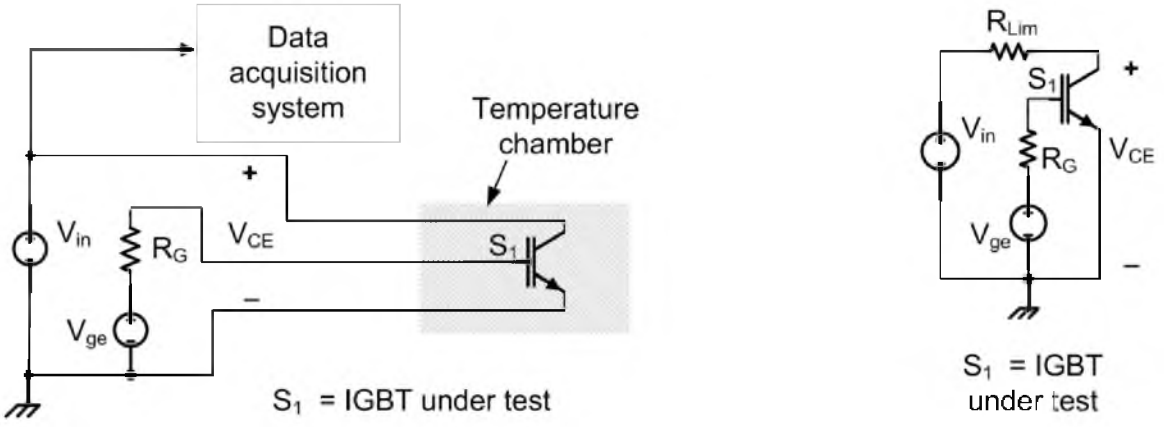



Figure 2.6: Schematic of the test setup to conduct accelerated aging of MOSFETs in groups.




(a) (b)

Figure 2.7: (a) Experimental setup used for quantifying the accelerated aging of the IGBTs; (b) experimental setup used to measure $R_{CE}$.

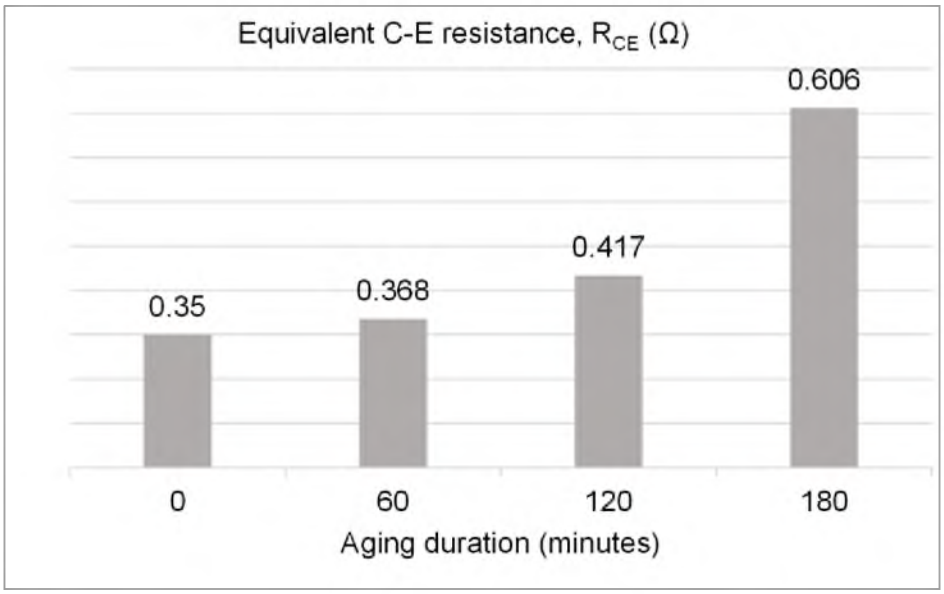



Figure 2.8: Measured $R_{CE}$ for different IGBTs (G1 – G4) as a function of aging duration.

Table 2.1: Devices under test and their corresponding parameters.

| **Component** | **Test with** | **Applied Stress** | **Observed parameter** |
|---|---|---|---|
| Capacitor | **Single** electrolytic capacitor circuit | Thermal | ESR |
| MOSFET | **Single** MOSFET circuit | Both power and thermal | $R_{DS\ (ON)}$ |
| | **Multiple** MOSFETs circuit | | |
| IGBT | **Single** IGBT circuit | Both power and thermal | $V_{CE}$ and $R_{CE}$ |
| | **Multiple** IGBTs circuit | | |

Table 2.2: Experimental results obtained from the capacitor characterization test conducted with thermal stress.

| Capacitors | **C1 [New]** | **C2 [Aged]** | **C3 [Aged]** | **C4 [Aged]** |
|---|---|---|---|---|
| Aging temperature | ------ | $150^{O}C$ | $160^{O}C$ | $170^{O}C$ |
| Capacitance (µF) before aging | 1003 | 1001 | 998 | 997 |
| Capacitance (µF) after aging | ------ | 968 | 953 | 942 |
| ESR (mΩ) before aging | 197 | 197 | 200 | 195 |
| ESR (mΩ) after aging | ------ | 208 | 223 | 220 |
| Ripple voltage (V) before aging (p-p) | 1.88 | 1.82 | 1.86 | 1.86 |
| Ripple voltage (V) after aging (p-p) | ------ | 1.94 | 1.96 | 1.96 |

Table 2.3: Measured $R_{DS\ (ON)}$ for multiple MOSFETs aged by power and thermal stress.

| MOSFETs | M1 | M2 | M3 | M4 | M5 |
|---|---|---|---|---|---|
| Aging duration (minutes) | 0 | 60 | 120 | 180 | 240 |
| $R_{DS\ (ON)}$ (mΩ) | 33.26 | 35.34 | 39.57 | 39.58 | 43.65 |

Table 2.4: Measured $R_{DS\ (ON)}$ for three groups of MOSFETs before and after accelerated aging.

| MOSFETs | | $R_{DS\ (ON)}$ (mΩ) before aging | $R_{DS\ (ON)}$ (mΩ) after aging |
|---|---|---|---|
| Group 1 (not aged) | M6 | 34.823 | ---- |
| | M7 | 34.751 | ---- |
| | M8 | 34.751 | ---- |
| | M9 | 35.050 | ---- |
| Group 2 (moderately aged) | M10 | 34.275 | 42.968 |
| | M11 | 34.161 | 42.622 |
| | M12 | 34.123 | 42.613 |
| | M13 | 34.303 | 41.410 |
| Group 3 (extremely aged) | M14 | 33.884 | 41.231 |
| | M15 | 34.021 | 35.862 |
| | M16 | 34.206 | **6899** |
| | M17 | 34.188 | 46.718 |

Table 2.5: Measured $R_{CE}$ for multiple IGBTs aged by power and thermal stress.

| IGBTs | G1 | G2 | G3 | G4 |
|---|---|---|---|---|
| Aging duration (minutes) | 0 | 60 | 120 | 180 |
| $V_{CE}$ (V) | 0.95 | 0.98 | 1.10 | 1.50 |
| $R_{CE}$ (Ω) | 0.350 | 0.368 | 0.417 | 0.606 |

Table 2.6: Measured $R_{CE}$ for three groups of IGBTs before and after accelerated aging.

| IGBTs | | $V_{CE}$ (V) before aging | $V_{CE}$ (V) after aging | $R_{CE}$ (Ω) before aging | $R_{CE}$ (Ω) after aging |
|---|---|---|---|---|---|
| Group 1 (not aged) | G5 | 2.07 | ---- | 0.828 | ---- |
| | G6 | 2.08 | ---- | 0.832 | ---- |
| | G7 | 2.06 | ---- | 0.822 | ---- |
| | G8 | 2.05 | ---- | 0.820 | ---- |
| Group 2 (moderately aged) | G9 | 2.10 | 1.9 | 0.845 | 0.754 |
| | G10 | 2.10 | 1.5 | 0.843 | 0.568 |
| | G11 | 2.10 | 1.5 | 0.841 | 0.570 |
| | G12 | 2.08 | 1.65 | 0.836 | 0.658 |
| Group 3 (extremely aged) | G13 | 2.05 | 3.03 | 0.826 | 1.3001 |
| | G14 | 2.05 | **15** | 0.827 | ∞ |
| | G15 | 2.06 | **15** | 0.830 | ∞ |
| | G16 | 2.03 | **15** | 0.825 | ∞ |

# CHAPTER 3

# EXISTING AGING MEASUREMENT TECHNIQUES AND THEIR LIMITATIONS

There exist several real time methods to estimate the state of health of power converters. This section presents the comparison of the proposed method with conventional device characterization techniques, elucidating advantages of the proposed method. Reference [35] proposed a real time monitoring of capacitor ESR based on the power dissipation across the capacitor and the capacitor current. Capacitor voltage and currents are continuously monitored to determine power dissipation. An online monitoring method was presented in reference [36] that measures the junction temperature of power devices in a voltage source inverter, and this temperature was found directly related to the operating states of the inverter. Online fault diagnosis methods in power electronic drives were described in reference [37] by measuring capacitor ESR, MOSFET $R_{DS\,(ON)}$ and $V_{CE(sat)}$ of IGBT. ESR was calculated from capacitor voltage and current. $R_{DS\,(ON)}$ was calculated from corresponding ripple voltage and ripple current of the MOSFET. Measurements of $V_{CE}$ were taken to identify degradation of IGBTs.

Monitoring solder joint fatigue in power modules using the case above ambient temperature was proposed in [38]. The case above ambient temperature was measured using a two channel thermometer, and the module power loss was calculated using this

temperature. Power loss is directly related to thermal resistance, which is an indicator of aging. Another online fault diagnosis technique in DC-DC converters was proposed in [39] by calculating the ESR of the DC bus capacitor. ESR was calculated from input current and output voltage ripple of the converter. In reference [27], $R_{DS\ (ON)}$ of power MOSFETs was calculated as the ratio of drain-source voltage ($V_{DS}$) and drain current ($I_D$) during on-state. Reference [40] proposed an online diagnosis method considering the variation in parasitic/internal resistance of components in a DC-DC converter. However, this diagnosis method is applicable to diagnose the entire system, not individual components. Chapter 2 describes several aging affected parameters of components used in power converters and methods used to detect these parameters. Most of the methods are only suitable for detection of component based degradation.

# CHAPTER 4

# PROPOSED METHODOLOGY

Spread spectrum time domain reflectometry (SSTDR) has been used in this project to extract different component parameters in a live power converter. Most of the conventional techniques estimate a converter's reliability by measuring individual components' characteristics while they are disconnected from the circuit. Even though they are characterized in real time, results obtained by characterizing individual components cannot be applied for prediction of overall converter reliability. In order to overcome this limitation, spread spectrum time domain reflectometry (SSTDR) has been used to obtain several parameters of the individual components as well as the converter circuit. Reflectometry is conventionally used for locating wiring faults, and references [41]- [47] presented several reflectometry techniques to identify aircraft wiring faults and aging.

## 4.1 Fundamentals of SSTDR

Fundamentals of SSTDR and its operation are described in this section. Using reflectometry, a high frequency electrical signal is sent down the wire, and it reflects from any impedance discontinuity. The reflection coefficient gives a measure of how much signal is returned and is given by $\rho$.

$$\rho = \frac{z_t - z_o}{z_t + z_o} \tag{4.1}$$

where $Z_o$ is the characteristic impedance of the transmission line and $Z_t$ is the impedance connected at the terminatinfg end of the transmission line. The time or phase delay between the incident and reflected signals provides the distance to the fault, and the observed magnitude of the reflection coefficient provides the impedance at discontinuity. It has been discussed in the previous sections how the measurable electrical attributes of power MOSFETs in a power converter can be determined to characterize the aging in a power converter. As the aging of capacitors and semiconductor switches are directly related to the impedance variation, reflectometry can be used to identify the gradual changes of impedance of capacitors and semiconductor switches in a power converter by comparing the impedance values with the reference values consistent with a new converter.

A block diagram of SSTDR setup is shown in Figure 4.1. A sine wave generator (operating at 30–100 MHz) is used as master system clock, and this generator's output is converted to a square wave via a shaper, and the resulting square wave drives a pseudo-noise digital sequence generator (PN gen). The sine wave is multiplied by the output of the PN generator in the SSTDR setup, and the test signal is injected into the cable. The other end of the cable is connected across the device under test. The reflected signal from the cable (including any digital data or AC signals in the cable, and any reflections observable at the receiver) are fed to a correlator circuit along with the reference signal. Inside the correlator, the received signal and the reference signal are multiplied, and the result is fed to an integrator. The output of the integrator is sampled with an analog-to-digital converter (ADC). A full correlation can be collected by repeatedly increasing the phase delay using

the variable phase delay unit and acquiring the correlated output using the ADC. The location of the various peaks (either positive or negative) in the full correlation indicates the location of impedance discontinuities such as open circuits, short circuits, and arcs (intermittent shorts).

## 4.2 Other reflectometry methods

There are several reflectometry methods such as time domain reflectometry (TDR), frequency domain reflectometry (FDR), sequence time domain reflectometry (STDR) and so on, which are commonly being applied to detect cable fault. Other than cable fault detection, there are several applications of reflectometry techniques to detect degradation in circuits. TDR sends a step voltage from the source end, and this method was used in reference [48] to measure the parasitic parameters of printed circuit boards (PCB). Reference [49] presented characterization of interconnect parasitic in switching power converters using TDR. In addition, TDR was used in [50] [51] to detect two interconnect failures: solder joint cracking and solder pad separation. Techniques for prognostic solder joint degradation using TDR has been discussed in [52]. Capacitance of a pad in CMOS process was estimated using an "on wafer" TDR measurement system in [53], and the method of extracting series resistance of capacitors using TDR was presented in [54]. The major limitation of TDR is the higher cost compared to other techniques and limited performance in live networks. In order to overcome the limitations of TDR, SSTDR has been used to estimate the state of health of power semiconductor switches and electrolytic capacitors. SSTDR uses a sine wave modulated pseudo noise (PN) code as the test signal. SSTDR has already been commercially used for locating faults in aircraft wires [45] as

well.

## 4.3 Reasons behind using SSTDR for device characterization

The proposed solution for device characterization is application of Spread-spectrum time domain reflectometry (SSTDR) technique. The major advantages of this method are usability in live system and negligible interference with system noise. SSTDR generates various correlated peak values depending on the impedance of device under test. From the aging effect on device parameters described in the previous chapter, it is found that impedance values of capacitors and semiconductor switches shifted from their initial states. Therefore, SSTDR can be applicable to identify the changes of device parameters. SSTDR generated correlated outputs for open circuit and short circuit at the end of 50 foot cable are given in Figure 4.2.

A typical SSTDR generated plot across a 13 Ω carbon film resistor is shown in Figure 4.3. SSTDR hardware generates correlation plots for various frequencies (96 MHz, 48 MHz, 24 MHz, 12 MHz) sent from the PN signal generator, and the exact peak value of the correlated outputs varies with the frequency. The plot shown in Figure 4.3 is generated for 96 MHz frequency. It has been found in the conducted experiments that the SSTDR data generated at 24 MHz and 48 MHz of PN signal present the best performance in determining parameters of failure sensitive devices (capacitors and semiconductor switches) in power converter circuit.

SSTDR was applied to three carbon film resistors having different values (13 Ω, 9.1 Ω and 1.6 Ω) for comparing the correlated data and it generated three different peak values. The lower the resistor values, the lower the correlated peak values and vice versa. The plots

are shown in Figure 4.4.

## 4.4 Individual component characterization using SSTDR

SSTDR was applied to electrolytic capacitors, power MOSFETs and IGBTs for characterization purpose while these devices were connected to an energized circuit. A 54 foot 75 Ω (RG 59) coax cable was connected in between the test circuit and the SSTDR system while SSTDR was applied across the device under test. Because of the uniform impedance of the coax cable over the entire length, a peak in correlated output was observed only at the starting point (due to the impedance mismatch between SSTDR hardware and the coax cable) and at the end terminal of the cable (due to the impedance mismatch between the coax cable and the devices under test). The amplitude of the peak is dependent on the value of the impedance of the device under test. Detailed experimental results of device characterization using SSTDR are described in the following sections.

### 4.4.1 Electrolytic capacitor characterization

SSTDR was applied to the aged capacitors (C2, C3, C4), and a new capacitor (C1). An unfiltered rectified voltage was used as the voltage source and the test schematic is shown in Figure 4.5. The input of the rectifier was 3 V (RMS) 60 Hz. The change in capacitance, ESR and correlated outputs from SSTDR hardware for aged capacitors (C2, C3, C4) and the new capacitor (C1) are given in Table 4.1. From Table 4.1, it is apparent that the ESR and the capacitances change due to thermal aging, and the SSTDR measurement can identify these variations.

4.4.1.1 Mapping capacitor characteristics as a function of aging

Aging level of capacitors (C1, C2, C3, and C4) were calculated considering 100% increments in ESR as 100% aging [8]. Variation in ESR and correlated outputs as a function of level of aging in the case of electrolytic capacitors are shown in Figure 4.6. Figure 4.6 shows that the ESR of the capacitors increased with higher aging. The ESR of C4 became less than that of C3 after aging. However, the increment in ESR compared to the initial value is higher in the case of C4 than the increment observed in C3. SSTDR hardware cannot identify very small impedance variation and this is why the correlated output of C3 is lower compared to C4, although C3 should have the highest correlated output because of its highest ESR.

### 4.4.2 Power MOSFET characterization

SSTDR was applied to all five MOSFETs (M1 ~ M5) in order to compare the characteristics of M1 with the aged MOSFETs as shown in Table 4.2 and Figure 4.7. Data from SSTDR test system were extracted into MATLAB, and the correlated outputs vs. distance characteristics are shown in Figure 4.8. The correlated amplitude is the true measure of the reflected power, and the reflected power is a function of the impedance at the far end of cable. If correlated waveform is normalized to the highest peak in the data, all amplitudes would be a fractional number between -1.0 to +1.0.

From the difference in correlated output (Figure 4.9) at the far end of the cable, it was found that the difference in $R_{DS\,(ON)}$ values for M1 and M5 were the highest, and the corresponding difference in reflection coefficient (SSTDR generated correlated output) were the highest as well. A similar phenomenon was observed for M3 and M4 where the

difference in their $R_{DS\ (ON)}$ was the lowest. SSTDR hardware generates several sampled values of correlated outputs along the coax cable, and because the MOSFETs were connected at end terminals of the cable, the peak value of correlated amplitude at this point (~ 54 feet) is different for various MOSFETs under test. These differences were calculated by subtracting the correlated amplitudes of one MOSFET from another MOSFET. The difference in correlated peak was 93 when difference in $R_{DS\ (ON)}$ was 10.39 mΩ, and the difference in correlated peak was 6 when difference in $R_{DS\ (ON)}$ was 0.01 mΩ. So, if the values of $R_{DS\ (ON)}$ are nearly equal, then SSTDR will generate similar or approximately equal values of correlated output. The existing SSTDR hardware used for taking measurements for this project cannot generate distinct data if the difference in impedance is 1~2 mΩ. This will be shown in later experimental results. From the above experimental results, the variation in $R_{DS\ (ON)}$ can be predicted from the variation in the amplitude of the correlated outputs. Because the value of the $R_{DS\ (ON)}$ is directly related to the state of health of power MOSFETs, the variation in correlated output is a true representation of the MOSFET aging. Calculation of $R_{DS\ (ON)}$ from the SSTDR generated peak correlated outputs are discussed in later sections.

SSTDR was applied to the MOSFETs aged in multiple MOSFET circuit as well. The test schematic was similar to Figure 4.7. A 54 foot long 75 Ω coax cable was connected between the SSTDR hardware and the device under test. The peak of the correlation data for each of the MOSFETs are given in Table 4.3. From the peak values generated by the SSTDR hardware it is apparent that SSTDR can generate consistent output depending on the impedance of the devices. However, the existing SSTDR hardware cannot faithfully detect a change in impedance that is very small (1~3 mΩ). The $R_{DS\ (ON)}$ of M13 are smaller

than that of M10 and M11, and the corresponding SSTDR output of M13 should be more negative compared to M10 and M11. However, the SSTDR hardware generated almost equal peak values in the case of these three MOSFETs. Due to the drastic increment in $R_{DS\ (ON)}$ of M16, the peak SSTDR is significantly smaller than the other MOSFETs. Therefore, this MOSFET can be considered as a damaged one.

4.4.2.1 Mapping MOSFET characteristics as a function of aging

The failure threshold can be considered as 25% increase in $R_{DS\ (ON)}$ for power MOSFETs [26]. Failure threshold is calculated as the ratio of change in $R_{DS\ (ON)}$ ($\Delta R_{DS\ (ON)}$) to the initial $R_{DS\ (ON)}$. This ratio can be used to measure the approximate aging level of MOSFETs M1 to M5, although it is an arbitrary value. Calculated aging level of M1 to M5 are given in Table 4.4. The $\Delta R_{DS\ (ON)} / R_{DS\ (ON)}$ in case of M5 is 31.24% which is more than 25%. However, M5 is considered as 100% aged and all MOSFETs' initial $R_{DS\ (ON)}$ was considered as 33.26 mΩ for simplicity (this initial $R_{DS\ (ON)}$ value is consistent with the value obtained from the datasheet). Using M1 and M5 as the two extreme boundaries, the level of aging associated to M2, M3 and M4 were calculated. Variation in $R_{DS\ (ON)}$ and correlated outputs as a function of level of aging are shown in Figure 4.10. This figure also shows that $R_{DS\ (ON)}$ as well as the correlated output becomes larger with the level of aging. From Table 4.4, M3 and M4 have almost equal values of $R_{DS\ (ON)}$ which corresponds to ~60% aging level. However, there is a small variation observed in the correlated outputs of these two MOSFETs. SSTDR hardware may generate slightly different outputs while measuring the same impedance. This is why a mismatch in correlated outputs was observed at 60% aging level although they have almost equal values of $R_{DS\ (ON)}$.

### 4.4.3 IGBT characterization

SSTDR was applied to the IGBTs (G1 ~ G4) in order to compare the characteristics of the new device (G1) with the aged devices (G2, G3, G4) similar to MOSFETs as shown in Figure 4.7. Measured equivalent impedances of IGBTs and corresponding SSTDR correlated amplitudes for both aged and new IGBTs have been provided in Table 4.5. It was noticed that SSTDR generates the lowest correlated peak output for highly aged IGBT and highest correlated peak output for new IGBT. As the equivalent resistance of IGBTs are related to the level of aging and SSTDR output is a true measurement of the impedance of the device under test, the lowest peak output was observed in highly aged IGBT. SSTDR was applied to IGBTs G5 ~ G16 as shown in Figure 4.7 and the corresponding peak correlated outputs generated by SSTDR system with equavalent impedances of each IGBTs are provided in Table 4.6.

## 4.5 Parameter estimation from correlation peak amplitude

For parameter estimation, only MOSFETs were analyzed to extract the parameter from the SSTDR generated correlated outputs. This section describes how the $R_{DS\,(ON)}$ values can be calculated from the correlated outputs generated by the SSTDR system. Once the initial $R_{DS\,(ON)}$ and corresponding SSTDR generated correlated outputs are known, the new $R_{DS\,(ON)}$ after accelerated aging can be easily determined from the SSTDR data. Using the data summarized in Table 4.2, Figure 4.11(a) was drawn and it shows the relationship between the $R_{DS\,(ON)}$ values and correlated outputs. This relationship can be quantified as shown in equation 4.2 using the basic fitting tool in MATLAB. Here 'x' and 'y' represent peak correlated output and $R_{DS\,(ON)}$, respectively.

$$y = -6.3558 \times 10^5 - 47.029x - 0.0008699x^2 \quad (4.2)$$

Using equation 4.2, it is possible to calculate the $R_{DS\,(ON)}$ of MOSFETs M6 to M17 by using the SSTDR data given in Table 4.3. The actual $R_{DS\,(ON)}$ values, SSTDR outputs and $R_{DS\,(ON)}$ values calculated using equation 4.2 are given in Table 4.7. A graphical comparison between actual and calculated $R_{DS\,(ON)}$ is given in Figure 4.11(b).

Calculated $R_{DS\,(ON)}$ of all MOSFETs except M16 are nearly equal to the actual $R_{DS\,(ON)}$ values. SSTDR generates outputs depending on the equivalent impedance across the test nodes. According to Figure 4.7, SSTDR was applied across the drain and source nodes of MOSFET which is in parallel with ($R_{Lim} + R_S$), where $R_S$ is the source's internal resistance. Therefore, SSTDR generates output based on the impedance of "$R_{DS\,(ON)} \parallel (R_{Lim} + R_S)$." $R_{DS\,(ON)}$ values of all MOSFETs except M16 are very small (in the range of 34 ~ 47 mΩ) compared to "$R_{Lim}$ (=5 Ω) + $R_S$." Therefore the SSTDR generated outputs can be considered as true representations of actual $R_{DS\,(ON)}$ values. However, this statement is not correct in the case of M16 because of its very high $R_{DS\,(ON)}$ value. The best fit curve of Figure 4.11(a) and the function given in equation 4.2 were derived for very low $R_{DS\,(ON)}$ values compared to $R_{DS\,(ON)}$ of M16, and this might not be suitable for calculating the exact impedance of M16. Considering a normal aging process, the proposed SSTDR system can detect aging associated to the devices as well as any faults or damages (M16). The test setup for applying stress to the devices and characterizing the devices using SSTDR is shown in Figure 4.12.

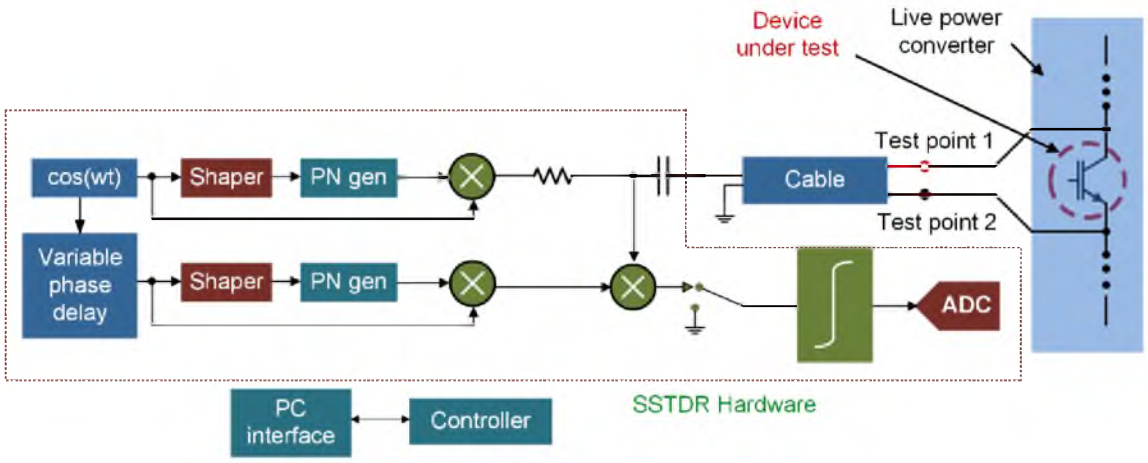



Figure 4.1: Block diagram of the SSTDR test system (adapted from [45]).

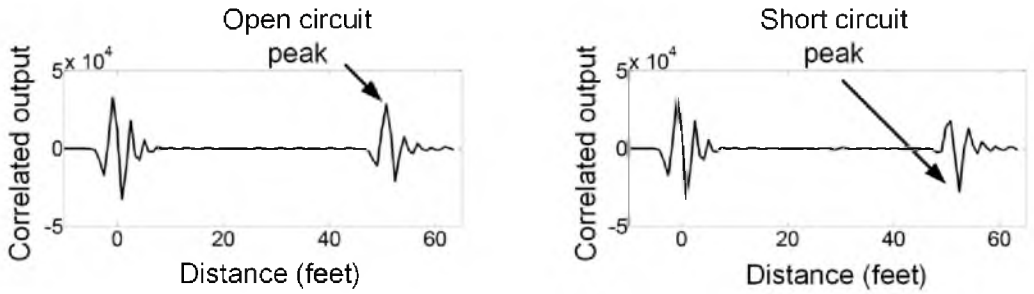



Figure 4.2: SSTDR generated open and short circuit plots across a 50 foot coax cable.

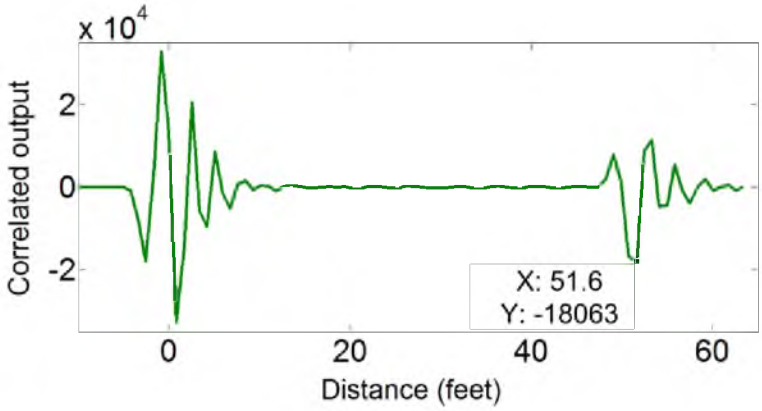



Figure 4.3: Typical SSTDR generated plot across a 13 Ω carbon film resistor.

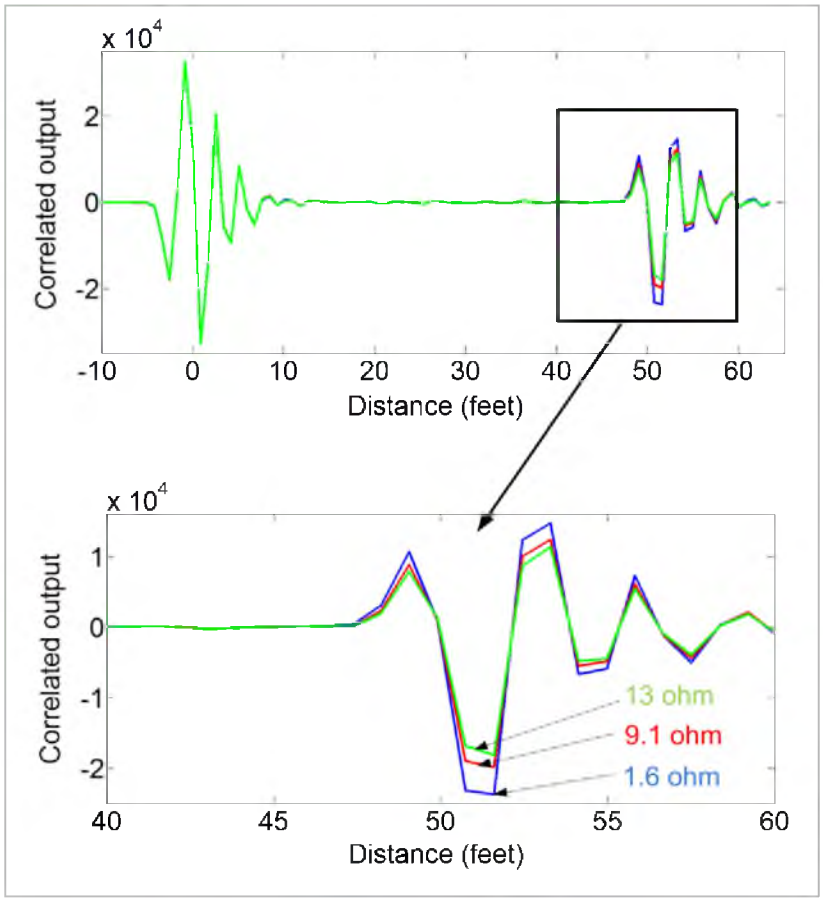



Figure 4.4: Variation in correlated output for three different resistors.

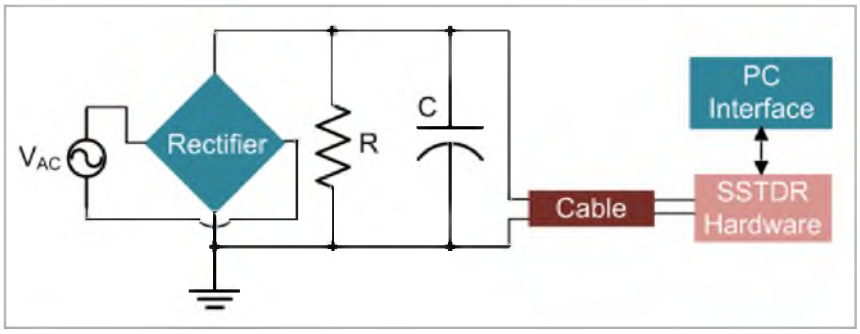



Figure 4.5: Test schematic to characterize the electrolytic capacitors using SSTDR.

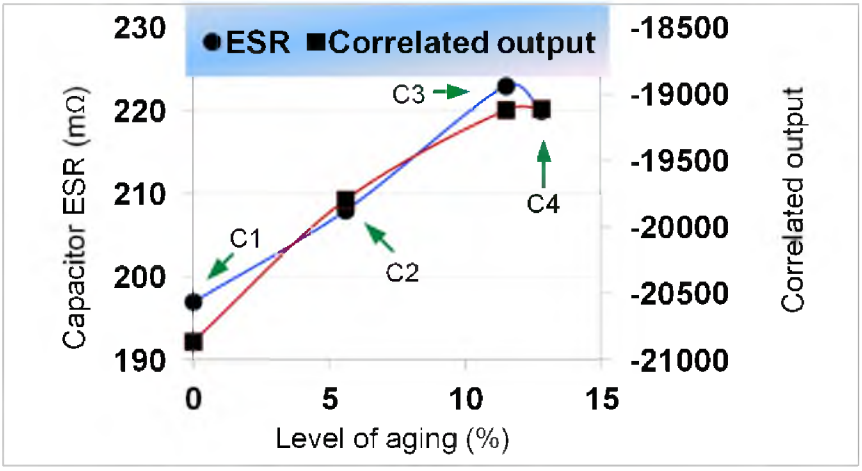



Figure 4.6: Variation in capacitor ESR and correlated output as a function of aging.

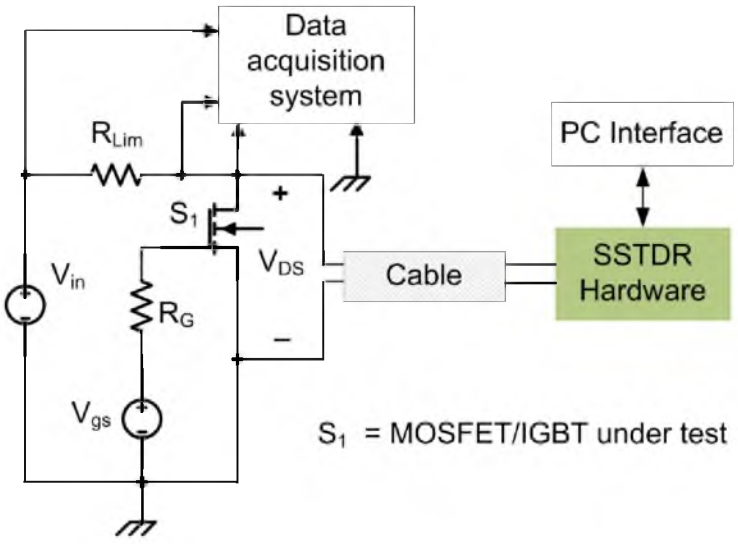



Figure 4.7: Test setup to characterize MOSFET/IGBT using SSTDR.

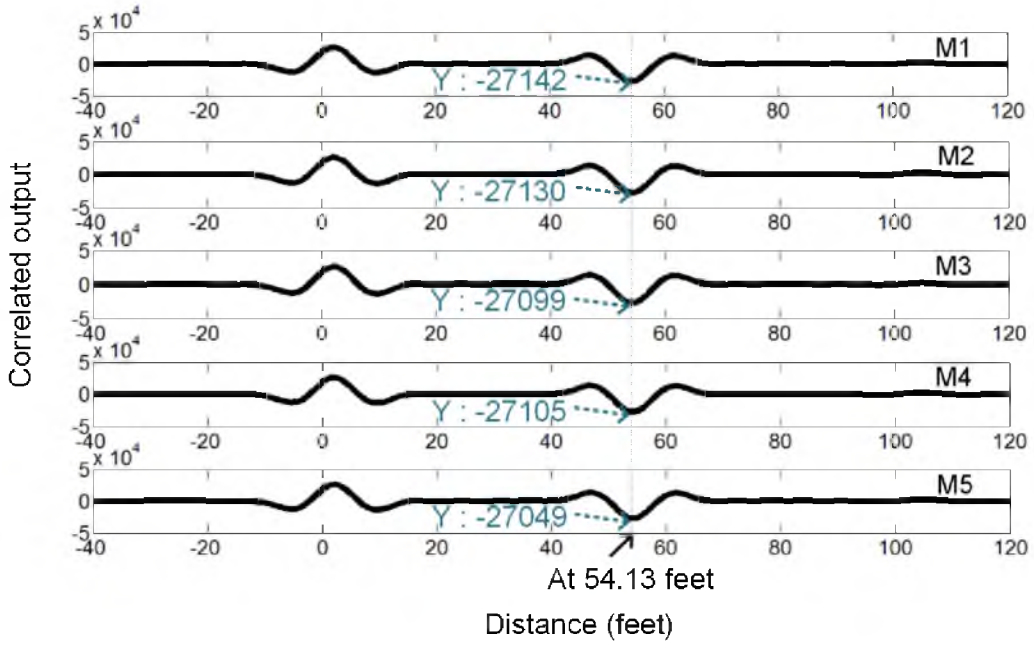



Figure 4.8: Correlated output for five different MOSFETs (M1, M2, M3, M4 and M5) obtained from test setup shown in Figure 4.7.

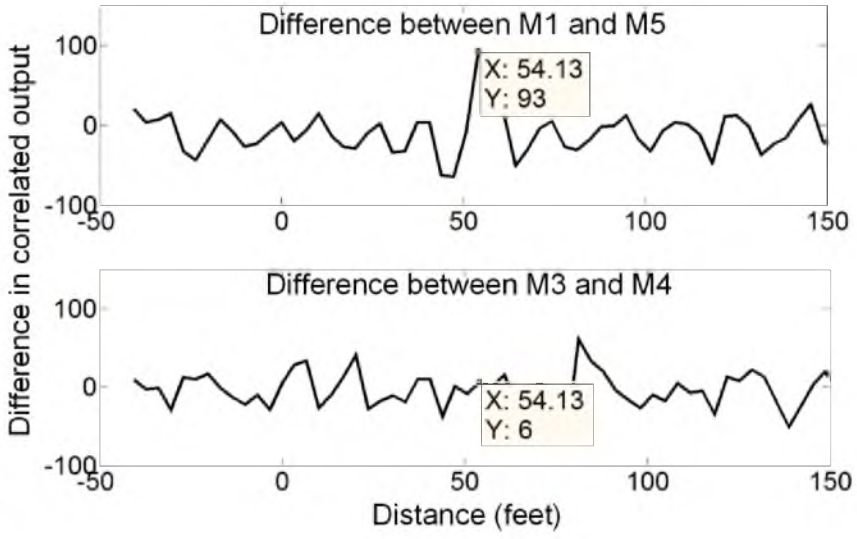



Figure 4.9: Differential correlated output associated with various MOSFETs under test.

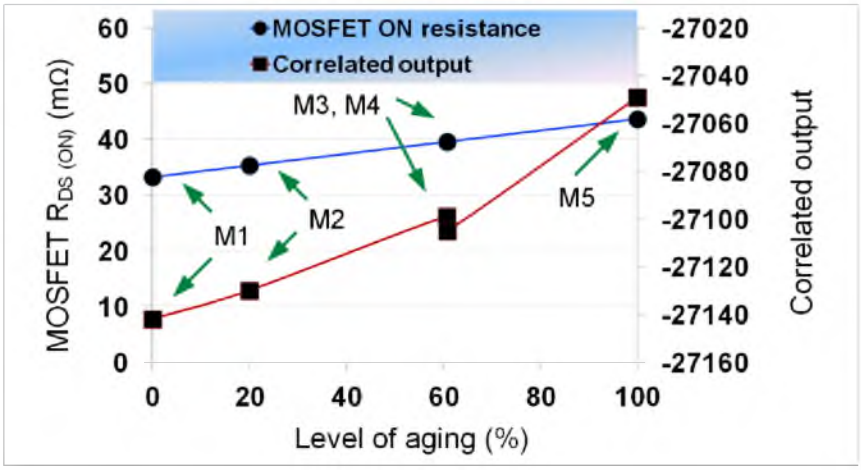
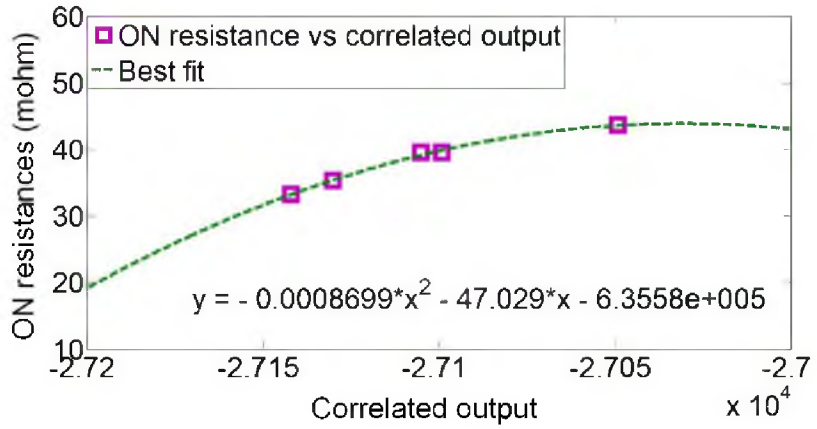
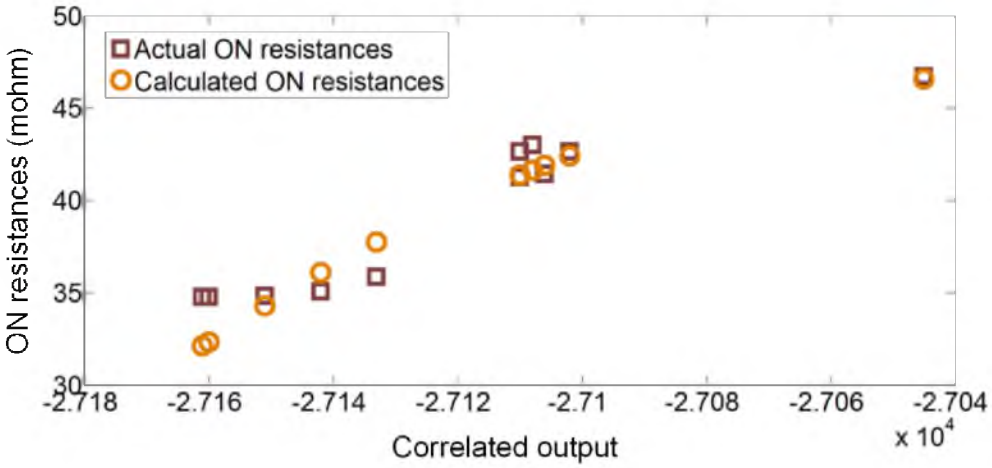



Figure 4.10: Variation in MOSFET's $R_{DS\ (ON)}$ and correlated output as a function of aging.

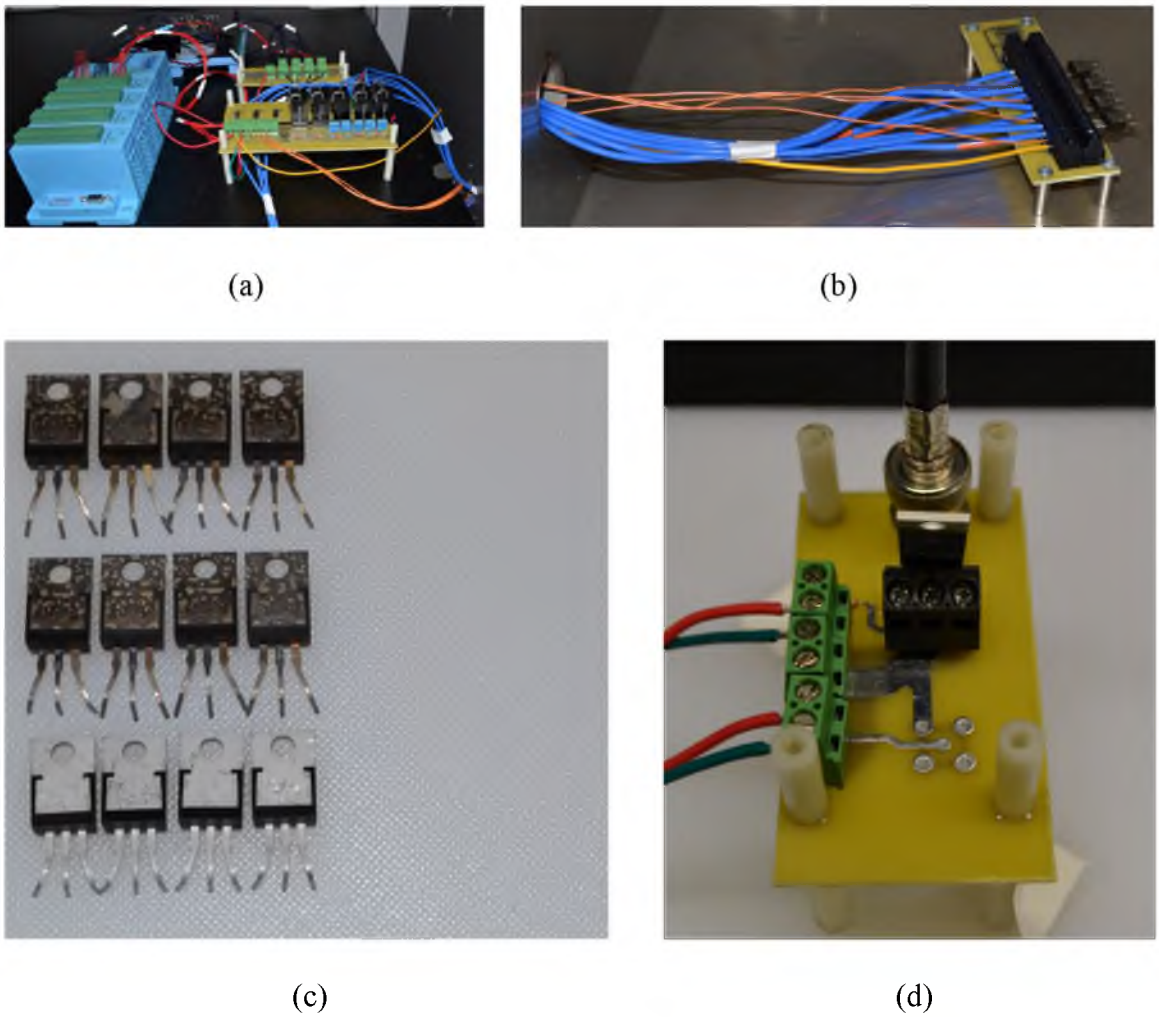



(a)




(b)

Figure 4.11: (a) Relationship between $R_{DS\,(ON)}$ and correlated output; (b) graphical comparison between actual and calculated $R_{DS\,(ON)}$.



(a) (b)

(c) (d)

Figure 4.12: Test setup showing the (a) data acquisition system connected to devices under test during accelerated aging procedure; (b) MOSFETs in the environment chamber (temperature chamber); (c) aged MOSFETs; (d) dc-dc converter circuit to characterize MOSFETs.

Table 4.1: Variation in peak correlated output, ESR, capacitance across the electrolytic capacitors under thermal stress.

| Capacitors | **C1 [New]** | **C2 [Aged]** | **C3 [Aged]** | **C4 [Aged]** |
|---|---|---|---|---|
| Capacitance (μF) | 1003 | 968 | 953 | 942 |
| ESR (mΩ) | 197 | 208 | 223 | 220 |
| Correlated amplitude | -20862 | -19794 | -19117 | -19109 |

Table 4.2: Peak values of correlated output and measured $R_{DS\,(ON)}$ for multiple MOSFETs aged by power and thermal stress.

| MOSFETs | M1 [New] | M2 [Aged] | M3 [Aged] | M4 [Aged] | M5 [Aged] |
|---|---|---|---|---|---|
| Duration of aging (minutes) | 0 | 60 | 120 | 180 | 240 |
| $R_{DS\,(ON)}$ (mΩ) | 33.26 | 35.34 | 39.57 | 39.58 | 43.65 |
| Correlated amplitude | -27142 | -27130 | -27099 | -27105 | -27049 |

Table 4.3: $R_{DS\ (ON)}$ and corresponding peak SSTDR output for three groups of MOSFETs.

| MOSFETs | | $R_{DS}$ (mΩ) | Peak SSTDR output |
|---|---|---|---|
| Group 1 (not aged) | M6 | 34.823 | -27151 |
| | M7 | 34.751 | -27160 |
| | M8 | 34.751 | -27161 |
| | M9 | 35.050 | -27142 |
| Group 2 (moderately aged) | M10 | 42.968 | -27108 |
| | M11 | 42.622 | -27110 |
| | M12 | 42.613 | -27102 |
| | M13 | 41.410 | -27106 |
| Group 3 (extremely aged) | M14 | 41.231 | -27110 |
| | M15 | 35.862 | -27133 |
| | M16 | **6899** | **-24566** |
| | M17 | 46.718 | -27045 |

Table 4.4: Calculated aging level of MOSFETs M1, M2, M3, M4 and M5. Table calculated with data from [26].

| MOSFETs | M1 | M2 | M3 | M4 | M5 |
|---|---|---|---|---|---|
| Change in $R_{DS\ (ON)}$, $\Delta R_{DS\ (ON)}$ = MOSFET $R_{DS\ (ON)}$ – initial $R_{DS\ (ON)}$ | 0 | 2.08 | 6.31 | 6.32 | 10.34 |
| Aging level = ($\Delta R_{DS\ (ON)}$ × 100%) / ($\Delta R_{DS\ (ON)}$ of M5) | 0% | 20% | 60.7% | 60.8% | 100% |

Table 4.5: Peak values of correlated output and measured $R_{CE}$ for several IGBTs aged by applying both power and thermal stress.

| IGBTs | **G1 [New]** | **G2 [Aged]** | **G3 [Aged]** | **G4 [Aged]** |
|---|---|---|---|---|
| Duration of aging (Minutes) | 0 | 60 | 120 | 180 |
| $R_{CE}$ (mΩ) | 35.01 | 36.79 | 41.706 | 60.606 |
| Correlated amplitude | -27449 | -27391 | -27358 | -27140 |

Table 4.6: Measured $R_{CE}$ and corresponding peak SSTDR output for three groups of IGBTs.

| IGBTs | | $R_{CE}$ (Ω) | Peak SSTDR output |
|---|---|---|---|
| Group 1 | G5 | 0.828 | -26832 |
| | G6 | 0.832 | -26858 |
| | G7 | 0.822 | -26855 |
| | G8 | 0.820 | -26837 |
| Group 2 | G9 | 0.754 | -26793 |
| | G10 | 0.568 | -27009 |
| | G11 | 0.570 | -27033 |
| | G12 | 0.658 | -26955 |
| Group 3 | G13 | 1.3001 | -26446 |
| | G14 | ∞ | **17711** |
| | G15 | ∞ | **17881** |
| | G16 | ∞ | **17775** |

Table 4.7: Calculated $R_{DS\ (ON)}$ using equation 4.2 and corresponding SSTDR data.

| MOSFETs | | Actual $R_{DS\ (ON)}$ (mΩ) | Calculated $R_{DS\ (ON)}$ (mΩ) | SSTDR peak at the load end |
|---|---|---|---|---|
| Group 1 (not aged) | M6 | 34.823 | 34.2798 | -27151 |
| | M7 | 34.751 | 32.3346 | -27160 |
| | M8 | 34.751 | 32.1097 | -27161 |
| | M9 | 35.050 | 36.0841 | -27142 |
| Group 2 (moderately aged) | M10 | 42.968 | 41.6287 | -27108 |
| | M11 | 42.622 | 41.3582 | -27110 |
| | M12 | 42.613 | 42.3984 | -27102 |
| | M13 | 41.410 | 41.8922 | -27106 |
| Group 3 (extremely aged) | M14 | 41.231 | 41.3582 | -27110 |
| | M15 | 35.862 | 37.7475 | -27133 |
| | M16 | 6899 | -5240.1 | -24566 |
| | M17 | 46.718 | 46.5865 | -27045 |

# CHAPTER 5

# AGING DETECTION IN AN H-BRIDGE AC-AC CONVERTER USING SSTDR

## 5.1 Aging and reliability

Reliability analysis of power converters allows researchers to predict failures based on the reliability of its components. Reliability theory predicts that even those systems that are entirely composed of nonaging elements (with a constant failure rate) will nevertheless deteriorate over time. A real time health monitoring system for a power converter is indispensable for satellite and other mission-critical power systems. An intelligent prognostic system can characterize the gradual degradation and failure mechanism of a power converter in an unknown environment, and it can also predict the future failures and prevent the associated damages. There is an imminent need to develop a real time method that can identify the location of an aged component as well as predict the overall system performance considering the aging associated to individual components. The bathtub curve of failure rate is the most accepted failure rate model for systems having electrical and mechanical components. This is shown in Figure 5.1 (a). The infant failure of the components is generally linked to poor design, poor installation or misapplication. Constant failure rate defines the useful lifetime of the component. The increasing failure rate after the constants failure rate is the wear-out failure rate. A system's availability can

be increased by conducting scheduled and unscheduled maintenance in four different ways: (1) in reactive maintenance, repair or replacement of damaged equipment is done when obvious problems occur, (2) preventive maintenance is performed at predetermined time intervals and it may be possible to repair/replace equipment before failure, 3) predictive maintenance is performed when mechanical or operational conditions are at the end of warranty, and 4) reliability centered maintenance (RCM) utilizes sophisticated failure analysis and prognostic maintenance in order to predict and pinpoint the potential failure mechanism. Figure 5.1(b) shows a comparative study showing that RCM applied in a pump system results in the lowest maintenance cost. No similar analysis was found for power converters and could be investigated under the scope of this project.

Future tasks under the scope of the project involve application of SSTDR to monitor the state of the health of different components in the system. SSTDR can detect the most critical devices that may lead a component or complete system failure. It is possible to process the data from SSTDR system to measure the reliability of components and replace those components before failure. Therefore, SSTDR is potentially an excellent candidate for reliability centered maintenance (RCM) program.

## 5.2 Challenges in measuring aging in a complex circuit

In a practical circuit, it is most likely that multiple components are connected in complex combination. It is difficult to find the aged component by applying SSTDR across random test pairs. Therefore, it is important to select the appropriate test pairs and where to apply the SSTDR to determine the aged devices in a power converter circuit. In addition, SSTDR generates correlated outputs based on the equivalent path impedance across the

device under test. Let us assume an H-bridge ac-ac converter shown in Figure 5.2. There are four test points to apply SSTDR. If the SSTDR is applied across test points one and two, SSTDR will generate correlated data based on the equivalent impedance between these two points. So, it is necessary to develop a reverse synthesis method to determine the impedance of any specific component from the equivalent impedances obtained from SSTDR generated data. The analysis will be described in the following sections.

## 5.3 Test setup for applying SSTDR to an H bridge ac-ac converter

SSTDR was applied to a power converter circuit while the converter was operational. This test was performed to verify if the proposed technique can identify an aged component in a live converter. The arrangement is shown in Figure 5.3, and the schematic of the converter circuit is shown in Figure 5.2. As there is no external trigger in the SSTDR hardware, the converter was operated at a very low switching frequency to make sure the measured SSTDR data were generated during the ON/OFF states of the switches. SSTDR data were recorded across each test pair during the following two states: (i) State I (S1 and S2 are turned ON, S3 and S4 are turned OFF); and (ii) State II (S3 and S4 are turned ON, S1 and S2 are turned OFF). The key objective of this test was to observe the peak SSTDR outputs across various components in a converter. There are four test points in this circuit (Figure 5.2), and SSTDR was applied in different combinations to map these four test points. A 5 V (RMS) 60 Hz AC input voltage was applied to the circuit, and the load resistance ($R_L$) was set to 5 Ω. The equivalent circuits of the H-bridge converter are shown in Figure 5.4 for both switching states, and the internal resistance $R_D$ of diodes D1, D2, D3 and D4 were considered equal for simplicity. Here, $R_S$ is the source's internal resistance,

ESR is the equivalent series resistance of the DC bus capacitor, and $R_{S1}$, $R_{S2}$, $R_{S3}$, and $R_{S4}$ are the ON resistances of MOSFETs S1, S2, S3 and S4, respectively.

SSTDR generates correlated outputs depending on the equivalent path impedances across the device under test. Therefore, it is necessary to calculate the equivalent path impedances across each possible test pair of the converter circuit. The MOSFET capacitances were neglected in calculating the equivalent path impedances as the capacitive impedances are very high at 24 MHz ~ 96 MHz compared to MOSFET $R_{DS\,(ON)}$. The ON resistances will be dominant when they are in parallel with MOSFET capacitances during the circuit's operating mode. ESR is always in parallel to the series combination of two diode resistances and the source resistance. If S1 and S2 are activated, the equivalent path impedance between test points one and two is the parallel combination of the two branches shown in Figure 5.5(b). As $R_{S1} << (R_{eq}+R_L+R_{S2})$, the equivalent path impedance can be approximated as $R_{S1}$ shown in Figure 5.5(c). Here, $R_{eq}$ is considered as equivalent to "$R_D + R_S + R_D \parallel ESR$." When S3 and S4 are activated, the equivalent path impedance between test nodes one and two is the series combination of $R_{eq}$ and $R_{S4}$ i.e. "$R_{eq} + R_{S4}$" (Figure 5.6). Similarly, the path impedance between one and three will be $R_{S3}$ or the series combination of $R_{S2}$ and $R_{eq}$.

The equivalent path impedance between nodes one and four is always $R_{eq}$ (Figure 5.7), and the equivalent path impedances between nodes two and three are "$R_{S1} + R_{eq} + R_{S2}$" or "$R_{S3} + R_{eq} + R_{S4}$" (Figure 5.8). All the equivalent path impedances between the test pairs have been derived and given in Table 5.1.

## 5.4 Formulating the reflection based impedance matrix for the H-bridge ac-ac converter

A reflection matrix has been constructed from the single phase H-bridge ac-ac converter shown in Figure 5.9. For i=1-4 and j=1-4, $A_{ij}$ represents peak SSTDR output across any two test points among these four nodes. As explained earlier, the SSTDR generated output is the true reflection of the equivalent path impedances of different test pairs given in Table 5.1. SSTDR generates negative output in short circuit conditions or in situations with extremely low impedances ($< z_0$ in equation 1), and it generates positive outputs in open circuit conditions or in cases of higher impedances ($> z_0$ in equation 1). From the equivalent path impedances given in Table 5.1, it is apparent that $A_{12}$ and $A_{34}$ will be the lowest during State I (when S1 and S2 are activated). Similarly, $A_{13}$ and $A_{24}$ will be the lowest during State II (when S3 and S4 are activated). However, $A_{14}$ and $A_{23}$ should be unaffected in both switching states.

A test case was created to observe the changes in matrix elements if one MOSFET is aged. Assuming, $R_{S1} = R_{S2} = R_{S3} = R_{s4} = 40$ mΩ, ESR = 33 mΩ, $R_L = 5$ Ω, the equivalent path impedances for each test pair were calculated using simulations in PSIM software. The reference impedance matrix was formed using these calculated values shown in Figure 5.10. The values of matrices shown in Figure 5.10 will eventually be changed as the converter ages. These variations could be incremental for normal aging or substantial for any failure. This matrix could be formed for any power converter, and a "Reference matrix" could be constructed from a nonaged power converter for comparison purpose. For example, if MOSFET S1 is aged, its $R_{DS\ (ON)}$ may increase to 50 mΩ, and these path impedances should be impacted accordingly. Using this new assumed value of $R_{S1}$ while

other values remain unchanged, a PSIM simulation was performed to calculate the path impedances. A matrix was formed using these path impedances and it is clearly observable that only few matrix elements changed due to aging of S1 (Figure 5.11). In this case, second row and second column are affected only during the state when S1 and S2 are activated and no changes were found during the state when S3 and S4 are activated. Therefore, it is possible to determine the aged component by observing the matrix elements. The location of the elements indicates which component is aged and the value of the elements indicates how much the component is aged.

The SSTDR generated outputs in both switching conditions with all new components (zero aging) are given in Figure 5.12. These two matrices will be used as reference matrices. It is of paramount importance to study how the impedance matrix changes when one or multiple components are aged in this ac-ac converter circuit. According to the analysis stated above, only the elements of the second row and the second column will be affected due to any aging in switch S1 during State I. However, no change is expected to be observed in matrix elements during State II due to the aging in S1. For analysis purpose, it is assumed that S1 has been aged and the corresponding modified matrix has been formed during State I, and it is given in Figure 5.13. This figure shows that the matrix element $A_{12}$ increases due to any aging in MOSFET S1, and $A_{13}$ should not be affected due to this aging. However, there may be some capacitive effect in the real circuit and $A_{13}$ may change due to any aging with S1.

A similar experiment was performed using IGBTs in the H-bridge converter circuit. Initially these matrices were formed using all new IGBTs, shown in Figure 5.14. After this test, one aged IGBT (G10) was used in place of S1, and the matrix was modified for State

I. From the matrix in Figure 5.15, the matrix element $A_{12}$ will have a lower value due to aging in IGBT S1. Similar to MOSFETs, $A_{13}$ changed due to the aging of S1. The experimental setup to characterize the ac-ac converter using SSTDR is shown in Figure 5.16.

## 5.5 Analysis of the experimental data: reverse synthesis method

In order to derive a reliability model of the converter under test, we need the aging information consistent with every component in the core converter circuit. The SSTDR hardware is a two terminal device that needs to be connected across the device under test such as any MOSFET, capacitor, IGBT and so on. The proposed solution applies SSTDR signal across various components in a power converter in order to detect the impedance degradation associated with those components. While doing so, the results associated with any component is influenced by all other components such as free-wheeling diodes, parasitic and source/load impedance connected in parallel to that aged component of interest. Therefore, we need a new algorithm that can de-embed the correlated output corresponding to only that affected component.

Section 5.4 has shown how to create the impedance matrix based on the SSTDR data. These impedances are simply the $R_{DS\ (ON)}$ of the corresponding MOSFETs while other components were connected across them during the taking of measurements. Therefore, we need to derive a new function to correlate the actual $R_{DS\ (ON)}$ and SSTDR data. Figure 5.17 shows the relationship between measured $R_{DS\ (ON)}$ and the corresponding correlated outputs. The $R_{DS\ (ON)}$ of these MOSFETs were calculated by simply measuring the voltage and current through the MOSFET while SSTDR was applied. The SSTDR frequency was

48 MHz, which is different from the SSTDR measurement done for characterizing isolated components. A curve fitting method was used to find the relationship between the SSTDR data and the corresponding $R_{DS\,(ON)}$, and this nonlinear function is given in equation (5.1). In this equation 'x' and 'y' represent correlated output and $R_{DS\,(ON)}$, respectively.

$$y = -4.747 \times 10^{5} - 58.905x - 0.0024344x^{2} - 3.3509x^{3} \times 10^{-8} \tag{5.1}$$

Using equation 5.1, the $R_{DS\,(ON)}$ corresponding to an aged S1 can be calculated while other components were connected across it. The correlated output, x is -23683 from Figure 5.13. Using this value, the $R_{DS\,(ON)}$ 'y' can be calculated as 44.2821 mΩ. The calculated $R_{DS\,(ON)}$ from the voltage and current measurement was found as 45.567 mΩ. Therefore the values of $R_{DS\,(ON)}$ calculated from SSTDR data and from the conventional voltage and current measurement are in good agreement.

As mentioned earlier, an impedance vector consistent with components under test needs to be derived from the impedance matrix. The number of elements in this vector should be the same as the number of aging affected components. In forward transform, an impedance matrix could be created from impedance vector, and this project thus needed the reverse transform. The forward transformation has been shown in Figure 5.18 for $i$=1-4 and $j$=1-4, X$ij$ represents the equivalent impedance between any two test points among the four different nodes. X$ij$ = 0 for $i$=$j$ because it would be a short circuit. Therefore, all the diagonal elements of this matrix are "0." In fact, there exist two impedance matrices for two different operating states of the converter, and these two matrices are shown in Figure 5.19. For simplification, it was assumed that impedance between nodes one and four

would be:

$$R_{eq} = ESRII(R_D + R_S + R_D) \approx ESR \tag{5.2}$$

Because of the nonlinearity and over deterministic nature of the system, it is not possible to inverse the operator and to determine the impedance vector from the impedance matrix. In order to identify the variation in impedances across node pairs, the new impedance vector needs to be consistently determined with the aged converter, and a comparison with the initial vector can be used to identify the level of aging associated with any particular component. Even if the impedance matrix and the operator are known, the process is not reversible because of its nonlinear nature.

Therefore, an error function was defined in MATLAB with the expression:

$$F = (X_{13} - X_{e\_13})^2 + (X_{24} - X_{e\_24})^2 \tag{5.3}$$

In order to verify whether the reverse synthesis method could reproduce the impedance vector with reasonable accuracy, a test case was created where both the impedance vector and the corresponding impedance matrix are known. The impedance vector was:

$$\begin{bmatrix} R_{DS1} \\ R_{DS2} \\ R_{DS3} \\ R_{DS4} \\ ESR \\ R_L \end{bmatrix} = \begin{bmatrix} 0.042 \\ 0.040 \\ 0.034 \\ 0.034 \\ 0.020 \\ 5 \end{bmatrix} \tag{5.4}$$

The affected components were $R_{DS1}$, $R_{DS2}$ and ESR. Due to the aging associated with these three components, the actual impedance matrix in State I looks like the matrix shown in Figure 5.20. Using the error function, an iterative program was executed in MATLAB, and $R_{DS1}$ was varied from 0.034Ω to 0.050 Ω with a 0.0005 Ω interval. The corresponding simulation results have been summarized in Figure 5.21 and Table 5.2. The error function becomes the smallest when $R_{DS1}$ is equal to 42mΩ, which is the correct solution, and this iterative solution can accurately reconstruct the impedance vector from the impedance matrix.

In real life, the SSTDR hardware will measure reflections at various node pairs and therefore, construct a matrix equivalent to the impedance matrix. By knowing the non-linear operator, the change in individual components could be identified using this process.

## 5.6 Reliability analysis of an H-bridge ac-ac converter

Reliability analysis of the H-bridge converter (shown in Figure 5.2) has been discussed in this section considering power MOSFETs are used as semiconductor switches S1, S2, S3 and S4. Various circuit parameters used in this experiment are given in Table 5.3. It was assumed that the $R_{DS\,(ON)}$ of the MOSFET S1 changed from 34 mΩ to 44 mΩ due to natural aging (which is consistent with the experimental results summarized in Table 4.2 and Table 4.3). Although in real converters all the components will age naturally with time, only one of the MOSFET's aging has been considered to simplify the analysis. The circuit was simulated in Powersim (PSIM) using the parameters given in Table 5.3. It was assumed that the circuit is operating in open loop condition.

Considering a constant failure rate, reliability of the system can be calculated as

$$R_S(t) = e^{(-\lambda_{SYSTEM} \times t)} \text{ [57]} \tag{5.5}$$

Here, $R_S(t)$ is the probability that the system will not fail within time $t$ and $\lambda_{SYSTEM}$ is the failure rate of the system. The mean-time-to-failure MTTF can be calculated from the reliability of the system using the equation 5.6:

$$MTTF = \int_0^\infty R_S(t)dt = \frac{1}{\lambda_{SYSTEM}} \tag{5.6}$$

Failure rate of an *N*-channel MOSFET can be written as,

$$\lambda_{SW} = \lambda_B \pi_T \pi_A \pi_E \pi_Q \text{ [58] [59]} \tag{5.7}$$

The base failure rate $\lambda_B$ is constant and equal to 0.012. The application and quality factors $\pi_A$ and $\pi_Q$ are 8 (for switches rated at 135 W). Environment factor $\pi_E$ is considered as 9 for equipment installed on wheeled or tracked vehicles. Temperature factor and junction temperature can be calculated using equations 5.8 and 5.9.

$$\pi_T = \text{temperature factor} = \exp\left[-1925\left\{\left(\frac{1}{T_j + 273}\right) - \frac{1}{298}\right\}\right] \tag{5.8}$$

$$T_j = T_a + (\theta_{ja})P_{SW} \tag{5.9}$$

Ambient temperature, $T_a$ is 25° C and junction to ambient thermal resistance $\theta_{ja}$ is 62 °C/W (based on the datasheet of different TO-220 package MOSFETS). The total power dissipation (conduction loss + switching loss) of the switching device is $P_{SW}$. Therefore, considering the values stated above in equation 5.10:

$$\lambda_{SW} = \lambda_B \pi_T \pi_A \pi_E \pi_Q = 0012 \times \pi_T \times 8 \times 9 \times 8 = 6.912 \times \pi_T \tag{5.10}$$

The power loss (conduction loss + switching loss) was calculated to be 0.2972 watt in a power MOSFET from simulation when the $R_{DS\,(ON)}$ is 0.034 Ω.

$$T_j = T_a + (\theta_{ja}) P_{SW} = 25 + (62 \times 0.2972) = 43.4264 \tag{5.11}$$

$$\pi_t = \exp\left[-1925\left\{\left(\frac{1}{T_j + 273}\right) - \frac{1}{298}\right\}\right] = 1.4567 \tag{5.12}$$

$$\lambda_{SW} = 6.912 \times 1.4567 = 10.068 \text{ failures/million-hours} \tag{5.13}$$

Failure rate of a diode can be written as:

$$\lambda_{DIODE} = \lambda_B \pi_T \pi_S \pi_C \pi_E \pi_Q \text{ [58] [59]} \tag{5.14}$$

The base failure rate $\lambda_B$ is 0.003 for schottky devices. The stress factor $\pi_S$ accounts for the operational reverse-voltage stress of the diode relative to the rated voltage. Considering $V_{OUT} / V_{RATED-DIODE} \leq 0.3$, stress factor $\pi_S$ is 0.054. The effect of the diode's physical contact with the printed circuit board is denoted by the contact construction factor $\pi_C$, and this is unity for metallurgical bonded contacts. Quality and environment factors (for equipment installed on wheeled or tracked vehicles) $\pi_Q$ and $\pi_E$ are 8 and 9, respectively. Temperature factor can be calculated as equation 5.15:

$$\pi_T = \text{temperature factor} = \exp\left[-3091\left\{\left(\frac{1}{T_j + 273}\right) - \frac{1}{298}\right\}\right] \tag{5.15}$$

$T_j$ is the junction temperature and it is computed in the same manner as was done for MOSFET. Power loss in a diode is considered to be 2.3935 watt from simulation.

$$T_j = T_a + (\theta_{ja}) P_{diode} = 25 + (50 \times 2.3935) = 144.675 \tag{5.16}$$

$$\pi_t = \exp\left[-3091\left\{\left(\frac{1}{T_j + 273}\right) - \frac{1}{298}\right\}\right] = 19.5308 \tag{5.17}$$

Therefore, considering the values stated above,

$$\lambda_{DIODE} = \lambda_B \pi_T \pi_S \pi_C \pi_E \pi_Q$$

$$= 0.003 \times 19.5308 \times 0.054 \times 1 \times 9 \times 8 = 0.2278 \text{ failures/million-hours} \qquad (5.18)$$

The failure rate of DC aluminum or dry electrolyte polarized capacitor can be expressed as equation 5.19:

$$\lambda_{CAP} = \lambda_B \pi_{CV} \pi_E \pi_Q \text{ [58] [59]} \qquad (5.19)$$

$$\lambda_B = \text{base failure rate} = 0.0028 \times \left[ \left( \frac{S_{CAP}}{0.55} \right)^3 + 1 \right] \exp \left[ 4.09 \times \left( \frac{T + 273}{358} \right)^{5.9} \right] \qquad (5.20)$$

$$S_{CAP} = \frac{V_{OUT} + (\Delta V_{OUT} / 2)}{V_{RATED-CAP}} \qquad (5.21)$$

$$\pi_{CV} = 0.32(C\mu F)^{0.19} \qquad (5.22)$$

The operational voltage stress $S_{CAP}$ is defined as the ratio of the peak-to-rated capacitor voltage. The capacitance factor $\pi_{CV}$ denotes the failure rate based on the value of capacitance in microfarad. Finally, $\pi_E$ and $\pi_Q$ are 2 and 10, respectively, for equipment installed on wheeled or tracked vehicles. A capacitor with 4700 μF capacitance was used for 100V output. The rated voltage was 200V and p-p ripple voltage was 5.11926 V.

Considering the values stated above,

$$S_{CAP} = \frac{V_{OUT} + (\Delta V_{OUT} / 2)}{V_{RATED-CAP}} = \frac{100 + (5.11926/2)}{200} = 0.512798 \tag{5.23}$$

$$\lambda_B = 0.0028 \times \left[ \left( \frac{S_{CAP}}{0.55} \right)^3 + 1 \right] \exp\left[ 4.09 \times \left( \frac{T + 273}{358} \right)^{5.9} \right]$$

$$= 0.0028 \times 1.8105 \times 3.9978 = 0.020266 \tag{5.24}$$

$$\pi_{CV} = 0.32(C\mu F)^{0.19} == 0.32(4700)^{0.19} = 1.5953 \tag{5.25}$$

$$\lambda_{CAP} = \lambda_B \pi_{CV} \pi_E \pi_Q = 0.020266 \times 1.5953 \times 12 \times 10$$

$$= 3.8797 \text{ failures/million-hours} \tag{5.26}$$

The H-bridge converter circuit shown in Figure 5.2 does not have any redundant component and requires zero failures for proper operation. Therefore, the failure rate of the converter can be calculated as:

$$\lambda_{SYSTEM} = 4 \times \lambda_{SW} + \lambda_{CAP} + 4 \times \lambda_{DIODE} \tag{5.27}$$

Using the calculated failure rates of active switches, diodes and capacitors,

$$\lambda_{SYSTEM} = 4 \times \lambda_{SW} + \lambda_{CAP} + 4 \times \lambda_{DIODE}$$

$$= 4 \times 10.068 + 3.8797 + 4 \times 0.2278$$

$$= 45.0629 \text{ failures/million-hours} \tag{5.28}$$

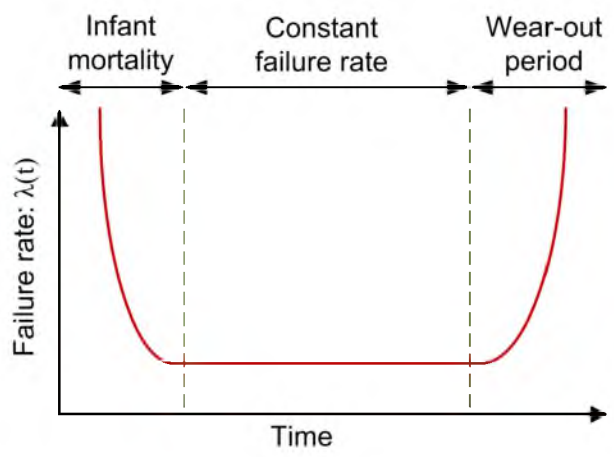
Therefore,

$$MTTF = \frac{1}{\lambda_{SYSTEM}} = \frac{10^6}{45.0629} = 22191.2 \text{ hours/failure}$$

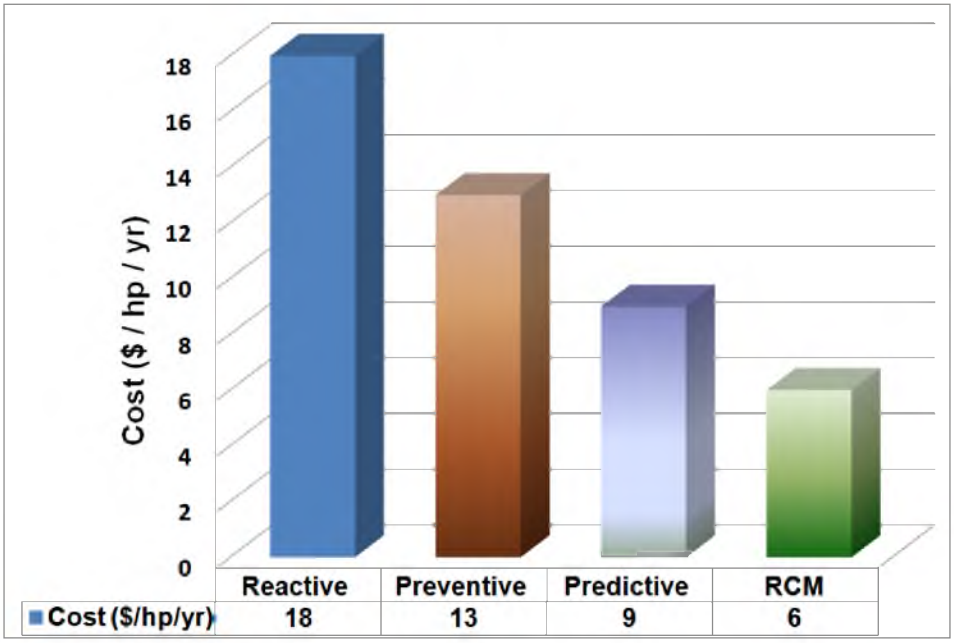
$$= 2.533 \text{ years/failure} \quad (5.29)$$

A MATLAB script based on the analysis presented above was executed to estimate the converter's failure rate and MTTF as a function of aging in the MOSFET, and the obtained results have been summarized in Figure 5.22. The power loss associated with the MOSFET will eventually increase due to aging in MOSFET S1, and that has been demonstrated in Figure 5.22(a). Figure 5.22(b) shows that the MOSFET failure rate will significantly increase if $R_{DS\,(ON)}$ continues to increase, and Figure 5.22(c) demonstrates that converter reliability can be expressed as a function of MOSFET $R_{DS\,(ON)}$. The MTTF can vary from 2.541 to 2.473 for a variation in $R_{DS\,(ON)}$ from 0.034-0.044 Ω. The MTTF of the converter would be even lower if aging in other components in the circuit are considered. For simplicity, only the aging associated with one MOSFET has been considered in the MATLAB script.

$R_{DS\,(ON)}$ of S1 prior to accelerated aging was measured to be 35.64 mΩ from the voltage and current through the MOSFET, and the calculated $R_{DS\,(ON)}$ (=45.567 mΩ) obtained from the SSTDR data was nearly in very good agreement (=44.2821 mΩ). Therefore the actual MTTF of the H-bridge ac-ac converter can be approximated from the calculated $R_{DS\,(ON)}$ using the SSTDR generated data.




(a)




(b)

Figure 5.1: Reliability analysis (a) bathtub curve for component failure rate; (b) cost analysis for different schemes applied to electric pumps (adapted from [55] [56]).

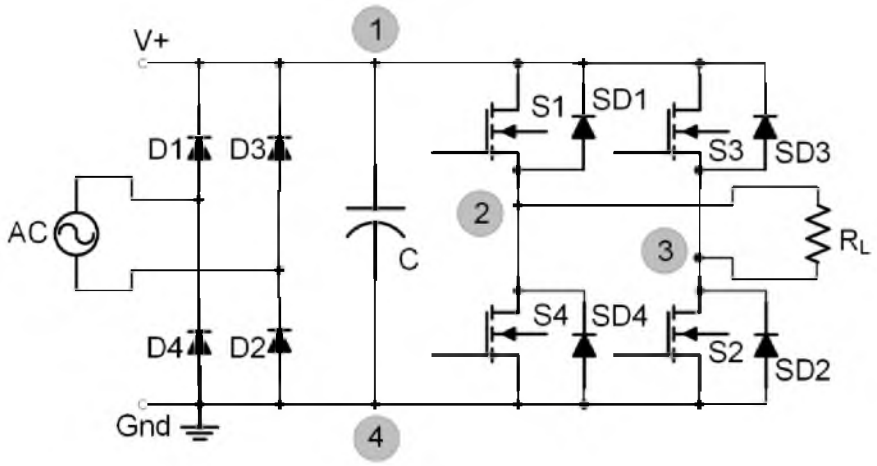



Figure 5.2: Schematic of the H-bridge ac-ac converter showing the SSTDR test points.

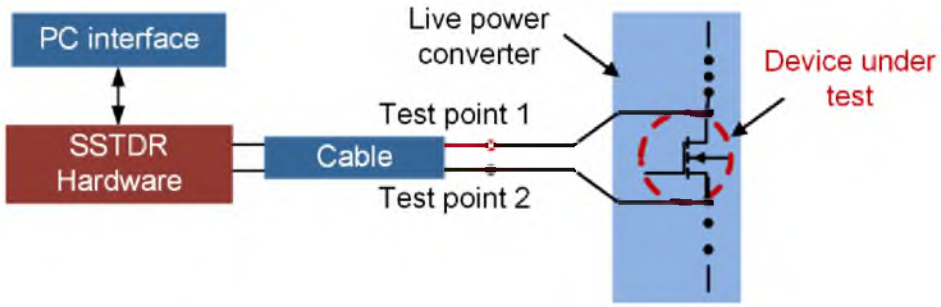



Figure 5.3: Schematic of the test setup showing the applied SSTDR to the device under test while the device is connected in a converter circuit.

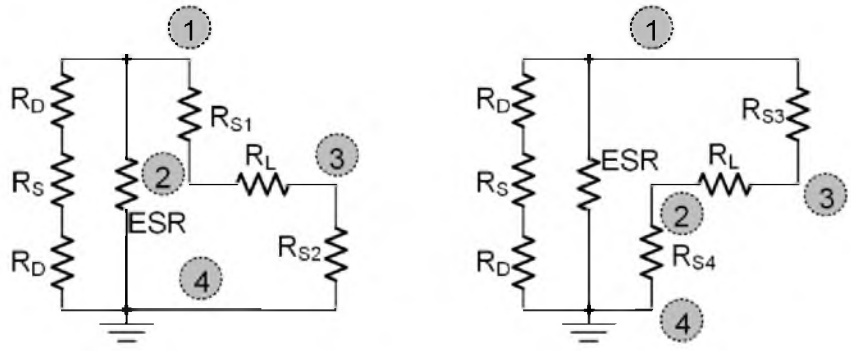



Figure 5.4: Equivalent circuit of the H-bridge ac-ac converter (shown in Figure 5.2) during both switching states. (a) S1 and S2 are activated; (b) S3 and S4 are activated.

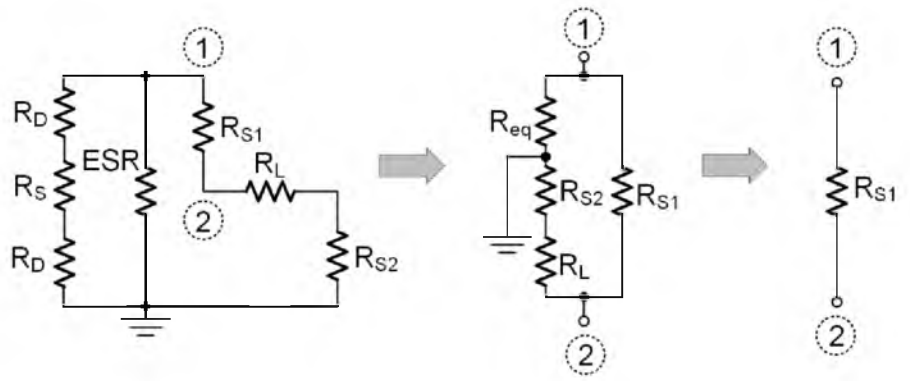



Figure 5.5. Equivalent path impedances between test nodes 1 and 2 when S1 and S2 are activated.

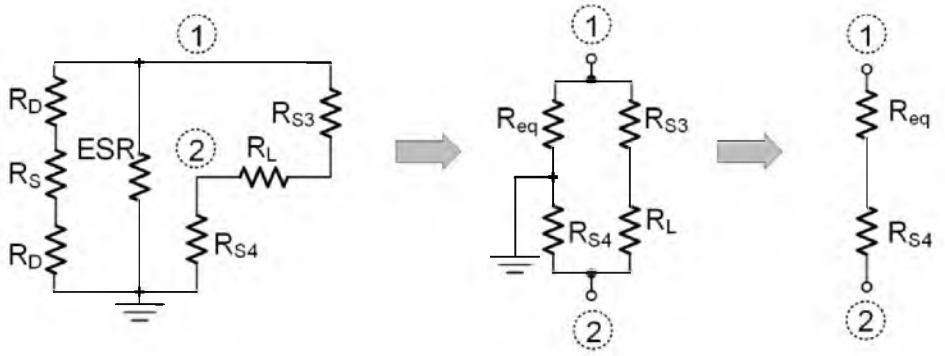
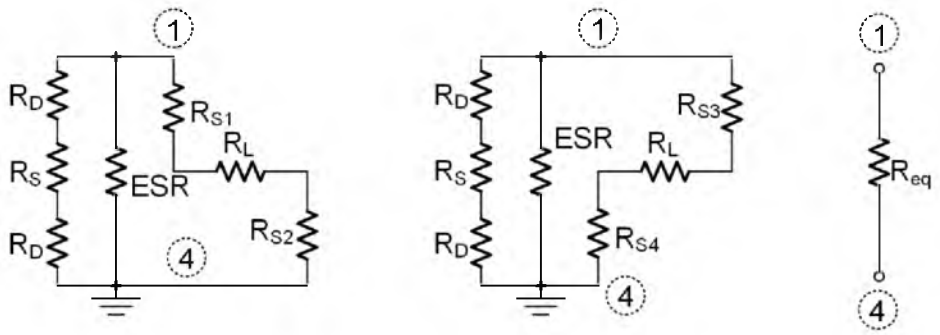
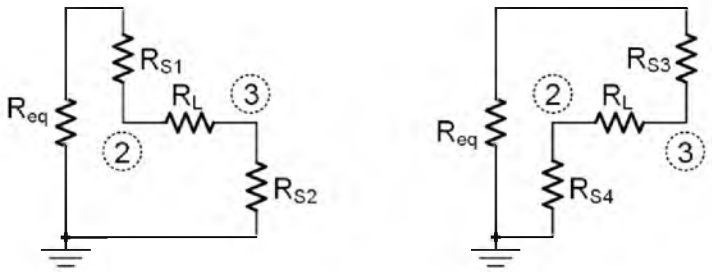



Figure 5.6. Equivalent path impedances between test nodes 1 and 2 when S3 and S4 are activated.




(a) (b) (c)

Figure 5.7. Equivalent path impedances between test nodes 1 and 4 for both switching states; (a) S1 and S2 are activated; (b) S3 and S4 are activated; (c) calculated equivalent path impedance in any of the switching states.




(a) (b)

Figure 5.8. Equivalent path impedances between test nodes 2 and 3 for both switching states; (a) S1 and S2 are activated; (b) S3 and S4 are activated.

$$A=\begin{pmatrix} A_{11} & A_{12} & A_{13} & A_{14} \\ A_{21} & A_{22} & A_{23} & A_{24} \\ A_{31} & A_{32} & A_{33} & A_{34} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{pmatrix}$$

Figure 5.9: The generic form of the impedance matrix created using the SSTDR technique applied to the H-bridge ac-ac converter.

**When S1, S2 are "ON" and S3, S4 are "OFF"**

$$\text{Reference A} = \begin{pmatrix} 0 & 39.6871 & 71.9578 & 32.787 \\ 39.6871 & 0 & 110.502 & 71.9578 \\ 71.9578 & 110.502 & 0 & 39.6871 \\ 32.787 & 71.9578 & 39.6871 & 0 \end{pmatrix}$$

**When S1, S2 are "OFF" and S3, S4 are "ON"**

$$\text{Reference A} = \begin{pmatrix} 0 & 71.9578 & 39.6871 & 32.787 \\ 71.9571 & 0 & 110.502 & 39.687 \\ 39.687 & 110.502 & 0 & 71.9578 \\ 32.787 & 39.6871 & 71.9578 & 0 \end{pmatrix}$$

Figure 5.10: Reference impedance matrix.

**When S1, S2 are "ON" and S3, S4 are "OFF"**

$$\text{Only S1 aged, A} = \begin{pmatrix} 0 & \mathbf{49.5120} & 71.9598 & 32.7874 \\ \mathbf{49.5120} & 0 & \mathbf{120.0468} & \mathbf{81.6553} \\ 71.9578 & \mathbf{120.0468} & 0 & 39.6877 \\ 32.7874 & \mathbf{81.6553} & 39.6877 & 0 \end{pmatrix}$$

**When S1, S2 are "OFF" and S3, S4 are "ON"**

$$\text{Only S1 aged, A} = \begin{pmatrix} 0 & 71.9578 & 39.6871 & 32.787 \\ 71.9571 & 0 & 110.502 & 39.687 \\ 39.687 & 110.502 & 0 & 71.9578 \\ 32.787 & 39.6871 & 71.9578 & 0 \end{pmatrix}$$

Figure 5.11: Impedance matrix assuming S1 is aged. The impedances that are changed due to aging of S1 are indicated in bold and red.

**When S1, S2 are "ON" and S3, S4 are "OFF"**

$$\text{Reference,A} = \begin{pmatrix} -24672 & -23793 & -21560 & -24083 \\ -23793 & -24672 & -21234 & -21366 \\ -21560 & -21234 & -24672 & -23538 \\ -24083 & -21366 & -23538 & -24672 \end{pmatrix}$$

**When S1, S2 are "OFF" and S3, S4 are "ON"**

$$\text{Reference,A} = \begin{pmatrix} -24672 & -21444 & -23711 & -23849 \\ -21444 & -24672 & -21202 & -23779 \\ -23711 & -21202 & -24672 & -21390 \\ -23849 & -23779 & -21390 & -24672 \end{pmatrix}$$

Figure 5.12: Impedance matrix created from SSTDR generated output with all new MOSFETs (M6, M7, M8, and M9), dc bus capacitor and diodes in an H-bridge ac-ac converter circuit during both switching states.

$$A = \begin{pmatrix} -24672 & \mathbf{-23683} & -21415 & -24044 \\ \mathbf{-23683} & -24672 & \mathbf{-21041} & \mathbf{-21209} \\ -21415 & \mathbf{-21041} & -24672 & -23506 \\ -24044 & \mathbf{-21209} & -23506 & -24672 \end{pmatrix}$$

Figure 5.13: Matrix built from SSTDR generated peak output of the H-bridge ac-ac converter while S1 was replaced by an aged MOSFET during State I.

**When S1, S2 are "ON" and S3, S4 are "OFF"**

$$\text{Reference, } A = \begin{pmatrix} -24672 & -24279 & -20860 & -23507 \\ -24279 & -24672 & -16337 & -20273 \\ -20860 & -16337 & -24672 & -24045 \\ -23507 & -20273 & -24045 & -24672 \end{pmatrix}$$

**When S1, S2 are "OFF" and S3, S4 are "ON"**

$$\text{Reference, } A = \begin{pmatrix} -24672 & -20425 & -24105 & -23570 \\ -20425 & -24672 & -15853 & -24787 \\ -24105 & -15853 & -24672 & -20532 \\ -23570 & -24787 & -20532 & -24672 \end{pmatrix}$$

Figure 5.14: Impedance matrix created from SSTDR generated peak output with all new IGBTs (G5, G6, G7, and G8), dc bus capacitor and diodes in an H-bridge ac-ac converter circuit during both switching states.

$$A = \begin{pmatrix} -24672 & \mathbf{-24497} & -20708 & -23615 \\ \mathbf{-24497} & -24672 & \mathbf{-16080} & \mathbf{-20419} \\ -20708 & \mathbf{-16080} & -24672 & -24021 \\ -23615 & \mathbf{-20419} & -24021 & -24672 \end{pmatrix}$$

Figure 5.15: Matrix built from SSTDR generated peak output of the H-bridge ac-ac converter while S1 was replaced by an aged IGBT during State I.


Figure 5.16: Experimental SSTDR setup to generate the impedance matrix for the H-bridge ac-ac converter.

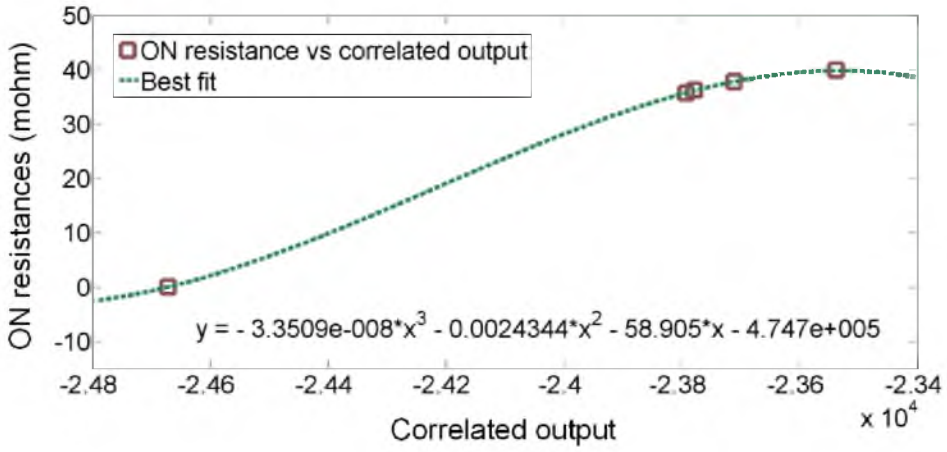



Figure 5.17: Deriving the relationship between the correlated output and $R_{DS\,(ON)}$ at the MOSFETs used in the H-bridge ac-ac converter.

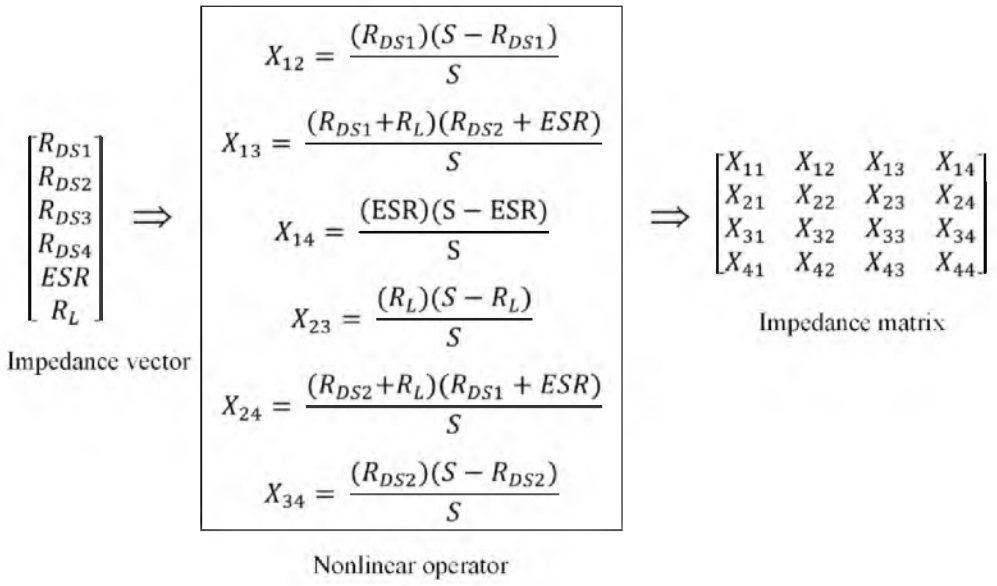



Figure 5.18: System transform model to obtain the impedance matrix from the impedance vector. Here, [$S = R_{DS1} + R_{DS2} + ESR + R_L$].

$$A_{\text{State I}} = \begin{pmatrix} 0 & 0.03377 & 0.05048 & 0.01694 \\ 0.03377 & 0 & 0.08357 & 0.05048 \\ 0.05048 & 0.08357 & 0 & 0.03377 \\ 0.01694 & 0.05048 & 0.03377 & 0 \end{pmatrix}$$

(a)

$$A_{\text{State II}} = \begin{pmatrix} 0 & 0.05048 & 0.03377 & 0.01694 \\ 0.05048 & 0 & 0.08357 & 0.03377 \\ 0.03377 & 0.08357 & 0 & 0.05048 \\ 0.01694 & 0.03377 & 0.05048 & 0 \end{pmatrix}$$

(b)

Figure 5.19: Impedance matrices for the power converter created from the original impedance vector shown in equation 5.4 during (a) State I; (b) State II.

$$A = \begin{bmatrix} 0 & 0.04165 & 0.05929 & 0.01992 \\ 0.04165 & 0 & 0.09996 & 0.06125 \\ 0.05929 & 0.09996 & 0 & 0.03968 \\ 0.01992 & 0.06125 & 0.03968 & 0 \end{bmatrix}$$

Figure 5.20: Modified impedance matrix during State I due to aging with $R_{DS1}$, $R_{DS2}$ and ESR.

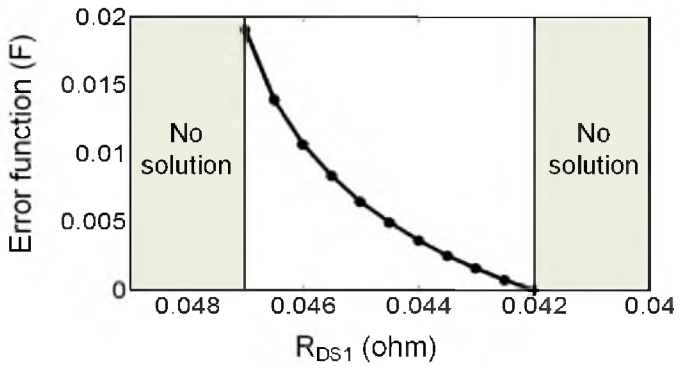



Figure 5.21: The variation in the error function as a function of $R_{DS1}$. The solution produces imaginary results for $0.042>R_{DS1}>0.047$.

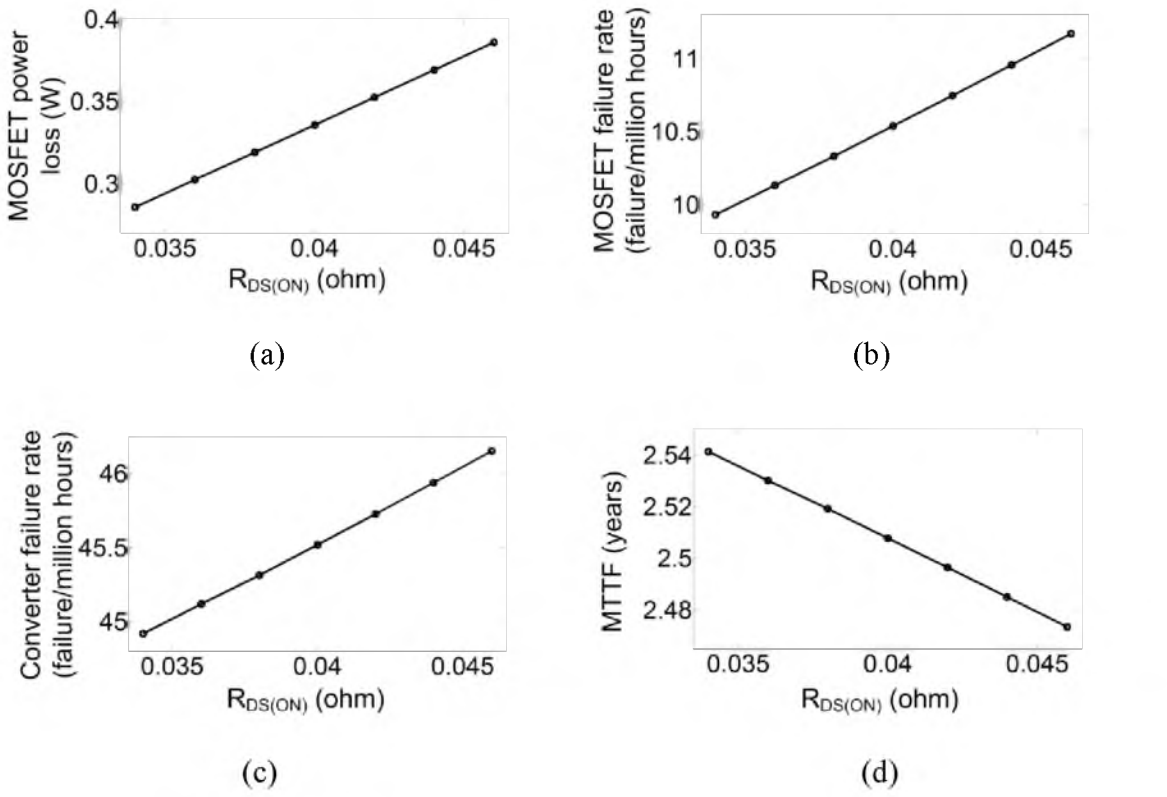



Figure 5.22: Analytically computed reliability and failure analysis results for the H-bridge ac-ac converter (a) variation in MOSFET power loss; (b) MOSFET failure rate; (c) converter failure rate; and (d) mean time to failure (MTTF) of the entire converter as a function of $R_{DS\,(ON)}$.

Table 5.1: Equivalent path impedances across node pairs in an H-bridge ac-ac converter circuit during both switching states.

| Test point | 1 and 2 | 1 and 3 | 1 and 4 | 2 and 3 | 2 and 4 | 3 and 4 |
|---|---|---|---|---|---|---|
| S1 and S2 are "ON" | $R_{S1}$ | $R_{eq}+R_{S2}$ | $R_{eq}$ | $R_{S1}+R_{eq}+R_{S2}$ | $R_{eq}+R_{S1}$ | $R_{S2}$ |
| S3 and S4 are "ON" | $R_{eq}+R_{S4}$ | $R_{S3}$ | $R_{eq}$ | $R_{S3}+R_{eq}+R_{S4}$ | $R_{S4}$ | $R_{eq}+R_{S3}$ |

Table 5.2: Simulation results showing the converging steps used to identify the drifted $R_{DS1}$.

| $R_{DS1}$ (Ω) | $R_{DS2}$ (Ω) | $R_L$ (Ω) | ESR (Ω) |
|---|---|---|---|
| 0.04700 | 0.04447 | 0.24379 | 0.02099 |
| 0.04650 | 0.04403 | 0.29503 | 0.02090 |
| 0.04600 | 0.04359 | 0.34641 | 0.02081 |
| 0.04550 | 0.04314 | 0.40568 | 0.02072 |
| 0.04500 | 0.04270 | 0.47892 | 0.02062 |
| 0.04450 | 0.04225 | 0.57486 | 0.02053 |
| 0.04400 | 0.04180 | 0.70895 | 0.02043 |
| 0.04350 | 0.04135 | 0.91294 | 0.02032 |
| 0.04300 | 0.04090 | 1.26542 | 0.02022 |
| 0.04250 | 0.04045 | 2.03055 | 0.02011 |
| 0.04200 | 0.04000 | 5.00000 | 0.02000 |

Table 5.3: Electrical parameters of the components used in the H-bridge ac-ac converter.

| Symbol | Description | Value |
|---|---|---|
| $V_{in}$ | AC Input voltage | 80 V (RMS) |
| $V_{out}$ | Output voltage | 100 V |
| $r_{sw}$ | MOSFET $R_{DS\,(ON)}$ | 0.034 - 0.044 |
| $r_D$ | Diode on resistance | 0.03 Ω |
| $V_f$ | Diode forward voltage | 0.7 V |
| $C$ | Output capacitance | 4700 μF |
| $V_{RATED\text{-}CAP}$ | Rated voltage of capacitor | 200 V |
| $r_C$ | ESR of the capacitor | 0.017Ω |
| $R_L$ | Load resistance | 35 Ω |

# CHAPTER 6

## CONCLUSIONS AND FUTURE WORK

A nonintrusive measurement technique to estimate the state of health of power converters has been described in this paper. MOSFETs and IGBTs were aged using both power and thermal stress and electrolytic capacitors were aged using thermal stress in a controlled environment. SSTDR was applied to identify the aged and damaged devices while the devices were connected in an operational circuit. It was found that SSTDR can detect any degradation as well as any fault in active switches and capacitors. SSTDR was applied in a single phase ac-ac converter across different test point pairs and corresponding peak SSTDR outputs were obtained. Matrices were formed using these SSTDR generated data for all new MOSFETs/IGBTs in the converter circuit. In addition, SSTDR data were generated to investigate the effect of aging and damage of one single MOSFET/IGBT in the circuit. Matrices were formed using these SSTDR generated peak data as well where one single MOSFET/IGBT was aged or damaged. Comparing the matrix elements with the reference matrix, where all the elements are new, it is possible to identify which components are aged and the level of aging. Using the correlation between the SSTDR data and actual impedance, the equivalent impedances among various test nodes could be predicted. Therefore, the proposed technique could be considered as a landmark in

predicting the state of health of live power converters by knowing the degradation associated with individual components. The present research from the University of Utah power engineering and automation research lab (PEARL) team indicates that this technique could be used to conduct diagnostics and prognostics for many other elements of power electronics such as solar cells, batteries, transformer, electric motors, and so on.

As future work, we recommend hardware modification in the existing SSTDR set up. The present SSTDR hardware is suitable to detect aged semiconductor switches if the switching frequency is very low. However, for high frequency operation (hundreds of hertz or more) of the converter, the present SSTDR hardware is unable to locate the aged semiconductor switch due to the lack of synchronization. In addition to the synchronization between converter and SSTDR system, hardware resolution needs to be improved as well to detect impedance discontinuity in very close proximity, such as a few millimeters. The modified system should be capable of detecting impedance variation as small as 1 mΩ. This is required to detect aging level in MOSFETs with extremely low $R_{DS\,(ON)}$. Therefore, both synchronization and resolution improvement are equally important for future reliability analysis of power converters using SSTDR.

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