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# IMPROVED DATA TRANSMISSION VIA INDUCTIVE LINK FOR NEURAL RECORDING DEVICES

by

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A thesis submitted to the faculty of
The University of Utah
in partial fulfillment of the requirements for the degree of

Master of Science

Department of Electrical and Computer Engineering

The University of Utah

August 2011

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**The University of Utah Graduate School**

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# ABSTRACT

Fully integrated, implantable, and wireless neural interface systems typically require a forward data link in addition to the telemetry link that transmits data from the chip. One popular way to create this forward data link is to amplitude modulate the magnetic field of the inductive link that provides the device with wireless power. However, the limitations of these channels when loaded with a rectifier and amplitude modulated have not previously been characterized, and this lack of understanding caused previous versions of the Integrated Neural Interface (INI) to have forward data communication issues, which needed to be corrected for the next generation of the device, INIR8. This thesis first develops an analytical method of characterizing this sort of wireless channel. It then shows measurement data that verifies the validity of the model in the desired region of operation. The available bandwidth as determined by this analytical method, and confirmed by simulation, is insufficient for many applications. Therefore, the next subject of this thesis is to increase the data rate beyond what the bandwidth of the system can intrinsically support by using an equalization technique. This technique is shown to support very robust data recovery under a variety of operating conditions and to data rates much higher than otherwise possible. Another way to improve the reliability of data recovery is to develop a robust digital control system with error detection capabilities. This was done for INIR8, and works very reliably. The end result of this effort is a very robust forward data communication in INIR8, as well as a new analytical method for characterizing inductively coupled channels with certain loads and modulation techniques.

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## ACKNOWLEDGEMENTS

I would first like to thank my adviser, Reid Harrison, for his support and patience as I asked innumerable questions. The immense amount of knowledge I have gained during this process is primarily due to his influence. Also I thank those who supported me in testing: Dave Warren for his extensive support in testing and developing the MATLAB code for the INIR8, and Asha Sharma who answered many questions, especially when I was new to the project. I would also like to thank the rest of my committee, Darrin Young and Bradley Greger, for their support and encouragement. Finally, I would like to thank my parents for instilling in me the value and importance of education, and for their support of my undergraduate studies.

# CHAPTER 1

# INTRODUCTION

The study of devices that interface with the brain and nervous system is quickly becoming one of the most important topics in electrical engineering. These devices can be used for a variety of purposes, from the diagnosis of diseases, to exploratory neuroscience research, to the development of brain-machine interfaces that will allow unresponsive or prosthetic limbs to function by observing the neural activity in certain parts of the brain.

In order to observe and stimulate neural activity while limiting the risk of infection in study subjects, it is important to develop neural recording systems that can be surgically implanted without the need for transcutaneous wires. It is also desirable to have a large number of electrodes, such as the Utah Electrode Array (UEA) shown in Fig. 1.1, that simultaneously record neural activity [1]. Achieving these goals is a very complex task that has been the focus of significant research in universities around the world in the past decade.

The Integrated Neural Interface (INI) project is one attempt at solving this problem. The INI is a fully wireless system that sends and receives all power and data signals wirelessly, and without a battery (see Fig. 1.2). In achieving this goal, the device must perform amplification and signal processing on-chip, and then wirelessly transmit the data off-chip. Additionally, the device must be wirelessly powered and forward control data must also somehow be wirelessly transmitted. All of these must be done without effecting damage to the surrounding tissue, so stringent power requirements must be obeyed.

The developed integrated circuit is then is flip-chip bonded to a 100-electrode UEA and requires only three additional off-chip components, namely a coil to receive power and data via inductive coupling, a resonating capacitor used to increase the coupling

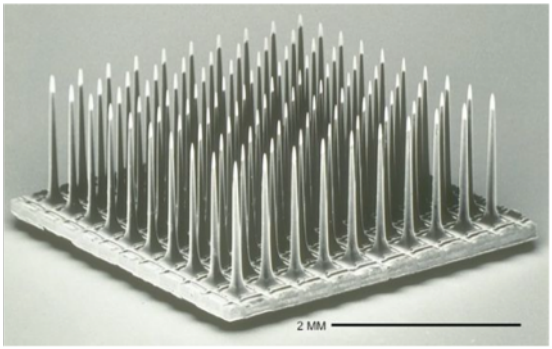


**Figure 1.1**. SEM Image of the Utah Electrode Array.

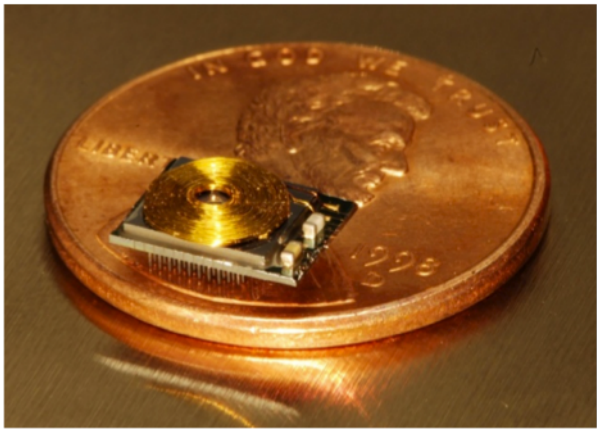

**Figure 1.2**. A fully-integrated INI device.

efficiency of the power transfer, and a smoothing capacitor to be used with the rectifier circuit. The small form factor that results from this high level of integration is ideal for implantation in the body.

Four fundamental components must be wirelessly transmitted and received: forward control data, reverse telemetry data, power, and a clock signal, to be used by the digital electronics. This thesis concerns itself with the reliable transmission of control data via modulation of the inductive link used for power transmission. This method is desirable because it simplifies implant design. The power receive coil serves dual purposes for both power and data recovery, eliminating the need for an additional antenna. There is little power expended in signal recovery, since the envelope of the modulation is recovered automatically by the chip's voltage rectifier when amplitude

modulation (AM) is utilized.

The use of inductive links for wireless power and data transmission has been a significant worldwide research effort, and some of that research will be discussed in Section 1.1. The current state of the INI project, especially that concerned with forward data transmission and the issues that it currently has will be discussed in Section 1.2. The reliable transmission of control data has been a serious problem in the INI project, and the primary purpose of this thesis is to address these issues. Section 1.3 will discuss how this thesis plans to address these issues.

## 1.1 Review of Inductive Link Technology

One of the primary methods of generating power wirelessly is the use of two magnetically coupled inductors. On one end, a power amplifier generates an oscillating sinusoidal waveform across one of the inductors. This amplifier is typically a Class-E power amplifier [2]. This amplifier configuration has efficiency approaching 100% for well designed amplifiers, because the current and voltage waveforms are nonzero only half of the period and can be offset by 180°.

The inductor that receives power is magnetically coupled to the transmitting inductor that is part of the Class-E amplifier. The transmitting inductor is typically large, but the receiving coil is typically quite small so that it can be surgically implanted. As a result, the coupling coefficients of these amplifiers are usually low, and a large voltage must appear across the transmitting coil. This occurs naturally in a Class-E amplifier, since the amplifier always drives a high-$Q$ $LC$ tank circuit in order to produce a robust sinusoid. This type of configuration is seen in [3, 4, 5].

Although the Class-E power amplifier is desirable due to its high efficiency operation, one of the major drawbacks is the vulnerability to variations in inductor and capacitor value, since it relies on a large resonant peak to achieve high efficiency. This is especially troublesome because they inductor value can vary with environmental factors, such as nearby metal objects. As a result, there have been efforts to implement a closed-loop system to compensate for variability in capacitor and inductor values [6, 7, 8], typically by varying the carrier frequency to ensure it is always at the peak

of resonance.

It is also common to transmit data using the inductive link. By modulating the power carrier in some fashion, data can be transmitted to the device with low overhead. Modulation has been done in a variety of ways, most commonly using some form of amplitude-shift keying (ASK) or frequency-shift keying (FSK). Amplitude-shift keying has historically been the primary means of data transmission across inductive links. This is primarily due to the ease of implementation for both the transmitter and receiver [9, 10, 11]. Frequency-shift keying the magnetic field is an alternative to ASK, and has two primary advantages. First, it does not suffer from the smoothing capacitor charging effects that are the subject of Chapter 2 of this thesis, and it also is more robust against noise and interference [12, 13].

All of the previously mentioned literature discusses the use of a single inductive link to transmit both power and data, but more recent research has begun to explore the possibilities of using multiple carriers by utilizing multiple carriers. In [14, 15], two inductors are used to recover power and data links at different frequencies. They are placed orthogonally to minimize the interference between the two coils. In both cases, the power transmission coil is placed in the traditional configuration to receive the maximum magnetic field, and an additional coil is wrapped around the transmit coil, where both the transmit and receive data coils are in the same plane.

A third use of the multiple carrier technique is seen in [16]. Instead of using geometric alignment to eliminate interference between the power and data band, Zhao et al. have both transmit and receive coils geometrically coaxial, and utilize a differential phase-shift keying (DPSK) demodulation technique to cancel interference between the two coils.

A fourth use of the multiple carrier technique is presented in [17]. Simard et. al. choose to use a coplanar technique, where the coils are in the same plane but are not coaxial. Data is modulated using offset quadrature phase-shift keying (OQPSK) to achieve very high data rates (4.16 Mb/s) with low bit error rates ($2 \times 10^{-6}$). They also include a coplanar back-telemetry link, making the system bidirectional.

## 1.2 INI Project Previous Work

The INI project is an attempt to develop fully integrated neural recording and stimulation devices that can be flip-chip bonded to a Utah Electrode Array. The first two attempts at developing this system were the INI1 and INI2 devices, documented in [18]. These devices had issues with digital interference and required several off chip components, so a second major revision, INI3, was developed as discussed in [19]. Since that time, several minor revisions have been made, and the newest attempt is INIR8, which has been redesigned for the 0.35 $\mu$m process and contains the changes indicated in this thesis.

One of the primary issues that still plagues the INI devices is the reliable wireless transmission of forward control data. Existing devices up to INIR7 have seen significant problems for two reasons.

First, the wireless data is transmitted via ASK, and there were significant data attenuation issues due to a lack of complete understanding of channel behavior. The result was that square wave modulation of the power signal resulted in a received triangle wave modulation. This, in combination with noise and small dc offsets caused the device to recover data unreliably because the transitions between high and low modulation were unreliably recovered. One attempt was made to reduce this problem by changing the waveform of the ASK envelope. By creating a large initial voltage at the beginning of the amplitude shift, modest improvements in performance were seen. However, it was still clear that a better solution was needed.

The other issue with transmission of control data was the way that control data was interpreted by the device. As discussed in [18], control of the device is achieved by transmitting a very long string of bits (1024 bits for the INIR7), which essentially means that the entire device is reprogrammed every time a single change is desired. When using a wireless channel to transmit this data that already has significant reliability issues, this large amount of data means that it becomes very difficult to successfully transmit an entire string of bits. The result is that when changing one control register, a pseudo-random change in another register is likely to occur. Additionally, because there is no error detection capability, these changes may go

unnoticed, and the chip may operate in an undesired state. A more robust technique for controlling the device and error detection are clearly both desirable.

## 1.3 Scope of this Thesis

The purpose of this thesis is to address the concerns identified in Section 1.2. When determining how to address the problem, several approaches were identified. There are clearly several ways to transmit data with inductive links, as discussed in Section 1.1, and most are more reliable and robust than ASK. The need for clock recovery from the power transmission frequency eliminates the possibility of using a single-carrier FSK system without requiring a power-hungry phase-locked loop. Dual-carrier systems have a lot of advantages, but they require considerable additional fabrication complexity. As a result, ASK was still determined to be the most appropriate choice for this project.

Although there has been significant prior work done using the inductive link as a data carrier, the bandwidth of this using ASK has never been characterized. In fact, many papers assume that the bandwidth is directly related to the quality factor ($Q$) of the transmit and receive coils, while in reality the $Q$ factor is only a second order concern for AM. This assumption caused previous implementations of the INI chip to overestimate the available bandwidth for transmitting data across the inductive link, which resulting in very unreliable transmission. Chapter 2 concerns itself with characterizing the bandwidth of this inductive link channel.

The resulting bandwidth derived from Chapter 2 is relatively small, and while it could be utilized for neural recording applications with some success, it would cause data transmission times that could become large enough to be perceptible by operators for longer command sequences. Additionally, this same system could be used for stimulation chips that require a much larger forward data bandwidth. Thus, a solution for increasing the bandwidth of the system was needed. The solution implemented in the INIR8 is presented in Chapter 3.

As discussed, the existing INI system requires a complete transmission of the entire set of control data across the inductive link for each change in parameter. Chapter 4

discusses a new digital control interface that eliminates this need, which also increases the reliability of the forward data link.

In Chapter 5 the results of all work are reviewed and discussed.

# CHAPTER 2

# CHARACTERIZING THE INDUCTIVE LINK CHANNEL

The steady state behavior of inductively powered systems is well understood [3, 20]. However, an understanding of their transient behavior is relatively unexplored, and is very important when the inductive coupling is also used for data transmission, as is the case with the INI project. A power efficient and simple method for achieving low data rate wireless transmission to an inductively powered biological implant is through amplitude modulation of the magnetic field [19, 21, 7].

Intuitively, an understanding of transient behavior should possible with knowledge of standard second order LC systems; however, real systems loaded with voltage rectifiers and ripple smoothing capacitors can have dramatically altered behavior, as will be demonstrated in this paper. Unfortunately, direct linear circuit analysis of a system with a rectifier is not possible due to the nonlinearities introduced by the diodes. Instead, another approach must be taken to develop an understand the transient behavior. In this chapter a method is developed that characterizes and models the transient response and the resulting bandwidth of a rectifier-loaded inductively powered system that uses amplitude-shift keying (ASK) for data transmission.

This chapter is organized as follows: Section 2.1 gives the reader a general understanding of power and ASK data transmission using inductive coupling; Section 2.2 will develop an analytical model for the behavior of this type of system; Section 2.3 will show measurement results that confirm the accuracy of this model; and Section 2.4 will discuss the impact of these results.

## 2.1 Inductive Power and Data Transmission

Fig. 2.1(a) is an example of an inductively powered system. The voltage transmitted by $V_A$ can be amplitude modulated, which produces an amplified voltage on $L_T$, ($V_T$) that may be attenuated by the bandwidth of the transmitting LC tank. $L_T$ is magnetically coupled to $L_R$, and some percentage of the transmitted voltage is received across $L_R$ (see [3, 20]). The attenuation of the received voltage is not primarily determined by the bandwidth of the receive coil and resonanting capacitor. Instead, the various load resistances, ($R_L$, $R_R$, and the loss in the diodes), and the size of the smoothing capacitor $C_S$ turn out to be the dominant parameters.

One method of evaluating system bandwidth is simply to ignore losses other than the load resistance. This would result in a recovered voltage with an envelope described by the time constant $\tau_{env} = R_L C_S$, and from that time constant the bandwidth of the system could easily be derived. In most cases; however, this

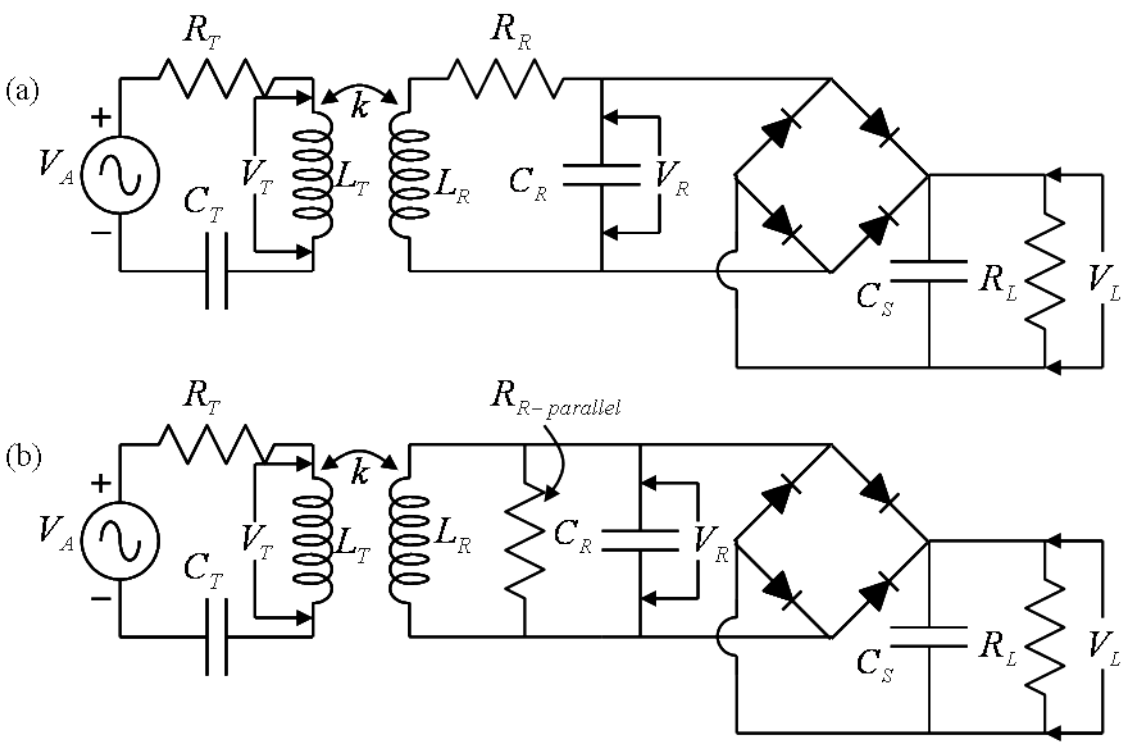


**Figure 2.1**. Circuit diagram of inductively powered RLC system with diode bridge rectifier load. (a) shows the circuit with series parasitic resistance; (b) shows the narrowband equivalent circuit with parallel parasitic resistance.

method is overly conservative and can dramatically underestimate system bandwidth. Instead, a method was developed to describe the time constant accounting for the entire system, a task made more complex by the nonlinear nature of rectification.

Fig. 2.2 shows a typical ASK waveform at various locations in the circuit seen in Fig. 2.1(a). The first waveform is of the ASK modulation created by the amplifier, which is essentially ideal in most cases. The second waveform shows the shape of the waveform across $L_T$. The shape of this waveform depends on $L_T$, $C_T$, and $R_T$, and may have overshoot in an underdamped system. However, this transient is also typically negligible when compared to $V_R$, the received voltage across the parallel $LC$ tank. Understanding this third waveform is an important goal for this thesis, and the question is explored here.

Values predicted by the standard equations for a linear second order system tell us almost nothing about how that system will respond to amplitude modulation when rectification is added. In fact, for conditions typical of devices developed for the INI project, the standard second order equations predict a time constant of the received voltage envelope that is between one and two orders of magnitude removed from the measured value.

## 2.2 Modeling the Transient Response

The first concern is the development of an analytical model that will attempt to characterize the transient response of the system. The purpose of this model is to be simple and intuitive, and some accuracy is sacrificed in achieving this goal.

### 2.2.1 Basic Model

Analysis of the circuit in Fig. 2.1(a) cannot be done using standard linear circuit analysis, because the diodes create nonlinear behavior. Instead, a fundamental definition of the quality factor $Q$ of a second order RLC circuit is used as a basis for analysis of the circuit behavior. This definition is given in Equation 2.1 [22].

$$Q = \omega_{res} \frac{energy\ stored}{average\ power\ dissipated} \tag{2.1}$$

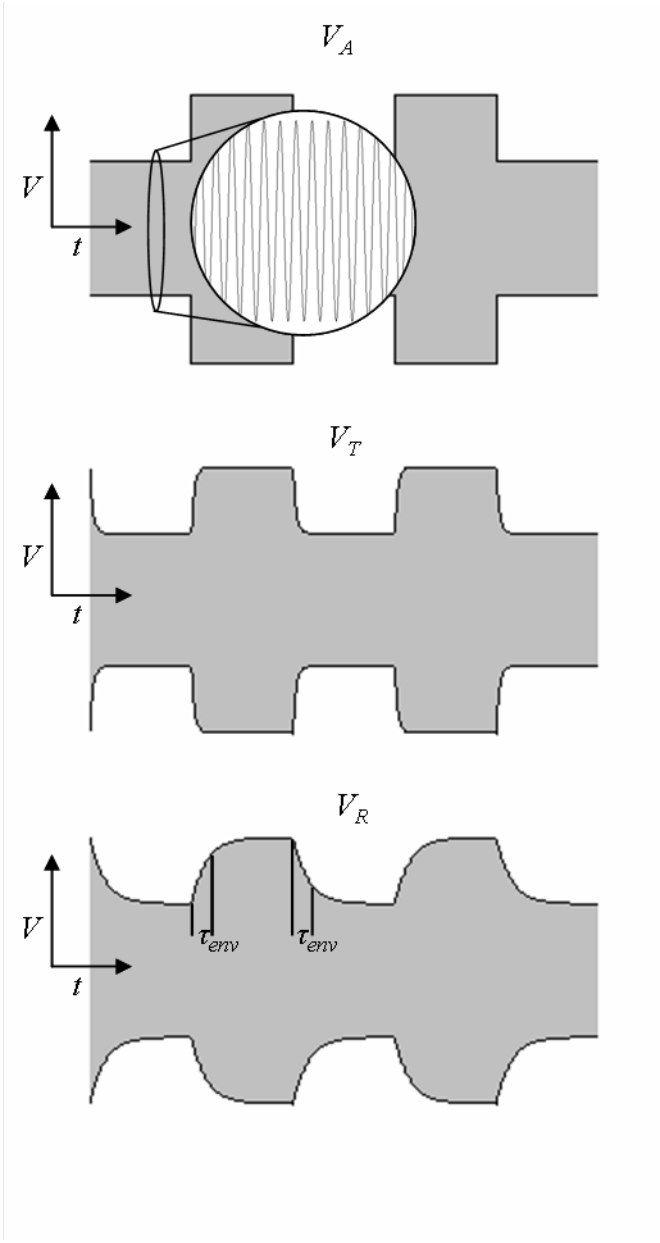


**Figure 2.2**. ASK waveform viewed at the amplifier output ($V_A$), the transmit inductor ($V_T$) and the receive tank ($V_R$).

By considering the total energy stored and the total power dissipated in the system, a $Q_{pseudo}$ can be obtained that reasonably describes the transient behavior of the system. This has been done in Equation 2.2.

$$Q_{pseudo} \equiv \omega_{res} \frac{\frac{1}{2}C_R V_{R-peak}^2 + \frac{1}{2}C_S V_L^2}{\frac{V_L^2}{R_L} + P_{rect} + \frac{V_{R-rms}^2}{R_{R-parallel}}} \tag{2.2}$$

The energy stored in the receive side of the circuit can be completely described by the numerator of Equation 2.2. Energy is stored in two places in the circuit shown in Fig. 2.1: oscillating between $L_R$ and $C_R$, and in the smoothing capacitor $C_S$. The energy stored in the tank can be described by $\frac{1}{2}C_R V_{R-peak}^2$ because at the peak voltage all of the energy is stored in the capacitor. The energy stored in $C_S$ is described by $\frac{1}{2}C_S V_L^2$.

The average power dissipated in the circuit is given by the denominator of Equation 2.2. There are three terms that represent the primary sources of power dissipation in the circuit: the load, represented by $R_L$ in Fig. 2.1; loss in the diode bridge rectifier; and coil loss, represented by $R_R$ in Fig. 2.1(a). Because the power dissipated in the rectifier circuit is nonlinear and varies considerably, it is noted simply as $P_{rect}$ in this equation. Also, while the receive LC tank's resistance is due to the resistance of the coil, and is thus a series resistance, it can be converted to a narrowband equivalent parallel resistance by considering that $R_{R-parallel} \approx Q_R^2 R_R$ [22]. This can be seen in Fig. 2.1(b) and results in the approximate direct expression for $R_{R-parallel}$ given in Equation 2.3.

$$R_{R-parallel} \approx \frac{\omega_{res}^2 L_R^2}{R_R} \tag{2.3}$$

At this point the expression for $Q_{pseudo}$ is still fairly complicated, but a few simplifications can still be made. First, since the size of the resonating capacitor of the receive coil $C_R$ is determined by $C_R = (\omega_0^2 L_R)^{-1}$, when $f_0$ is on the order of a few megahertz and $L_R$ is a few tens of microhenries, a smoothing capacitor on the order of tens of nanofarads will completely dominate $C_R$, since $V_{R-max}$ and $V_L$ are similarly valued.

The next simplification, which will be shown to reduce the accuracy of the model, is to completely idealize the diodes, giving them no power dissipation. Also, the voltage drop across the diodes are neglected, so $V_{R-max} = V_L$ is assumed. Neglecting the diode drop will cause the power dissipated in the load to be somewhat overestimated. The diode drop could be as high as 1 V, depending on what type of diode is selected. So, for a typical $V_{R-max}$ of 5 V, this can result in as much as a 20% error in calculating the power in the load. The complete neglect of the power dissipated in the diode drop has an even larger effect, and in the opposite direction. Nevertheless, both of these components are ignored in order to obtain a first order expression that, as will be shown, does a reasonably good job of modeling the results.

The resulting equation from these simplifications is shown here:

$$Q_{pseudo} \approx \frac{\omega_{res} C_S}{1/R_{R-parallel} + 2/R_L} \tag{2.4}$$

Then, by considering that $\tau_{env} = 2Q/\omega_{res}$, a simple and interesting expression can be derived for the time constant of the envelope, which is shown here:

$$\tau_{env} \approx \frac{C_S}{1/(2R_{R-parallel}) + 1/R_L} \tag{2.5}$$

$\tau_{env}$ describes the rate that the envelope of voltage seen at $V_R$ can change, as noted on the $V_R$ waveform in Fig. 2.2 This value is fundamental in determining the bandwidth of the system.

This expression for $\tau_{env}$ shows that the loss in the coil takes the form of a resistance in parallel. $R_{R-parallel}$ is doubled because it has an oscillating voltage across it and half power is dissipated with respect to the peak voltage of oscillation ($V_L$). There would be another term if the power lost in the diodes were included, and as the coil loss and diode loss become smaller the expression simplifies to the time constant of the simple RC circuit defined by the smoothing capacitor and load resistance. So, for very efficient coils with negligible diode power lost, the transient response of the voltage envelope is dominated by the simple first order RC system load, and the inductive link behaves as an ideal current source.

For a conceptual understanding of the dominance of the load in determining the transient response of the LC tank, consider that when the receive coil is being charged by the transmit coil, a large portion of the charge that would otherwise resonate in the system is being discharged into the smoothing capacitor. Additionally, there is reflected resistance into the tank system from the power lost in the diodes and the load. As soon as the voltage $V_R$ across the resonating capacitor increases above the voltage on the smoothing capacitor (at one diode drop above $V_L$), current flows into the $C_S$. This happens every cycle, so the charge buildup is dramatically slowed in the LC tank.

As $V_R$ is reduced, the smoothing capacitor must induce a current that flows through the load resistance and then through the diodes and LC tank, so a net charge is introduced into the tank from the load, slowing the rate of decay. The rising edge transient has the same time constant as the falling edge, though it should be noted that when there is no charge in the LC tank, such as when the system is turned off, the time constant becomes simply $\tau_{env} = R_L C_S$.

Because the charge required on $C_S$ does not contribute to the resonating charge in the coil, $Q_{pseudo}$ is not a true quality factor. It can accurately predict the bandwidth of the system, and thus the time constant of the amplitude transient, but it cannot be used to predict the actual amplitude of the voltage at resonance.

### 2.2.2 Accounting for a Nonideal Rectifier

A reasonable intuition can be gained about a system using Equation 2.5; however, if more accurate results are needed, the rectifier must be more carefully considered. Most importantly, the power dissipated in the rectifer must be accounted for. However, because diodes are nonlinear, understanding the power dissipated in them is not trivial.

In order to account for the diode power, the current passing through the rectifier must be approximated. The current through the rectifier is driving some load resistance $R_L$ and the smoothing capacitor $C_S$. For a parallel RC system driven by a stepped current response, the voltage response will be exponential with a time constant $\tau$. Thus, if the $\tau$ is approximated as simply the RC time constant of the load

resistance and smoothing capacitor, the rectifier behaves like a step-response current source, so the current through the load can be assumed to be approximately constant and given by the steady state current through the resistor. This results in Equation 2.6.

$$i_{avg} \approx \frac{V_{L-max}}{R_L} \tag{2.6}$$

Making this approximation eliminates the need to calculate a numerical solution and greatly simplifies the resulting expression. Of course, $\tau$ is not actually governed by the load resistance and smoothing capacitance alone. Because $\tau$ will actually be smaller than the value used here, the current drawn by the load actually spikes and then decays exponentially. As a result, the predicted power dissipation will also be underestimated. This effect is small enough to be neglected when the power dissipation in the load is dominant, but becomes significant as the power dissipation in the rectifier and in the coil become more significant. The results can be seen in the measurements section.

Now that a reasonable estimation of the average current is known, the power dissipation can be easily derived by considering the voltage drop in the diodes and the current through them, as shown in Equation 2.7. (There are two diodes in the path for a diode bridge rectifier.)

$$P_{avg} \approx 2V_{diode}\frac{V_{L-max}}{R_L} \tag{2.7}$$

Finally, it would be useful to consider Equation 2.7 with units of admittance instead of power, so that it matches the denominator terms in Equations 2.4 and 2.5 and can be added easily as an additional term. In order to accomplish this, $1/V_L^2$ must be factored. This results in Equation 2.8.

$$\frac{1}{R_{diode}} \approx \left[\frac{2V_{diode}}{V_{L-max}}\right]\frac{1}{R_L} \tag{2.8}$$

The voltage ratio defines the relative significance of this term. For large load voltages, this term will become negligible, as expected. The value of $V_{L-max}$ depends

on the transmit coil components, the coupling of the coils, and the receive coil components, and is described in [20]. One additional value must be defined to solve this expression—the value of $V_{diode}$. The way that this value is determined depends on the type of diode being used in the system. For many applications where inductive power is used, a CMOS or bipolar device is used as a diode, as described in [23], where the value of the diode drop is also defined. For a discrete semiconductor diode, the voltage drop can be calculated using the standard diode equation, measured experimentally, or given by the manufacturer. In general, a discrete diode can be thought to have a voltage drop of about 0.7 V at the current levels typically encountered (a few mA). This value is what will be used for this paper.

Taking the results from Equation 2.8 and including them in Equation 2.5, Equation 2.9 is derived, where $D$ is the "diode factor" given in Equation 2.10. Thus, the end result of this attempt to include the diode power loss in the equation is to decrease the size of $R_L$ proportionate to a correction factor, $D$.

$$\tau_{env} \approx \frac{C_S}{\frac{1}{2R_{R-parallel}} + \frac{D}{R_L}} \tag{2.9}$$

$$D \equiv \frac{2V_{diode}}{V_{L-max}} + 1 \tag{2.10}$$

### 2.2.3 Boundaries of the Improved Model

The approach taken in Section 2.2.2 is accurate in many cases; however, in cases where $R_L$ is not the dominant source of power dissipation, this simple expression becomes less accurate. These conditions are not likely to be encountered, because the entire purpose of inductive powering is to power the load.

The reason for the loss of accuracy in this corner case is the assumption that the current through the diodes is constant, made for Equation 2.6. To understand this, consider the expression for current leaving the rectifier, shown here:

$$i_{rect}(t) = C_S \frac{dV_L}{dt} + \frac{V_L}{R_L} \tag{2.11}$$

If the voltage transient that is the object of this analysis is considered to be perfectly exponential, the resulting expression is Equation 2.12, where $\tau$ is the same value that is under investigation and $\Delta V_L = V_{L-max} - V_{L-min}$.

$$V_L(t) = (1 - e^{-t/\tau})\Delta V_L + V_{L-min} \tag{2.12}$$

If Equation 2.12 is used in Equation 2.11, the current leaving the rectifier is also given by Equation 2.13. Notice that if $\tau = R_L C_S$, the expression reduces to Equation 2.6.

$$i_{rect}(t) = \Delta V_L \left( \frac{C_S}{\tau} - \frac{1}{R_L} \right) e^{-t/\tau} + \frac{V_{L-max}}{R_L} \tag{2.13}$$

This expression looks approximately like a flat line unless $\tau \gg R_L C_S$ or $\tau \ll R_L C_S$. For our purposes, $\tau$ will never be greater than $R_L C_S$, so we need only worry about the latter case. This occurs when the power dissipated in the load is comparable or less than the power dissipated in the rectifier and coil. This is most likely to occur because the wirelessly powered device is not drawing much power. In this case, the approximations made to derive Equation 2.9 are no longer as accurate. When $\tau \ll R_L C_S$, the equation begins to look look a decaying exponential. This is confirmed in measurement by a spike in current through the rectifier that decays exponentially.

### 2.2.4 Time Constant and Ripple Tradeoff

The peak-to-peak ripple voltage $V_{ripple}$ of a full-wave rectifier is given as shown in Equation 2.14. This equation is similar to those presented in many textbooks, and simply considers an exponential decay over a period defined by twice the carrier frequency. It can also be represented in terms of 3 dB bandwidth if you consider that $\omega_{3dB} = 1/\tau$, as also shown.

$$\frac{V_{ripple}}{V_L} = \frac{\pi}{\tau \omega_{res}} = \pi \frac{\omega_{3dB}}{\omega_{res}} \tag{2.14}$$

This expression gives a clear indication of the tradeoff between bandwidth and ripple voltage, but is only accurate when the ripple voltage is small with respect to the load voltage. Essentially, to achieve a desired ripple factor, the available bandwidth

is $\pi$ times smaller than that same ratio of carrier frequency and bandwidth. Thus, decreasing the frequency and increasing ripple are the primary parameters available for increasing bandwidth. As an example, to achieve a 1% ripple factor, assuming a carrier frequency of 2 MHz, the 3 dB bandwidth for ASK is 6.3 kHz.

## 2.3 Measurement Results

The analysis presented in Section 2.2 was verified by building and testing a discrete prototype. The transmit coil was powered by a Class-E amplifier producing a sinusoidal 2.765 MHz voltage. The supply voltage to the Class-E amplifier was modulated to effect amplitude modulation on the coil. The transmit coil was a flat PCB coil with an inductance of 25 $\mu$H, an outer diameter of 5.8 cm, an inner diameter of 1.0 cm, 28 turns on a single layer, and an equivalent series resistance of 11 Ohms at 2.765 MHz. The transmit coil powered a 25 $\mu$H small gold receive coil typical of a coil that would be used on an implanted device. The receive coil had an outer diameter of 5.5 mm, an inner diameter of 1.0 mm, and three layers with 30 turns per layer, and an intrinsic equivalent series resistance of 25 $\Omega$ at 2.765 MHz.

The receive coil was placed in parallel with a 100 pF resonating capacitor, which when combined with parasitic capacitance gave them a resonant peak of approximately 2.765 MHz. Across this parallel combination a diode bridge rectifier constructed of four 1N914 diodes. At the output of a rectifier, a default smoothing capacitor $C_S$ of 18 pF, and a default load resistance $R_L$ of 2.2 k$\Omega$ were used unless otherwise specified. Also, the Q of the receive coil was lowered by placing a 22 $\Omega$ resistor in series with the coil as needed.

The measured data shown in Fig. 2.3 and Fig. 2.4 in all cases had a rectifier output voltage modulated between $V_L = 4$ V and $V_L = 5.2$ V, in order to simulate reasonable conditions for real use of inductive links for wireless data transfer. This was done by experimentally changing the conditions of the transmit coil in order to obtain the desired results. The time constant was measured by a least squares fit of the resulting exponential waveform in MATLAB.

In Fig. 2.3, various capacitor values are used and the resulting time constant is

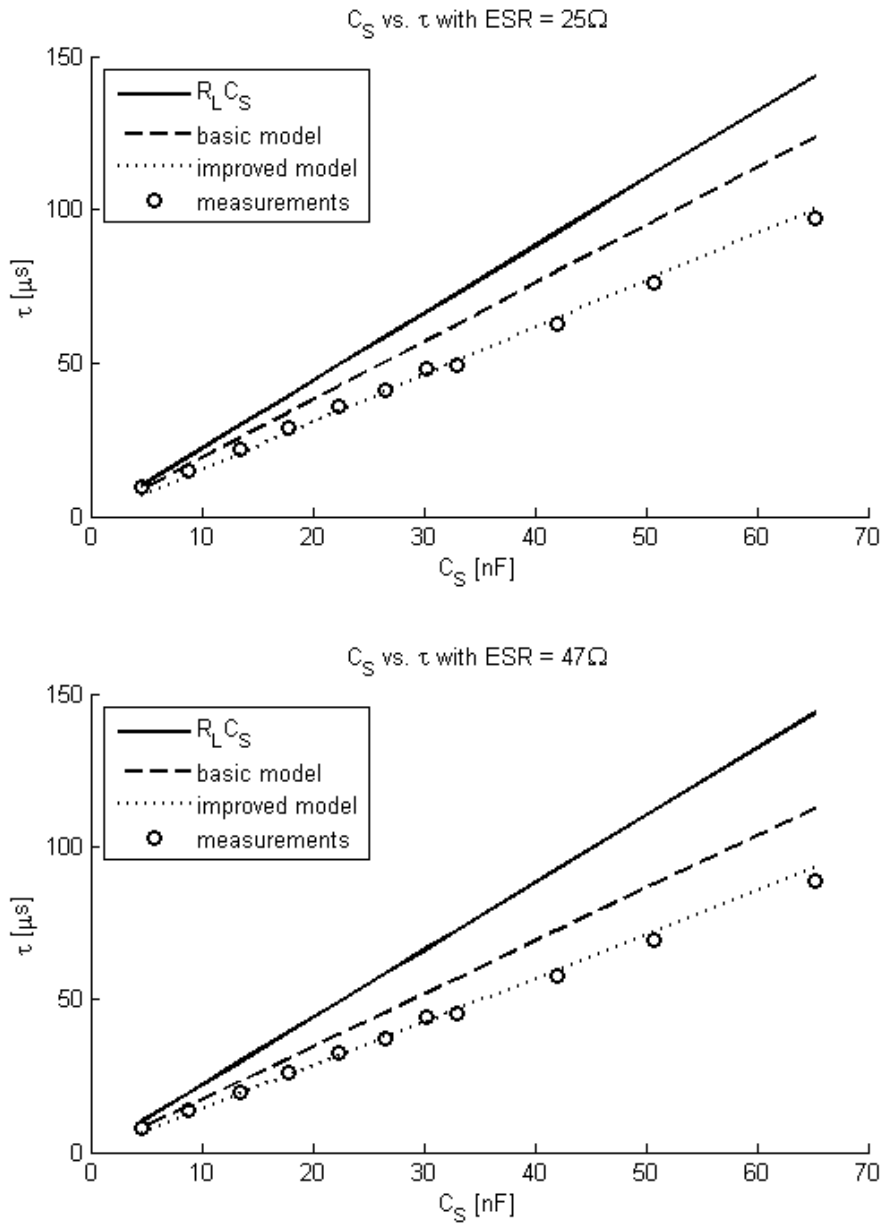


**Figure 2.3**. Sweep of smoothing capacitor values for two different inductor equivalent series resistances. The circles are the measured data points. The solid line represents the time constant predicted by just considering the load resistance and smoothing capacitance. The dashed line represents the time constant predicted by the basic model developed in Section 2.2.1. The dotted line represents the improved model that accounts for power lost in the rectifier.

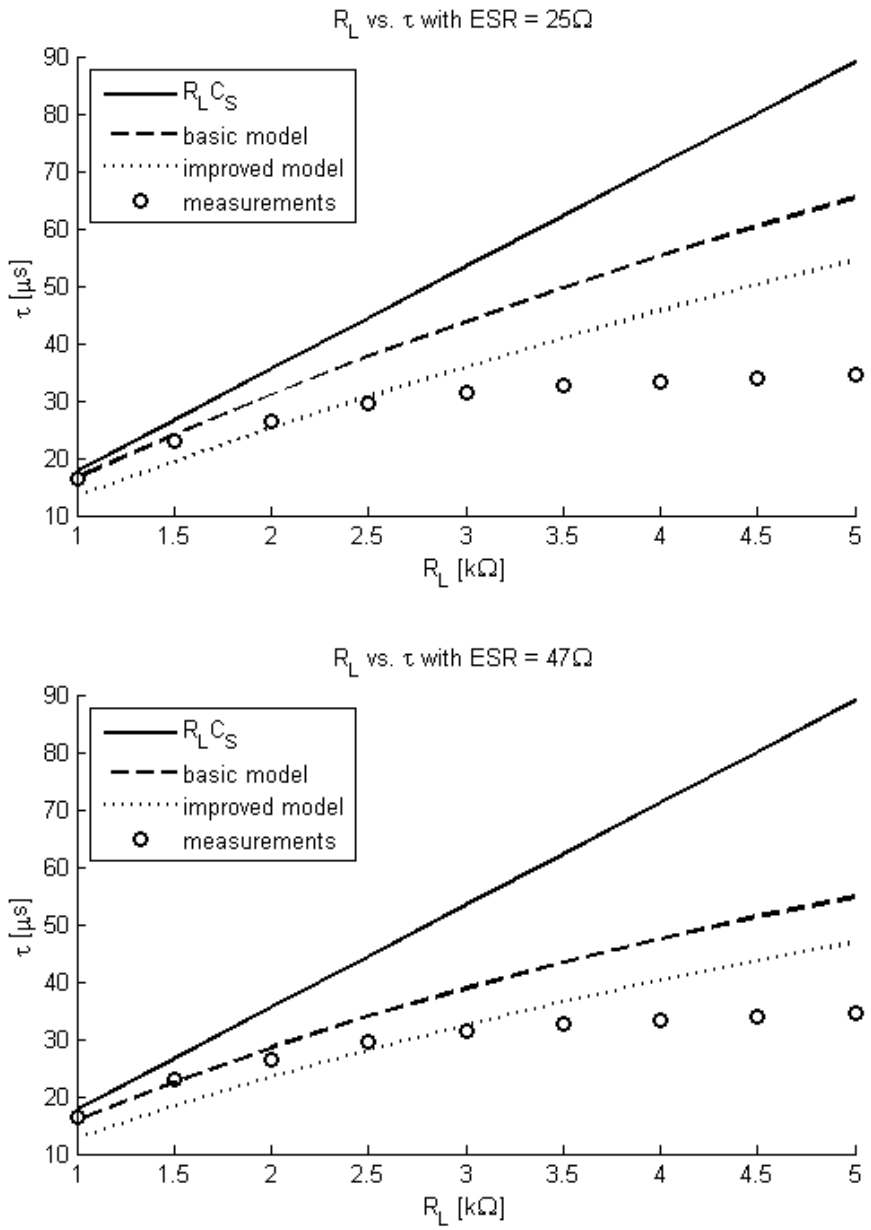


**Figure 2.4**. Sweep of load resistance values for two different inductor equivalent series resistances. The circles are the measured data points. The solid line represents the time constant predicted by just considering the load resistance and smoothing capacitance. The dashed line represents the time constant predicted by the basic model developed in Section 2.2.1. The dotted line represents the improved model that accounts for power lost in the rectifier.

measured for a lower-$Q$ and higher-$Q$ case. In the former case, the coil is used without any additional series resistance, so the ESR is 25, and thus the $Q$ of the receive coil is 17.4. In the latter case, a $22\,\Omega$ resistor is placed in series with the coil, resulting in a $Q$ of 9.2. The results make it clear that reducing the $Q$ of the RC tank is not an effective means of increasing the channel bandwidth under these conditions. It is clear that there is some effect, but this is negligible when compared with the loss in power efficiency. Consider that the $Q$ of this system, even when considering the effect of $R_L$ as described in [20] is 3.9. This should correspond to a time constant of $0.45\,\mu$s, but the results clearly show that to be off by an order of magnitude or more.

The next item to consider from Fig. 2.3 is the accuracy of the various models. As predicted by the model, the changes in capacitance present a linear change in the time constant. The inadequacy of simply considering $R_L C_S$ is clearly evident; the slope of the line is too large and results in errors on the order of 50%. Additionally accounting for the power lost in the coil, as the dashed line shows, makes the slope more accurate. This line is more accurate in the case with the lower $Q$ because relatively more of the power is dissipated in the coil than in the diode. Finally, accounting for the power lost in the diode via the method described in Section 2.2.2 provides very accurate results as the capacitance is swept in both cases.

Fig. 2.4 shows a sweep of the load resistance $R_L$ for the high and low $Q$ conditions. At low resistances, the load resistance completely dominates the other power dissipation in the system, so all three of the analytical models predict similar results. At moderate load resistance levels (between $2\,\mathrm{k}\Omega$ and $3\,\mathrm{k}\Omega$, the model that accounts for diode power loss is most accurate, as expected. However, at resistances much above $3\,\mathrm{k}\Omega$, all three models begin to lose accuracy. The reason for this is simple: the method used to calculate the diode contributions assumes that the time constant is that of the load resistance and smoothing capacitor alone, and thus a constant current can be assumed. As the load resistance increases that time constant becomes less and less accurate, and the actual current waveform develops a much larger spike of current at the beginning of the transient, which makes the power lost in the diode the dominant source of power dissipation in the system, and results in a reduced time

constant not predicted by any of the models. Thus, this model is only highly accurate when the primary source of power dissipation is not the rectifier. Since the purpose of inductive powering is to provide power to the load, this will rarely be an issue in practice. Also, even when the rectifier loss dominates the load, the improved model is still far more accurate than any other analytical method, and has the correct shape, unlike simply considering $R_L C_S$.

## 2.4 Impact of Results

In this chapter an analytical method was presented that allows a designer the ability to develop some intuition about the behavior of inductive links, particularly their behavior when used as an AM carrier. The model developed is not intended to be as accurate as simulation. The approach is valid only when the rectifier is not the dominant source of power dissipation in the system, but is still gives useful intuition even when the rectifier is dominant.

With this analysis, a designer can better understand the tradeoffs between the size of the smoothing capacitor and the resulting bandwidth of the channel and therefore make design decisions about the size of this capacitor. Experimental results show that simply using the time constant of the load and smoothing capacitor alone is far too conservative, and it is completely incorrect to use the characteristics of the unloaded RLC tank to estimate the bandwidth of the channel for amplitude modulation, as many previous papers have assumed.

Using the results of this analysis with the ripple factor requirements for the INI devices shows that the bandwidth is very low, and perhaps inadequate. As a result, a means of increasing the data bandwidth was developed, which will be discussed in the next chapter.

# CHAPTER 3

# INCREASING INDUCTIVE LINK DATA RATE

Previous INI chips have experimentally shown the need for a very clean power supply both to eliminate noise from the neural amplifiers and to increase the reliability of the RF transmitter. This requires a large smoothing capacitor after the rectifier and results in the effects discussed in Chapter 2.

In order for the device to function reliably, the minimum smoothing capacitor size was found in previous INI chips to be 10 pF, and a larger value would further improve performance. This corresponds to a ripple factor of approximately 1% given a 1 kΩ load and a carrier frequency of 2.765 MHz. The carrier frequency must remain fixed, because the clock is recovered from this frequency. Using Equation 2.14, a 3 dB bandwidth of 8.8 kHz is calculated. Simulations of the resulting recovered voltage envelope with a 10 nF smoothing capacitor and a 1 kΩ load are shown in Fig. 3.1 for square wave inputs of various frequencies.

Fig. 3.1 shows that the signal becomes severely attenuated above 10 kHz, as expected under these conditions. Beyond this point data recovery can be significantly impaired by small voltage offsets, or become very noisy in the transitions because they occur so slowly. For neural recording applications it is possible to work around this problem by using an extremely low data rate, since the forward data traffic is minimal. However, using the digital control scheme described in Chapter 4, some operations (such as changing the threshold voltage of all spike detectors) in the INIR8 will require 102 30-bit words to be transmitted. Assuming a 50% distribution of logic 0, this would require a transmission time of approximately 0.39 s using the pulse length scheme described in Chapter 4. This is a duration that is certainly noticeable to a

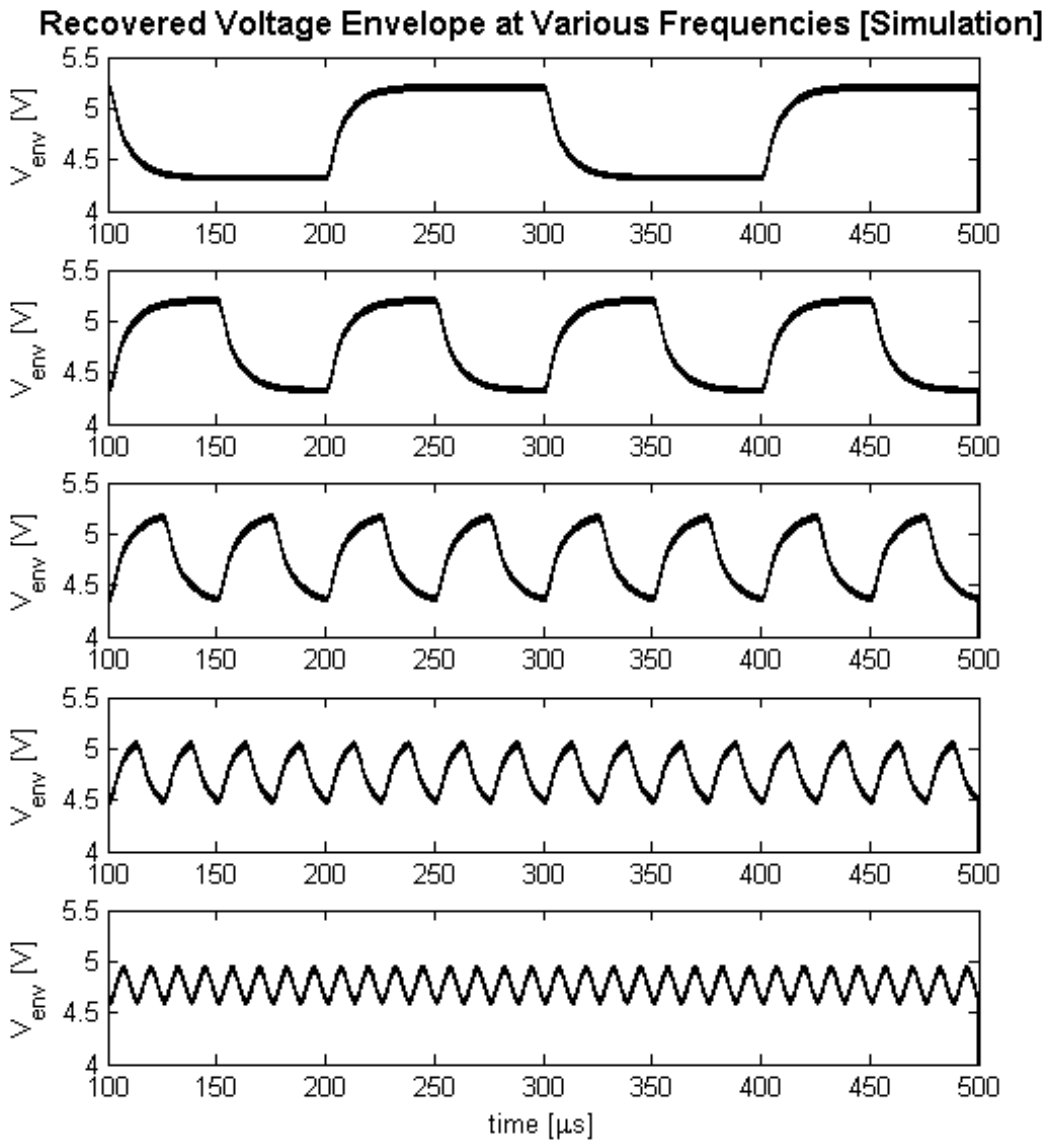


**Figure 3.1**. Recovered voltage envelope for square wave modulation of transmit coil voltage. Modulation frequencies are 5 kHz, 10 kHz, 20 kHz, 40 kHz, and 80 kHz respectively.

human operator. Additionally, for neural stimulation applications, a bandwidth on the order of 10 kHz is insufficient for many applications. In order to stimulate visual cortex, for example, bandwidths approaching those needed for video transmission are required. Clearly, achieving data rates much higher than those currently possible with amplitude modulation is highly desirable. Thus, a method developed to dramatically increase the data rate of an amplitude modulated inductive link channel will be described in this chapter.

## 3.1 General Approach

When modulating with square waves at frequencies much greater than the bandwidth of the channel, the resulting waveform looks much like a triangle wave, as seen in Fig. 3.1. If a large enough smoothing capacitor is utilized and the data rate is high enough, the envelope is effectively being integrated. The equations describing the received voltage envelope presented in Chapter 2 are accurately described by a 1st order RC circuit with a time constant $\tau$. This RC circuit is a low pass filter with a corner frequency at $1/\tau$, so for $f \gg 1/\tau$, the transfer function looks like an integration. Thus, a transmitted square wave is integrated and is received as a triangle wave. In Fig. 3.1, only the 80 kHz waveform looks completely triangular. The other waveforms are not perfectly integrated, because their fundamental frequencies are too close to the corner frequency of $R_L C_S$.

Since the received voltage envelope can be viewed as an integrated version of the transmitted envelope, differentiation should theoretically reconstruct the original waveform, if we ensure that the transmitted frequency is much greater than the corner frequency of the load and smoothing capacitor. However, differentiation is generally undesirable in circuit design because it amplifies high frequency noise more than the desired signal. This is especially problematic because the carrier frequency, while suppressed, still exists on the recovered voltage envelope. For this reason careful design of the amplifier must be undertaken to ensure that no gain exists at the carrier frequency, and also that high frequency noise is suppressed.

## 3.2 Implementation

Instead of using an ideal differentiating circuit, a high-pass filter configuration is used. A high pass filter has an additional pole that can be used to limit the gain at high frequencies, while still maintaining a differential slope at lower frequencies. The filter should have gain around 0 dB at the square-wave fundamental frequency, should increase in gain at 20 dB/decade for the first few harmonics of the square wave ($\approx 20f_f = 20 \times 20\,\text{kHz} = 400\,\text{kHz}$), and then quickly roll off to well below 0dB at the carrier frequency (2.765 MHz). The circuit implemented on the INIR8 is shown in Fig. 3.2. The input $V_{env}$ is the output of the voltage rectifier. Previous INI implementations, as discussed in [24, 25], had separate envelope detection circuits, but these envelope detectors track closely with the rectified voltage signal, so the rectifier itself is used as the envelope detector in INIR8. $V_{ref}$, as indicated in Fig. 3.2 is taken from an on-chip bandgap reference directly, since this reference has a voltage of about 1.2 V, nearly the center of the suppy ($V_{DD} = 2.5\,\text{V}$).

No voltage division is required for the incoming signal in a wide variety of cases because the 'low pass' nature of the rectifier smoothing capacitor significantly attenuates the envelope amplitude. The DC offset of the voltage envelope is moved to the reference voltage by the high pass filter, since this reference voltage is used as the 'ground' input to the high-pass filter. This same reference voltage is then used as an input to the comparator, which eliminates the need for a voltage averaging circuit, e.g., [24, 25]. The output of the comparator is then used as the input to the digital

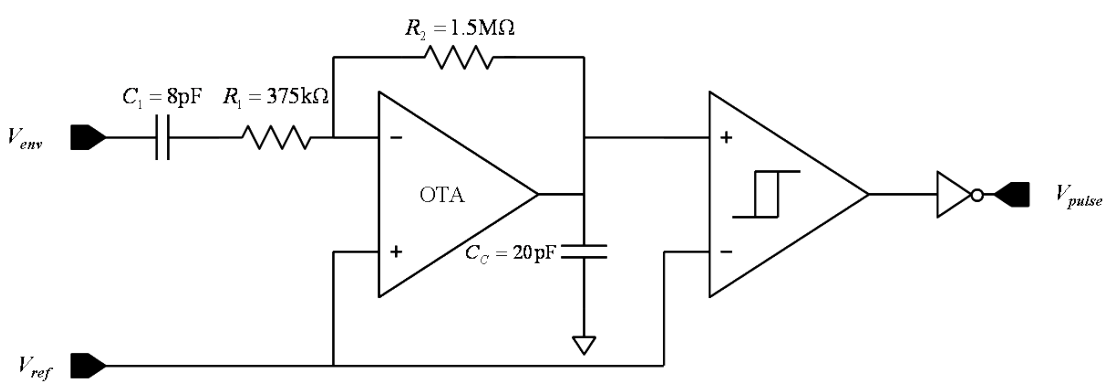


**Figure 3.2**. Design of the Data Recovery Filter Circuit

control logic, described in Chapter 4.

The entire implementation has a chip area of $0.0431\,\mathrm{mm}^2$. Most of this area is taken up by the large capacitors and resistors required to develop poles in the hundreds-of-kilohertz range. The total power dissipation including all biasing circuitry with the designed 2.5 V supply voltage, is $163\,\mu\mathrm{W}$.

### 3.2.1 Filter Stage

The first stage is an active high-pass filter using a single-stage differential pair (Fig. 3.3) as the op-amp. The gain requirements of this amplifier are low, so a single-stage amplifier was sufficient. The amplifier was loaded with a 20 pF capacitor to intentionally lower the output pole in the differential pair. A Bode plot of the simulated frequency response of this amplifier with feedback network is shown in Fig. 3.4. Note that the phase is shifted 90 degrees by the capacitor at the input, so a phase shift of 270 degrees would be required for instability. The feedback network creates a corner frequency of $\omega_c = 1/(R_1C_1) = 2\pi \times 53\,\mathrm{kHz}$. Since $R_2 = 4R_1$, the high frequency gain (were it not compensated away) would be $A_{hf} = R_2/R_1 = 4 = 12\,\mathrm{dB}$. This low gain requirement is the reason a single stage amplifier is sufficient.

Based on the high frequency gain, the corner frequency is at 9 dB. The square wave fundamental frequency is on the order of 20 kHz, and $log_{10}(20\,\mathrm{kHz}/53\,\mathrm{kHz}) = -0.42$ decades, which, at 20 dB per decade rolloff should equal 0.6 dB, since $9\,\mathrm{dB} - 20\,\mathrm{dB} \times 0.42\,\mathrm{decade} = 0.6\,\mathrm{dB}$.

### 3.2.2 High-Frequency Attenuation

In this implementation a large 20 pF capacitor is added to the load of the amplifier in order to supply an additional pole and eliminate the need for a low-pass filter stage. By reducing the frequency of the first amplifier pole, a rapid frequency attenuation occurs so that the filter is below 0 dB at the carrier frequency.

The reason for this rapid attenuation deserves a more detailed analysis. First, note that the angular frequency of the first pole in an active current mirror differential pair is approximately given by Equation 3.1 [26], where $r_{dsN}$ is the drain-source resistance of the nMOS devices, $r_{dsP}$ is the drain-source resistance of the pMOS devices, and $C_L$

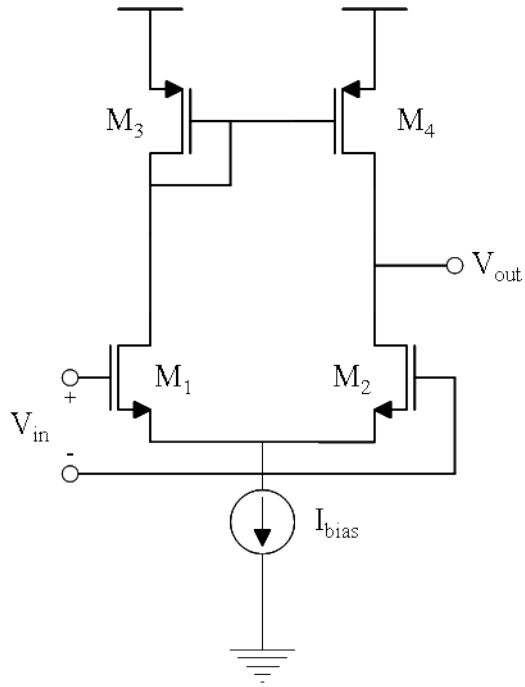


**Figure 3.3**. Single-stage amplifier used for the high pass filter. $M_1 = M_2$ have $W = 3\,\mu$m, $L = 0.7\,\mu$m, and $M = 2$. $M_3 = M_4$ have $W = 3\,\mu$m, $L = 0.7\,\mu$m, and $M = 1$. $I_{bias} = 40\,\mu$A, and $V_{DD} = 2.5\,$V.

is the capacitance loading the output of the amplifier. There is a second pole due to the current mirror gate node that is at a much higher frequency and given by 3.2 [26], where $g_{mP}$ is the transconductance of the pMOS devices and $C_E$ is the capacitance of the current mirror gate node to ground. Finally, there is also a zero that occurs approximately at $2\omega_{p2}$.

$$\omega_{p1} \approx \frac{1}{(r_{dsN}||r_{dsP})C_L} \tag{3.1}$$

$$\omega_{p2} \approx \frac{g_{mP}}{C_E} \tag{3.2}$$

The values for $r_{dsN}$ and $r_{dsP}$ were found via simulation both to be approximately 500 kΩ. These approximate values allow a rough estimation of the proper value for the capacitance by using Equation 3.1, but are not precise because the saturation current is highly nonlinear due to short channel effects. The goal is to create a double pole at the corner frequency for the high pass filter so that the filter transitions

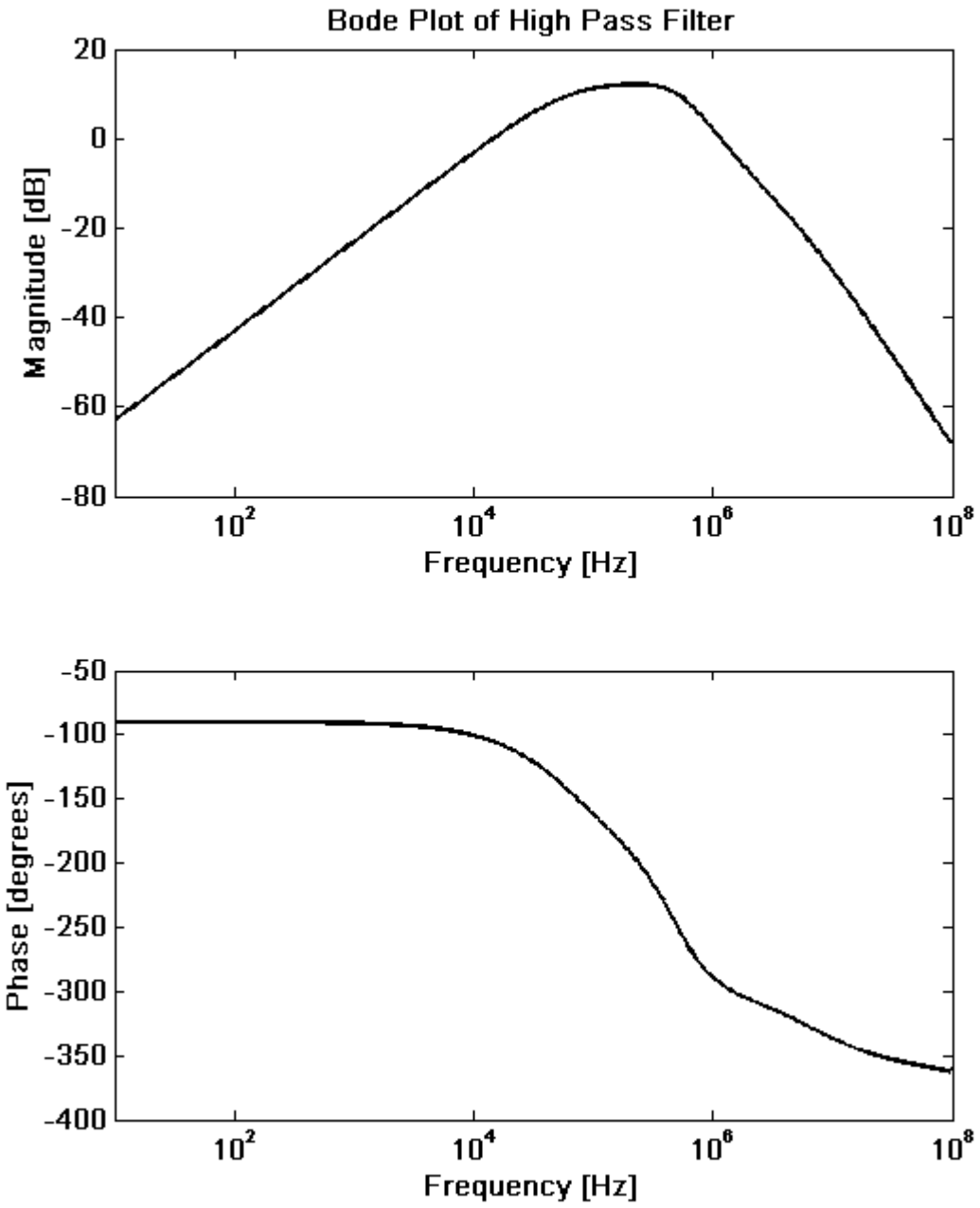


**Figure 3.4**. Bode plot of the data recovery circuit.

quickly from increasing at 20 dB/decade to decreasing at 20 dB/decade or more. The 20 pF capacitor that was finally chosen gives a pole close to the corner frequency of the high-pass filter at approximately 33 kHz; this final value was chosen by repeated simulation.

The capacitance per unit area was calculated using the process specifications as $4.6\,\mathrm{fF}/\mu\mathrm{m}^2$. This gives a ballpark estimate of the capacitance on the current mirror node of $C_E \approx 15.5\,\mathrm{fF}$. Since $g_{mP} \approx 100\,\mu\mathrm{A/V}$, Equation 3.2 results in a second pole at approximately 1.0 GHz. The small transistor size has driven this second pole to an extremely high frequency, so it is not a significant factor in this analysis.

### 3.2.3 Comparator Stage

The second stage is a hysteretic comparator with noninverting output that is followed by an inverter that corrects for the inversion caused in the OTA stage. The comparator takes the output of the filter stage as the input, and uses the same reference voltage as the OTA for the comparison threshold. Previous implementations [10] utilized a voltage averaging circuit for the threshold reference, which required carefully designed pulses so that the average value would be centered. Because this implementation uses the bandgap reference voltage as the positive input to the high-pass filter, the output waveform will be centered around this voltage. Thus, no averaging circuit is needed. The output is the set of pulse trains that will be utilized by the digital logic described in Chapter 4 that control the chip.

The transistor level schematic of the data recovery comparator is shown in Fig. 3.5. It is very similar to the design in [10], as described in [27], except that it has been redesigned for the X-Fab 0.35 $\mu$m CMOS process. It consists of a single-stage comparator, a second pMOS common source stage used to increase the gain, and an inverter used to smooth the high-gain stage output. The purpose of the high-gain stage is to ensure that the output voltage swing of the comparator is large enough to nearly span the full range of the supply voltage. The inverter then completes the digitization by making the signal fully rail-to-rail.

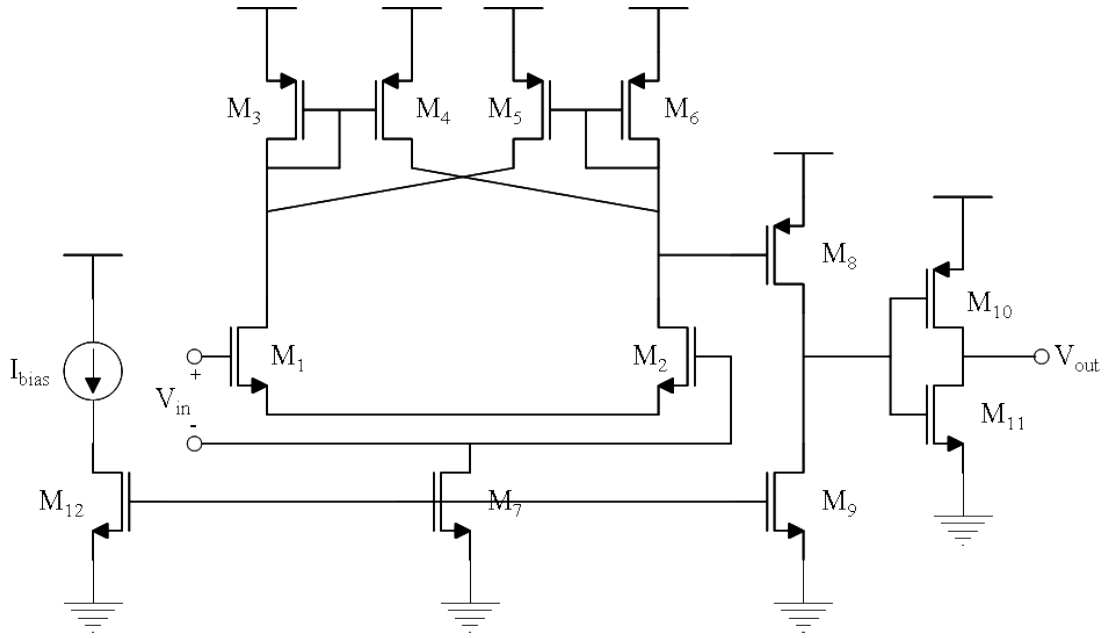


**Figure 3.5**. Transistor level schematic for the data recovery comparator. $M_1 = M_2$ have $W = 2.4\,\mu$m, $L = 0.55\,\mu$m, and $M = 2$. $M_3 = M_4 = M_5 = M_6$ have $W = 2.2\,\mu$m, $L = 0.55\,\mu$m, and $M = 2$. $M_7 = M_9 = M_12$ have $W = 5.5\,\mu$m, $L = 0.55\,\mu$m, and $M = 1$. $M_8$ has $W = 13.5\,\mu$m, $L = 0.55\,\mu$m, and $M = 1$. $M_{10}$ has $W = 4.4\,\mu$m, $L = 0.35\,\mu$m, and $M = 1$. $M_{11}$ has $W = 2.2\,\mu$m, $L = 0.35\,\mu$m, and $M = 1$. $I_{bias} = 1\,\mu$A, and $V_{DD} = 2.5\,$V.

## 3.3 Measurement

The results of testing the signal conditioning hardware were generally very positive. Most of these waveforms were taken from a test chip fabricated on the same wafers as the INIR8 QFP version. Several different test chips were used to obtain these results. There were many conditions to be tested to verify the functionality and robustness of this solution, and these will be discussed in the following subsections.

Testing was conducted using a test chip (fabricated on the same wafer as INIR8) that has the received voltage envelope output, a buffered version of the filter output, and the comparator's output available for measurement. In order to drive the device, a 25 $\mu$H printed circuit board (PCB) coil driven by a Class-E amplifier that was previously developed for the INI project was used to drive a 25 $\mu$H gold receive coil that is identical to those used in the fully integrated INI package. The gold receive coil was placed approximately 2 cm from the transmit coil, a distance that is the

worst case situation for human transcranial use. The coil was placed in resonance by experimentally adjusting the size of a resonant capacitance to produce the largest unregulated voltage. Nominally, a 1 kΩ load resistance was used across $V_{unreg}$ to simulate the chip load. The size of the smoothing capacitor is an important parameter, and varied in nearly every test. The transmitter was generally powered so that a 4 V unregulated voltage was generated. The conditions of the transmit coil varied depending on the conditions in the receive structure, since those conditions affect the unregulated voltage as well. The nominal modulation depth for these tests was 20%.

Fig. 3.6 shows an example output of the test chip. In this case, the smoothing capacitor is 50 nF, the value determined to be most appropriate for the INIR8 chip. The transmit coil was driven with what will be a series of alternating 1's and 0's after interpretation by the digital logic. A logic '1' has a high period of 30 $\mu$s followed by a 10 $\mu$s low period, while a logic '0' has a 15 $\mu$s high period also followed by a 10 $\mu$s low. Similar plots under other conditions can be found in Appendix A.

The first plot in Fig. 3.6 is the control voltage tied to the base of a bipolar junction transistor. This transistor is a part of the PCB Class-E amplifier that behaves as an emitter-follower and modulates the supply voltage into the amplifier. This serves to modulate the amplitude of the Class-E output waveform. It is shown here to indicate what pulse durations the comparator output should recover. This plot shows the AC coupled waveform, so the voltage scale indicates only change in voltage.

The second waveform is the recovered voltage envelope of the received coil voltage. It is equivalently the unregulated voltage supply, since the rectifier serves a dual purpose as envelope detector. This waveform is also AC coupled. The reason for the large offset for the entire waveform is that there is a transient change in amplitude that is related to the size of the modulation and smoothing capacitor. This will be discussed in more detail shortly. This waveform clearly shows that the transmitted square wave is being received as a triangle wave.

The third waveform is the recovered voltage envelope after filtering. This waveform is also AC coupled. The results here are very promising, and as will be shown, are robust in a variety of operating conditions. The large spikes are noise from the

digital switching of the comparator. Note that this waveform is inverted, since the filter has an inverting output.

The final plot is of the comparator. The transitions are crisp, there is no noise in the middle of the pulses, and the waveform reproduces the input control voltage with high accuracy. Note that this waveform has been inverted again to correct for the inversion of the filter.

The measurement results will be covered in more detail in the following subsections.

### 3.3.1 Robustness to Smoothing Capacitor

Decreasing the size of the smoothing capacitor without signal conditioning would directly trade off bandwidth for a lower ripple voltage. In the case of the INIR8

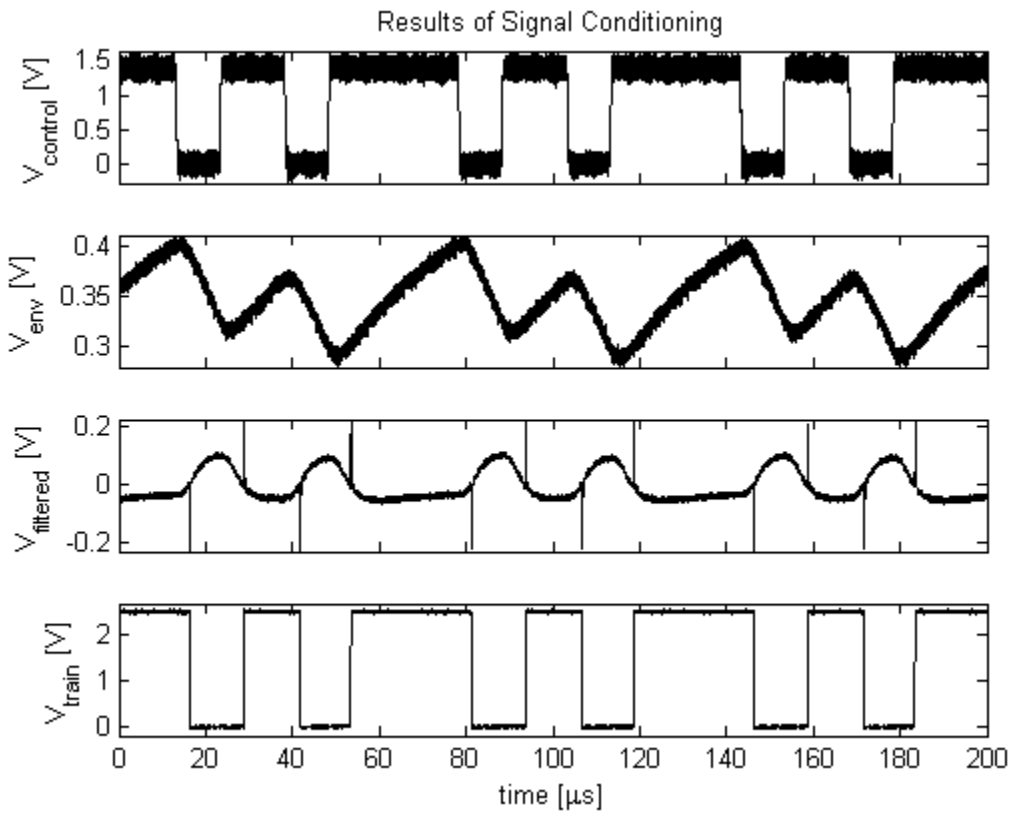


**Figure 3.6**. Sample test chip output with default setup. Alternating '1' and '0' pulsetrain.

this relationship is similar, but the effects are greatly reduced. A larger smoothing capacitor will reduce the ripple voltage and also reduce the signal-to-noise ratio (SNR) of the high-pass filter output waveform. However, the SNR is not a linear function of capacitance, because larger smoothing capacitors will reduce both the signal and the noise. Theoretically the signal and noise decrease proportionately with smoothing capacitor size, but this is not seen empirically.

For smaller ripple capacitors the $\tau$ is close enough to the frequency of the input square wave that perfect integration is not achieved by the channel. This can reduce the fidelity of the filter output. The ideal capacitor size is the largest that does not reduce the SNR to the point that the signal cannot be adequately recovered, but ideally the filter will also be robust to changes in the size of this capacitor. The results are shown in the Fig. 3.7.

Predictably, the amplitude of the received voltage envelope depends significantly on the size of the smoothing capacitor. The filtered envelope is also affected by this change in amplitude. The amplifier was designed to have a gain of about 0 dB at the modulation frequency, and this is clearly true when comparing the plots. However, the small amplitude has no adverse effects on the recovered pulsetrain, as seen.

Fig. 3.7 clearly shows that the pulsetrain is reliably recovered even with large smoothing capacitors. Large smoothing capacitors do cause a longer settling time for the pulsetrain, but the signal is still completely usable. Small smoothing capacitors cause no issue for short pulse durations (as shown), but for longer pulse durations the filtered waveform will asymptotically approach the nominal value. However, due to the hysteresis of the comparator, this actually does not cause any issues either.

### 3.3.2 Robustness to Load Resistance

Robustness to various load resistances is less important in the INIR8, since the amplifiers can no longer be individually turned off. The resulting current is thus much more stable. However, to prove robustness of this technique from product to product, it is a good idea to verify the robustness to varying load resistance. A lower load resistance can significantly reduce the Q factor of the receive coil, requiring larger transmit coil voltages. The load resistance can also have a significant effect on the

time constant of the received voltage envelope, as discussed in Chapter 2.

Testing revealed that the primary limiting factor for load resistance is the decrease in quality factor. Thus, low load resistances cause the device to require too much power on transmit coil long before there are any data transmission issues. As seen previously for changes in capacitance, the transmitted signal is reliably recovered for relatively large and small time constants. The device recovers data reliably for any value of load resistance that is large enough to power the device under reasonable operating conditions.

### 3.3.3 Robustness to Modulation Depth

Modulation depth can also have a significant impact on the quality of the received voltage envelope. Because of the smoothing capacitor, a transmitted voltage envelope

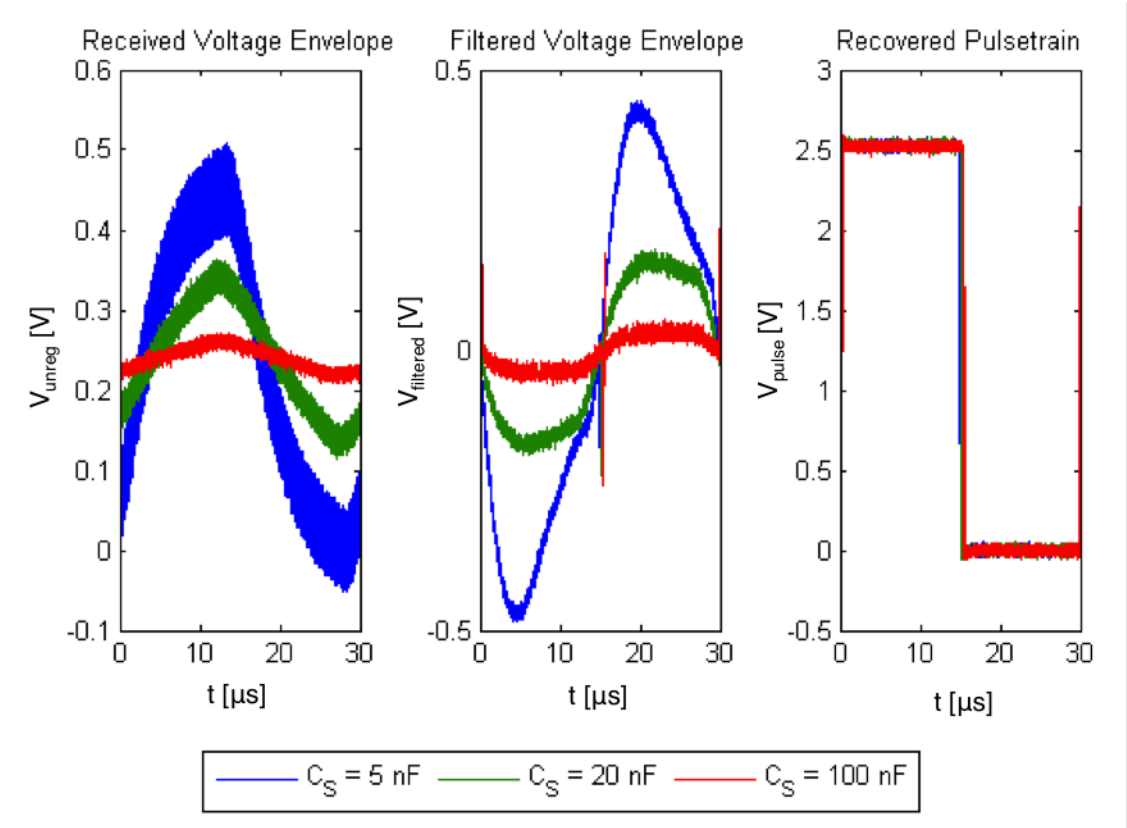


**Figure 3.7**. Parametric sweep of $C_S$ for small [5 nF], moderate [20 nF], and large [100 nF] smoothing capacitors for one period of a 33.3 MHz square wave modulation.

is significantly attenuated at the receiver. The main limitation on the size of the voltage envelope is the 10 V limit on the supply voltage to the transmit coil. A 100% modulation depth would require that the nominal supply voltage to the Class-E amplifier be 5 V. Clearly, a small modulation depth is desirable for the flexibility in transmit coil voltage that it allows.

There is a tradeoff between smoothing capacitor size, modulation depth, and SNR. The size of the received modulation depth for the three capacitor values is summarized in Table 3.1. The SNR is similarly shown in Table 3.2. A green colored cell indicates that the settling time of the comparator was less than 1 $\mu$s. Yellow indicates a settling time between 1 $\mu$s and 4 $\mu$s, and red indicates a settling time greater than 4 $\mu$s.

Table 3.1 shows that the modulation depth is attenuated for all capacitor sizes at 33.3 kHz. The attenuation is far more severe with larger capacitors. Interestingly, data can be reliably recovered with modulation depths as low as 0.60%.

The SNR table should theoretically have the same values regardless of capacitor size, since both the signal amplitude and noise amplitude depend linearly on $C_S$.

**Table 3.1**. Received Modulation Depth by Transmitted Modulation Depth

| $m_t$ | 5 nF | 20 nF | 100 nF |
|---|---|---|---|
| 30% | 15% | 6.8% | 1.3% |
| 20% | 12% | 4.9% | 1.0% |
| 10% | 6.5% | 2.8% | 0.60% |
| 5% | 3.4% | 1.4% | 0.31% |
| 3% | 2.1% | 0.91% | 0.21% |
| 1% | 0.75% | 0.31% | 0.080% |

**Table 3.2**. SNR by Transmitted Modulation Depth

| $m_t$ | 5 nF | 20 nF | 100 nF |
|---|---|---|---|
| 30% | 17 dB | 19 dB | 14 dB |
| 20% | 15 dB | 17 dB | 12 dB |
| 10% | 9.6 dB | 12 dB | 7.3 dB |
| 5% | 4.1 dB | 6.3 dB | 1.6 dB |
| 3% | -0.41 dB | 2.3 dB | -2.0 dB |
| 1% | -9.9 dB | -7.0 dB | -11 dB |

However, looking at the problem more closely it is clear why they are not equivalent. First, the noise amplitude is primarily due to the ripple voltage. Since the ripple is occurring at twice the carrier frequency, it is always in the linear regime of the exponential. The same can be said for the signal in the 20 nF and 100 nF case, since the received voltage envelope looks very triangular for these values. However, with a 5 nF smoothing capacitor and a 1 kΩ load, the received voltage envelope still has exponential characteristics. This explains the reasons for a lower SNR for that column.

The 100 nF smoothing capacitor also has a lower SNR than the 20 nF case. This may be because other noise sources (such as parasitic inductive coupling) become more apparent with very low ripple voltages, essentially creating a noise floor that is larger than the actual ripple voltage. Looking at the ripple in this case seems to confirm this theory.

Another interesting point is that while the 20 nF and 100 nF cases seem to have trouble recovering data below about 2 dB SNR, the 5 nF configuration has no trouble. However, this makes sense given that the 5 nF case does not create a perfect triangle wave. The exponential shape of this waveform causes the high pass filter to create a waveform where the data asymptotically approaches the reference voltage. As a result, the filtered data quickly passes through the reference voltage when the value changes, and very little settling time is required for the comparator.

The results of this analysis show that, as long as the recovered voltage envelope is a triangle wave, an SNR above approximately 2 dB is required for reliable data recovery with a transition time of less than 1 $\mu$s. Thus, the system should be able to recovery data at modulation depths at least as low as 5%, as long as the ripple voltage is the dominant noise source. However, experimental evidence with real INIR8 devices shows that this analysis may overestimate the actual tolerance to modulation depth. This may be due to other factors, because the pulse train is recovered very cleanly even at this low modulation depth (see Appendix A).

The methodology for determining these tables merits discussion. First, the test chip was driven with a voltage modulated signal at the appropriate modulation depth

at a frequency of 33.3 kHz. The resulting output was captured on an oscilloscope and imported to Matlab. In order to determine the SNR, an FFT of the received voltage envelope was taken, and then an ideal low pass filter with a corner frequency of 1 MHz was created by zeroing all values greater than 1 MHz. After taking the inverse FFT, the result is a relatively noiseless version of the envelope. This version was then subtracted from the original signal to recover the noise-only portion of the signal. The RMS value of these signals was taken and their ratio defines the SNR. In order to determine the modulation depth, the noiseless version of the recovered voltage envelope was used.

### 3.3.4 Maximum Input Frequency

Another important characteristic of this system is the maximum input square wave frequency that the system can successfully recover a pulse train from. For this measurement, $C_S = 20\,\text{nF}$, since that is a large enough smoothing capacitor for clean power production, and larger smoothing capacitors only serve to further attenuate the signal at very high frequencies. As Fig. 3.8 shows, this circuit is able to cleanly recover pulses at 200 kHz. This allows for a data rate of 160 kbps using the pulse train modulation described in Chapter 4.

Consider also that the Q factor of the transmit coil is approximately 40, given that it is a 25 $\mu$H inductor with an equivalent series resistance of 11 $\Omega$. The 3 dB bandwidth of an inductor with a $Q$ of 40 operating at 2.765 MHz is 35 kHz, so this data recovery circuit allows data rates several times what is possible even without a large smoothing capacitor.

These data rates still are not high enough for visual cortex stimulation, but it seems very plausible to achieve those data rates by using a higher frequency carrier, given these results.

### 3.3.5 Reliability of Recovered Pulses

Small DC offsets in the comparator and filter op-amp as well as the size of the smoothing capacitor (and resulting transient time) cause the recovered pulsetrain to differ somewhat from the transmitted modulation. This subsection attempts to

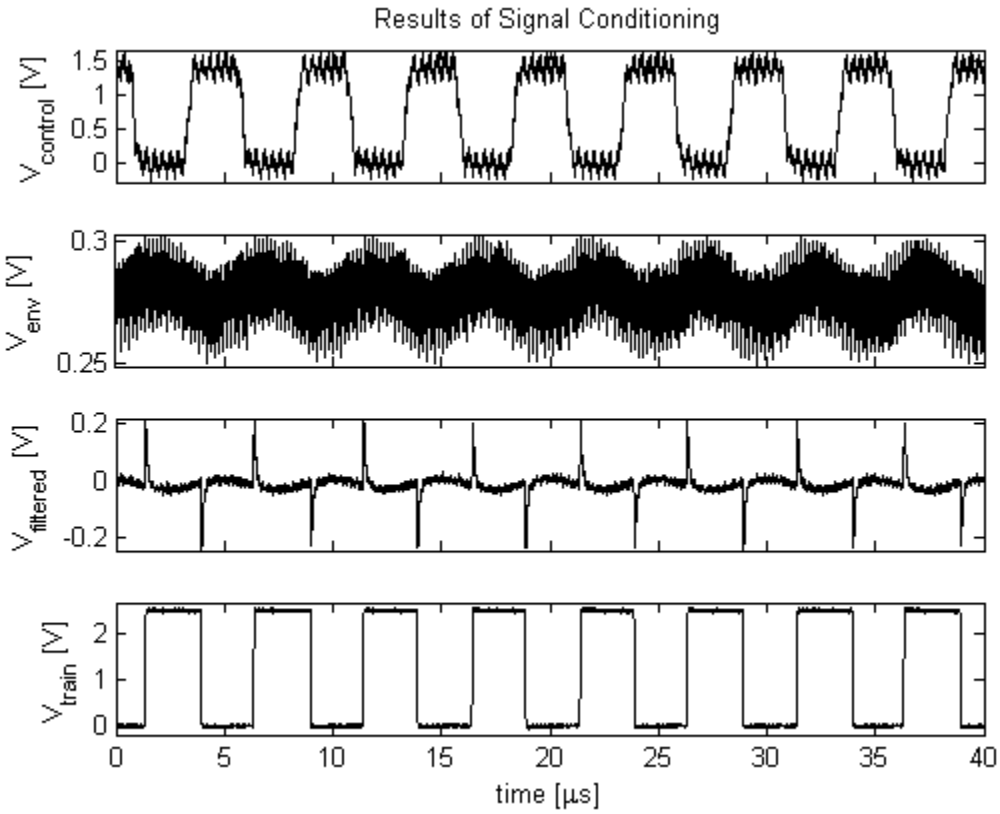


**Figure 3.8**. Pulse train recovery at 200 kHz.

illustrate the differences and comment on their significance. For these measurements, $C_S = 50\,\text{nF}$. Table 3.3 demonstrates the results.

At several frequencies around the transmit frequencies of interest, the lag time for the positive and negative edges, and the resulting high and low durations are shown. The final column is the duty cycle, which is being used as a figure of merit.

The numbers in this table are not highly accurate, since the transition time for the transmitted voltage envelope is on the order of 10s of nanoseconds, but they do illustrate the reliable recovery of the signal at all frequencies of interest, with very little difference between the transmitted and received pulses. The overall delay of the signal increases with frequency, but the difference between the rising edge and falling edge delay stays roughly constant. This analysis shows that the pulse train is reliably recovered at all frequencies of interest, with some slight error.

## 3.4 Results

The data recovery circuit described in this chapter has been found to be robust to a wide variety of operating conditions, and across various individual test chips. It can achieve much higher data rates than those theoretically achievable using other modulation techniques that do not charge and discharge a smoothing capacitor. A summary of circuit specifications is given in Table 3.4. The end result of this research is a novel technique for recovering an attenuated data stream from amplitude modulation of the magnetic field of two inductors that is extremely robust, and may present opportunities for efficiently transmitting data at relatively higher rates than previously possible.

**Table 3.3**. Reliability of Recovered Pulses at Several Frequencies

| $f$ | posedge lag | negedge lag | high duration | low duration | duty cycle |
|---|---|---|---|---|---|
| 10 kHz | 2.9 $\mu$s | 3.1 $\mu$s | 50.2 $\mu$s | 48.8 $\mu$s | 50.2% |
| 20 kHz | 3.6 $\mu$s | 3.9 $\mu$s | 25.3 $\mu$s | 24.7 $\mu$s | 50.6% |
| 40 kHz | 4.1 $\mu$s | 4.3 $\mu$s | 12.7 $\mu$s | 12.3 $\mu$s | 50.8% |

**Table 3.4**. Data Recovery Circuit Specifications

| **Parameter** | **Value** |
|---|---|
| Supply Voltage | 2.5 V |
| RMS Power (sim) | 163 $\mu$W |
| Chip Area | 0.0431 mm$^2$ |
| Minimum $C_S$ | $< 5$ nF |
| Maximum $C_S$ | $> 100$ nF |
| Recommended $C_S$ | 50 nF |
| Minimum Modulation Depth | 5% |
| Maxmimum Modulation Frequency | 200 kHz |

# CHAPTER 4

# DIGITAL CONTROL SYSTEM FOR THE INI-R8

Another way to improve the performance of the wireless link is to reduce the amount of data that needs to be transmitted across it without an error. The existing INI system incorporates what is fundamentally a shift register that is several hundred bits long. The simplicity of this older technique is highly desirable, but it introduces reliability problems. Changing the conditions for a single component on the device requires retransmitting the entire string of bits, and reprogramming the entire device.

This method of operation creates a lot of unneeded traffic across the inductive link, and the large number of bits required for transmission increases the probability of a failure. As a result, when changing the state of one part of the device, the probability of inadvertently changing the state of another part of the device is quite high. Additionally, the existing INI device has no error-checking capability, so it is difficult for the operator to determine both whether a failure occurred, and sometimes the cause of failure. This probability of failure can be modeled with a Binomial distribution with $n$ equal to the number of bits, $k = 0$ failures, and $p$ as the bit-error rate. After simplifying for $k = 0$, $P[success] = (1 - p)^n$.

The first part of this thesis addresses reducing the size of $p$. This chapter is concerned with reducing the size of $n$, and will also describe the general implementation of all digital logic for the wireless transmission of data. The approach taken in this thesis is to create an address space for the chip and a very general opcode description that will allow for one or many individually addressed registers to be changed with a single transmission. The next few sections will describe the entire digital system that takes the pulse train produced by the system designed in Chapter 3 and reads

and writes to the appropriate locations while handling any errors in transmission.

This chapter is organized as follows: Section 4.1 describes the general operation of the digital control system; Section 4.2 discusses the conversion of the pulse train created as described in Chapter 3 to a serial stream of bits; Section 4.3 describes the encoding used on the transmission to detect errors; Section 4.4 describes the address space of the system, and how the various components effect control; Section 4.5 discusses the wired override functionality of the system; and finally Section 4.6 discusses the results of integrating this system in the INI-R8.

## 4.1 Wireless Data Transmission System Overview

The op-codes comprise an 8-bit address, a 10-bit data field, and a write enable bit. This leaves 3 bits of unused space. The address consists of a 4-bit $x$-location and a 4-bit $y$-location. The system is shown in Fig. 4.1. Note that there is also an override system that allows for manual clocking of data that is not shown. In the case where override mode is engaged, data is loaded directly into the 22-bit op-code register. This functionality is discussed in more detail in Section 4.5.

For wireless transmission, each set of data is sent by first transmitting priming bits, then a 22-bit header, then some number of 22-bit op-codes, and finally a 22-bit footer. The header, op-codes, and footer should be Hamming encoded and interleaved according to Section 4.3. After encoding, the data should be transmitted MSB-first.

The data, organized as described in the previous paragraph, first encounters the logic for the pulse conversion FSM, which is described in Section 4.2. After conversion to a serial bit stream, the data enters a 30-bit shift register (the encoded data is 30 bits per word), where it is also decoded and deinterleaved combinationally. If the data is deemed valid (no bit errors are detected), the data valid flag will be combinationally high. If the header is detected, an active bit register is set, signaling that real data may occur. This bit is cleared if a footer is encountered. This active bit in combination with the data valid bit (which is also dependent on the shift count that begins after a header is detected) produce a toggle. This toggle is the clock input to all control registers. When it strobes, the data in the register (after decoding, if applicable) is

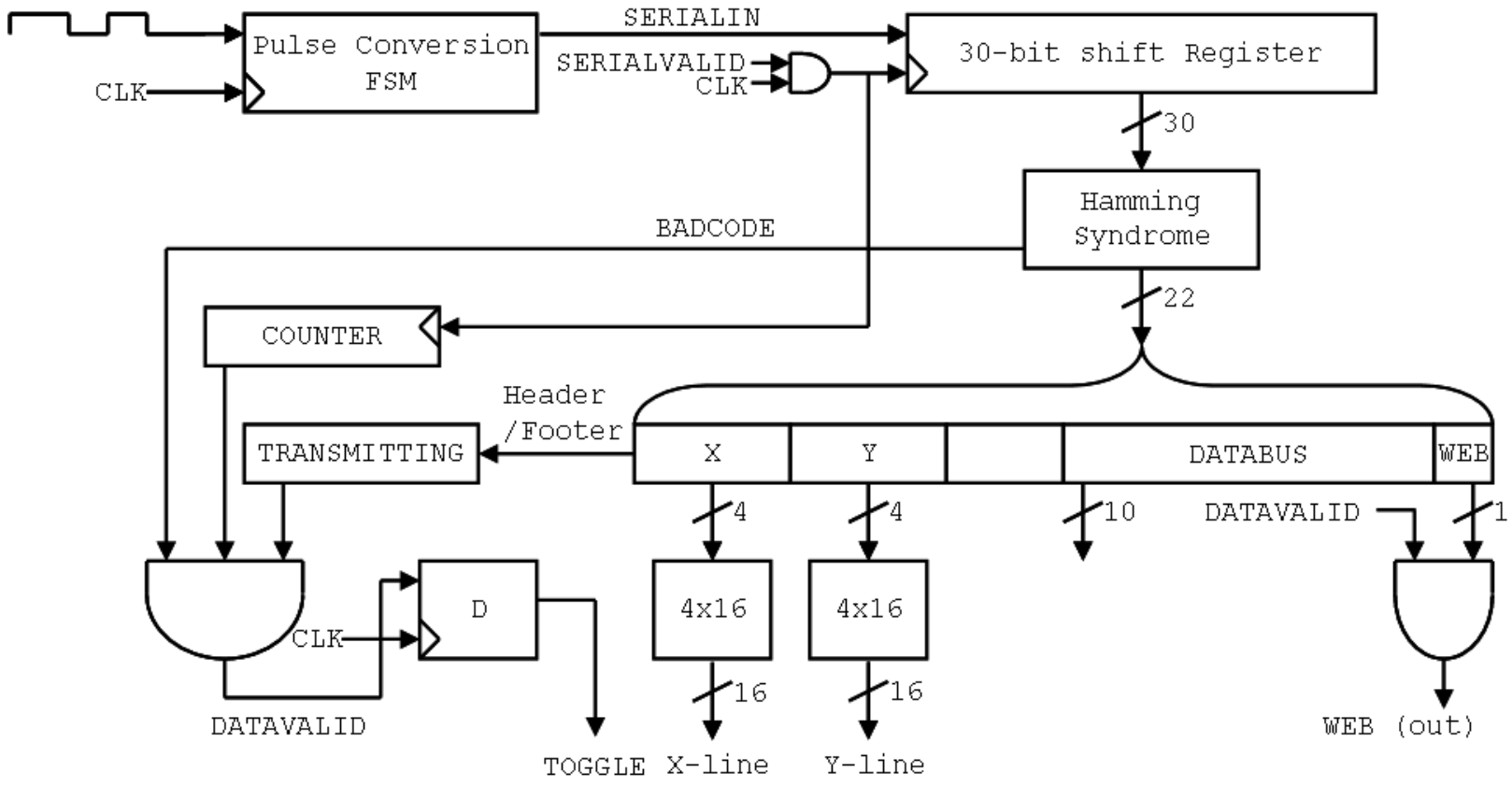


**Figure 4.1**. INI8 digital controller block diagram

applied to the address space.

Fig. 4.2 and Fig. 4.3 show the decode logic in action at a large and small scale. The inputs in the simulation are CLK, SERIALIN, SERIALVALID, and RSTB (not shown). This serial data is parallelized, passed through Hamming syndrome logic, and decoded into the op-code components. The resulting outputs are ADDR, which contains the $x$ and $y$ location of the opcode; DATABUS, which is the bidirectional data bus; TOGGLE, which is a positive edge trigger for all of the control registers in the system; and WEB, which indicates whether the op-code is a read or write.

The remaining signals are internal to the logic, and are shown here to shed more light on system operation. BADCODE toggles high when the syndrome indicates a bit error, and combinationally writes '1010101010' to the data bus to be read by the diagnostic register. CLRB resets COUNTER, which keeps track of the parallelization of data in the shift register. It begins counting after a header is detected and keeps track of the 30-bit segments of data. DATAVALID triggers TOGGLE on the next half clock cycle, since DATAVALID itself is triggered on the same edge as all of the other transitions. DECODED is the Hamming decoded data before it has been further decoded into the op-code components. TRANSMITTING is the flag that indicates a header has been detected and a footer has not yet occurred.

The large scale simulation shown in Fig. 4.2 demonstrates a series of data being parsed through by the system. Note that when TRANSMITTING is low, TOGGLE does not trigger. This is how the system ensures that data is written only while the system is meant to be active.

The small scale simulation in Fig. 4.3 shows how an individual decode actually occurs. The plot begins toward the end of a count to 30 that indicates the next serial-to-parallel conversion should occur, and shows the results. The value contained in SERIALIN is fed serially into the DATA shift register on the negative edge of CLK when SERIALVALID is high. Each time this occurs, COUNTER is increased. When the COUNTER reaches **0x1E**, on the next positive edge of CLK the data is output by setting DATAVALID to high (if BADCODE is low), which causes both TOGGLE to go high and COUNTER to reset on the following negative edge of CLK. This is

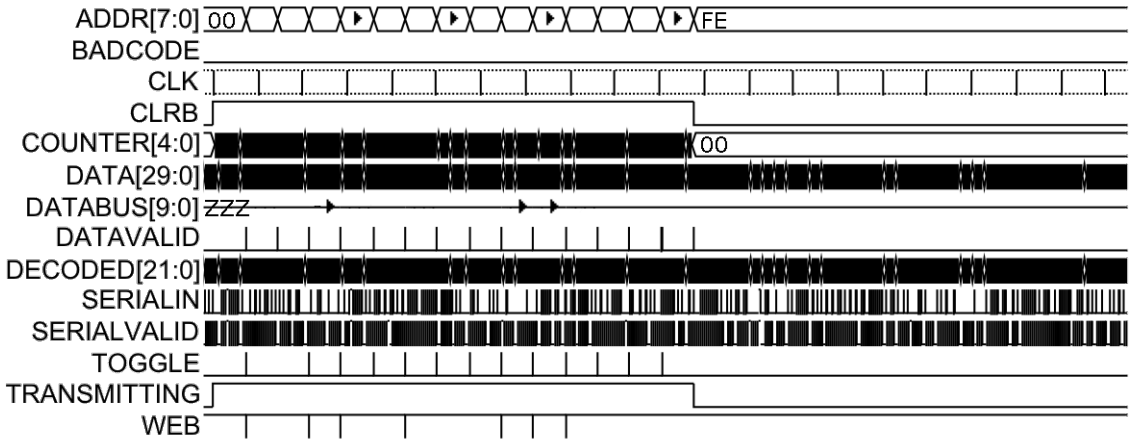


**Figure 4.2**. Large scale simulation of serial data being parallelized and decoded.

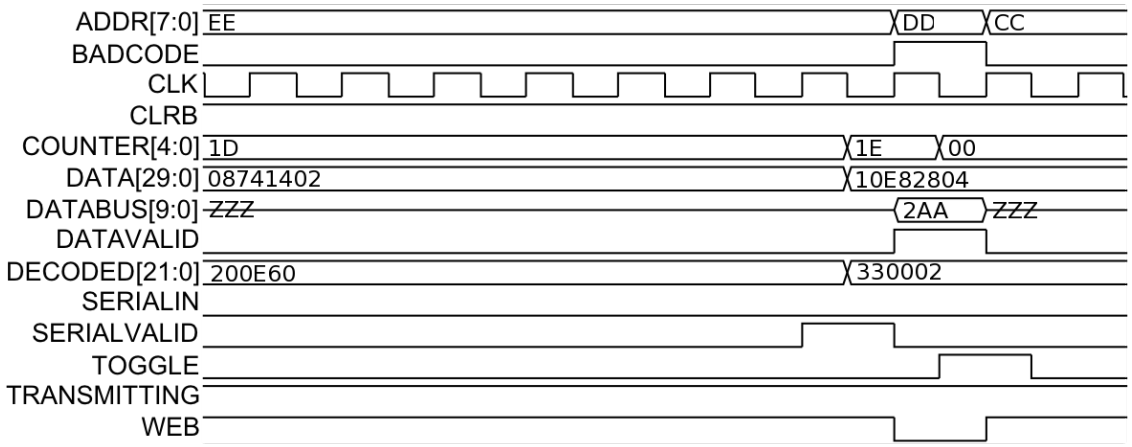


**Figure 4.3**. Simulation of serial data during the completion of parallelization.

the general functionality that allows data to be input to the system.

### 4.1.1 Priming Bits

Before beginning any transmission, a priming sequence is required. Whenever data begins to be transmitted, there is an increase in voltage proportional to the duty cycle of the signal and the peak voltage that would be achieved with a 100% duty cycle. Basically, if the priming period contains 70% high and 30% low data, the final settling value for the high value will be 70% of the value with only a high pulse. The 100% duty cycle value is proportional to the peak voltage when not transmitting and the modulation depth. The amount of time required to reach this state does not vary with duty cycle, but does vary with the size of the smoothing capacitor, since the time constant of the envelope with change. Unlike previous INI systems, there is no averaging circuit, so the priming duration is relatively shorter. Experimentally, a 10-bit priming sequence of alternating **1** and **0** pulses was found to be sufficient.

### 4.1.2 Header

After priming the system, the INI-R8 system requires a standard op-code sized (22-bit) header. This header must be encoded like any other data transmission. The pre-encoded header in hexadecimal is **0x3fad54**. After transmitting the header, all data transmitted will be interpreted as command data. Any additional header will be ignored by the digital logic. Using a header provides security on two fronts. First, it avoids any accidental instruction from being input during the priming stage or due to noise, and second, it resynchronizes the shift register in the event of a lost bit for the next transmission. Data should be transmitted immediately following the header.

### 4.1.3 Op-codes

One or more op-codes can be transmitted sequentially. If more than one is to be transmitted, the next op-code should follow immediately behind the currently transmitted code. After the final op-code is completed the footer should immediately follow. Each op-code is a 22-bit word. Bits 21:18 are for the x-address, bits 17:14 are for the y-address, bits 13:11 are reserved for future expansion, bits 10:1 are the

data field, and bit 0 is the write enable (low). More details on exactly how to address various components in the system are given in Section 4.4.

### 4.1.4 Footer

After all commands have been transmitted, a footer must complete the transmission. This is to ensure that the system does not interpret noise on the wireless link as data. The footer can be sent out of sequence so that it can terminate transmissions that have shifted due to a fade. The footer in hexadecimal is **0x3f92ab**. It is a good idea to transmit two footers at the conclusion of every data transmission to ensure that a bit-error in the footer does not leave the system open to receive transmissions.

## 4.2 Converting the Pulse Train to a Bit Stream

The method chosen in previous INI chips to transmit data via amplitude modulation was a series of pulses of different lengths, with shorter pulses assigned a value of '0', while longer pulses were assigned a logic '1' [28]. This method is fairly robust and easy to implement, so it was retained in the new system. The method for decoding these pulsetrains was changed; however, and is a Mealy machine described by the state diagram seen in Fig. 4.4. A sample output simulation can be seen in Fig. 4.5. The two inputs are PULSE, which is the pulse train, and COUNTER, which counts the number of clock cycles at 1.38 MHz that elapse between transitions of PULSE. The three outputs are CLRB, which resets and enables the counter where appropriate; BITOUT, which reflects whether the received pulse indicated a '1' or a '0'; and OUTVALID, which indicates whether the value of BITOUT is real data.

While in the default WAITING state, if the PULSE input goes to '1', the CLRB signal also goes to '1' to enable the counter, and the system transitions to the START state. The purpose of this state is to verify that the change was of sufficient duration to be considered a real pulse. This has been experimentally shown to be necessary even though the comparator at the input (described in Chapter 3) has hysteresis, especially around the time a transition occurs [25]. While in the START state, if PULSE changes to '0', the system will return to the WAITING state and CLRB will be set to '0'. While waiting for COUNTER to reach VCYCC, the number of cycles

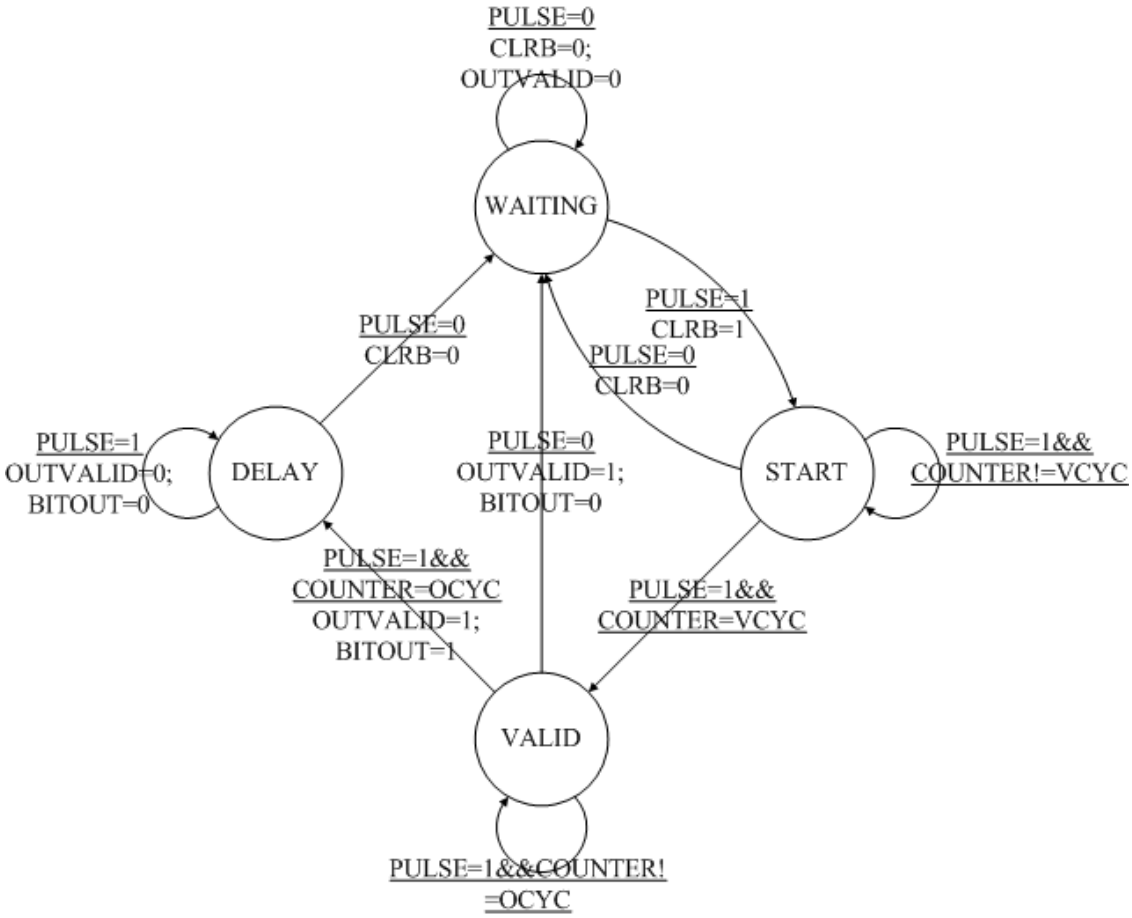


**Figure 4.4**. State diagram for pulse train to bit stream conversion

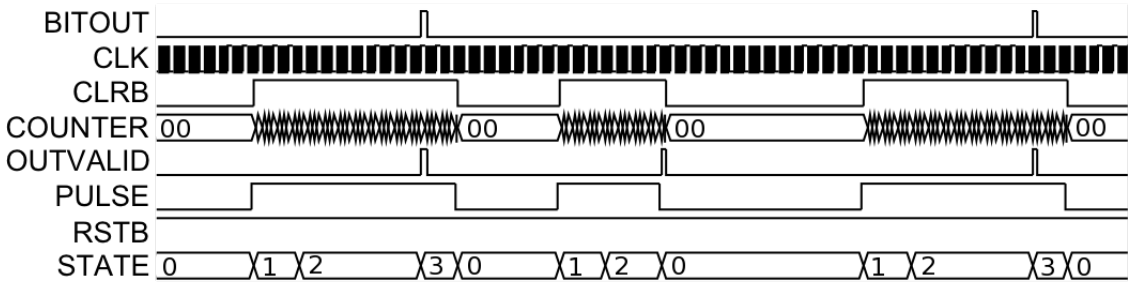


**Figure 4.5**. Simulation of State Machine for '101' bit stream. For the simulation both **1** and **0** pulses are given the same period. This dramatically simplifies testbench design, but the low period following a pulse can be any duration longer than a single clock cycle, at least from the digital logic perspective.

determined to denote valid data, it stays in WAITING. Once this number is reached, the state changes to VALID, with no change in outputs.

Once in the VALID state, the system will stay there until either the PULSE input goes to '0', or the COUNTER input reaches OCYC, which is cycle threshold to denote a '1'. If PULSE goes to '0', BITOUT also goes to '0' and OUTVALID goes to '1', indicating the value is a legitimate '0'. The clearing of the counter is left for the WAITING state's self-return. If PULSE does not change, the state will transition to DELAY when COUNTER reaches OCYC. This indicates that the pulse was long enough to denote a '1', so during this transition the OUTVALID and BITOUT outputs both become '1'. As soon as the DELAY state is entered, OUTVALID and BITOUT are both made low, to avoid double counting. The purpose of the DELAY state is to wait until PULSE becomes '0' again, so that the process can be restarted. If PULSE lasts longer than the size of the counter, the operation is undefined, and it is likely that an extra bit will appear in the output. This is one potential cause of a bit error.

### 4.2.1 Specifications for Operation

This section describes the specific quantitative requirements of the INIR8 system for the state machine described above. The clock used for the state machine operates at one-half the carrier frequency of wireless power transmission, or 1.3825 MHz. In this implementation, VCYC is 9 cycles, which corresponds to a duration of 6.51 $\mu$s. OCYC in this implementation is 33 cycles, which corresponds to a delay of 23.87 $\mu$s. Thus, each '0' encoding should have a pulse duration between approximately 7 $\mu$s and 23 $\mu$s while a '1' encoding should have a pulse duration longer than 24 $\mu$s. Typically, a value of 15 $\mu$s should be chosen for a '0' encoding, and a value of 30 $\mu$s should be chosen for a '1' encoding. After sending the pulse, some amount of low pulse time is required before sending another pulse in order to allow the state machine to return to the START state. Experimentally, 10 $\mu$s was shown to be sufficient. The resulting data rate for a data stream that has an equal number of '0' and '1' bits is 31 kbps. An example amplitude modulation is shown in Fig. 4.6.

## 4.3 Hamming Encoding

Each 22-bit word corresponds to a 30-bits of transmitted data that are composed of two interleaved (15, 11) Hamming codes [29, 30, 31]. The two different codes correspond to bits 21:12 and 11:0 of the op-code. After encoding, the two 15-bit encoded values are interleaved, with the encoded version of the top half of the word as the first bit.

The (15, 11) Hamming code was chosen, without any error correction ability, because it best addresses the most likely cause for an error: the loss of a bit. Error correction schemes, while desirable, would wreak havoc on the system in the event of a lost bit. A (15, 11) Hamming code can detect 2 bits of error before a false positive occurs. This means that 2 bits transmitted in a given 15 bit sequence can be incorrect and still detected. However, because of the nature of the transmission scheme, the most likely scenario for a transmission error is a loss of a bit during a fading period. This is the primary reason to go with the extra sparsity of a Hamming encoding versus something simpler like parity encoding. With parity, 50% of the possible bit combinations are valid codes, while with a (15, 11) Hamming code only $2^{11}/2^{15} = 6.25\%$ of the codes are valid. This means that for a given op-code, which is two of these encodings, there is a $6.25\% \times 6.25\% = 0.39\%$ chance that a bit shift error will go undetected. In addition, there is always at least a footer following every op-code that also has the same 0.39% chance of going undetected, for a total worst case probability of 0.000015%. Beyond this, if the footer were not detected as a bad code, the system would continue to accept new codes and eventually one of these codes would be detected (with a 99.61% chance that it would be the next one). When the system is notified of an error by the FSK transmitter, the software should immediately send a footer. During the intermediate time, there is a small

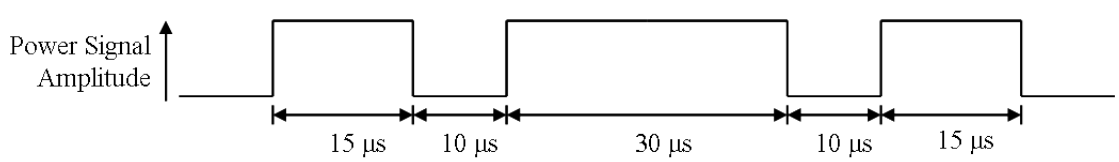


**Figure 4.6**. Timing of a transmission of '010' using the INIR8 modulation scheme

possibility (again, 0.39%) that a valid code will be transmitted. However, after a single bit error the entire packet of op-codes is retransmitted, so this is not a serious issue. Finally, the reason that (15, 11) Hamming code was chosen over a shorter code like (7, 4) Hamming was to increase the coding efficiency. The (7, 4) Hamming code has 42.9% overhead, while the (15, 11) Hamming code only has 26.7% overhead. To determine the optimal code length, overhead had to be balanced with probability of a false postive, and the (15, 11) code was a good compromise.

The INI-R8 (15, 11) Hamming encoding for the forward data link has the generator matrix shown in Equation 4.1 and syndrome matrix shown in Equation 4.2. Commands must be encoded in this format in order for the on-chip data acquisition hardware to correctly interpret the data. The coding efficiency of a (15, 11) Hamming code is 73%, so the real data rate of the system is about 23 kbps.

$$\mathbf{G} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{4.1}$$

$$\mathbf{H} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{4.2}$$

## 4.4 Addressable Components

The addressing system is flexible. It functions via op-codes that contain an address, data payload, and write enable bit. The decoded 22-bit op-code is formatted as follows: bits 21:18 are the $x$-address; bits 17:14 are the $y$-address; bits 13:11 are unused by the current system; bits 10:1 are the data payload; and bit 0 is the write enable. Writing is enabled by setting bit 0 low.

In the INIR8 there are several different types of registers that are of varying lengths. In cases where the register length is shorter than the length of the data field, the least significant bits are used. The following sections will discuss how to address the various components, and also what the data field of the op-code does for each. A summary of this information is presented in Table 4.1.

### 4.4.1 Diagnostic Register

The INIR8 system has a new 10-bit diagnostic register that is periodically read by the RF telemetry transmitter. The register can function in three distinct ways. First, in the event that a read op-code is transmitted, the data being read is written into this diagnostic register for transmission off-chip. Second, the diagnostic register can be written directly by addressing it at $x_{addr} = X, y_{addr} = 13$. This is useful for determining if the device is working correctly. Finally, if a bit error is detected, the diagnostic register will take on a special value of **1010101010**.

### 4.4.2 Spike Detector Threshold Control

Every electrode in the INI8 has a 6-bit register that determines the threshold of the spike detector for that particular location. Bits 0-4 of the register set the

**Table 4.1**. Summary of Addressable Components in INIR8 System.

| type | $x_{addr}$ | $y_{addr}$ | description |
|---|---|---|---|
| diagnostic register | X | 13 | 10-bit register containing most recent read data or bit-error code; can also be written |
| amplifier control | 0-9 | 0-9 | 6-bit register that determines spike-detector threshold; bits 4:0 determine amplitude; bit 5 determines polarity |
| polarity register | 0-9 | 10 | 10-bit register that sets polarity of spike detector threshold; each bit corresponds to one row |
| RF TX control | X | 12 | 4-bit register that determines the RF transmitter frequency; conditions determined empirically for each device |
| amplifier select | X | 11 | 9-bit register that determines output of ADC; bits 3:0 are x-mux-select; bits 7:4 are y-mux-select, and bit 8 is DAC select |

amplitude of the threshold while bit 5 is a sign bit. If bit 5 is high, the threshold is negative, while if bit 5 is positive, the threshold is positive. The output-referred step-size is 4.5 mV, which corresponds to an electrode-referred step-size of 4.5 $\mu$V.

Addressing of the amplifiers is done with the origin in the top right corner when the device is flip chip bonded, which is the same addressing scheme as that used in the Matlab graphical user interface. The $x$-address can be 0-9, with 0 as the rightmost column and 9 as the leftmost column, while the $y$-address can be 0-9, with 0 as the uppermost row and 9 as the lowermost row.

### 4.4.3 Spike Detector Polarity Registers

The spike detector polarity registers determine whether the spike detectors trigger when the waveform goes above the threshold or below the threshold. Each is a 10-bit register with a single bit corresponding to each amplifier in that particular row. Each bit in the register corresponds to the same row number. For example, bit 0 corresponds to row 0. The $y$-address for these registers is 10, and the $x$-address corresponds to the desired column in the amplifier array.

### 4.4.4 RF Transmitter Control

The purpose of this register is to control the transmit frequency of the RF register. It is a 4-bit register where all bits are used for this purpose. The address of this register is, $y_{addr} = 12$, $x_{addr} = X$. The step size and nominal value must be determined empirically for each device due to the nature of the RF transmitter.

### 4.4.5 ADC Amplifier Select

The last register is the ADC amplifier select. This register is located at $y_{addr} = 11$, $x_{addr} = X$. The purpose of this register is to determine which amplifier output is sent to the ADC, and also to determine whether the waveform or the output of the DAC is transmitted. It is a 9-bit register where bits 3-0 are $x$-mux-select, bits 7-4 are $y$-mux-select, and bit 8 is DAC select. When DAC select is low, the amplifier output is sent, while when DAC select is high, the spike detector threshold output of the DAC is sent.

## 4.5 Wired Command Protocol

All of the previous sections have discussed wireless operation of the INIR8 device, but the device can also function with a wired command interface for cases when the device is powered using a DC voltage source. The wired override mode is enabled by setting the *override* pin (pin 51 on the INIR8 QFP package) high. When override is high, any data that comes via the wireless link is ignored, and data is instead read from using *aux_clk* (pin 42) and *aux_serial* (pin 40) inputs. The interface is a clocked serial input, and is transmitted MSB-first.

Bits are read by the chip from the *aux_serial* port on the positive edge of the *aux_clk* port. The 22-bit op-codes described in the previous sections should be used, but no Hamming encoding, priming, header, or footer should be included.

There is no need to tie *override* to ground; it has an on chip pull-down resistor that automatically drives it to 0 if it is not being driven.

## 4.6 Results

This digital control system was implemented in the INIR8, and the existing Matlab interface for the previous INI chips was modified to accommodate the new method of controlling the chip. The chip appears to have some issues, but the functionality of the digital interface appears to work properly. The device correctly and reliably interprets changes to the RF transmit frequency, can modify the diagnostic register directly, and displays the proper error code in the diagnostic register if a data transmission was not correctly received. The device also successfully writes and reads back data from a variety of registers across the system. In combination with the envelope recovery circuits developed in Chapter 3, the new system has dramatically improved the robustness and reliability of forward data transmission on the INIR8.

# CHAPTER 5

# CONCLUSIONS

The stated purpose of this thesis was to improve the reliability of inductive link data transfer using amplitude-shift keying (ASK) so that the INIR8 could robustly receive command data. In order to achieve this goal, three critical achievements were needed. First, it was important to establish a greater understanding of the behavior of inductively coupled wireless channels. Second, based on the results from the analysis of inductively coupled wireless channels, the ability to transfer data at higher rates than possible was desirable. Finally, developing an improved digital control system for the INIR8 would reduce the difficulty in reliably transmitting data. Each of these attempts were highly successful.

Previous versions of the INI chip had issues with transmitted control data envelopes becoming integrated in the inductive link channel and being recovered as a triangular envelope. The reason for this phenomenon was unknown. Chapter 2 solved this unexplained problem by identifying the ripple smoothing capacitor and load resistance as significant components in determining channel bandwidth. In the process, a model was developed that gives designers intuition about the behavior of rectifier loaded inductive links. Measurement results confirmed that this model was accurate for the regions of operation that are usually encountered with these devices. The results also indicate that the data bandwidth may be insufficient for reliable data transmission.

In order to increase this bandwidth so that the devices could operate at data rates already being attempted in previous INI versions, circuits had to be developed that would reliably recover the transmitted data envelope at the receiver. A method was developed to differentiate the received triangle envelope and recover a square

wave without amplifying high-frequency noise. Measurement results proved that this method was highly robust to a variety of operating conditions and components. Also, data rates that were higher than inductive links without a rectifier load could achieve were demonstrated.

Previous INI chips utilized a single command sequence to reprogram the entire chip, and had no error detection ability for data transmission. As a result, unpredictable behavior often occurred when registers were incidentally changed while another change was attempted. In this thesis, a digital control system was developed that utilized modular op-codes in order to decrease the size of transmitted data packets and eliminated incidental changes in control registers. In addition, error detection codes were added so that the user could be aware of any incorrectly transmitted data. These two improvements made forward control data much more robust and predictable.

Between the signal conditioning described in Chapter 3 and the new digital control system described in Chapter 4, the INIR8 has much more reliable communication via the inductive link than previous INI versions. Data is reliably recovered across the entire system robustly, and the system notifies the user if there are communication errors. It does currently take longer to reprogram the entire chip, because each opcode has its own priming, header, opcode, and then two footers. The system is capable of a complete reprogram using only a single header and footer, but it is difficult to know if and where there is a bit error in this case. Eliminating this issue is one potential improvement to the system that could be undertaken in a future revision.

There are two primary novel contributions of this thesis. The first is the analysis of rectifier loaded inductive link transients presented in Chapter 2. Many previous papers made false assumptions about the behavior of this sort of channel using ASK, and even those that did have a grasp of the behavior arrived at their conclusions empirically. The second novel contribution is the use of a high pass filter to recover a square wave after attenuation. This is similar to equalization techniques that have been practiced for many years on low noise channels, but is novel to use these techniques to recover ASK data from an inductive link in this way.

Both of these novel contributions, as well as the new digital control system for the INI have the potential to have impact on the neuroscience community. Rectifying the forward data communication issues that have plagued the INI project opens the door for the device achieving it's potential as a 100 channel neural recording device, and also has the potential to improve stimulation chips as well.

# APPENDIX

# ADDITIONAL DATA RECOVERY FIGURES

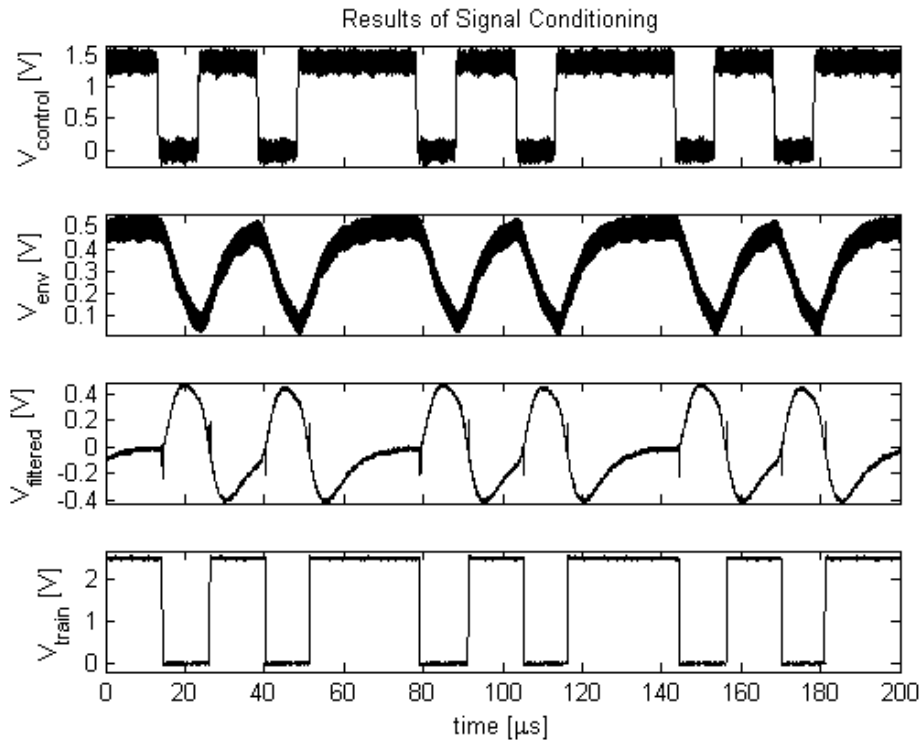


**Figure A.1**. Pulse train recovery with a 5 nF smoothing capacitor.

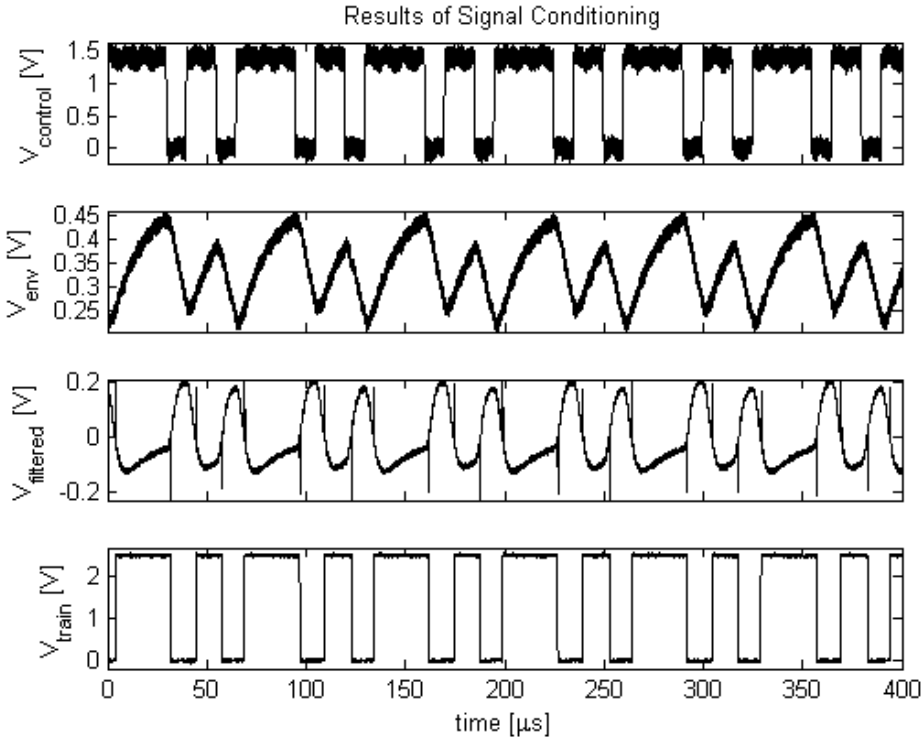


**Figure A.2**. Pulse train recovery with a 20 nF smoothing capacitor.

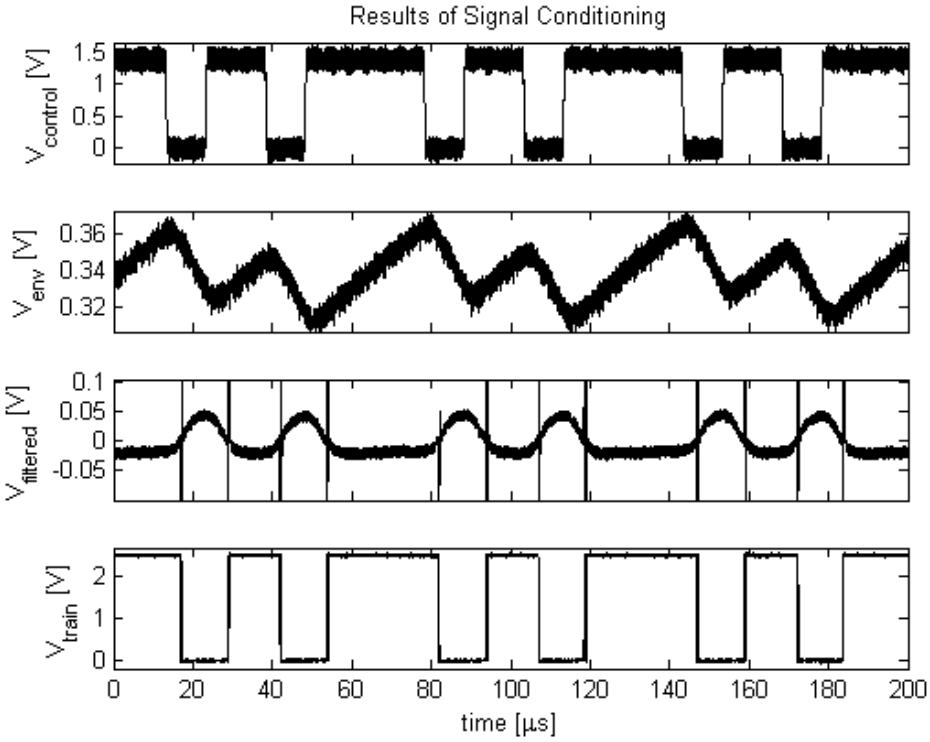


**Figure A.3**. Pulse train recovery with a 100 nF smoothing capacitor.

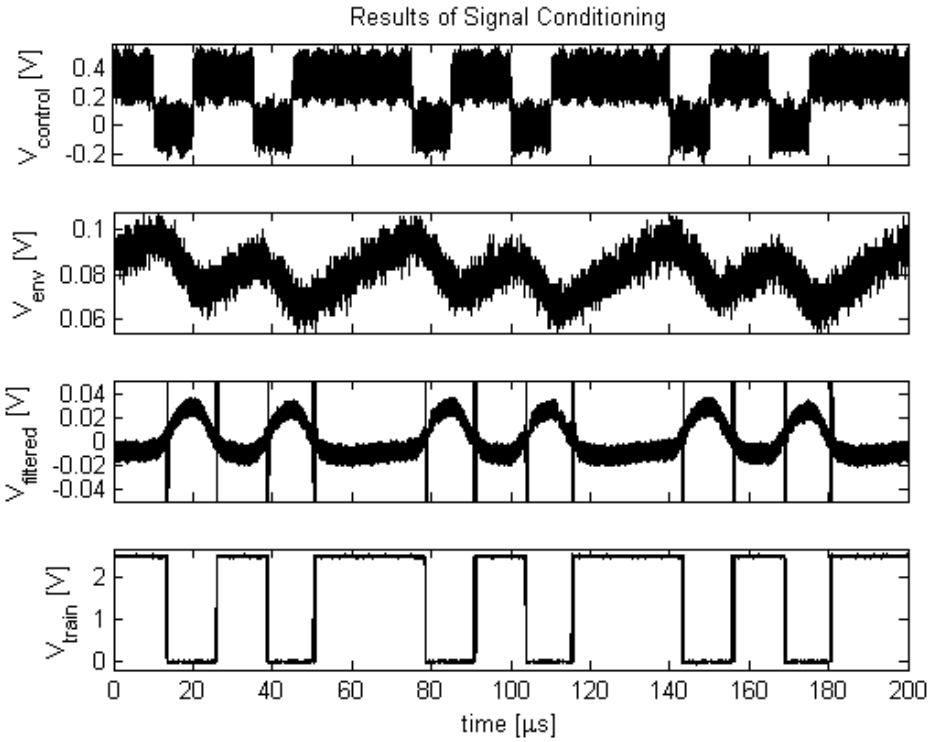


**Figure A.4**. Pulse train recovery with a 50 nF smoothing capacitor and a 5% transmitted modulation depth.

## REFERENCES


[1] C. T. Nordhausen, E. M. Maynard, and R. A. Normann, "Single unit recording capabilities of a 100 microelectrode array," *Brain Research*, vol. 726, no. 1-2, pp. 129 – 140, 1996.

[2] N. Sokal and A. Sokal, "Class E-a new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168 – 176, Jun. 1975.

[3] W. Ko, S. Liang, and C. Fung, "Design of radio-frequency powered coils for implant instruments," *Medical and Biological Engineering and Computing*, vol. 15, pp. 634–640, 1977.

[4] P. Cong, N. Chaimanonart, W. Ko, and D. Young, "A wireless and batteryless 10-bit implantable blood pressure sensing microsystem with adaptive rf powering for real-time laboratory mice monitoring," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3631 –3644, Dec. 2009.

[5] G. Kendir, W. Liu, G. Wang, M. Sivaprakasam, R. Bashirullah, M. Humayun, and J. Weiland, "An optimal design methodology for inductive power link with class-E amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 5, pp. 857 – 866, May 2005.

[6] M. Baker and R. Sarpeshkar, "Feedback analysis and design of RF power links for low-power bionic systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 28 –38, Mar. 2007.

[7] P. Troyk and M. Schwan, "Closed-loop class E transcutaneous power and data link for microimplants," *IEEE Trans. Biomed. Eng.*, vol. 39, no. 6, pp. 589 –599, Jun. 1992.

[8] B. Ziaie, S. Rose, M. Nardin, and K. Najafi, "A self-oscillating detuning-insensitive class-E transmitter for implantable microsystems," *IEEE Trans. Biomed. Eng.*, vol. 48, no. 3, pp. 397 –400, Mar. 2001.

[9] C.-C. Wang, Y.-H. Hsueh, Y.-T. Hsiao, U. F. Chio, C.-C. Huang, and P.-L. Liu, "An implantable neural interface micro-stimulator chip with external controllability," in *Proc. 2004 IEEE Asia-Pacific Conf. Adv. Sys. Integ. Circuits 2004*, Aug. 2004, pp. 356 – 359.

[10] N. Neihart and R. Harrison, "Micropower circuits for bidirectional wireless telemetry in neural recording applications," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 11, pp. 1950 –1959, Nov. 2005.

[11] B. Smith, Z. Tang, M. Johnson, S. Pourmehdi, M. Gazdik, J. Buckett, and P. Peckham, "An externally powered, multichannel, implantable stimulator-telemeter for control of paralyzed muscle," *IEEE Trans. Biomed. Eng.*, vol. 45, no. 4, pp. 463 –475, Apr. 1998.

[12] M. Ghovanloo and K. Najafi, "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 12, pp. 2374–2383, Dec. 2004.

[13] P. Troyk and G. DeMichele, "Inductively-coupled power and data link for neural prostheses using a class-E oscillator and FSK modulation," in *Proc. IEEE 25th EMBS Conf.*, vol. 4, Sep. 2003, pp. 3376 – 3379 Vol.4.

[14] M. Ghovanloo and S. Atluri, "A wide-band power-efficient inductive wireless link for implantable microelectronic devices using multiple carriers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 2211 –2221, Oct. 2007.

[15] L. Jung, P. Byrnes-Preston, R. Hessler, T. Lehmann, G. Suaning, and N. Lovell, "A dual band wireless power and FSK data telemetry for biomedical implants," in *Proc. 29th Ann. Int. Conf. IEEE EMBS*, Aug. 2007, pp. 6596 –6599.

[16] M. Zhou, M. Yuce, and W. Liu, "A non-coherent DPSK data receiver with interference cancellation for dual-band transcutaneous telemetries," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2003 –2012, Sep. 2008.

[17] G. Simard, M. Sawan, and D. Massicotte, "High-speed OQPSK and efficient power transfer through inductive link for biomedical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 192 –200, Jun. 2010.

[18] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123 –133, Jan. 2007.

[19] R. Harrison, R. Kier, C. Chestek, V. Gilja, P. Nuyujukian, S. Ryu, B. Greger, F. Solzbacher, and K. Shenoy, "Wireless neural recording with single low-power integrated circuit," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 322 –329, Aug. 2009.

[20] R. Harrison, "Designing efficient inductive power links for implantable devices," in *Proc. 2007 IEEE Int. Symp. Circuits Syst. (ISCAS 2007)*, May 2007, pp. 2080 –2083.

[21] G. Kendir, W. Liu, G. Wang, M. Sivaprakasam, R. Bashirullah, M. Humayun, and J. Weiland, "An optimal design methodology for inductive power link with class-E amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 5, pp. 857 – 866, May 2005.

[22] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits.* Cambridge University Press, 2003.

[23] M. Ghovanloo and K. Najafi, "Fully integrated wideband high-current rectifiers for inductively powered devices," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1976 – 1984, Nov. 2004.

[24] N. Neihart, "Circuits for transcutaneous power and data transfer," Master's thesis, University of Utah, 2004.

[25] D. Black, "A power, clock, and data recovery system for fully-implantable neural recording devices," Master's thesis, University of Utah, 2006.

[26] B. Razavi, *Design of Analog CMOS Integrated Circuits.* McGraw Hill Higher Education, 2001.

[27] P. Allen and D. R. Holberg, *MOS Analog Circuit Design.* Oxford University Press, 2002.

[28] D. Black and R. Harrison, "Power, clock, and data recovery in a wireless neural recording device," in *Proc. 2006 IEEE Int. Symp. Circuits Syst. (ISCAS 2006)*, 2006, pp. 4 pp. –5086.

[29] R. W. Hamming, "Error detecting and error correcting codes," *Bell System Technical Journal*, April 1950.

[30] W. C. Huffman and V. Pless, *Fundamentals of Error-Control Codes.* Cambridge University Press, 2003.

[31] S. Lin, *Error Control Coding: Fundamentals and Applications.* Prentice-Hall, Inc., 1983.