ULTRAFAST NANOELECTROMECHANICAL SWITCHES

FOR VLSI POWER MANAGEMENT

by

Sri Ramya Venumbaka

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STATEMENT OF THESIS APPROVAL

The thesis of **Sri Ramya Venumbaka**

has been approved by the following supervisory committee members:

Massood Tabib-Azar	, Chair	**08/18/2010** Date Approved
Carlos H. Mastrangelo	, Member	**08/18/2010** Date Approved
Hanseup Kim	, Member	**08/18/2010** Date Approved

and by **Gianluca Lazzi** , Chair of

the Department of **Electrical and Computer Engineering**

and by Charles A.Wight, Dean of The Graduate School.

ABSTRACT

Power consumption is a major concern in the present chip design industry. Complementary Metal Oxide Semiconductor (CMOS) technology scaling has led to an exponential increase in the leakage power. The excessive power dissipation can result in more heat generation, which in turn increases the temperature. According to Intel's source, power density increased to a value of 1000 W/cm^2 and is approaching the value which is equal to the radiation from the sun's surface (10000 W/cm^2). This leads to reliability issues in nanometer-scale CMOS as Silicon starts melting at 1687K. To resolve this issue, we introduce a novel architecture to design nanoelectromechanical switches and implementation results with virtually zero leakage current, ~1 V operation voltage, ~1 GHz resonant frequency and nanometer-scale footprint. Microelectromechanical Switches (MEMS) have very low "on" and very high "off" resistances. Their switching voltages are usually high (5-50 V), switching speeds are usually low (1 MHz) and their footprints tend to be very large (many um^2). We have designed and fabricated devices with very low actuation voltages and very high speed using tuning fork geometry compatible with conventional CMOS fabrication technologies. This unique switch geometry decreases the actuation voltage by a factor of 1.4 and doubles the switching speed. It consists of a cantilever beam that acts as a ground plane. Upon actuation, both the ground plane and the switch's main beam move towards each other that makes the center of mass stationary during switching and thus, the switching speed doubles.

These tuning fork nanoelectromechanical switches can be readily implemented in Very Large Scale Integration (VLSI) circuits to manage leakage power. The thesis will describe the Nanoelectromechanical systems (NEMS) structures, their characteristics, leakage reduction techniques, reliability of the devices and piezo actuator structures to determine contact resistance and longevity of switches.

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CHAPTER 1

INTRODUCTION

1.1 History of Mechanical Switches, MEMS and NEMS

Various technologies of miniaturization are the driving forces behind Microelectromechanical Systems (MEMS) and Nanoelectromechanical Systems (NEMS). The art of miniaturization has been a design endeavor since the 13th century when watch makers tried to minimize the size of a watch. There has always been an interest to examine matter at a micro scale which was always the factor of motivation behind the invention of electron microscopes. With the compound microscope that was invented in the 1600s, it was possible to observe microbes, objects at macro scale. The later invention of electron microscopes enabled us to observe the objects at molecular and atomic scale. The invention of a transistor turned out to be a revolutionary factor in the electronics industry. Miniaturization of a transistor is one of the success stories. They are being made smaller and smaller to reduce the size of gadgets and electronic devices. Today's integrated circuits have transistors of 0.18 microns. The size of the transistor is approaching 10 nanometers in research laboratories. Scaling down the size of electronic devices has opened a new era of microdevices. This is currently paving the way for designing nanodevices. Improving the characteristics along with miniaturization is the most important buzz word in the present electronics industry.

1.2 The Scale of Electronic Systems

Present Very Large Scale Integration (VLSI) and semiconductor technologies are using 32 nanometer scales for most of the devices, which is almost several thousand times smaller than the diameter of human hair. Micro- and nanotechnologies differ from the perspective of processing. The microsystems rely on top-down fabrication whereas nanosystems rely on bottom-up fabrication using a self-assembly process [1]. Micro- and nanoelectromechanical systems open up a new perspective of controlling the miniature devices. These technologies integrate the mechanical elements like sensors, cantilevers and actuators that analyze the environment with electronic circuitry to control the devices. Fig. 1.1 is an example of particles like drive gear chain and linkages, pollen grain and blood cells that demonstrate the scale. Various elements of nanometer range are shown in Fig. 1.2.

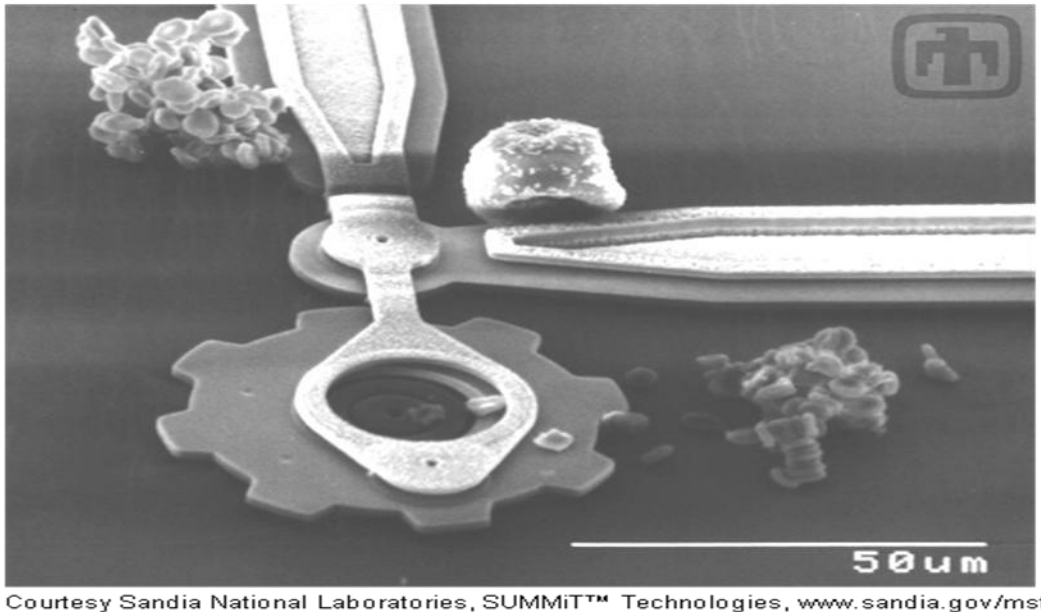

Figure 1.1 Drive gear chain and linkages, with a grain of pollen (top right) and coagulated blood cells (lower right, top left) to demonstrate scale

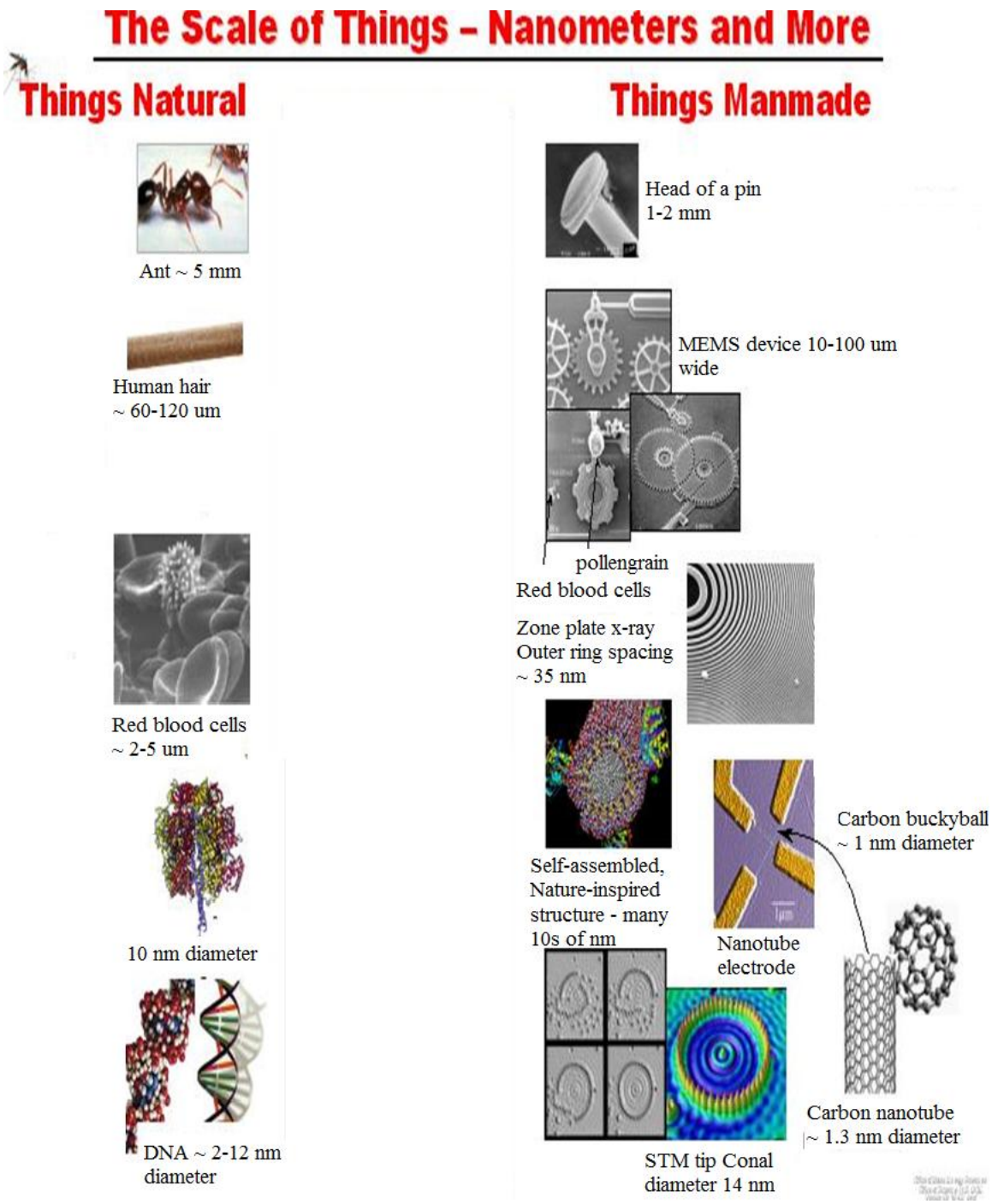

Figure 1.2 The scale of things
Courtesy Office of Basic Energy Sciences, Office of Science, U.S. Department of Energy

MEMS and NEMS technologies open up a new perspective of controlling miniature devices. They combine the mechanical elements such as sensors, cantilevers and actuators. There are some limitations in producing the minidevices capable of performing tasks using conventional technologies. MEMS-NEMS technologies turn out to be a possible solution for those limitations. They combine electrical properties with mechanical components at micro- and nanoscale. Various behaviors and properties of these structures are yet to be explored and exploited in the case of NEMS technology.

1.3 Definitions and Terms

1.3.1 MEMS and Microtechnology

MEMS, also known as Microelectromechanical Systems, can be defined as the technology of very small mechanical devices driven by electricity. They refer to devices that have characteristic length in the range of microns and are formed by the integration of electrical and mechanical components. They are fabricated using integrated circuit batch-processing technologies. They are essentially miniature devices that use a mechanical movement to achieve a short circuit or an open circuit in a transmission line [2].

Dr. Richard Feynman, a Nobel Laureate physicist, is considered the father of today's MEMS and NEMS based on his inspirational lecture, "There is Plenty of Room at the Bottom," delivered at the annual meeting of the American Physical Society, Pasadena, California, December 1959 [3]. Here is a statement from his lecture:

> How many times when you are working on something frustratingly tiny, like your wife's wrist watch, have you said to yourself, "If I could only train an ant to do this!" What I would like to suggest is the possibility of training an ant to train a mite to do this. What are the possibilities of small but movable machines? They may or may not be useful but they surely would be fun to make.

He stated that new applications would emerge as the behavior of matter is different at atomic scale and conventional bulk scale. He expressed his doubts on the advantages of devices at atomic scale. Even so, MEMS and NEMS devices are finding a wide variety of applications in the present chip design industry with a potential market value in the billions of dollars worldwide. There are various factors that led to the rapid development of microelectromechanical devices. These factors include the invention of the transistor, the rapid scaling down of its size consistent with Moore's law, the discovery of piezoelectricity in semiconductors and the discovery of silicon as a visible material for micromachining.

In terms of commercial success, microsensors proved to be of great value. The commercial success resulted in the development of various pressure sensors, strain gauges, accelerometers and gyroscopes. Conventional accelerometers that are used for crash air bag deployment systems in automobiles have several limitations in terms of speed, weight and size. Cost is also a major factor as it is high. MEMS accelerometers turned out to be a great alternative with small size, less weight, more reliability and multiple functionality. Cost also turned out to be less by at least 10 times that of conventional macroscale accelerometers.

Another important section of MEMS that has rapidly developed is the optical MEMS device design. These devices include bar code readers and fiber optic telecommunication cables that make use of wide band gap materials and ceramics. The Digital Light Processor (DLP), which is used for projection displays, is the best example of an optical MEMS device that is successful in a commercial way. It is developed by

Texas Instruments [4]. Deformable mirrors are the MEMS devices that can be used to enhance imaging in the retina of the eye.

MEMS device accelerometers find a major application in computer hard drives. They are used to sense the rapid motion of the head. They avoid the damage of the surface during a fall by parking the head during rapid motion. It is the MEMS accelerometer that automatically rotates the display of an iPhone when the user rotates it.

1.3.2 Biomedical Applications of MEMS

MEMS devices have revolutionized the field of biomedical applications. These include complex procedures like drug delivery and implants [1]. There are various advantages of using MEMS like small size, lower cost, simple surgical procedures, less number of test samples needed, high diagnosis speed and fast patient recovery time. MEMS pumps can be used to infuse insulin for diabetes patients and its small size enables patients to have it directly on the skin to analyze glucose levels. They are used for DNA testing, drug delivery and blood testing. We also have MEMS implants, to replace the retina and eardrum. Purdue researchers made a detector to identify the mass of a single virus particle using microresonators with nanoscale thickness. The device vibrates at its natural frequency. Frequency changes when a virus particle falls on its cantilever beams. Cantilever beams are coated with antibodies that attract virus particles in order to create detectors to particular pathogens.

1.3.3 NEMS and Nanotechnology

A nanometer is a billionth of a meter. The diameter of human hair is approximately 100000 nanometers and that of a red blood cell is around 10000 nanometers. Nanotechnology is nothing but dealing with devices at the nanometer (10^{-9}) scale. Nanotechnology uses conventional device physics along with new approaches like molecular self-assembly to make new devices within the scale of nanometers [1].

The elements, carbon and silicon, share the same periodic column. Carbon is playing a major role in nanotechnology as it can form strong and stable covalent bonds. It has a property of existing in various physical forms based on the size/length of carbon chains. It exists in the form of a gas in short chains, as liquid in medium chains and as plastic in long chains.

Carbon nanotubes are allotropes of carbon with a cylindrical nanostructure. Various types of carbon nanotubes comprise single-walled, multiple-walled and nanobud structures. Carbon nanotubes are known for their properties of directional stiffness and strains. There are various applications such as nanotweezers, memory devices, super sensitive sensors and tunable oscillators.

1.3.4 Nanofabrication

Micro- and nanofabrication technologies are used to integrate mechanical devices, sensors and electronics in micro- and nanoscale on a common Silicon substrate. The electronics components are manufactured using integrated circuits (IC) process sequences while the micromechanical components are fabricated using compatible micromachining processes. Micromachining enables one to etch away parts of a silicon wafer or add new structural layers to form the electromechanical device. These devices are generally used

to analyze the environmental conditions, that is, to sense, collect data and produce a signal to make desired changes to the environment. Various fabrication methods are being implemented for making devices at micro- and nanoscale. The methods commonly used are described below:

(i). AC Electrophoresis: Cantilever structures are fabricated using this process by inducing charge in tubes for electromechanical switching. An electric field is created using ac current, which can be used to make a proper contact with cantilevers.

(ii). Electrostatic Manipulation: This process makes use of a Scanning Tunnel Microscope (STM) to make atoms slide/suspend by electrostatic forces in a proper arrangement. This process is complicated as it is time consuming and requires special conditions to prevent sliding of atoms out of place.

(iii). Pattern Electron Beam Lithography: It is the practice of scanning a beam of electrons in a patterned fashion across a surface covered with a film called the resist [5]. It is used to create very small structures in the resist by etching. The primary advantage of this is that it overcomes the limit of diffraction of light.

(iv). Dip Pen Lithography: It is another way of depositing a layer of material on a surface using an atomic force microscope (AFM) probe tip. It is just like writing on paper using a pen. Biosensors fabrication uses this sort of technology to draw a pattern on a surface.

(v). Self Assembly: It is a process of forming an organized structure or pattern from a disordered system of pre-existing components. Various examples of self-assembly comprise snowflakes, salt crystals and soap bubbles. It also gained prominence because of low cost efficient manufacturing processes.

Various modifications are being implemented to improve the manufacturing process of these micro- and nanodevices.

1.4 Merging of Technologies

Present technologies are dealing with the devices in nanoscale. It is an emerging field that uses MEMS as a bridge to enable the applications like biosensors.

1.5 Impact of MEMS and NEMS

MEMS and NEMS technologies are having a tremendous impact on our lives. These emerging technologies are opening up new career opportunities in various fields like semiconductors and biological areas. Fabrication of MEMS and NEMS involve new methods that are different from semiconductor manufacturing methods. It is therefore opening up new teaching and manufacturing jobs. The biological and optical applications are new emerging areas in the fields of MEMS and NEMS technologies. Research in these fields is being encouraged by universities and government by providing funds to design new products. They are advantageous due to less weight, durability and more efficiency.

On the other hand, NEMS technology needs to be properly and carefully explored as carbon-based NEMS may be toxic. NEMS may contain heavy metals that damage the body's immune system. Therefore, it is required to explore the dangers of nanotechnology by doing more research and higher investments.

The field of electronics witnessed a new revolution by semiconductors in the 20^{th} century. Similarly, there is a chance to witness another revolution through MEMS and NEMS technologies. The research that is going on in these fields is expanding at a fast

pace. Increase in the number of programs and centers that are working on MEMS and NEMS itself proves the pace at which they are developing. There are at least 40 centers in the US and hundreds all over the world [1]. There are also a significant number of patents of around 10,000. These technologies serve almost all industries like aerospace, information technology, automotive, defense, medical and telecommunications. The complexity involved in these technologies is demanding intensive research, engineering and technological developments.

Reliability of the products and packaging are the major challenges. Designing, testing and predicting the behavior of MEMS and NEMS require proper computational models. Intense efforts are required to make the manufacturing of all these NEMS devices more reliable as it is more promising in our nanoscaled futures.

1.6 Functional Classification

Electromechanical systems are classified into three types [1] -

- Conventional electromechanical systems
- Microelectromechanical systems (MEMS)
- Nanoelectromechanical systems (NEMS).

The behavior of the first two systems can be analyzed by classical mechanics and electromagnetism. An in-depth analysis of the behavior and parameters of NEMS switches requires various disciplines like classical mechanics and quantum physics. General analysis of actuation voltage and switching speed are described in this work.

Fig. 1.3 describes the classification of electromechanical systems.

1.7 Motivation

1.7.1 Increase in the Demand

Moore's Law states that the transistor density on integrated circuits doubles every two years. Today, adding transistors on pace with Moore's Law continues to drive increased functionality, performance and decreased cost of computing and communications technology. With the continuous research going on in the field of computing and communications, there is a greater demand for improving more functionality and speed as well as reducing the costs. Moore's law is to be followed to design the devices that satisfy all the requirements mentioned above. Thus, the electronics industries are trying to make devices according to Moore's law and at the same time, they are making sure to meet all the demands. The number of transistors that are being integrated on a single chip is increasing to enable high functionality. This increases the frequency to ensure higher

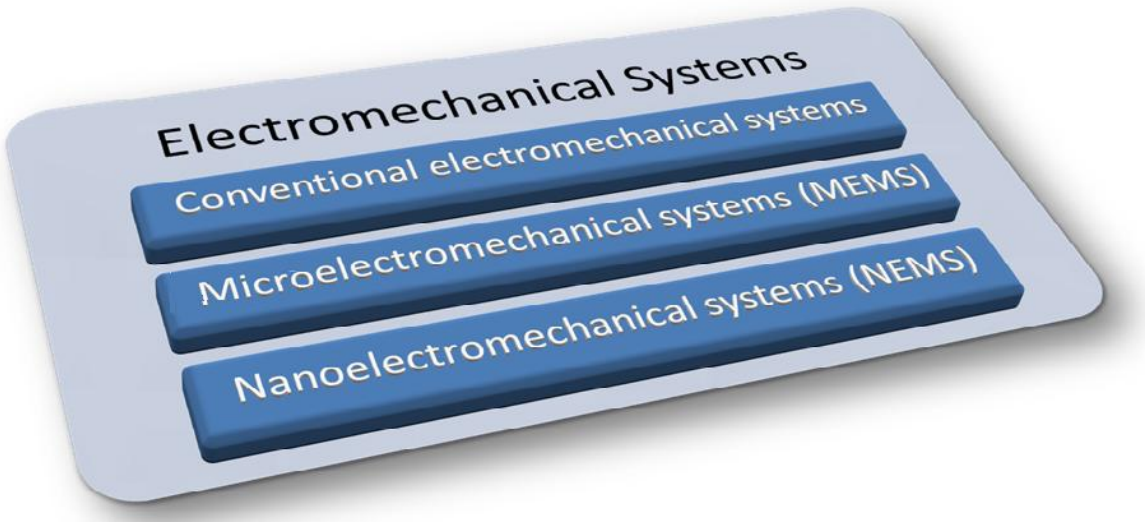

Figure 1.3 Electromechanical systems functional block diagram

performance. As a result, power dissipation increases and due to higher integration of transistors, power density also increases. The demand for high functionality and speed is resulting in various challenges like power consumption.

1.7.2 Power Consumption

Efficient power and thermal management are vital as systems become smaller or more capable with every generation of Moore's Law. Power must be delivered and used efficiently by the chips, wiring and display, while effectively dissipating heat from the system –economically, of course. Addressing the power challenge allows a continuation of the trend toward smaller, faster, cost effective chips and devices. As a result, futuristic applications that require more powerful processors may be realized. Increasing capability and density of computing and communications chips may be sustained. Comprehensive power and thermal management techniques are a fundamental part of continuing to receive the benefits of Moore's Law.

The growth of microelectronics over the last 40 years, from the first successful large scale integration (LSI) of microprocessor and memory chips to the present very large scale integration (VLSI), has been truly spectacular. The key to this growth has been the drive to much smaller dimensions using the principles of scaling introduced in the early 1970s. The basic idea of scaling is to reduce the dimensions of the MOS transistors and the wires connecting them in integrated circuits.

High computation speed, large data storage and fast information processing are the most important considerations of the present chip design technologies. Complementary Metal Oxide Semiconductor (CMOS) technology scaling has tremendously improved the speed by reducing switching delay and power while

improving area density. But scaling down the size of the transistor resulted in various technological challenges, among which leakage power is of highest priority in modern chip design industry. Modern high performance microprocessors show drastic increase in leakage power with CMOS technology scaling, which can be clearly seen from Fig. 1.4. Due to short channel effects, subthreshold leakage and hot carriers injection, the power dissipation increased dramatically in the sub-100 nm CMOS technology. Various factors of power dissipation comprise the intradie and interdie process and thermal variations. It is predicted that the leakage power constitutes nearly 50% of the total chip power beyond 65 nm CMOS technology. This barrier of exponential increase in leakage power is clearly a major concern in memory systems and it also decreases robustness of read/write operations. Fig. 1.5 clearly depicts the increase in the power density over years as the devices are being scaled down. Power dissipation may approximately approach the power density radiated by the sun's surface over years, according to Intel.

Mobile embedded systems and their applications are demanding devices that promise limited power dissipation, which is allowable. The devices with heat removal are more advantageous. International Roadmap for Semiconductors (ITRS) is predicting CMOS devices beyond 22 nm by the end of 2015 [6]. Most likely, they are suggesting a physical gate length of 10 nm, which leads to a power dissipation of 93 Wcm^{-2} approximately. Reduction of power dissipation requires complete transformation from pure downscaling to new combined functionality and innovations. Research is being done to explore devices that are compatible with CMOS technology.

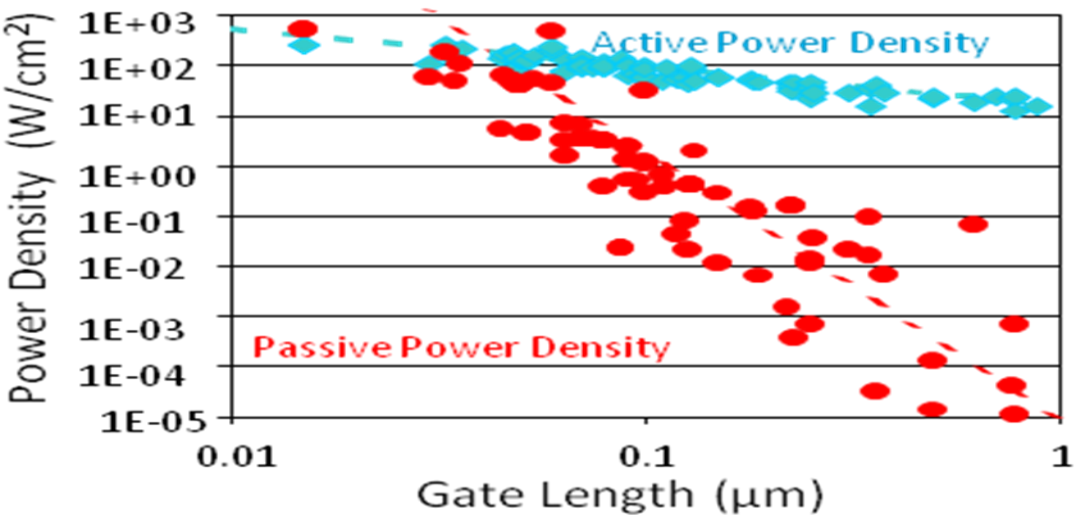

Figure 1.4 Power density vs. gate length of transistors
Source: B. Meyerson (IBM) Semi co Conf., January 2004.

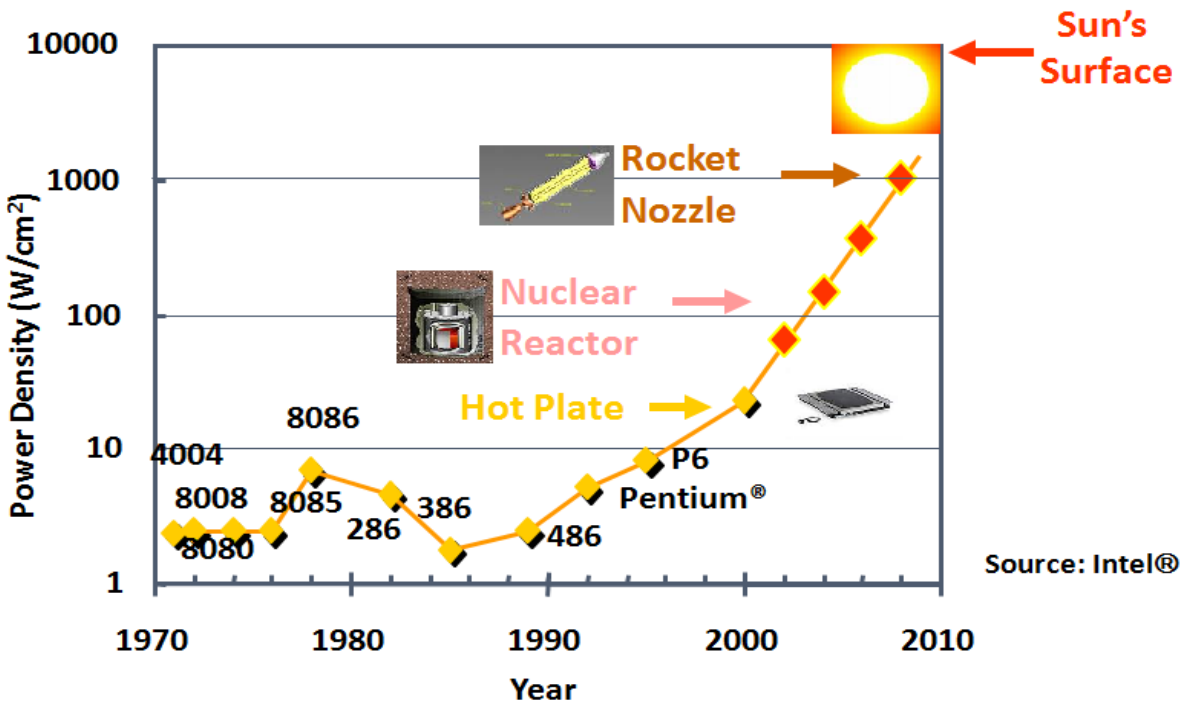

Figure 1.5 Increase in the power density over years

Such devices demand high manufacturing cost as well as design methods. The most beneficial way of exploring these devices is to make a new device using conventional CMOS-VLSI fabrication procedures without complicated manufacturing methods. Use of conventional CMOS design methods and architectural styles for making novel devices reduces overhead to a large extent.

1.8. Types of Switches and Their Comparison

A switch is a basic building block of any electronic circuit. It can be considered as a simple contact that can make or break a circuit. The contact is defined by two metals that when they touch each other, the switch is said to be closed which allows current to flow through it. The switch is said to be open when the metals do not touch each other. The broken circuit implies that the current flowing through the switch is zero. Miniaturization also paved the way to design switches as tiny as possible.

There have been drastic improvements in the size, design and fabrication of switches with technology scaling. Mechanical switches are large in size and operating speed is low because of the mechanical movement involved. Electromechanical switches have the advantages of improved speed. This is because of the electrostatic forces that are responsible for switching. Technology scaling has led to the design of switches at micro- and nanoscale. Decreases in the size of devices resulted in higher performance in terms of speed and computation capabilities. Scaling down the size of devices, however led to an increase in power consumption at micro- and nanolevels. Various types of nanoelectromechanical switches are manufactured. Some of them are based on carbon nanotubes. They help in the reduction of cell and bit line leakages in logic and memory switches. We introduce a novel switch at nanoscale with tuning fork geometry, which

reduces the actuation voltage by a factor of 1.4 and doubles the speed. Their switching characteristics and leakage reduction techniques are discussed in the next chapters.

CHAPTER 2

LITERATURE SURVEY- CONTACT MATERIALS FOR NEMS

2.1 Contact Plating

Contact plating as well as sealing is the most important process in the manufacture of reed switches. The quality of contact plating determines the contact characteristics of the reed switch.

2.2 Materials for Contact Plating

In ordinary reed switches, gold is plated onto 52-alloy as a ground layer, and rhodium or ruthenium in some cases is plated on the ground layer [7].

2.2.1 Ground Plating

Gold is usually plated as a ground layer. There are two kinds of gold-plating solutions: pure gold and cyanic. The pure gold type is in popular use. Gold striking is performed before gold plating in many cases. Gold striking may be necessary to attain secure adhesion. If the required adhesion and other characteristics can be attained by gold plating only, gold striking can be omitted.

Recently, palladium has been attracting attention as an alternative to gold. The density of palladium is about 60% that of gold and so the weight of palladium is about 40% less than that of gold plating for the same plating thickness. Moreover, the cost of palladium is about one-third that of gold. This reduces the cost of ground plating

considerably. It is also advantageous in terms of performance because of the high melting point and hardness twice that of gold.

2.2.2 Rhodium Plating

Rhodium is now used most commonly as a contact material for reed switches. Rhodium has a high melting point and hardness, and has excellent abrasion resistance, resistance against sticking and corrosion resistance. At present, the primary matter concerning rhodium is cost. For avoiding this problem of cost, ruthenium as an alternative to rhodium seems to be more feasible.

2.2.3 Ruthenium Plating

The atomic number of ruthenium is 44, adjacent to rhodium, with an atomic number of 45, in the periodic table. Ruthenium has a higher melting point and hardness and better abrasion resistance, resistance against sticking and corrosion resistance than rhodium. Less ruthenium is produced than rhodium, but its price is extremely low because it is unfit for ornaments as a result of poor gloss due to the low reflectance of visible rays. As for technical problems, the problem of cracks in plated layers is the most serious one. Crack-free rhodium plating as thick as up to 10 um is now possible because of the development of an excellent stress releasing agent and the establishment of an optimum clearing system. Regarding performance, the thin plating of ruthenium has life several times that of rhodium at low-intermediate loads. It does not require the surface deactivation treatment after plating because a thin, stable oxide film is formed on the plated surface. One of the attempts to increase the plating thickness of ruthenium is alloy plating which uses rhodium containing about 10% ruthenium.

2.2.4 Copper Plating

Nonmagnetization is attained by plating a contact with copper. This copper plating is complex as it involves the optimum selection of copper-plating solution, diffusion treatment, and frequent gold striking. But this plating results in stable contact characteristics. In the initial stages, heat in surface treatment and sealing caused problems in copper plating. At present, copper plating is free of problems and provides stable contact properties.

2.2.5 Tungsten Plating

The melting point of tungsten is much higher than that of rhodium and ruthenium. Therefore, tungsten turns out to be a very useful contact material for switches. It is plated by chemical vapor deposition (CVD). The advantages of this plating are excellent abrasion resistance and resistance against sticking. The problem with this plating is that it oxidizes in air, leading to high contact resistance in the initial stages. It is solved by surface treatment after CVD [7].

2.2.6 Rhenium Plating

Rhenium also has a high melting point like that of tungsten. Rhenium plating requires a three-layer structure of Re-Au-Re to suppress metal transfer caused by a molten metal bridge when the contacts begin to open.

There are various factors to be considered before selecting a suitable material to fabricate NEMS switches. They include melting point, resistivity, Young's modulus and various other factors that determine the contact characteristics of the devices. Fig. 2.1 is the plot of melting points and resistivity of various materials with the exact values in Table 2.1. Similarly, Fig. 2.2 and Table 2.2 include melting points and Young's modulus.

2.3 Criteria for Material Selection

There are different criteria to be considered while selecting the materials for making nanoelectromechanical switches. These criteria include melting points, resistivity and Young's modulus. The following Figures 2.1 and 2.2 and corresponding Tables 2.1 and 2.2 demonstrate the factors of various materials suitable for making switches. The conditions suitable for making switches would be low melting point, high resistivity and high Young's modulus.

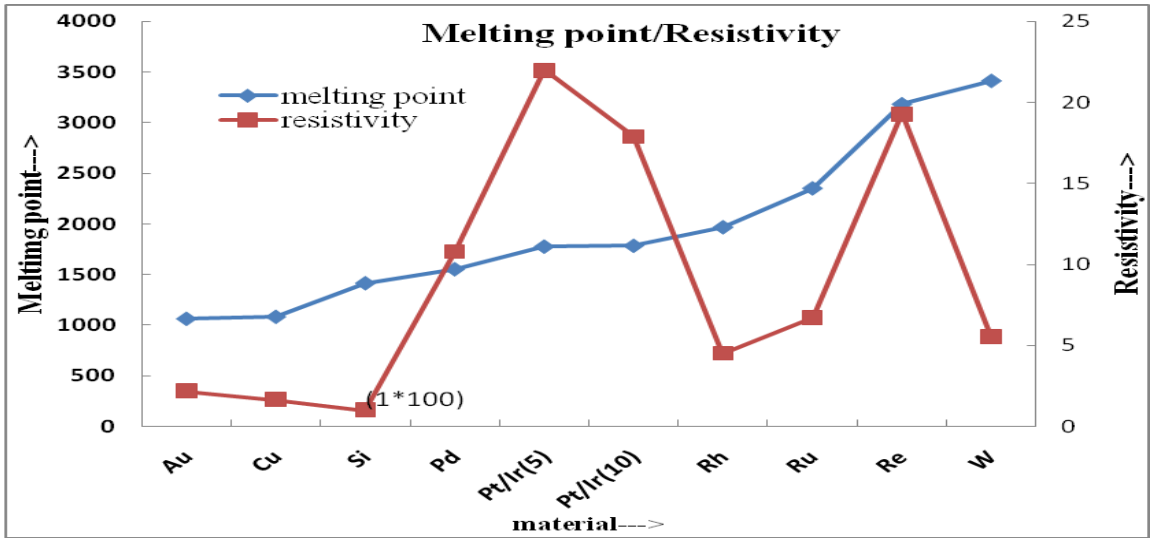

Figure 2.1 Melting point and resistivity of various materials

Table 2.1 Melting point and resistivity of various materials

Material	Melting point©	Resistivity (uohm cm)
gold	1063	2.19
copper	1083	1.65
silicon (n-type)	1414	100
palladium	1552	10.8
platinum/iridium alloy(5/10)	1775/1783	22/17.9
rhodium	1966	4.51
ruthenium	2350	6.71
rhenium	3180	19.3
tungsten	3410	5.55

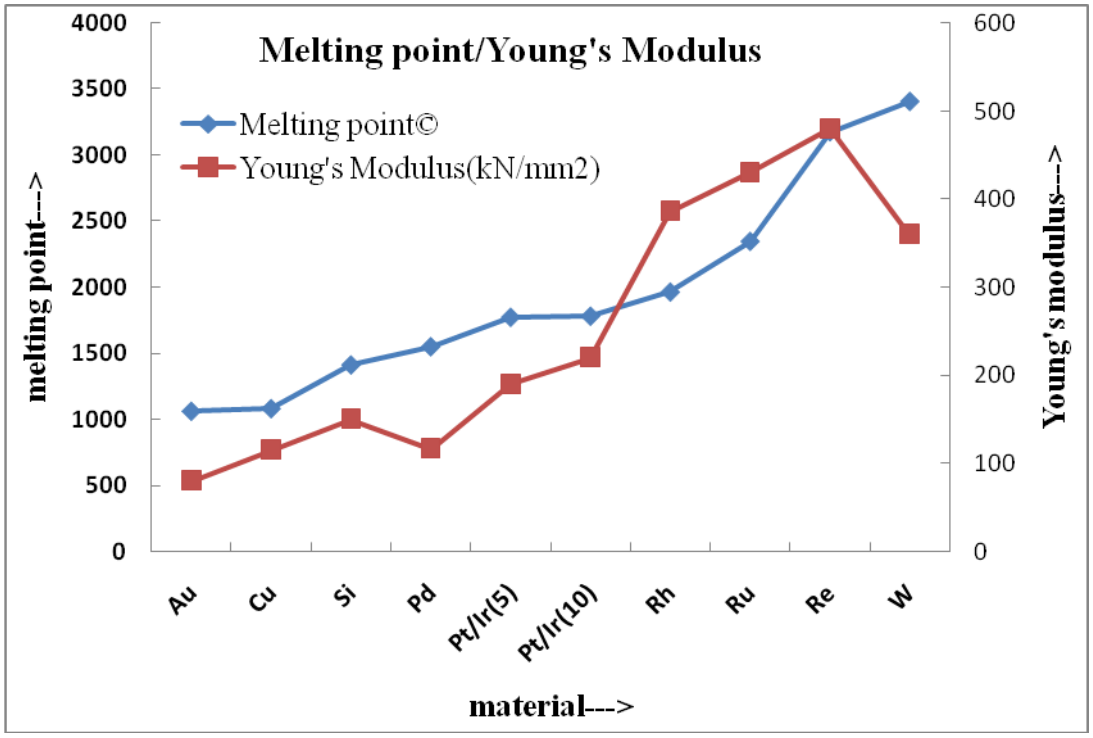

Figure 2.2 Melting point and Young's modulus of various materials

Table 2.2 Melting point and Young's Modulus of various materials

Material	Melting point©	Young's Modulus (kN/mm2)
gold	1063	80
copper	1083	115
silicon (n-type)	1414	150
palladium	1552	117
platinum/iridium alloy (5)	1775	190
platinum/iridium alloy (10)	1783	220
rhodium	1966	386
ruthenium	2350	430
rhenium	3180	480
tungsten	3410	360

Based on all these factors, we are making switches with tungsten. The high melting point and low contact resistance are the major factors. The selection of suitable material for making switches depends on the desired characteristics such as low leakage power, high reliability or fast switching.

CHAPTER 3

CHARACTERIZATION OF NEMS

To address some of the limitations mentioned in Chapter 1, a novel nanoelectromechanical switch (NEMS) is implemented with virtually zero leakage current, very low operation voltages and fundamental resonant frequency range of the order of GHz and nanometer –scale footprint. These nanoelectromechanical switches can be dropped in and hybridized with CMOS at the metallization or device levels to manage leakage power and current. The design methods, circuits, architectures and design automation techniques from CMOS can be readily used to realize CNEMS logic gates and processors.

A novel architecture for a tuning fork NEM switch is introduced. The switch has an operating voltage range of 1-3V, 1 ns switching speed, and nanometer-scale footprint. Fig. 3.1 shows the schematic of the metallic tuning fork geometry. The tuning fork geometry, the two active cantilever beams with nanometer- footprint, and the mechanical and electrical properties of the nickel and poly-Si result in the unique characteristics of these nanoelectromechanical switches. The two cantilever beams are actuated by an electrostatic force caused by the application of voltage difference between the two cantilever beams. When this voltage difference becomes large enough (Pull-in voltage) such that it can overcome the elastic force, the two cantilever beams are attracted to each

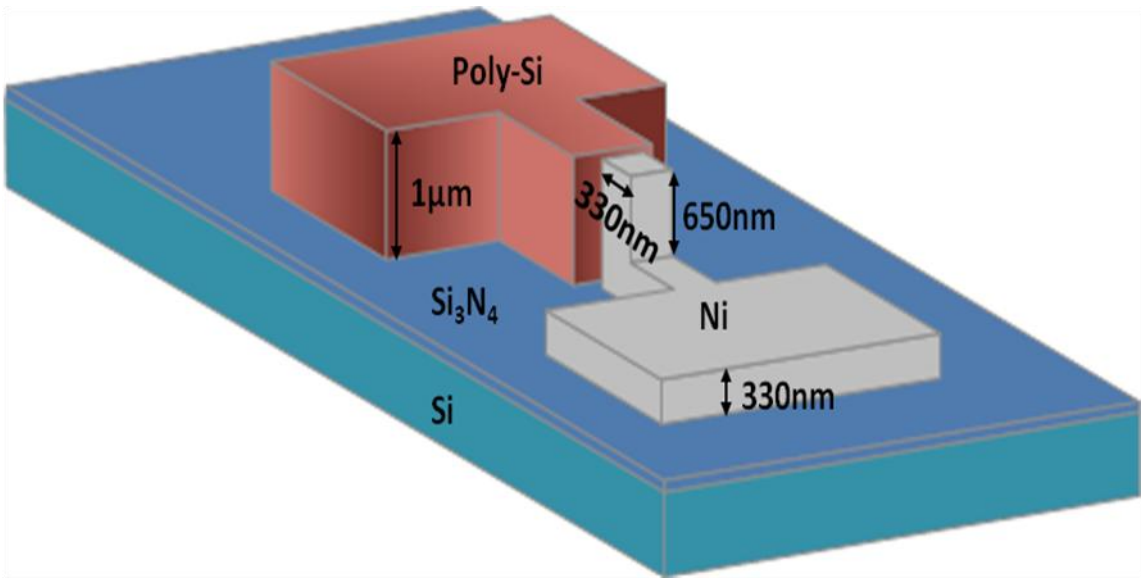

Figure 3.1 Schematic diagram of metallic nanoelectromechanical switches (NEMS) on silicon substrate

other until a critical displacement is reached. At this displacement, the two cantilever beams collapse abruptly. This causes the switch to close. When the applied voltage decreases enough (Pull-out voltage), the elastic force overcomes the electrostatic force and the other intermolecular forces, causing the switch to be opened.

NEMS switches can be considered as switches having at least two dimensions smaller than 100 nm. Some switches have been demonstrated on this scale. We developed a novel sort of NEMS switch.

3.1 Fabrication

Fig. 3.2 shows the schematic diagram of the proposed fabrication process that is used to make exquisitely well-developed metallic nanoelectromechanical switches (NEMS). The fabrication steps of Nanoelectromechanical Switches include the following:

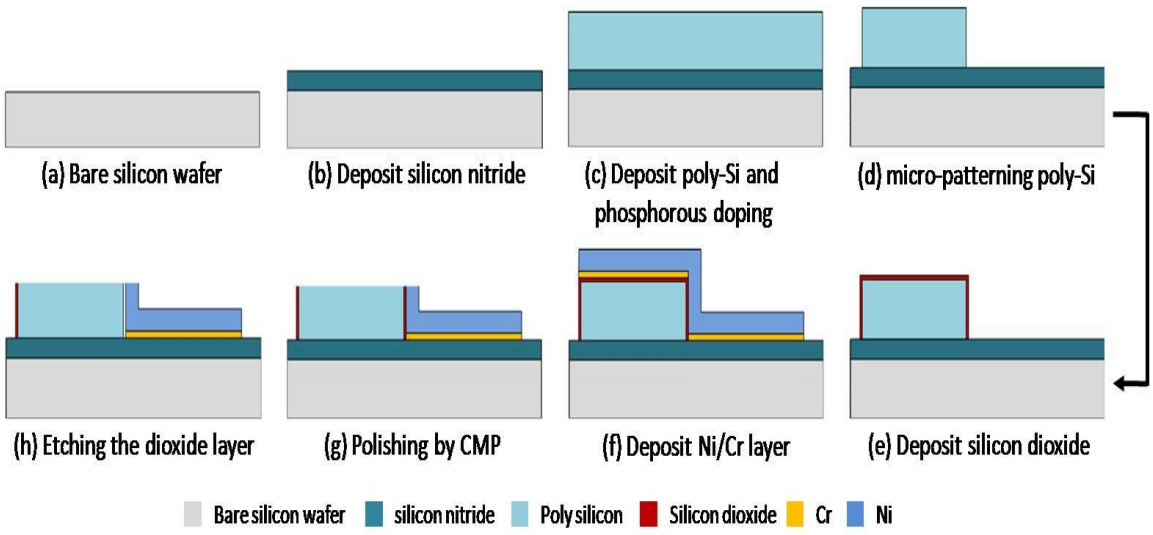

Figure 3.2 Schematic of the fabrication process for metallic nanoelectromechanical switches (NEMS) on silicon substrate

(a) Preparation of cleaned silicon wafer after RCA-1 process.

(b) The deposition of the silicon nitride film by low pressure chemical vapor deposition.

(c) The deposition of the polysilicon (Poly-Si) layer with thickness of 1.5µm on the top of the silicon nitride layer. Then, the polysilicon layer was doped by phosphorus from a TP-470 dopant source at 1050ºC.

(d) Etching at the outside of photoresist micropatterns up to the silicon nitride layer by using reactive ion etching in an inductive coupled plasma (ICP) after photolithography.

(e) Depositing the silicon dioxide layer with a thickness of 8nm on the micropatterned Poly-Si by thermal oxidation, critically.

(f) Depositing 330nm of Ni film followed by a 20nm adhesion layer of Cr by sputter (Denton, USA).

(g) Polishing the Ni-deposited wafer with FCN-560 slurry on a chemical mechanical polishing (CMP) tool (Strasbourg 6EC, USA).

(h) Etching the sacrificial oxide layer by buffered oxide etchant.

3.2 Tuning Fork NEMS Switch

Tuning fork geometry is introduced to achieve low switching voltage and high switching speed. It has advantages of the switching voltage of the range 1-3 V, switching speed ~ 1-5 ns and very low "ON" resistance.

The tuning fork structure shown in Fig. 3.3 achieves high operation frequencies because of the higher frequency of its second resonant mode (~2f0). The higher switching speed coupled with very low RC time constant associated with charging/discharging of the metallic interconnect transmission lines (feeding the RF signal to the switch) leads to a very high switching speed only limited by the "mechanical" response of the moving parts of the switch. The device geometry with a 1 nm gap minimizes the damping by air molecules that have mean free paths of ~ 1um in 1 atmosphere at room temperature. The tuning fork geometry achieves higher speed because in second resonant mode, the center of mass is stationary and the two vertical cantilever beams move against each other, as indicated in Fig. 3.4. The SEM picture of the tuning fork NEMS switch is shown in Fig. 3.5.

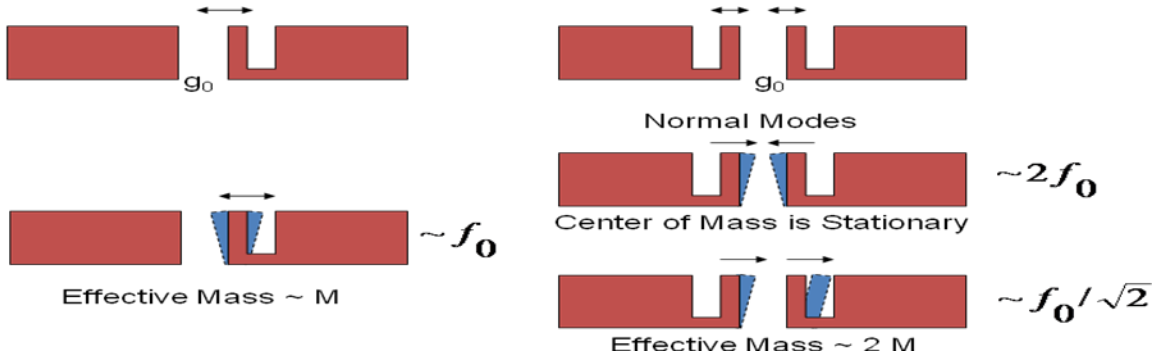

Figure 3.3 Frequency advantages of tuning fork geometry

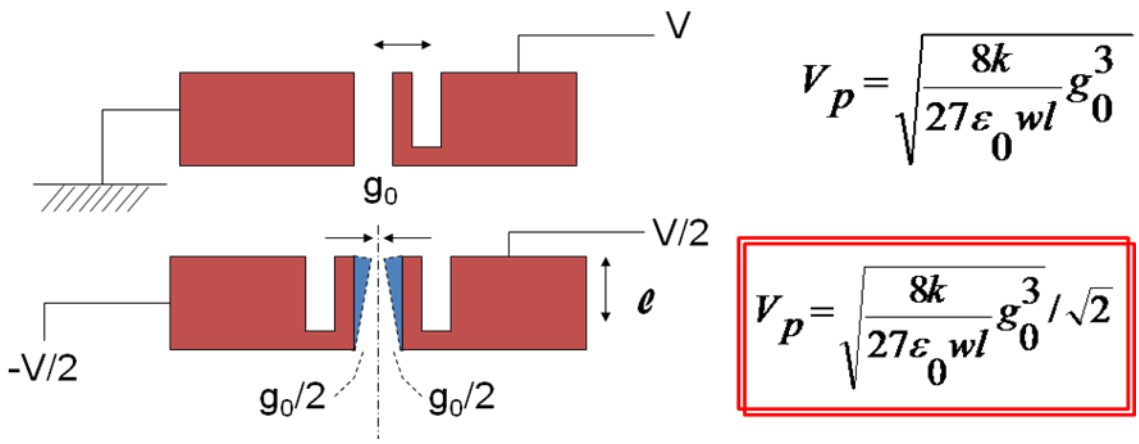

Figure 3.4 Reduction in switching voltage with tuning fork geometry

3.3 I-V Testing

Electric measurements of nanoelectromechanical switches show well-defined ON and OFF states as a DC bias up to a few volts is applied. When DC voltage is applied between the source and Ni electrode, a transient charge develops with increasing voltage. Current remains very low up to a certain voltage and increases rapidly once voltage crosses a point called switching voltage or actuation voltage. The magnitude of current increases by 4 times when the voltage exceeds the actuation value. It remains of the order of pA and rises rapidly beyond the actuation voltage. Vanderwaal forces exist between the sources and pull electrodes. These forces result in hysteresis between the increasing and decreasing bias voltage paths. This switching voltage mainly depends on the air gap between Ni and source terminals. Experiments revealed a direct relationship between switching voltage and air gap. A typical NEM switch with an air gap of 30 nm resulted in the switching voltage of 27 V, as shown in Fig. 3.6. Our main intention is to reduce the actuation voltage, to operate the switches at very low applied voltages. It can be seen from Fig. 3.7 that for an air gap of 1nm, switching voltage is around 1-2V.

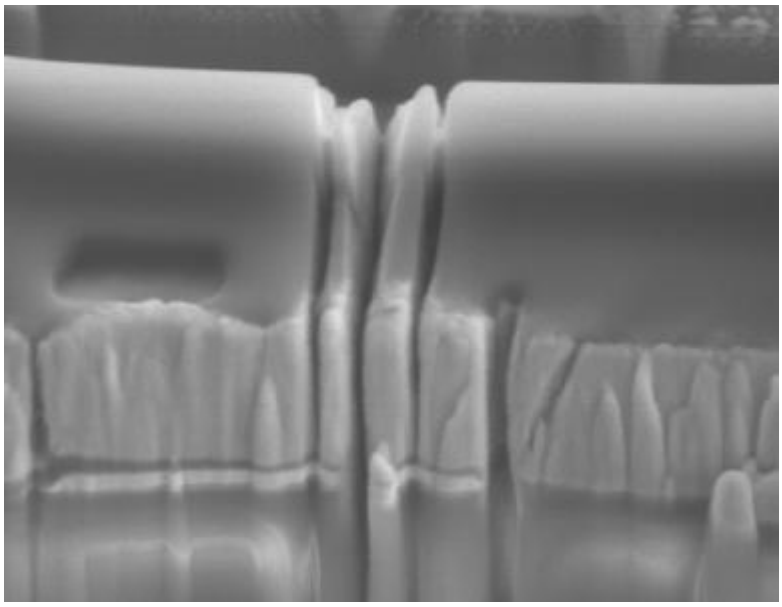

Figure 3.5 SEM picture of tuning fork NEMS

The rapidly rising current regime arises in both forward biased and reverse biased cases. Switching behavior is polarity-independent, which rules out field emission as a likely mechanism at these voltages.

Electromechanical measurements are performed to investigate the switching properties of the NEMS. The I-V characteristics of the NEMS switch are taken to measure actuation voltages. A DC voltage range of 0-3 V is applied and compliance is set to 3mA. The measurements revealed that the switching voltage is around 1-2V (1.6V specifically).

Leakage is currently one of the main factors limiting increased computer processor performance. Efforts to minimize leakage include the use of strained silicon, high-k dielectrics and stronger dopant levels in the semiconductor. It is true that new materials can reduce the leakage current, but we introduce a simple way to reduce the

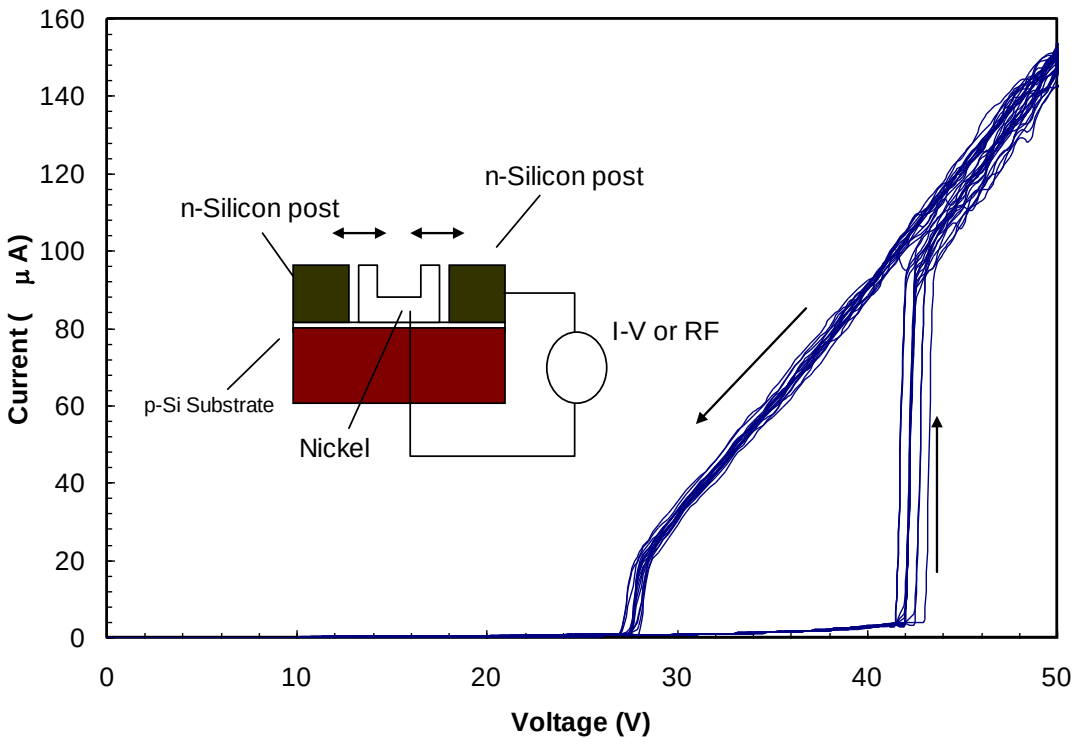

Figure 3.6 I-V characteristics of a NEMS switch with an air gap of 30 nm

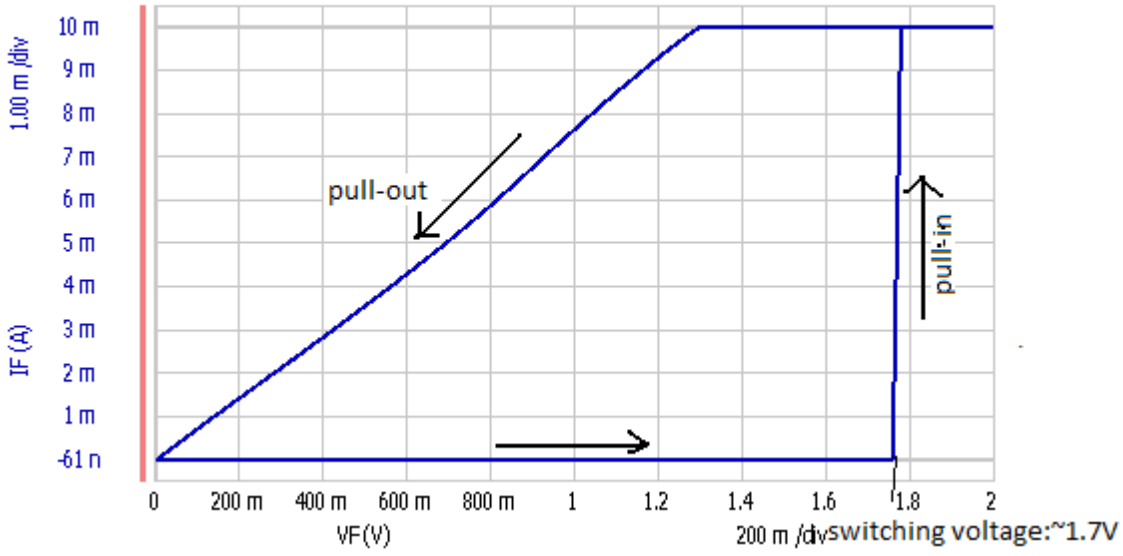

Figure 3.7 I-V characteristics of a NEMS switch with an air gap of 1 nm

leakage current by a new process, which can continue Moore's law. The simple way is to treat switches with oxygen plasma for 1 and 2 min, SF6, water and vacuum.

After the surface treatment of O_2 plasma, we found that the leakage current can be decreased, and their performance can be greatly improved. Moreover, this good status can be maintained for a long time.

Fig 3.1 shows our NEMS switch. When applying a voltage on the two electrodes, the cantilever will bend, and the switch will be turned on if the voltage is high enough. The current can be expressed by the following formula:

$$I = Ae^{V/V_0} - A + B_1V + B_2V^2 \qquad \text{Eq. (3-1)}$$

in which A, V_0, B_1 and B_2 are parameters of each switch [8]. The first two terms of this formula come from the tunneling current, and A is the so-called leakage current. We discovered that, after the O_2 plasma treatment, molecules (water, CO_2, etc.) and ions (Na^+, Cl^-, H^+, OH^-, etc.) can be cleaned to some extent, so that the characteristics of some devices can be improved. We also discovered that after several days, there may be a natural oxide layer on the surface which can protect the device from contamination again.

3.4 Leakage Reduction

In order to measure the leakage current, the voltage range is set to 0-1V and compliance to 1mA. The leakage currents of all the devices are measured with this input voltage. To reduce the leakage current, various phenomena are considered like treating the devices with oxygen plasma (for 1 min and 2 min), vacuum (for 30 min), SF6 (for 30 sec) and water (for 30 min). Our devices are tested immediately after their respective treatments to measure leakage current. After preservation for one week, we

measure those devices again. The leakage currents of these three situations are then compared to show the improvements.

Our 25 switches are treated with oxygen plasma for 1 minute.

The I-V curves of the 8th switch are shown in Fig. 3.8, in which the red line and blue line represent the I-V characteristic before and after treatments, respectively, and the green line represent the I-V characteristic after a week. By exponential fitting, we can get the corresponding I-V equations as (3-2), and the figure is plotted in Fig. 3.8.

$$I_4 = 0.000671\left(e^{0.373V} - 1\right) - 0.000249V - 0.0000491V^2$$
$$I_4' = 0.000533\left(e^{0.377V} - 1\right) - 0.000200V - 0.0000401V^2 \qquad \text{Eq.(3-2)}$$
$$I_4'' = 0.0000129\left(e^{0.704V} - 1\right) - 0.00000904V - 0.00000248V^2$$

Fig. 3.9 shows the plot of logarithmic values of current and applied voltage of 25 switches in all three cases. When 1V voltage is applied on the switches, the logarithm of the currents of the 25 switches is shown is Fig. 3.9. The parameters of V0, A (leakage current), B1 and B2 are shown in Fig. 3.10, Fig. 3.11, Fig. 3.12 and Fig. 3.13, respectively.

Reduction of leakage current is one of the primary criteria in the design of nanoelectromechanical switches. The air gap between the two cantilever beams also effects the leakage current. It is very important to design these switches with proper air gap such that switching voltages and leakage currents are very low. Leakage current must be reduced to the maximum extent possible in order to achieve very low power dissipation.

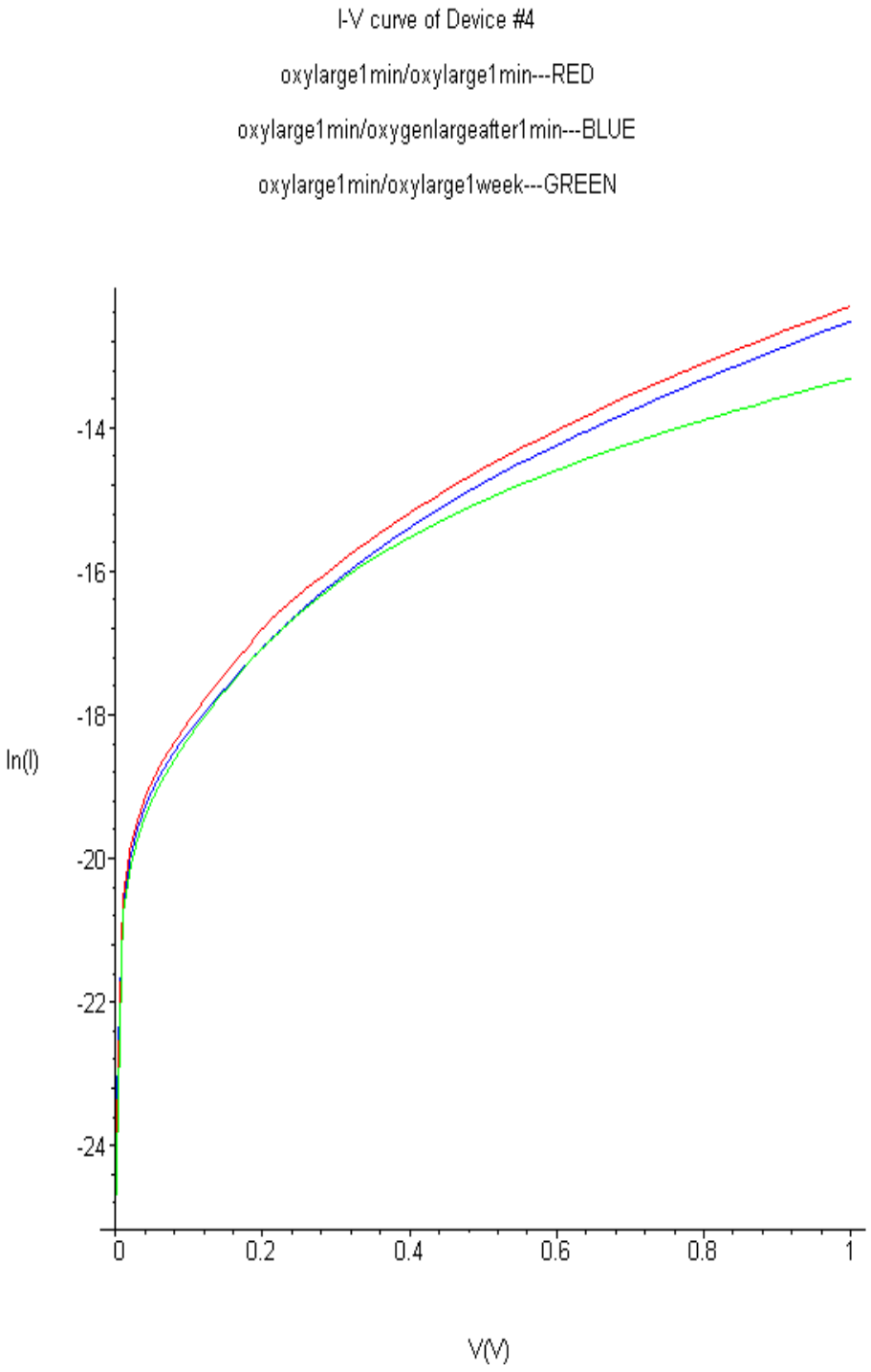

Figure 3.8 ln (I) -V curves before and after treatment

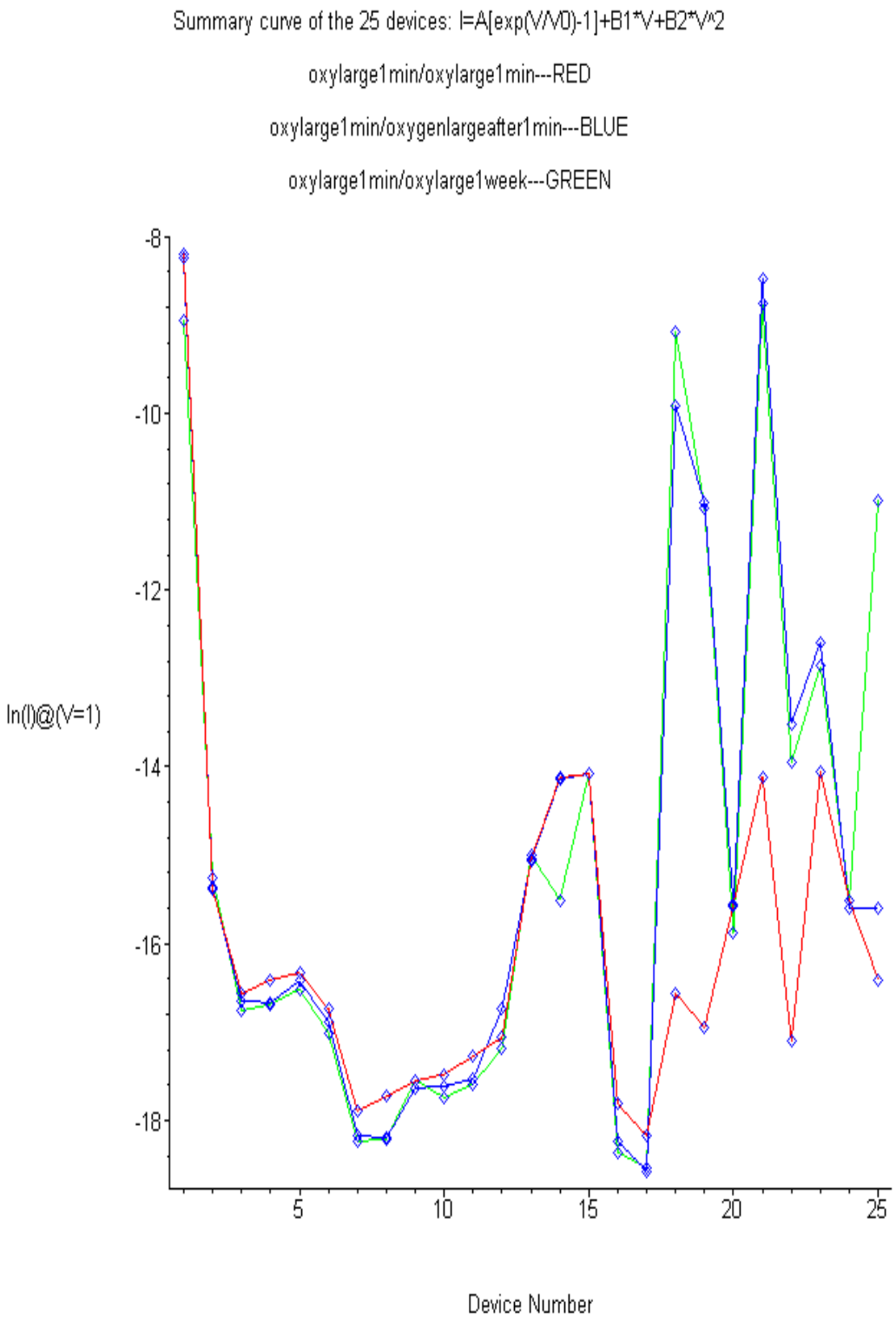

Figure 3.9 The logarithm of the current of 25 switches when 1V voltage is applied

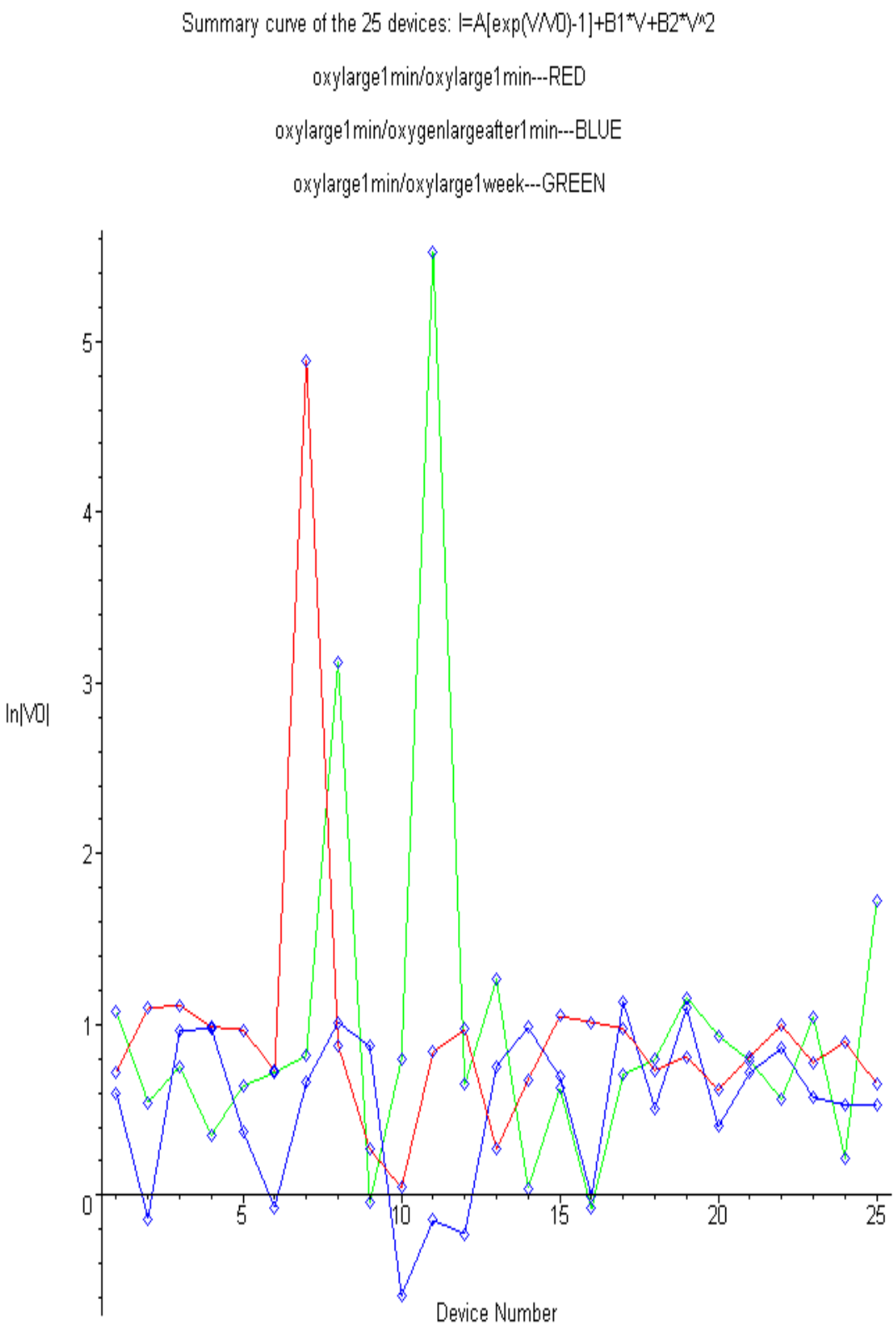

Figure 3.10 ln (V0) of 25 switches

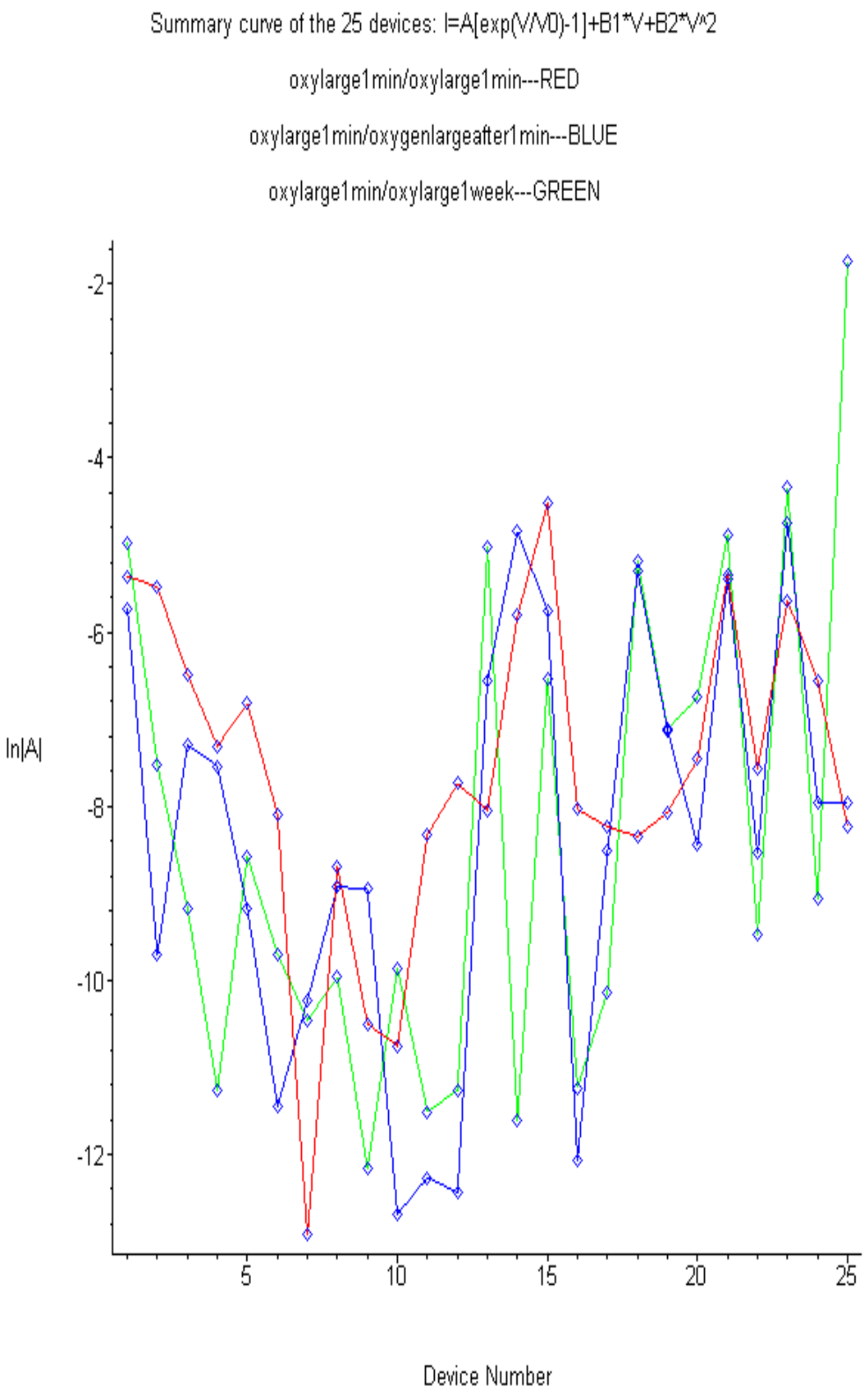

Figure 3.11 The leakage current A of 25 switches after treatment

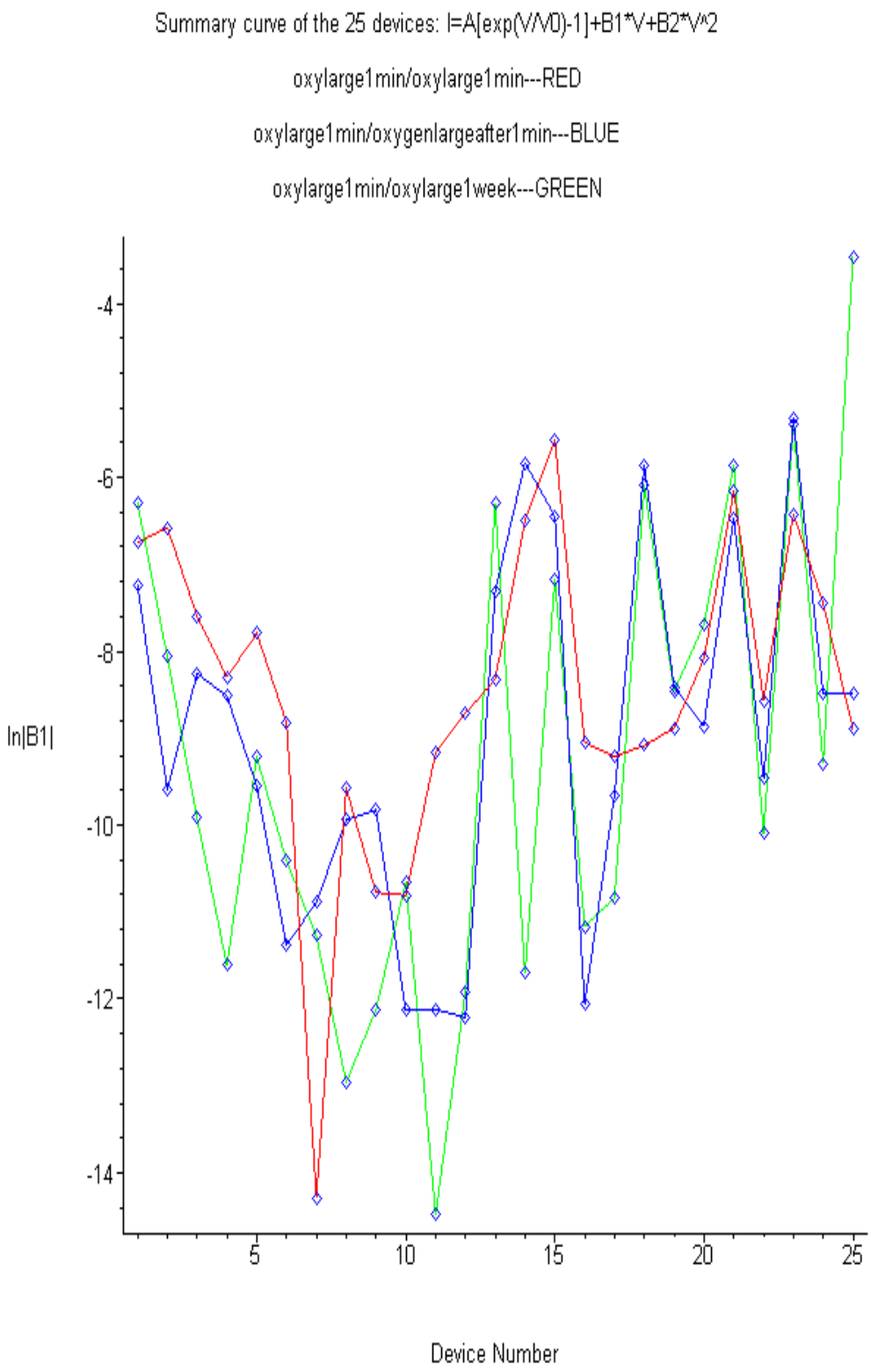

Figure 3.12 ln (B1) of 25 switches

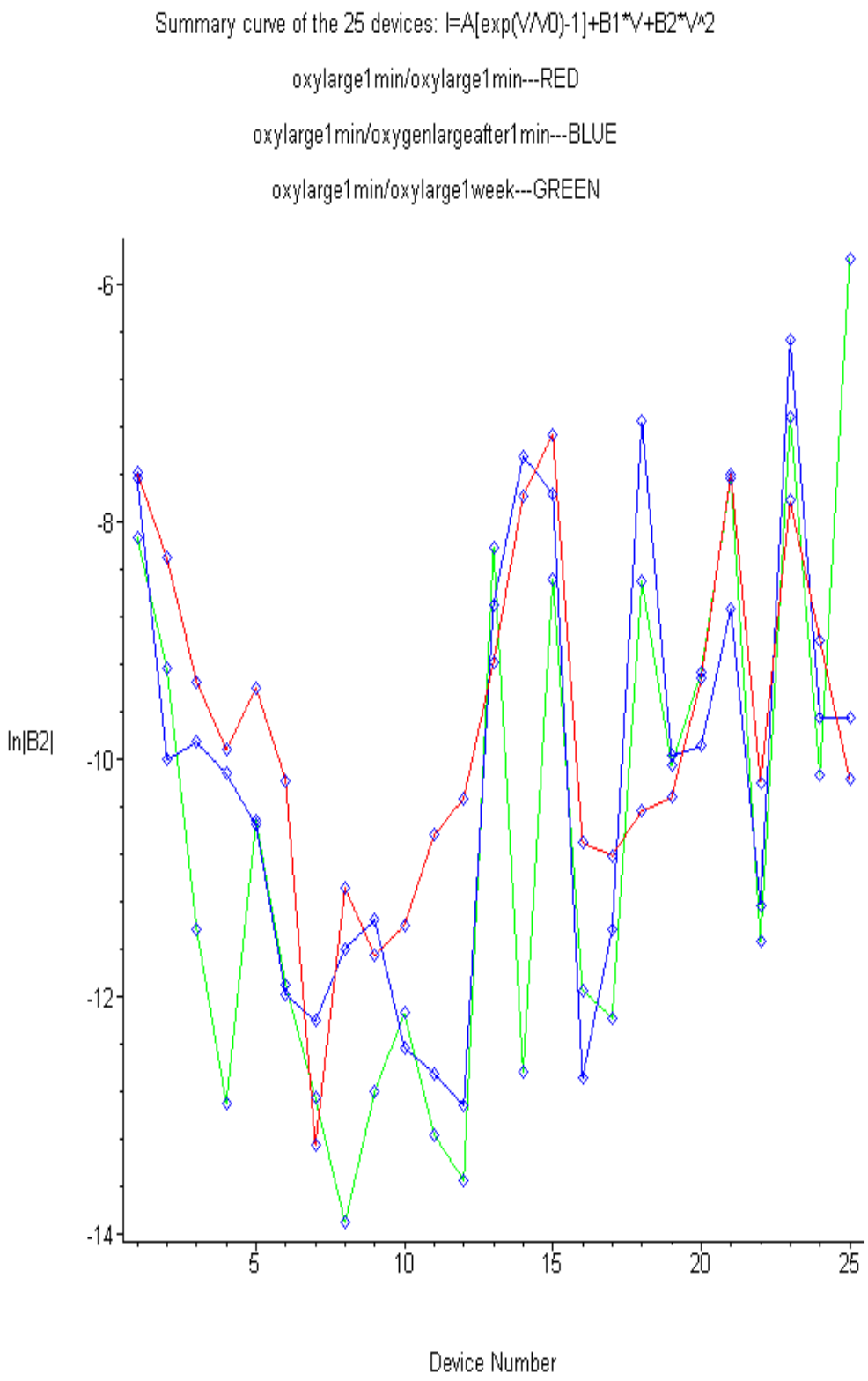

Figure 3.13 ln (B2) of 25 switches

These figures demonstrate that the treatment with oxygen plasma for 1 min resulted in the lower leakage currents of most devices when compared to those before treatment. And after preservation for one week, the performance seems even better.

3.5 Effect of Temperature on Switching Characteristics

The devices are placed in a special instrument with vacuum inside. The temperature is varied by making use of a temperature controller. The devices are tested both at room temperature- 298 K and higher values. The maximum temperature that can be attained by the temperature controller was 409 K. The differences in the switching voltages were clearly evident. The devices switched at early voltages when the temperature was raised to 409 K. The switching voltage at room temperature was around 1.2 V and that at 409 K was around 0.7 V. Fig. 3.14 clearly shows the I-V characteristics of a device at 298 K and 409 K. The conductivity of metals increases with temperature which speeds up the switching of these devices.

The devices are tested repeatedly to examine if the switching characteristics are reproducible. Fig. 3.15 depicts the switching characteristics when the device is tested continuously for 12 times. The switching characteristics were almost reproducible but started deteriorating after 4-5 appends approximately. There were slight changes in the switching voltages, as they increased slightly when repeated. The characteristics completely deteriorated after 15 appends approximately. The research is still being done to improve the switching characteristics and to avoid deterioration when tested repeatedly.

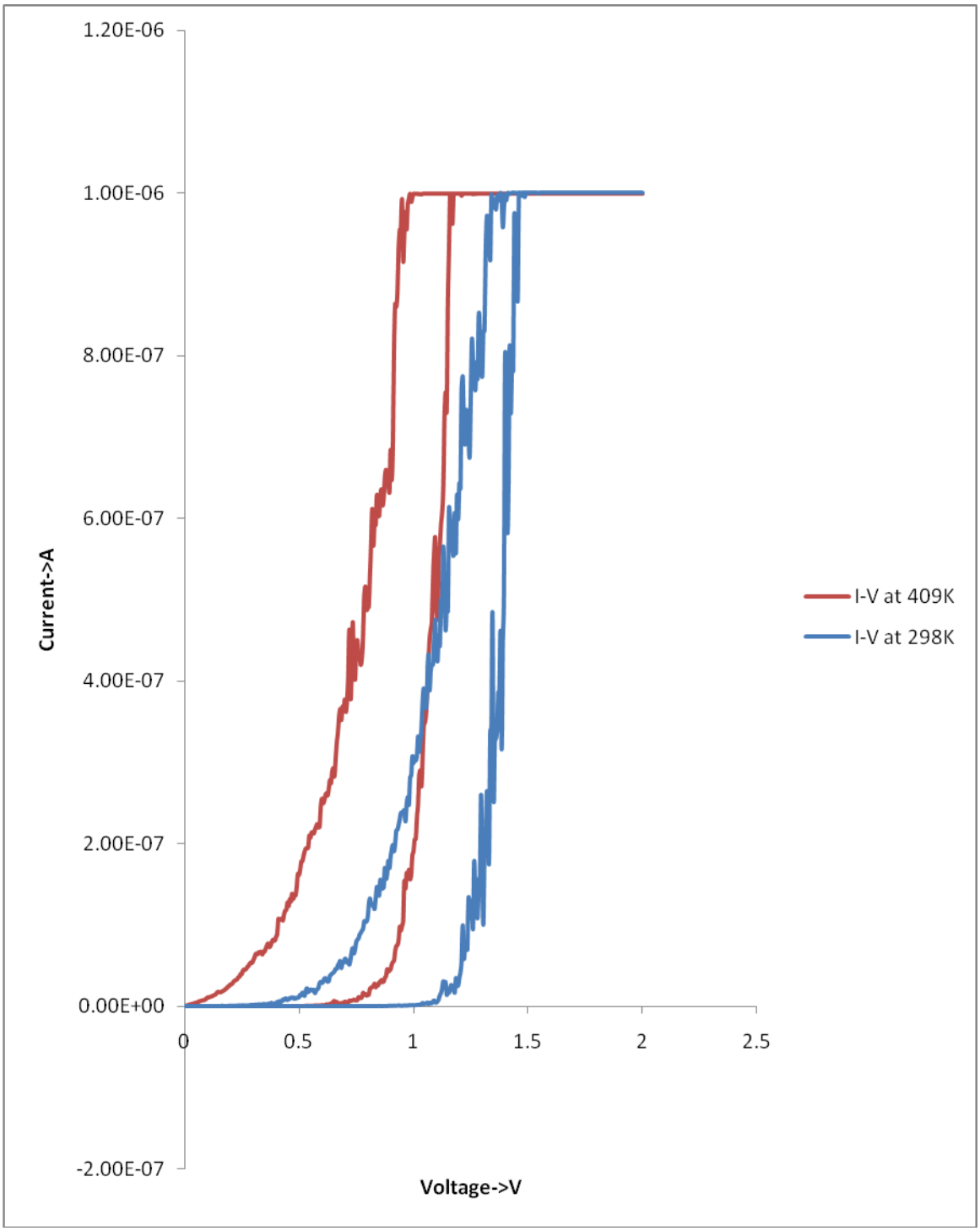

Figure 3.14 I-V characteristics of a device at 298 K and 409 K

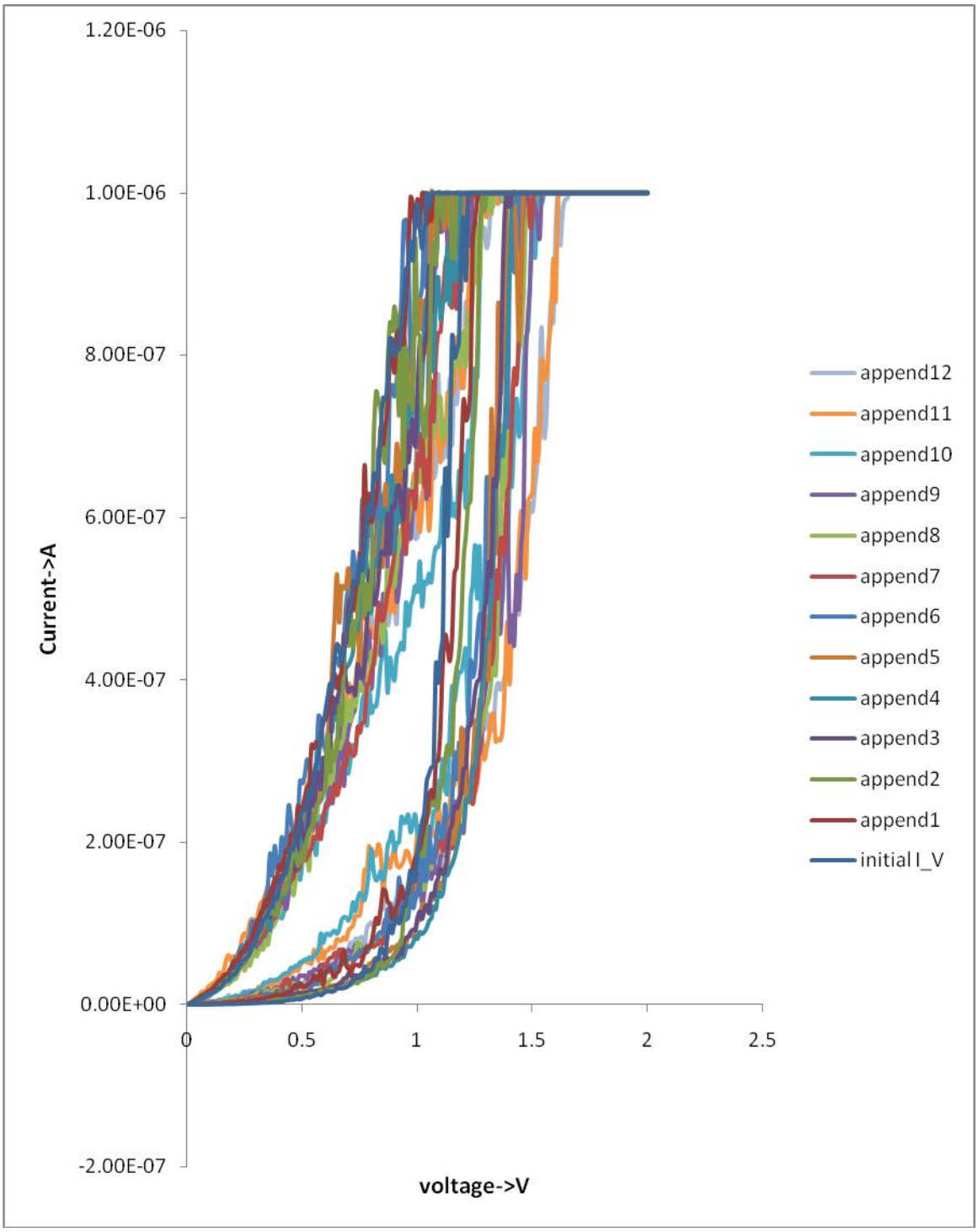

Figure 3.15 I-V characteristics of a device with 12 appends @ 409 K

3.6 Switching Characteristics

A simple circuit is used to examine the switching characteristics of nano-electromechanical switches [9]. It is clearly shown in Fig. 3.16. The circuit consists of a pulse generator unit (PGU) and a simple resistor. The output of the PGU is given as an input to the device and the output is connected across the resistor. The switching characteristics are observed by connecting both pulse input and output to a high-end Digital Phosphor Oscilloscope.

The amplitude of the input pulse is varied from 0.5V to 4V in order to observe exact switching of the device. The results showed that there was switching to some extent at lower voltages (~0.5V) due to parasitic capacitance. The switching was very slow at these voltages. The switching times improved rapidly as the voltage level is increased. Higher voltage resulted in faster switching. Figures 3.17 and 3.18 clearly depict their switching characteristics.

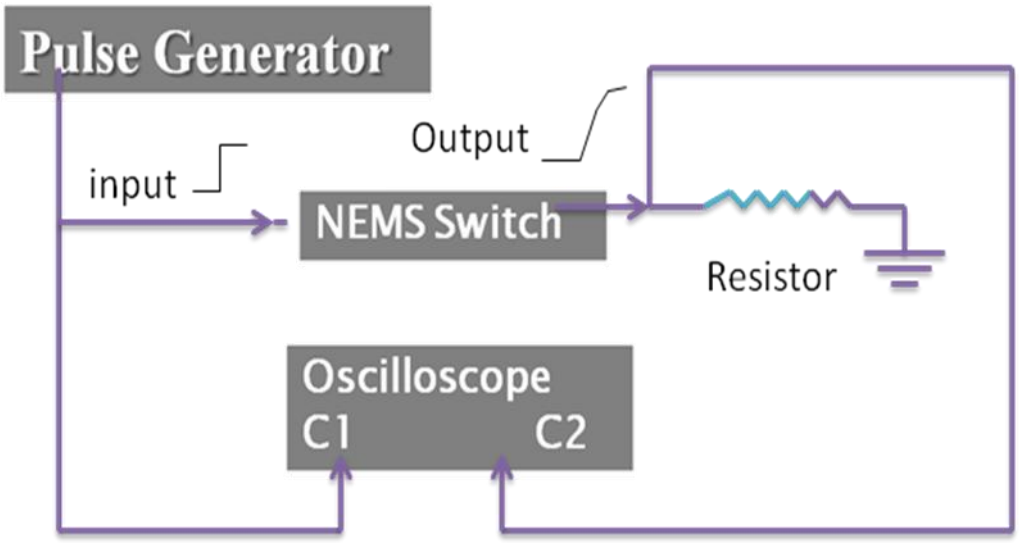

Figure 3.16 Experimental set-up to measure switching characteristics

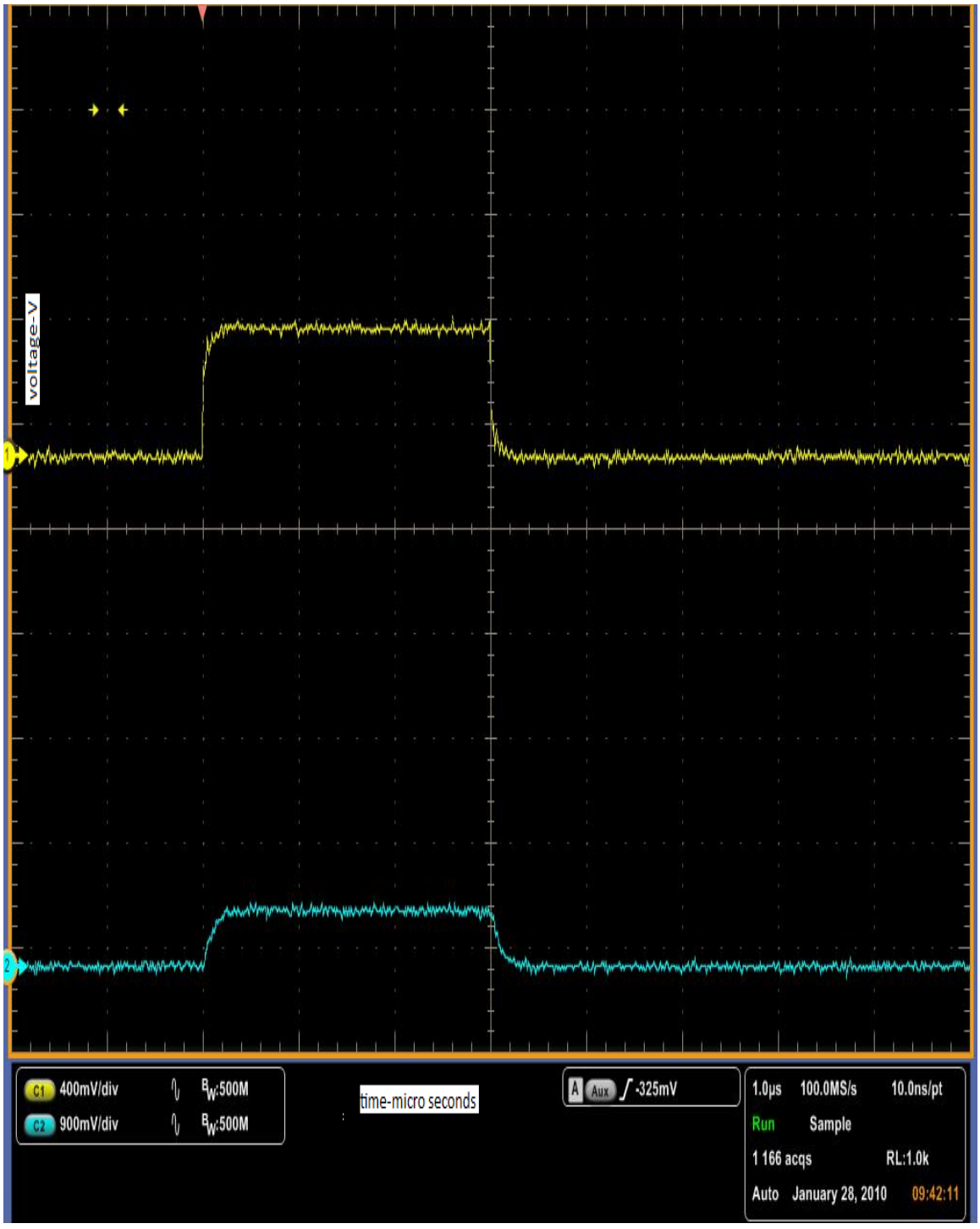

Figure 3.17 Input and output waveforms when a pulse input of 0.5 V is applied

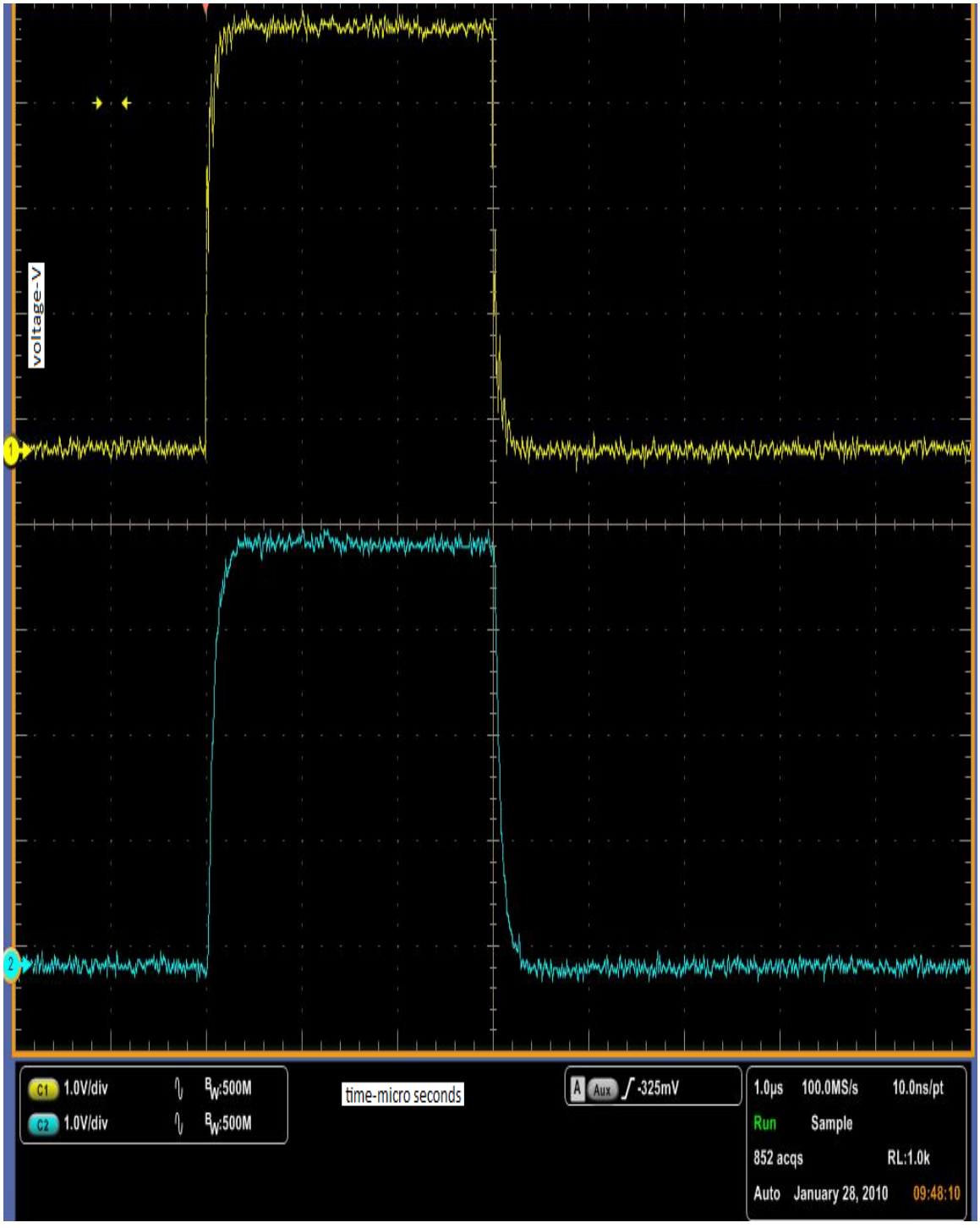

Figure 3.18 Input and output waveforms when a pulse input of 4 V is applied

3.7 Design of a Switch Using Piezoelectric Actuator

3.7.1 Experimental Set-up

A switch is designed using a piezoelectric sensor as an actuator. An actuator is a device that helps in moving or controlling a system. Some form of energy is required to move or control it and usual sources of the energy include air, voltage or electric current. The normal piezoelectric effect is generating electricity from squeezing the crystal. They have polarity and behave differently when positive and negative voltages are applied. Fig. 3.19 shows a piezo actuator and Fig. 3.20 shows the expansion and contraction when voltage is applied. Flexiglass is used to design a micrometer setup. Two hinges are arranged using flexiglass pieces to support a piezo actuator. A spring is used to adjust the distance between the piezo actuator and the metal base. This defines the experimental set-up for a micrometer (adjusting the distance using a spring). Fig. 3.21 clearly shows the experimental set up of a switch circuit using a piezo sensor. Fig. 3.22 depicts a flexi glass set-up.

Figure 3.19 Piezo actuator

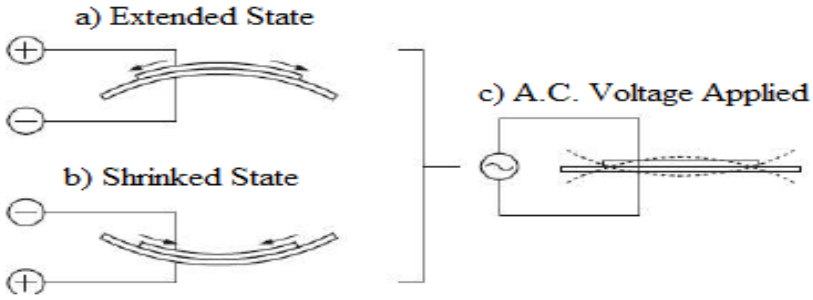

Figure 3.20 Expansion and contraction when voltage pulse is applied to a piezo actuator

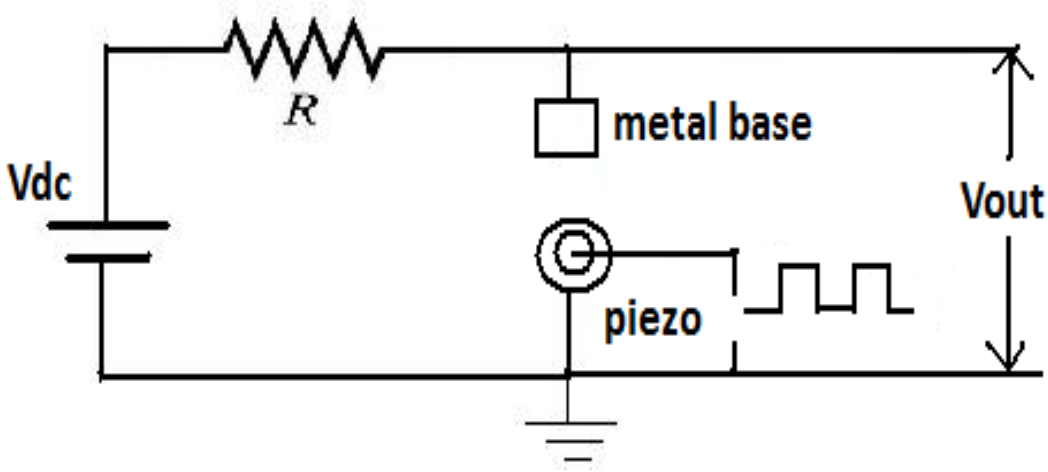

Figure 3.21 Circuit diagram of a switch using a piezo actuator

3.7.2 Basic Functionality of the Circuit

The two terminals of the piezo sensor are connected to a square wave signal from a signal generator and ground. The metal base is connected to a DC voltage source through a 88.7 Kohm resistor. The frequency and amplitude of the square wave signal are adjusted to get proper oscillations. The metal base is connected to an oscilloscope for monitoring output signal. The piezo starts vibrating due to its expansion and contaction properties when voltage is applied. These vibrations of the piezo sensor result in contact with the base (metal). When the piezo touches the metal, it results in a short circuit and output is zero at that point of time. When it moves up, the circuit is open and output voltage is equal to DC voltage applied to the metal base through a resistor. The output is a pulse that oscillates between the DC voltage and zero. The frequency of the sine wave signal is 1KHz and the amplitude is adjusted to get stable oscillations. Fig. 3.23 clearly shows the input and output signals.

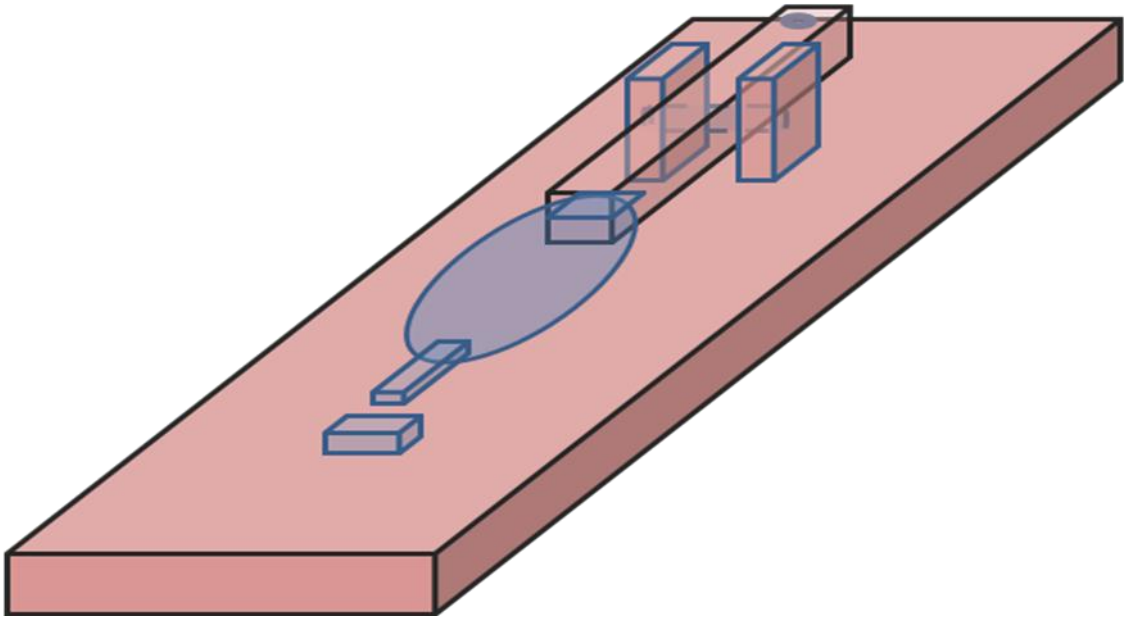

Figure 3.22 Flexi glass set-up

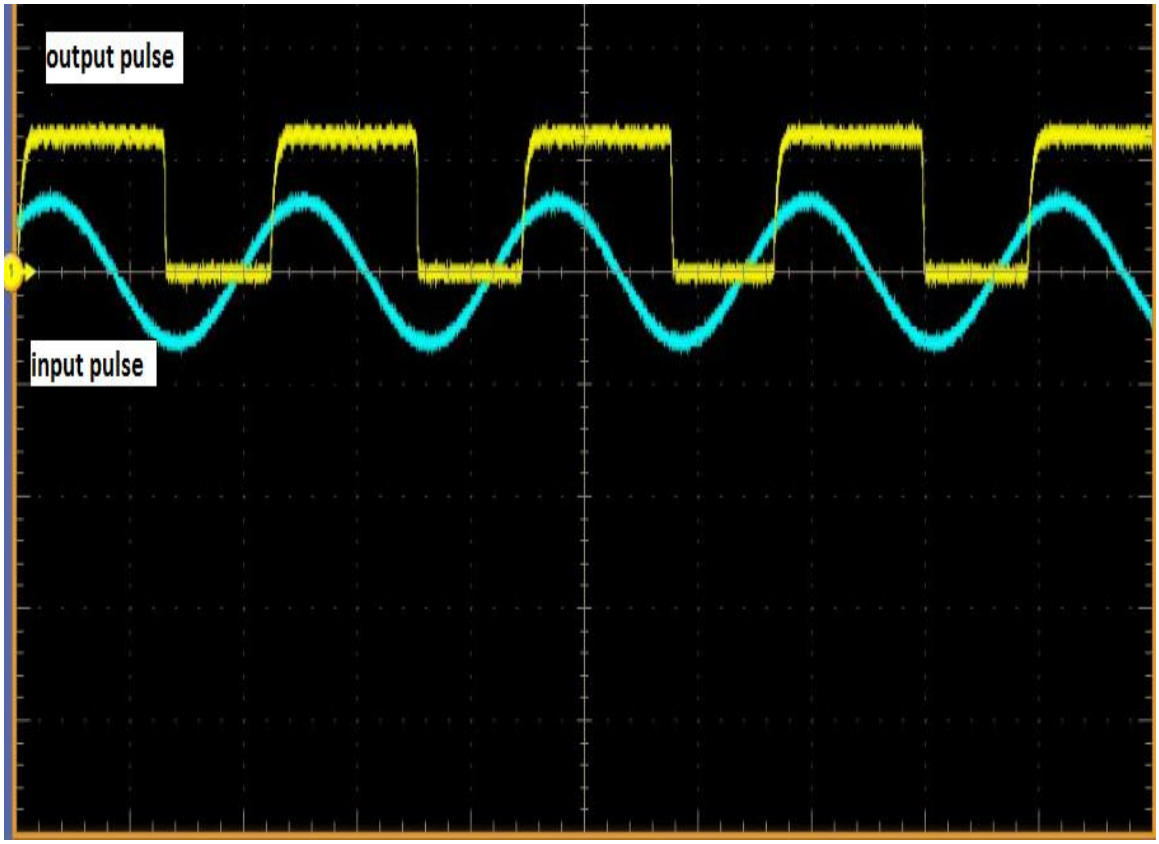

Figure 3.23 Input and output pulses

A chamber is designed with a vaccuum such that environmental conditions will not effect the device. Triax cables are used to connect the voltage sources to both the piezo and metal base. The chamber is tightly closed to avoid interactions with the atmosphere. The device is placed in the chamber and then it is closed with a lid. The oscillations are monitored for a long time to observe the longevity of the switch. The oscillations damp out after some time (3-4 hrs) due to characteristics of the metal base. There are various conditions that affect the functionality of the switch. These factors include oxidation of the metal base, contact resistance variations with time and environmental conditions. Fig. 3.24 clearly depicts the oscillations for a certain amount of time.

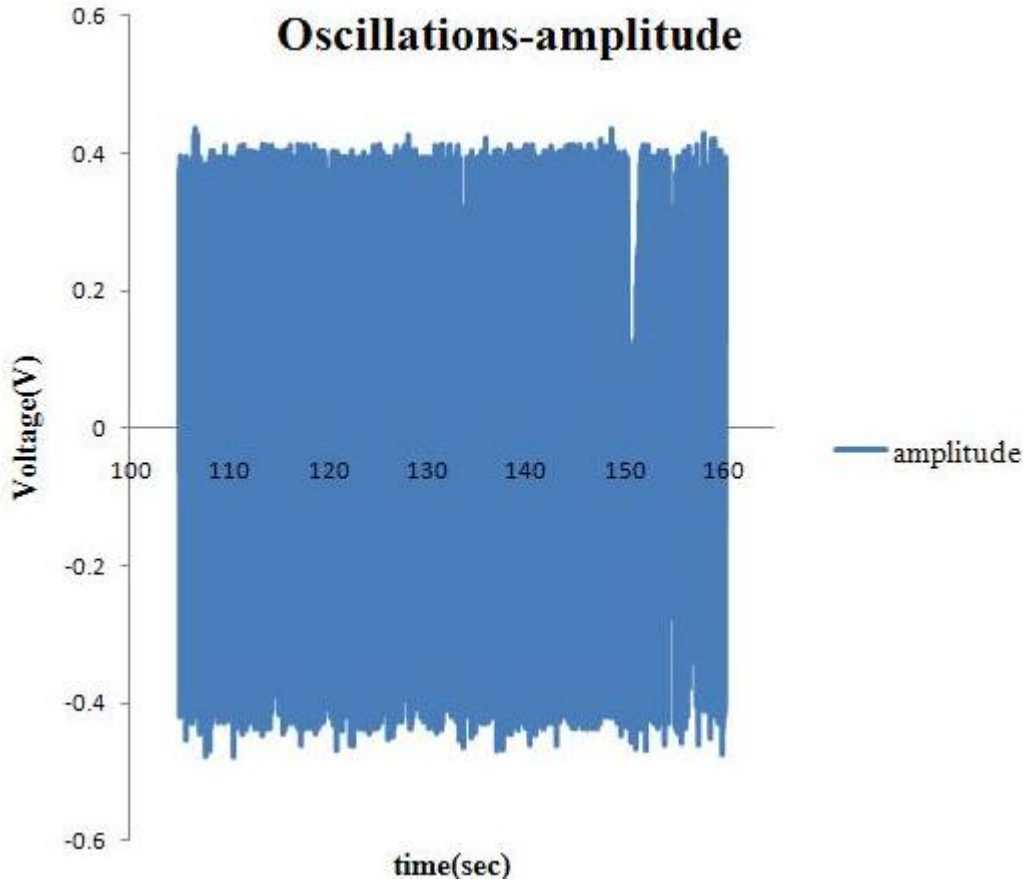

Figure 3.24 Amplitude of oscillations observed for certain amount of time

3.8 Design of an AND Gate Using Piezoelectric Actuator

3.8.1 Basic Functionality of Circuit

The **AND gate** is a digital logic gate that implements logical conjunction - it behaves according to the truth table, Table. 3.1. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the *minimum* between two binary digits, just as the OR function finds the *maximum*.

3.8.2 Experimental Set-up

The AND gate logic is implemented using piezo sensors. The input signals are connected to two piezo actuators. The output is taken across the contact between piezo's and ground as shown in the Fig. 3.25. The input signals are adjusted such that all four cases are covered. The time periods of both the input signals is 3.4 ms with their ON and OFF periods being different. Fig. 3.26 clearly depicts that the output is HIGH only when both the inputs are HIGH and it appears after certain delay of 1 ms.

Table 3.1 AND gate – truth table

INPUT		**OUTPUT**
A	**B**	**A AND B**
0	0	0
0	1	0
1	0	0
1	1	1

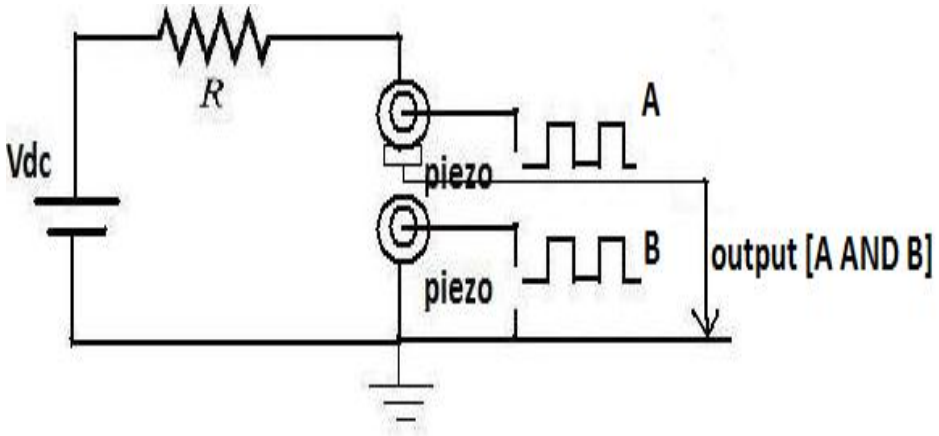

Figure 3.25 Circuit diagram of an AND gate using piezo actuators

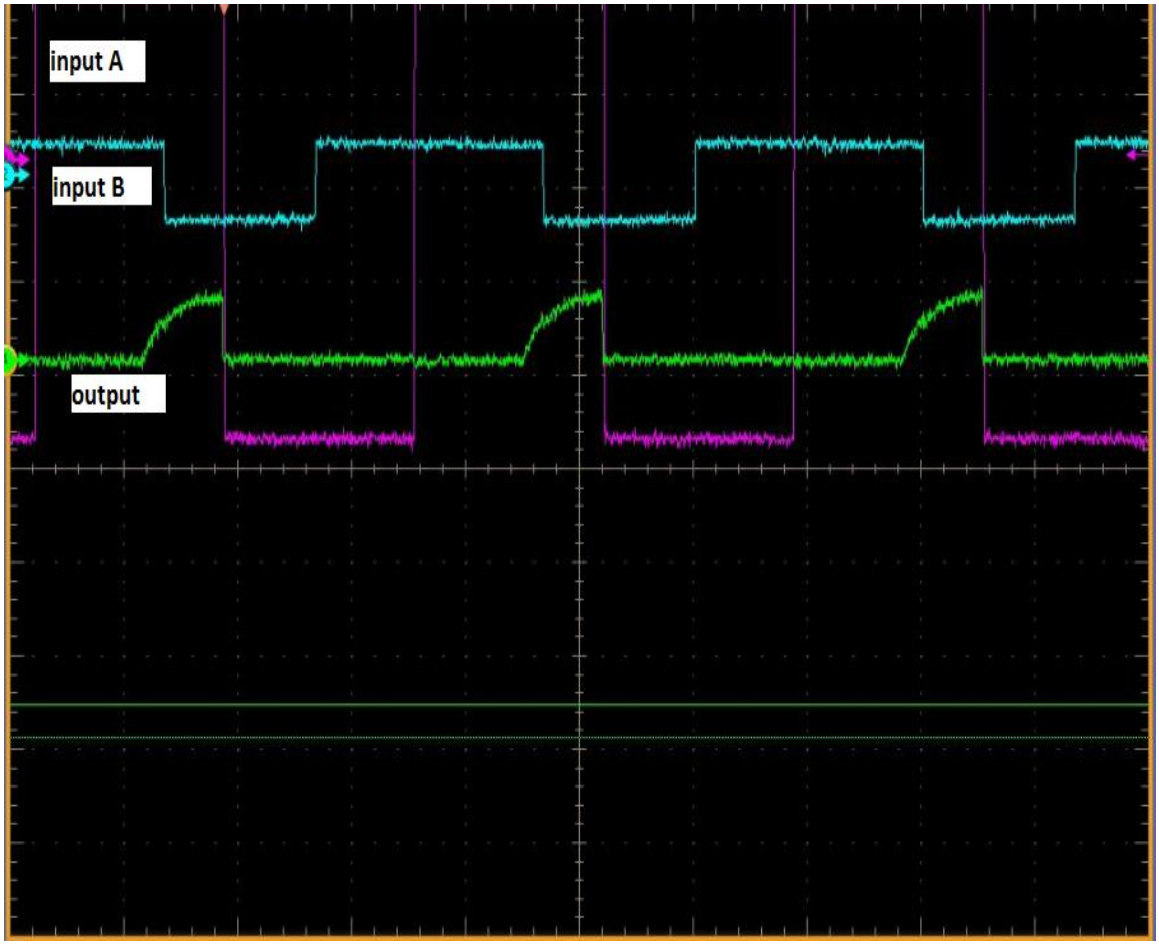

Figure 3.26 Inputs A, B and output (A AND B)

CHAPTER 4

CONCLUSION

A novel device has been proposed with tuning fork geometry that promised high speed of operation and low actuation voltages. Gaps of the order of a few nm between metal and silicon have shown excellent performance at lower voltages. Simulation has been realized to estimate the relationship between switching voltage and the gap. From the result of simulation, the thickness was appraised to 1~3 nm. The thickness of 1~3 nm resulted in very low actuation voltages of the range 1~5 V.

Leakage current is the major concern of using nanoelectromechanical switches. Various techniques have been explored to find out the best option for reducing the leakage current. The devices were treated with oxygen plasma, SF6, water and vacuum for a fixed amount of time. The switching characteristics revealed that treatment of the devices with oxygen plasma for 1 min resulted in the best reduction.

The effect of temperature on switching characteristics was also examined. The devices are placed in a special instrument and temperature was varied. The switching characteristics are compared at room temperature- 298 K and 409 K. The increase in temperature improved switching voltages to some extent. The devices are tested repeatedly at higher temperatures to observe their longevity.

The switching speed of the devices is examined by using an experimental set-up with a pulse generator and a resistor. The switching times are large when the amplitude of

pulse is less than the switching voltage. The switching times are very fast when the pulse amplitude exceeds the actuation voltage. The devices are tested with RF signals using a Network Analyzer to examine the gain at GHz frequencies.

Piezo electric sensors are used to make a switch by a flexi glass set-up. The oscillations of piezo actuators result in closing and opening of a switch. The output amplitudes are considered to calculate the contact resistances of various materials like ruthenium and tungsten. This helped in determining the longevity of devices using a chamber with a vacuum such that environment will not affect them.

4.1 Future Work and Recommendations

Research in the field of nanoelectromechanical switches is still in the preliminary stages. The NEMS devices are supposed to replace the conventional VLSI technologies. This requires extensive work to achieve all the specifications concerned with low actuation voltages, high operating frequencies and functioning at high temperatures. The current work assures very low switching voltages of the range 1~2 V and operating frequencies of the order of GHz. Future work is to be done to achieve the repeatability of switching characteristics. The nanoswitches are supposed to switch endlessly and this is to be explored.

The three basic gates of AND, OR and NOT are considered to be the universal set to design any VLSI circuit. Thus, these gates are to be designed using nanoelectromechanical switches. The contact resistance should not change with time and repeated testing. The switching characteristics depend on the materials used to make the cantilever beams. Suitable metals for fabricating switches must be decided based on the contact resistance, actuation voltages and speed of switching. The main focus is to make

NEMS switches with very low actuation voltages, high speed, very small footprint and repeated functionality in comparison with conventional VLSI devices.

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