DESIGNING A HIGH-SPEED LOW-COST ELECTRICAL IMPEDANCE TOMOGRAPHY DATA ACQUISITION SYSTEM USING COMMERCIAL OFF-THE-SHELF COMPONENTS

by

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STATEMENT OF THESIS APPROVAL

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ABSTRACT

As unattended, remote controlled, and self-driving aerial and ground vehicles become increasingly prevalent, the need for real-time structural health monitoring (SHM) systems that can sense, localize, and quantify internal structural damage with low latency, low power, and small size and weight requirements, is increasing. One such methodology, electrical impedance tomography (EIT), shows promising results, but is limited in its scalability and portability due to lack of hardware support outside of expensive and bulky laboratory-grade equipment. In this master's thesis, a data acquisition system of low cost and small form factor is designed and prototyped to rapidly and efficiently collect EIT measurements for SHM applications. System scalability is abstracted to small data acquisition modules that communicate to a host computer via a USB connection. Fitting the palm of your hand, and at a cost of only 250 USD, each module is capable of collecting EIT data at a rate of 10,000 voltage measurements per second with 10-bit resolution. This study describes the design process that attempts to achieve the desired data collection rate, transfer speed, and size requirements for this application using only readily available commercial off-the-shelf electronic components. The performance, precision, accuracy, and EIT reconstruction results of the designed EIT measurement system are characterized and compared to a laboratory-grade EIT data acquisition system.

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CHAPTER 1

INTRODUCTION

Recent thrusts in engineering have focused on realizing aerial and ground-based vehicles that enable unattended, long-term continuous operation that will greatly benefit the transportation, communication, commerce, and military sectors. For example, solar-powered drones may be airborne for months at a time to provide wireless data connectivity to remote locations [1], or fleets of taxis comprised of self-driving cars aimed at reducing or removing human operator derived drawbacks [2]. To achieve the vehicular requirements brought on by these visions, engineers have turned to using new materials and manufacturing methods that do not have the same level of experience with regard to long-term reliability.

One class of materials with increasing utilization is fiber-reinforced composite materials, particularly in the aerospace [3], automotive [4], and military [5] industries. The adoption of composites is mainly due to their high strength-to-weight ratios, resistance to corrosion and fatigue, and high conformability. While composites have these attractive attributes, they remain susceptible to damage modes that manifest internal to their structure that can be difficult to detect using traditional visual means [6]. This has required the use of nondestructive evaluation methods, such as ultrasonic inspection [7], that can be time-consuming and thus costly due to the high level of human interaction required from the operation. In addition, if structural damage occurs to an autonomous vehicle, no person may be present to notice; failure may cause significant damage to human life and property [8]. Currently, these materials are being pushed to their limits to enable solar-powered, circumnavigating aircraft [9], and engineers are turning to additive manufacturing to enable complex and automated manufacturing [10]. In this same vein, we envision an automated structural health monitoring (SHM) system that detects, localizes, and assesses the extent of damage in real-time to provide the vehicle and its

owner with a metric to determine if the vehicle requires service to prevent catastrophic failure. Furthermore, this approach would significantly reduce the cost of structural health assessments by replacing current human-performed nondestructive evaluation methods with automated methods. This application imposes dramatically new requirements on the sensing system, including significantly lower latency, lower power, and smaller size and weight requirements than possible with today's SHM systems.

1.1 Structural Health Monitoring Methodologies

Modern SHM methods include, but are not limited to: foil-based strain gauge networks [11], optical fiber Bragg gratings [12], acoustic and ultrasonic-based sensing [13]–[15], and many others [16]. These methodologies continue to be investigated due to their promising results, but each has tradeoffs. In general, these systems require large and expensive hardware and data acquisition systems [6], and most are point-based methods that require interpolation and other estimation methods when sensing damage located further from the point of sensing [17]. Furthermore, many methods have explored embedding transducers and sensors, such as piezoelectric and ultrasonic, into the structures themselves, which, in the case of composite-based structures, can lead to locations of concentrated stress and induce premature damage or aging [17], [18]. Other drawbacks include overall system weight and installation and maintenance cost [19], [20]. Together, these limitations have motivated the need to develop sustainable low-cost, lightweight, and miniature SHM systems [19]–[22].

An alternative methodology that has been recently proposed to be used for SHM is electrical impedance tomography (EIT). Native to the medical industry, EIT has been used for decades to spatially image different parts of the human thorax and provide relatively quick, nonintrusive evaluations to assist in the detection of cancers and other abnormalities within a human body [23]. It has also been used in nonmedical applications such as detecting gas bubbles in pipes and estimation of mineral resources [24]. The application of EIT requires a conductive medium (such as human tissue) that is bounded by electrodes. Traditionally, alternating currents are pulsed into one electrode at a time and voltage measurements from the remaining electrodes are used in EIT reconstruction algorithms to estimate the internal conductivity distribution of the medium [25]. As not all materials

are conductive by nature, this can pose a problem. However, by utilizing a sprayable conductive thin film paint [26], both new and existing structures can benefit from the application of a conductive surface to enable EIT monitoring without significant difficulty.

1.2 Problem Statement

The EIT methodology for SHM has been validated by previous work [26], [27]. However, few EIT systems have been specifically designed for SHM. State-of-the-art SHM EIT data acquisition systems (DAS) are typically composed of various pieces of large, expensive, slow, and power-hungry laboratory-grade test equipment [24], [25], [28]–[31]. These characteristics pose several challenges and limitations for using these systems in practical SHM applications including real-time monitoring, cost, field deployment, weight, power consumption, scalability, and ultimately, industry adoption. This master's thesis aims to overcome these challenges by developing an EIT DAS using low-cost, readily available commercial off-the-shelf (COTS) components. The resulting design aims to be a custom all-in-one, modular data acquisition system of lower cost, lower power, smaller and lighter form factor, with high speed data acquisition as a solution for a more portable, scalable, field-deployable, and easily available system.

1.2.1 Design Specifications for Electrical Impedance Tomography Data Acquisition System

In order to achieve the goals of this thesis, yet provide suitable data for EIT reconstruction, several design specifications were determined for the new portable DAS:

1. The system should be capable of performing high speed measurements at a low cost, with a target rate of 100 frames[1] per second (fps) at an overall cost of less than 1000 USD per EIT DAS module. Collecting data at a high frame rate will: i) enable the ability to real-time monitor; ii) mitigate adverse effects of physical perturbations

[1]The speed of an EIT DAS is typically measured in "frames per second (fps)" [28]. Each frame consists of data from an injection pattern. An injection pattern consist of multiple patterns, sometimes called projections. Each pattern, or projection, consists of an electrode pair, one representing the electrode through which electrical current is injected, and the other representing the electrode connected to electrical ground. Finally, a signal averaging factor is also considered, representing the number of samples measured at each electrode during a single pattern. Therefore, the total number of measurements performed during a single frame is calculated as $measurements\ per\ frame = num\ of\ patterns \times num\ of\ electrodes \times num\ of\ averaging\ samples$. Here, a frame will always represent an injection pattern consisting of 32 patterns, connected to a 32 electrode system with a signal averaging factor of N. Therefore, $1\ frame = 32 \times 32 \times N = 1\ \text{k} \times N$ voltage measurements.

(i.e., compression/decompression, flexing, etc.) during data collection on dynamic applications; and iii) reduce latency in large-scale systems that require large data collection. The low cost will improve the appeal, accessibility, and scalability of this system for a wider range of applications.

2. Each module should be lightweight and have a small form factor. This constraint will make the system more portable, easily deployable, and suitable for a variety of new and existing applications.
3. The system should be capable of testing structures made from a variety of materials. While an end product derived from this research might be permanently deployed to monitor a single specific structure, the prototype produced in this study must be able to test a variety of materials of varying orders of magnitude of resistance to validate the effectiveness as an EIT DAS for SMH. Therefore, each module should support an independent, controllable electrical current source with the range 1 µA–100 mA. This constraint is critical for maximizing the signal-to-noise ratio (SNR) by setting an appropriate current value for a given material's resistance.
4. For test purposes, the system must have a graphical user interface (GUI) that allows a user to control the measurement process. The GUI should allow the user to set the value of the current source (within the supported range) and support user defined injection patterns.
5. The system should be modular. By abstracting the system into modules, individual modules can be used for hot-spot monitoring, or scalability can be achieved by connecting several modules together to form one larger system. This provides flexibility to meet the specific needs of various SHM applications.

1.3 Contributions

The major contributions made by my thesis research include the novel design and realization of a high-speed, low-cost, and small form factor data acquisition system that performs EIT measurements using only readily-available COTS components [32]. The presented design and prototype is 200 times faster, 40 times less expensive, and 50 times lighter than the leading comparable laboratory-grade data acquisition system used for collecting EIT measurements for SHM applications. The significance of the speed, cost,

and weight improvements are monumental in advancing towards a real-time, practical SHM methodology for a variety of applications, including autonomous vehicles. While the total realization of the final design and prototype was a two-man effort, my personal contributions reside largely in the system design, digital circuit design of the hardware, and the development of both firmware and software to enable fast, efficient, and reliable EIT measurements.

1.4 Thesis Overview

As the goal of this thesis is to design an EIT DAS for SHM, Chapter 2 begins with a greater explanation of EIT as an SHM methodology. It also describes the technical details and specifications behind the design and architecture of a single EIT DAS module. Details of the hardware, firmware, and software aspects of the system are presented. Also discussed are the technical challenges encountered and the important decisions made to sustain the above design specifications using only readily-available COTS components. The revision history of the new portable DAS is presented.

Chapter 3 discusses and analyzes the characteristics of the new portable DAS, such as timing and data acquisition rate, accuracy and precision, and SNR. As part of the discussion, the characteristics and EIT reconstruction results of the new portable DAS are compared to those of an accessible laboratory-grade data acquisition system.[2] This work refers to the accessible laboratory-grade data acquisition system as LGDAS, while the new portable system is referred to by revision names.[3]

Chapter 4 provides the conclusion of this research and summaries the relevant contributions and important results. Future research directions pertaining to the new portable DAS is also provided.

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[2]The laboratory-grade data acquisition system is composed of the following pieces of laboratory-grade equipment: Keithley 6621 AC/DC Current Source, Agilent 34980A Multifunction Switch/Measure Mainframe and Modules, and Agilent 34410A Digital Multimeter.

[3]Revisions are sometimes referred to as *Revision X.Y* and sometimes as *XvY*.

CHAPTER 2

DESIGN

This research is a continuation of a five-person undergraduate senior capstone project, completed at the University of Utah (2014-2015). Therefore, the relevant research and progress for this master's thesis begins where the senior capstone project concluded. In order to understand the continued progress, it is important to understand the design decisions made during the senior capstone project. A brief overview of the senior capstone project is provided as part of the revision history. Detailed explanations of the relevant research pertaining to this master's thesis are then presented.

2.1 Electrical Impedance Tomography for Structural Health Monitoring

Traditionally, EIT is performed by first bounding a conductive sensing area with a set of electrodes. Alternating electrical currents (AC) are injected into one of the electrodes and propagate across the conductive medium to another electrode connected to an electrical ground [24], [25], [33]. Voltage measurements are recorded at the remaining electrodes with reference to the grounded electrode. The data is then processed using previously developed EIT algorithms that reconstruct the spatially distributed conductivity within the sensing area bounded by the electrodes [26]. For this work, however, direct electrical current (DC) was used instead of alternating currents, which eliminates reactance measurements and simplifies the problem to deal only with resistance values (calculated through Ohms Law). This method is also referred to as electrical resistive tomography (ERT) [34].

As the sensing area experiences strain, or suffers damage, the conductivity (or resistance) of the sensing area changes, and thus the distributed paths electrical current takes to electrical ground also change. The resulting change in the current paths will also affect

the relative values of the voltages measured at each bounding electrode. This relative change is then made manifest in the results of the EIT reconstruction and can be used as an SHM method to identify location, size, and severity of the damage introduced within the sensing area.

2.2 System Design for a Single EIT DAS Module

The challenge of creating an EIT DAS for SHM that conforms to the design specifications, as outlined in the Introduction of this work, is both simplified and abstracted to a smaller system consisting of individual modules. This approach allows us to validate a simplified system through prototyping and laboratory testing. The EIT DAS module performs EIT measurements around relatively small (4.5 in^2) sensing areas bounded by a set of 32 electrodes—16 or 32 electrodes is typical of other systems [24]–[27], [33], [34]. As a starting point for finding COTS components capable of the electrical ratings of the system, the measurable voltage range on each electrode is limited to 0 V–5 V.

The following discussion splits the design of the new portable EIT DAS into three aspects: hardware, firmware, and software. Each of these aspects has been refined over several revisions. The revisions that relate to the senior capstone project are Revisions 1.0–3.0. As Revision 3.0 did not meet all the desired specifications, the work was continued. All later revisions, work, improvements, and analysis performed constitutes continued work relative to this master's thesis.

2.3 Hardware Design

2.3.1 Revision 1.0

The system design contains two aspects, as shown in Figure 2.1: i) a host computer, and ii) an EIT DAS module. The host computer runs a GUI that is responsible for providing user interaction and communicating the desired actions to the EIT DAS module, and is discussed in the software section of this paper. The EIT DAS module is composed of a central microcontroller, a digitally controlled current source, two analog switches, and four 8-channel 24-bit analog-to-digital converter (ADC) devices. The reason for each COTS component chosen follows.

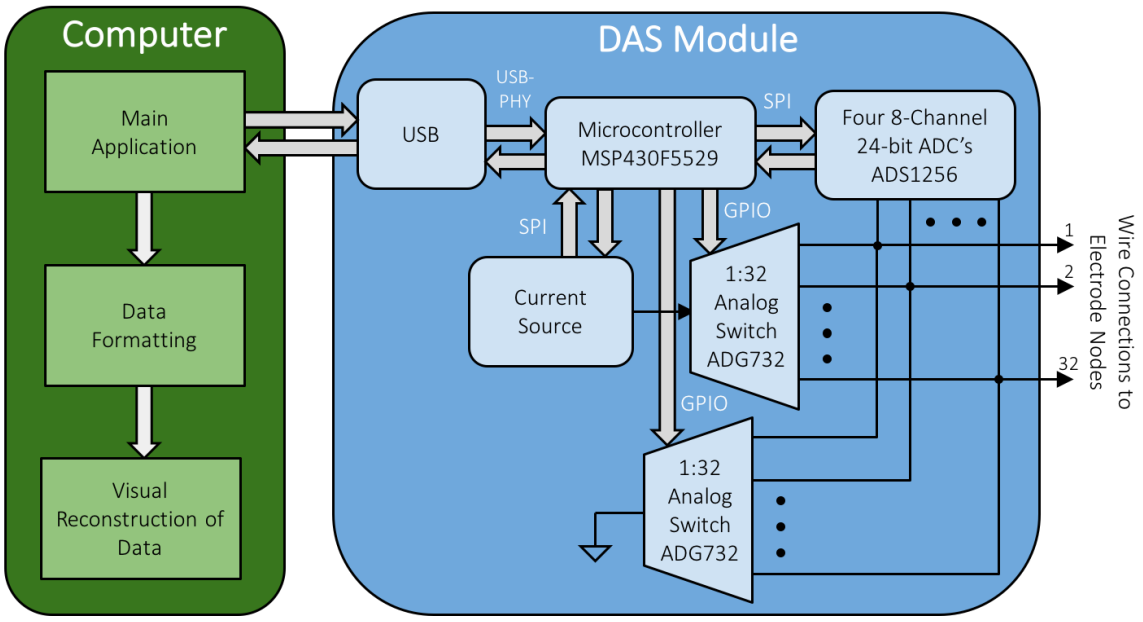

Figure 2.1. The EIT DAS is split into two parts: the host computer and the EIT DAS module. The main components/functions of both aspects are displayed in this system diagram for Revision 1.0.

2.3.1.1 Microcontroller: Texas Instruments (TI) MSP430F5529

This microcontroller (MCU) belongs to TI's ultra low-power MSP430 microcontroller family. It was originally elected not only for its low cost and low-power operation, but also for its integrated communication abilities, including USB and serial peripheral interface (SPI) communication protocols, which were necessary for this project. It also has sufficient (63) general purpose inputs and outputs (GPIO) to support the control of the analog switches and ADCs. With 128 kB built-in flash memory, it was determined that the microcontroller would likely not need any additional nonvolatile memory support to house the program application. Furthermore, TI's software support for this family of microcontrollers helps ease device driver and firmware development.

2.3.1.2 Analog Switch: Analog Device ADG732

When determining how to switch electrical current or electrical ground to any one of the 32 possible electrodes, it is desirable to find a single device capable of switching between all electrodes to mitigate both cost and size. This analog switch is a 1-to-32 channel switch, matching the number of electrodes of the module. With bidirectional

capability, it can direct a single input to any of 32 possible outputs, or it can take in 32 possible inputs and direct them to a single output. The FET design achieves high switching rates (40 ns), while maintaining a low on-resistance (4 Ohms). Also important is the device's ability to handle the voltage and current ranges of the application.

2.3.1.3 Analog-to-Digital Converter (ADC): TI ADS1256

This device uses a multiplexing architecture to direct any one of eight analog inputs into a single on-chip 24-bit, 30 ksps (samples per second) sigma-delta architecture ADC. By using four of these devices, all 32 electrodes are directly connected to its own dedicated analog input for voltage measurements. These devices are capable of sampling across a 5 V range, and can be biased to measure voltages in the range of 0 V–5 V.

2.3.1.4 Current Source: TI LM334

This device was selected due to its ability to be tuned to the desired current. Tunable from 1 µA–10 mA, with the support of three digital potentiometers, this device does not quite match the specifications of the system, but was determined to be a sufficient starting place for system validation. With three potentiometers, the current source could be tuned by 1 µA increments.

2.3.1.5 Power Supply

Initially, the design of the power supply supported a battery operated system. This design included both buck and boost converters to provide for the voltage needs of the system. However, this design was never functional, which also did not allow for functional testing of the system. With many mistakes in the first prototype, a second prototype was developed.

2.3.2 Revision 2.0

The main purpose of Revision 2.0 was to create a new power supply design. As a way to ease laboratory testing, the battery power supply design was replaced by a power supply design that can connect to an AC power source. Additionally, care was taken to improve the physical layout and symmetry to mitigate wire delays and noise of the system. Unfortunately, some mistakes in the layout design rendered the power supply of

the manufactured boards unusable. With a simple hack to input external voltage, system functionality tests were performed.

This design confirms the ability to program and execute the application on the main microcontroller, switch channels on the analog switches, measure data using the ADCs, and communicate via a USB communication channel with a host computer. However, one major challenge was made manifest when testing the ability to control the current source. The current source was initially designed to source current into the conductive substrate, requiring the current source to be placed in series with the substrate. Ideally, the design would guarantee a maximum potential voltage drop across the substrate of 5 V. When the potential drop across the substrate is less than 5 V, the remaining voltage is then dropped across the current source. However, the current source requires a minimum voltage drop of approximately 1.1 V in order to correctly bias the the BJTs. This limits the effective voltage range over the substrate from the ideal 5 V to 3.9 V, which could significantly impact the signal-to-noise ratio (SNR) of the measurements. To maintain the ideal voltage drop over the substrate, the current source was then supplied with a higher voltage. However, due to bypass diodes contained in the digital potentiometers, the 5 V supply was shorted to protect the internal resistive digital-to-analog converters from voltages higher than their supply. Consequently, the current source would no longer regulate its output. Therefore, a new design for the current source needed to be considered to increase the voltage potential drop across the substrate and maximize the SNR of the ADCs.

2.3.3 Revision 3.0

A potential solution to the current source challenges discovered in Revision 2.0 is to introduce a current mirror into the system. The mirror essentially decouples the voltage drop across the test substrate from the voltage required by the current source. This design is implemented as shown in Figure 2.2.

Improving upon the previous revisions, Revision 3.0 yields a functional EIT DAS module. However, though the current source in this revision is usable, it is limited in its range from about 10 µA–10 mA. A brief timing characterization of this unit was performed. With the signal averaging factor set to 5, this revision is capable of measuring one frame in 9.06 seconds (565 voltage measurements per second). This is a tenfold increase over the

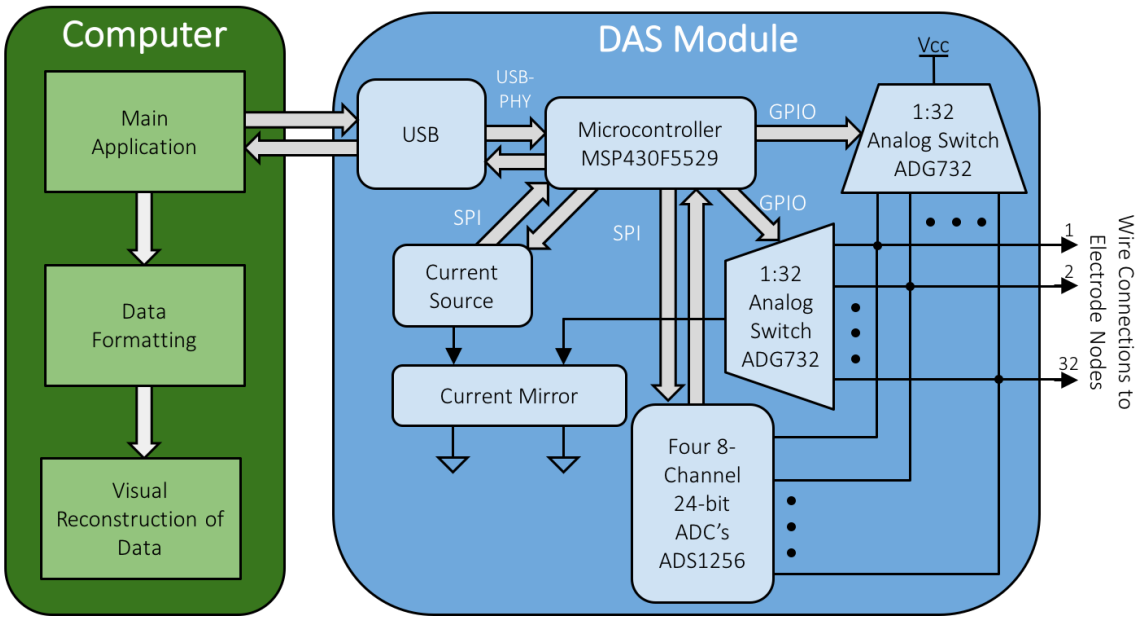

Figure 2.2. A current mirror is introduced in Revision 3.0 to alleviate the voltage potential drop across the current source.

LGDAS, as data collection of a single frame on the LGDAS, with a signal averaging factor of 5, takes 90 seconds (56 voltage measurements per second). Accuracy and precision of this revision's measurements were never evaluated as no valid EIT reconstruction was produced with this module. This functional unit marks the completion of the senior capstone project, and all continued work constitutes as research relevant to this master's thesis.

2.3.4 Revision 3.1

While Revision 3.0 achieves a functional EIT DAS module, the power supply design is unreliable, and a potential detriment to the quality of EIT measurements collected. To improve the design, the power supply noise characterization for Revision 3.0 was first performed, as seen in Table 2.1. A more robust power supply design was then explored and ultimately implemented in Revision 3.1. The power supply noise characterization for Revision 3.1 is presented in Table 2.2.

At this point in the design process, two additional hardware aspects were readdressed. First, although the noise seen on the power supply lines was reduced by an entire order

Table 2.1. Power Supply Noise Characterization for Revision 3.0 (Unloaded)

Version	Supply	Ripple (V_{pk-pk})	Noise (V_{rms})
3.0	5 V	230 mV	43 mV
	3.3 V	19.9 mV	3.45 mV

Table 2.2. Power Supply Noise Characterization for Revision 3.1 (Unloaded)

Version	Supply	Ripple (V_{pk-pk})	Noise (V_{rms})
3.1	5 V	16.30 mV	1.51 mV
	3.3 V	15.60 mV	1.32 mV

of magnitude from Revision 3.0 to Revision 3.1, using 24-bit ADCs results in voltage measurements determined at a granularity of 5 V $\div$ 2^{24} $\approx$ 3 µV per step. Therefore, nearly 5,400 steps, or 12.5 bits of data, are corrupted by noise introduced by the power supply. This means only 11 of the 24 bits are estimated to be noise free, which only allows for correct measurements at the granularity of 5 V $\div$ 2^{11} $\approx$ 2.4 mV per step.

The second concern addressed was the sampling rate of the employed ADCs, the ADS1256. As the goal of the system is to measure 100 fps (i.e., 100 k voltage measurements per second), it was originally thought that by utilizing four 30 ksps ADCs in a parallel fashion the achievable data rate would exceed the desired specification (4×30 ksps $= 120$ ksps). Such a parallel design requires four SPI modules on the main microcontroller. The TI MSP430F5529 supports four hardware SPI modules. However, since the digital potentiometers in the current source design occupy one of the SPI modules, an additional SPI interface would require ancillary software design (bit banging). Therefore, the resulting ADC hardware/firmware was designed to take measurements in a serial fashion. This choice was made to keep the design simple, but ultimately lead to a slower sampling rate than desired. As discussed in Section 2.3.3, the overall measured sampling rate is 565 voltage measurements per second, less than 1% the desired rate. This sampling rate includes the added overhead of data transfer to the host computer.

These two system inadequacies provided the motivation for a successive revision. However, before the next revision was completed, it was also desirable to determine the general correctness of Revision 3.1. While functionality had been confirmed by the ability to collect and transmit EIT measurements according to specified injection patterns, the accuracy

and precision of those measurements had not yet been performed. Furthermore, EIT reconstruction results were infeasible at the time due to challenges regarding incompatible specimens with the EIT reconstruction algorithms. Therefore, to determine the correctness of the 3v1 DAS, measurements were taken on a shared specimen with both the LGDAS and the 3v1 DAS. Once the measurements were obtained, the raw data was compared between the two systems, using the LGDAS as the baseline measurement, since it had already been proven for correctness previously [24], [25] . It was found that the 3v1 DAS has an average bias of 21.1 mV from the LGDAS, with a standard deviation of 6.8 mV, as seen in Table 2.3. It was thought that a consistent offset might not pose an issue regarding relative measurements, but such a large standard deviation would certainly introduce challenges in being able to correctly identify and localize relative changes on an observed specimen.

2.3.5 Revision 4.0

Though Revisions 3.0 and 3.1 yield functional EIT DAS modules, these units do not meet the desired data collection rate and current source specifications for the system. Despite the improvements already achieved with the Revision 3.1 design [32], the shortcomings motivated a successive revision.

At this point in the design process the three main technical challenges were to increase data collection rate, improve the quality of the measurements taken, and increase the current source range. To begin, a new design was explored that makes use of a single ADC and improves the data collection rate and quality of measurements by improving the SNR of the measurements. For this design to work, another analog switch was added to direct each of the 32 electrode's inputs to the new single-terminal ADC, as shown in Figure 2.3.

Recall that the previous ADC, the ADS1256, is a sigma delta ADC architecture, which has a maximum sampling rate of 30 ksps. With a desired data collection rate of 100 ksps, such speed could not be achieved with the ADS1256 triggering in serial fashion. Therefore,

Table 2.3. Revision 3.1 Measurement Statistics

System	Std. Dev.	Bias
Revision 3.1	6.8 mV	21.1 mV

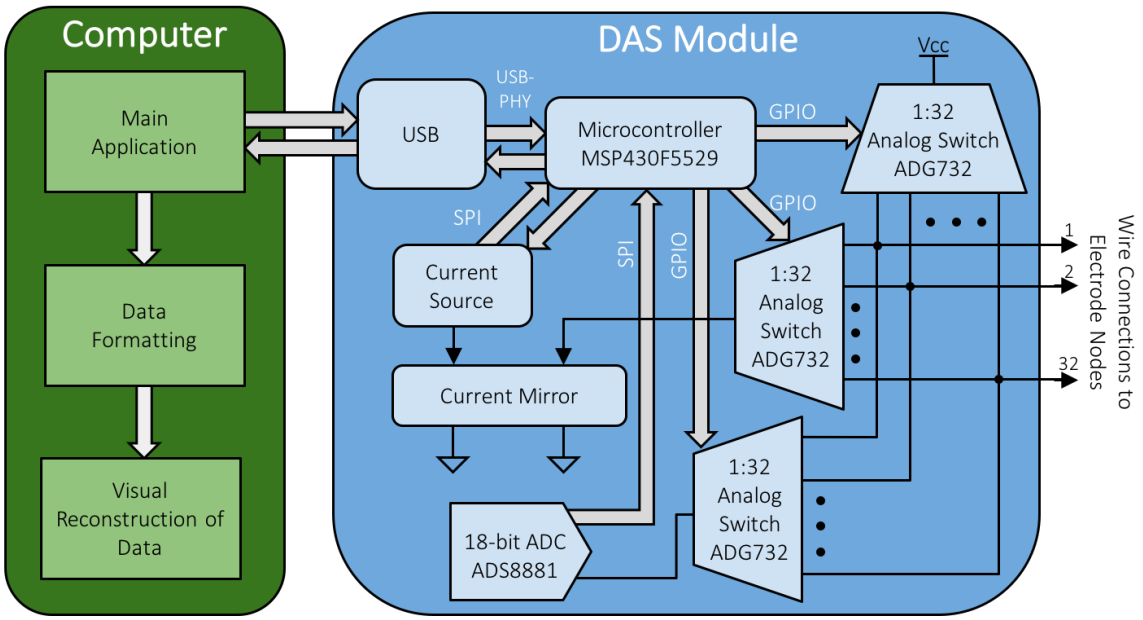

Figure 2.3. Revision 4.0 introduces the TI ADS8881 ADC and additional analog switch to increase the data collection rate.

research for a faster ADC was undertaken. During the research process, two things were discovered: i) the sigma delta architecture is inappropriate for this application, as sigma delta architectures are typically employed in continuous sampling applications [35]; and ii) as the sampling rate of the ADC increases, the number of analog inputs, or channels, on the ADC chip tend to decrease.

Given the first discovery, further research was performed to determine the correct ADC architecture, which suggests a successive approximation register (SAR) architecture for this application [33], [35]. This type of architecture is useful for applications where a specific, directed sample is desired. Modern day SAR ADCs provide up to 18 bits of data at sampling speeds in the mega samples per second range. While searching for high-resolution, faster than 100 ksps capabilities and SAR architecture, the component choice was narrowed between two ADCs: the TI ADS8881 and the Analog Device AD7984. To determine which ADC to use to in the forthcoming revision, an intermediate ADC development board was designed to determine ease of use and accuracy of each ADC.

During the process of designing and developing the ADC development board, several design improvements were achieved. First, the design of the power supply was

significantly improved. Referencing the AD7984 datasheet, low drop-out regulators are recommended for the power and reference supply designs. These regulators are power inefficient relative to their switching regulator counterparts, but introduce relatively low noise. Reducing the noise on the power supply lines and the reference voltage for the ADC helps improve the SNR of the measurements and the quality of the EIT reconstruction results.

Second, appropriate signal conditioning circuits for the SAR ADCs are required, as such conditioning is not performed on-chip. These circuits were taken directly from each ADC's respective datasheet to guarantee low latency, sufficient signal differential amplification and proper buffering. These circuits require the use of additional COTS components, but proved critical in improving the SNR of the measured voltages.

Third, care was taken during this design to improve the layouts of both the microcontroller and supporting circuitry (including JTAG programming header and USB circuitry). These improvements ultimately lead to better separation of analog and digital signals and reduced layout footprint. Keeping digital and analog signals separate helps reduce the effect of high-frequency digital lines seen on the analog measurements, and ultimately helps improve the quality of the EIT reconstruction results.

The new power supply design was characterized for noise, as seen in Table 2.4. With an 18-bit ADC at a 5 V reference, the granularity of each step relates to $2 \times 5\text{ V} \div 2^{18} \approx 19\ \mu\text{V}$ (note that the readings are interpreted as two's complement numbers). This means that 172 measurement steps, or 8 bits, are essentially rendered unusable due to the power supply noise. This design therefore anticipates only 10 bits of noise-free data, allowing for accurate measurements at the granularity of 4.88 mV, a 35% improvement from Revision 3.1.

Ultimately, the TI ADS8881 was selected for use with the next revision (Revision 4.0) due to its ease of use and measurement accuracy. Although the ADS8881 boast the ability

Table 2.4. Power Supply Noise Characterization for Revision 4.0 (Unloaded)

Version	**Supply**	**Ripple (V_{pk-pk})**	**Noise (V_{rms})**
4.0	5 V	3.26 mV	308.0 µV
	3.3 V	3.27 mV	300.0 µV

to sample at up to 1 Msps, this is largely dependent on the rate at which the measured data is shifted out. To achieve 1 Msps, a 70 MHz master clock would have to be provided on the SPI interface to shift out data. As the microcontroller can only support up to a 25 MHz system clock, and will be operating on a 4 MHz clock for testing, the design is expected to suffer in sampling frequency. However, future performance improvement for this device should be achievable simply by swapping the 4 MHz crystal oscillator for a higher frequency oscillator and updating the appropriate USB drivers.

During this time, the current source was also improved. A second constant current source was added in parallel with a switch connection to allow for the additional range on the current source to expand from 1 µA–100 mA to 1 µA–200 mA. This design aims for better control over the current source by introducing a course grain tuning with the new source and maintaining fine grain tuning with the already implemented current source. With these improvements made, Revision 4.0 represents the latest DAS module, and its detailed characterization is provided in Chapter 3.

2.4 Firmware Design

Firmware is permanent software programmed into read-only memory and is application specific. In this application, the firmware is the binary program, stored in on-chip flash memory, that will be executed by the central microcontroller to control the process and execution of performing EIT measurements. The firmware for this system was developed entirely in the C programming language.

There are three main aspects to this application's firmware:

1. Communication with a host computer
2. Subsystem communications
3. Measurement control

2.4.1 USB Communication and Packet Protocol

Due to its ubiquity, USB was chosen as the main method of communication with the host computer. As explained in the hardware discussion of this paper, the microcontroller that was elected for this system, the TI MSP430F5529, was chosen for its communication abilities, including an integrated USB 2.0 physical layer and USB-PLL (phase-locked loop).

By using USB 2.0, each DAS module could theoretically communicate up to 12 Mbps over a secure channel with the host computer. A simple USB hub would then allow for multiple DAS modules to be connected as a larger, modular EIT system.

Raw USB development can be very challenging. Fortunately, TI provides a great deal of support for this particular family of microcontrollers, including developer support for USB drivers and protocol. This greatly simplifies the USB implementation. With the installation of a custom USB device driver for the application, a host computer can properly connect to the DAS module for a secure communication channel.

As seen in Figure 2.4, the USB connection status maintains the highest priority in the DAS module subsystem. Instructions can be carried out only when the USB status reports connected. When disconnected, the DAS module tries to reconnect itself with the host. If

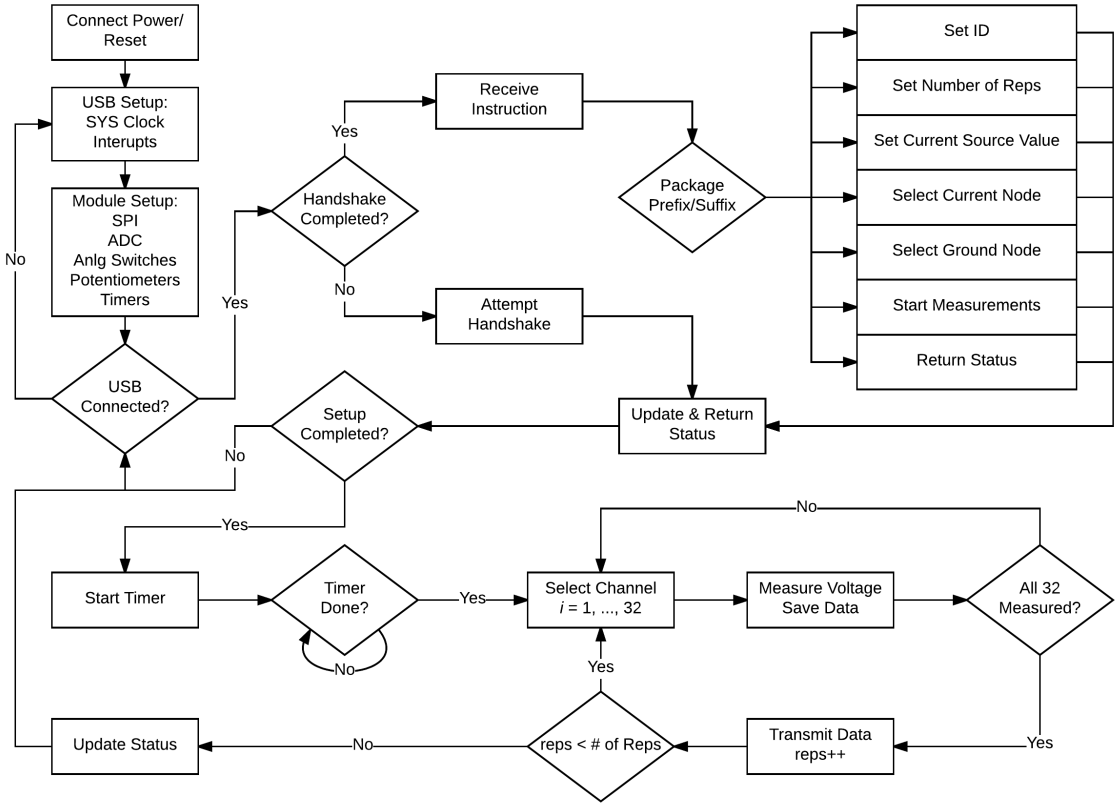

Figure 2.4. Firmware flow diagram for Revision 4.0. The firmware consists of three main aspects: i) communication with host computer via USB; ii) system communications (SPI, GPIO); and iii) measurement control.

the connection cannot be achieved, the DAS module eventually enters a low-power mode to conserve energy.

Upon connecting to the host, the DAS module waits to receive a handshake. This helps ensure that the DAS module communicates specifically with the custom software designed for this application. This handshake is simplified to consist of only two single-byte transfers from the host computer, interleaved with two single-byte acknowledgments from the DAS module. Each byte transfer is referred to as a "magic number," and is specifically selected as an uncommon or nontrivial bit sequence to prevent unintentional handshakes with other software. In the case of this application, the magic numbers sent by the host are bytes 0xDE and 0xAD, and the acknowledgments from the DAS module are bytes 0xBE and 0xEF.

With the USB connected and handshake complete, the DAS module is then ready to receive instructions from the host computer. The instructions, sent in packets, are used to setup the DAS module preparatory to performing measurements and to trigger the measurement process. In order to distinguish each instruction, a packet protocol was established. Unique packet prefixes and suffixes identify each instruction, and a DAS module ID identifies the instruction's intended DAS module when multiple modules are connected to the system. This protocol doubles as a means for error detection, as each packet is checked for both valid prefix and suffix before the instruction data is evaluated. The structure of the instruction packet is shown in Table 2.5. A list of instruction packet prefix and suffix pairs is provided in Appendix B.

As each instruction is received and executed, or if miscommunication occurred, a status packet is then sent back to the host containing the updated status and error codes for the DAS module. The structure of the five byte status packet is shown in Table 2.6, and a full list of statuses and error codes is provided in Appendix B. Once all the instructions needed to set up the DAS module have been received and executed, the DAS module status reflects that the measurement process can execute.

To start the measurement process, the host computer sends an instruction to the DAS module triggering it to start measuring. Once all the measurements have been performed for each connected electrode, the data is sent back in packets, 99 bytes in size ($3\ bytes/electrode \times 32\ electrodes = 96\ bytes$). This process is repeated for the specified

number of averaging samples. The DAS module ID is used to help the host computer identify the relative location of the measured data within the whole system. The structure of the measured data packet is shown in Table 2.7.

2.4.2 Subsystem Communications

As the central orchestrator of the measurement process, the microcontroller needs to be properly configured to control each digital component of the DAS module. Aside from the USB communication, three main component communication schemes are set up using the universal communication modules available on the MSP430F5529 and other GPIO pins. The components that will occupy the communication schemes include the ADC, digital potentiometers, and analog switches.

Two SPI modules are occupied in this application, one by the TI ADS8881 ADC, and the other by three different digital potentiometers used to control the value of the current source. The MCU's integrated hardware SPI modules make communication setup with the ADC and digital potentiometers straightforward, with each setup referencing the SPI protocol (found in the datasheet) for each component. For the digital potentiometers, three different chip select signals are included in the SPI protocol to direct communication to each potentiometer independently.

From the remaining GPIO pins on the MCU, a total of 32 pins are configured to control each of the 32x1 analog switches. The GPIO pins on the MCU were carefully selected to

Table 2.5. Instruction Packet Protocol

Instruction[0]	Instruction[1]	Instruction[2]	Instruction[3]	Instruction[4]
Prefix	ID	Data_0	Data_1	Suffix

Table 2.6. Status Packet Protocol

Status[0]	Status[1]	Status[2]	Status[3]	Status[4]
Prefix = 0xAE	ID	Status	Errors	Suffix = 0xAF

Table 2.7. Measured Data Packet Protocol

Data[0]	Data[1]	Data[2]	...	Data[97]	Data[98]
Prefix = 0xBE	ID	Data_0	...	Data_95	Suffix = 0xEF

simplify the layout and routing of physical traces. A total of eight more GPIO pins are used to control six additional 2x1 analog switches and two LEDs.

2.4.3 Measurement Control

As seen in Figure 2.4, once the DAS module has received all the instructions necessary for setup, it can begin taking measurements. The method for taking measurements is straightforward—loop through all 32 electrodes and sample the voltage at each electrode. Each voltage sample is saved into a data array that is then transferred back to the host computer as part of the measured data packet. This process is repeated for as many averaging samples, or repetitions, as was specified by the user through the "Set Number of Repetitions" instruction.

Once the measurements have been performed for the number of specified repetitions, the DAS module status is reset such that the host is required to send a new pattern (current/ground electrode pair) and trigger the measurement process. Since the DAS module ID, number of repetitions, and current value are not expected to change, this process can occur relatively quickly.

An important discovery about the current source behavior was made while observing the measurement process. It was found that each time a new projection was executed (i.e., each time the analog switches connecting either the current injection electrode or the grounded electrode switched channels) the current source would shut down. This behavior is caused by the introduction of a brief open circuit. Once the switching on the analog switch is complete, the current source ramps back up to the desired value. Because of this behavior, a timer was introduced into the firmware design to allot enough time for the current source to rise to the correct value before proceeding to take measurements.

Figure 2.5 shows the shut down of the current source and its corresponding rise time after the switch closes at time 0, for five different target current values. This observation was made by observing the voltage across a fixed resistor yielding an approximate 4.5 V drop relative to the observed current. Based on these results, a generous 4 µs wait interval was introduced to stall the beginning of the measurement process until after the second electrode switch was completed. This was done to eliminate any potential data skew.

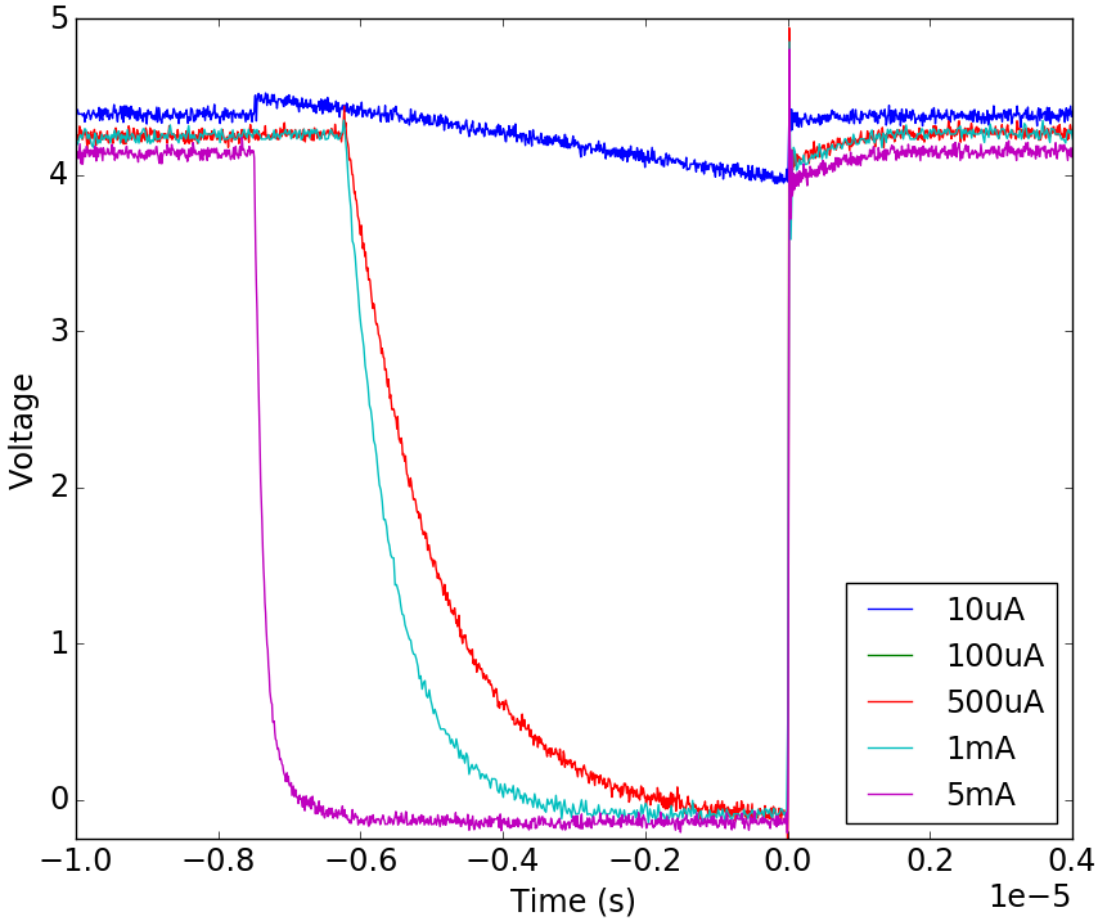

Figure 2.5. The switching between electrodes introduces a brief open circuit, causing the current source to shut down. The rise time (after the switch closes at time 0 s) for five different current values was evaluated. Generous rise time was determined to be approximately 4 µs.

2.5 Software Design

Referring to the system design as shown in Figure 2.3 (pg. 14), the second aspect of the EIT DAS is the software. As customary, the software design consists of two components: i) the front end and ii) the back end. The front end software is the presentation layer, or graphical user interface (GUI), while the back end software is the data access layer, or the software that controls USB communication and performs data manipulation.

It is important to note that the majority of the software aspect of the system was previously developed during the senior capstone project. Therefore, only a brief discussion of functionality and relative updates is provided.

For the front end software, a custom GUI provides user control. The GUI, as shown in Figure 2.6, was developed entirely in the C# programming language for the following reasons:

1. Language familiarity
2. High-level object oriented language with large .NET support
3. Simple and elegant GUI development

The GUI provides the user the following abilities, as desired by the design specifications:

1. Load predefined current injection patterns
2. Determine where to save data files
3. Receive visual feedback of data collection progress
4. Inform user of DAS module statuses

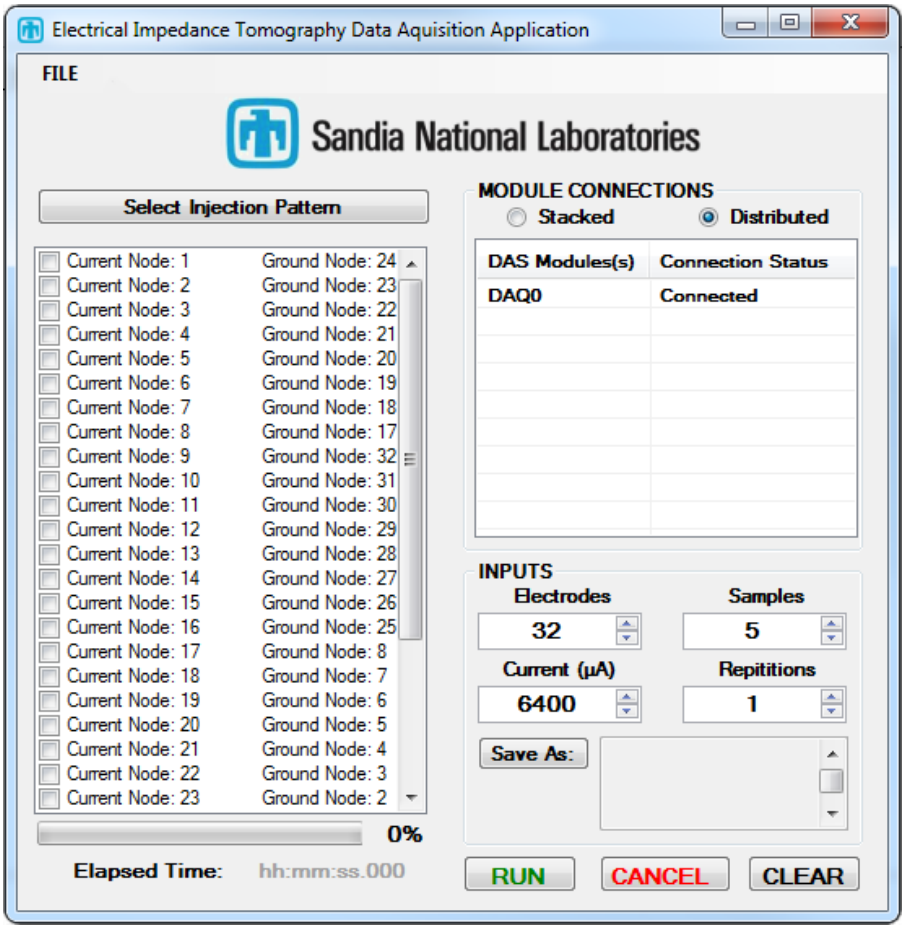

Figure 2.6. The most recent version of the EIT GUI, compatible with the Revision 4.0 DAS.

While much of the EIT measurement process is embedded in the DAS module firmware, the software back end is responsible for controlling all the instructions that get sent to the DAS modules. Therefore, the back end software essentially acts as the dual of the firmware. The back end sets each DAS module's ID, keeps track of each connected DAS module's status, transmits user defined current values, number of averaging samples, and injection patterns. In order to streamline these responsibilities, an instruction order was determined so that orchestrating large, modular systems might be simplified. This order is listed in Appendix B.

For modularization support, the back end utilizes each DAS module's ID in order to set current and ground electrodes, as only two electrodes are ever set a time for a given pattern, even for larger systems. Since each DAS module requires its status to register complete before taking measurements, the back end also identifies which modules do not have electrodes set, and updates their statuses (virtually confirming current/ground nodes set) so measurements can still occur. The start measurement instruction was introduced so that all DAS modules could start measuring once the trigger was received, rather than measuring each module in a serial fashion. The DAS module ID is also used to sort the data for post measurement data formatting.

Finally, the back end is also responsible for correctly formatting the measured data into a CSV output file that can later be read by the EIT reconstruction algorithms. Note that the EIT algorithms are independently controlled from this EIT application.

Minor updates were made to the back end as hardware and firmware updates were also made.

2.6 EIT Measurements

In order to perform EIT measurements, nine fixed specimens were created on 6 in^2 G-10 FR-4[1] coupons. A 4.5 in^2 conductive region made from spray-deposited carbon black paint was then used to emulate predefined damage patterns onto eight of the nine specimens. One specimen's conductive region was painted entirely to emulate a pristine specimen without damage. This fully painted specimen, marked as the "Master" specimen, would

[1] G-10 FR-4 is a thermosetting industrial fiber glass composite laminate.

serve as the baseline specimen for detecting the relative change in conductivity due to damage in the other specimens. Emulated damage patterns consisted of a moving sequence of a 0.25 in^2 square, a single cross region, and regions of differing layers of paint, as seen in Figure 2.7.

A square test fixture, shown in Figure 2.8, was also created using a CNC laser cutter to cut two pieces of 1/16 in thick acrylic. Eight small holes were cut along each side, spaced 0.5 in apart. Thirty-two small, spring-loaded electrical contacts were then inserted into each cut hole and sandwiched between the two cut pieces of acrylic. Each connector was then soldered to an independent wire on a ribbon cable terminating in a 37-pin D-SUB connector, providing a standardized interface connection that can be used with both the LGDAS and 4v0 DAS. In this configuration, each specimen was measured by physically placing the test fixture on top of the specimen and stacking a small two-pound weight on top of the test fixture backing so that each spring-loaded electrode would maintain contact with the specimen.

The injection pattern used for all of the EIT measurements in this master's thesis consists of 32 projections between two electrodes directly across from one another, as seen in Figure 2.7 (a), where each blue line represents a single projection (i.e., current/ground node pair). The electrode pairs for said injection pattern are given in Appendix C.

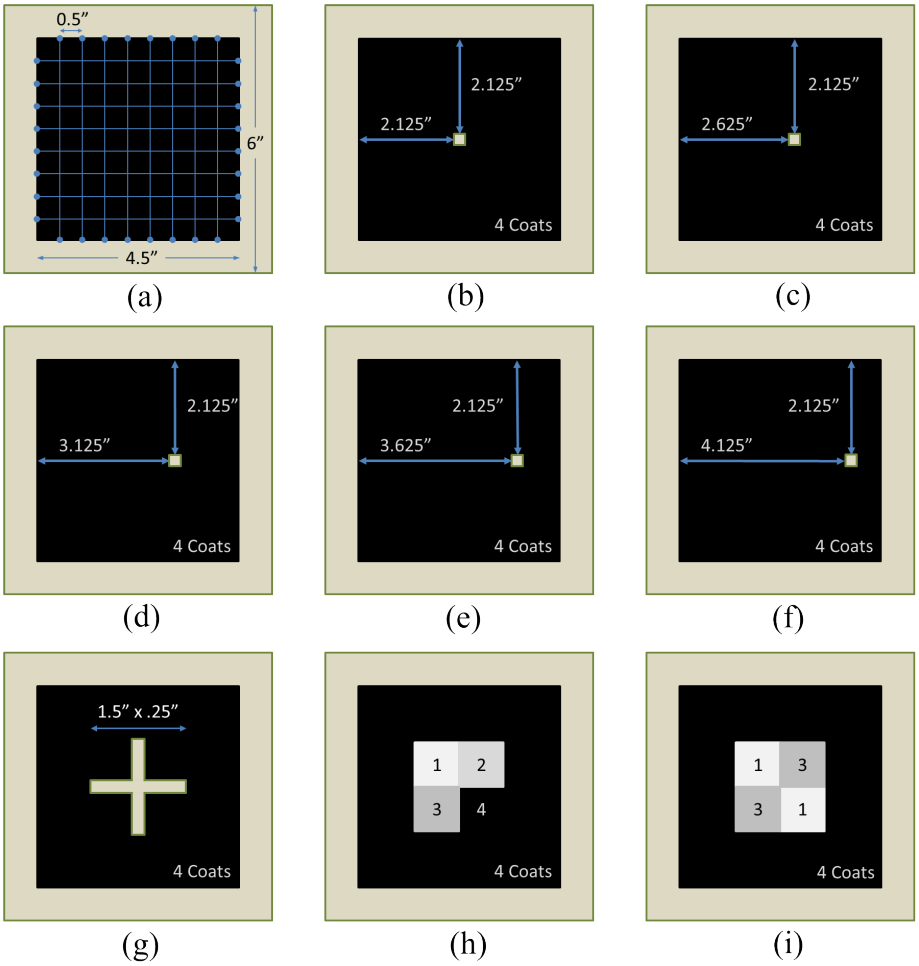

Figure 2.7. (a) "Master" specimen with no emulated damage. The blue dots represent the contact points for each of the 32 electrodes. The blue lines represent the injection pattern projections. (b) "Moving Square 0" (MS0) with a 0.25 in^2 "hole" centered in the specimen. (c) "Moving Square 1" (MS1) with the 0.25 in^2 hole shifted 0.5 in from center. (d) "Moving Square 2" (MS2) with the 0.25 in^2 hole shifted 1.0 in from center. (e) "Moving Square 3" (MS3) with the 0.25 in^2 hole shifted 1.5 in from center. (f) "Moving Square 4" (MS4) with the 0.25 in^2 hole shifted 2.0 in from center. (g) "Cross" damage pattern. (h) "Patches 1:2:3:4" with regions of differing layers of carbon black paint to emulate regions of differing conductivity. (i) "Patches 1:3" with regions of differing layers of carbon black paint.

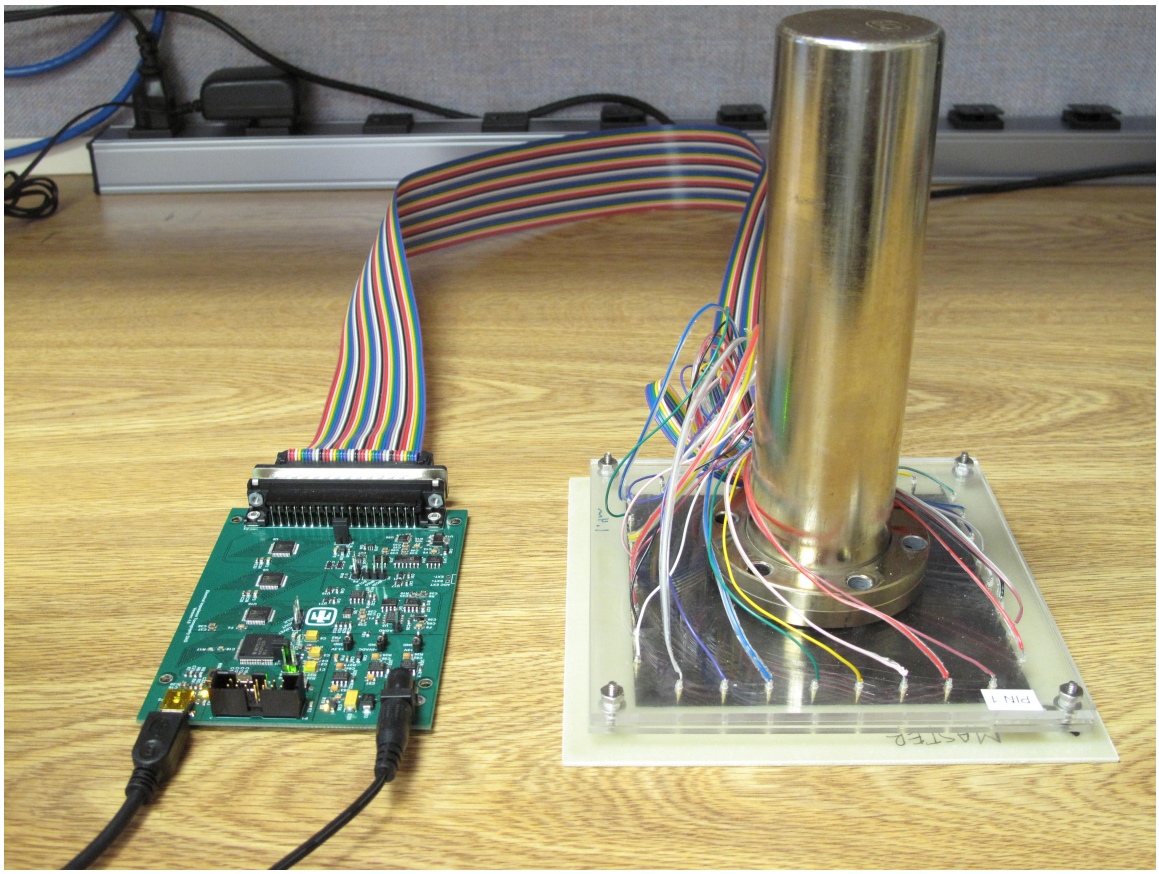

Figure 2.8. A custom test fixture was created using laser cut acrylic to hold spring-loaded electrical contacts. Each electrical contact was soldered to the appropriate wire of a ribbon cable terminating in a 37-pin D-SUB connector to interface with both the DAS module and LGDAS. A two-pound weight was used to compress the spring-loaded contacts to the sensing area.

CHAPTER 3

RESULTS AND DISCUSSION

With the completion of hardware, firmware, and software for Revision 4.0, timing, accuracy, and precision characterizations were performed. EIT measurements were taken for three different predefined damage patterns with both the LGDAS and 4v0 DAS. The reconstructed tomography from both systems is compared. An evaluation of cost, form factor, and other design specifications is also presented.

3.1 System Timing and Data Acquisition Rate

Timing analysis is important to identify potential bottlenecks in the system. Therefore, each aspect of the communication, execution, and measurement processes were timed to determine overall performance. It is important to note that timing analysis was performed for a DAS module operating on a 4 MHz system clock.

Frame rate analysis was first performed using the C# GUI. However, an important discovery was made during the observation of the software's USB communication. With a DAS module connected, a USB analyzer was used to observe the packet transfers between the host and the DAS module. This revealed that the host occasionally floods the communication channel with transfers to the DAS module. Since USB 2.0 is a half-duplex communication scheme, data can only be transferred in one direction at a time. Therefore, an infinite stall would then follow as the DAS module could not send back updated status packets. A quick hack to solve this problem was introduced into the back end software such that the software would sleep for a short interval to allow the DAS module to communicate its updated statuses. Since this hack would skew any true timing analysis for the system, it was then decided to perform timing characterization using a software interface written in Python. Table 3.1 shows the timing analysis for each instruction needed to perform EIT measurements. Clearly the handshake, setting the current source value, and

Table 3.1. Timing Characterization for Revision 4.0.

Action	Python (s)	MCU Cycles	MCU Time (s)	Overhead (s)
Handshake	0.002309628	6586.7	0.001646675	0.000662953
Set DAS module ID	0.00099296	1436.9	0.000355923	0.000633739
Set Num. Reps	0.001007818	1423.0	0.00035575	0.000652068
Set Crnt Val	0.002993462	9631.8	0.00240795	0.000585512
Sel Crnt Node	0.001021756	1489.1	0.000372275	0.000649484
Sel Gnd Node	0.00971782	1438.1	0.000359525	0.000612257
Measurement Process	0.00260954	7106.33	0.001776583	0.000832957

performing measurements are the most time consuming task in the process. Fortunately, the handshake and setting the value of the current source only need to happen once, so their timing eventually loses significance for large injection patterns.

As seen in Table 3.1, the measurement process is characterized for a total of one averaging sample. However, as the number of averaging samples increases, so does the time of the measurement process. Since the number of averaging samples directly affects the EIT frame rate, timing analysis was performed to determine the EIT frame rate relative to averaging samples, and the relationship is shown in Figure 3.1. According to this data, there is an approximate 68.629 ms increase per additional averaging sample. The overall frame rate is then calculated as 5 fps for a single averaging sample—meaing 5 k voltage samples per second. For five averaging samples, the frame rate is 2 fps—meaning 10 k voltage samples per second. For 40 averaging samples, the frame rate is 0.34 fps—meaning 13.6 k voltage samples per second. This clearly shows that the overhead of switching current/ground electrodes and waiting for the current source to rise after each switch has a significant effect on the frame rate for lower averaging samples. Inversely, the overhead of the data transfer reduces as the number of averaging samples increases. Unfortunately, the measured frame rates do not achieve that of the design specification—100 fps—which would require 100 k voltage samples per second. However, with five averaging samples, the data collection rate is almost a 200% increase from the LGDAS, which measures just 56 voltage samples per second.

It is important to recall that these measurements were taken with a DAS module system clock of 4 MHz and that the DAS module has the potential to run on a 25 MHz system clock. The increased clock rate would certainly improve MCU timing and measurements,

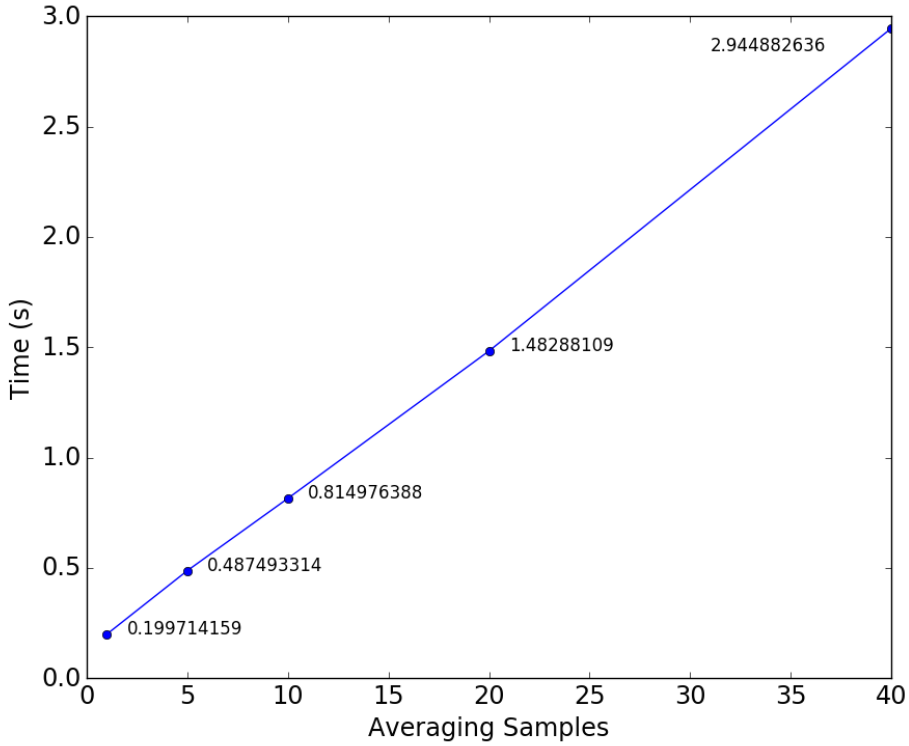

Figure 3.1. There is a linear relationship between the number of averaging samples and the overall EIT frame rate.

although the communication overhead would remain constant. Future work includes increasing the system clock rate, analyzing the EIT reconstruction results, and determining the faster system timing.

3.2 Measurement Accuracy and Precision

More important than the EIT frame rate is the accuracy and precision of the measurements taken. Accuracy is important so that the measured data correctly represents the observed specimen. Precision is important because EIT is a relative methodology. Therefore, a small standard deviation of measured values is extremely desirable. Even at a high frame rate, if the data are not precise and accurate, then the EIT measurements would prove useless.

To perform accuracy and precision characterizations, a discrete load was used, as this is a standardized approach used to evaluate EIT systems [28], [36]–[38]. A custom PCB

was designed to connect a DAS module to a discrete resistor ring, so that all 32 electrodes would be separated by a single fixed resistor value. Using this method, it was then possible to calculate the true value of the voltage at each electrode given the value of each resistor and the value of the injected current.

For a current value of 815 µA, a 560 Ohm resistor value was chosen to populate all 32 resistors so that the largest voltage potential to be measured would remain below 4.5 V. Figure 3.2 (a) shows the calculated expected values of the 560 Ohm resistor ring for a single frame. For comparisons with the true values of the resistor ring, data for 10 frames were collected. Figures 3.2 (b) and (c) show the measured RMS values of the resistor ring with both the LGDAS and the 4v0 DAS, respectively, determined from the 10 measured frames. Accuracy is the closeness of the measured value to the known, or true value. Therefore, to compare the accuracy of both systems, the bias plots of both systems are shown in Figures 3.2 (d) and (e). It is clear that the LGDAS has a lower bias than the 4v0 DAS by nearly fivefold. Interesting are the voltage biases of the 4v0 DAS seen in injections 10–20 of Figure 3.2 (e). While the high bias voltages may seem alarming, as long as the bias remains constant, then the relative change seen in the EIT reconstruction should theoretically prove accurate. Moreover, the bias voltage can be used as a calibration method for the measured values to provide more accurate data for absolute EIT applications.

Precision is the closeness of two or more measurements to each other. Therefore, the precision is then determined by calculating the standard deviation of each measurement across the 10 measured frames. Figure 3.3 shows the calculated standard deviation for both the LGDAS and the 4v0 DAS. The 4v0 suffers up to a 2.25 mV standard deviation, while the LGDAS has a maximum standard deviation of only 45 µV, outperforming the 4v0 DAS by up to fiftyfold. Thus, it would be expected that the 4v0 DAS would not provide as pronounced of a change in the relative conductivity of the sensing region.

To determine the effectiveness of the measurements taken, especially for the 4v0 DAS, the SNR was determined for each DAS. The measurement was performed by sweeping several current values across an appropriate fixed resistance. To extend the range of voltage measured, three different resistor values were used for three different current ranges: 45 kOhms for 10 µA–100 µA; 4.5 kOhms for 100 µA–1 mA; 900 Ohms for 1 mA–5 mA. Current values were incremented by a factor of 10 for both the 10 µA–100 µA and 100

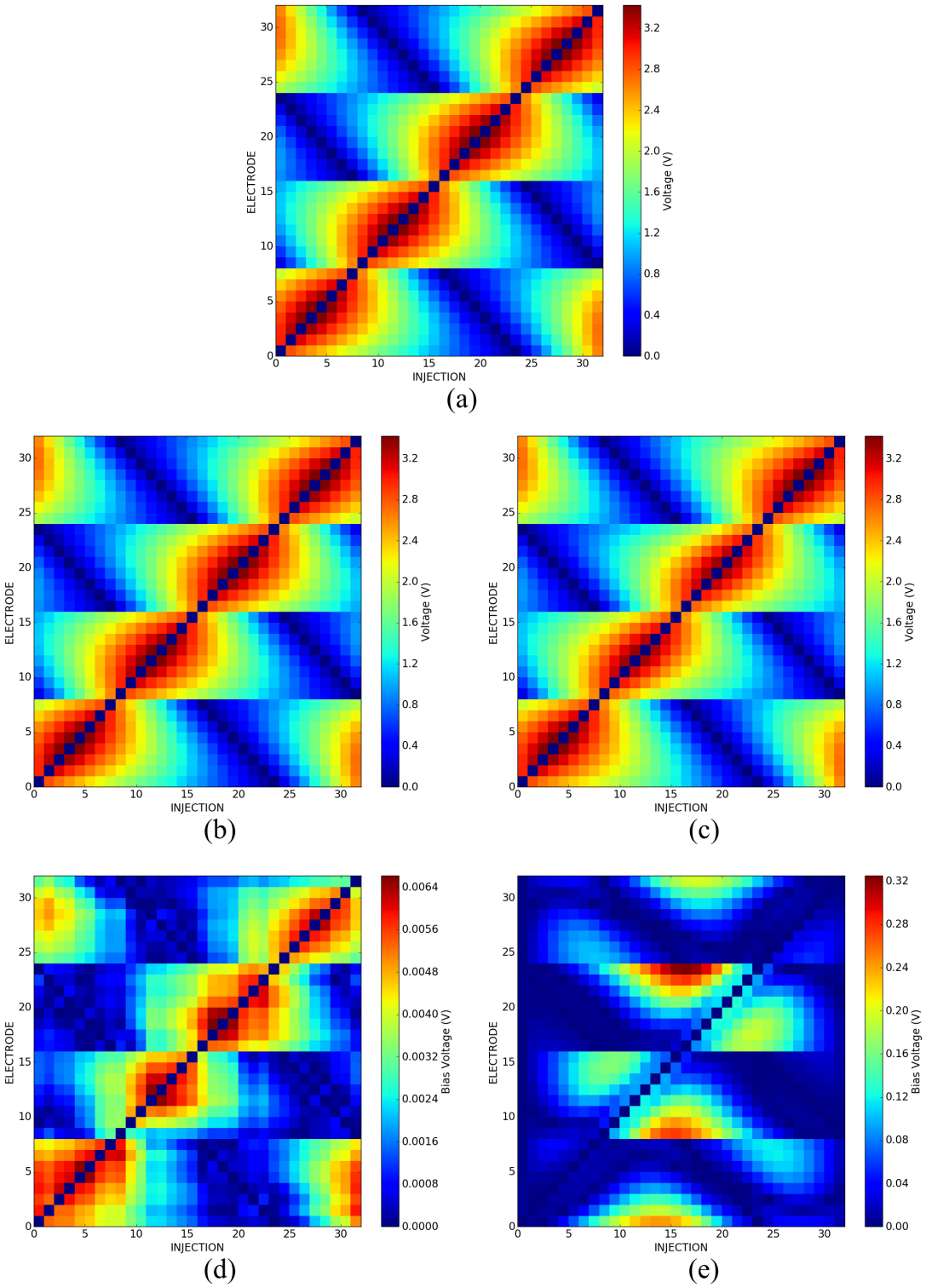

Figure 3.2. Calibration was performed using a resistor ring composed of 32 560 Ohm resistors. Each plot represents the voltage value at the 32 electrodes for 32 patterns using 1 mA current. (a) Calculated true voltage value; (b) Measured RMS voltage value from the LGDAS; (c) Measured RMS voltage value from the 4v0 DAS; (d) Bias plot for the LGDAS; (e) Bias plot for the 4v0 DAS.

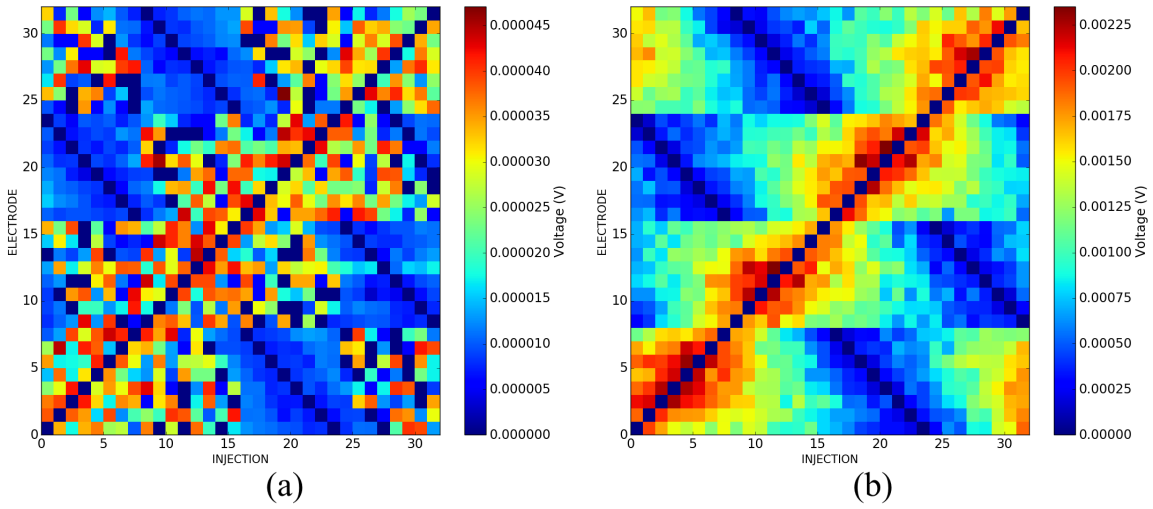

Figure 3.3. The standard deviation for each electrode across 32 patterns was determined across 10 frames. (a) Standard deviation for the LGDAS; (b) Standard deviation for the 4v0 DAS.

µA–1 mA ranges, and by increments of 1 mA for the 1 mA–5 mA range. For each value of current, repeated measurements were performed (i.e., the signal averaging factor was set to $N = 100$). The RMS value and the standard deviation were used to determine the SNR, as seen in the following equation [39]:

$$SNR = 10 \times \log_{10}\left(\frac{V_{RMS}}{\sigma_{NOISE}}\right) \tag{3.1}$$

where

$$V_{RMS} = \sqrt{\frac{1}{N}\sum_{n=1}^{N} V_n^2} \tag{3.2}$$

and

$$\sigma_{NOISE} = \sqrt{\frac{1}{N}[(V_1-\mu)^2 + (V_2-\mu)^2 + ... + (V_n-\mu)^2]}, \text{ where } \mu = \frac{1}{N}(V_1 + ... + V_n) \tag{3.3}$$

For signals of lower voltage, it is expected that any sources of noise might interfere with the readings. As seen in Figure 3.4, the SNR for either DAS is greatest in the upper voltage region. The 4v0 DAS has an SNR between 20-43 dB while the LGDAS maintains a higher SNR that ranges from 40-158 dB. The lower voltage regions are likely to pose a challenge for EIT reconstruction, as a low SNR makes true conductivity changes hard to detect, especially further away from the electrodes. As seen by other systems, it is desirable to maintain an SNR of greater than 70 dB [28], [39]. However, for a system design on a two-layer PCB, the SNR can be expected to improve by moving towards a multilayer PCB with correct signal shielding and analog/digital separation to improve noise characteristics.

3.3 EIT Reconstruction

EIT data was collected from both the LGDAS and 4v0 DAS for comparison using the nine fixed specimens as shown in Figure 2.7. EIT reconstruction was performed on the

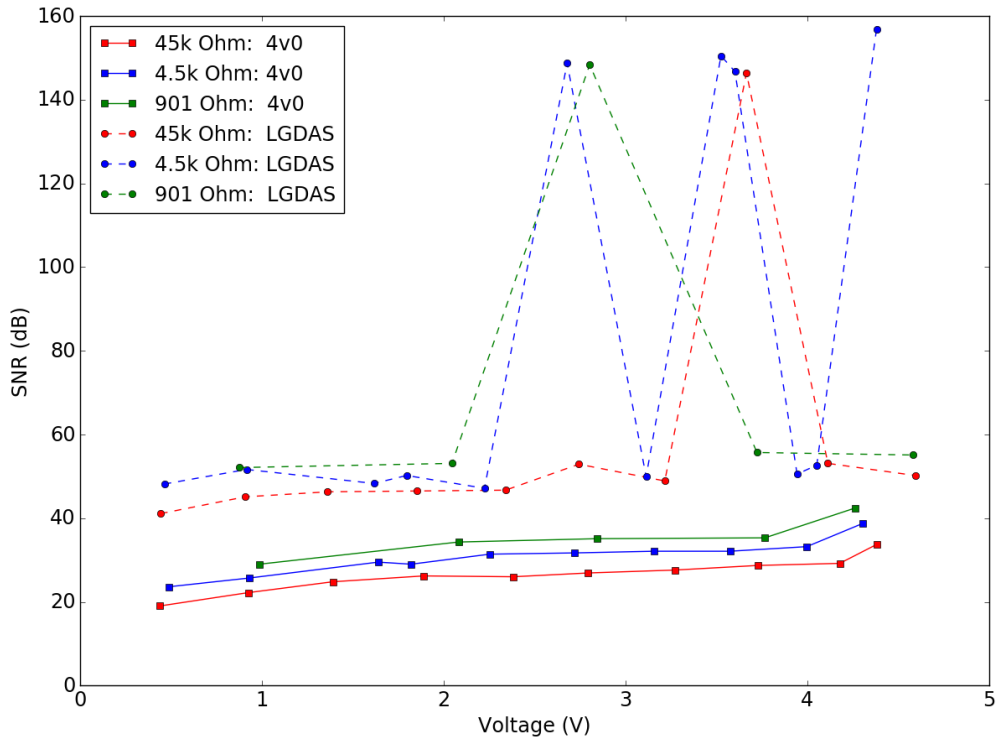

Figure 3.4. SNR comparison for currents ranging between 10 µA–5 mA. The corresponding resistor values were used for the following three current value ranges: 45 kOhms for 10 µA–100 µA; 4.5 kOhms for 100 µA–1 mA; 900 Ohms for 1 mA–5 mA.

measured data and the resulting images are shown in both Figure 3.5 and Appendix D. It is clear that the LGDAS produces a higher resolution image, capturing a more evident change in the normalized conductivity of the sensing region. However, the 4v0 DAS performs comparably well, identifying the same regions of predefined damage. These results show the promising potential of the 4v0 DAS as a low-cost system for SHM. At a fraction of the cost, size, and weight of the LGDAS, the 4v0 DAS can enable SHM monitoring in applications that were never previously possible with today's large and expensive EIT data acquisition systems.

3.4 System Design Specification Results

Recall the design specifications outlined in the Introduction. Table 3.2 shows the design specification results for three different systems, including Revision 4.0. From these results, it is clear that Revision 4.0 does not satisfy all the desired specifications, but it exceeds the unit cost, footprint, and power specifications desired by an SHM system. Furthermore, Revision 4.0 proves a near 200% increase in acquisition speed and a 40% decrease in price when compared to the LGDAS.

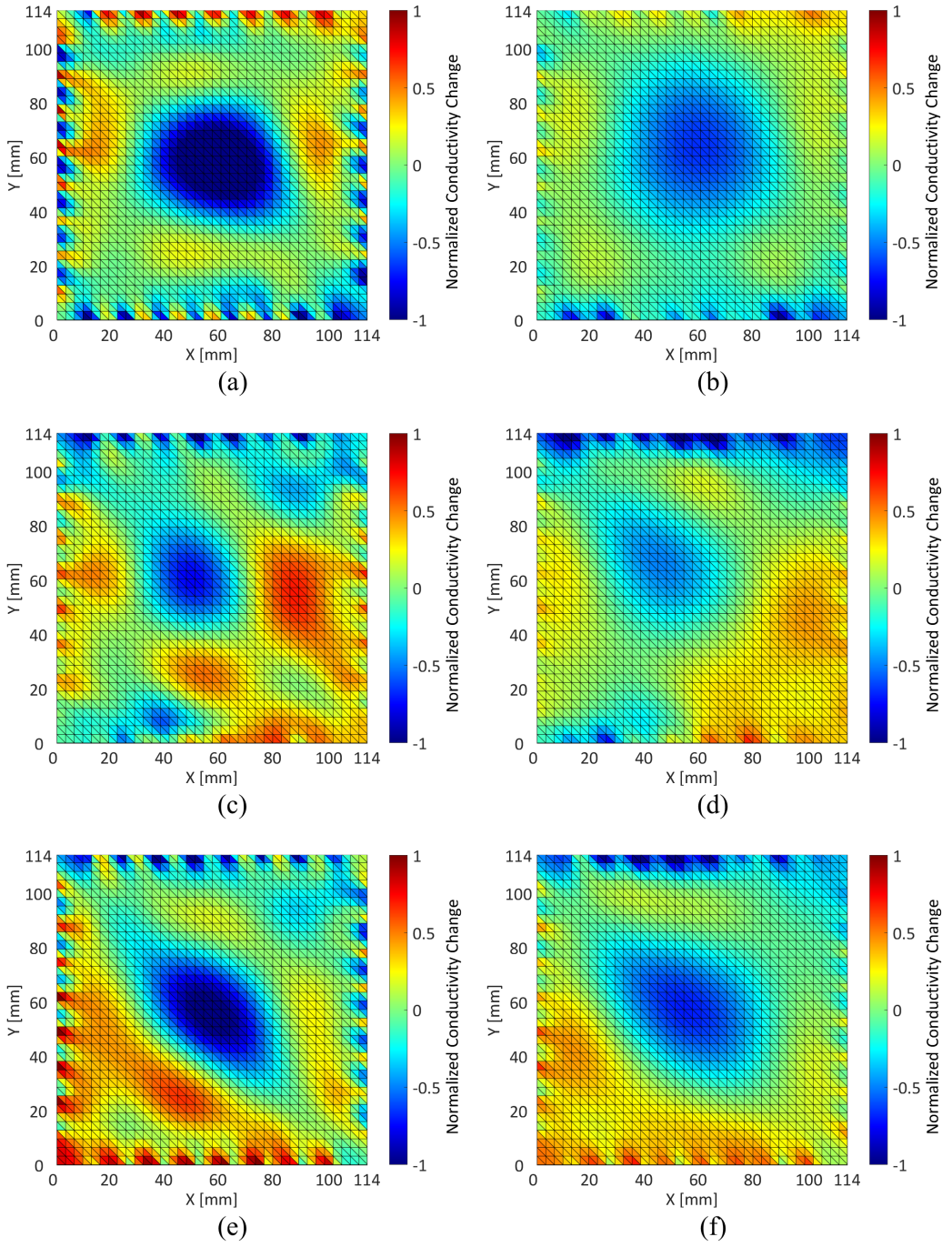

Figure 3.5. The EIT reconstruction results for three different predefined damage patterns. (a) Cross pattern EIT reconstruction for the LGDAS. (b) Cross pattern EIT reconstruction for the 4v0 DAS. (c) Patches 1:2:3:4 pattern EIT reconstruction for the LGDAS. (d) Patches 1:2:3:4 pattern EIT reconstruction for the 4v0 DAS. (e) Patches 1:3 pattern EIT reconstruction for the LGDAS. (f) Patches 1:3 pattern EIT reconstruction for the 4v0 DAS. These results show the 4v0 system is comparable to the LGDAS for identifying the general size, location, and severity of the damage.

Table 3.2. Design Specification Results: 4v0 vs 3v1 vs LGDAS

Specification	**Desired**	**4v0**	**3v1**	**LGDAS**
Voltage Meas/s	100 k	10 k	565	56
Unit Cost	<$1,000	$252	$422	apx. $10,000
Current Src Range	1 µA–100 mA	10 µA–100 mA	10 µA–10 mA	100 fA–105 mA
GUI	Yes	Yes	Yes	No
Size	—	15 in^2	16 in^2	420 in^2
Weight	—	<1 lb	<1 lb	apx. 50 lbs
Communication	Hardwire	USB 2.0	USB 2.0	USB 2.0
Operating Power	—	apx. 2 W	apx. 2 W	>10 W
Standby Power	—	apx. 0.1 W	apx. 0.1 W	—

CHAPTER 4

CONCLUSION

The lasting contribution of this work is the introduction of a low-cost, low-power, lightweight, and small form factor electrical impedance tomography data acquisition system that can be used for practical structural health monitoring applications outside of the laboratory setting. Fitting the palm of your hand, one system module is capable of taking 10,000 measurements per second, or 2 fps with a signal averaging factor of 5, at 10 bits of resolution. For the following three current ranges, the system achieves an average SNR of 26.4 for 10 µA–100 µA, 30.7 dB for 100 µA–1 mA, and 35.2 dB for 1 mA–5 mA. EIT measurements were performed with a single module on predefined damage pattern of size 4.5 in^2 and the results were compared to those of a laboratory-grade EIT data acquisition system. Even with less than ideal SNR, the reconstructed results were comparable for determining size, shape, and location of the damage within a bounded region. Using only readily-available commercial off-the-shelf components, this custom all-in-one system has an approximated module cost of only 250 USD. The combined performance and cost of this system validates its potential as an effective and low-cost SHM solution for a variety of new and existing applications.

4.1 Future Research

While the 4v0 DAS shows promising results, it does not yet achieve all of the desired specifications as an SHM system. Therefore, additional improvements for the future include increasing the data collection rate, improving the SNR, improving the current source control, and solving the modularity problem.

While the 4v0 DAS was able to achieve a low-cost solution, it is unable to perform at the desired frame rate. One solution to this problem, potentially requiring only a simple hardware change and firmware updates, is to improve the system clock of the MCU. By

improving from 4 MHz to 25 MHz system clock, instruction execution and data collection can happen at a much faster rate. Simplifying and improving the firmware for efficiency will also enhance system performance. The challenge will be to not lose any quality in the measured data with the increased system frequency.

As the SNR of the 4v0 DAS is less than ideal, translating the design to a multilayer board could potentially resolve many of the noise issues hindering this design. Other shielding, such as a proper enclosure for the DAS module, could also help eliminate hazardous environmental noise. Ultimately, by reducing noise issues, the SNR will be improved, resulting in a direct positive impact on the EIT reconstruction results.

The current source design has a nonlinear control pattern, making it difficult to set. One idea is to utilize a design consisting of a resistor network. This would cause the tunability of the current source to be more coarse, but would allow the design to eliminate the current mirror and improve the overall control of the current source. By eliminating the current mirror, the current source could then be used to source, rather than sink, current into the sensing region and establish a true ground reference point to enable modularity.

Though both the firmware and software were designed with modularity in mind, modularity remains unachievable with Revision 4.0. One of the biggest challenges surrounding the modular design is maintaining the same "ground" reference among multiple DAS modules. One potential solution would be to use a power over Ethernet scheme. This scheme also has the potential to eliminate a probable communication bottleneck with USB 2.0 as more DAS modules are connected. Modern Ethernet networks can communicate in the gigabits per second range. Such a communication scheme would also require continued hardware, firmware, and software revisions and support.

Finally, to make the system more deployable and field friendly, moving to an embedded computing platform would also improve overall system cost and ease of use, allowing for an all-in-one embedded solution by eliminating the need for an external host computer.

APPENDIX A

HARDWARE DEPICTIONS OF EIT DAS MODULE REVISIONS

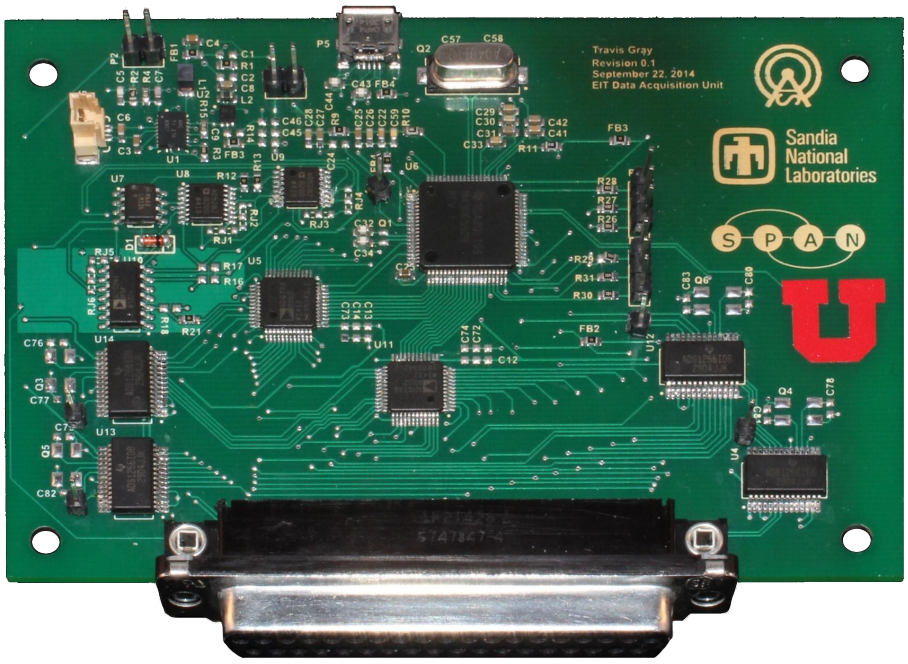

Figure A.1. Hardware depiction of Revision 1.0.

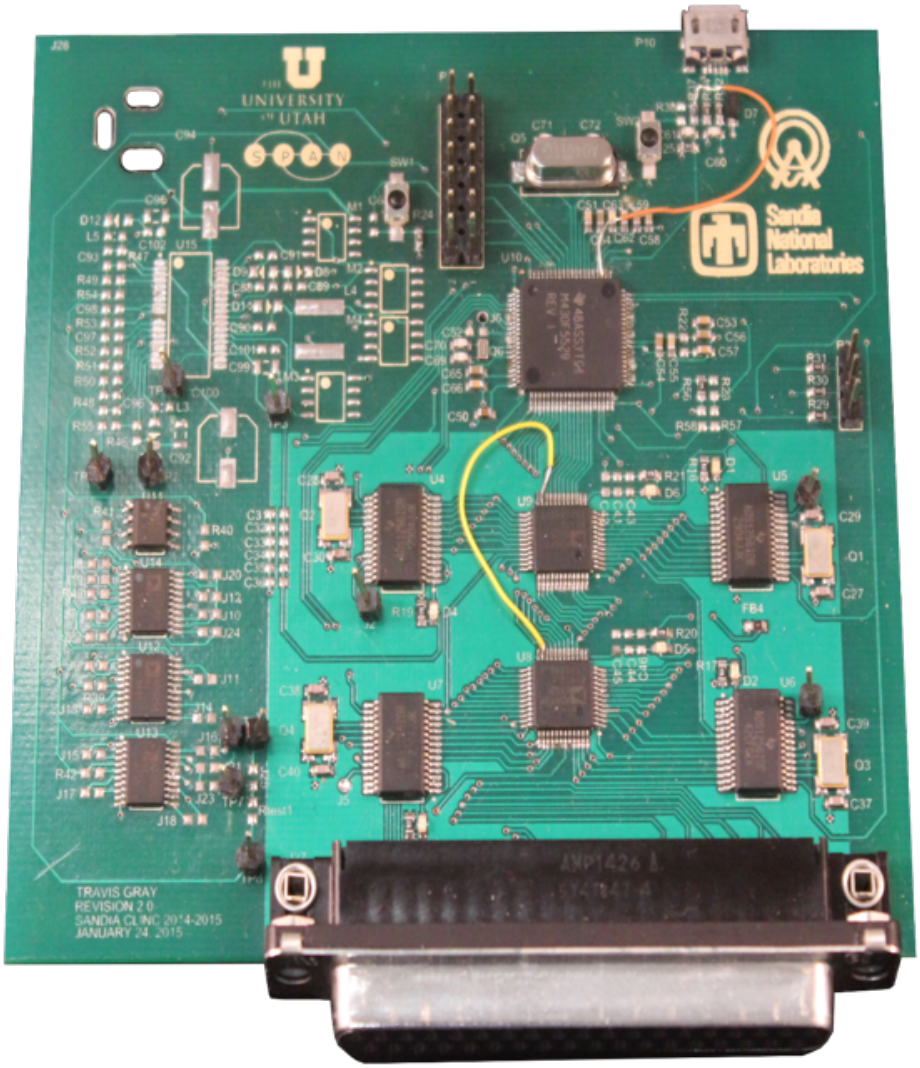

Figure A.2. Hardware depiction of Revision 2.0.

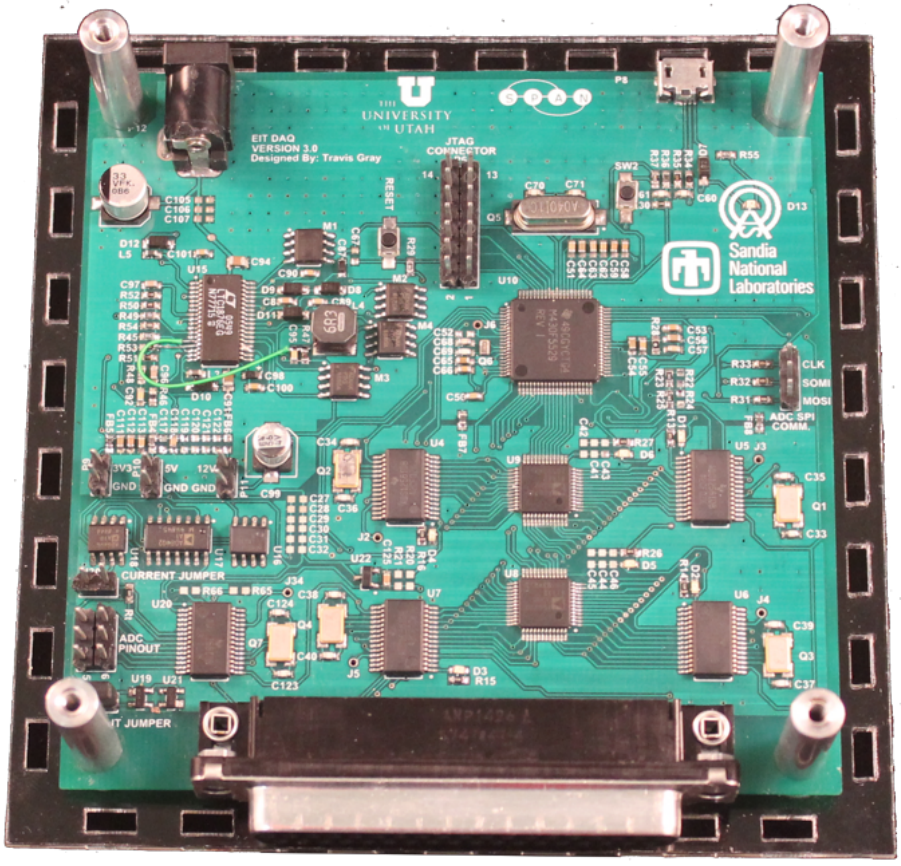

Figure A.3. Hardware depiction of Revision 3.0.

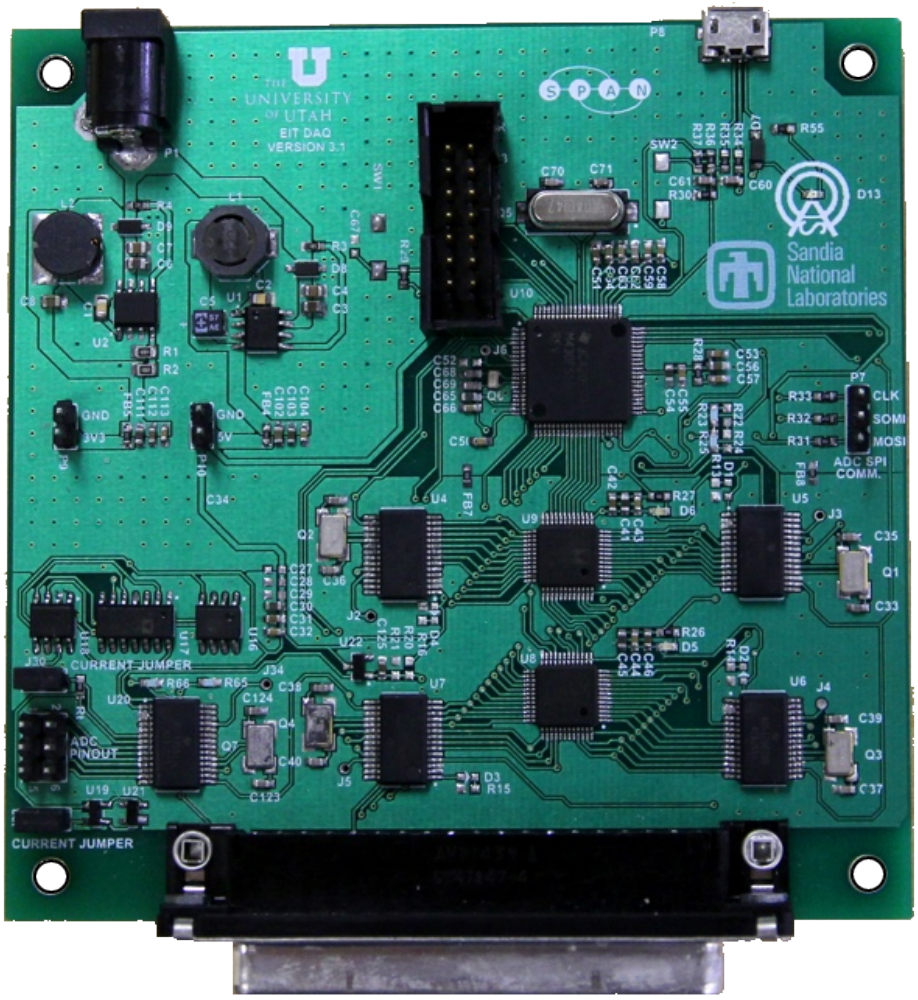

Figure A.4. Hardware depiction of Revision 3.1.

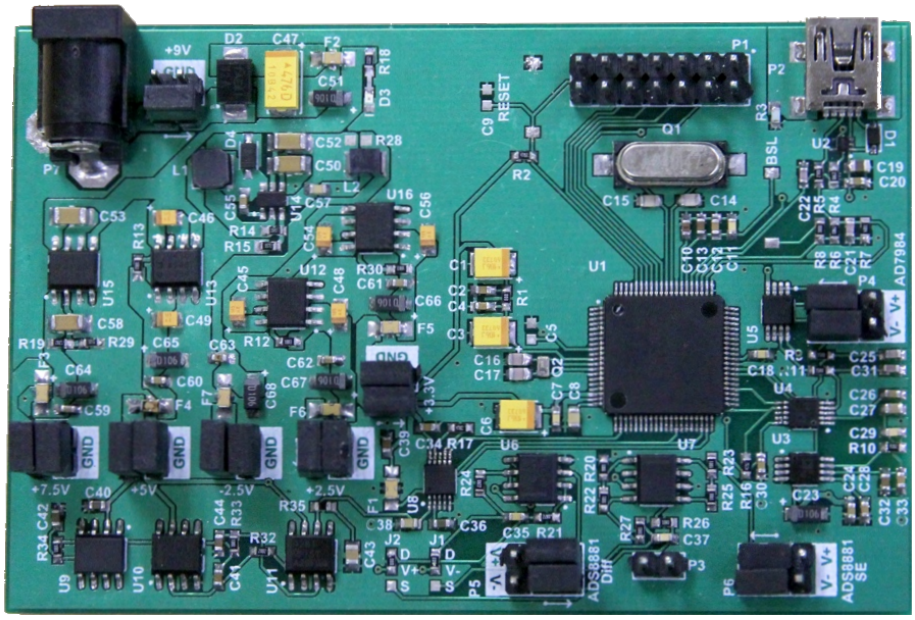

Figure A.5. Hardware depiction of the ADC Development board.

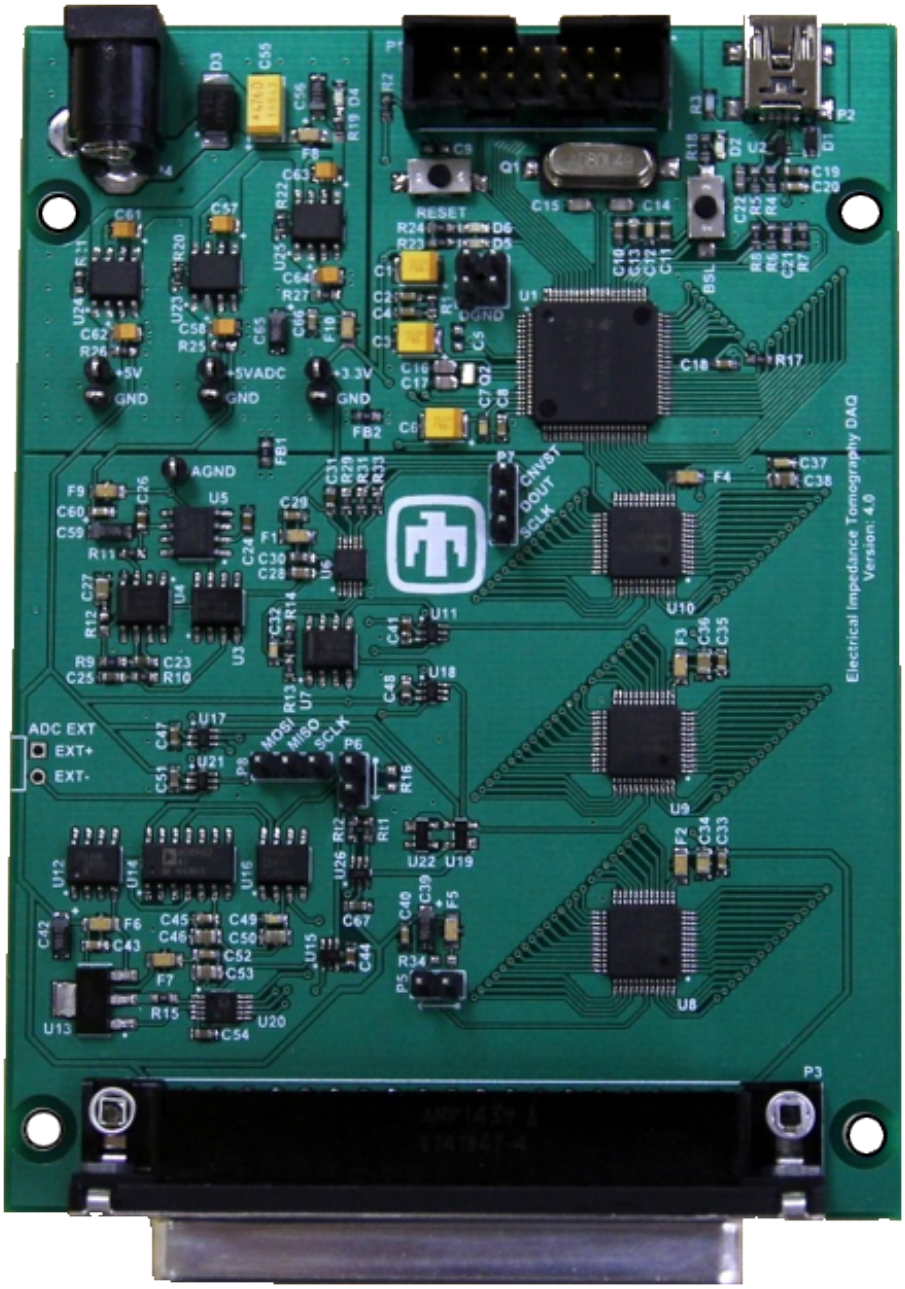

Figure A.6. Hardware depiction of Revision 4.0.

APPENDIX B

COMMUNICATION PROTOCOL INFORMATION

B.1 Packet Protocol: Prefix and Suffix

Table B.1. Instruction Order and Packet Protocol: Prefixes and Suffixes

Instruction	Order	Prefix	Suffix
Get Status	0	0xAE	0xAF
Set ID	1	0xFA	0xEA
Set Number of Repetitions	2	0xAC	0xBC
Set Current Source Value	3	0xCE	0xFF
Select Current Node	4	0xCC	0xDD
Select Ground Node	5	0xCD	0xDF
Start Measurements	6	0xFE	0xEB

Table B.2. Status Packet Protocol: Prefix and Suffix

Packet	Prefix	Suffix
Status	0xAE	0xAF

Table B.3. Data Packet Protocol: Prefix and Suffix

Packet	Prefix	Suffix
Measured Data	0xBE	0xEF

B.2 DAS Module Status Packet

Table B.4. Status Packet: Status Codes

Bit	Status Code
0	Nothing Set
1	Current Value Set
2	Current Node Selected
3	Ground Node Selected
4	ID Set
5	Number of Repetitions Set
6	Start Triggered
7	*NONE*

Table B.5. Status Packet: Error Codes

Byte Value	Error Code
0x00	No Errors
0x01	Invalid Instruction
0x02	Invalid Current Value Suffix
0x03	Invalid Current Node Suffix
0x04	Invalid Ground Node Suffix
0x05	Invalid Get Status Suffix
0x06	Invalid Set Status Suffix
0x07	Invalid Set ID Suffix
0x08	Invalid Set Number of Repetitions Suffix
0x09	Invalid Start Measurement Suffix

APPENDIX C

560 OHM RESISTOR RING COMPARISONS

Table C.1. Injection Pattern Used for Characterization

Injection	Current Node	Ground Node
1	1	24
2	2	23
3	3	22
4	4	21
5	5	20
6	6	19
7	7	18
8	8	17
9	9	32
10	10	31
11	11	30
12	12	29
13	13	28
14	14	27
15	15	26
16	16	25
17	17	8
18	18	7
19	19	6
20	20	5
21	21	4
22	22	3
23	23	2
24	24	1
25	25	16
26	26	15
27	27	14
28	28	13
29	29	12
30	30	11
31	31	10
32	32	9

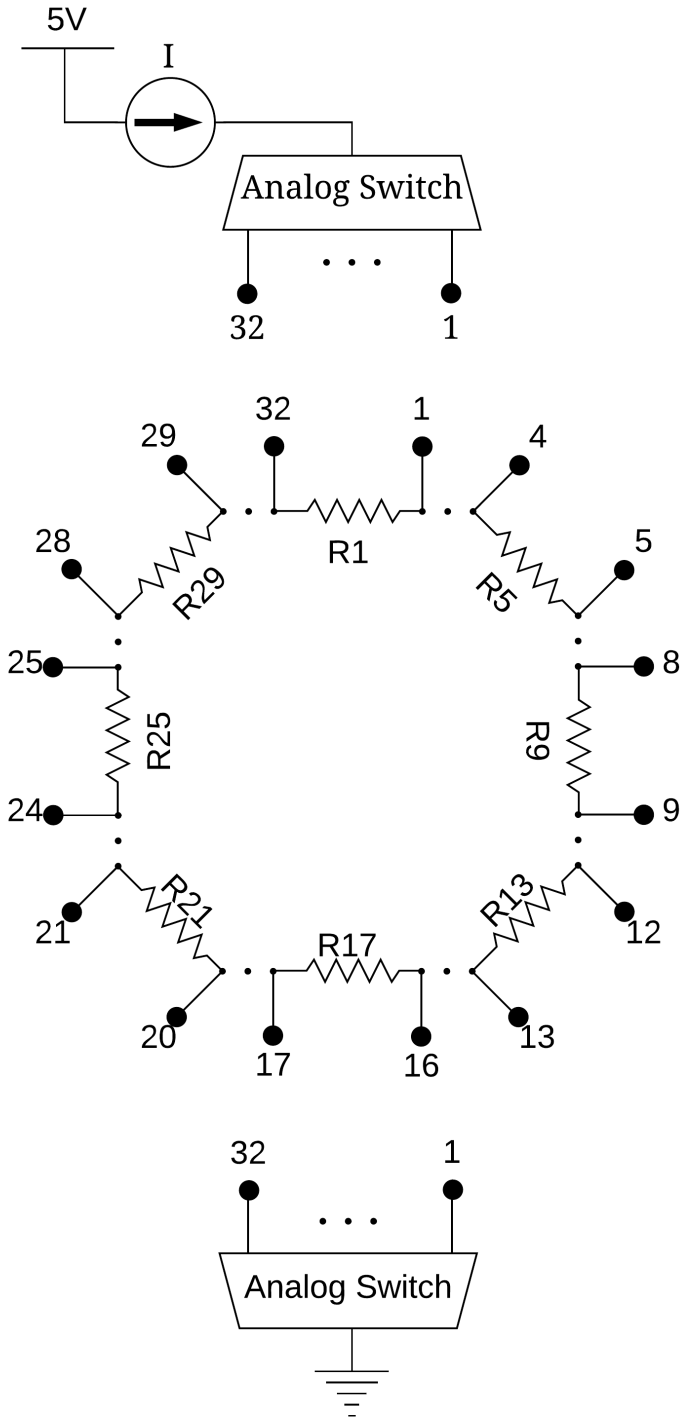

Figure C.1. A resistor ring that separates each of the 32 electrodes by a fixed value is used for calibration.

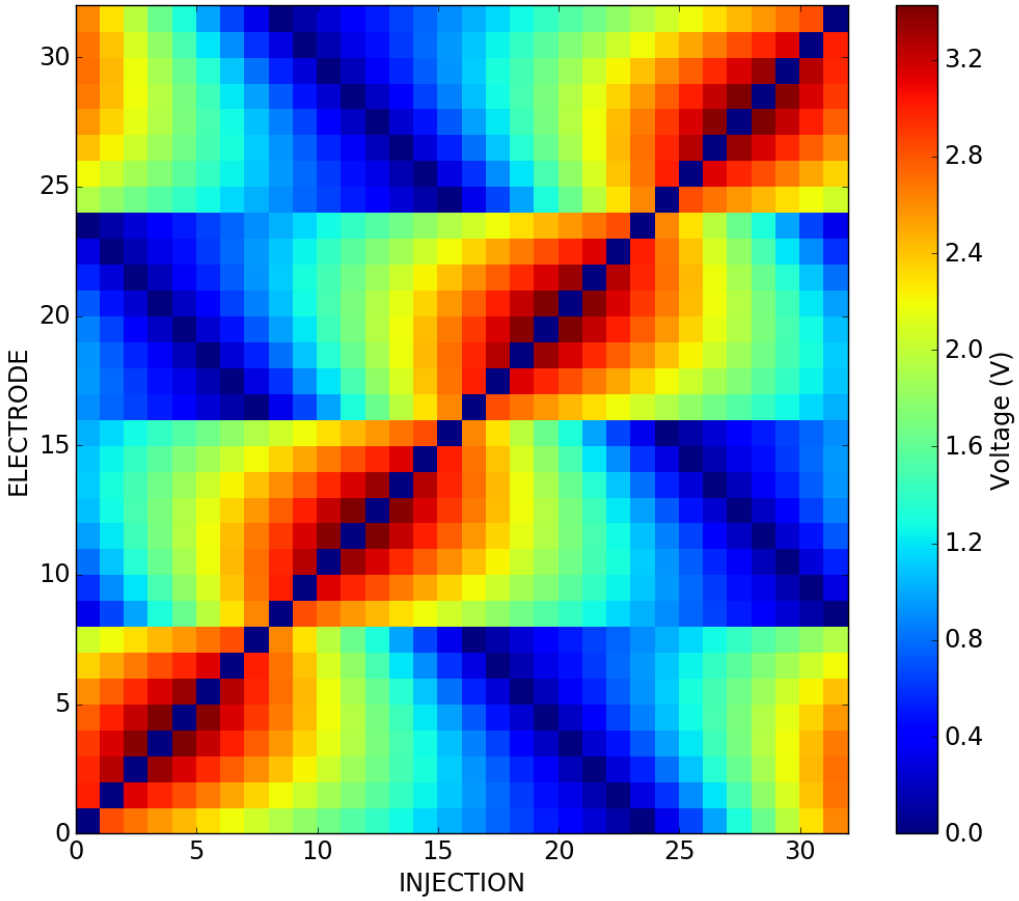

Figure C.2. Calculated true values for a 560 Ohm resistor ring and 1 mA of current.

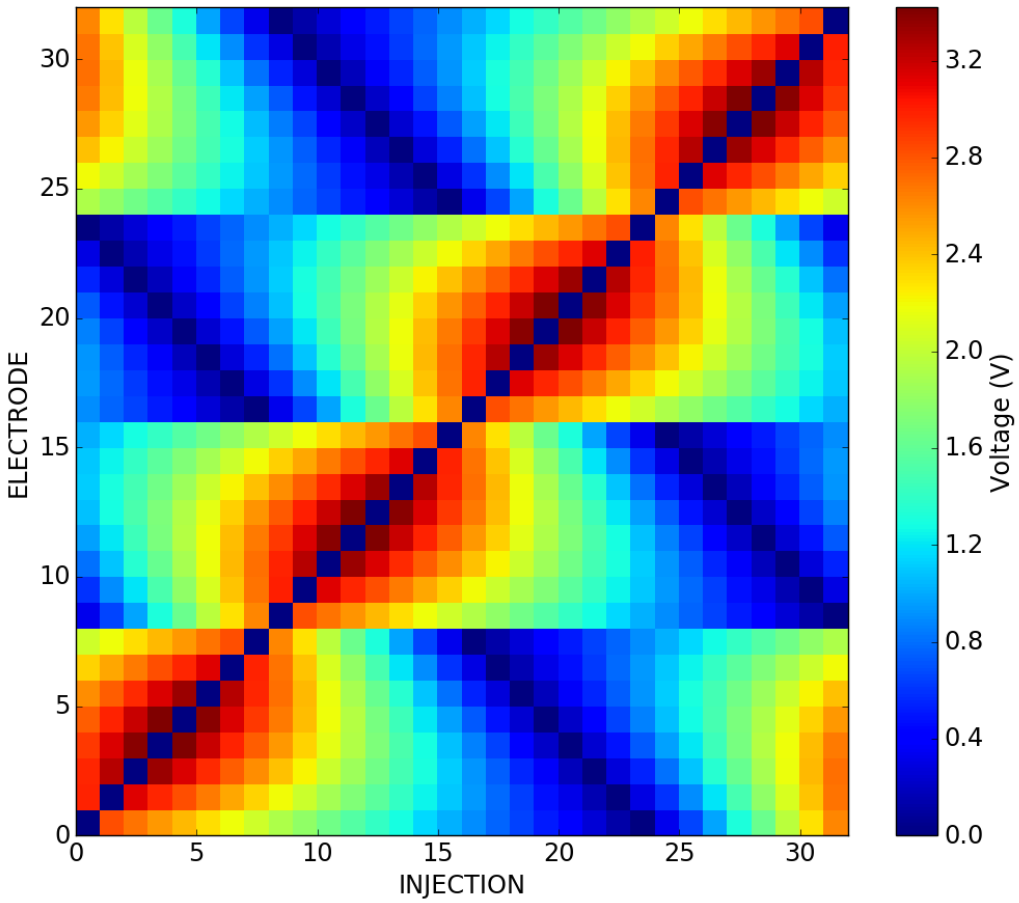

Figure C.3. Measured RMS values of resistor ring using the LGDAS and 1 mA of current.

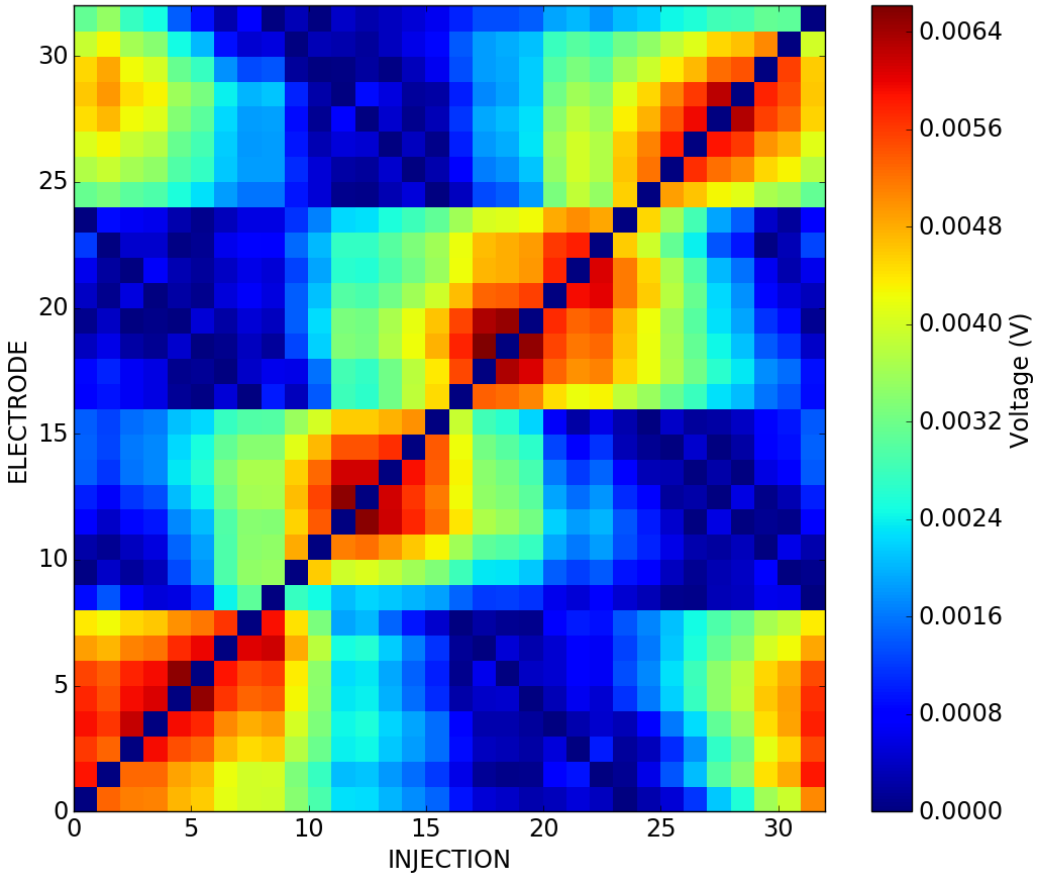

Figure C.4. Bias plot of true value minus measured RMS value for the LGDAS.

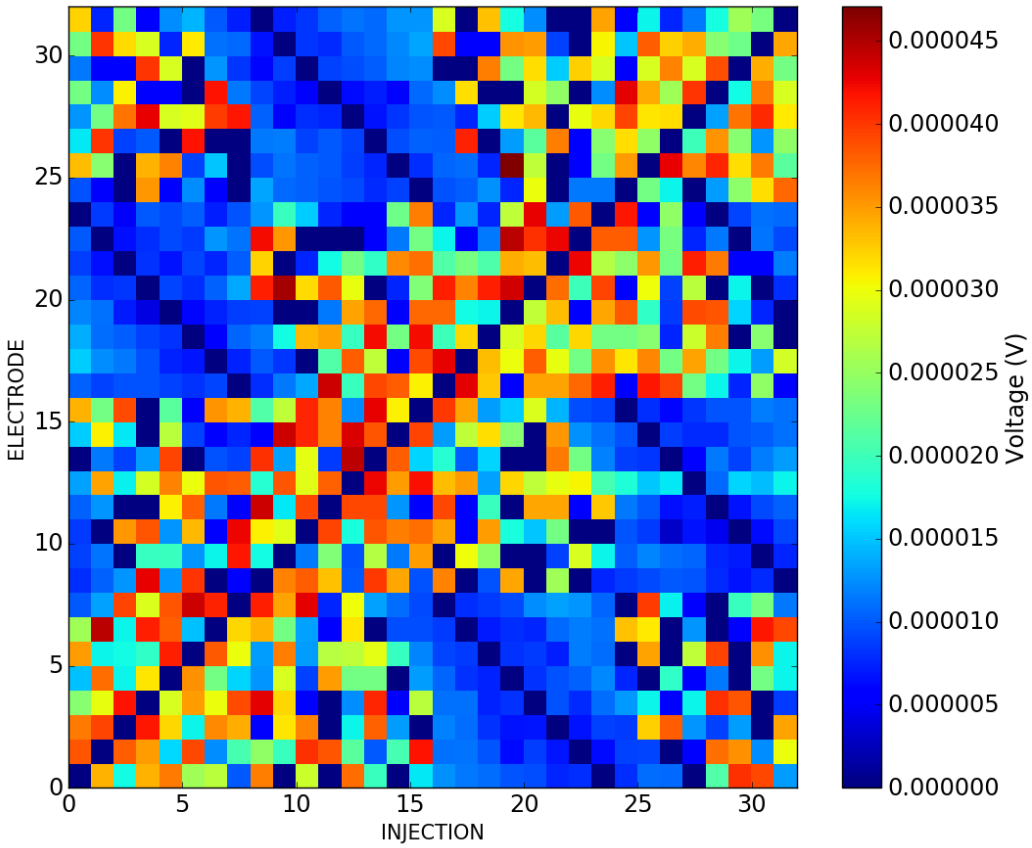

Figure C.5. Standard deviations for each electrode measurement across 10 frames for the LGDAS.

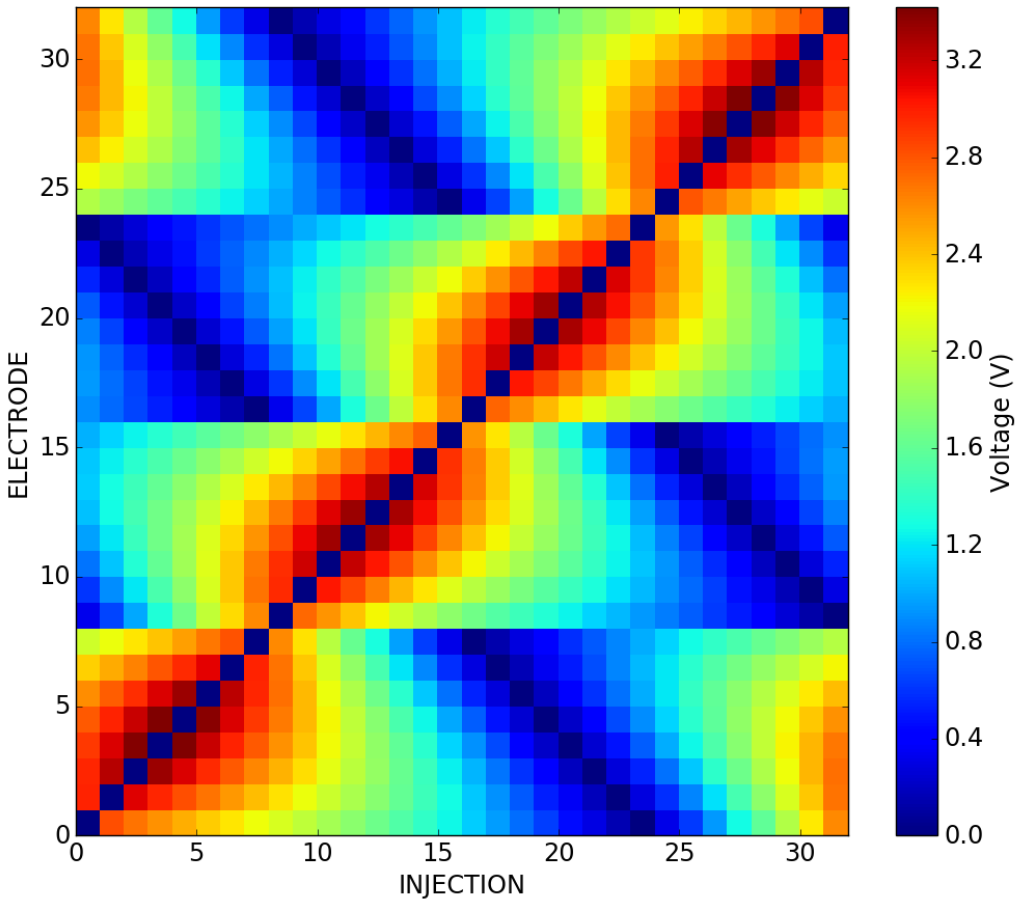

Figure C.6. Measured RMS values of resistor ring using the 4v0 DAS and 1 mA of current.

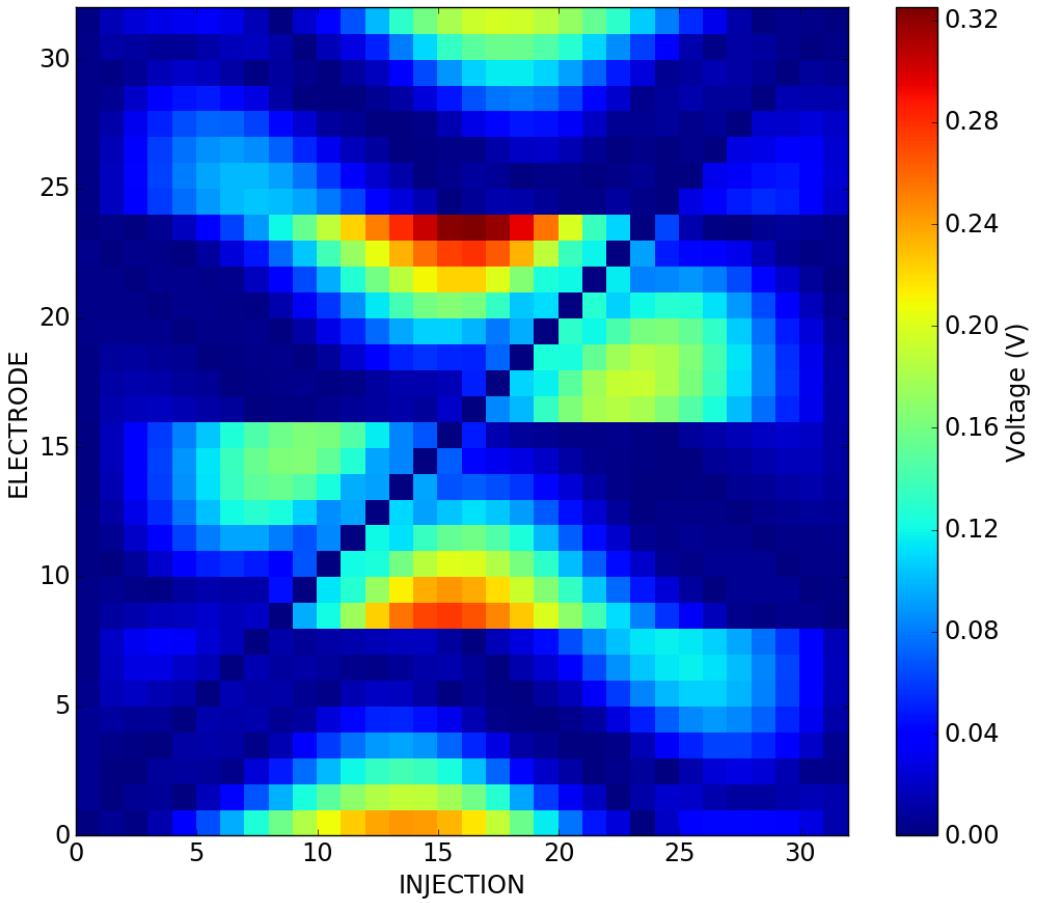

Figure C.7. Bias plot of true value minus measured RMS value for the 4v0 DAS.

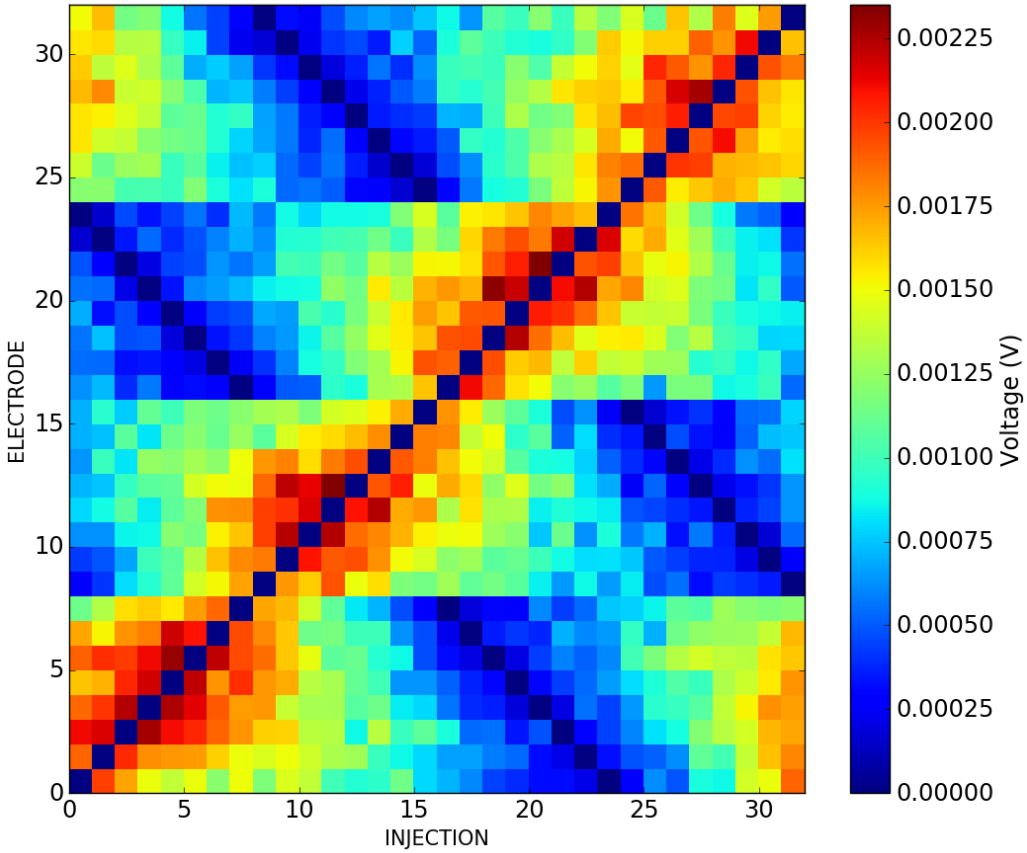

Figure C.8. Standard deviations for each electrode measurement across 10 frames for 4v0 DAS.

APPENDIX D

EIT RECONSTRUCTION: MOVING SQUARE SEQUENCE

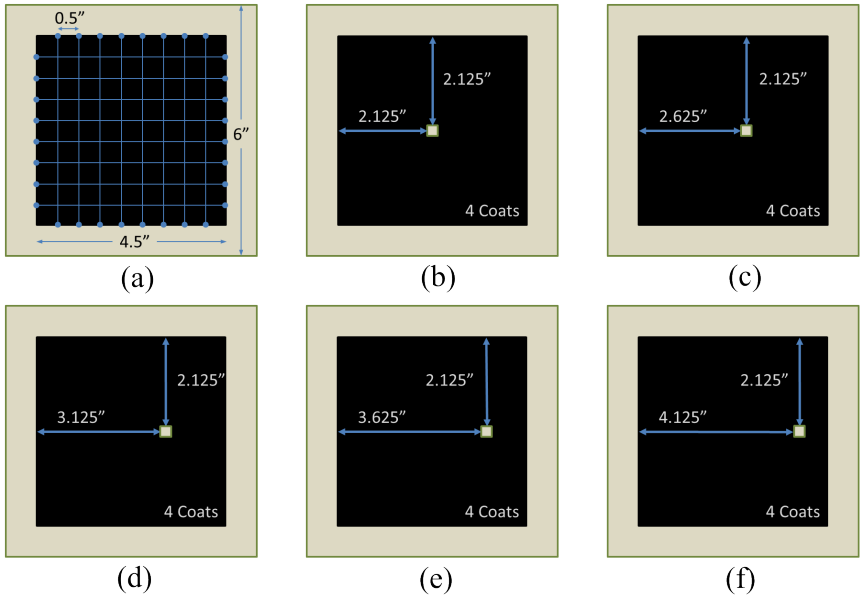

Figure D.1. Representation of the predefined damage patterns for a moving square sequence. (a) "Master" specimen with no emulated damage. The blue dots represent the contact points for each of the 32 electrodes. The blue lines represent the injection pattern projections. (b) "Moving Square 0" (MS0) with a 0.25 in^2 "hole" centered in the specimen. (c) "Moving Square 1" (MS1) with the 0.25 in^2 hole shifted 0.5 in from center. (d) "Moving Square 2" (MS2) with the 0.25 in^2 hole shifted 1.0 in from center. (e) "Moving Square 3" (MS3) with the 0.25 in^2 hole shifted 1.5 in from center. (f) "Moving Square 4" (MS4) with the 0.25 in^2 hole shifted 2.0 in from center.

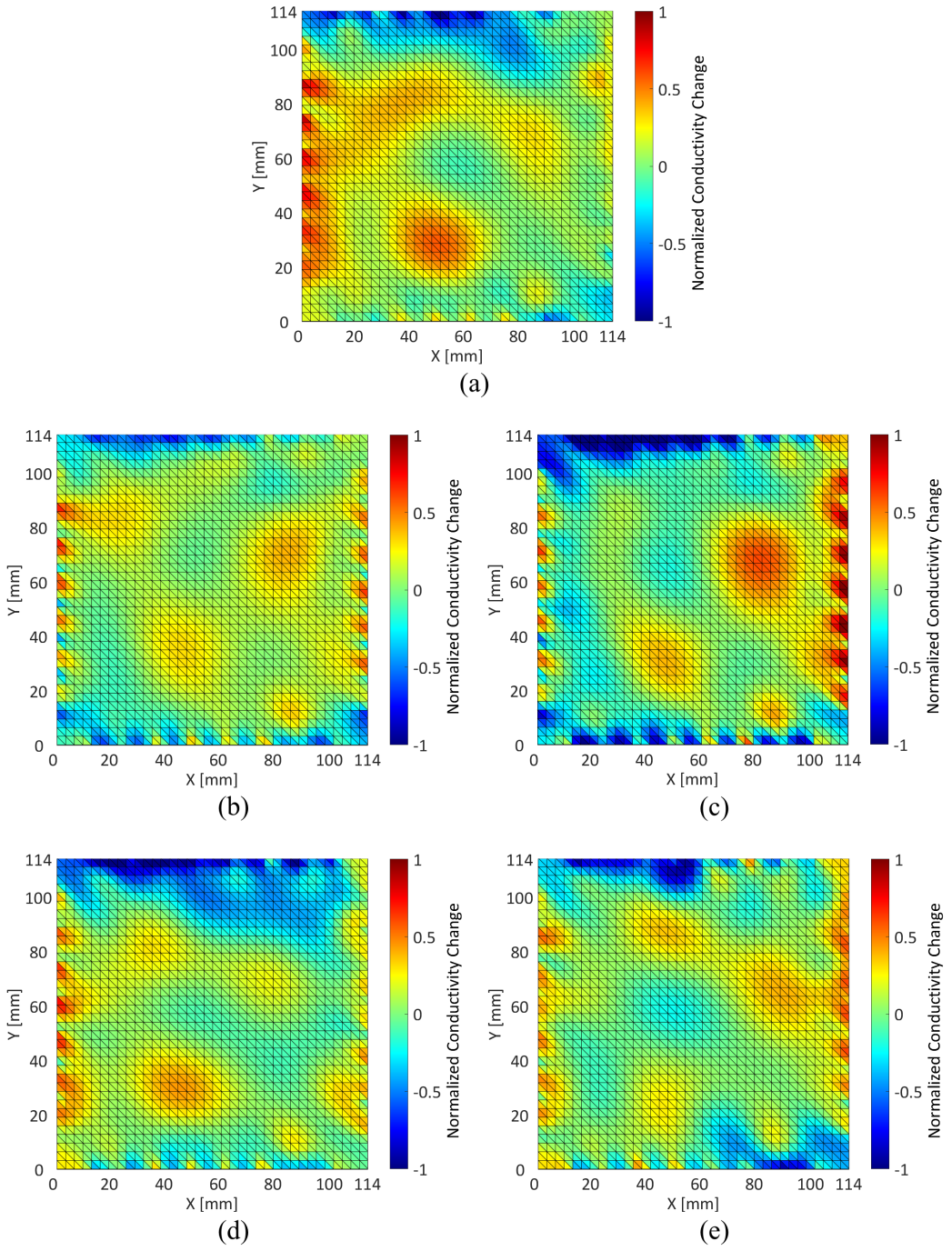

Figure D.2. The LGDAS EIT reconstruction results of the moving square sequence. Figure D.2 (a) relates to the predefined damage pattern shown in Figure D.1 (b), Figure D.2 (b) relates to the predefined damage pattern shown in Figure D.1 (c), and so on. Overall, the results of these measurements expose both the inconsistencies and deficiencies of the test fixture, as seen by the unexpected, drastic changes in conductivity along the electrode border. No conclusions about the damage can be determined, suggesting that the resolution of the system might not be high enough to detect this particular set of damage patterns.

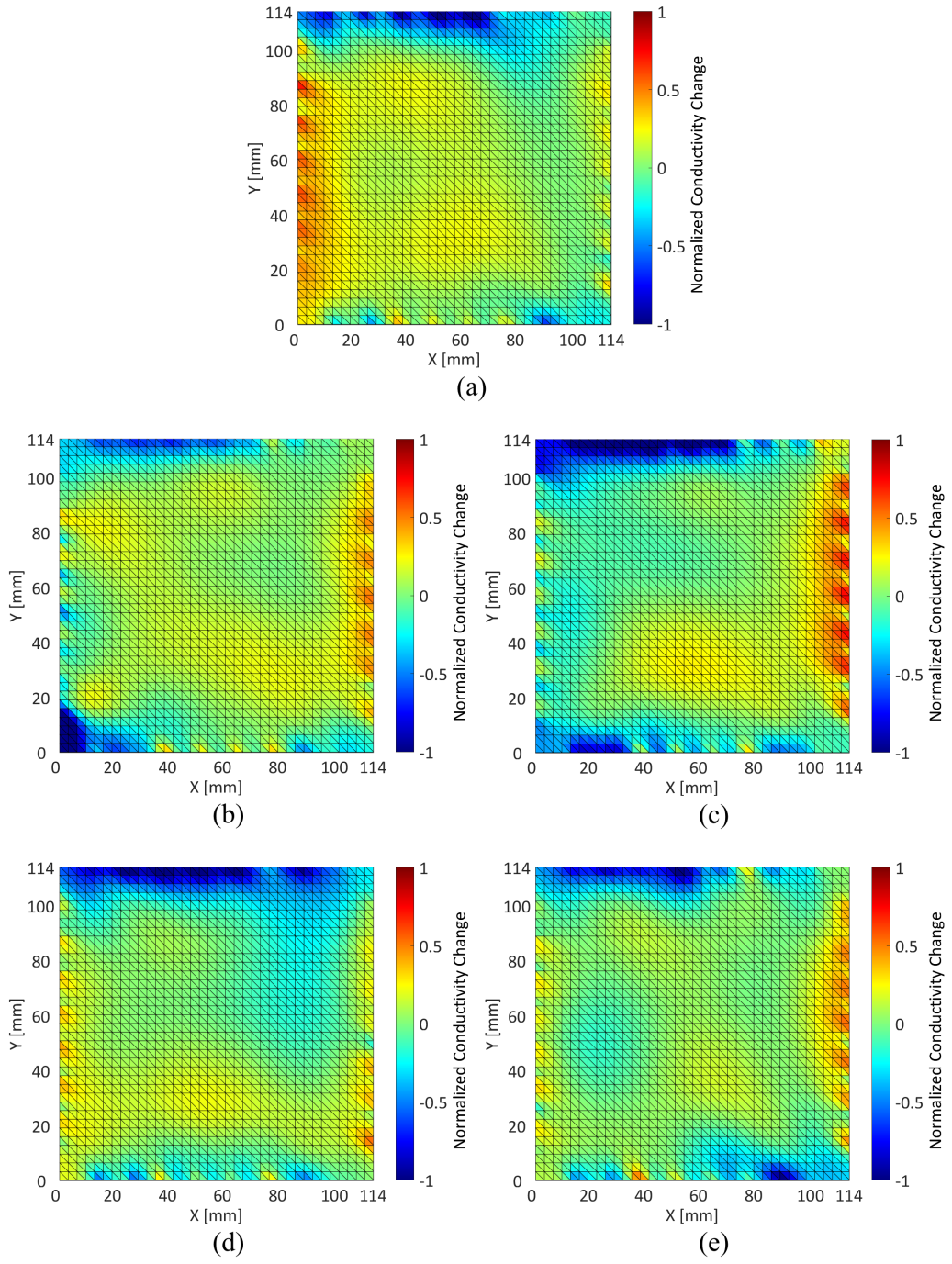

Figure D.3. The 4v0 EIT reconstruction results of the moving square sequence. Figure D.3 (a) relates to both Figure D.2 (a) and to the predefined damage pattern shown in Figure D.1 (b); Figure D.3 (b) relates to both Figure D.2 (b) and to the predefined damage pattern shown in Figure D.1 (c), and so on. Similar to the results shown in Figure D.2, no interesting conclusions about the damage sequence can be drawn from the 4v0 results. However, these results also show that the 4v0 system was no less able to detect the damage sequence than the LGDAS.

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