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NOISE SHAPING IN SAR ADC

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Abstract. *The successive approximation register (SAR) analog-to-digital converter (ADC) is currently the most popular type of ADC architecture, owing to its power efficiency. They are also used in multichannel systems, where power efficiency is of high importance because of the large number of simultaneously working channels. However, the SAR ADC architecture is not the most area efficient. In SAR ADCs, the binary weighted capacitive digital-to-analog converter (DAC) is used, which means that one additional bit of resolution costs double the increase of area. Oversampling and noise shaping are methods that allow an increase in resolution without an increase of area. In this paper we present the new SAR ADC architectures with a noise shaping. A first-order noise transfer function (NTF) with zero located nearly at one can be achieved. We propose two modifications of the architecture: with zero-only NTF and with the NTF with additional pole. The additional pole theoretically increases the efficiency of noise shaping to further 3 dB. The architectures were applied to the design of SAR ADCs in a 65 nm complementary metal-oxide semiconductor (CMOS) with OSR equal to 10. A 6-bit capacitive DAC was used. The proposed architectures provide nearly 4 additional bits in ENOB. The equalent input bandwitdth is equal to 200 kHz with the sampling rate equal to 4 MS/s.*

Key words: *SAR ADC, Noise Shaping, FoM.*

1. INTRODUCTION

SAR ADCs with a capacitive DAC in the feedback loop are currently the most popular type of ADCs. The general benefit of this architecture is its power efficiency. Some of the recently published SAR ADCs can achieve an FoM of several fJ/conv.-step [1].

To provide the required accuracy, a binary weighted capacitive DAC is usually employed. The matching of capacitors has a significant influence on the characteristics of SAR ADCs [2]. To improve the matching, the best option is to use metal-insulator-metal (MIM) capacitors, which have relatively high capacitance and area. Other types of capacitors, such as metal-oxide-metal (MOM), have also been used to design SAR ADCs,

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but additional techniques have to be used to provide the required precision because of poor matching (for example, calibration [3], or dithering [4]), even to achieve 10 bit linearity.

Larger MIM capacitors provide good matching, but the final layout of the ADC requires a large chip area. Furthermore, the larger capacitance leads to higher DAC power consumption, for two reasons: First, because of energy drawn from the reference source to switch the capacitors; second, because of the power dissipated in the larger switches. The first problem can be solved by using an advanced switching scheme, such as previously proposed in [5] and [6]. The second problem has no known solution, except for a decrease of DAC capacitance.

Noise shaping and oversampling are the next alternative solutions, which allow a decrease in the number of capacitors in the DAC for the same ADC resolution. This thematic field is relatively new, with the first important work conducted at the beginning of the 2010s.

2. REVIEW OF STATE-OF-THE-ART NOISE SHAPING SAR ADC ARCHITECTURES

The basic idea of noise shaping can be described as follows. The digital output d(n) of an ADC can be expressed as

$$d(n) = x(n) + q(n),$$

where *x(n)* is the analog input value, and *q(n)* is a quantization error. In conventional ADCs, the *q(n)* value is not used. The basic idea of noise shaping is to append the quantization error of a previous sample to the current sample, for example as

$$d(n) = x(n) + q(n) - q(n-1).$$

In this case, the transfer function of an ADC can be expressed as

$$D(z) = X(z) + (1 - z^{-1})Q(z).$$

It is evident that the quantization error is filtered with the first order high pass filter. The quantization error power is moved to the high frequency part of the spectrum, meaning that the SINAD of the ADC increases in the low frequency part of the spectrum. The noise shaping only makes sense if used with oversampling.

The most obvious way to implement noise shaping is to store the remainder of the last conversion on the DAC, while sampling the current sample. A noise-shaping scheme realizing this approach is described in [7]. The simplified circuit is shown in Fig. 1(a). In this approach, the active amplifier is used to feed the residue of the previous sample back to the DAC. This schematic allows lowering of the DAC area, but it utilizes the active amplifier in the feedback loop, which renders it impractical for low power applications.

Fully passive noise shaping is more promising approach. The most of them use the four input comparator to append the previous sample to the converted input [8]. Similar designs were presented in [9, 10], but in these works the OTA is used for residue filtering. So, these schemes cannot be called fully passive. These ADCs achieve the FoMs of several and several tens of fJ/conv.-step, while providing the effective resolution of 10-12 bits with the effective bandwidth of several MS/s. All these schemes utilize the four input (or fully differential) comparator. The first two differential inputs are connected to the DAC, the second two to the output of the filter, which processes the residue (see Fig. 1(b)).

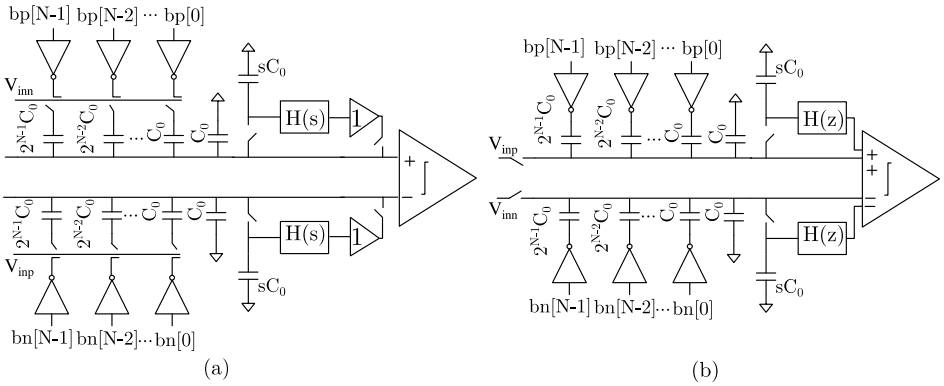

Fig. 1 Typical noise shaping SAR architectures: (a) – with active filtering of quantization error; (b) – fully passive

In 2019, we also proposed two fully passive noise shaping schemes [11, 12], which are based on the completely different principle. In our schematic we do not use the four input comparator. These schemes will be described in detail in next sections of this paper. The DAC capacitors and the residue filter capacitor are connected to each other through the attenuation capacitor (see Fig. 2). After the charge redistribution the new voltage at a DAC equals to the attenuated sample plus the filtered residue of previous sample. So, the usual two-input comparator can be used. Furthermore, our schematic allows to implement the most efficient noise shaping, as its noise transfer function (NTF) zero lies very near to one, to be exactly 0.943. By the competitors the zero location is between 0.5 and 0.75 (see Fig. 3). So, it did not make sense to sample with OSRs higher than 8, as no gain in ENOB could be achieved. Both our noise shaping schemes allow the use of higher OSRs – up to 15. This schematic allows designing the competitive SAR ADCs.

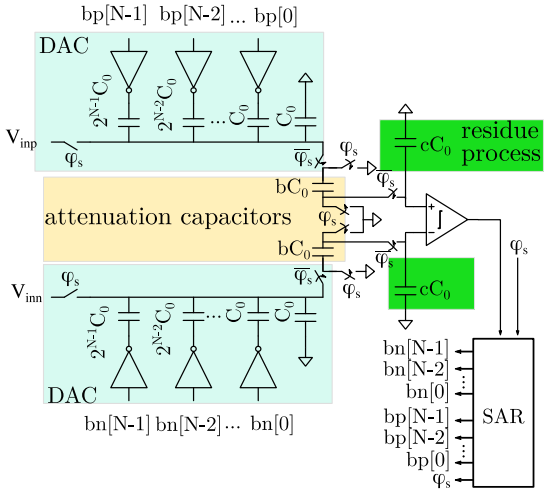

Fig. 2 Proposed fully passive noise-shaping SAR ADC architecture

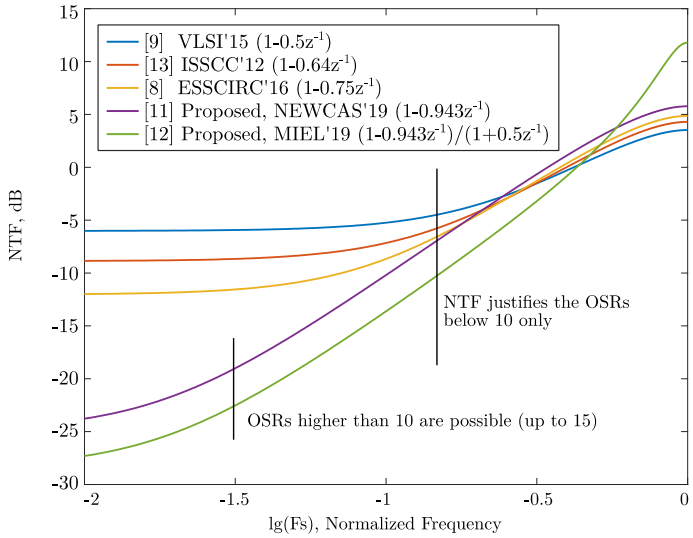

Fig. 3 Comparison of state-of-the-art fully passive noise-shaping SAR ADCs. The both proposed schemes allow the use of OSR higher than 10

3. Proposed Noise Shaping SAR Architecture

The proposed noise shaping architecture is shown in Fig. 2. Dependent on the connection of the attenuation capacitor after the conversion phase this architecture can be split into two sub-architectures: one implements the zero-only NTF, the other has the NTF with additional pole. The pole has the influence on the systems stability, but also increases the attenuation of the noise in the frequency band of interest.

The circuit utilizes additional capacitors equal to bC_0 and cC_0, where b and c are integers, and 8 switches, which can be implemented as single N-channel MOS (NMOS) transistors. Additionally, the most-significant-bit (MSB) capacitor should be equal to 2^{N-1}, where N is the DAC's resolution. So, the DAC is twice as big in comparison to the standard monotonic switching SAR architecture [14]. The additional capacitor cC_0 is needed to obtain the value of quantization error $e(n)$ at the end of conversion, as in the noise-shaping architecture presented in [15].

3.1. Architecture without the pole in NTF

First, we consider the architecture without the pole in NTF. In this case, the digital control logic does not differ much from the standard SAR logic. The additional switches are operated with the sampling signal φ_s and inverted sampling $\overline{\varphi_s}$. During sampling the capacitors bC_0 are discharged to ground, the comparator and cC_0 are disconnected from the capacitive DAC. The cC_0 capacitor holds the remainder voltage of previous conversion. During conversion phase the DAC is connected to the comparator and cC_0 through the discharged attenuation capacitor bC_0.

The working principle is shown in Fig. 4. Only one side of the DAC is shown for simplicity. The following equations can be written for the charge redistribution after the end of sampling phase (B in Fig. 4):

$$\begin{cases} \Delta q = 2^N C_0 (x(n) - k(n)) \\ \Delta q = bC_0 (k(n) - \mathrm{g}(n)) \\ \Delta q = cC_0 \left(\mathrm{g}(n) - \frac{\mathrm{e}(n-1)}{1/C_0 \left(1/2^N + 1/b + 1/c \right)} \right) \end{cases} \quad (1)$$

Where x(n) is the sampled analog input, $e(n–1)$ is the quantization error of previously converted digital output $d(n)$, $g(n)$ is an actually converted analog value, which appears on the comparator input after the initial charge redistribution after the sampling phase and before the start of conversion, $k(n)$ is the voltage on the capacitive DAC obtained at the same moment. From this set of equations the voltage $g(n)$ can be found as:

$$\mathrm{g}(n) = \frac{1/c\, x(n) + \left(1/2^N + 1/b \right) e(n-1)}{c \left(1/2^N + 1/b + 1/c \right)} \quad (2)$$

After initial charge redistribution the conventional monotonic SAR algorithm can start. At the end of conversion, the voltage at comparator will equal to:

$$\mathrm{g}(\mathrm{n}) - \frac{\mathrm{d}(\mathrm{n})}{\mathrm{c}\left(1/2^N + 1/b + 1/c \right)}, \quad (3)$$

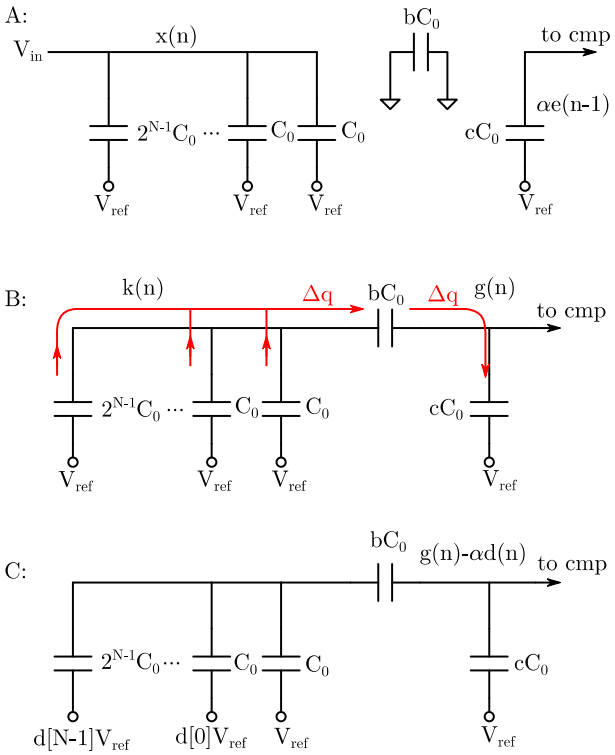

Fig. 4 Working principle of the proposed noise shaping architecture. A: Sampling phase; B: Charge redistribution after sampling phase; C: SAR matrix and voltages at the end of conversion cycle. $\alpha = 1 / (1/2^N + 1/b + 1/c)$

where $d(n)$ is the digital output code of the SAR. This voltage, obviously, equals to the quantization error $e(n)$ divided by the coefficient equal to c ($1/2^N + 1/b + 1/c$). Taking this into account, the following equation can be written for the digital output $D(z)$ in the complex frequency domain:

$$D(z) = X(z) - \left(1 - \frac{1/2^N + 1/b}{1/2^N + 1/b + 1/c} z^{-1}\right) E(z) \quad (4)$$

The following observations can be made. First, with the increase of c, the coefficient at z^{-1} approaches "1". Secondly, from the equation (2) with the increase of c, the voltage at the comparator input at the beginning of conversion cycle becomes independent on the $x(n)$, and so, the circuit becomes nonfunctional.

In the practice it means, that to provide better NTF we have to increase the resolution of the comparator. For example, in this work, the following configuration was applied: $c = 2^{N-1}$, $b = 1$. That configuration provides the NTF equal to $(1–0.9429z^{-1})$, while the $x(n)$ is divided by 17.5. So, in the proposed design, the comparator resolution should be equivalent to 10.13 bit. However, the design of comparator can be relaxed in comparison to the comparator in the classical 10-bit monotonic scheme, as the common mode variation in the proposed scheme is also no more than V_{ref} / 17.5.

3.2. Architecture with the pole in NTF

The additional pole in the NTF provides additional attenuation of the noise in the band of interest. But, for the realization of this architecture additional control signals are needed. Furthermore, the charge on the attenuation capacitor should be divided by two to provide the circuits stability. The modified schematic is shown in Fig. 5.

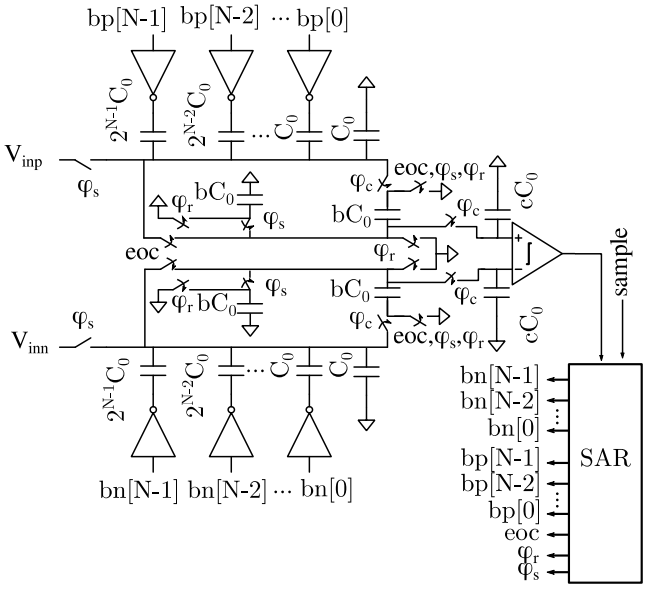

Fig. 5 Architecture modification to implement additional pole in NTF

The simplified functional diagram of the proposed SAR ADC architecture is shown in Fig. 6. Initially, the input signal $x(n)$ is sampled on the top plates of the capacitive DAC. At the same time, the residue voltage of previous sample (voltage on the capacitive DAC after the end of conversion) saved on the capacitor bC_0 is divided by two. Without this step the pole will be equal to one and the circuit will become unstable. The capacitor cC_0, with the previous quantization error divided by $\alpha = (1/2^N + 1/b + 1/c)$, is disconnected from the DAC. After the end of sampling phase, the DAC is connected to the quantization error storage capacitor cC_0 through the capacitor bC_0 like in previous circuit. The charge redistribution occurs, which can be described as:

$$\begin{cases} \Delta q = 2^N C_0 (x(n) - k(n)) \\ \Delta q = bC_0 (k(n) - g(n) + 0.5 V_{res}(n-1)) \\ \Delta q = cC_0 \left(g(n) - \frac{e(n-1)}{1/C_0 \alpha} \right) \end{cases}, \tag{5}$$

where $k(n)$ and $g(n)$ are the voltages on the DAC and quantization error storage capacitor cC_0, respectively, after charge redistribution, $e(n–1)$ is the quantization error of previous sample. After the charge redistribution the conversion begins. As the capacitor cC_0 is connected directly to comparator, after the end of conversion, its voltage will be equal to $e(n) / \alpha$. The voltage at the DAC will be equal to:

$$V_{res} = g(n) - d(n), \tag{6}$$

Where $d(n)$ represents the digital DAC input (ADCs output).

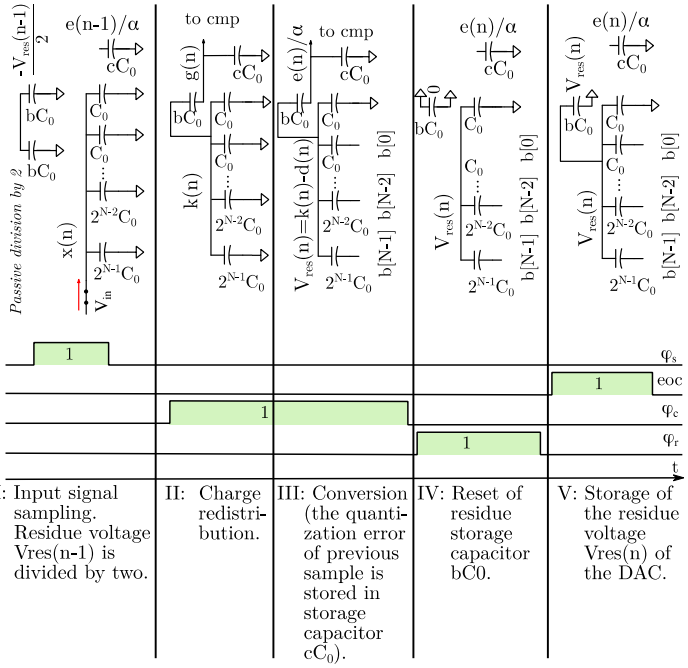

Fig. 6 Functional diagram of the proposed ADC architecture

After the end of conversion the new value of $V_{res}(n)$ can be saved on capacitor bC_0 (if $bC_0 << 2^N C_0$).

From (5)-(6) the following equation can be written for the determination of output digital code $D(z)$:

$$D(z)\left(1+\left(0.5+{}^{1}/_{2^N\alpha}\right)z^{-1}\right)=X(z)(1+0.5z^{-1})+ \\ +E(z)\left(1-\frac{{}^{1}/_{2^N C_0}+{}^{1}/_{bC_0}}{\alpha}z^{-1}-\frac{{}^{0.5}/_{2^N C_0}}{\alpha}z^{-2}\right) \quad (7)$$

If ${}^{1}/_{2^N} << 1$, this equation can be simplified to:

$$D(z)=X(z)+\frac{1-\frac{{}^{1}/_{2^N C_0}+{}^{1}/_{bC_0}}{\alpha}}{1+0.5z^{-1}}E(z) \quad (8)$$

If c, $N>>1$, the equation (8) can be rewritten as:

$$D(z)\approx X(z)+\frac{1-z^{-1}}{1+0.5z^{-1}}E(z) \quad (9)$$

So, the circuit will perform the first order noise shaping. The pole gives additional 3 dB noise shaping in the input frequency band.

To implement this architecture the modification of the SAR logic is needed, which is shown in Fig. 7. It can be seen that only 6 additional combinational logic blocks and one delay are used to generate the signals for noise shaping. Our innovative delay design [16] is used to provide low power consumption.

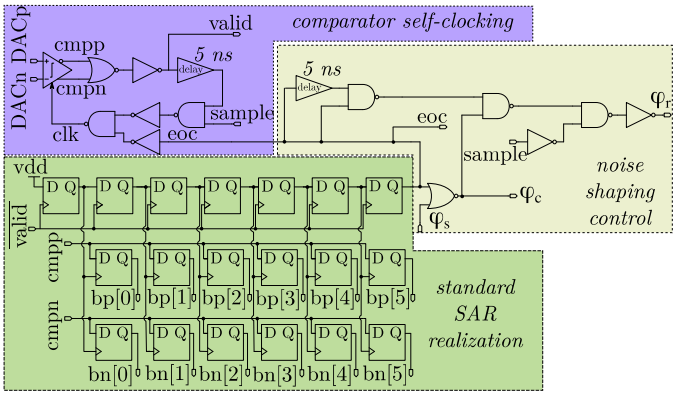

Fig. 7 Control logic modification for the realization the proposed noise-shaping SAR ADC architecture (with additional pole)

4. Simulation Results and Comparison of Proposed Noise Shaping SAR Architectures

For both architectures we used 65 nm technology of UMC. A binary weighted capacitive DAC is built with minimum metal-insulator-metal (MIM) capacitors (5µm x 5µm, 51 fF). Two capacitors are connected in series to implement C_0, so the C_0 value is equal to 25.5 fF. A $16C_0$ ($c=16$) MIM capacitor is used to store the quantization

error. The attenuation capacitor is set to $2C_0$ ($b=2$). So, the input voltage $x(n)$ is devided by 17.5 at the input of the comparator. So, in this configuration the comparator resolution should be equivalent to 10.13 bit. The common mode voltage on the input of the comparator sequentially decreases from $V_{ref}/2/17.5$ to zero, so one p-type input differential pair can be used in comparator circuit. A common dynamic one stage topology shown in Fig. 8 was used.

All switches are realized as single n-MOS transistors with minimum length and width except for the input sampling switch, where a bootstrapped switch is used to suppress harmonics, what is quite common in SAR ADCs with upper plate sampling.

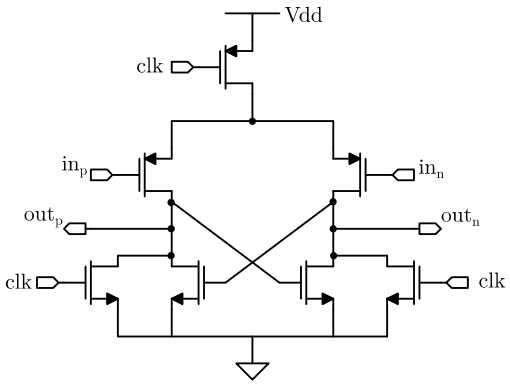

Fig. 8 Simple one stage comparator used in this design

The second architecture does not affect the area of the significantly. The area estimation of both architectures (automatic place and route) equals to *0.05 mm*^{2}.

The circuits were simulated with Cadence Spectre. The sampling speed was set to 4 MS/s. The simulated output spectrums of the proposed ADCs with 191.47 kHz @0.9151 dB sinusoidal input are shown in Fig. 9.

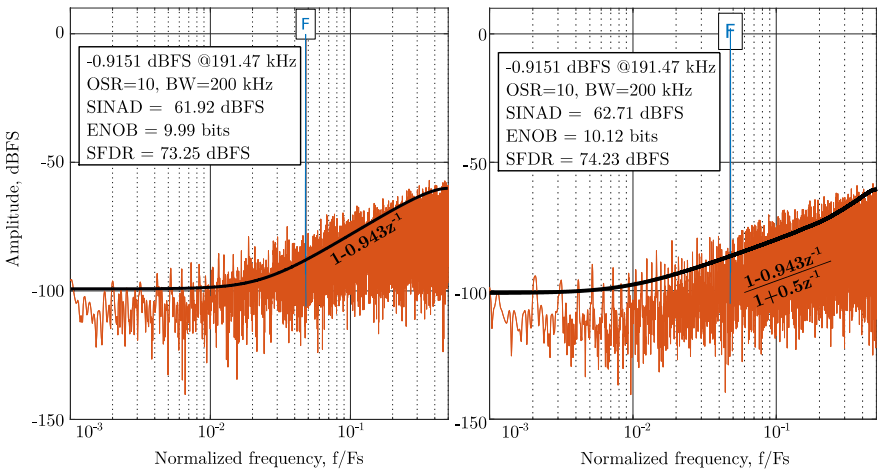

Fig. 9 Simulated output spectrum of the proposed architectures

A comparison with other architectures and both proposed architectures is given in Table 1.

Table 1 State of the art Noise Shaping SAR ADCs

	[8]	[10]	[9]	Zero-only	Zero+pole
Architecture					
NTF zero location	0.75	0.5	0.65	→1	
Need of OTA	No	Yes	Yes	No	
Need of comparator modification	Yes	Yes	Yes	Yes	
Input attenuation	No	Yes	No	Yes	
Number of unit capacitors	2^N	2^{N+1}	2^N	$3(2^{N-1})$	
Circuit Performance					
Technology, nm	130	65	65	65	
Bandwith, MHz	0.125	6.25	11	0.2	
DAC size, bit	10	8	8	**6**	
ENOB, bit	12	10	9.35	10.0	10.12
Additional bits in ENOB, bit	2	2	1.35	**4.0**	**4.12**
OSR	8	4	4	10	
FoM, fJ/conv.-step	59.6	14.8	35.8	19.4	18.0
FoMs, dB	167	165.2	163.3	**167.2**	**167.9**
Verification	Meas.	Meas.	Meas.	Simulation	
Year				2019	

It can be noted that the architecture variant with pole gives only slight improvement in the SINAD - 0.8 dB, which corresponds only to 0.12 bits in ENOB. The power consumption of the second architecture is slightly higher (because of additional logic and switches): for the zero only architecture the average power consumption equals to 7.94 µW, while for the architecture with additional pole it is 8.0 µW. For both implementations DAC consumes nearly 50% of power, comparators power consumption is nearly 40%, while the rest is consumed by digital logic.

The theoretical 3 dB improvement of SINAD in the frequency band of interest was not achieved. The nonideality of the division by two with the real switch and capacitor can be the cause of it.

So, by now we recommend to use the more simple variant without the pole.

Both proposed schemes do not need any modification of comparator circuit, the additional capacitor needed for storage of the quantanization error is compensated by the use of monotonic switching. So, the total area of the proposed architectures is near the same as in other noise shaping schemes.

The main advantage of the proposed architectures is the possibility to use higher OSRs. It gives the possibility to achieve higher number of effective bits with less area. The previously reported noise-shaping SAR ADCs typically achieve only 2 additional bits, while proposed SAR ADC achieves the 10-bit resolution with the 6-bit capacitive DAC.

4. CONCLUSION

Two new, fully passive noise shaping architectures for a SAR ADC were proposed. In both architectures the theoretically achievable NTF zero location tends to one. In the proposed implementation of the architectures the real zero location is 0.943, while in the alternative solutions the maximum NTF zero was 0.75. The architectures introduce only a slight modification of the standard SAR ADC scheme. A four-input comparator is not needed. The digital logic remains unmodified for the first architecture (zero only) and slightly modified for the second architecture (6 additional logic gates).

The second architecture theoretically can give additional 3 dB attenuation of quantanization noise in the frequency band of interest. However, in practical implementation the additional attenuation was equal to 0.8 dB, which makes the first architecture more suitable, because of its simplicity.

Both architectures were used to implement the SAR ADC in 65 nm CMOS technology of UMC. The 6-bit capacitve DAC and OSR ration equal to 10 were used. The input frequency bandwidth was set to 200 kHz. Both architectures provide 4 additional bits in ENOB. According to simulation results both ADCs have Walden FoM of less than 20 fJ/conv.-step and Schreier FoM of more than 167 dB.

Further research can concentrate first, on the more accurate investigation of the lower attenuation of quantization noise in the second architecture with additional pole in NTF, and second, on the implementation of second order NTFs by, for example, a combination of the proposed architecture with the architecture with 4-input comparator.

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