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An Output Ripple-Free Fast Charger for Electric Vehicles Based on Grid-Tied Modular Three-Phase Interleaved Converters

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***Abstract*— An off-board dc fast battery charger for electric vehicles (EVs) with an original control strategy aimed to provide ripple-free output current in the typical EV batteries voltage range is presented in this paper. The proposed configuration is based on modular three-phase interleaved converters and supplied by the low-voltage ac grid. The ac/dc interleaved three-phase active rectifier is composed of three standard two-level three-phase converter modules with a possibility to slightly adjust the dc-link voltage level in order to null the output current ripple. A modular interleaved dc/dc converter, formed by the same three-phase converter modules connected in parallel, is used as an interface between the dc-link and the battery. The use of low-cost, standard and industry-recognized three-phase power modules for high-power fast EV charging stations enables the reduction of capital and maintenance costs of the charging facilities. The effect of coupling on the individual input/output inductors and total input/output current ripples has been investigated as well, considering both possible coupling implementations, i.e. inverse and direct coupling. Numerical simulations are reported to confirm the feasibility and the effectiveness of the whole EV fast charging configuration, including the proposed control strategy aimed to null the ripple of the output current. Experimental results are provided by a reduced scale prototype of the output stage to verify the ripple-free output current operation capability.**

***Keywords*—Electric vehicle, fast charging, modular interleaved converter, ripple-free output current.**

I. Introduction

Electric vehicles (EVs) have become more popular in recent years due to concerns about the environment and the fossil fuel shortage. Progressive public policies are fostering electrification and decarburization of transports. New standards are already in the process of being implemented by governments worldwide. The shift from internal combustion engine (ICE) vehicles towards EVs is unlikely to take long. However, in order to achieve this changeover, one of the main challenges that have to be faced is the development of suitable chargers, capable of realizing fast battery charging that complies with grid standards.

Battery chargers can be categorized into three basic types, wireless, on-board (both typically slow chargers) and off-board (typically fast/ultrafast chargers). Fig. 1 shows a principal scheme of an on/off board and wireless EVs charging system with different power levels (1, 2 and 3). The topologies and the power ratings of the converters in each type of the chargers differ significantly. Many configurations have been proposed, compared and evaluated based on the power levels, charging time, and other factors [1]-[4]. Wireless chargers have been also studied and evaluated in terms of costs, consumer acceptance and limitations in power electronic technologies [5]. The one-element resonant topologies have been analyzed and compared in [6]. In [7], dynamic wireless charging systems have been proposed being able to charge the EV wirelessly while it is driving.

Nowadays, on-board battery charging is widely employed, allowing the use of low-power domestic utilities to recharge an EV. However, this strategy restricts casual daily usage of the electric cars, due to the long charging cycle. For a wider use of EVs, fast battery chargers are necessary.

Although the term “fast charging” is not strictly defined, the concept of fast battery charging implies that in an approximately ten-minutes long charging cycle, an EV’s battery gains enough energy to increase the car’s cruising range of about hundred kilometers (i.e., almost 15 kWh). Nevertheless, this charging type, which requires massive power densities in a low battery’s voltage range (400–800 V), makes power electronics, involved in the charging system, unique or even impractical for on-board implementation. Fast charging mainly refers to off-board dc charging stations with rated power equal to or higher than 50 kW [8].

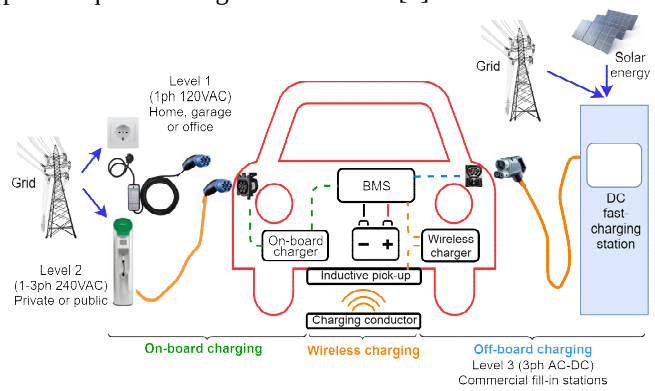

Fig. 1. On/off-board and wireless EVs charging system and power levels.

In general, there is a variety of off-board charging configurations for EVs. Since the industry is still in its infancy, there is a lack of EV fast charging standards. Many scientific studies have been recently developed to examine the possible converter configurations which will provide several features, such as low distortion operation, high power capability, fully adjustable power factor, minimum current and voltage ripples, reduced size/losses of input/output LC filters [9]-[13].

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Among the different converter topologies, the most promising ones are: a) Vienna rectifier topology, featuring compact size, high power density, high efficiency, low current total harmonic distortion and a simple control circuit [14], b) multilevel neutral point clamped (NPC) choppers [15], offering different output voltage levels to fit the battery requirements, and c) interleaved (multiphase) converters with reduced output current ripple and an increased efficiency.

In contrast to interleaved converters, Vienna rectifier is limited to unidirectional power flow and requires an additional buck-output stage for output voltage regulation, whereas multilevel NPC choppers add to system complexity because of higher number of power switches. Interleaving concept has as a main benefit the reduction in total current ripple amplitude and the increase in its efficiency by distributing the current (and the power) symmetrically among the phases. In that way, the reduction of size and cost of the passive components (filters) is achieved, and the overall cost of the system as well. Another great advantage of the interleaved configuration is modularity, standard and simple cell configuration, and inherent bidirectional power/current operating mode, particularly suitable for the energy storage management.

The interleaved topology has been used in ac/dc [16]-[18] and dc/dc [19]-[22] converter applications. In particular, [16] presents the design and the experimental verification of a three-phase unity-power-factor single-stage ac–dc converter based on the interleaved flyback topology. In [17] a comprehensive analysis of the impact of interleaving on the ripple currents in dc-side passive components of paralleled three-phase inverters has been presented. The effects of interleaving on the dc-side ripple currents were analyzed analytically for the simpler sinusoidal PWM scheme, and numerically for more complex modulation schemes. The design and control of a three-phase grid-connected interleaved voltage source inverter (VSI), employing an LC filter, has been presented in [18]. The topology proposed in [15] offers the advantages of reduced filter size, and high-grid disturbance rejection compared to an equivalent conventional two-level voltage source inverter with an LCL output filter. The construction and implementation of a high power density dc/dc converter for automotive applications were discussed in [20] and the thermal management of the converter was considered. A control technique, based on harmonic elimination, which allows for ripple minimization under asymmetric conditions of interleaved multiphase dc–dc converters has been introduced in [21], whereas [22] deals with the optimization of the components of a multiphase interleaved operated buck converter for battery charging applications.

The impact of PWM schemes on the common mode voltage of interleaved three-phase VSCs is analyzed in [23]. Hybrid multilevel-interleaved schemes have been also developed, trying to join the benefits of both configurations [11].

In this paper, a novel topology of an off-board dc fast battery charger for electric vehicles is proposed based on modular three-phase interleaved converters preliminarily introduced in [24]. A detailed description of the fast charging system has been provided in Section II. Section III focuses on the grid side interleaved segment of the charging system. Section IV enters more in details of current ripple analysis at the output dc stage of the charger. In addition, an effective control strategy is proposed in this section, providing ripple-free output current in a wide output voltage range. The effect of coupling on the individual inductor current ripple and the total input/output current ripple is discussed in Section V, considering two possible implementations of coupling, i.e. inverse and direct coupling. Realistic numerical simulations and corresponding experimental results are presented in Section VI to prove the effectiveness and the feasibility of the proposed voltage control strategy for the output dc segment of the charging system to obtain ripple-free output current. Finally, the conclusion is given in Section VII with a summary of the obtained results.

II. Proposed Fast Charging Conversion Scheme

The proposed fast charger is composed of an ac/dc interleaved 3x three-phase active rectifier and a dc/dc 3x three-phase interleaved chopper, sharing the same dc-link. As shown in Fig. 2, the proposed charger consists of six identical basic cells, each of them made of a standard two-level three-phase converter with three inductors. In case of the three-phase rectifier, basic charger cells are placed one in each phase, while in case of the chopper, three of them are connected in parallel (nine legs). The case study refers to the system parameters given in Table I.

Configuration on Fig. 2 offers many benefits, such as modularity, balanced power sharing among cells, robustness, low implementation cost, and straightforward configuration. Moreover, by employing identical modules (cells) the fast charger can be easily upgraded to higher output power rating. Since the charger is based on a modular scheme, it is inherently designed for easy maintenance and repair. Furthermore, by employing identical electric components, the charger can benefit from uniform power sharing among basic cells and its internal components. The similarity in components' operational characteristics ensures homogeneous voltage and thermal stresses among corresponding system elements.

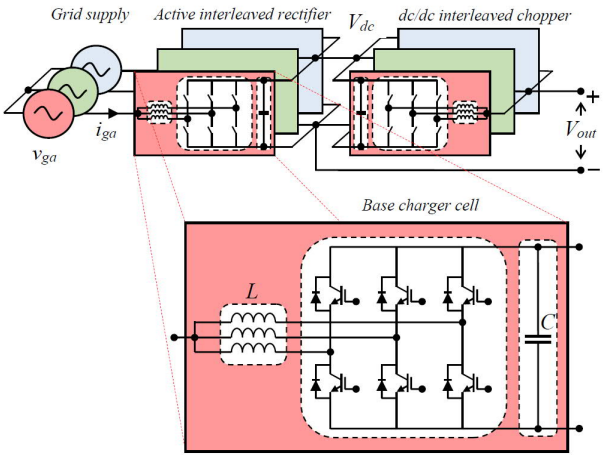

Fig. 2. Proposed modular scheme of the fast charger (top), consisting of the six identical basic cells having three interleaved legs (bottom).

Further advantage of using the proposed modular scheme is that the entire system can be built by a cheap and widely commercialized low-power two-level three-phase converter. For example, the three-phase basic cell in Fig. 2 can be sized just for 1/3 of a fast charger's rated power (the individual legs for 1/9 of the fast charger's rated power). It should be highlighted that voltage and current ratings between ac and dc side of the topology are quite similar. Since those three-phase power modules are commonly used in industry, there are many cheap and compact designs available on the market, which are optimized in terms of thermal layout, electromagnetic interferences, protections, and driver units. This provides unique opportunity to design reliable charging systems for a wide range of rated powers and voltages.

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TABLE I – MAIN SYSTEM PARAMETERS (CASE STUDY)

Parameter	Value
Total rated power, P (kW)	150
Individual base cell power with three interleaved legs (kW)	50
Line-to-line grid voltage (RMS), V_g (V)	400
Dc-link voltage, V_{dc} (V), rated at 700 V	600-800
Ac grid inverter and dc chopper switching frequency, f_{sw} (kHz)	16
Individual inductor parameters: L (mH), R (mΩ)	0.5, 20
Individual dc-link capacitance, C (mF)	1

III. INTERLEAVED GRID-INVERTER

The interleaved grid inverter has the task to regulate the dc-link voltage V_{dc} according to the strategy introduced in the next Section. The grid current control has been implemented in the synchronous rotating dq reference frame, according to the block diagram presented in Fig. 3, in order to obtain fast transient response, decoupled current component regulation, and no steady-state error.

In particular, grid voltages and currents are transformed from the abc to the dq reference frame. A phase-locked loop (PLL) algorithm is used to determine the phase angle ϑ_g of the grid voltage even in the presence of noise or harmonics. Direct and quadrature currents, i_d and i_q, are used to control active and reactive powers, respectively. The reference direct current is set to i_d^*, determined by the PI voltage controller comparing the actual dc-link voltage with its reference, whereas the reference quadrature current is set to zero to get unity power factor. Voltage components v_d^* and v_q^* are calculated by PI controllers and the decoupling reactor parameters (L and R, scaled by 3). The grid reference voltages are obtained by the inverse Park's transform, implemented by the centered PWM technique to maximize the modulation index. In the considered inverter scheme, the 3x base cell is adopted for each phase; therefore, three phase-shifted carriers are implemented to determine the firing signals.

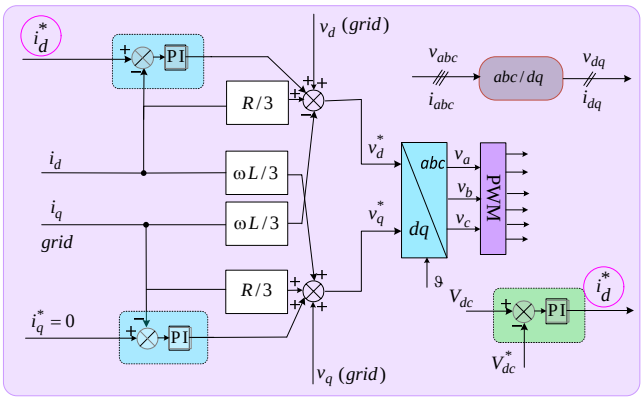

Fig. 3. Block diagram of dc-link voltage and grid current controllers for three-phase interleaved converter.

The maximum peak current ripple on the ac-link inductor (L) in case of a single two-level three-phase converter can be calculated according to [25]:

$$\Delta i_{L,ac}^{\max} = \frac{m}{4\sqrt{3}} \frac{V_{dc}}{L f_{sw}} \tag{1}$$

In the considered case of 3x interleaved three-phase converter, the maximum peak current ripple of the total grid current (Δi_{in}) is reduced almost 3 times compared to the individual inductor current ripple (Δi_L), according to [18]. Fig. 4 shows an operating example, pointing out the benefits of the interleaving with reference to the current ripple reduction in the proposed configuration.

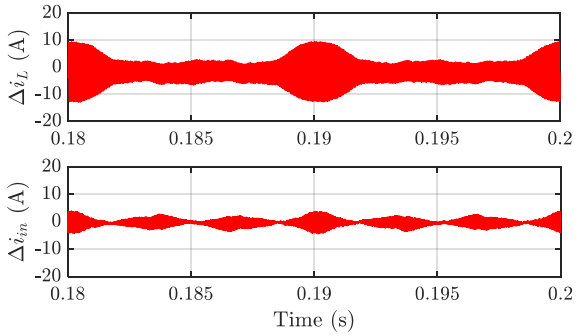

Fig. 4. Individual inductor current ripple (top trace) and total input (grid) current ripple (bottom trace) for the 3x interleaved three-phase converter at rated conditions (no mutual coupling).

IV. MINIMIZATION OF OUTPUT CURRENT RIPPLE

A. Effects of interleaving on current ripple

It is well known that multiphase interleaved dc/dc buck converters (IBCs) have an inherent capability to significantly reduce the output current ripple (amplitude), whereas inductor current ripple in each individual leg is not affected. The total instantaneous output current can be expressed as:

$$i_{out}(t) = \sum_N i_L(t), \tag{2}$$

where $i_L(t)$ is the instantaneous inductor current for each one of the N legs. The latter term is composed by its average value I_L and the instantaneous ripple component $\Delta i_L(t)$:

$$i_L(t) = I_L + \Delta i_L(t), \tag{3}$$

Also the total output current can be similarly written:

$$i_{out}(t) = I_{out} + \Delta i_{out}(t). \tag{4}$$

Therefore, from (2), (3) and (4) it results:

$$\begin{cases} I_{out} = \sum_N I_L \\ \Delta i_{out}(t) = \sum_N \Delta i_L(t). \end{cases} \tag{5}$$

From (5) it results that, in order to maximize the converter performance, I_L should be equally shared among the N legs, and Δi_L could be arranged to minimize the output ripple.

Taking into account the system parameters V_{dc}, f_{sw} and L, the peak inductor current ripple can be written as:

$$\Delta i_L(D) = \frac{V_{dc}}{2 L f_{sw}} D(1-D), \tag{6}$$

where D is the duty cycle of individual upper leg switch, and uncoupled inductors are considered. If carriers of N-phase IBC have constant shift 360°/N among themselves, then the peak output current ripple for $0 \le D \le 1/N$ can be written as

$$\Delta i_{out}(D) = \frac{V_{dc}}{2 L f_{sw}} D(1-ND). \tag{7}$$

General expression for full duty cycle span D = [0, 1] can be derived by shifting (7) to the right in steps of $1/N$, leading to:

$$\Delta i_{out}(D) = \frac{V_{dc}}{2 L f_{sw}} \left(D - \frac{k-1}{N}\right)\left(1 - N\left(D - \frac{k-1}{N}\right)\right), \tag{8}$$

for $(k-1)/N \le D \le k/N$, where $k = 1,\ldots, N$.

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To quantitatively estimate the benefit of interleaving, the ratio r of global maximums of output and inductor current ripples can be introduced:

$$r = \frac{\max\left(\Delta i_{out}(D)\right)}{\max\left(\Delta i_L(D)\right)} = \frac{1}{N}. \quad (9)$$

An increase of number of interleaved phases to N leads to a decrease of the peak value of output current ripple to $1/N$, which can be confirmed by Fig. 5 (bottom).

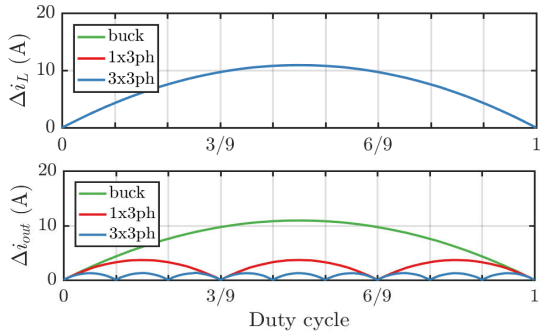

Fig. 5. Inductor current ripple (top, traces overlap) and output current ripple (bottom) for the three considered topologies (peak ripple).

Fig. 5 shows the distribution of current ripple amplitude for the three considered configurations: classic buck, 1×3 phase (i.e. 3-phase) IBC, and 3×3 phase (i.e. 9-phase) IBC. It must be pointed out that the first two topologies can be also recognized as building blocks of the proposed 3×3 phase IBC. For each topology, two current ripples corresponding to inductor (individual) and output (total) current are depicted.

Fig. 5 brings to light the existence of N–1 intermediate discrete duty cycles $D = k/N$, for which the corresponding output current ripple is exactly zero. On the contrary, an increase in phase number does not affect the inductor current ripples at all. Fig. 6 illustrates the aforementioned arguments for a worst case, corresponding to $D = 0.5$, as time series.

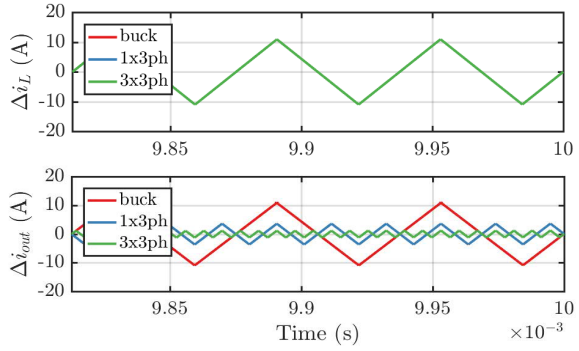

Fig. 6. Inductor current ripple (top, traces overlap) and total output current ripple (bottom) at $D = 0.5$ (general worst case) and $V_{dc} = 700$ V.

B. Proposed voltage control strategy

Currently, due to an infant development stage of high-power, high-energy batteries for EV application, there is no clear consensus on allowable output current ripple for fast chargers. However, there are different charging protocols, which are optimized for short charging time and efficiency, while maintaining a long-life cycle of a battery. Common feature of these protocols is an underlying assumption of minimum (or null) instantaneous charging current ripple.

Output current ripple characteristic (Fig. 5) of IBC suggests that is possible to achieve the objective of ripple-free output current if the 3×3 phase IBC works exclusively with a set of $N + 1$ duty cycles $\mathbf{D}_1 = \{k/N \mid k = 0, 1 \ldots N\}$. For all these operating points zero output current ripple is always guaranteed. In order to preserve a continuous range of output voltage $V_{out} = D \cdot V_{dc}$, the dc-link voltage V_{dc} must be adapted accordingly.

Furthermore, the constraints of the charging system should be taken into account (Table I). In particular, it is reasonable to assume that output voltage in the range from 200 V to 800 V will cater the needs of the majority of modern EVs. Having in mind that V_{dc} (intermediate dc-bus) can be controlled from $V_{dc,min} = 600$ to $V_{dc,max} = 800$ V by the grid converter (Fig. 3), the viable operating region can be identified (white area in Fig. 7). This region is intersected by specific set of duty cycles $\mathbf{D} = \{k/9 \mid k = 3, 4 \ldots 9\}$.

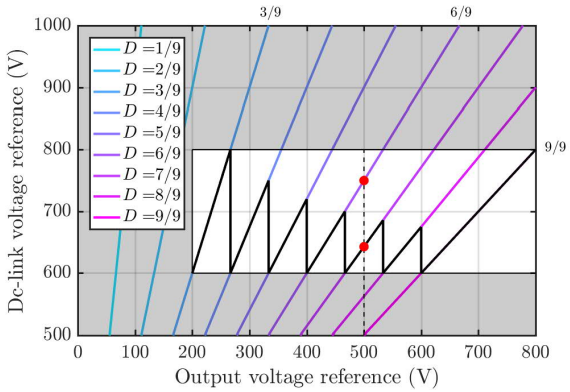

Fig. 7. Proposed voltage control strategy for ripple-free output current with dc-link voltage reference range V_{dc}^* = (600-800) V, resulting in a continuous output voltage reference range V_{out}^* = (200-800) V (thick black line).

Note that the dc-link voltage can be set precisely by the interleaved three-phase grid inverters, according to the control scheme of Fig. 3. In fact, in the considered case of balanced grid voltages and currents, the only residual dc-link voltage ripple is the switching ripple [26] that is completely negligible comparing to the dc-link voltage level [27].

By taking into account the above features and limitations of interleaved topology, the proposed ripple-free output current control strategy is depicted as thick black line in Fig. 7. Fig. 7 graphically confirms that even by restricting IBC operation to discrete duty cycles D, it is feasible to continuously control the output voltage from 200 V to 800 V with zero output current ripple. Fig. 7 also indicates that there are multiple choices of duty cycles for particular output voltages (e.g. for $V_{out}^* = 500$ V two different working points have been highlighted with red dots in Fig. 7 and later in Fig. 10).

Of course, the preferred duty cycle is the one that minimizes the inductor current ripple as well as voltage stress on the system components. It is obvious that the recommended control characteristic (thick black line) always follows the duty cycles associated with lower V_{dc}^* (e.g. lower red dot is preferred for $V_{out}^* = 500$ V). The resulting proposed control algorithm is given in Table II.

A remark concerning tracking capability of the proposed strategy is necessary. Because the algorithm (Table II) is an open-loop scheme, it does not compensate for voltage drops in real operating conditions, which results in steady-state error $e = V_{out}^* - V_{out}$. However, the primary objective of the proposed algorithm is to provide a ripple-less output current for all steady-state operation points, not the ideal tracking of V_{out}^* per se. The algorithm ensures that even in real conditions, the output current will remain without ripple. Tracking with zero steady-state error, if needed, can be easily restored by an appropriate outer voltage control loop (see blue outer loop in Fig. 12).

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TABLE II – ALGORITHM FOR DC-LINK VOLTAGE REFERENCE ($N = 9$)

Input: Output voltage reference V_{out}^*
Input: dc-link voltage limits $V_{dc,min}$ and $V_{dc,max}$
Output: dc-link voltage reference V_{dc}^*
1: **switch** V_{out}^*
2: **case A**: $V_{dc,min} \le V_{out}^* \le V_{dc,max}$
3: select $D = 9/9$ and $V_{dc}^* = V_{out}$
4: **case B**: $8/9 \cdot V_{dc,min} \le V_{out}^* < V_{dc,min}$
5: select $D = 8/9$ and $V_{dc}^* = 9/8 \cdot V_{out}$
6: **case C**: $7/9 \cdot V_{dc,min} \le V_{out}^* < 8/9 \cdot V_{dc,min}$
7: select $D = 7/9$ and $V_{dc}^* = 9/7 \cdot V_{out}$
8: **case D**: $6/9 \cdot V_{dc,min} \le V_{out}^* < 7/9 \cdot V_{dc,min}$
9: select $D = 6/9$ and $V_{dc}^* = 9/6 \cdot V_{out}$
10: **case E**: $5/9 \cdot V_{dc,min} \le V_{out}^* < 6/9 \cdot V_{dc,min}$
11: select $D = 5/9$ and $V_{dc}^* = 9/5 \cdot V_{out}$
12: **case F**: $4/9 \cdot V_{dc,min} \le V_{out}^* < 5/9 \cdot V_{dc,min}$
13: select $D = 4/9$ and $V_{dc}^* = 9/4 \cdot V_{out}$
14: **case G**: $3/9 \cdot V_{dc,min} \le V_{out}^* < 4/9 \cdot V_{dc,min}$
15: select $D = 3/9$ and $V_{dc}^* = 9/3 \cdot V_{out}$
16: **end**

Voltage control strategy given in Fig. 7 and Table II ensures zero output ripple and continuous range of output voltage from 200 V to 800 V for steady-state operation. Every change in the reference output voltage V_{out}^* requires an adjustment of V_{dc} and D. The generalized procedure for evaluating the reference dc-link voltage V_{dc}^* for any number of phases N can be summarized by the following equation

$$V_{dc}^* = \begin{cases} \dfrac{N}{\text{floor}\left(\dfrac{N V_{out}^*}{V_{dc,\min}}\right)} V_{out}^* & V_{out}^* \le V_{dc,\min} \\ V_{out}^* & V_{out}^* > V_{dc,\min} \end{cases} . \quad (10)$$

The reference dc-link voltage V_{dc}^* is sent to the controller of the active rectifier that will adjust the actual value V_{dc} accordingly. Because V_{dc} cannot change instantaneously, a short transient is needed to reach $V_{dc} = V_{dc}^*$. In order to ensure $V_{out} \approx V_{out}^*$ during the transient, the duty cycle D is determined using the actual dc-link voltage instead of reference dc-link voltage

$$D = \frac{V_{out}^*}{V_{dc}} . \quad (11)$$

In this paper, the number of phases N for the dc-dc interleaved converter is equal to 9. It is worth noting that by considering $N = 9$ and steady-state condition, (10) and (11) lead to Table II. Fig. 8 shows a performance of the voltage control strategy during transient operation. The reference output voltage V_{out}^* increases in 7.6 V steps every 50 ms (top subplot), which results in the output current increase of 50 A for each step (bottom subplot). Red traces in the center subplots depict D and V_{dc}, respectively. The strategy behind (11) ensures that output voltage tracks its reference (allowing for steady-state error in real conditions) with high bandwidth $V_{out} \approx V_{out}^*$, which does not depend on the dc-link dynamics. In fact, the bandwidth of the output voltage tracking depends solely on the sampling frequency of the fast charger. This is crucial for a real battery charger application, where an outer dc-current control loop is implemented to track the current reference by adjusting reference output voltage V_{out}^*.

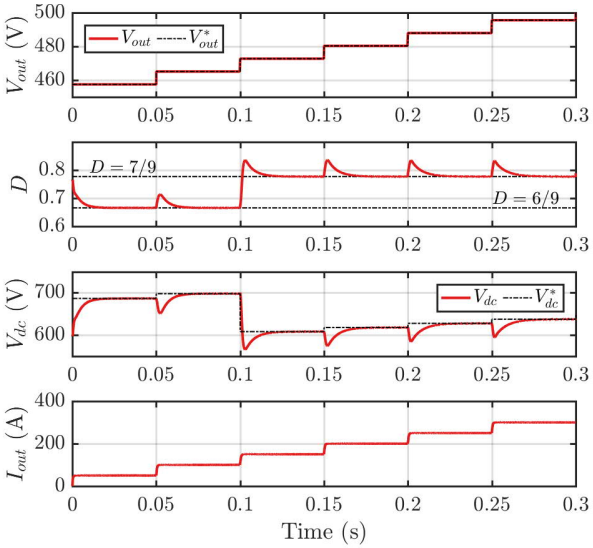

Fig.8. Voltage control strategy performance for V_{out}^* stepwise changes.

The immediate consequence of (11) is that during the transient the fast charger is not working in the ripple-free point (Fig. 9). However, as soon as the transient is over and the steady-state condition is reached ($V_{dc} = V_{dc}^*$), the output current ripple is zero again as can be seen on Fig. 9. As the transients are comparatively short, this mode of operation is acceptable.

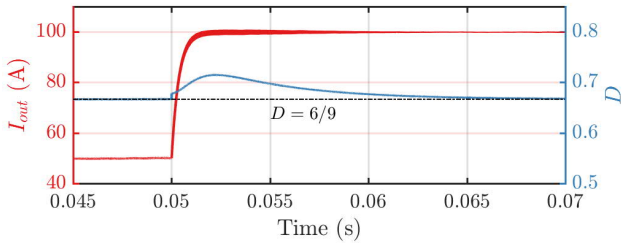

Fig. 9. Output current and duty cycle during one transient from Fig. 8.

Fig. 10 shows accompanying inductor current ripple in case of bounded dc-link voltage range. The proposed control characteristic also ensures lowest possible current ripple throughout operating range (thick black line). This is expected, because the proposed voltage strategy always chooses the duty cycle D associated with lower V_{dc}. The relevant cases occurring for D = 3/9, 6/9, and 9/9 (Fig. 5), giving zero ripple also for the base cell current, do not introduce additional benefits.

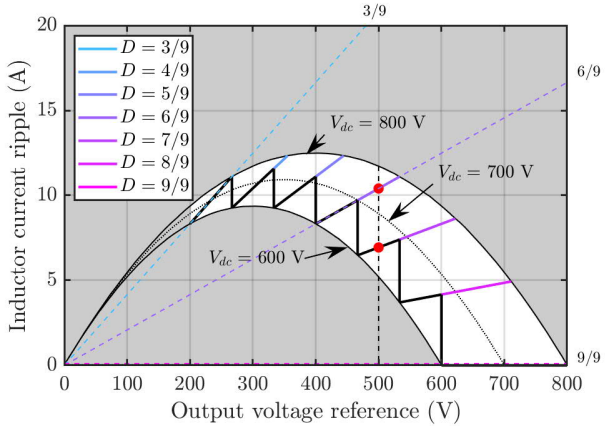

Fig. 10. Inductor current ripple with bounded dc-link voltage range for $f_{sw} = 16$ kHz and $L = 0.5$ mH; thick black line corresponds to proposed control characteristics in Fig. 7.

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In order to illustrate the results of proposed control strategy, Fig. 11 depicts inductor, base cell, and output current waveforms in case of i_{out} = 300 A and V_{out} = 500 V. This particular operating point can be obtained with two different duty cycles, i.e. D = 6/9 and D = 7/9 (left and right in Fig. 11, red dots in Figs. 7 and 10). Even though the output current ripple is zero for both cases, the inductor current ripple is clearly lower in case of D = 7/9, in agreement with Fig. 10.

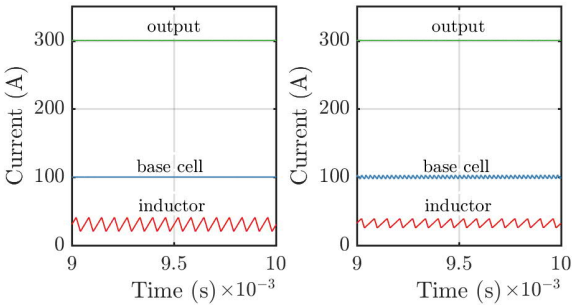

Fig. 11. Inductor, base cell, and total output current for V_{out} = 500 V, in case of: D = 6/9, V_{dc} = 750 V (left), and D = 7/9, V_{dc} = 640 V (right).

Final step in designing battery-charging method is a choice of charging mode, e.g. constant current or constant voltage mode. In any case, a closed-loop with suitable control law (e.g. PI controller) is added to the proposed control algorithm, as shown in Fig. 12. The controller then adapts V_{out}^*, in order to track i_{out}^* or $V_{out,cl}^*$ without steady-state error even in real conditions. The output current i_{out} will remain without ripple, independent of the chosen charging mode.

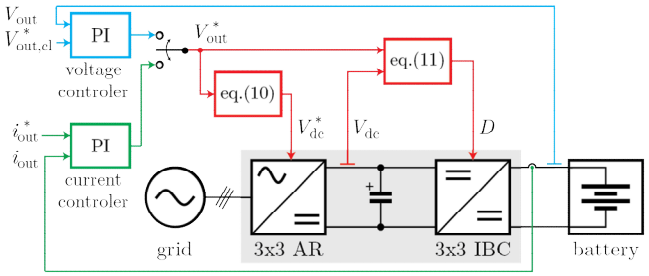

Fig. 12. Two possible closed-loop control upgrade for voltage (blue) or current (green) charging modes.

V. Effects of Three-phase Mutual Coupling

Inductor size greatly contributes to the total volume and cost of the conversion system. A possible way to reduce the dimensions of inductors and enhance the system's efficiency is to introduce magnetic coupling between phases [23]. By doing so, the three separate inductors within each base cell are replaced by three mutually coupled inductors, where L is self-inductance and M is mutual inductance between pair of inductors. Coupling coefficient k_c is defined as a negative ratio of mutual inductance M and self-inductance L

$$k_c = -\frac{M}{L}. \tag{12}$$

There are two possible implementations of the coupling, i.e. inverse coupling ($k_c > 0$) and direct coupling ($k_c < 0$).

A. Output (dc battery) side

The inverse coupling in IBC enables a reduction of dc magnetic flux density and thereby a decrease of core losses in inductors [28]. At the same time this measure affects inductor current ripple and, by extension, copper losses (Fig. 13). Thus, a design of the mutually coupled inductors is a multi-objective optimization problem, which aims to minimize the volume and total losses in inductors [29].

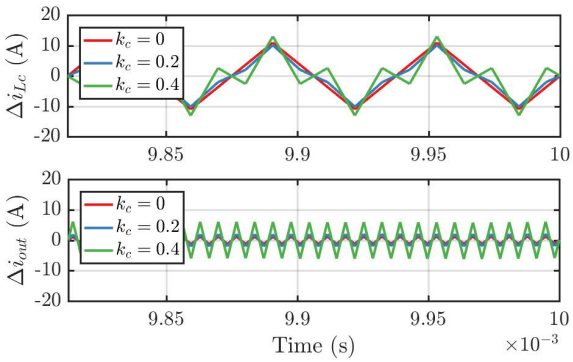

Fig. 13. Effect of coupling on inductor (top) and output (bottom) current ripple (D = 0.5 and V_{dc} = 700 V).

In this subsection, we evaluate the influence of the mutual coupling on the proposed ripple-free fast charger. If mutual coupling does not worsen the fast charger performance (in particular zero output current ripple), this design optimization methodology can be readily employed. By introducing mutual coupling, the inductor current ripple (Δi_{Lc}) becomes function of the coupling coefficient k_c. In order to assess the coupling effect, it is beneficial to compare the inductor current ripple for coupled and uncoupled (Δi_L) inductors. Adopting the results from [30, 31] one can obtain:

$$\Delta i_{Lc}(D,k_c)=\begin{cases}\dfrac{1-\left(\dfrac{D}{1-D}+\dfrac{1}{2}\right)2k_c}{(1+k_c)(1-2k_c)}\Delta i_L, & 0\le D\le\dfrac{1}{3}\\[2ex] \dfrac{1-\left(\dfrac{1}{3D(1-D)}-\dfrac{1}{2}\right)2k_c}{(1+k_c)(1-2k_c)}\Delta i_L, & \dfrac{1}{3}\le D\le\dfrac{2}{3}\\[2ex] \dfrac{1-\left(\dfrac{1-D}{D}+\dfrac{1}{2}\right)2k_c}{(1+k_c)(1-2k_c)}\Delta i_L, & \dfrac{2}{3}\le D\le 1\end{cases} \tag{13}$$

where inductor current ripple Δi_L is defined by (6).

The following analysis is limited to the evaluation of the coupling effect and does not include the magnetic design of the inductors. At the end, we nevertheless give a recommendation on the optimal coupling coefficient given the constraints of the proposed voltage control strategy.

Fig. 14 illustrates the dependence given in (13) as a 3D surface plot. The edge of the plot at coupling coefficient k_c = 0 shows inductor current ripple for non-coupled inductors Δi_L. For k_c = [0, 0.3] the inductor current ripple Δi_{Lc} remains very close to Δi_L for almost all duty cycles. However, for k_c > 0.3 the Δi_{Lc} starts to increase and in case of ideal coupling (k_c = 0.5), where dc magnetic flux density is cancelled completely, inductor current ripple rises infinitely. That being said, there are also two distinct regions around D = 3/9 and D = 6/9, where inductor current ripple Δi_{Lc} actually steadily decreases with increasing coupling. This detail is better visible in Fig. 15 (top), which shows corresponding parametric 2D plot for three coupling coeficients k_c = 0, k_c = 0.2 and k_c = 0.4. By increasing mutual coupling, the inductor current ripple decreases around D = 3/9 and D = 6/9, while at the same time increases elsewhere. It can

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be noted that $k_c = 0.2$ is actually more suitable choice than $k_c = 0.4$, since it effectively guarantees the lowest inductor current ripple for nearly all duty cycles.

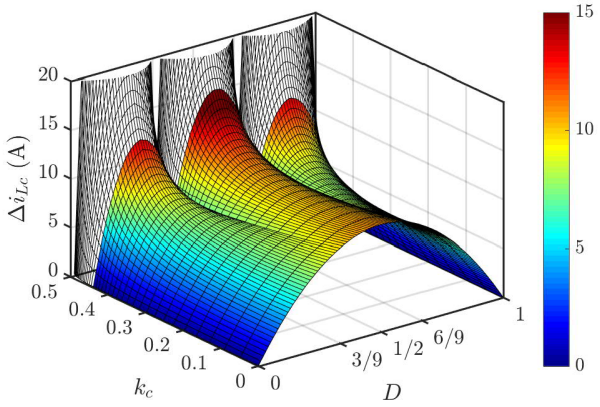

Fig. 14. Inductor current ripple for 3×3 phase IBC at V_{dc} = 700 V.

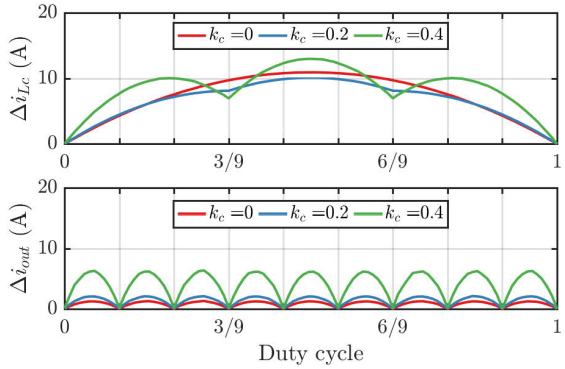

Fig. 15. Inductor and output current ripple – inverse coupling ($k_c > 0$).

The influence of mutual coupling on the output current ripple Δi_{out} can be seen in Fig. 16. For almost all duty cycles the mutual coupling causes an increase in Δi_{out}. However, it is important to note that the coupling does not deteriorate the performance at the specific set of duty cycles $\mathbf{D}_1 = \{k/9 \mid k = 0, 1 \ldots 9\}$. Output current ripple remains exactly zero regardless of coupling. Therefore, the coupling does not influence the original choice of discrete duty cycles **D** and proposed control strategy (Fig. 7) remains valid for coupled case as well.

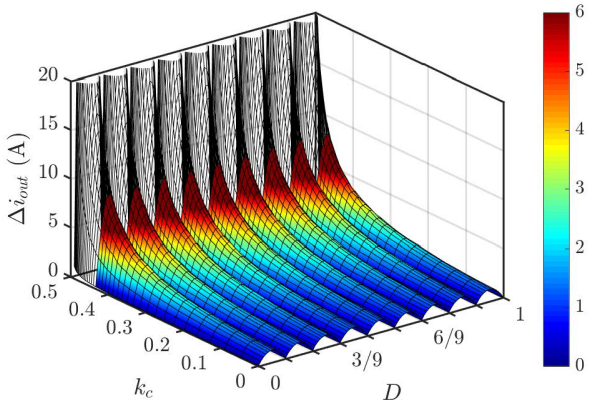

Fig. 16. Output current ripple for 3×3 phase IBC at V_{dc} = 700 V.

For the sake of completeness, Fig. 17 shows corresponding inductor and output current ripples in the case of direct coupling ($k_c < 0$). In this case, an increase in coupling always causes higher inductor current ripple, whereas its output counterpart always decreases. However, since proposed control method guarantees zero output current ripple by definition, the use of direct coupling is not beneficial. Moreover, the direct coupling increases a dc magnetic flux density and core losses, therefore is not a reasonable solution.

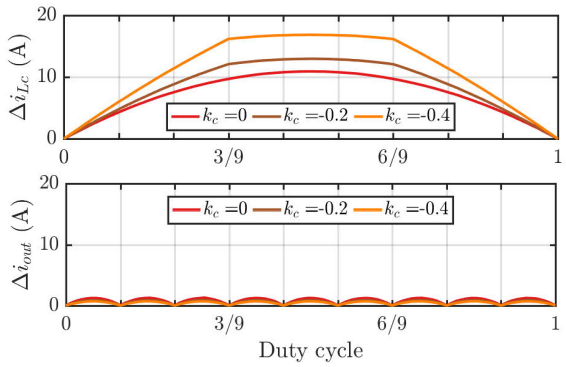

Fig. 17. Inductor and output current ripple – direct coupling ($k_c < 0$).

Fig. 18 presents the relation of inductor current ripple and coupling for a chosen set of duty cycles **D**.

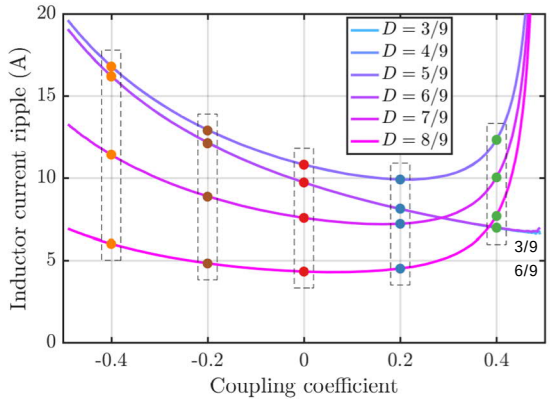

Fig. 18. Inductor current ripple for a proposed set of duty cycles D. Group of dots denote inductor current ripples for k_c = –0.4 (orange), k_c = –0.2 (brown), k_c = 0 (red), k_c = 0.2 (blue), and k_c = 0.4 (green).

Note, that some lines are overlapping, namely for D = 3/9 and D = 6/9, as well as for D = 4/9 and D = 5/9, due to a plane symmetry of the current ripple around D = 0.5. It is possible to define an objective function composed of inductor current ripples at duty cycles **D**

$$J(k_c) = \sum_{k=3}^{9} \Delta i_{Lc}\left(\frac{k}{9}, k_c\right), \tag{14}$$

and determine its minimum, which is $k_c^{\min} = 0.239$ for the proposed topology. This value could be considered a good comprise for minimizing inductor current ripple, while using proposed control strategy.

B. Input (ac grid) side

Since the compact modular solution is preserved unchanged for input (grid) side as well, the effect of inverse coupling on input currents has been verified too (Fig. 19 and Fig. 20). In case of k_c = 0.2 (Fig. 19), the mutual coupling causes slightly lower inductor current ripple (top) and higher input current ripple (bottom) in comparison to non-coupled case (Fig. 4). As expected, this effect is the same as for the output side. However, in case of k_c = 0.4 (Fig. 20), it causes an opposite effect resulting in an increase in both inductor and total current ripple compared to non-coupled case.

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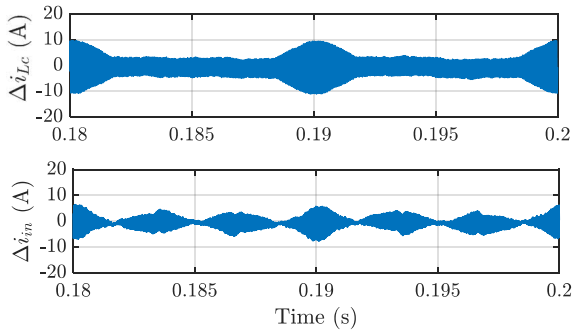

Fig. 19. Individual inductor current ripple (top trace) and total input (grid) current ripple (bottom trace) for 3x interleaved three-phase converter at rated conditions in case of inverse coupling (k_c = 0.2).

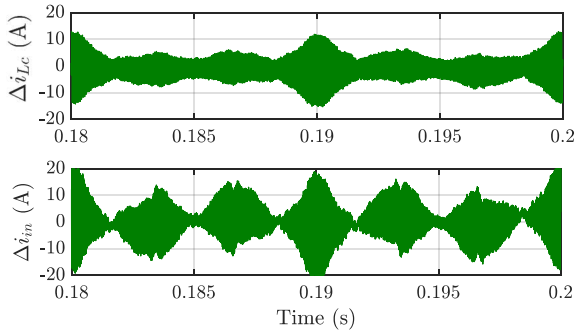

Fig. 20. Individual inductor current ripple (top trace) and total input (grid) current ripple (bottom trace) for 3x interleaved three-phase converter at rated conditions in case of inverse coupling (k_c = 0.4).

It should be pointed out a major difference between input (grid) and output (battery) sides in terms of current ripple amplitudes. On the battery side, the undesirable output ripple is completely canceled by employing proposed voltage control strategy, which ensures zero output current ripple for any operating condition. On the other hand, the input (grid) side cannot be provided with comparable zero-ripple solution, and the operation with some grid current ripple is unavoidable.

It is interesting to consider the direct coupling of the 3x three-phase inductors (Fig. 21 and Fig. 22). Here, the inductor current ripple (top) unavoidably becomes larger, whereas total grid current ripple actually decreases (bottom). Since the instantaneous currents in interleaved configuration are essentially the same, the directly coupled inductor acts as a common mode filter.

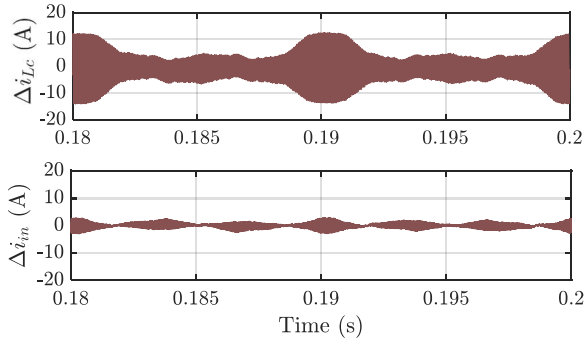

Fig. 21. Individual inductor current ripple (top trace) and total input (ac) current ripple (bottom trace) for 3x interleaved three-phase converter at rated conditions in case of direct coupling (k_c = – 0 .2).

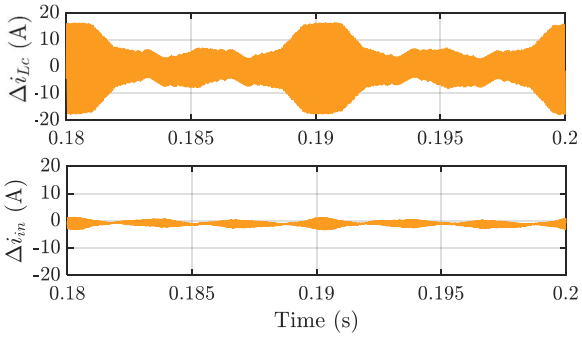

Fig. 22. Individual inductor current ripple (top trace) and total input (ac) current ripple (bottom trace) for the 3x interleaved three-phase converter at rated conditions in case of direct coupling (k_c = – 0.4).

VI. Simulation and Experimental Results

The practical implementation of the proposed fast charger (rated at 150 kW with the parameters of Table I) can be carried out based on compact three-phase power modules, such as the Mitsubishi PS22A79 intelligent power IGBT module (1200V, 50A).

Since the ac/dc converter works in standard conditions, only the 9-phase output dc/dc interleaved converter has been realized for the experimental tests, in order to verify the ripple-free output current operation capabilities. In particular, the output converter has been implemented by interleaving 3x three-phase cells, according to Fig. 2. The 3x three-phase cells are driven by a TMS320F28379D DSP microcontroller board via optical interface links.

Working test conditions have been scaled down according to the limited power/voltage capabilities available in the Laboratory. In particular, comparing to Table I, dc-link voltage range has been scaled down 4 times by a factor of 4 (150-200 V), and the output current by a factor of 10 (max 30 A), making possible to use two series-connected TDK-Lambda GEN100-33 dc power supply (max ratings 2x100 V, 33 A).

In order to properly scale down the individual inductor current ripple, output inductances have been increased to 1.73 mH, with a preliminary custom-made air-core inductors, built for the sake of the flexibility to adjust the desired parameters. A power resistors arrangement with a total resistance of 6 Ω has been adopted as a dc load to absorb the power corresponding to the battery charge.

The detailed view of an individual three-phase cell and the tower arrangement of three base cells is given in Fig. 23, whereas the view of the whole experimental setup is shown in Fig. 24.

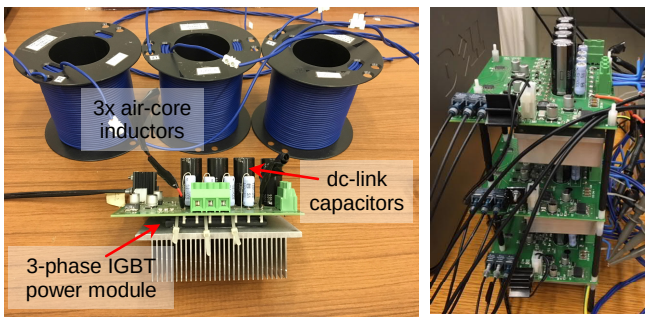

Fig. 23. Basic three-phase power cell and tower arrangement of three cells.

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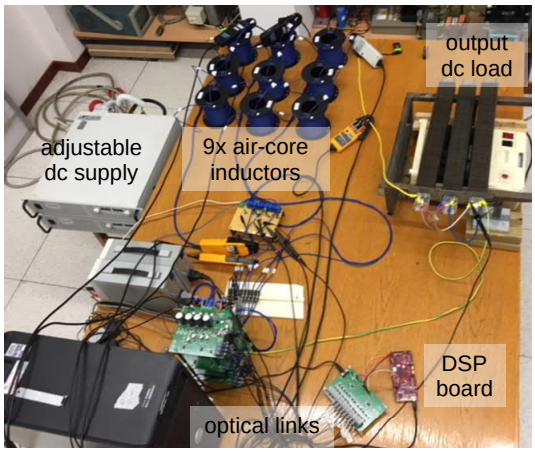

Fig. 24. View of the whole experimental setup.

In order to better support the experimental verifications, corresponding simulation tests are carried out for the 9-phase dc/dc interleaved converter, according to Fig. 2. The circuit simulations are performed by Matlab/Simulink. The pre-set parameters (resistances, inductances, capacitances, etc.), used in these simulations, have practically equivalent values measured in the real experimental setup. Simulation and experimental parameters are summarized in Table III.

TABLE III – REDUCED-SCALE SYSTEM PARAMETERS (SIMULATIONS AND EXPERIMENTS)

Parameter	Value
Dc-link voltage, V_{dc} (V)	150-200
Dc chopper switching frequency, f_{sw} (kHz)	16
Individual interleaved phase inductance, L (mH)	1.73
Individual interleaved phase resistance, R (Ω)	0.73
Output (load) resistance (Ω)	6

The experimental results (measured signals) were acquired, using digital oscilloscopes (Rigol DS 1054Z), with sampling rate 25MSa/s and memory depth 6Mpts. Later, the stored experimental data was plotted via Matlab. The time windows of corresponding time series plots were shifted accordingly to present their agreement more evident.

Fig. 25 (a) and (b) presents simulation and experimental results, respectively, for individual inductor currents in the case of D = 6/9, i_{out} = 21 A and V_{out} = 125 V. The dc-bus voltage V_{dc} must be set at the level of 192.1 V. By operating the system at this working point, the average inductor current is around 2.33 A, while the peak value of ripple component is in the order of 0.75 A, which is consistent with the theoretical result given by (8), i.e. Δi_L = 0.77 A.

To illustrate the performance of the proposed charger and its original control strategy, Fig. 26 depicts individual inductor, base cell, and output current waveforms. The same operating conditions have been considered for the examined working points (D = 6/9, D = 6.5/9 and D = 7/9), namely i_{out} = 21 A and V_{out} = 125 V. The ripple-free output current occurs at specific duty cycles, which are multiple duties of 1/N. In particular, two duty cycles belonging to the proposed control strategy, i.e. D = 6/9 and D = 7/9, are considered (corresponding to Fig. 11). A third additional intermediate case D = 6.5/9 is shown to emphasize the advantage of operating the system at the specific working points.

However, even though the output current ripple is zero for both cases (6/9 and 7/9), the inductor current ripple is clearly lower in case of D = 7/9. This is in agreement with Fig. 5 (top) and Fig. 10. Meanwhile, a reverse increase of base cell currents can be found going up from D = 6/9 to 7/9 (red trace in Fig. 5).

The harmonic content of inductor, cell and output currents is shown in Fig. 27, from top to bottom. Fig. 27(a) presents the simulation results, whereas Fig. 27(b) presents the corresponding experimental results.

It is well visible that the *THD* of the inductor current in both simulation and experimental results (Fig. 27 – top), decreases while increasing the duty cycle (as in Fig. 5), with the existence of the fundamental switching harmonic (16 kHz) and its multiples.

For the base cell current (Fig. 27 – middle), the *THD* is practically zero for all duty cycle having duties 3k/N, which is the case of 3/9 and 6/9. The *THD* of base cell current increases while increasing the duty cycle from 6/9 to 6.5/9 and 7/9 with the existence of harmonics multiple of three.

For the output current (Fig. 27 – bottom), the *THD* is practically zero for all duty cycle having duties k/N. In the intermediate case D = 6.5/9 the residual *THD* is introduced by the presence of the N-th harmonic (and its multiples).

A so-called 'form factor' of a signal was calculated for each current waveform presented in Fig. 27. The form factor is denoted as k_f and calculated as the ratio of I_{rms} - RMS (root mean square) value of the considered current waveform to I_{mean} - the average value of that current (mathematical mean of absolute values of all points of the waveform). The computed values of form factors are depicted in the plots' legends (see Fig. 27) in correspondence to a current in the particular study case.

Despite the unavoidable noise that is present in experimental results (overall the magnitude of its individual harmonics is less than 1% with respect to magnitude of the current's dc component), a good match between simulation and experimental results can be observed, supporting analytical developments made in this paper.

VII. CONCLUSION

In this paper, a new grid-connected high-power fast battery charger for electric vehicles has been proposed. The topology is based on modular arrangement of six three-phase interleaved converters, individually rated around 50 kW and giving a total power of 150 kW in the case study.

Such a topology permits the use of classic and reliable three-phase power switch modules (either IGBTs or SiC MOSFETs) with typical voltage class and current rating. With respect to reasonable system constraints (dc-bus voltage: 600–800 V and output voltage: 200–800 V) an original control strategy has been proposed, ensuring zero output current ripple in entire output voltage range.

Although the inductor design by itself was not the focus of the paper, the influence of mutual coupling has been investigated as well. However, no significant advantages of mutual coupling on system performance could be confirmed.

A set of numerical and experimental results referred to a reduced scale prototype focused on the output stage of the considered fast battery charger configuration has been carried out, confirming the effectiveness of the proposed output ripple-free control strategy.

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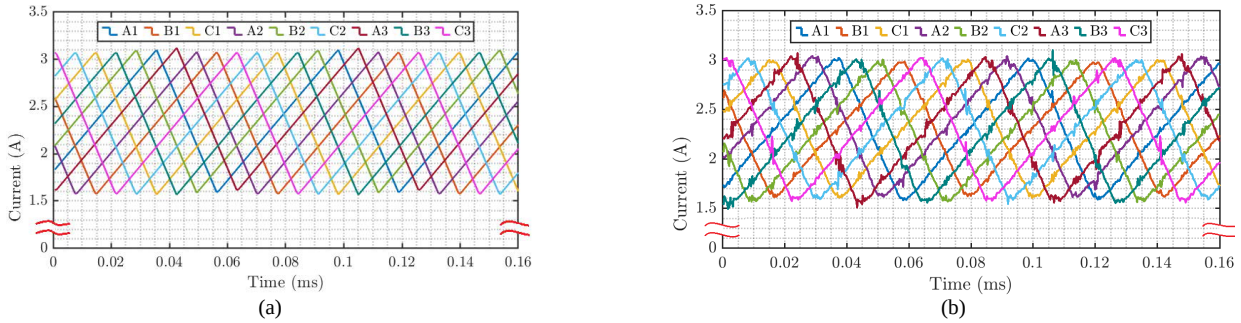
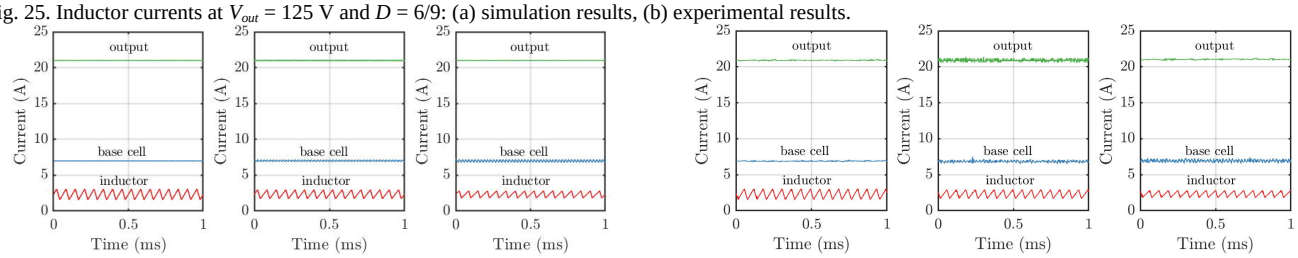


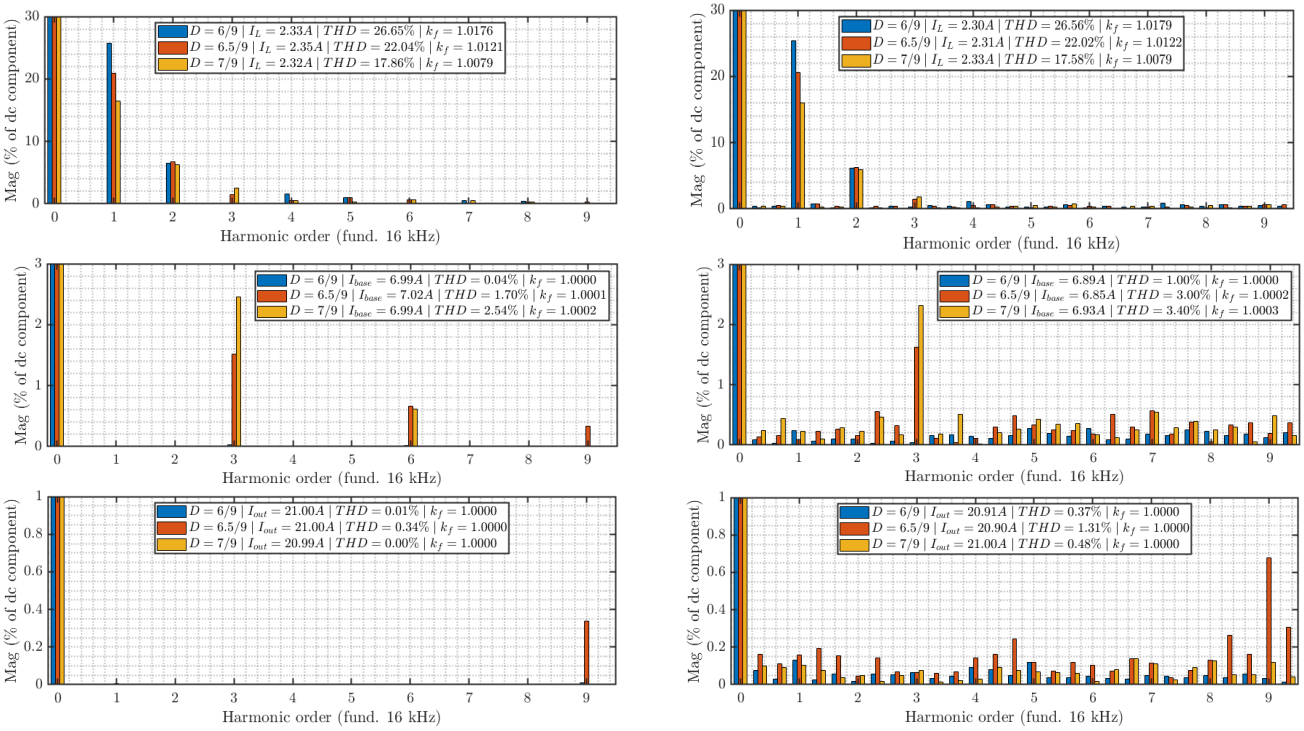
(a) (b)

Fig. 25. Inductor currents at V_{out} = 125 V and D = 6/9: (a) simulation results, (b) experimental results.



(a) (b)

Fig. 26. Inductor, base cell, and total output current at V_{out} = 125 V, in case of D = 6/9, V_{dc} = 192.1 V (left), D = 6.5/9, V_{dc} = 176.8 V (middle) and D = 7/9, V_{dc} = 167.2 V (right): (a) simulation results, (b) experimental results.



(a) (b)

Fig. 27. Harmonic contents of individual inductor (top), base cell (middle) and output (bottom) currents for the cases D = 6/9, D = 6.5/9 and D = 7/9: (a) simulation results, (b) experimental results.

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