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Abstract The DBBC3 is a flexible VLBI backend and environment that supports a wide range of observational needs via a suite of FPGA firmware types. The hardware can sample up to eight 4 GHz-wide baseband signals and convert to digital streams over multiple 10GE links on fibre. The development team has an ongoing development programme that has enhanced existing modes and introduced new desired modes as user requirements evolve. Three different firmware types for observing have been implemented which will be briefly summarised: Direct Sampling Conversion (DSC), arbitrary selection of bands (OCT), Digital Down Conversion (DDC). These modes cover all the requirements of astronomical, VGOS and legacy geodetic VLBI of the present, but also of the near future. At the same time the DBBC3 is an important platform for additional new modes to be implemented for the BRAND receiver. This paper describes the use of the DBBC3 for the receiver development, pointing out which element in the current DBBC3 structure will be part of the BRAND receiver in order to simplify its introduction into the existing VLBI environment at telescopes with a DBBC3 backend.

Keywords Digital Receiver · VLBI · VLBI Backends

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1 Introduction

The Digital Base-Band Converter 3 (DBBC3) is the third generation VLBI backend developed in a European collaboration under the lead of G. Tuccari (see e.g. Tuccari et al., 2019). The system is modular and, as of today, in a configuration with eight sampler/processor pairs is fully VGOS compliant. It takes as input eight 4 GHz-wide IFs in the range 0 GHz to 15 GHz. Different channel (sub-band) widths of 1-2-4-8-16-32-64-128 MHz can be selected from each 4 GHz input via Digital DownConverter (DDC) firmware for output. Alternatively OCT filters allow the selection of arbitrary parts of the band using 32-tap FIR convolutional filters acting on the time series from the sampler. Filter tap weights have been designed to produce filter widths of 512 MHz, 1024 MHz and 2048 MHz and others are possible by simply loading different weights into the tap registers. When using the 2048 MHz filter one can use two filters to cover the full 4 GHz, which makes this mode compatible with the R2DBE system used in the Event Horizon Telescope. The full 4096 MHz band can be output also without any channelisation. The resulting output data rates are 16/32/64/128 Gbps.

For the European VLBI Network (EVN) the DBBC3 shall replace the DBBC2 using its backward-compatible modes, and at the same time open the

Fig. 1: DBBC3 VGOS model: 8 IFs with 8 groups of ADB3 samplers and CORE3 processing boards. This unit can deliver 128 Gbps with 2-bit samples (output limit is 512 Gbps).

Fig. 2: Four bands (IFs) are fed to the four inputs of the sampler chip (blue). They are either one of 0 GHz to 14 GHz or 14 GHz to 15.5 GHz and one of the possible polarisations. In the FPGAs (green) the serial data streams are converted to parallel. Next step is band selection, then polarisation conversion or other pre-processing. Last the digitised data are streamed to ethernet. In the DBBC3 (red), standard VLBI channelisation and formatting are performed with output of the VLBI data to internet or recorders.

avenue to observations with data-rates up to 32 Gbps, possible with EVN's widest IFs at higher frequencies.

2 Modifying the DBBC3 for the BRAND project

The BRAND EVN project is a EU-sponsored engineering research effort to develop and build a prototype receiver with a frequency coverage from 1.5 GHz to 15.5 GHz (see Alef et al., 2019). The full band will be sampled in the receiver box without any down-conversion. All usable parts of the band will be selected on the same board as the sampler chip via four powerful FPGA processors. Pieces of up to 4 GHz width represented as 8-bit samples will be sent to the backend via optical fibres. The overall structure of the data flow can be seen in Fig 2.

The DBBC3 is used here as an ideal platform to handle 4 GHz portions of the full 14 GHz input band for creating compatible VLBI channels with the observing modes described in the introduction. The actual bandwidth of the BRAND EVN channels will be slightly different from VLBI standards due to the different sampling frequencies compatible with the sampler chip. The sampler device includes its own synthesizer which operates in a restricted range from which sampling clocks can be selected. The value selected for BRAND, 28.732 Gsps, is not a power of 2 but allows one to derive integer MHz bandwidths
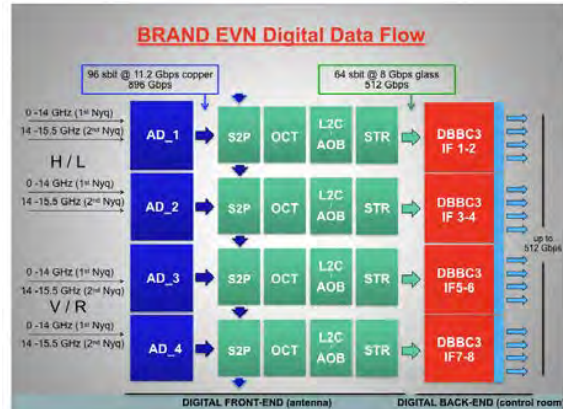
in the digital signal processing chain. This leads to channelised bandwidths of 7/14/28/56/112/224 MHz out from the digital frontend, from which the OCT or DDC firmware in the DBBC3 selects bands of 4/8/16/32/64/128 MHz (plus optional resampling), ensuring compatibility with the bandwidths currently used in VLBI.

The BRAND EVN data flow involving sampling and digital processing can be functionally divided into two blocks, one placed in the receiver frontend in the antenna and one in the control room where traditionally the backends are located. For this reason we can define the first part a digital frontend and the second a digital backend. The distinction is useful because different functions are performed in the two separated locations.

The main process in the digital frontend part will, in the first implementation, be the formation of 4 GHz slices as input to the digital backend. The process in the digital backend will be the normal VLBI process of further channelisation to select sub-bands from the 4 GHz slice, truncating to 2 bits, and producing VDIF streams for recording.

In more detail, the digital frontend is now the locus directly following the analogue signal path which consists of antenna, feed, filters, low-noise amplifiers and other components, all of which bring the signal to a level suitable for the sampler to sample with a nomi-

nal 8-bit depth. The digitised data from the sampler are then converted from serial to parallel streams, filtered with a 4 GHz OCT filter, decimated, time-stamped, formatted as VDIF with 8-bit depth, and prepared in IP packets for transmission on 16 10 GE links per analogue input to the digital backend. Four such analogue inputs are sampled by one sampler chip, coming from the four channels carrying the ranges 0-14 GHz/14-15.5 GHz in both polarisations from the analogue section of the receiver. (Fig 2).

The resulting data rate from the sampler is huge – more than 900 Gbps. It is transferred from the digital frontend to digital backend on a large number of optical fibers (64) carrying VLBI standard VDIF packets, which contain also the sampling time information along with the data packed as the DBBC3 receiving section requires.

The timestamps inserted by the digital frontend are the time reference used for later correlation of VLBI data, therefore the UTC 1 PPS and frequency reference must be available at the frontend digital receiver, which includes for instance connecting a GPS receiver to the digital frontend.

The digital backend DBBC3 will receive the data into the CORE3H boards via the ethernet connectors using a dedicated firmware/software to be loaded for this mode. Subsequent processing proceeds as usual for the DBBC3 when doing VLBI.

The digital frontend can in principle perform other more complex operations which will be implemented in the future, like dynamic OCT filtering for RFI mitigation, broadband polarisation conversion, and other desired tasks compatible with the DBBC3 system.

As mentioned above the first version of the firmware for the digital frontend will be to send 4 GHz bands to the DBBC3, which requires the so-called CORE3H2 configuration of the CORE3 boards. The CORE3H2 makes use of all eight transceivers on-board in receiving mode. This architecture allows one to receive 4 GHz bands with 8-bit representation, which is similar to feeding a CORE3H using the standard ADB3L sampler boards as in standard DBBC3s.

It is worth noting that if required, there could be full compatibility with a standard DBBC3 equipped with ADB3L sampler boards to be compatible with traditional receivers whose analogue signal is sampled in the backend. Indeed switching between input data to the CORE3H boards coming from the local ADB3L or

Fig. 3: The FPGA processing board CORE3H can be populated with up to eight optical transceivers. They can work as output (standard DBBC3 VDIF streams for recording) and as input to the FPGA (application for "digital" receivers.

via the digital frontend could be implemented by using different firmware.

Another architecture could also be chosen when additional functionality is required. This is for example the case for the digital linear to circular polarisation in FPGA. The conversion is required for the BRAND receiver, which is linearly polarised, to work with circularly-polarised VLBI networks. The conversion can be performed in analogue with a hybrid junction after the feed, or in the digital domain with a Hilbert transform in FPGA to give accurate 90 degree phase shift over a wide fractional bandwidth. The additional FPGA resources for performing this process in the CORE3H are not available due to the great demands of the main function of down conversion and packet forming. A clean solution can be provided by replacing a number (or all) the ADB3L with additional standard CORE3H processing boards, if required. Indeed CORE3H boards can be connected in functional sequence through their optical transceivers. The flexibility of the DBBC3 allows one to configure the system blocks in diverse ways to satisfy the changing and highly demanding requirements.

3 Conclusions and outlook

We have shown in this article that the DBBC3 is a very versatile backend. The development to adapt it to the
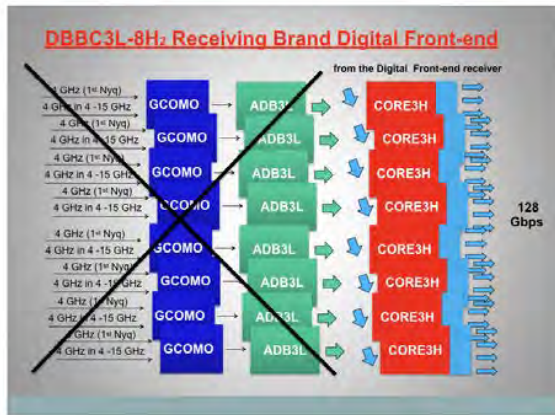
Fig. 4: The block diagram shows a DBBC3 whose analogue and sampling parts are by-passed by digital signals from the BRAND (or other) digital frontend.

BRAND digital receiver opens a cost-effective path to handle the data flood which the BRAND receiver will produce.

At the same time the BRAND digitiser/processor unit in or close to the receiver box together with the modified DBBC3 backend can be adapted efficiently to other receivers with large bandwidths. One immediate application will be the triple-band receiver for the high frequencies 22 GHz, 43 GHz, and 86 GHz. Rather than renewing the limited IF cabling of, for instance, the Effelsberg antenna we are planning to sample as much bandwidth as possible close to the triple-band receiver with the BRAND sampler/processing unit and transport the IF as digital on fibre, which is much easier. We use one or two DBBC3s to form channels (sub-bands) suitable for VLBI correlation. Assuming 8 GHz bandwidth per polarisation and receiver, we could see data rates of up to 192 Gbps on output.

It should also be noted that the control of the DBBC3 in this new mode via the Field System[1] will be an extension of the existing implementation, which should be cost effective to realise.

References

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[1] See for instance http://www.metsahovi.fi/pub/evn-om/4fs-4.html