

# Highly-efficient grating couplers based on transfer-printing technology

Fabio Pavanello<sup>1,2</sup>, Grigorij Muliuk<sup>1,2</sup>, Gunther Roelkens<sup>1,2</sup>

<sup>1</sup>Ghent University - imec, Technologiepark 15, 9052 Ghent, Belgium

<sup>2</sup>Center for Nano- and Biophotonics, Ghent University, Belgium

e-mail: fabio.pavanello@ugent.be

## ABSTRACT

We propose a new approach that allows highly efficient fiber-to-chip coupling using transfer-printing technology. The novelty of the approach relies on the integration of a mirror between a top (source) grating coupler circuit and a bottom (target) photonic integrated circuit (PIC) and on a wide directional coupler to transfer the light between the two waveguide layers before tapering the waveguide to single mode widths. We propose an apodized, partially etched, grating coupler integrated with a directional coupler implemented in amorphous Si, while a crystalline 220nm Silicon-on-Insulator (SOI) platform is used for the target PIC. We achieve a simulated 2D coupling efficiency of 96.2% (-0.17 dB) with a 1 dB bandwidth of 45 nm. The bandwidth takes into account the broadband directional coupler, which is very compact. The alignment tolerance along the direction orthogonal to the light propagation is better than  $\pm 2 \mu\text{m}$  to achieve an insertion loss penalty lower than 1 dB, which is well within reach with transfer printing.

**Keywords:** Silicon photonics, grating couplers, transfer-printing technology.

## 1 INTRODUCTION

Transfer-printing is an emerging technology which allows to heterogeneously integrate photonic integrated circuits and devices (PICs) that are fabricated separately e.g. on a Silicon-on-Insulator (SOI) platform and on a III-V platform. The technique allows for high throughput assembly because of the parallel nature of the printing process (large arrays of devices can be assembled in a single printing cycle, compared to flip-chip integration where a single device is assembled at a time). Also the device size can be extremely small, down to a few micron a side. [1]. This integration technique provides a clear path towards resolving some of the major problems of current silicon photonic platforms, which do not offer suitable materials as gain medium and where III-V modulators and photodetectors may achieve higher performance compared to their silicon counterparts for particular applications. Another key challenge for photonic integrated circuits is the high efficiency and robust fiber-to-chip light coupling. In particular, grating couplers allow to achieve vertical coupling on a compact footprint, contrary to approaches based e.g. on spot-size converters [2]. Here, we propose a novel fiber-to-chip grating coupler approach based on transfer-printing technology, which consists of depositing an Au patch acting as a mirror onto the target PIC before printing the source grating coupler + directional coupler. By achieving the transfer of light from the top grating coupler to the target PIC using a very wide directional coupler prior to the tapering of the waveguide to single mode widths, it is possible to print grating structures with very compact footprint and with very high alignment tolerance, thus providing a concrete path towards high-throughput, robust and high-efficiency I/O ports patterned on a single source wafer and transferred in a single printing operation.

## 2 DESIGN AND PERFORMANCE

### 2.1 Target and source PIC specifications

The target PIC is based on a 220 nm SOI platform with a 70 nm partial etching step (see Fig. 1(a)). A 100/50 nm thick SiO<sub>2</sub>/BCB bi-layer is present to promote the adhesion with the printed grating coupler structure. The reason of having a dielectric bi-layer is to reduce the thickness variations associated with the BCB layer (used as a bonding agent) during processing, while at the same time providing planarization and encapsulation for the rib waveguides. The cross-section of the grating structure on the source wafer is based on a custom SOI platform with a 265 nm thick a-Si layer deposited on a 150 nm thick SiO<sub>2</sub> layer. The latter is deposited on a bulk Si substrate which will be underetched in the transfer printing process flow, when the a-Si device coupons are released from their substrate. The thicknesses of the a-Si layer and of the bottom SiO<sub>2</sub> layer on the source wafer are determined by design as explained below. Another 150 nm thick SiO<sub>2</sub> layer is then deposited above the a-Si layer to have a symmetrical structure to balance the stress which will prevent the released structure from buckling. After the printing a 850 nm thick polymer with the same refractive index as SiO<sub>2</sub> is deposited for planarization. A 70 nm thick Au mirror is deposited after partially etching a recess in the target PIC (see Fig. 1(b)). This section defines where the grating coupler will be printed.

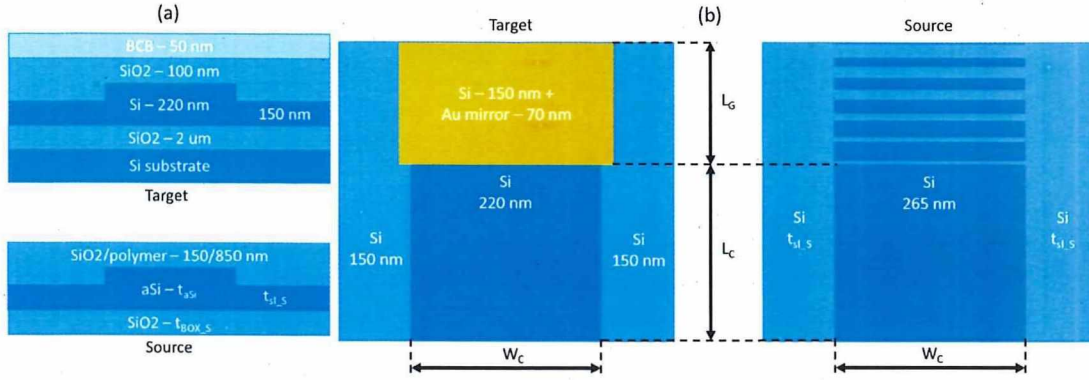


Figure 1. Target and source waveguide cross-sections and top views. (a) Cross-sections of the target and source structures. Parameters  $t_{aSi}$ ,  $t_{si,S}$  and  $t_{BOX,S}$  are determined by design. (b) Top view of the target and source structures. The PICs will be vertically stacked through transfer printing achieving an abrupt interface at the end of the coupler on the grating coupler structure, while the target PIC waveguide will continue with a taper to single mode waveguide.

## 2.2 Grating coupler and directional coupler designs

The thickness  $t_{aSi}$  of the a-Si layer ( $n = 3.35$  at  $1550$  nm from measurements) is determined by simulating the supermodes' effective index dispersion as a function of the thickness ( $t_{aSi}$ ) and by selecting the thickness  $t_{aSi} = 265$  nm at which anti-crossing appears (initial separation between waveguides of  $400$  nm). This results in phase matching between the a-Si and c-Si waveguide. Afterwards, the vertical separation of the two waveguides is determined by aiming at approximately  $20$   $\mu\text{m}$  coupling length  $L_C$  for compactness. This leads to a total separation of  $300$  nm and a  $\text{SiO}_2$  BOX thickness for the source structure  $t_{BOX,S}$  of  $150$  nm. This value is used as initial input in the grating simulation. The coupling width  $W_C = 13.5$   $\mu\text{m}$  is kept equal to the grating width to achieve optimal mode matching with the  $10.4$   $\mu\text{m}$  mode field diameter of the gaussian beam of the fiber without introducing any tapering on the source structure. The 2D grating simulation is performed in Lumerical FDTD launching the mode into the waveguide  $10$   $\mu\text{m}$  away from the first tooth and recording the scattered field at the top surface of the source PIC ( $1$   $\mu\text{m}$  above the top a-Si waveguide) as done in [2] assuming angled cleaved fibers and a  $\text{SiO}_2$  index matched environment. The electric field recorded is multiplied by the analytically computed magnetic field of the fiber mode and integrated along the direction of propagation to extract the coupling efficiency after power normalization [2]. The grating apodization for mode matching of the scattered field with the fiber mode field is based on the methodology introduced in [3] where a linear coefficient  $FF_{lin}$  is applied for the fill factor, which is tailored along the propagation direction taking into account local corrections of the grating period according to the grating formula  $k_0 \sin(\theta) = k_0 n_{eff}^G - K$  where  $k_0$  is the vacuum wavevector,  $\theta$  the fiber angle,  $K$  is the reciprocal lattice vector and  $n_{eff}^G = FF n_{eff}^{thick} + (1 - FF) n_{eff}^{thin}$  is the grating effective index with  $n_{eff}^{thick}$  and  $n_{eff}^{thin}$  the effective indices for full and partial thickness waveguides, respectively. A  $20$

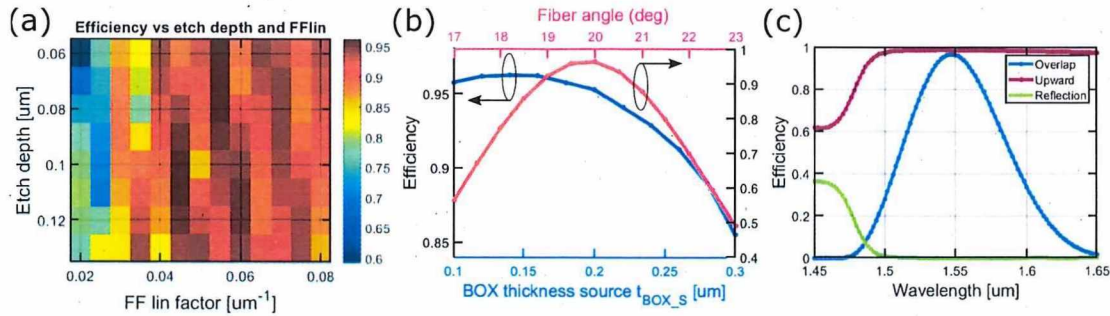


Figure 2. Performance of the grating coupler. (a) Sweep of the linear fill factor  $FF_{lin}$  and of the etch depth. (b) Sweep of the BOX thickness  $t_{BOX,S}$  on the grating coupler source wafer using the optimal values found in (a). The angle is swept to find the optimum by using the optimal value of  $t_{BOX,S}$ . (c) The grating response versus wavelength. Only a small mismatch of approximately 2.5% is present compared to the upward radiation at  $1550$  nm.

deg angle has been chosen because it provided the highest scattered power (without Gaussian overlap) for the choice of thickness  $t_{BOX,S}$  of  $150$  nm using an initial guess for the linear fill factor ( $0.05$   $\mu\text{m}^{-1}$ ) and the etch depth ( $100$  nm) in order to sweep multiple designs at their respective angles. The grating is composed of 25 periods. The design flow consists first of sweeping the linear fill factor coefficient and the etch depth of the grating (see Fig. 2(a)). This allows to find the optimum linear fill factor  $FF_{lin} = 0.045$   $\mu\text{m}^{-1}$  and the optimal

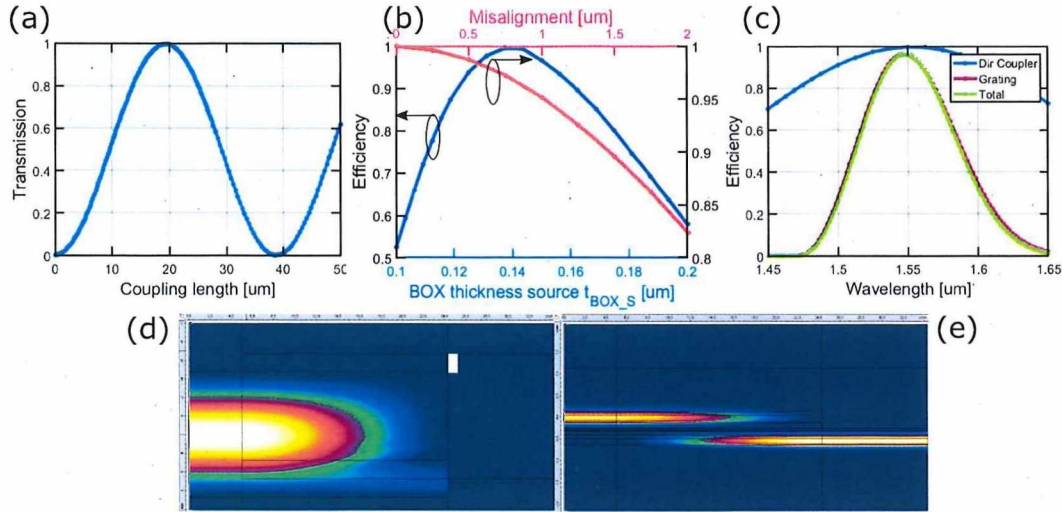


Figure 3. Performance of the directional coupler. (a) Transmission versus coupling length. (b) Efficiency as a function of the misalignment and variation of BOX thickness. (c) The directional coupler response versus wavelength. The grating coupler response has been added as well in order to compute the total bandwidth of the device which is dominated by the grating coupler. (d) shows a top-view of the simulation with 2  $\mu\text{m}$  of misalignment, indicated by the white bar. (e) shows a cross-section of the same simulation.

etch depth,  $t_{sl\_S} = 165$  nm. A fine sweep of the BOX thickness  $t_{BOX\_S}$  allows to optimize the interference upward leading to a value of 140 nm as in Fig. 2(b). The last sweep is on the fiber angle, where we keep the optimal design fixed varying the angle. This leads to an optimal angle of 20 deg as in design and to a simulated efficiency of 96.2% (-0.17 dB) shown in Fig. 2(c). The total power radiated upward is close to 99%. The difference is due to the imperfect overlap with the gaussian mode. The reflection reaches -27 dB around the central wavelength thanks to the apodization and the small etch step. The total length of the grating section is 18.4  $\mu\text{m}$ .

The optimal value for the BOX thickness  $t_{BOX\_S}$  of the source PIC and the optimal etch depth are used in the final simulation of the directional coupler to simulate the correct coupling length. The simulation carried out using fimmwave is based on 3 sections: the input section based on the cross-section of the waveguide structure on the source wafer Fig. 1(a), the coupling section that corresponds to the stack of source and target structures and the output section based on the target PIC. A nearly lossless power transfer (see Fig. 3(a)) can be achieved with a length of 19.3  $\mu\text{m}$  where the reflection is negligible because of the large separation between the waveguides. Fig. 3(b) shows the response of the directional coupler to tolerances such as lateral misalignment (source PIC and target PIC are misaligned orthogonal to the propagation direction) and variation of BOX thickness  $t_{BOX\_S}$  (or of BCB thickness because of their similar refractive indices). It is possible to achieve better than 1 dB of insertion loss with a misalignment as large as  $\pm 2$   $\mu\text{m}$  thanks to the wide waveguides. The broadband behavior allows to achieve a directional coupler 1dB bandwidth of 144 nm, while the overall 1dB bandwidth of the grating coupler + directional coupler is 45 nm, dominated by the grating coupler response as shown in Fig. 3(c). Figs. 3(d)-(e) show the top view and the cross-section of a simulation with misalignment of 2  $\mu\text{m}$  where it is possible to observe the effect of the presence of a misalignment on the optical mode distortion.

### 3 CONCLUSIONS

The proposed approach paves the way for efficient, compact and robust fiber-to-chip coupling using transfer-printing technology allowing to easily integrate multiple I/O ports onto a PIC. The compactness of the coupler allows also to reduce the costs of the source structure, which may be fabricated using e.g. e-beam, immersion lithography or extreme UV lithography for the best performance.

### REFERENCES

- [1] A. De Groote, P. Cardile, A. Z. Subramanian, A. M. Fecioru, C. Bower, D. Delbeke, et al., "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters," *Opt. Exp.*, vol. 24, pp. 13754–13762, 2016.
- [2] D. Taillaert, P. Bientman and R. Baets, "Compact efficient broadband grating coupler for silicon-on-insulator waveguides," *Opt. Lett.* vol. 29, pp. 2749–2751, 2004.
- [3] R. Marchetti, C. Lacava, A. Khokhar, X. Chen, I. Cristiani, D. J. Richardson, et al., "High-efficiency grating-couplers: Demonstration of a new design strategy," *Scientific Reports*, vol. 7, pp. 1–8, 2017.