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Catarina Alexandra Xavier Belchior

Amplificador de Potência para Sistemas 5G

Power Amplifier for 5G Systems

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor Pedro Miguel da Silva Cabral, Professor auxiliar do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro, e do Doutor Luís Carlos Cótimos Nunes, Investigador do Instituto de Telecomunicações.

o júri / the jury

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Prof. Dr. António José Nunes Navarro Rodrigues
Professor auxiliar da Universidade de Aveiro

vogais / examiners committee

Dr. Francesc Purroy Martin
Power Amplifiers Team Leader, Huawei Technologies, Sweden AB

Prof. Dr. Pedro Miguel da Silva Cabral
Professor auxiliar da Universidade de Aveiro

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Palavras Chave

Amplificadores de Potência, Banda X, Eficiência, Largura de Banda, Nitreto de Gálio, Rádio-Frequência, Transístor, 5G.

Resumo

Nos últimos anos, os sitemas 5G têm estado em destaque e a forma como os seus requisitos irão mudar a vida da sociedade está a tornar-se ainda mais relevante. O facto de um desses requisitos ser providenciar os utilizadores com centenas de MHz de largura de banda, juntamente com um espetro escasso e lotado abaixo dos 3GHz, levou a um aumento da frequência de operação. Seguindo esta ideia, esta dissertação tem como objetivo projetar, implementar e testar um amplificador de potência para sistemas 5G, em particular para a banda X (8-12GHz).

Nesta banda de frequências, o comportamento dos componentes de RF (condensadores) e outras estruturas (vias, substrato e conetores) têm de ser cuidadosamente analisados de modo a entender como é que estes elementos podem afetar o desempenho geral dos circuitos. Com esse propósito, vários circuitos de teste foram projetados, implementados, e de seguida, os resultados simulados e medidos foram comparados. Este passo inicial no trabalho prático permitiu fazer algumas atualizações no processo de simulação e tirar outras conclusões úteis. Posteriormente, um amplificador de potência para a banda X foi concebido.

Para atingir o objetivo final, foram projetados vários protótipos intermédios de modo a tornar possível a identificação e correção de potenciais fontes de erro, como por exemplo nas malhas de adaptação e no modelo do transístor. No final foi possível projetar e implementar um amplificador de potência para a banda de frequências de 9 a 9.6GHz, ou seja, com 600MHz de largura de banda. A eficiência de dreno máxima alcançada foi de 41-55% com um ganho entre 6-12dB. Estes resultados demonstraram-se competitivos com o estado-da-arte atual.

Todo o projeto e simulação foram realizados usando o *software Advanced Design System 2019* e *Momentum* da *Keysight Technologies*.

Keywords

Bandwidth, Efficiency, Gallium Nitride, Power Amplifiers, Radio-Frequency, Transistors, X band, 5G.

Abstract

In recent years, 5G systems have been in the spotlight and the discussion of how its requirements will change people's lives is becoming increasingly more relevant. The fact that one of these requirements is to provide users with hundreds of MHz of available bandwidth, coupled with a scarce and crowded spectrum below 3GHz, has led to an increase in the operating frequency. Following this idea, this dissertation has the objective to design, implement and test a power amplifier for 5G systems, specifically for frequencies in the X band (8-12GHz).

In this frequency band, the behaviour of RF components (capacitors) and other structures (via hole, substrate and connectors) have to be carefully analysed in order to better understand how these elements can affect the overall performance of the circuits. For this purpose several test circuits were designed, implemented and then, the simulated and measured results were compared. This initial step on the practical work allowed to make some updates on the simulation process and to draw other useful conclusions. After that, the design of a power amplifier for the X band was conceived.

In order to reach the final objective, several intermediate prototypes were designed to make possible the identification and correction of potential error sources, for example in the matching networks and in the transistor model. In the end, a power amplifier for the frequency band of 9 to 9.6GHz, which means, 600MHz of bandwidth, was designed and implemented. The maximum drain efficiency achieved was 41-55% with a gain between 6-12dB. These results have proved to be competitive with the actual state-of-the-art. All design and simulation were performed using the Advanced Design System 2019 and *Momentum* software from Keysight Technologies.

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List of Acronyms

4G Fourth Generation Mobile Communication System

5G Fifth Generation Mobile Communication System

ACPR Adjacent Channel Power Ratio

ADS Advanced Design System

AI Air Interface

CW Continuous Wave

DAC Data Access Component

DFN Dual-Flat-no-Lead

DhPA Doherty Power Amplifier

DUT Device Under Test

EER Envelope Elimination and Restoration

EHF Extremely High Frequency

ET Envelope Tracking

EM Electromagnetic

FET Field-Effect Transistor

FoM Figures of Merit

GaN Gallium Nitride

HB Harmonic Balance

HEMT High Electron Mobility Transistor

IMD Intermodulation Distortion

IMN Input Matching Network

IMR Intermodulation Ratio

IP3 Third-order Intercept Point

ISO International Organization for Standardization

ITU International Telecommunication Union

LTE Long Term Evolution

MN Matching Network

OMN Output Matching Network

OPBO Output Power Back Off

PA Power Amplifier

PAE Power Added Efficiency

PAPR Peak Average Power Ratio

PCB Printed Circuit Board

Pout Output Power

RF Radio Frequency

SCS Signal Component Separator

SHF Super High Frequency

UMTS Universal Mobile Telecommunications System

VNA Vector Network Analyser

Chapter 1

Introduction

1.1 Motivation and Context

Ever since its birth, mobile communications have been undergoing more than three decades of explosive growth, and the mobile network has become a basic information network connecting human society. It not only profoundly changes the lifestyle of everybody, but also greatly promotes the advancement of society and economy.

The 2010s decade brought a massive expansion of wireless devices and it seems that this tendency is in accelerated growth, mainly due to the massification of smartphones, tablets and video streaming. These facts are expected to push the limitations of the current LTE-based 4G and, for this reason, both the scientific community and industry have been working on the development of a new generation of communication systems: the fifth generation of mobile communications, 5G [1].

Accordingly with International Telecommunication Union (ITU) 5G mobile network services can be classified into three categories [2]:

- **Enhanced Mobile Broadband (eMBB):** requiring hundreds of MHz of channel bandwidth in order to meet the people's demand for an increasingly digital lifestyle;
- **Ultra-reliable and Low-latency Communications (uRLLC):** aims to meet expectations for real-time connections enabling for example autonomous vehicles;
- **Massive Machine Type Communications (mMTC):** aims to focus on services that include high requirements for connection density (such as smart cities).

These services require higher traffic volume (indoor or hotspot traffic) and, spectrum, energy, and cost efficiency. Furthermore, and compared with 4G, 5G needs to support more various scenarios, integrate with other wireless access technologies, and fully utilize both low frequency and high frequency bands [3]. In the following figure it is represented a comparison of the performance characteristics and technical specifications (specifically: latency, data traffic, peak data rates, connection density and available spectrum) of 4G and 5G technology.

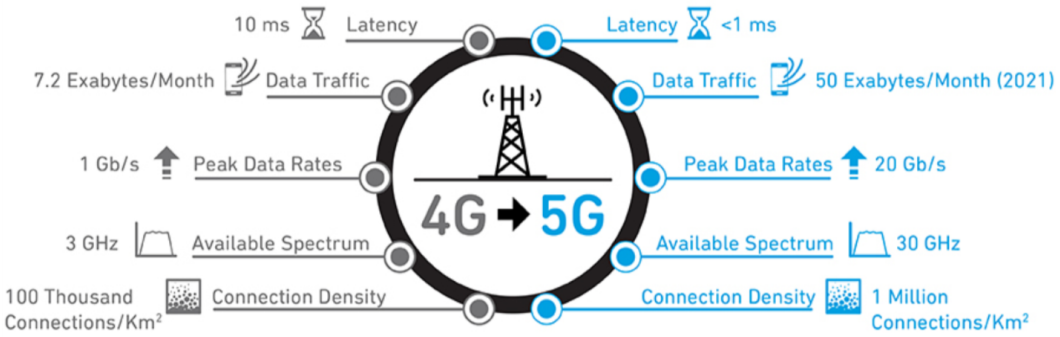


Figure 1.1: Comparison of the performance characteristics and technical specifications of 4G and 5G technology [4].

Considering 5G requirements and technology trends, 5G needs a brand new air interface (AI) to break the restriction of backward compatibility and make full use of various advanced technologies. The new air interface has two branches: low frequency and high frequency new AIs.

According to global spectrum planning and propagation characteristics on different frequency bands, 5G should include a low frequency new air interface working below 6GHz and high frequency new air interface working above 6GHz [5].

A low frequency new air interface of 5G is required to meet the demands of user experiences and massive connections in wide-coverage and high-mobility scenarios. A high frequency new air interface is needed to achieve ultra-high data rates and system capacity by utilizing abundant high frequency resources. In this case, it is necessary to consider the impacts of high frequency channel characteristics and radio frequency (RF) components.

It is believed that 5G will use the centimeter and millimeter wave band. The centimeter wave band (wavelength range from 1-10 cm), also called super high frequency (SHF), refers to the frequency range from 3GHz to 30GHz. The 30-300 GHz spectrum is known as millimeter wave band (wavelength range from 1-10 mm) or extremely high frequency (EHF).

The fact that the current cellular system, below 3GHz, has already a very crowded and scarce spectrum is the main motivation to use the cmWave and mmWave frequencies in future 5G networks. In this spectrum range (3-300 GHz), the amount of bandwidth available is enormous while compared to 4G and previous wireless network technologies. Besides that, another advantage is that the physical size of antennas at cmWave and mmWave can be so small that it becomes practical to build complex antenna arrays and/or further integrate them on chips or PCBs.

In this context, and since 5G specifications aim to provide users with hundreds of MHz of available bandwidth, increasing the central frequency of operation of power amplifiers (PAs) has become a necessity.

In 4G the frequencies do not surpass 6 GHz, but in 5G reaching frequencies close to 100 GHz is under consideration. Yet, the backbone of telecommunications is not expected to be above 10 GHz. For this reason, and since the purpose of this work is to implement a PA for 5G, the chosen operating frequency will be in the X band. Figure 1.2 illustrates the frequency spectrum from 300MHz to 300GHz, where it is possible to see the corresponding frequency bands.

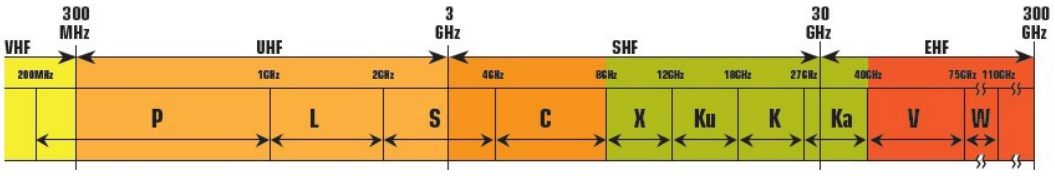


Figure 1.2: Frequency spectrum from 300MHz to 300GHz [6].

In wireless communication systems, PA is the main source of spectrum and energy inefficiencies. In fact, the power consumption of the RF part accounts for 80% of the overall power consumption and that of a PA accounts for 80% of the RF part [7]. With these high numbers, improve PAs efficiency is an objective, to consequently, reduce energy consumption. In the end, this will determine the number of users covered, the battery life and the available services that can be provided given a specific quality of service, with a certain cost of deployment and maintenance.

1.2 Objectives

The main purpose of this dissertation is the design, implementation and test of a power amplifier for 5G systems. That said, this is an ambiguous objective since 5G spectrum is enormous (frequencies above 6GHz), thus it is necessary to define specific targets in terms of frequency.

This work intends to be an intermediate step for the design of amplifiers between low frequencies (<6GHz) and higher frequencies (from Ku band). Thereby, the objective of this work is the design (using ADS), implementation and experimental validation of a power amplifier for the X band, more specifically between 9 and 10GHz with at least 5% of fractional bandwidth, and giving special importance to the efficiency performance, so that the PA can be highly competitive with the actual state-of-the-art. To evaluate this possibility, a number of secondary objectives should be accomplished.

Firstly, the theoretical concepts of microwave power amplifiers need to be studied and well understood. Secondly, it is necessary to understand how passive elements behave at the considered frequencies and what implications they may cause in the circuits. Thirdly, it is essential to gain expertise on the details of the appropriate design techniques of RF power amplifiers circuits, that lead us from the amplifier design goals to the implemented circuit. Finally, it is also desired to learn and gain experience on establishing setups in the laboratory and to properly handle the available RF instrumentation, in order to accurately and efficiently characterize an amplifier. By achieving these secondary goals, a proof of concept amplifier can be developed and tested.

1.3 Structure

In Chapter 1, the motivation, context, and objectives are identified and explained. Moreover, the structure of this dissertation is also clarified.

Chapter 2 aims to expose the studied theory of RF power amplifiers. This chapter is divided into two major sections: theory and figures of merit. In the first section amplifiers operation classes, design techniques, and also, methods of calibration are discussed. Finally, a brief analysis of efficiency techniques' state of the art is also made. In the second section, the figures of merit that allow to quantitatively characterize a power amplifier performance are studied. Here, concepts of linearity, non-linearity, gain, stability and efficiency are exposed.

Chapter 3 has the purpose of characterize and understand how passive elements behave at high frequencies.

Chapter 4 is dedicated to the PA development, from its design to its experimental validation. This can be considered as the main practical chapter, since all the designing, simulation, measurements and analysis of amplifiers are herein described.

Chapter 5, the final chapter, makes a brief summary of the work developed in this dissertation with the purpose to: verify if the defined goals were fulfilled; expose how well the developed amplifier compares with the other state-of-the-art examples; and identify its flaws. Furthermore, this chapter also includes some suggestions for future work.

Chapter 2

RF Power Amplifiers

Signal amplification is one of the most basic and prevalent circuit functions in modern RF and microwave systems [8]. The purpose of a power amplifier in a communications system is to increase the power of the carrier signal to be transmitted. The signal needs an adequate level of power to overcome the adversities of the media and allow the receiver(s) to capture the information at a certain distance, with a certain level of quality. Due to the difficulty in handling high power signals, the amplification is performed in most of the cases, just before propagation. As a result, the PA is usually one of the final devices in the communications systems overall architecture.

As represented in the next figure, an amplifier is a device designed to convert power from a DC power source into signal energy.

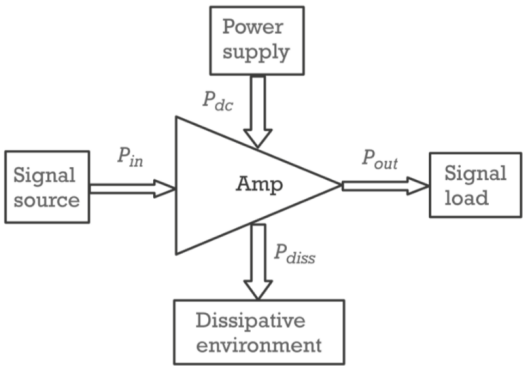


Figure 2.1: Power balance of a PA [9].

The main challenge in designing a PA is to achieve high efficiency, bandwidth and gain, while preserving linearity. These properties are given as requirements in most of the modern systems and imply a trade-off between them since the improvement of any parameter usually results in a degradation in others.

In this chapter the main concepts, techniques and figures of merit related to the characterization of PAs are discussed.

2.1 Theory

2.1.1 Classes of Operation

RF power amplifiers can be separated in classes, typically, A to F, where each letter gives a broad indication of an amplifier's characteristics and performance, since these classes differ in the method of operation, efficiency, and power output capability [10]. The methods of operation can be divided into two terms: switch-mode and transconductance-mode.

When a transistor operates as a switch, which is associated to classes D, E and F, the voltage and current waveforms can, in principle, be tailored so that they do not overlap, reducing (theoretically) the device dissipation to zero [11]. In this operation mode, the active device operates between the on and off state, as illustrated in the I-V curves in figure 2.2 [12]. In an ideal case, these two states can be represented by impedances of zero and infinity, respectively, and consequently, either the voltage across the switch or the current through the switch are zero, resulting in zero switching power in both stages. The reason to use the transistors as switches is to achieve high efficiency amplifier. However, switch-mode amplifiers are hard to model at GHz frequencies because the device does not sweep through its linear region fast enough to behave like a switch [13], (due to the difficulty of controlling the harmonics), thence classes D, E and F will not be studied in this dissertation.

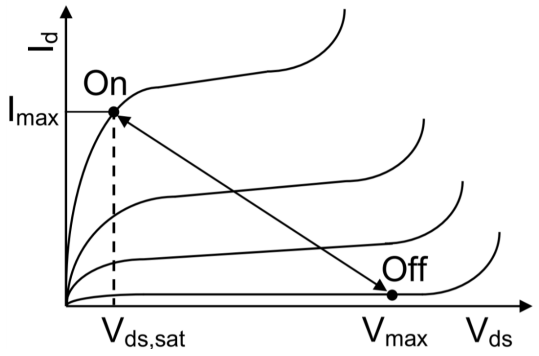


Figure 2.2: Switch states of transistor [12].

The transconductance based amplifiers are identified also as class A, AB, B to C considering the quiescent active device bias points. This mode of operation is based on manipulation of the output current waveform of the active device, in order to explore different compromises between linearity, efficiency and maximum output power [14]. When operating as a current source, the transistor conducts continuously, so there is overlap of the current and voltage. This situation limits efficiency because it results in dissipated power.

Figure 2.3 shows a generic circuit schematic where, depending on the value of V_{GS}, classes A, AB, B or C will be present.

The transistor is biased with two DC sources through an RF choke and thus the conduction angle is defined. The LC tank circuit at the output, resonant at the fundamental frequency, will short circuit the harmonics, only allowing the fundamental component to reach the load.

With I_{dq} and I_{dp} as the quiescent bias current and the RF current amplitude, respectively, a linear amplifier has a sinusoidal drain current given by:

$$I_d = I_{dq} + I_{dp}cos(\omega_0 t) \tag{2.1}$$

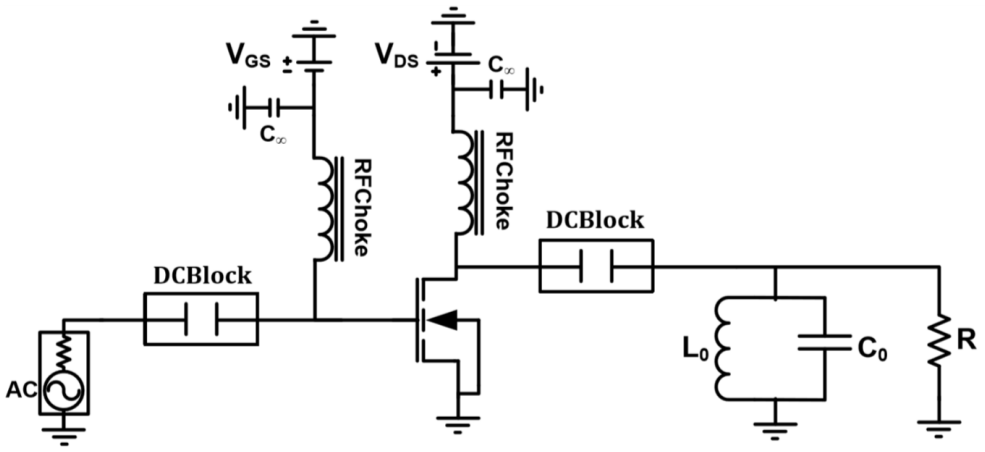


Figure 2.3: Generic schematic for A, B, AB or C classes.

The portion of time that the device spends in its active region is influenced by the applied bias. Accordingly, it is possible to define a conductance angle. If the full, the half or less than the half of the signal period is amplified, the conductance angles are 2π (class A), π (class B) or less than π (class C), respectively. Class AB has a conductance angle between π and 2π. In figure 2.4, the corresponding bias points are depicted.

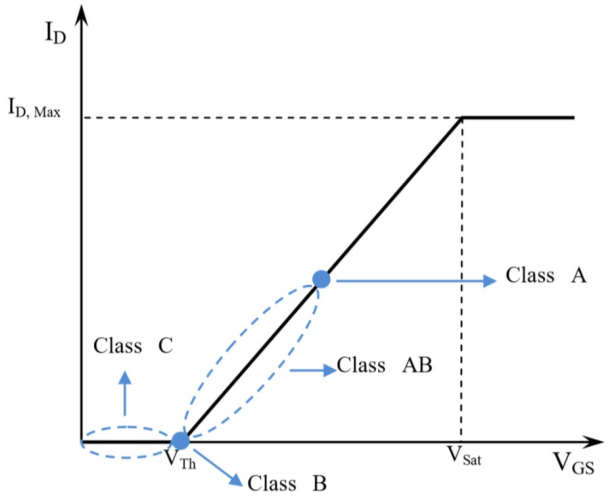


Figure 2.4: Polarization regions of operation classes, in the transistor I-V characteristic curve.

Based on the drain current, the DC and harmonic currents can be calculated by Fourier analysis yielding:

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} I_d(\theta)d\theta \tag{2.2}$$

and

$$I_{Ln} = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} I_d(\theta)cos(n\theta)d\theta \tag{2.3}$$

where I_{Ln} represents the magnitude of the n^{th} harmonic load current and $\theta = \omega$t.

Equations 2.2 and 2.3 are the base for harmonic and DC-power, efficiency and linearity calculations.

It is possible to express output power, DC power and efficiency of a PA as a function of the conduction angle (2θ). The maximum output power at the fundamental frequency is given by

$$P_{out} = \frac{1}{2} Re[V_1 I_1^*] = \frac{1}{2} V_{dc} \frac{I_{max}}{2\pi} \frac{2\theta - sin(2\theta)}{1 - cos\theta} \tag{2.4}$$

where V_1 and I_1 are the amplitudes of the fundamental components of voltage and current, respectively, and V_{dc} is the amplitude of the source voltage. It is assumed that saturation voltage is relatively small, and therefore V_1 is determined by V_{dc}.

DC power is given by the following expression:

$$P_{dc} = V_{dc} I_{dc} = V_{dc} \frac{I_{max}}{\pi} \frac{sin\theta - \theta cos\theta}{1 - cos\theta} \tag{2.5}$$

As we shall see further on, efficiency is expressed by:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.6}$$

which leads to a maximum efficiency of:

$$\eta_{max} = \frac{2\theta - sin(2\theta)}{4(sin\theta - \theta cos\theta)} \tag{2.7}$$

Class A

A class A RF power amplifier is theoretically a linear amplifier. A linear amplifier is supposed to produce an amplified replica of the input voltage or current waveform [15]. This class is the one that generates less harmonic components and for this reason, it is also the one that exhibits less distortion. This class of PAs have a conduction angle of 2π, which means the transistor is biased in conduction, and, therefore, consuming power even when no signal is being amplified. The maximum efficiency for a sinusoidal signal is 50%, which is rather low.

Class B

The gate in a class B PA is set at the threshold of conduction so the transistor is active half of the time and the drain current is half-sinusoidal [16]. As we could verify through equation 2.4, classes A and B have the same maximum output power, but class B presents a higher efficiency (maximum of 78.5%). This happens because of the reduction of the bias current, which results in lower DC current. No DC current is drawn in class B as long as there is no RF input signal. Consequently, the degradation of the efficiency at low signal amplitudes is not as significant as for the class A amplifier and, also, the energy dissipation and the heating are reduced. However, these benefits come together with drawbacks. Since one half of the signal is cut, strong undesired harmonics are generated and, when compared to a class A amplifier, class B requires twice the amount of the voltage swing at the gate of the transistor. In other words, the gain of a class B amplifier is only half of the gain of a class A [17].

Class AB

As its name suggests, the class AB amplifier has its properties between class A and B, yielding a good trade-off between efficiency and linearity. It has a higher efficiency and lower small-signal gain than class A and higher small-gain and lower efficiency than class B. As stated above, this class has a conductance angle between π and 2π.

Class C

A class C device is biased below the pinch-off level so that it conducts less than 50% of the time. The conduction angle is less than π resulting in higher efficiency when compared to other classes discussed so far. Although it is possible to increase the efficiency up to a theoretical limit of 100%, it is important to note that, in opposition, the output power and the gain decrease and the level of excitation required increases. Furthermore, this class is also considered the most non-linear one.

2.1.2 PA Characterization

IV Curves of the Transistor

As its name suggests, IV Characteristic Curves exhibit the relationship between the current flowing through a device and the applied voltage across its terminals. The I-V curves can be seen as a *pitch* where the limits dictate the boundaries for the microwave signal, as portrayed in figure 2.5. The boundaries are represented by the V_k (knee voltage), V_{BR} (breakdown voltage), zero and maximum current. If these limits are hit, the signal gets clipped and consequently compression and non-linear distortion appears.

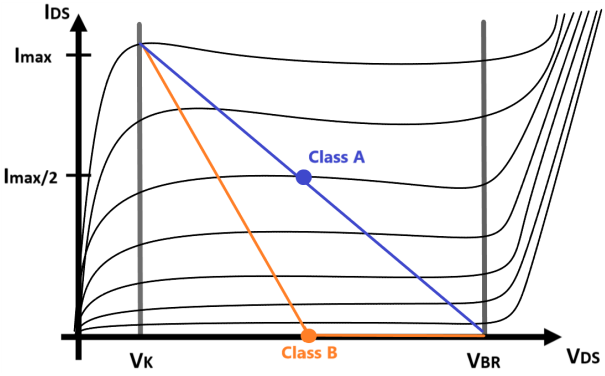


Figure 2.5: IV curves of a transistor with bias points and load-lines for classes A and B.

In figure 2.5 it can be observed the load-lines and the nominal bias points for classes A and B. As stated in the previous section, the location of the bias points defines the portion of time that the device is in the active region and hence the current (I_{DS}) waveform. The blue and orange lines indicate possible load-lines which an AC signal could swing back and forth. Class A has a bias point of $(V_{DC}, I_{DC}) = (\frac{V_{BR}+V_k}{2}, \frac{I_{max}}{2})$, and so, ideally, the blue load-line allows the maximum use of the I-V field and, therefore, allow the microwave signal to make use of the maximum current and voltage swing. However, it is recommended to give a certain margin for reliability of the design: the nominal bias voltage should be less than half of the breakdown voltage [18].

An important fact to notice in the figure above is that the several I-V curves observed are associated to different values of V_{GS}. The space between them is related to the transconductance, $g_m \approx \frac{\Delta I_{DS}}{\Delta V_{GS}}$, which in turn is related to the gain. It can be seen that near to the class B bias point, the curves are more closely spaced than in class A region, which means lower gain.

To optimize output power, which means to maximize current/voltage peaks before clipping, the load resistance must be reciprocal of the load-line slope. As declared previously, the maximum output power, for both load-lines, can be calculated through:

$$P_{out} = \frac{1}{2} Re[V_1 I_1^*] = \frac{1}{8} \Delta V \Delta I \tag{2.8}$$

where Δ V and Δ I corresponds to the voltage and current swings, respectively.

The previous equation can be also expressed as:

$$P_{out} = \frac{1}{8} R_{opt} \Delta I^2 \tag{2.9}$$

where R_{opt} is the optimum load to achieve maximum output power. Thus, $R_{opt} = \frac{\Delta V}{\Delta I} = -\frac{1}{m}$, being m the slope of the load-line.

In the next section a technique to select the optimum load, according to the design goals, is explained. Note that this could mean a selection of a load that maximizes gain, efficiency, or other parameter, and therefore, not improving specifically the output power.

Load-Pull Technique

The traditional load-pull system is a passive technique that uses two mechanical tuners: one to vary the gate (input) impedance and another to vary the drain (output) impedance for a common device under test (DUT), while accessing its performance parameters [19]. This technique came up due to the impossibility to access the intrinsic drain and sometimes, to the model, therefore, load-pull, allow from a practical point of view, to determine impedances. In this way, it is possible to present *a priori* a known impedance to a DUT in a precise fashion, to extract its optimal performance and thus associate conditions to deliver that performance in a network.

Nowadays, it is possible to perform, in a simulator, *virtual* load-pull measurements and then select a specific target in order to achieve a particular power delivered, efficiency, gain or other specification. Drawing the output power and efficiency contours in a Smith chart, figure 2.6, can be very useful for evaluating a prototype amplifier circuit, and for this reason, it is discussed below how this could be done.

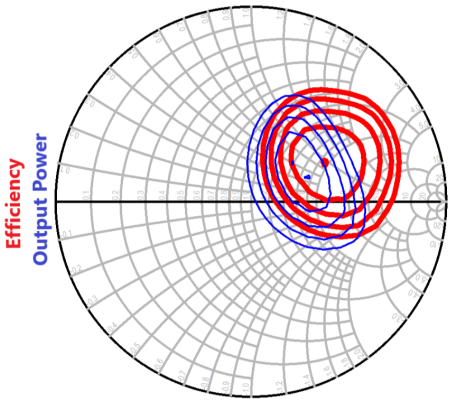


Figure 2.6: Typical load-pull data, where power delivered (blue) and efficiency (red) contours are represented.

The load-pull contour at the intrinsic reference plan can be plotted with the help of equation 2.9 by examining the movement of the RF load away from the optimum value of $Z_L = R_{opt} + j0$.

There are two resistive terminations that result in maximum linear power: when the device can swing over the full current range, which corresponds a lower resistive load (R_{LO}); or when the device can swing the full voltage range, which corresponds to a higher resistive load (R_{HI}). In the first case, the voltage swing is reduced and in the second one, the drive level has to be backed off to reduce current swing. So, we have two points on a load-pull contour for the same output power. These points can be now extended into a continuous arc of constant power by adding a series/shunt reactance/susceptance to the load, which increase

voltage/current swing, while the current/voltage swing remains as its maximum value [13]. This explanation is illustrated in figure 2.7. The fact that the contours are closed and the limiting points of constant power coincide with the intersection of the arcs drawn separately, justifies the oval shape of the output power contours.

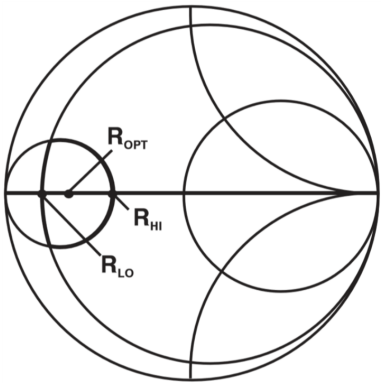


Figure 2.7: Construction of the power output contours [13].

To estimate the efficiency load-pull contours, first it is necessary to calculate the DC power consumption (P_{dc}). For a class B amplifier P_{dc} is given by

$$P_{dc} = V_{DD} I_0 = \frac{1}{\pi} V_{DD} I_{max} = \frac{2}{\pi} V_{DD} \frac{V_{DD} - V_k}{|Z_L|} \tag{2.10}$$

Therefore, efficiency is given by:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\pi}{8} \frac{R_L Imax}{V_{DD}} \tag{2.11}$$

This efficiency expression leads to the constant efficiency load-pull contour, set shown in figure 2.6.

In this dissertation, this technique was used for the design of amplifiers, and thereby, it became even more essential to understand the concepts associated with it.

Network Characterization

In order to totally characterize an unknown linear two-port device, it is necessary to make measurements under various conditions and compute a set of parameters. In this way, scattering parameters or S-parameters can be used to describe the electrical behaviour of the device (or network) by measuring the magnitude and phase of the incident, reflected and transmitted signals, when the output is terminated in a load, which is equal to the characteristic impedance of the test system. Therefore, these parameters are relatively simple to measure since it is not based on total current and voltage measurements (like H, Y and Z parameters), but with familiar measurements such as gain, loss, and reflection coefficient [20].

In the following image it is represented a generic two-port network with their travelling incident (a_1 and a_2) and reflect (b_1 and b_2) waves.

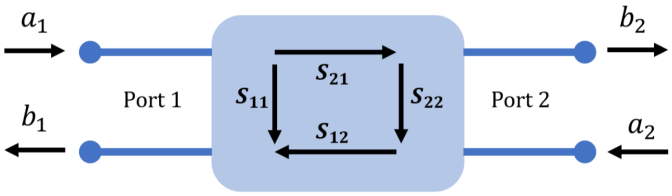


Figure 2.8: Generic two-port network.

The number of S-parameters of a device is equal to the square of the number of ports, so in this case, four S-parameters. The numbering convention for the S-parameters is that the first number is the port at which energy emerges, and the second is the port at which energy enters. Hence,

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1}|a_2 = 0 & \qquad S_{12} &= \frac{b_1}{a_2}|a_1 = 0 \\ S_{21} &= \frac{b_2}{a_1}|a_2 = 0 & \qquad S_{22} &= \frac{b_2}{a_2}|a_1 = 0 \end{aligned} \tag{2.12}$$

where S_{11} and S_{22} indicates a reflection measurement related to port 1 and 2, respectively; S_{21} and S_{12} are the forward and the reverse complex transmission coefficient, respectively.

In practise, the S-parameters of a device are measured using a Vector Network Analyser (VNA). However, the use of this equipment implies performing a calibration process in order to get accurate measurements.

Calibration is defined (by ISO) as *a set of operations that establish, under specific conditions, the relationship between values of quantities indicated by a measuring instrument or measuring system, or values represented by a material measure or a reference material, and the corresponding values realized by standards* [21].

In this work, it was used SOLT and TRL calibration, and therefore, these techniques are explained below.

SOLT

SOLT calibration kit consists of four standards: Short, Open, Load, and Thru. This is a defined standards calibration, meaning that each component behaviour is specified in advance using data or models. Since the behaviours of all standards are known, measuring them provides the opportunity to define all the error terms. The load behaviour largely sets the directivity terms. Together, the short and open are used to characterize directivity, source match and reflection tracking for each test port. The thru determines the forward and reverse transmission tracking, as well as the load match for each port [22].

TRL

TRL represents a family of calibration techniques which consists of three standards, Thru (T), Reflect (R) and Line (L). TRL calibration is most often performed when it is required a high level of accuracy and it is not available calibration standards of the same connector type as the DUT. This is usually the case when using test fixtures. Thus, this method can be used to remove fixtures by moving the measurements reference planes to the DUT.

Figure 2.9 represents the TRL calibration standards. The thru connects two transmissions lines directly - everything will be embedded by the calibration, unless an offset is specified in the kit definition; The reflect can be either an open or a short to provide a 180º phase shift; The line cannot be the same length as the thru standard - the phase difference between the thru and the line should be between 20º and 160º. This means that it is needed multiple (usually 2 or 3) lines standards, of different lengths, for a broad frequency coverage [23]. The line length is used in all cases for reference-plane tasks.

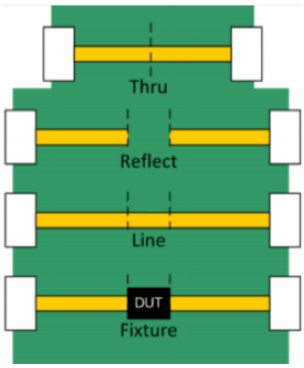


Figure 2.9: TRL calibration standards.

Comparing the two previous calibrations, TRL is, in most cases, more accurate than SOLT calibration, and besides that, it is easiest to characterize and manufacture the three standards of TRL than the four of SOLT. TRL standards are modelled, and not completely characterized, unlike SOLT calibration, which requires a full characterization of its standards. This fact could be seen as an advantage (since the characterization of the standards is simpler) or a disadvantage for TRL since there is less redundancy, and thus, more care is required to not degrade the TRL calibration and to allow repeatable connections. Finally, SOLT has a clear advantage versus TRL because it is not frequency limited, however it has lower accuracy at high frequencies [22].

2.1.3 Efficiency Techniques

Typical amplifiers have a range over which they can operate in a reasonably linear fashion, but, later on, they run into compression above a certain input level. The amplifier output cannot meet the demands of the input signal and the output tends to level off.

As seen in the previous section, the classic class B amplifier offers a maximum efficiency of 78.5%. However, this value is only reached in the (rare) signal envelope peaks, therefore, for modulation envelopes of high peak average ratio (PAPR), the class B PA average efficiency is much lower. Hence, to improve PA efficiency, but still keeping its linearity some techniques are used, which can be divided in two groups: DC supply modulation and load modulation.

DC Supply Modulation

This method is based on the dynamic V_{dc} adjustment, illustrated on figure 2.10, and is composed of two techniques: Envelope Tracking (ET) and Envelope Elimination and Restoration (EER).

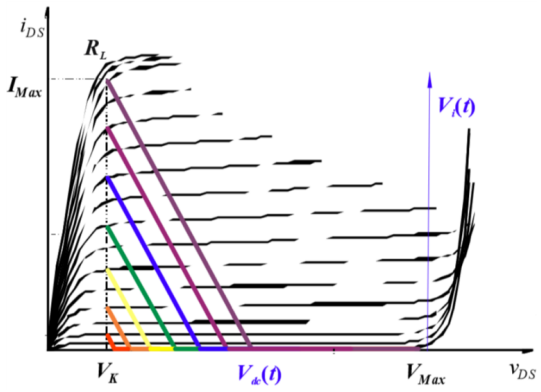


Figure 2.10: DC supply modulation principle: the load line is shifted according to the input signal, maintaining a constant slope [24].

Envelope Tracking

In the Envelope Tracking architecture, the power supply voltage applied to the RF PA is continuously adjusted to ensure that the amplifier is operating at peak efficiency for power required at each instant of transmission. To understand this technique, let's take a look at the following image:

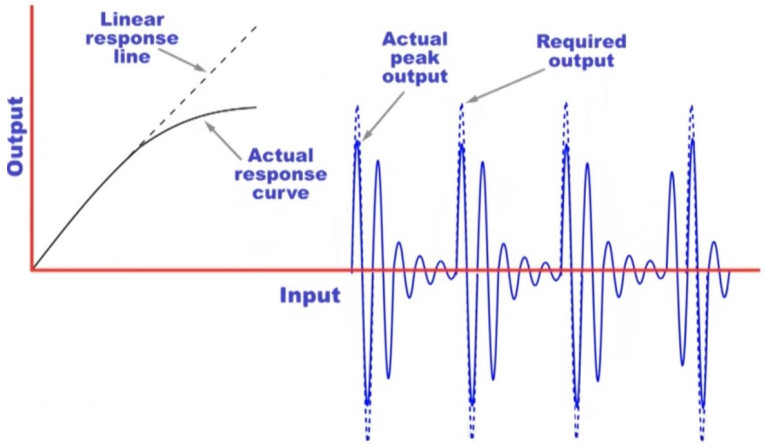


Figure 2.11: Distortion of the signal waveform as a result of amplifier compression.

The presented waveform has an amplitude element to the modulation and this needs to be preserved (which in the above example does not happen). To achieve this, the amplifier must be able to accommodate the peaks without distortion. In turn, this means the signal must be within the linear region of the amplifier, which implies a reduction of the average power level that the amplifier can accommodate. In fact, the peak to average power level is the key to the efficiency levels that can be achieved.

Over the years we have been following a progressive increase of the PAPR as mobile phone systems have migrated from the basic 3G UMTS to 4G LTE, and now to 5G. The problem with the high PAPR waveforms is that the RF amplifier requires the full voltage to be able to deliver power without running into compression, but during the periods of lower signal,

this voltage is not required and thus, power is dissipated in the device. Hence, one of the approaches that can be used is to employ envelope tracking technology, which must track the required voltage, so that, the dissipated power could be greatly reduced. The comparison between conventional and ET amplification is depicted in figure 2.12.

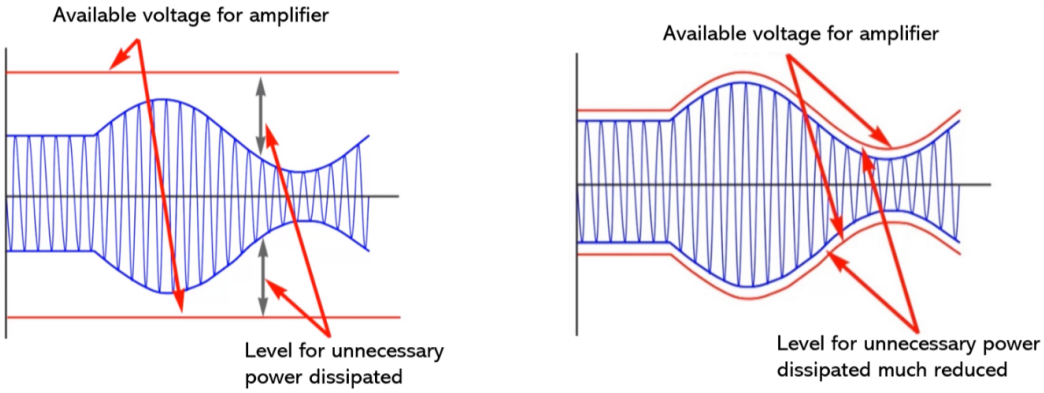


Figure 2.12: Comparison between conventional and ET amplification.

Figure 2.13 shows the block diagram of this architecture.

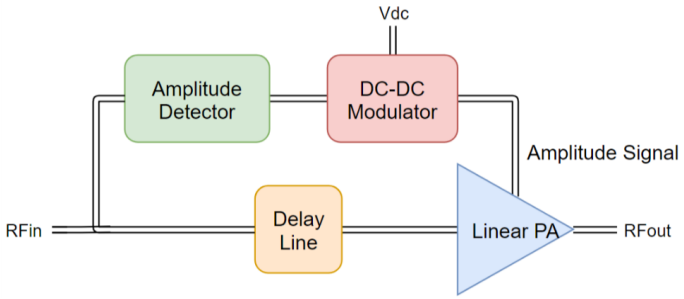


Figure 2.13: Envelope Tracking block diagram.

Envelope Elimination and Restoration

This architecture was proposed by L. R. Kahn in 1952 [25] and its working principal is identical to that of ET but, instead of a linear amplifier, it operates with a switching mode amplifier (class D, E or F). A switching mode PA does not have the same problems at lower input powers that linear PA does, since it is always operated with a square input wave.

First it is necessary to split the input modulated RF signal to form an envelope and a phase-modulated RF signal. The former and the latter signals can be generated by sending the input modulated RF signal into an envelope detector and a limiter, respectively [26]. The phase modulated signal is amplified and finally, the envelope information is restored at the amplified output signal. The block diagram of this architecture is portrayed in figure 2.14.

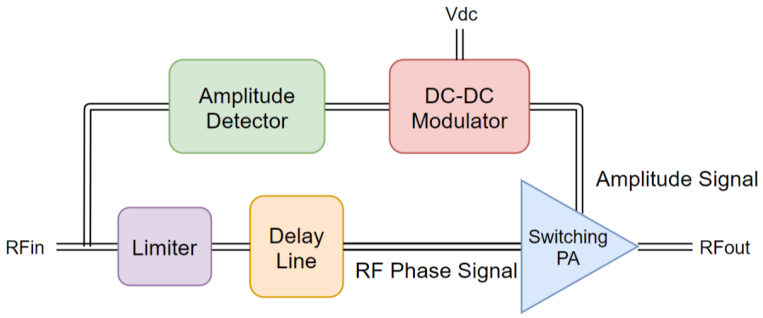


Figure 2.14: Envelope Elimination and Restoration block diagram.

Load Modulation

Load Modulation is a technique in which amplitude-modulated signals are produced with high efficiency by dynamic variation of the load impedance seen by the transistor [27], as illustrated in the figure below.

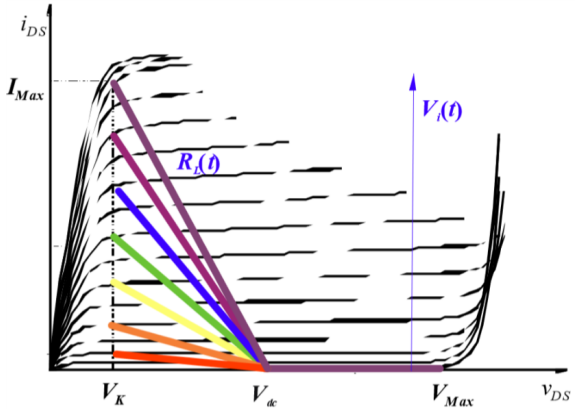


Figure 2.15: Load Modulation principle: the slope of the load line is changed according to the input signal [24].

The most popular load modulation applications in power amplifiers are the Doherty PA [28] and the Chireix Outphasing amplifier [29]. Doherty amplifiers use load-line modulation through turning on PAs at different power conditions; Outphasing amplifiers use load-line modulation through keeping PAs at peak power and producing a phase shift. Both architectures use more than one transistor.

Conventional Chireix amplifiers should behave as controlled voltage sources. A signal component separator (SCS) converts the incoming high PAPR signal into two outphased signals with a constant envelope [30]. The signals are amplified and then, a combiner sums up the outputs and reconstruct the varying envelope waveforms, resulting in an AM signal. In the Chireix combiner, the load is actively modulated by controlling the phase of the voltage at the outputs of the amplifiers.

The Doherty architecture is composed by two amplifiers: the carrier (or main) and the peaking (or auxiliary) connected by a quarter-wave transmission line. A block diagram of

DhPA is pictured in figure 2.16.

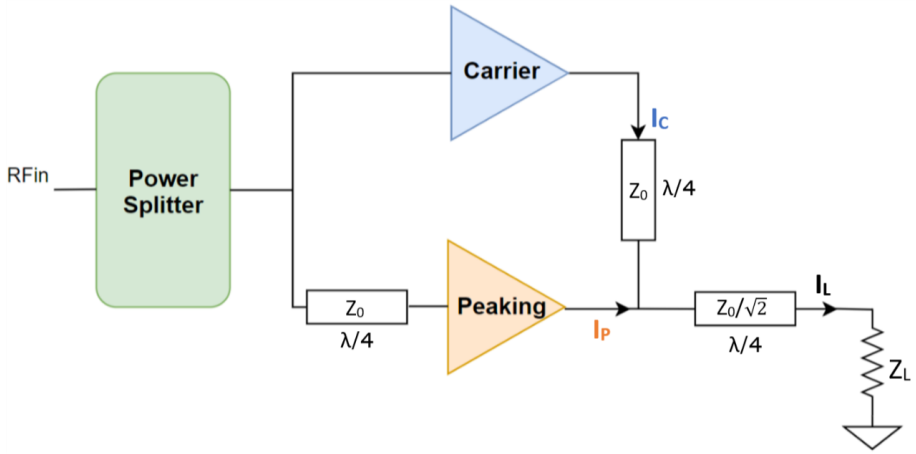


Figure 2.16: Block diagram of a traditional Doherty PA.

The DhPA technique is based on the load impedance change of each amplifier, referred to as load modulation, according to the input level. At low input signal amplitudes only the carrier is active, which is typically biased at class AB/B mode. When the amplitude of the envelope increases, the carrier PA starts to compress and, therefore, the auxiliary PA turns on, which is biased in class C. The current injected by the peaking PA along with the inverting network cause the impedance seen by the carrier, to decrease. Therefore, the slope of the load line of the main amplifier increases, keeping near saturation for higher input power levels and, this way, increasing its efficiency for a larger range of output power. Thereby, the peaking PA performs the so-called, dynamic Doherty load modulation of the carrier PA.

Note that the $\lambda/4$ line between the two PA is an impedance inverter but it also introduces a phase lag of 90 degrees at the output of the carrier PA. To adjust the same delay between the carrier and peaking PAs, a phase delay line is needed at the input of the peaking amplifier [31].

2.2 Figures of Merit

In order to numerical characterize a PA performance, several figures of merit (FoM) are defined, that are transversal to any amplification architecture and necessary for the understanding and proper design of this type of circuits. In this section, the concepts of linearity, non-linearity, gain and stability of amplifiers are studied.

2.2.1 Linearity

Linearity is the property of a mathematical relationship which means that it can be graphically represented as a straight line [32]. Linearity is mathematically defined as a function that satisfies the following two properties:

- Additivity:

$$H[x_1(t) + x_2(t)] = H[x_1(t)] + H[x_2(t)], \forall x_1(t), x_2(t) \tag{2.13}$$

  Observing the following block diagram it is concluded that this property allows to switch the adder block with the system H, maintaining the same functionality of the set.

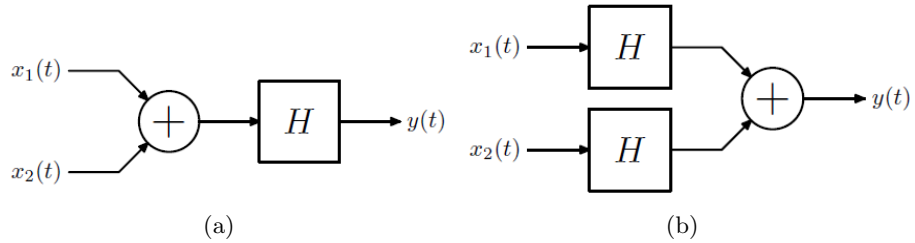


Figure 2.17: Diagram representation of linearity property.

- Homogeneity of degree 1:

$$H[\alpha x(t)] = \alpha H[x(t)], \forall x(t), \alpha \tag{2.14}$$

  Similarly, by analysing the diagram below, the conclusion obtained is that homogeneity property allows to switch the gain block with the system H, maintaining the same functionality of the set.

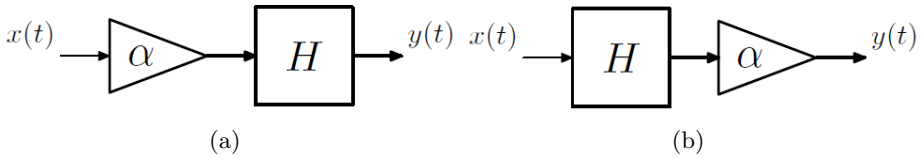


Figure 2.18: Diagram representation of homogeneity property.

Shifting this definition to the interest domain of this work, it means that if a PA is linear, its output power is proportional to the input power, by a constant gain factor, regardless of the excitation level, that is:

$$G_p = \frac{P_{out}}{P_{in}} \tag{2.15}$$

Using the power balance shown in figure 2.1 it is possible to prove the non-linearity of PAs:

$$P_{in} + P_{DC} = P_{out} + P_{dis} \tag{2.16}$$

Rearranging equations 2.15 and 2.16:

$$G_p = 1 + \frac{P_{DC} - P_{dis}}{P_{in}} \tag{2.17}$$

With this result it is impossible for an amplifier to keep a constant gain for any increasingly high input power, since the dissipated power has a theoretical minimum value of zero and the power supplied by the source is limited by a finite value. That means there is a minimum level of input power beyond which the amplifier will manifest an increasingly noticeable non-linear behaviour [9], so it is concluded that all PAs are non-linear. In fact, all devices are non-linear because, at some point, they will saturate.

A PA is usually a transistor biased to operate around a determined point. The characteristic operation curves of a field-effect transistor (FET) resemble the ones depicted in figure 2.19. The waveforms start to saturate as we approach the maximum limit that the power supply is capable of delivering, causing a smaller increase in output power, and consequently, gain compression and signal distortion. In this way, it becomes important and necessary to quantify the non-linearity of power amplifiers, which will be studied in the next subsection.

Specifically, in figure 2.19, non-linearities appear when the operation goes beyond the knee voltage (Vk) line and when the operation of the transistor falls into the cut-off region.

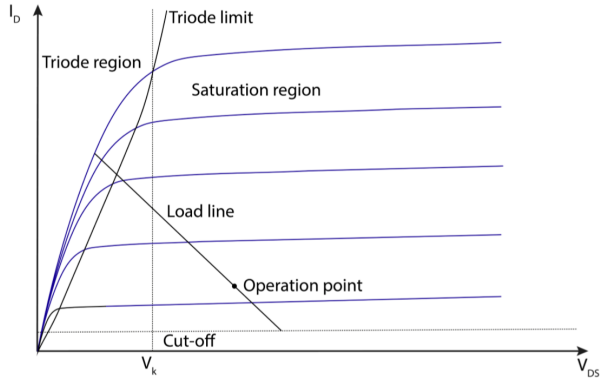


Figure 2.19: FET amplifier characteristic curves.

2.2.2 Measuring Non-Linearity

As stated previously, non-linear device characteristics can lead to undesirable effects such as gain compression and the generation of spurious frequency components. These effects may lead to increased losses, signal distortion, and possible interference with other radio channels or services [8]. Thus, the study of non-linearity becomes essential both for the design of a PA, in order to exploit the maximum power it is able to provide, and also for the development of linearization techniques that make it feasible for applications that require low level of distortion. The signal voltage is usually approximated by a Taylor series (in terms of the input signal voltage):

$$v_0 = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + ... \tag{2.18}$$

Where the Taylor coefficients are defined as

$$a_0 = v_0(0) \qquad \text{(DC output)} \tag{2.19a}$$

$$a_1 = \frac{dv_0}{dv_i}|_{v_i=0} \qquad \text{(linear output)} \tag{2.19b}$$

$$a_2 = \frac{d^2 v_0}{dv_i^2}|_{v_i=0} \qquad \text{(squared output)} \tag{2.19c}$$

and higher order terms. The constant term, a_0 leads to rectification, converting an AC input signal to DC; The linear term, a_1, models a linear attenuator (if $a_1 < 1$) or amplifier (if $a_1 > 1$); The second order term, a_2, can be used for mixing and other frequency conversion functions.

1dB Compression Point

Considering the input signal with a single carrier (one-tone), which means:

$$v_i = V_0 cos(w_0 t) \tag{2.20}$$

Through the equation 2.18, the output voltage will be:

$$\begin{aligned} v_0 &= a_0 + a_1 V_0 cos(w_0 t) + a_2 V_0^2 cos^2(w_0 t) + a_3 V_0^3 cos^3(w_0 t) + ... \\ &= (a_0 + \frac{1}{2} a_2 V_0^2) + (a_1 V_0 + \frac{3}{4} a_3 V_0^3) cos(w_0 t) + \frac{1}{2} a_2 V_0^2 cos(2w_0 t) + \frac{1}{4} a_3 V_0^3 cos(3w_0 t) + ... \end{aligned} \tag{2.21}$$

Retaining only terms through the third order, this result leads to the voltage gain of the signal component at frequency w_0:

$$G_v = \frac{v_0^{(w_0)}}{v_i^{(w_0)}} = \frac{a_1 V_0 + \frac{3}{4} a_3 V_0^3}{V_0} = a_1 + \frac{3}{4} a_3 V_0^2 \tag{2.22}$$

This result, 2.22, shows that the voltage gain is equal to the coefficient of the linear term, as expected, but with an additional term proportional to the square of the input voltage amplitude. In most practical amplifiers a_3 typically has the opposite sign of a_1, so that the

output of the amplifier tends to be reduced from the expected linear dependence for large values of V_0. This effect is called gain compression, or saturation. This is usually due to the fact that the instantaneous output voltage of an amplifier is limited by the power supply voltage used to bias the active device.

In figure 2.20 a typical amplifier response is shown.

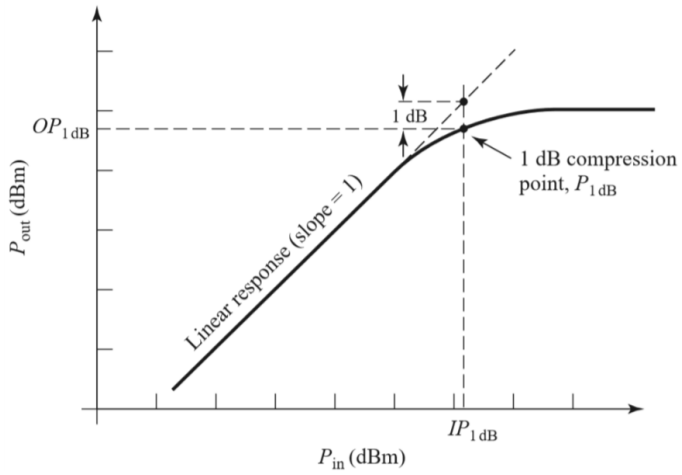


Figure 2.20: Definition of 1dB compression point [8].

1dB compression point is a measure of the non-linearity based on the gain of the amplifier. It is defined as the output power level at which the signal output is already compressed by 1 dB, as compared to the output that would be obtained by simply extrapolating the linear system's small signal characteristic [9]. The 1dB compression point can be regarded as the transition zone between small-signal operation and large-signal operation.

Harmonic and Intermodulation Distortion

For a single input frequency, w_0, the output will in general consist of harmonics of the input frequency of the form nw_0, for n = 0, 1, 2, ... Often these harmonics lie outside the passband of the amplifier and so do not interfere with the desired signal at frequency w_0. In addiction, they can be easily filtered out by the amplifier's output matching network, if necessary. The situation is different when the input signal consists of two closely spaced frequencies (two-tone):

$$v_i = V_0[cos(w_1 t) + cos(w_2 t)] \tag{2.23}$$

From 2.18 the output is

$$\begin{aligned} v_0 = {} & a_0 + a_1 V_0[cos(w_1 t) + cos(w_2 t)] + a_2 V_0^2[cos(w_1 t) + cos(w_2 t)]^2 \\ & + a_3 V_0^3[cos(w_1 t) + cos(w_2 t)]^3 + ... \end{aligned} \tag{2.24}$$

Developing the expression 2.24 it can be concluded that the output spectrum consists of harmonics of the form:

$$mw_1 + nw_2 \tag{2.25}$$

with m, n = 0, ± 1, ±2, ...

These combinations of two input frequencies are called intermodulation products, and the order of a given product is defined as $|m| + |n|$. Figure 2.21 presents a typical spectrum of the second and third order two-tone intermodulation products. As it can be seen, there are terms near the original input signals at w_1 and w_2 that will cause distortion of the output signal. This effect is called third order intermodulation distortion.

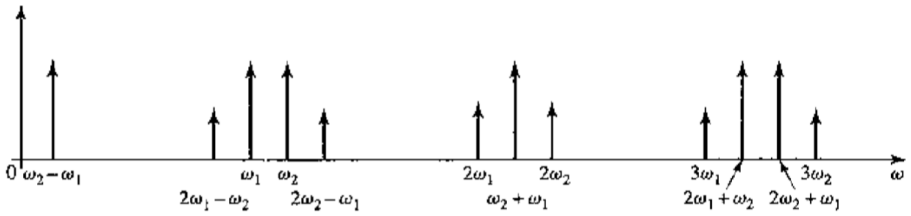


Figure 2.21: Output spectrum of second and third order two-tone intermodulation products, assuming $w_1 < w_2$ [8].

Intermodulation distortion (IMD) refers to components that are within the passband. The IMD is usually measured in terms of Intermodulation Ratio (IMR), which is defined as the ratio between the power at the fundamental and IMD output power. Typically, IMR is taken with the worst IMD component. Then, in the case of figure 2.21, the IMR is calculated with the third modulation product (which usually has the most power):

$$IMR = \frac{P_{fund}}{P_{IMD}} = \frac{P(w_1)}{P(2w_1 - w_2)} = \frac{P(w_2)}{P(2w_2 - w_1)} \tag{2.26}$$

For systems whose distortion in the lateral bands is asymmetrical, it's necessary to define the IMR for each one of them.

The presentation of this concept, intermodulation distortion, leads us to a definition of a very important figure of merit for characterizing the IMD in non-linear devices: the third-order intercept point, IP3.

Third-order Intercept Point

Equation 2.24 shows that as the input voltage V_0 increases, the voltage associated with the third order products increases as V_0^3. Since the power is proportional to the square of the voltage, then the output power of third-order products must increase as the cube of the input power. For small signal, the third order intermodulation products will be very small, but will increase quickly as input power increases. This effect is illustrated in figure 2.22.

At small-signal levels, the fundamental output power increases 1dB for each decibel rise of input power, while a 3dB per decibel is noticed for the IMD power. However, for high input power values, both curves will compress. IP3 is a fictitious point that is obtained when the extrapolated 1dB/dB slope line of the output fundamental power intersects the extrapolated 3dB/dB slope line of the IMD power [9]. IP3 can be specified as either an input power level ($IP3_i$), or an output power level ($IP3_O$) and they can be related through $IP3_O = \mathrm{G}\ IP3_i$.

Note that the IP3 can only be used for IMD characterization if it is guaranteed that no large signal effects are involved.

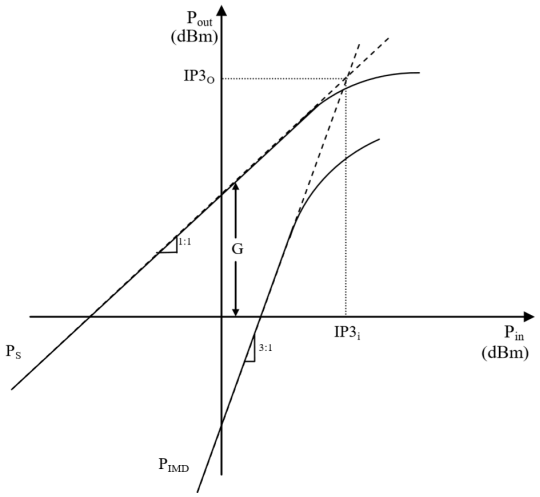


Figure 2.22: Graphical representation of fundamental output power, IMD power and IP3.

Adjacent Channel Power Ratio

Adjacent channel distortion is composed of all distortion components falling on the adjacent channel location. It behaves, therefore, as interference to a possible adjacent-channel [9]. To evaluate this type of distortion a figure of merit called *Total Adjacent-Channel Power Ratio* ($ACPR_T$) can be used. $ACPR_T$ is the ratio of total output power measured in the fundamental zone, P_o, to the total power integrated in the lower (P_{LA}), and upper (P_{UA}), adjacent channels bands (figure 2.23):

$$ACPR_T = \frac{P_o}{P_{LA} + P_{UA}} = \frac{\int_{W_{L2}}^{W_{U1}} S_o(w)dw}{\int_{W_{L1}}^{W_{L2}} So(w)dw + \int_{W_{U1}}^{W_{U2}} So(w)dw} \tag{2.27}$$

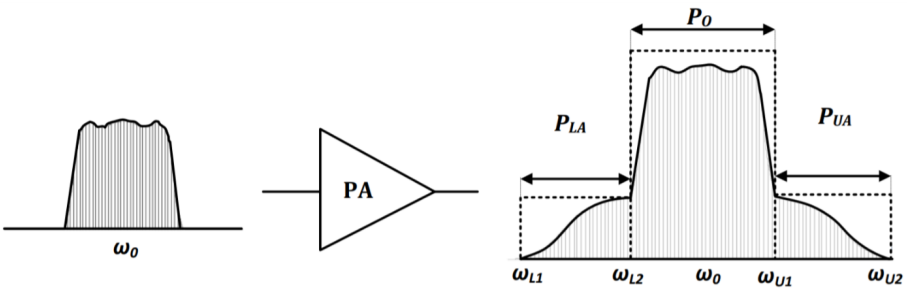


Figure 2.23: Continuous output spectrum from non linear system.

Therefore it measures the spectral regrowth caused by non-linearities. With this, it can be concluded that $ACPR_T$ is the equivalent of the IMR for continuous signals in the frequency domain.

2.2.3 Gain

Gain is one of the main FoM and it is also denominated as AM-AM conversion, since it characterizes the amplitude modulation of the output signal as a function of the amplitude of excitation at the input. More specifically, the power gain of a two-port network is defined as the ratio of the output power to input power [33]. For a two-port network, figure 2.24, the power gain can be defined in several ways in terms of its scattering parameters and the reflection coefficients, Γ_S and Γ_L, of the source and load.

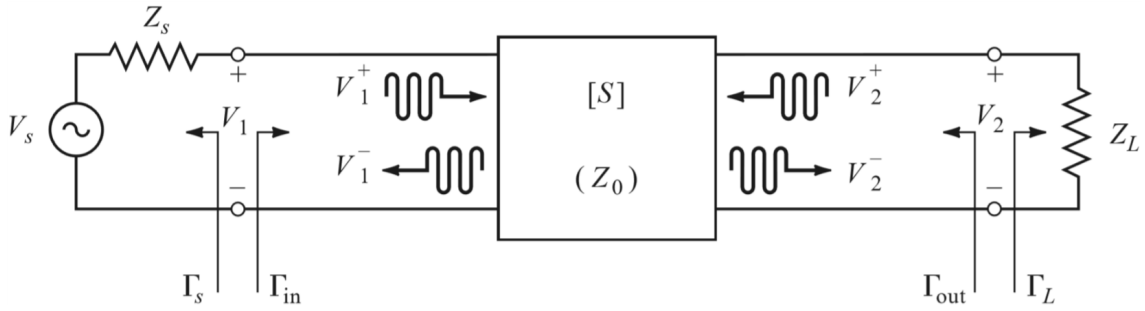


Figure 2.24: Two-port network with arbitrary source and load impedances.

- **Power Gain (G_P):** is the ratio of power dissipated in the load Z_L (P_L) to the power delivered to the input of the two-port network (P_{IN}). This expression assumes that there is maximum power transfer between the source and the amplifier.

$$G_P = \frac{P_L}{P_{IN}} = \frac{1}{|1-\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{2.28}$$

- **Available Power Gain (G_A):** is the ratio of power available from the two-port network (P_{AVN}) to the power available from the source (P_{AVS}). This definition assumes maximum transfer between the amplifier and the load, hence depends on Z_S, but not on Z_L.

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{|1-\Gamma_{OUT}|^2} \tag{2.29}$$

- **Transducer Power Gain (G_T):** is the ratio of the power delivered to the load (P_L) to the power available from the source (P_{AVS}). This is the most commonly used definition since it takes into account all variables and does not assume any type of power transfer condition. Thus, it depends of both Z_S and Z_L.

$$\begin{aligned} G_T = \frac{P_L}{P_{AVS}} &= \frac{1-|\Gamma_S|^2}{|1-\Gamma_S\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \\ &= \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2} \end{aligned} \tag{2.30}$$

A special case of the transducer power gain occurs when both the input and output are matched for zero reflection. Then $\Gamma_L = \Gamma_S = 0$, and (2.18) reduces to

$$G_T = |S_{21}|^2 \tag{2.31}$$

These definitions differ primarily in the way the source and load are matched to the two-port device. The gain is maximized if the input and output are both conjugately matched to the two-port device and $G_P = G_A = G_T$.

2.2.4 Stability

In RF and microwave bands, parasitic oscillations are much more common than in low-frequency designs because transistor feedback (either due to C_{bc} or L_e in bipolars, or to C_{gd} and L_s in FETs) and path delays (in lumped or distributed elements) increase with frequency. For this reason, and against the usual procedure followed in low-frequency amplifiers, where stability conditions are tested only after an almost completed design, at high frequencies, stability must be *a priori* guaranteed [9]. If instability develops, the PA amplifies with increasing gain, leading to an uncontrolled increase of the output power until the saturation of the device's waveforms, damaging it, if it exceeds the limit of power dissipation.

Referring to the circuit of figure 2.24, oscillation is possible if either the input or output port impedances have a negative real part, which implies that $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$ (therefore, out of Smith Chart). Because Γ_{IN} and Γ_{OUT} depend on the source and load matching networks, the stability of the amplifier depends on Γ_S and Γ_L as presented by the matching networks. Thus, it is possible to define two types of stability:

- **Unconditional Stability:** Implies $|\Gamma_{IN}| < 1$ and $|\Gamma_{OUT}| < 1$ for all passive source and load impedances ($|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).
- **Conditional Stability or Potentially Unstable:** Implies $|\Gamma_{IN}| < 1$ and $|\Gamma_{OUT}| < 1$ only for a certain range of passive source and load impedances.

Note that the stability condition of an amplifier circuit is usually frequency dependent since the input and output matching networks generally depend on frequency. Thusly, it is possible for an amplifier to be stable at its design frequency but unstable at other frequencies. Careful design should consider this possibility [34].

Tests for Unconditional Stability

Still referring to the circuit of figure 2.24, it is proved in [34] that the input and output reflection coefficients (Γ_{IN} and Γ_{OUT}) can be defined as a function of the S parameters (of the two-port network) and of the reflection coefficients of the source and the load (Γ_S and Γ_L):

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.32}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.33}$$

As stated previously, for an amplifier to be unconditionally stable it must meet the following conditions:

$$|\Gamma_S| < 1, |\Gamma_L| < 1 \tag{2.34}$$

$$|\Gamma_{IN}| = |S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}| < 1 \tag{2.35}$$

$$|\Gamma_{OUT}| = |S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}| < 1 \tag{2.36}$$

The manipulation of these expressions leads us to the **Rollett's Stability Factor**:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad \text{with} \qquad |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.39}$$

If these two conditions are met (also known as K - Δ *test*), the amplifier is unconditionally stable.

Another criterion was also proposed at [35] that combines the scattering parameters in a test involving only a single parameter, μ, defined as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.40}$$

Thus, if $\mu > 1$, the device is unconditionally stable. In addiction, it can be said that larger values of μ imply greater stability, so, in a certain way, this test measures the resistance of the circuit to oscillation.

The conditions of the two tests, K - Δ *test* and μ - *test*, are necessary and sufficient to prove unconditional stability, and are easily evaluated. If the device's scattering parameters do not satisfy the conditions, it is not unconditionally stable and stability circles must be used to determine if there are values of Γ_S and Γ_L for which the device will be conditionally stable.

Stability Circles

When a PA is conditionally stable, it is necessary to know which impedances make it stable in order to design the output and input networks ensuring stability. For that, the Smith chart is used to draw the so-called stability circles.

The equations of the stability circles can be derived from the expressions 2.35 and 2.36. It can be seen that the set of terminations leading to the stability limit, i.e.

$$|\Gamma_{IN}| = 1 \wedge |\Gamma_{OUT}| = 1 \tag{2.41}$$

are located, respectively, in circles described by

$$|\Gamma_L - C_L| = r_L \tag{2.42}$$

$$|\Gamma_S - C_S| = r_S \tag{2.43}$$

where C_L/C_S and r_L/r_S are the center and the radius of the circles in the Γ_L/Γ_S plane and are determined by the expressions:

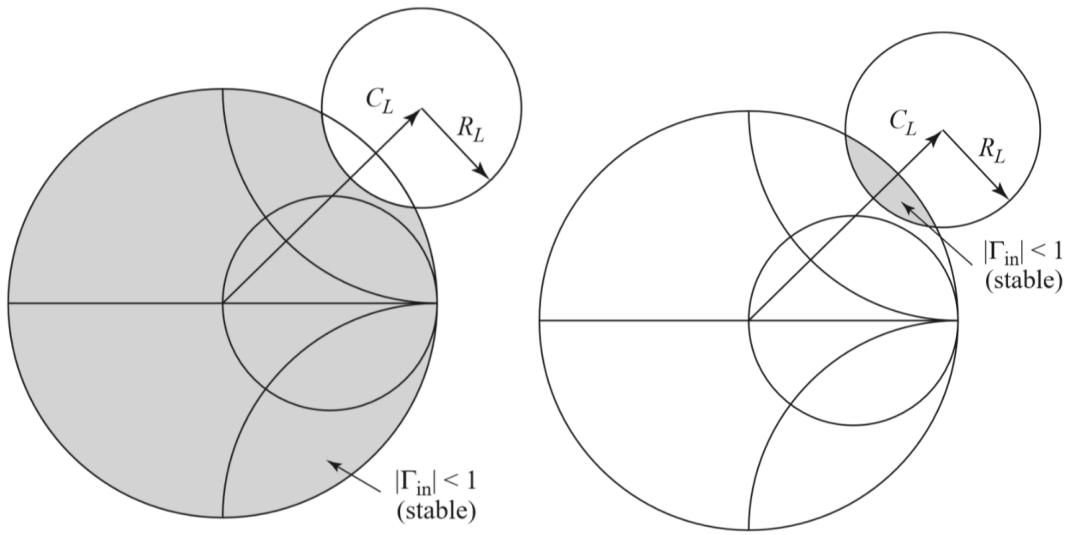
$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \qquad r_L = |\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}| \tag{2.44}$$

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \qquad r_S = |\frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2}| \tag{2.45}$$

Thus, given the scattering parameters of the transistor it is possible to plot the input and output stability circles to define where $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$. On one side of the output stability circle we will have $|\Gamma_{IN}| < 1$, while on the other side we will have $|\Gamma_{IN}| > 1$. Similarly, we will have $|\Gamma_{OUT}| < 1$ on one side of the input stability circle, and $|\Gamma_{OUT}| > 1$ on the other side. The stability circles then, define the boundaries between stable and potentially unstable regions of Γ_S and Γ_L.

These circles are drawn with their centers marked in relation to the center of the Smith chart. It is then checked whether the stable zone lies outside or inside the circle. We can easily identify the stable region assuming a load equal to the characteristic impedance. This implies Γ_L / $\Gamma_S = 0$, therefore, $|\Gamma_{OUT}| = |S_{22}|$ / $|\Gamma_{IN}| = |S_{11}|$.

If $|S_{11}| < 1$, then $|\Gamma_{IN}| < 1$, consequently the region involving the center of the Smith chart is the stable one (the outside of the circle in the example of figure 2.25(a)). Otherwise, the stable region will be complementary to the previous one (which is inside of the circle - figure 2.25(b)).



(a) $|S_{11}| < 1$ (b) $|S_{11}| > 1$

Figure 2.25: Output stability circles for a conditionally stable device [8].

The same reasoning can be applied to input stability circles.

If the device is unconditionally stable, the stability circles must be completely outside (or totally enclose) the Smith chart.

Maximum Stable Gain

Maximum stable gain (equation 2.46) is a useful figure of merit because it is easy to compute and offers a convenient way to compare the gain of various devices under stable operating conditions.

$$G_{msg} = \frac{|S_{21}|}{|S_{12}|} \tag{2.46}$$

2.2.5 Efficiency

One of the highest energy consuming components in a transmitter circuit is the PA, so amplifier efficiency is an important factor to be considered.

Efficiency characterizes DC-RF power conversion and is maximized by minimizing power dissipation at a desired output power [15]. Efficiency can be numerically represented using either drain efficiency or power added efficiency. Drain efficiency is defined as:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.47}$$

This expression does not take into account the supplied RF power, P_{in}.

Another way to represent the efficiency is to include the input power in the equation. This approach becomes particularly suitable when the gain (G) of the PA is relatively low or as it compresses when P_{out} approximates saturation. Power added efficiency is defined as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \eta(1 - \frac{1}{G}) \tag{2.48}$$

Finally, it is still possible to set the overall efficiency (η_{oe}) that characterizes the total power conversion supplied to the system in RF output power (2.49). This is a useful term to characterize the efficiency of a circuit constituted by multiple amplification stages and several (N in equation 2.49) power consuming elements (P_n in 2.49).

$$\eta_{oe} = \frac{P_{OUT}}{P_{DC} + \sum_{n=0}^{N} P_n} \tag{2.49}$$

Chapter 3

Passives Characterization

Since the purpose of this dissertation is to implement a power amplifier for frequencies above 9GHz, several tests need to be done in order to verify how some passive elements, namely, the substrate, via holes, connectors and capacitors behave at these frequencies. For this reason, the first step in the practical work is the design and implementation of six test circuits, with the objective to characterize and understand how these structures can affect the circuits by identifying possible mismatches between simulation and measurements.

Firstly, the substrate was chosen. The selected substrate was the Rogers4003C [36], available at Instituto de Telecomunicações which would allow local implementation of the circuits. The relevant parameters of the substrate for the simulation can be found in Table 3.1:

Substrate Height, H	0.508 mm
Conductor Thickness, t	35 μm
Dielectric Constant, ϵ_r	3.55
Dissipation Factor, TanD	0.0027

Table 3.1: Parameters (given by the manufacturer) used in the simulation model of the substrate Rogers4003C.

All the simulations were performed using the Advanced Design System (ADS) 2019 and *Momentum* software, both from Keysight Technologies.

The implemented test circuits are listed in table 3.2, where the respective analysis parameter is also exposed. The PCBs are shown in the figure 3.1, where they are identified from a) to f), following the order of table 3.2.

The circuits were measured with the aid of the Universal Test Fixture 3680K from *Anritsu*, so their dimensions (length and width) had to respect the range indicated in [37]. The minimum and maximum length are respectively 0.5cm and 5cm, and the minimum width is 1.4mm.

The S parameters were measured using the PNA-X from *Agilent Technologies*. The measurements were performed using two-ports and the calibration algorithm used was based on SOLT, which utilizes three impedances and one transmission standards to define the calibrated reference plane.

Figure 3.2 shows the setup made in the laboratory in order to perform the S-parameters measurements of the test circuits.

Test Circuits, Figure 3.1	Passive Structure to be Analysed
Open Stub, 3.1a)	ϵ_r of the substrate
Short Stub, 3.1b)	Via holes
50Ω Line, 3.1c)	Connectors
Series Capacitor, 3.1d)	Capacitor behaviour in series
Parallel Capacitor, 3.1e)	Capacitor behaviour in parallel
Filter, 3.1f)	Overall

Table 3.2: Tests circuits implemented to be analysed with reference to figure 3.1.

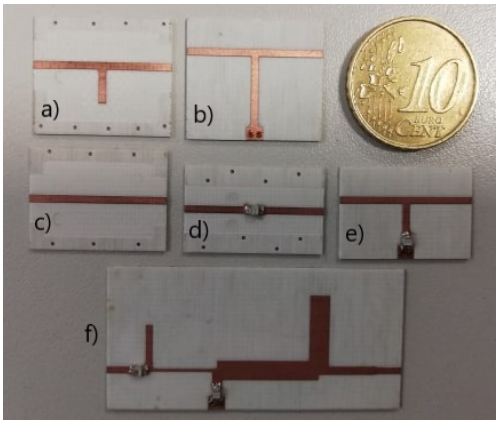


Figure 3.1: Test Circuits. a) Open Stub; b) Short Stub; c) 50 Ohm Line; d) Series Capacitor; e) Parallel Capacitor; f) Filter.

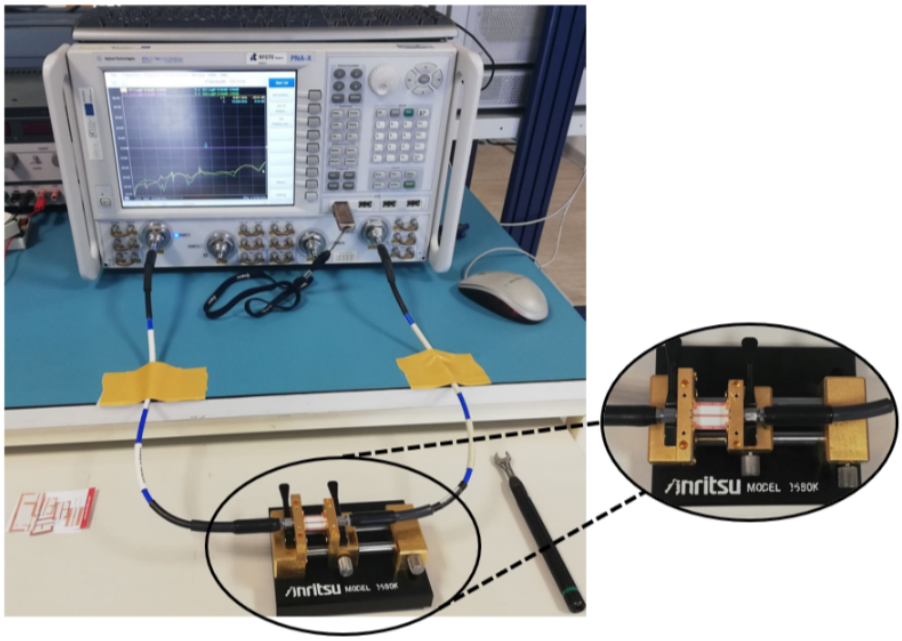


Figure 3.2: Complete setup including the PNA-X and the universal test fixture.

3.1 Open Stub

The circuit designated by open stub (figure 3.3) was designed to have a resonance at 9GHz, so the length of the stub is exactly $\lambda/4$. Besides that, the width of the lines was chosen to be a 50 Ω line. In this circuit it is assumed that the only source of error comes from the dielectric constant (ϵ_r) of the substrate.

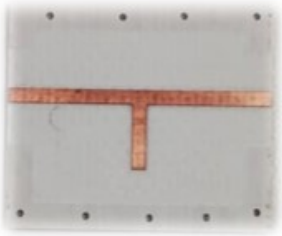


Figure 3.3: Open stub circuit.

The results of the EM simulation and the measurements are pictured in figure 3.4.

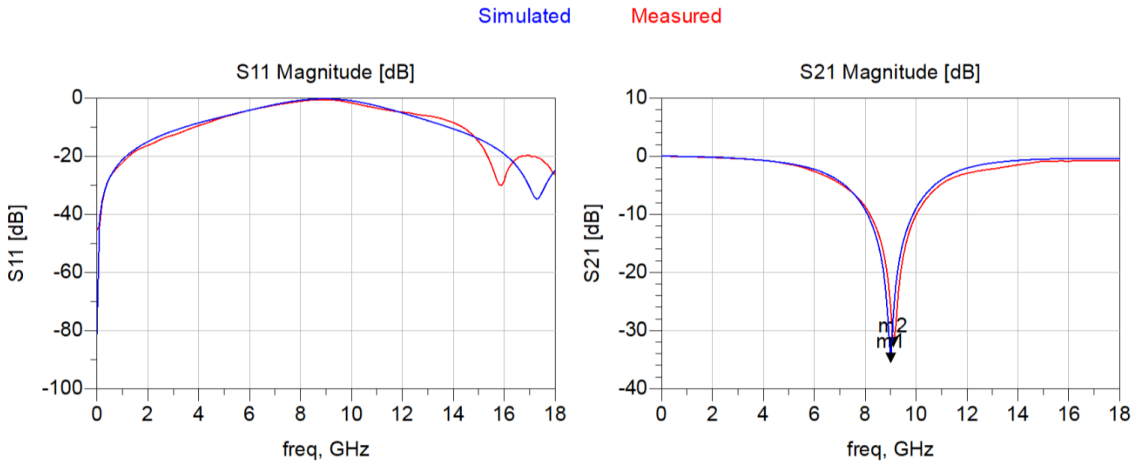


Figure 3.4: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.55$) with the measurements. Markers m1 and m2 point to the resonance frequency of the simulation (9GHz) and measurement (9.1GHz), respectively.

Observing the S_{21} we can verify that there is an offset of 100 MHz between the resonance peaks of the two graphs. After doing some simulations it can be concluded that reducing the ϵ_r to 3.45, ie., decreasing its value by 0.1, the simulated and measured values are coincident (figure 3.5). Analysing the datasheet of the substrate, [36], the manufacturer state a variation of 0.05 of the dielectric constant of the process, which does not cover the 0.1 offset verified in the experiment.

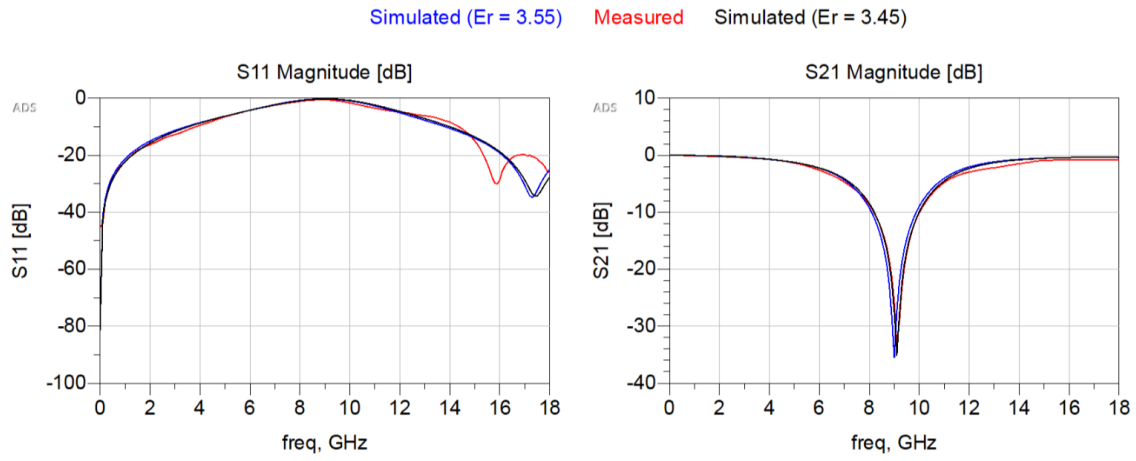


Figure 3.5: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.55$ and $\epsilon_r = 3.45$) with the measurements.

The following graphs correspond to the division between the measured and simulated values for the two dielectric constants. Thereby, it is possible to have a better perception of the similarity of the results. As we can see, we have a better match of results with $\epsilon_r = 3.45$.

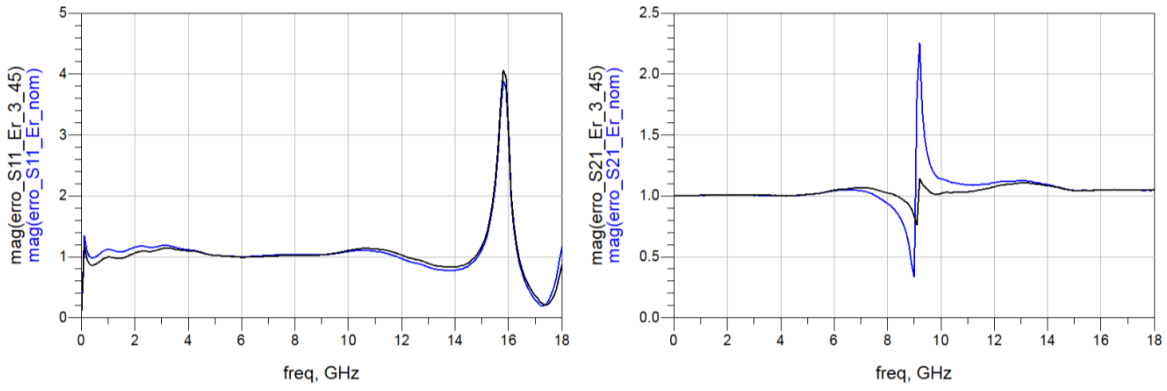


Figure 3.6: Division between the measured and simulated values (in magnitude). Blue line correspond to $\epsilon_r = 3.55$ (nominal) and the black one to $\epsilon_r = 3.45$.

In this case, the conclusions were made only observing and analysing the S_{21} measurements. The S_{11} measurements are more affected by the frequency response of the connectors and so, whenever possible, in this chapter, the analysis of the test circuits will be done through the measurements of S_{21} (but never losing sight of the S_{11} results). To prove this statement the following test with the open stub board was done: two lines with 5mm length were added to the circuit in order to represent the connectors (figure 3.7); after that, a Monte Carlo simulation was performed, varying the width of these two lines, that is, varying its characteristic impedance. In this way we can symbolically represent the circuit with different connectors.

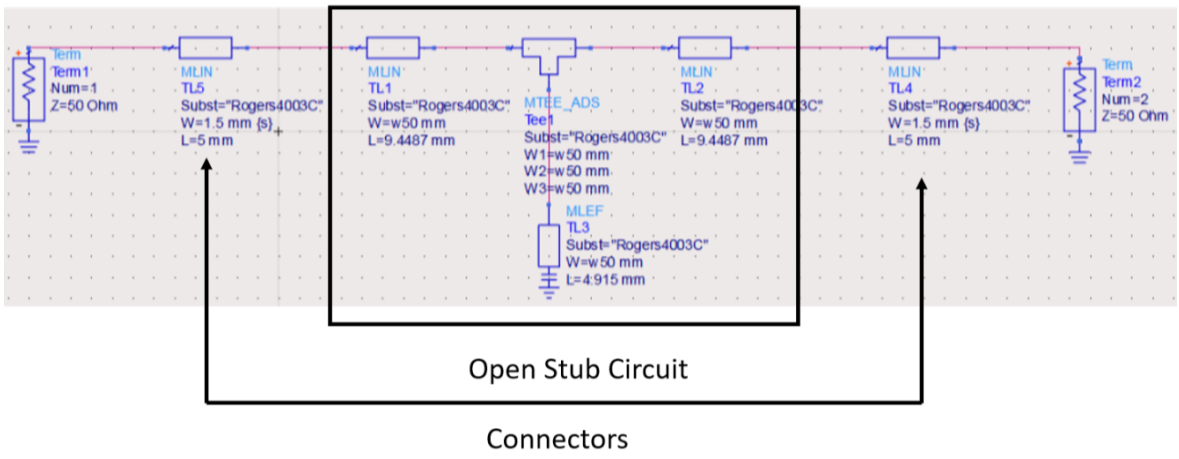


Figure 3.7: Schematic of the open stub circuit with symbolic representation of the connectors.

The S_{11} and S_{21} results were as follows:

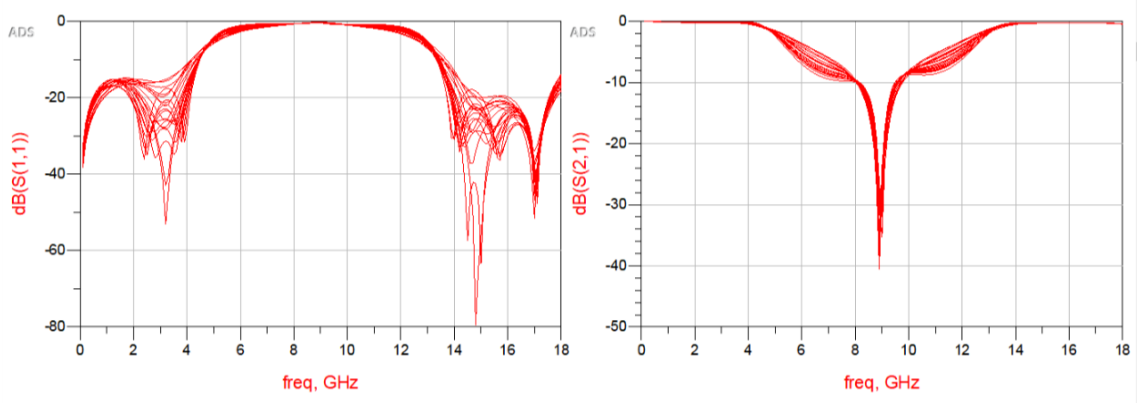


Figure 3.8: S_{11} and S_{21} results of Monte Carlo simulation.

From the previous results it is verified that for different connectors (that is, for different values of characteristic impedance of TL4 and TL5 lines) the minimum of the simulated S_{21} is not affected, being easier to identify the resonance than look into the S_{11}, which proves the initial statement.

3.2 Short Stub

Updated the value of the dielectric constant, it is now possible to add a new source of error, in this case the vias holes (figure 3.9).

Figure 3.9: Short stub circuit.

The comparison between the simulation and measurements is presented in figure 3.10.

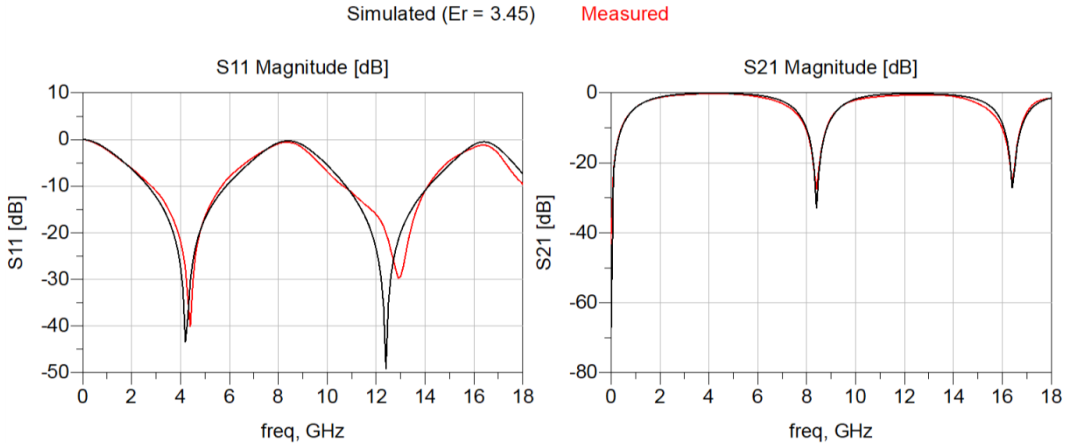


Figure 3.10: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.45$) with the measurements.

Analysing the results it can be concluded that the vias holes have no significant impact on the circuit, since the S_{21} plots are very similar, with no frequency deviation.

3.3 Parallel Capacitor

In this case, the objective is to evaluate the behaviour of the capacitor in parallel (figure 3.11).

Figure 3.11: Parallel capacitor circuit.

The test was made using a 1pF capacitor (ATC-800A1R0) and the results can be seen in the following images.

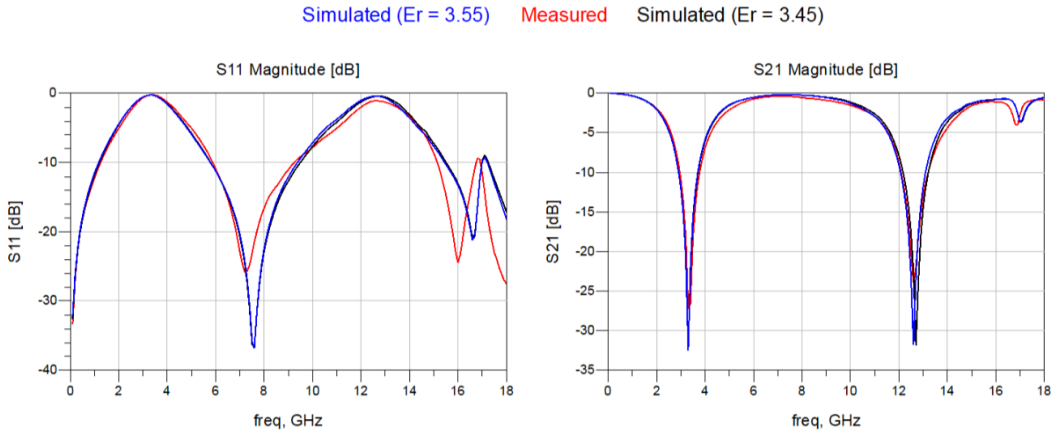


Figure 3.12: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.55$ and $\epsilon_r = 3.45$) with the measurements.

Observing the S_{21} graph the conclusion drawn is that the S-parameters used for the capacitor (given by the manufacturer) are accurate up to 14GHz. From this value onwards, a shift of around 100MHz is verified.

3.4 50 Ohm Line

This test board (figure 3.13) is intended to observe how the frequency response of the connectors may influence a circuit.

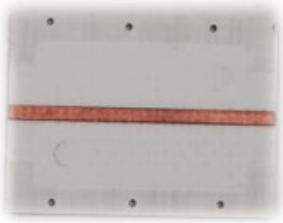


Figure 3.13: 50Ω line circuit.

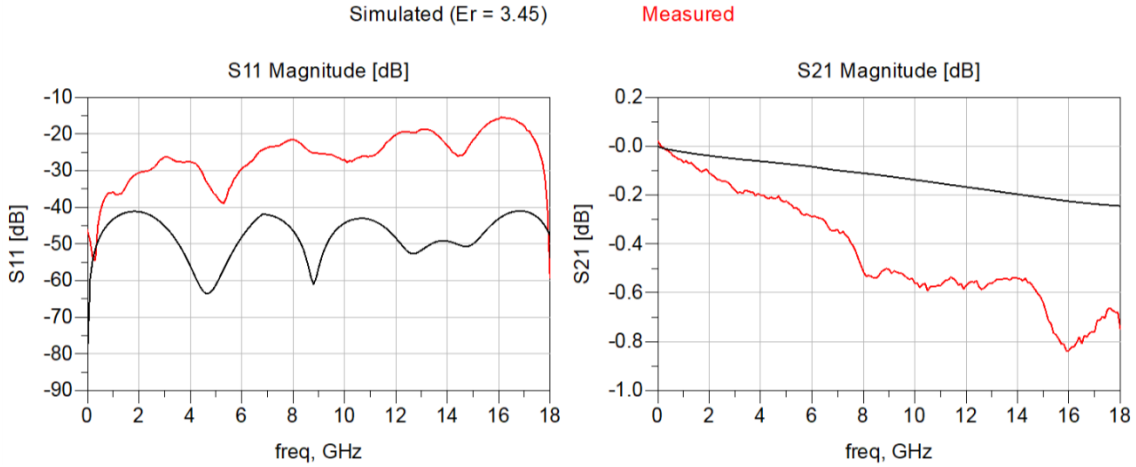


Figure 3.14: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.45$) with the measurements.

Analysing the results of figure 3.14, through S_{21}, the conclusion obtained is that the measured values present more losses than the simulated ones, which are introduced by the connects.

3.5 Series Capacitor

The analysis of this board (figure 3.15) does not allow to draw clear conclusions, since S_{11} measures are being analyse, and as already mentioned, these measurements are affected by the frequency response of the connectors. However, it can be observed (in figure 3.16) that the series resonance of the capacitor in the simulation is not very different from the one obtained in practice (offset of 300MHz). The same capacitor of the circuit of figure 3.11 was used.

Figure 3.15: Series capacitor circuit.

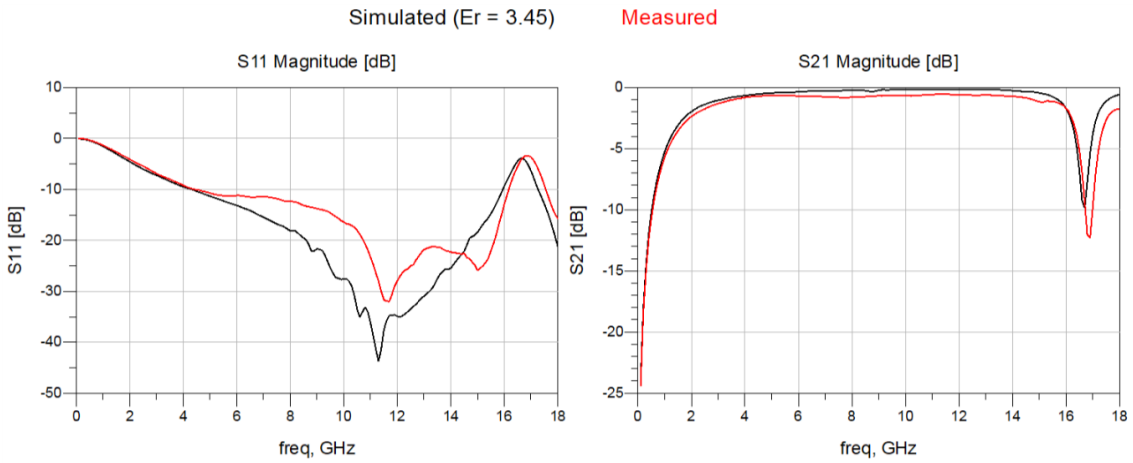


Figure 3.16: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.45$) with the measurements.

3.6 Filter

Finally, it was used a bandpass filter (whose layout was already available) with the purpose (figure 3.17) to conjugate in a single board all sources of error previously seen and then analyse the results. In figure 3.18 it is possible to compare the simulated values, with the two dielectric constants considered, with the measurements.

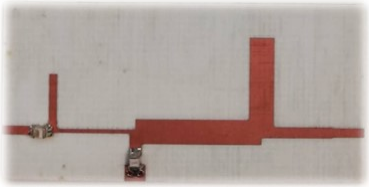


Figure 3.17: Filter circuit.

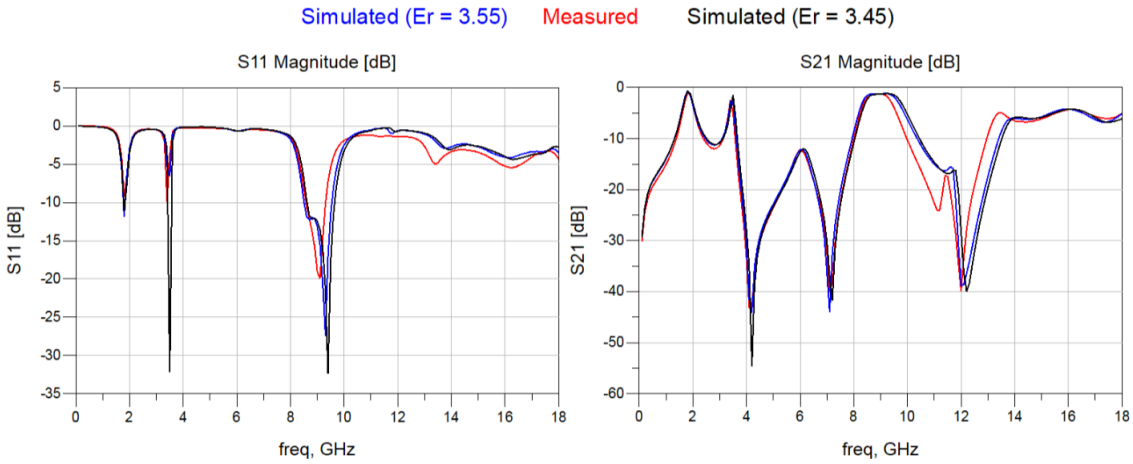


Figure 3.18: Comparison of the results of S_{11} and S_{21} obtained by simulation ($\epsilon_r = 3.55$ and $\epsilon_r = 3.45$) with the measurements.

Graph S_{21} shows that the measured values are consistent with the simulated ones (for both ϵ_r) up to 9GHz. After 9GHz the results start to differ in frequency (shift about 300MHz), introduced most likely due to the capacitors error already observed in figure 3.11.

3.7 Main Achievements

By comparing the simulated and measured results of these test circuits, it was possible to realize the impact that the substrate, vias holes, capacitors and connectors can have and thus, "fine-tune" the simulation process (in order to make it as close as possible of practice).

The main achievements of this work are stated in the following points:

- The dielectric constant of the substrate was updated to $\epsilon_r = 3.45$;
- The vias holes do not have significant impact on the results, at least, in passive elements;
- The S-parameters of the capacitors (given by the manufacturer) are considered accurate up 11GHz (since the series resonant occur at this frequency) and so, to implement a PA between 9 and 10 GHz these capacitors are reliable;
- The connectors have losses of 0.2dB (around 9GHz);
- The filter was the final test and it was proved that the passive elements analysed will not be the main cause of problems for a power amplifier design around 9GHz, since the simulations and measurements are consistent up to this frequency.

Chapter 4

PA Design, Simulation and Measurements

The main objective of this dissertation is to implement a power amplifier for the frequency between 9-10GHz with at least 5% of fractional bandwidth, which means, minimum of 500MHz. With this in mind, and also looking for the analysis made in the previous chapter, it was decided that the best compromise would be to implement an amplifier for the frequency range of 9 to 9.6GHz (600MHz of bandwidth). To achieve this final goal it was necessary to build a strategy that could make the implementation feasible at these frequencies.

Firstly, it was decided to design two amplifiers:

- Single frequency PA (central frequency between 9 and 9.6GHz);
- Multiple frequency PA (9-9.6GHz).

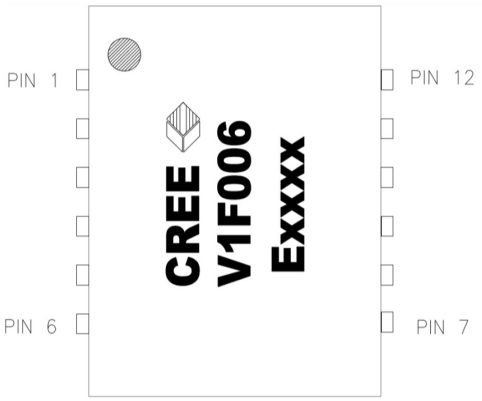
In design terms, the main difference between the two PAs is in the input matching network. The former has an RC circuit at the input to ensure unconditional stability, while the latter has not, so stability has to be guaranteed only through the matching networks. The reason for doing this is to verify the impact of the RC circuit in the overall performance of the PAs, which due to time constraints had to be simultaneously implemented.

In this chapter, the entire design process of the two amplifiers is exposed. This process, naturally, includes several steps which are: active device selection, transistor bias, load termination, matching network (MN), stability and experimental validation. The selected transistor, the chosen bias point and the DC bias network design are the same on the two amplifiers, thus these sections are common to both.

4.1 Active Device and Bias Analysis

4.1.1 Active Device

The first step in a power amplifier design is the selection of the active device. The selected transistor was the CGHV1F006S, an unmatched device from CREE Wolfspeed [38], whose ADS model was obtained from the manufacturer. This transistor can operate up to 15GHz, so it can be deployed for L, S, C, X and Ku-Band amplifier applications, which makes it suitable for a design for frequencies above 9GHz. The active device has a typical output power of 6W and uses the state of the art Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) technology. It is housed in a surface mount dual-flat-no-lead (DFN) package, whose schematic is present in figure 4.1.



Pin	Input/Output
1	GND
2	NC
3	RF IN
4	RF IN
5	NC
6	GND
7	GND
8	NC
9	RF OUT
10	RF OUT
11	NC
12	GND

Figure 4.1: Schematic of the transistor [38].

Observing the schematic it is possible to verify that the RFIN and RFOUT are associated with 2 pins each, that are located in the middle of the package. There are 4 GND pins in the extremities and other 4 pins that should not be connected. With this schematic and analysing the package dimensions in [38] a layout was set to place the transistor, which is pictured in figure 4.2.

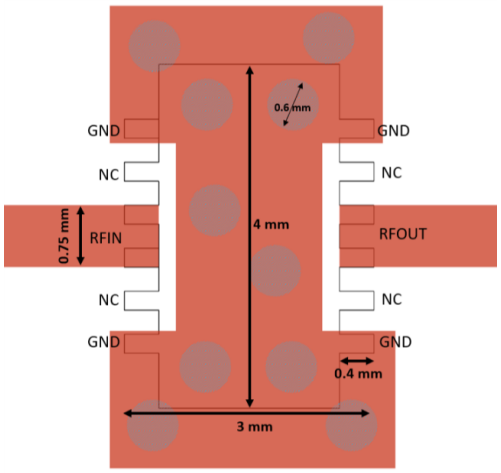


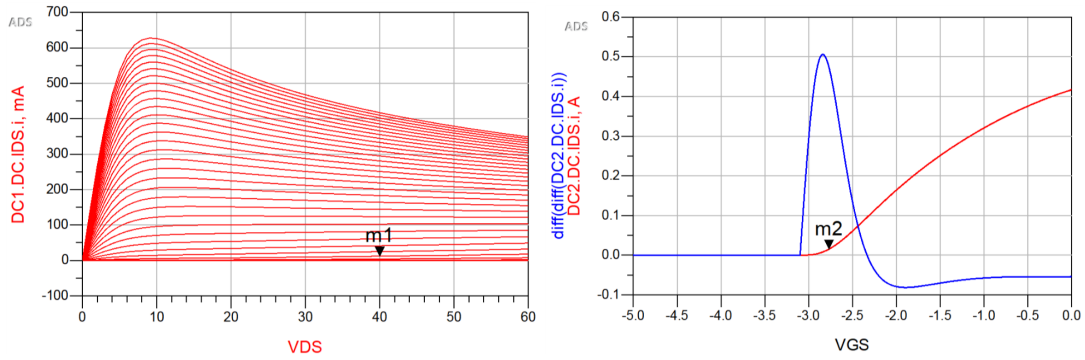
Figure 4.2: Implemented layout to place the device.

Although the diameter of the via hole is 0.6mm (due to the limitations of our PCB printing machine), the holes have to be separated at least 1mm because of the larger annular ring of the via, which means it is only possible to place two vias "side by side" underneath the transistor. The GND pins are connected to this ground plane, which also has the function of cooling the device.

4.1.2 Bias Point Selection

With the selection and analysis of the device, it is now possible to start the amplifier design by studying its biasing in ADS, using the model provided by CREE.

The bias point was selected in order to achieve a class B amplification, so the gate bias voltage (V_{GS}) should be at the threshold voltage of the transistor. Recommended by the manufacturer, it was selected a drain voltage of 40V (V_{DS}) and after that, the variation of the bias current, I_{DS}, with V_{GS} (figure 4.3(b)) was represented. Since the transition from the cut-off to the active region is not abrupt in real transistors (nor in the corresponding ADS model), the second derivate of the I_{DS} current with respect to V_{GS} was calculated (and also represented in figure 4.3(b)) because its maximum corresponds to the class B operation point [9]. Thus, a bias current of 15mA was chosen, which corresponds to a V_{GS} of -2.77V (marker m2). Figure 4.3(a) shows the transistor I-V curves, in which the marker m1 identifies the polarization point (40V, 15mA).



(a) (b)

Figure 4.3: I-V characteristic curves: (a) I_{DS} versus V_{DS} for different V_{GS} values and (b) I_{DS} current in function of V_{GS} for $V_{DS} = 40$V and 2^{nd} derivative of I_{DS} with respect to V_{GS}.

4.1.3 DC Bias Network

After selecting the bias point it is necessary to design a network that can allow the DC to pass to the gate and drain of the transistor, and at the same time, to present a high impedance at the fundamental frequency, and so preventing RF signals from leaking through the bias network.

The typical biasing circuit in a PA is composed by a RF choke and a DC block capacitor. The former connects the drain and the gate of the transistor to the respective power supply, behaving as a short circuit at DC and imposing a very high impedance at the operating frequency. The latter, as its name suggests, should block the DC component and behave as a short to RF signals. DC block capacitor is placed between the input and the gate, and between the drain and the output.

In this work, two radial stubs were dimensioned to ensure a short circuit at fundamental and second harmonic frequencies. After the stubs, a quarter wavelength line was added to create an open circuit at the fundamental and, therefore, a short circuit at second harmonic. This approach performs the function of the RF choke. The designed bias network is pictured below.

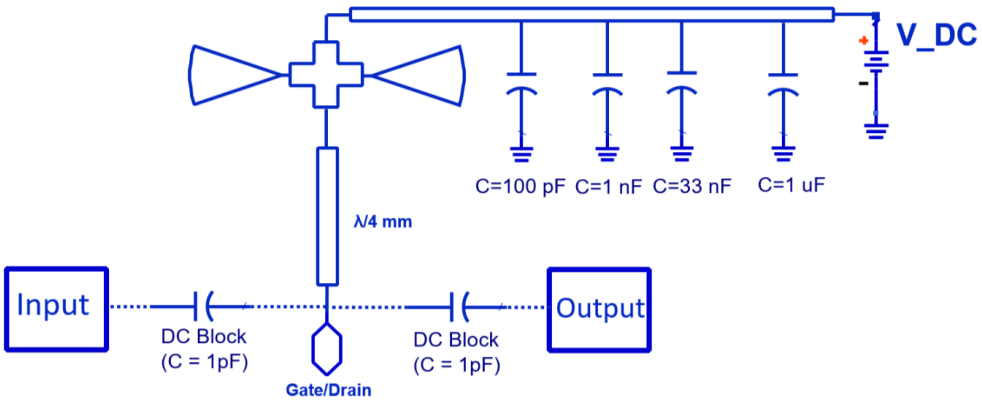


Figure 4.4: Designed bias network for input and output.

Above the radial stubs, where the power cables are welded, a few capacitors of different values (100pF, 1nF, 33nF and 1μF) were placed to ensure decoupling.

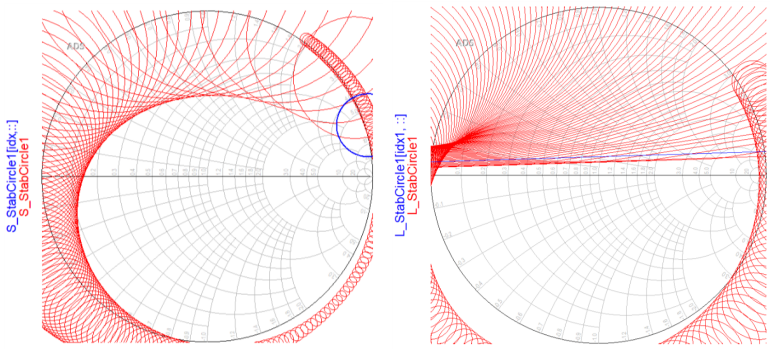
For the DC block, a 1pF capacitor was used, suitable for operation at considered frequencies.

4.2 Single Frequency PA

The design of this amplifier was done by looking just to one frequency. The fundamental frequency chosen was 9GHz.

4.2.1 Stability Analysis

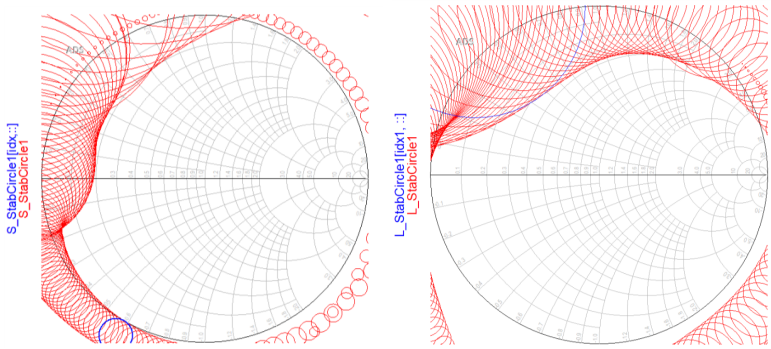
Once defined the bias network, the next step is to perform a stability analysis of the transistor to verify at which frequencies the device is potentially unstable, and thus, precautions can be taken to eliminate instability in the interest frequencies. The source and load stability circles for the frequency range of 100MHz - 19GHz are shown in figure 4.5.



(a) (b)

Figure 4.5: Input (a) and Output (b) Stability Circles.

At the fundamental frequency, the device is stable. However, from 100MHz to 8GHz and also for the frequency range of 15 - 19 GHz the transistor is potentially unstable since the stability circles cross the Smith chart. To overcome this problem it was added a 100Ω resistor in the input bias network. This approach allowed to ensure stability at low frequencies (100MHz to 1GHz) and to move the circles away from the center of the chart, figure 4.6.



(a) (b)

Figure 4.6: Input (a) and Output (b) Stability Circles.

Even so, another procedure was done to guarantee stability at all interest range, since the amplifier could still be unstable at frequencies between 2-4GHz (which in fact, was verified

at these frequencies after the matching network's design).

Introducing a capacitor in parallel with a resistor in the input RF path reduces the excessive gain of the active device, thereby improving stability. Thus, an RC parallel circuit was added to the input matching network. The RC circuit opens the branch at the desired frequency and lets the resistor cut the gain at other frequencies.

4.2.2 Output Matching Network - OMN

After the stability analysis the matching networks can be carefully projected so that the desired performance can be achieved.

The OMN has the objective to tune the load impedance at the fundamental frequency (9GHz) for a value that satisfies the desired requirements in terms of PAE and output power. To know what is the optimum load, Load-Pull technique is used.

As already mentioned in chapter 2, Load-Pull is a system that enables the synthesis of varying impedance environments at the output port of a DUT thus extracting the optimal performance from it and leading to the design of matching networks [39].

To find the optimum load at the fundamental frequency, *ADS 1-tone Load Pull for 3dB Gain Compression* template was used. The simulation was run considering the harmonic frequencies short-circuited and the source impedances set to be 50Ω. The results of this simulation are presented in figure 4.7, indicating a maximum PAE and power delivered of 53.7% and 38.3dBm, respectively.

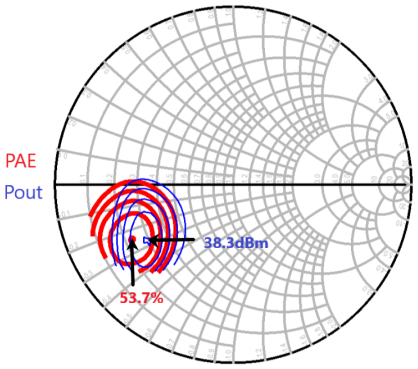


Figure 4.7: PAE and output power contours resulting from Load-Pull simulation at fundamental frequency.

The selected optimum load was the one which provided maximum PAE (53.7%) and enough power to the load (38dBm) : $Z_L = 11.355 - j11.967(\Omega)$.

The optimization of the OMN was done in order to get an amplifier performance (in terms of PAE and P_{out}) close to the values obtained in the load pull analysis, with the smallest possible network (which means less losses). Two goals were set: one to tune the OMN at 9GHz to the optimum load and another to limit the losses. The best compromise obtained for the OMN is portrayed in figure 4.8.

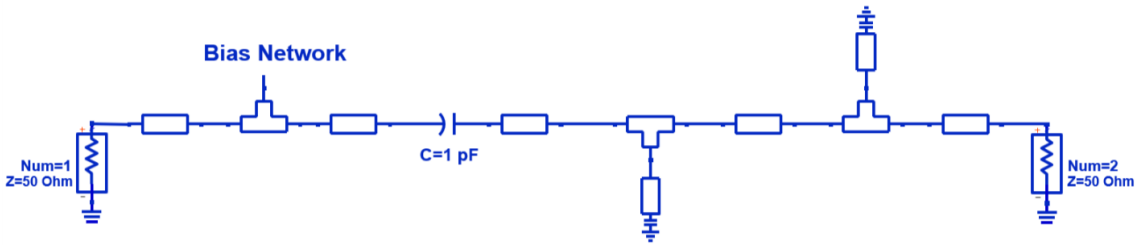


Figure 4.8: OMN schematic.

4.2.3 Input Matching Network - IMN

The final step in the schematic design is to project the input matching network. The IMN was designed taking into account two aspects: the gain of the amplifier and its stability. The optimization schematic (figure 4.9) was done with the OMN (created before) and with the S-parameters of the transistor where it was set a goal to obtain a gain above 13dB at the fundamental frequency.

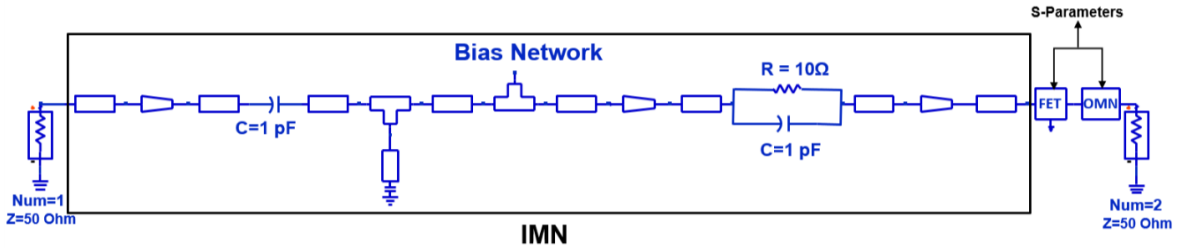


Figure 4.9: IMN schematic.

The stability test was performed in parallel with the optimization of the IMN, so the resistor and capacitor values could be adjusted simultaneously in order to ensure stability and the desired gain. The chosen values were 10Ω and 1pF for the components of the RC circuit.

Notice that other topologies were tried for the design of the matching networks, for example, using radial stubs. However, the one used (line x stub x line), proved to lead the amplifier to the best results.

4.2.4 Schematic Simulation

When the amplifier was finished at the schematic level, a harmonic balance (HB) simulation was set and the corresponding results of drain efficiency, PAE and gain are plotted in figure 4.10. The maximum drain efficiency and PAE are 54% and 50%, respectively; the gain at small-signal is 13.5dB.

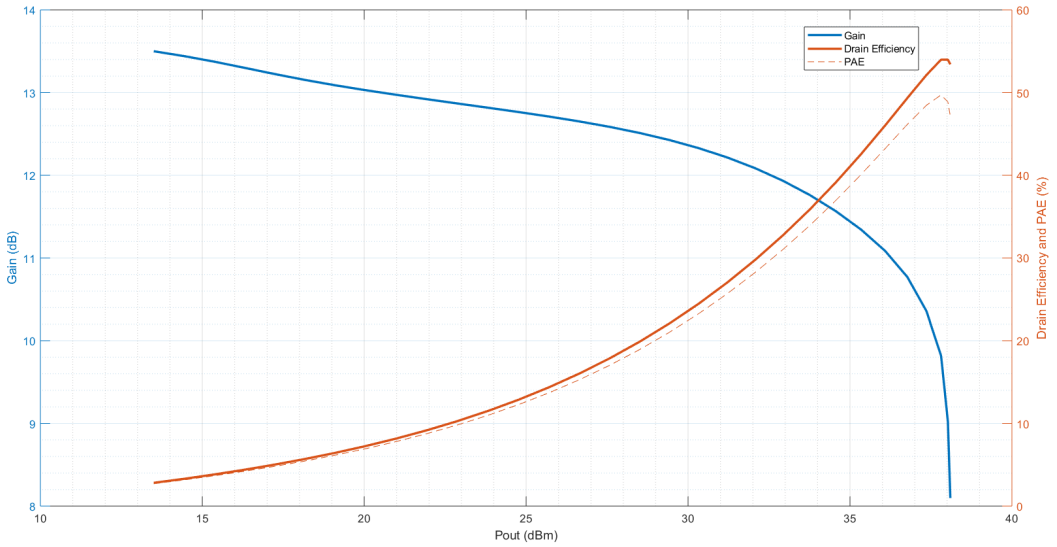


Figure 4.10: Drain efficiency, PAE and Gain versus output power.

These values are in accordance with load-pull results, since the maximum PAE and output power obtained are only 3% and 0.5dBm lower, respectively.

To verify if the PA performance is reliable, a Monte Carlo simulation was performed, so it can be investigate how the given manufacturing tolerances of the components (capacitor and resistors) and the transmissions lines affect the overall PA results. Table 4.1 presents the tolerances used in simulation and figure 4.11 shows the results of drain efficiency, PAE and gain versus output power with 40 iterations each.

Parameter	Tolerance
Transmission Line Widths	± 0.05 mm
Transmission Line Lengths	± 0.05 mm
1pF Capacitor	± 0.25 pF
Resistor Values	± 1%

Table 4.1: Tolerances used for Monte Carlo Simulation of transmissions lines, capacitors and resistors.

The tolerances of the transmissions lines are 25% of the minimum size of the drill of the printing machine, which is 0.2mm. The capacitor and resistor tolerances can be found in their datasheets, [40] and [41], respectively.

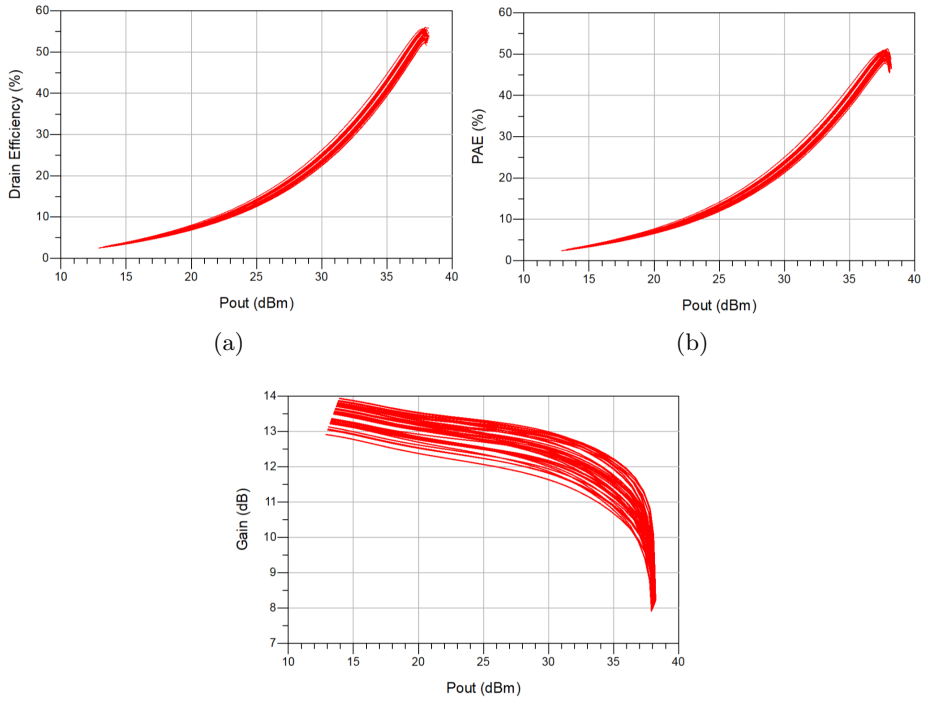


Figure 4.11: Efficiency (a) PAE (b) and Gain (c) versus output power.

The graphics from figure 4.11 show that the values of drain efficiency vary between 51-55%, while PAE vary between 47-51%. The gain presents a variation of 1dB (12.9-13.9dB).

This is an important analysis to make the project robust, since in practise these variations of the transmission lines and components do indeed occur.

4.2.5 Layout and Electromagnetic Simulation

Finally, after optimizing the matching networks in order to have the desired performance (at schematic level), the following step is to generate the layout of the circuit and to set an Electromagnetic (EM) simulation. The size of the discrete components, the position of the heat sink and its screw holes had to be taken into account.

As we increase the frequency it becomes even more important to be accurate and correct in port calibration. For this reason, additional line pieces had been created to weld resistors, capacitors and also the transistor, according to their pads' dimensions. In these ports, the calibration used was *TML zero length* with de-embedding of the added lines. The ports that connect to the connectors were calibrated with *TML*, as well as those that connect to the power supplies. A detailed explanation of port calibration can be found in [42].

Besides the ground plane created underneath the transistor (that was described in section 4.1), it was also added four holes with 1mm radius to screw the metal plate to the PCB and a main ground plane around the circuit to better shield it. Figure 4.12 shows the final layout of the PA, where it is represented (at yellow) the de-embedding resulting from the ports calibration.

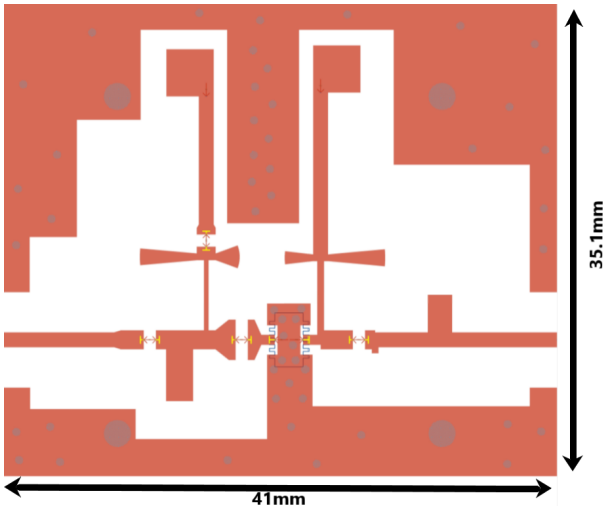


Figure 4.12: Final layout of the PA.

After setting the calibration and substrate, a mesh and S-parameters simulation were applied to the circuit, that was separated in two: the IMN and the OMN in order to reduce the simulation time.

When the EM S-parameters simulation was performed, a 1 tone HB was set up. In figure 4.13 is exposed the gain, drain efficiency and PAE curves as a function of output power.

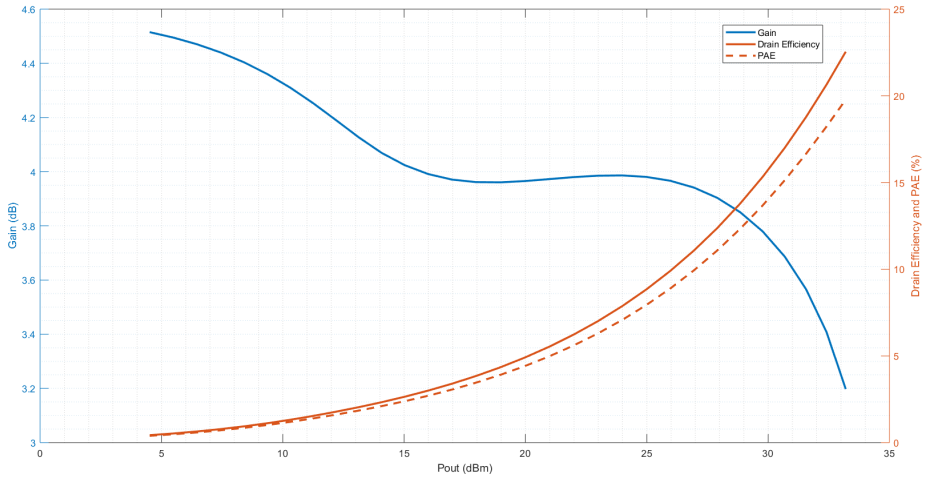


Figure 4.13: Simulated gain, drain efficiency and PAE curves for the project frequency, 9GHz.

The poor results obtained by the EM simulation allows to conclude that the performance obtained at the schematic level does not represent, at all, the one obtained from *Momentum* simulator. In this case, the gain in small-signal is 4.5dB, the maximum drain efficiency and PAE, are 22.5% and 20%, respectively.

This discrepancy of results was obviously investigated. By dividing the circuit into several parts and performing its EM simulations, it was concluded that the differences verified, occur essentially, because the models of the junctions and crosses of the schematic are not accurate at the considered frequency.

Considering these facts, it was observed the S_{21} of the EM simulation to verify if there was any frequency around 9GHz where the gain had a value close to the one obtained in the schematic simulation. S_{21} graphic showed that the gain had been shifted 500MHz to the right (9.5GHz). Therefore, it was performed another HB simulation at 9.5GHz and the results are in figure 4.14.

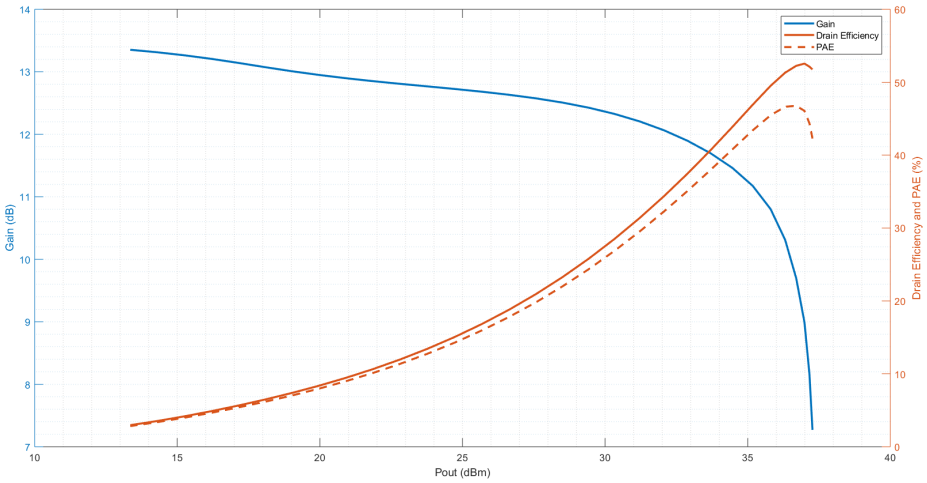


Figure 4.14: Simulated gain, drain efficiency and PAE curves for 9.5GHz.

The gain in small-signal is 13.3dB and the maximum drain efficiency and PAE are, respec-

tively, 52,5% and 47%. These values are in agreement with those observed in the schematic, except for a small decrease in the gain (0.2dB) and in drain efficiency and PAE (about 3% for both). In this way, and since 9.5GHz is still in the band initially defined, it was decided to adjust the fundamental frequency of the amplifier to 9.5GHz and to proceed to implementation and test.

It should be noted that this "schematic to layout" problem was solved in the following designs, as we shall see below.

4.2.6 Experimental Validation

The implemented amplifier was characterized by a continuous wave (CW) and also by a pulsed signal. For both measurements, a calibration process (for frequency and input power sweep) is needed, since the driver and the attenuator have different responses versus frequency and power. Using the PNA-X the S-parameters of the attenuator (and a cable) were measured and then, an attenuator vector was obtained through the expression:

$$attn = -10log_{10}\frac{1-|S_{11}|^2}{|S_{21}|} \tag{4.1}$$

After that, the driver is characterized and the software can de-embed the attenuator vector from the measured data.

The transistor was biased at the selected biasing point, which slightly deviated from the simulation values: for an $I_{DS} \approx 15mA$, it was required a $V_{GS} = -2.89V$.

CW Characterization

Firstly, CW measurements were performed. The test setup is represented in figure 4.15, which is composed by a Microwave Signal Generator, SMR 40 from *Rhode & Schwartz* ([43]), a power supply from *Keysight Technologies* ([44]), a driver amplifier (which characteristics can be seen in [45]), an isolator [46], 20dB attenuator and a *HP 437B* power meter, [47].

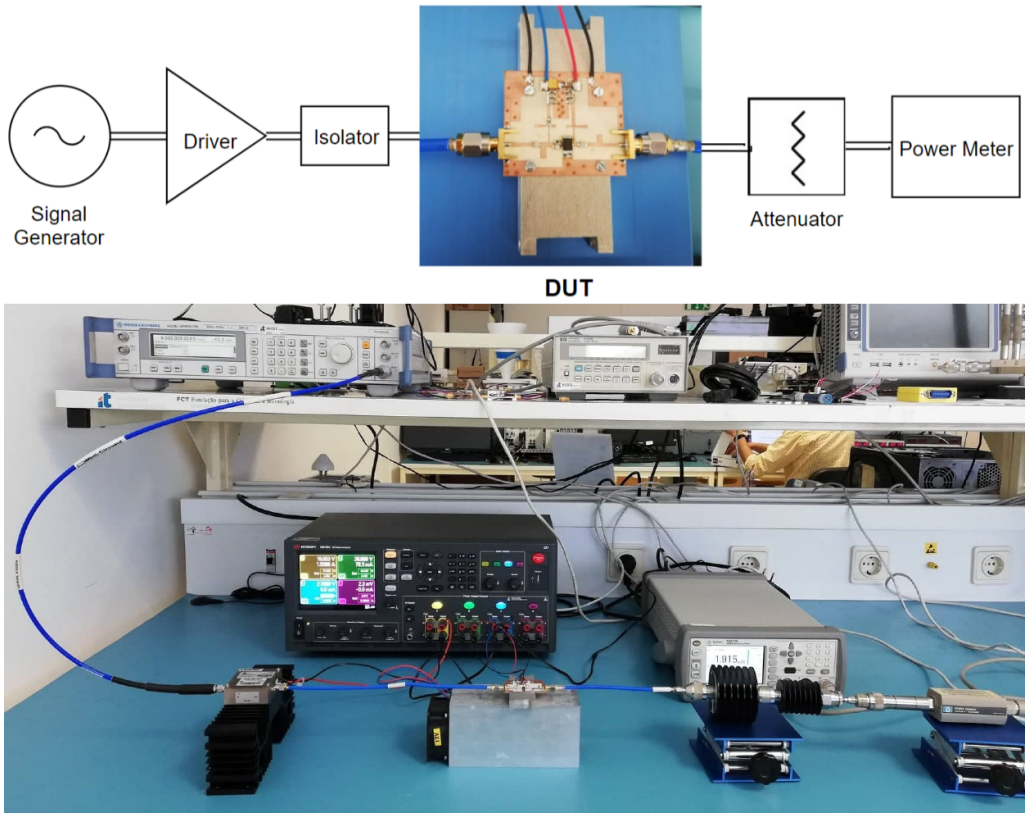


Figure 4.15: CW measurement setup with the final implemented PA.

The driver amplifier is used to increase the power provided by the generator, allowing enough input power to drive the PA. The isolator is used to prevent the RF signal of being detuned by a mismatched load, while the attenuator is used to protect the power meter sensor from high power.

Initially, a small-signal analysis was considered. Figure 4.16 shows the correspondent results from 9.3 to 9.7GHz.

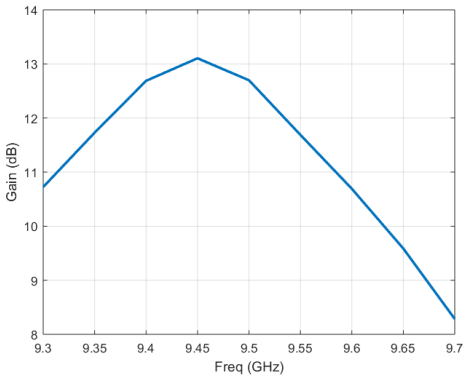
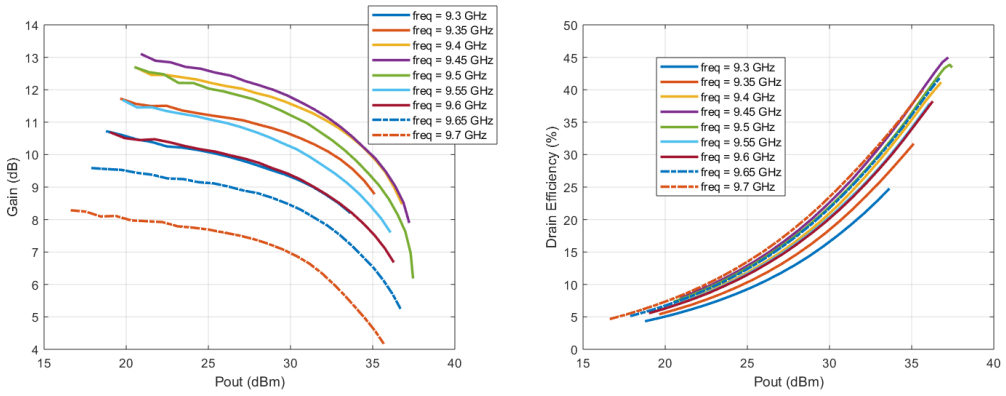


Figure 4.16: Small-signal gain of the "single frequency" PA - from 9.3 to 9.7GHz.

The maximum value of gain is for 9.45GHz, which is 0.5% shifted from 9.5GHz. After that, a power-sweep for the frequency band considered was performed. Figure 4.17 presents the curves of gain and drain efficiency versus output power from 9.3 to 9.7GHz.

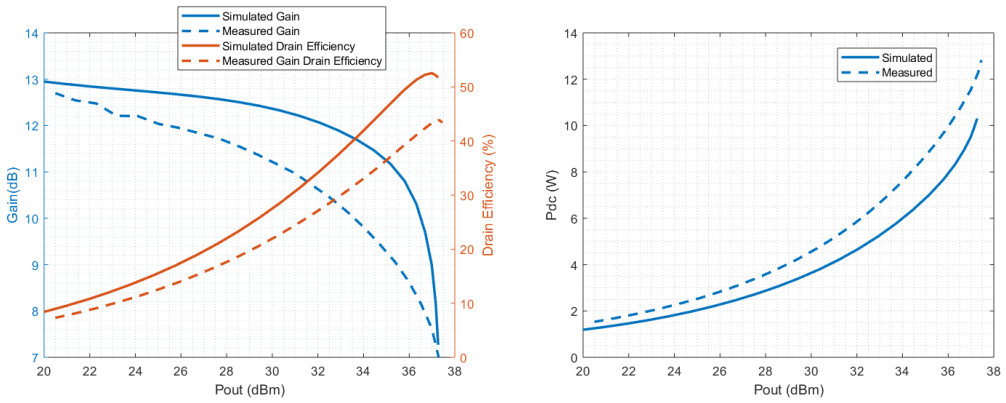


(a) Gain (b) Drain Efficiency

Figure 4.17: Gain (a) and drain efficiency (b) versus output power from 9.3-9.7GHz

From 9.4GHz to 9.7GHz it is obtained an efficiency between 38-45% and a gain between 8-13dB.

In figure 4.18 it is also represented the comparison between the measured and simulated values of the gain, drain efficiency and DC power for 9.5GHz.



(a) (b)

Figure 4.18: (a) Comparison between simulated and measured curves of gain, drain efficiency and (b) DC power for 9.5GHz.

Although the profile of the two curves slightly differ as the output power increases, the small-signal gain is similar to the one simulated. The maximum measured value of drain efficiency was 44%, below of the 52.5% simulated ones.

Through figure 4.18(b) it can be seen that efficiency is reduced because DC power is higher in the measurements than in simulation. For this reason, pulsed measurements were performed, whose setup and results are exposed in the next section.

Pulsed Characterization

The test setup is shown in figure 4.19 which is composed by an AWG (Arbitrary Wave Generator) [48], PSG Vector Signal Generator [49], UXA Signal Analyser [50], power supply ([44]), all from *Keysight Technologies*, and as CW setup, a driver, isolator and attenuators.

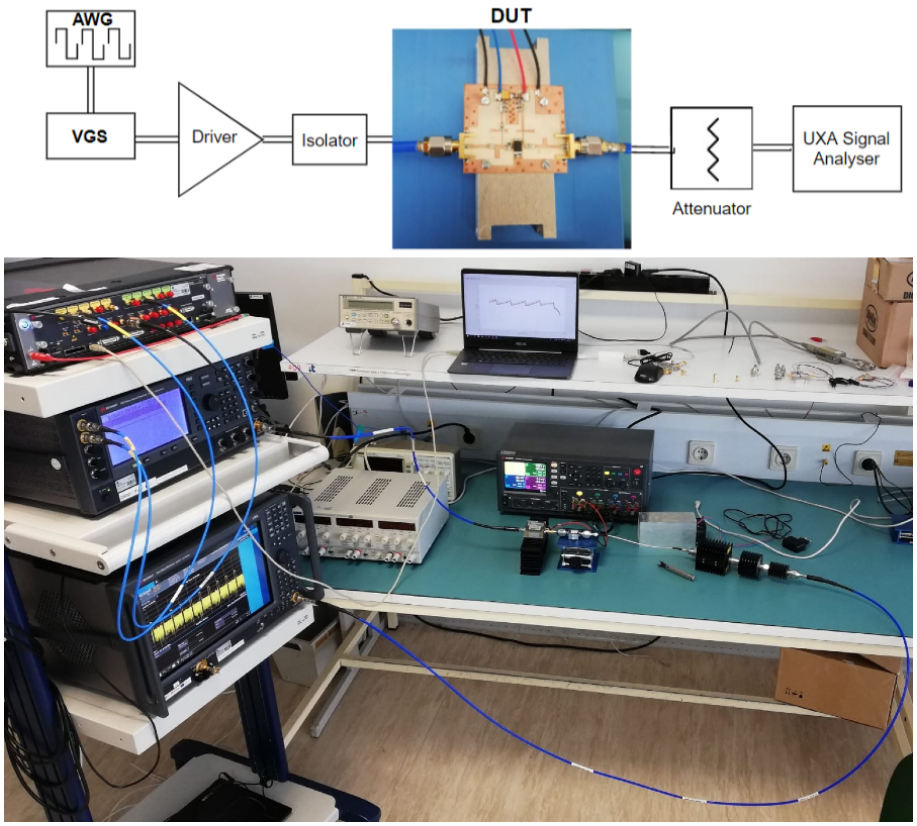
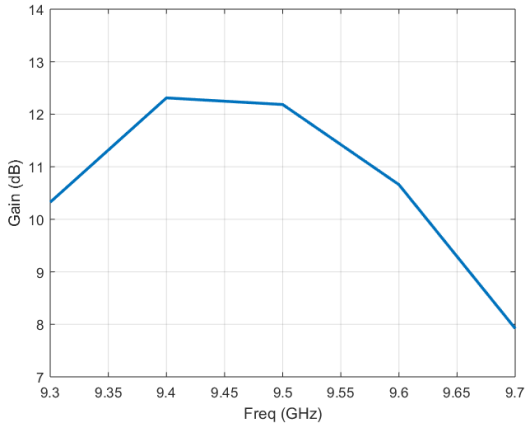


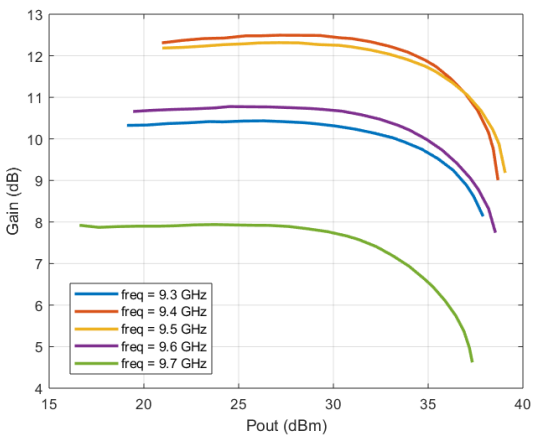
Figure 4.19: Pulsed measurement setup.

Figure 4.20 shows the results of small-signal gain which indicate a good agreement between pulsed and CW measurements. The gain and drain efficiency curves are also represented versus output power. In pulse operation, the gain curve is flat until 30dBm of output power, contrary to what is observed in CW measurements, where the gain compression occurs much earlier. This fact allow to achieve higher Pout and consequently a greater efficiency. At 9.5GHz the small-signal gain is 12.1dB and maximum drain efficiency achieved is 56.7% (ie, an increase of almost 13% comparing with CW). With these two types of measurements, it is possible to conclude that the increase of temperature (as a result of dissipated power) causes a noticeable degradation of the amplifier's performance.

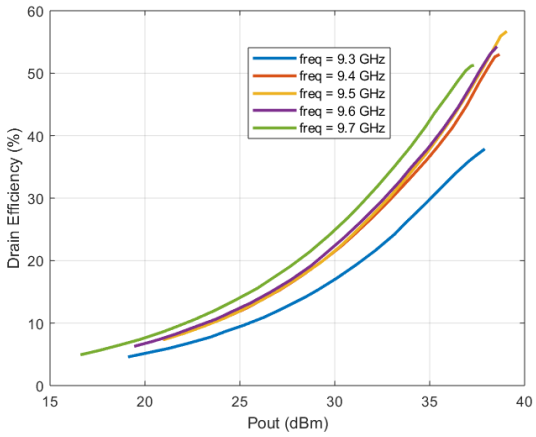
For a bandwidth of 300MHz (9.4-9.7 GHz) it is achieved a drain efficiency between 51.3-56.7 % and a small-signal gain of 8-12.3dB.



(a) Small-Signal Gain



(b) Gain



(c) Drain Efficiency

Figure 4.20: (a) Small-signal gain, (b) gain and (c) drain efficiency of the "single frequency" PA from 9.3GHz to 9.7GHz.

Since this was the first implemented prototype it was decided to verify the agreement between the simulation and measurements of the matching networks, as well as the S-parameters of the transistor. The fact that there was a TRL kit already implemented motivated this verification because it made the measurement process simple and reliable.

This analysis, which description is in the following section, proved to be very useful.

4.2.7 Amplifier Analysis

In this section, the objective is to do a deep analysis of the implemented amplifier to identify all possible errors so they can be corrected for a later design.

Both matching networks, input and output, were implemented in order to measure their S-parameters (figure 4.21). The measurements were done with the test fixture and the calibration algorithm used was based on TRL. The results are in the figures 4.22 and 4.23, where markers m1 to m4 point to the impedance at 9.5GHz.

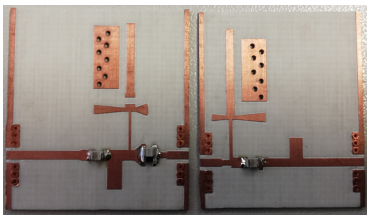


Figure 4.21: Input and output matching networks.

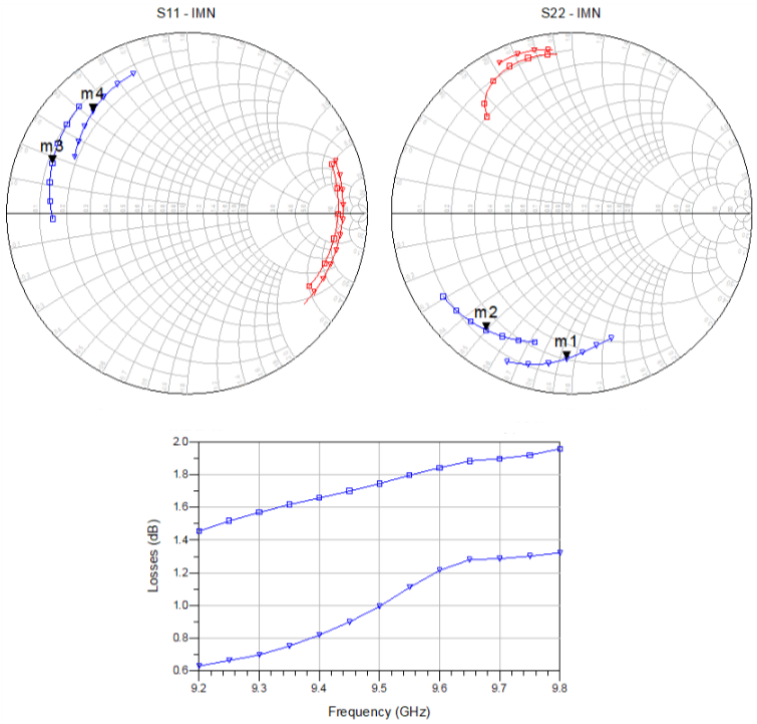


Figure 4.22: Comparison between simulated (triangles) and measured (squares) results of S_{11}, S_{22} and losses of IMN. Losses were calculated through equation 4.1. In blue and red are represented the frequencies around first (9.2 - 9.8 GHz) and the second (18.4 - 19.6 GHz) harmonic, respectively.

Analysing the S_{11} and S_{22} of the input matching network it can be seen that the measurements present a phase lag with respect to the simulated results. As expected, in the losses graphic it is verified greater losses in the measurements.

By analysing the S-parameters of the OMN (figure 4.23) it is verified that the measured and simulated impedances are similar for the 1st and 2nd harmonic, which indicates that OMN should not be the main cause of the decrease in efficiency. Through figure 4.23(c) it is possible to verify that there are more 0.2dB of losses for the measurements.

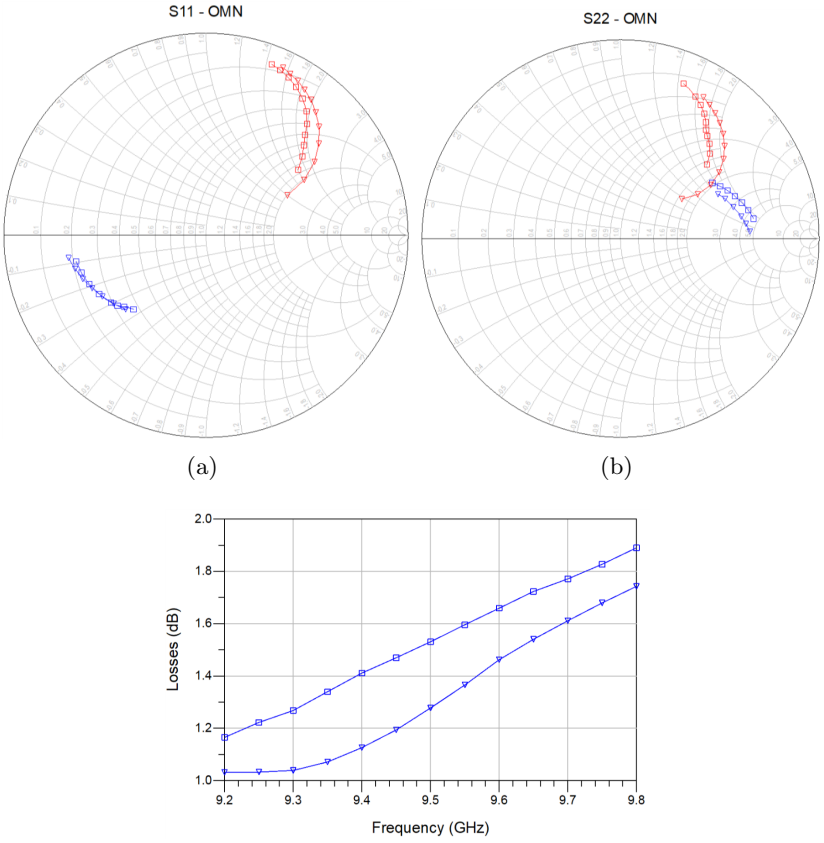


Figure 4.23: Comparison between simulated (triangles) and measured (squares) results of S_{11}, S_{22} and losses of OMN. Losses were calculated through equation 4.1. In blue and red are represented the frequencies around first (9.2 - 9.8 GHz) and the second (18.4 - 19.6 GHz) harmonic, respectively.

With these measurements, different tests were performed on ADS with the purpose to understand if the differences observed between the EM simulation and measured S-parameters of the matching networks could affect the PA performance. Table 4.2 shows the obtained results using the non-linear model with different combinations of the simulated and measured S-parameters of the IMN and OMN.

IMN	OMN	Drain Efficiency	PAE	Small-Signal Gain
Simulated	Simulated	52.5%	47%	13.4dB
Simulated	Measured	50%	46%	14.5dB
Measured	Simulated	47%	43%	7.4dB
Measured	Measured	44%	39%	7.2dB

Table 4.2: Values of Efficiency, PAE and Gain in small-signal of the PA (at 9.5GHz) for different contexts of the meshes.

As we can see through table 4.2 when the IMN is from simulation and the OMN is from measurements the results of drain efficiency, PAE and gain do not differ significantly from the complete simulation (IMN and OMN simulated). Consequently, it can be concluded that the implemented OMN is consistent with the simulation, so the differences noticed in figure 4.23 do not affect notably the results. On the other hand, when the IMN simulated is replaced by its measurements, the gain is greatly reduced. Due to the gain reduction the drain efficiency and PAE also decrease, about 3%. Hence, it is possible to conclude that the differences observed in figure 4.22 do affect the results.

Performing a HB simulation using the S-parameters measurements for the both matching networks, the results of efficiency are in accordance with the ones obtained in practise under CW signal. However, the fact that the gain is much lower than the practical one, leads to believe that there is another source of error, besides the one with the matching networks.

After analysing the matching networks, the next logical step is to verify if the simulation model of the device could be the other source of error. Therefore, the S-parameters of the transistor were measured using the PNA-X, where the device was also biased using its bias-tee. In this measurement, a special attention had to be paid, mainly to the input power limits of the PNA-X ports, in order to not damage it.

For this purpose, the circuit of figure 4.24 was implemented and measured with the universal test fixture, where the used calibrated technique was TRL. The obtained S-parameters, for the chosen bias point, are shown and compared with the ones given by the manufacturer's model in figure 4.25.

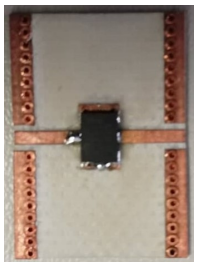


Figure 4.24: Implemented board to measure the device's S-parameters.

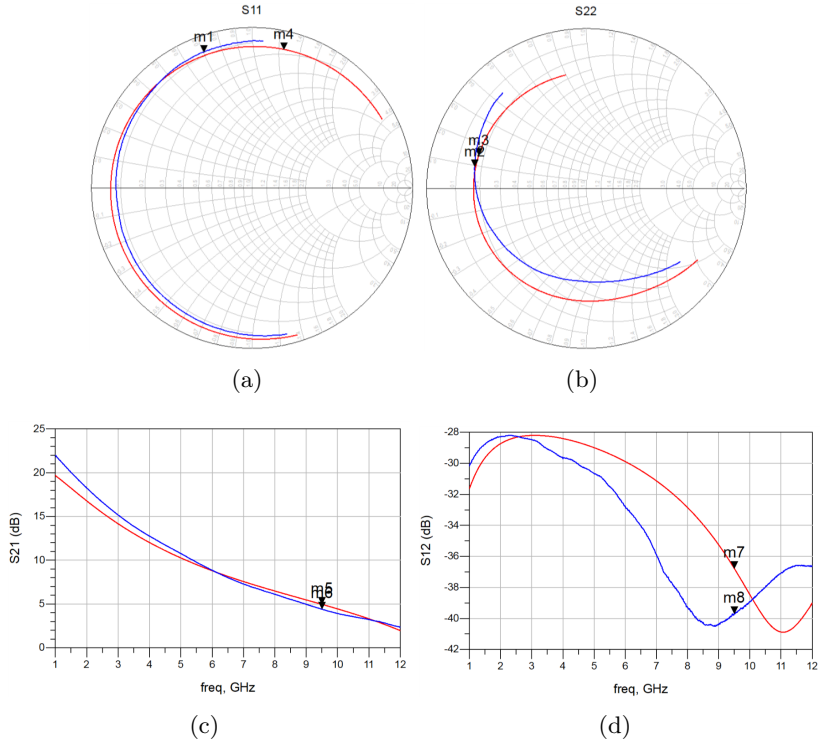
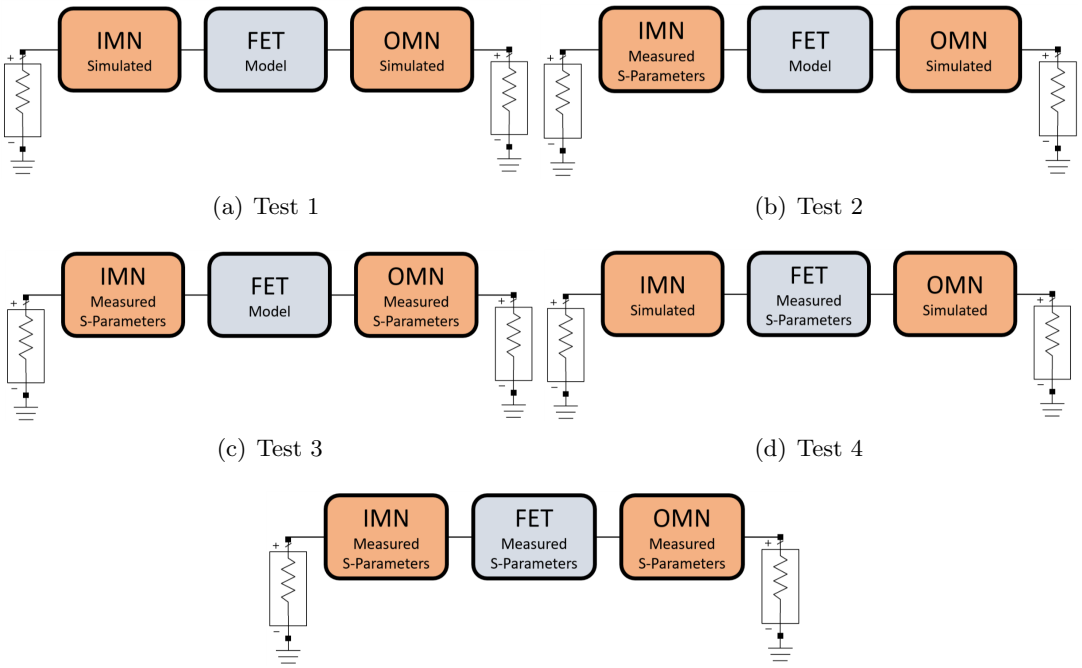


Figure 4.25: Comparison of the measured (blue) S-parameters and the ones given by the manufacturer (red) for 1 - 12 GHz. Markers m1 to m8 are at fundamental frequency (9.5GHz).

Analysing the results it is verified a phase lag on S_{11} measurements, unlike S_{22}, that at fundamental frequency the impedances are similar. At 9.5GHz it is possible to see a 0.5dB difference on S_{21} graphic. In S_{12} graphic, it is also verified a difference of 4dB between the model and the measurements, due to a phase lag.

With the previous measurements (of the matching networks and the transistor), the S_{21} of the following circuits was analysed to realize how the device and the MNs can affect the gain, figure 4.26.



(a) Test 1

(b) Test 2

(c) Test 3

(d) Test 4

(e) Test 5

Figure 4.26: Tests performed on ADS with different combinations (measured or simulated) of IMN, OMN and transistor.

Figure 4.27 portrays the S_{21} of the previous tests.

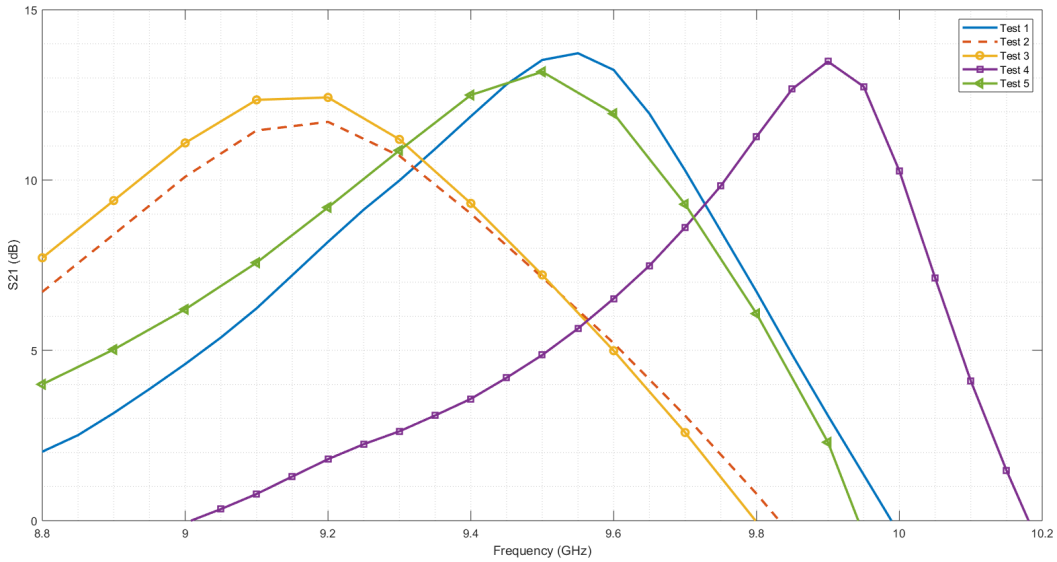


Figure 4.27: Comparison of the S_{21} of the circuits referred in figure 4.26.

By analysing these tests, several conclusions can be taken:

- Test 2 shows that the difference between the simulation and the measurements of the IMN causes the forward gain of the PA to have a shift to the left of around 400MHz, and so, the gain at 9.5GHz is about 7dB (as already verified);
- Tests 2 and 3 do not differ significantly, thus OMN of PA does not affect the small-signal gain. In fact, OMN even increases it by almost 1dB;
- Test 4 shows that the model given by the manufacturer it is not completely suitable for the produced PCB, since the gain shifts about 400MHz to the right;
- Finally, test 5 demonstrates that the final results of S_{21} are in accordance with the initially projected ones (excluding the losses), but, not because the implementation was consistent with the simulation, but because there were two errors that cancelled each other.

The differences verified on the IMN confirmed the initial suspicious. Analysing the IMN, a critical part of the circuit is the RC. The resistor used on the implemented PCB is not ideal and therefore, it has associated parasitics that were not contemplated in the simulation. In conclusion, this part is the most probably cause of the differences observed between the simulation and measurements of the IMN, and for this reason it was designed *a priori* another PA removing the RC.

Although the differences obtained on the IMN were not completely surprising, the fact that the simulation model of the transistor was not correctly represented was rather unexpected.

With this, the multiple frequency amplifier, whose description is in following section, will only allow to take defined conclusions about the cause of error of the IMN, since the design was done with the same device model. From another perspective, it can also be seen as a final test to have completely sure that the model is inaccurate, and it was not an isolated incident.

4.3 Multiple Frequency PA

The design of this amplifier was done by looking to a frequency band: 9-9.6GHz.

4.3.1 Output Matching Network - OMN

Similarly to the previous PA, the design of the matching networks starts with the selection of the optimum load, but, in this case, for a frequency band. To achieve that, it was done a load-pull analysis in order to elaborate the following table (4.3.1), which is composed by the optimal efficiency loads for the different frequencies of the band.

Frequency (GHz)	Optimal Efficiency Load (Ω)
9.0	11.08 - j7.58
9.1	10.75 - j8.87
9.2	12.12 - j9.29
9.3	11.75 - j10.63
9.4	11.75 - j10.63
9.5	11.36 - j11.97
9.6	12.65 - j12.5

Table 4.3: Optimum efficiency loads for a specific frequency.

After that, several optimizations were done tuning the OMN for each impedance of table 4.3.1 and performing a HB simulation (with a RF choke and a DC block capacitor on the input, since the IMN was still not designed) to evaluate the efficiency and output power of the amplifier. It was also tried to optimize the OMN dynamically, ie, for each frequency, tune the OMN to the respective optimal impedance. For this, a file with the information found in table 4.3.1 was created and with the Data Access Component (DAC) was possible to associate the frequency and the impedances to variables, thus allowing the optimization of the mesh. Nevertheless, the best performance obtained was with a fixed impedance (for all frequencies), which was 11.08 - j7.58 (Ω).

In order to optimize the matching network, an update was made relatively to the way done in the single frequency PA: after optimizing the OMN in a (total) schematic level, it was performed EM simulations with the T-junctions, as illustrated in figure 4.28, and then another optimization was done tuning the line lengths. This new way of optimization makes the process slower, however it also makes the schematic simulation reliable, since T-junctions and cross-junctions are responsible for most of the differences between schematic and layout. Thus, in the end, the simulation at schematic level will be similar to the one performed by *Momentum*.

Figure 4.28 shows the obtained OMN, where the goals to optimize the network were the same as the previous PA, that is, limit the losses and tune OMN to the optimal load, for 9-9.6GHz.

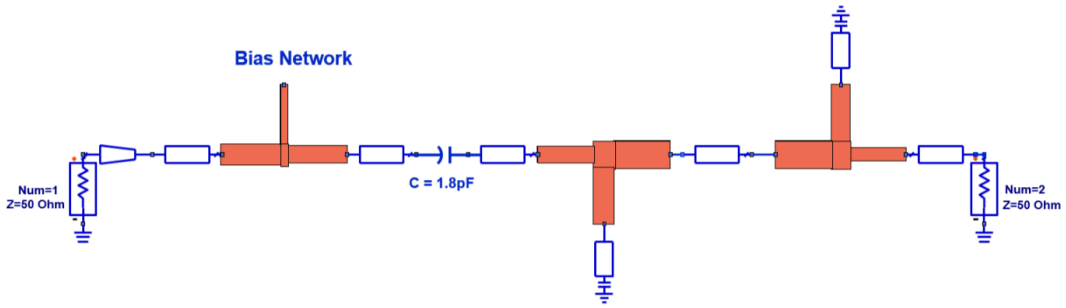


Figure 4.28: Representation of the output matching network, that was optimized in an different way.

4.3.2 Input Matching Network and Stability

As in the single frequency amplifier, the stability analysis and the IMN design were done simultaneously. However, the stability of this PA should be carefully analysed, since this design must remove the RC from the input MN.

Firstly, and like in the first PA, it was added a resistor to the input bias network to solve instability at lower frequencies; Secondly, the IMN was designed to have a forward gain (S_{21}) between 12-13dB; Thirdly, a stability test was performed with the IMN and OMN already designed, where it was verified that the PA was still unstable between 1.5GHz-2.5GHz. In order to overcome this problem the value of the resistor in the bias network was optimize to 39Ω and it was also set a goal to reduce the S_{21} below 8dB for 1.5-2.5GHz. These approaches allowed the stability of the amplifier for a 50Ω load (figure 4.29).

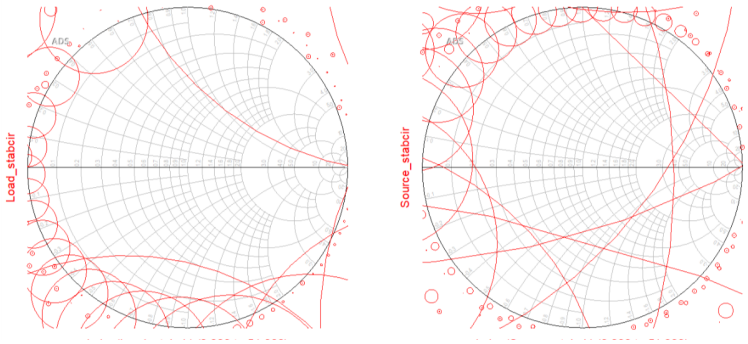


Figure 4.29: Load and source stability circles.

Note that the IMN optimization followed the same reasoning of the OMN, ie, the T-junctions were simulated electromagnetically and then, a final optimization was done adjusting the line lengths. Figure 4.30 presents the final schematic of the IMN.

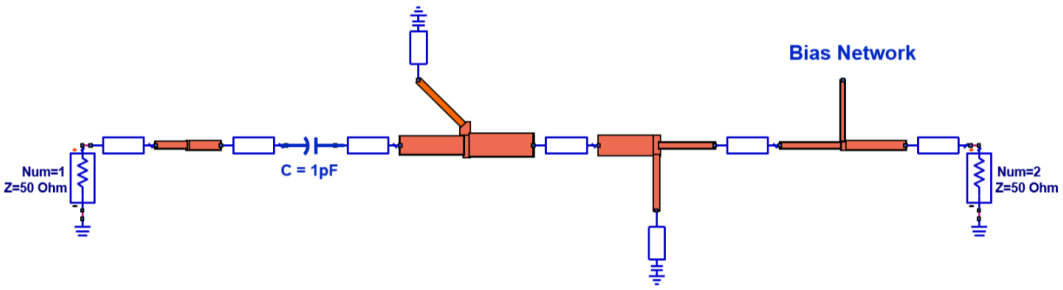


Figure 4.30: Input matching network schematic.

4.3.3 Layout and Electromagnetic Simulation

The purpose of this section is to present the final layout and compare the EM results with the ones obtained in the schematic, in order to verify if the adopted method to approximate the two simulations is satisfactory.

Following the same metrics in terms of layout and calibration of the 9.5GHz PA, the final multiple frequency amplifier is illustrated in figure 4.31.

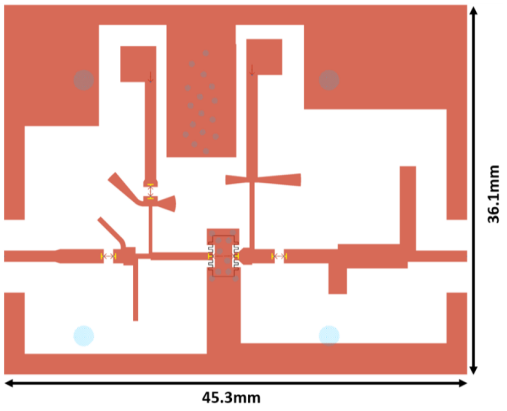


Figure 4.31: Final layout of the multiple frequency amplifier.

Figure 4.32 presents three graphics comparing the results of S_{21}, drain efficiency and output power versus frequency of schematic and EM simulation.

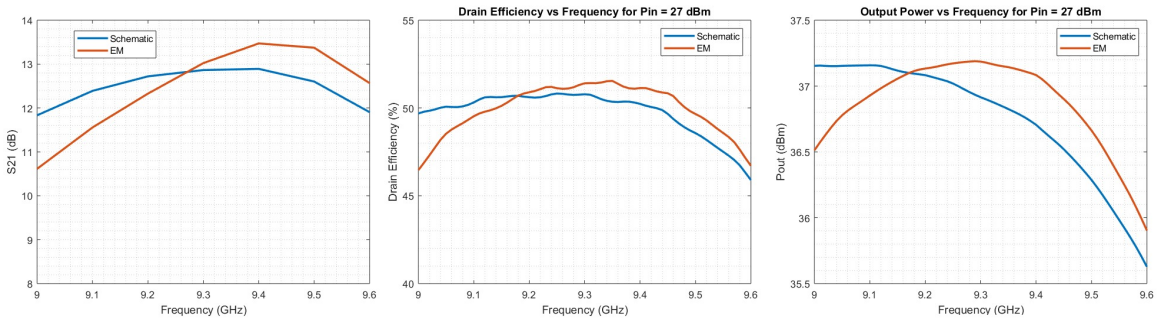


Figure 4.32: Comparison between schematic and EM simulation.

The similarity of the curves proves that the used method is adequate to approximate the schematic to the layout and it also gives "green light" to implement the PA. Figure 4.33 shows the EM gain and drain efficiency results between 9-9.6GHz as a function of output power. Although the variation of the gain with frequency is notorious, the efficiency curves are identical.

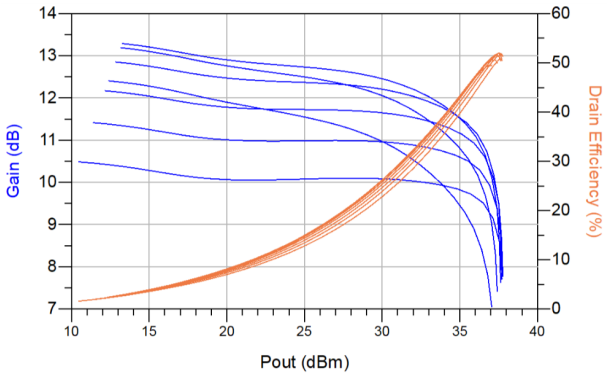


Figure 4.33: Gain and drain efficiency curves as a function of output power from EM simulation.

4.3.4 Experimental Validation

To characterize this amplifier it was used the same setup and methodology of the previous one. The results from CW and pulsed measurements are in the following sections.

CW Characterization

Initially, a small-signal gain analysis was considered. Figure 4.34 compares the measured and simulated curves as a function of frequency.

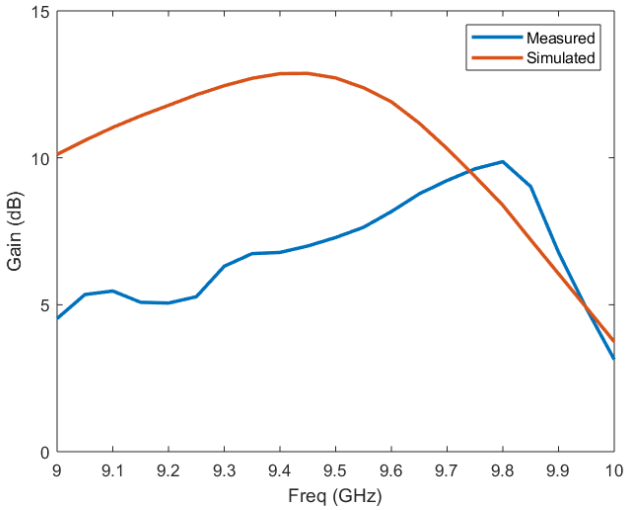
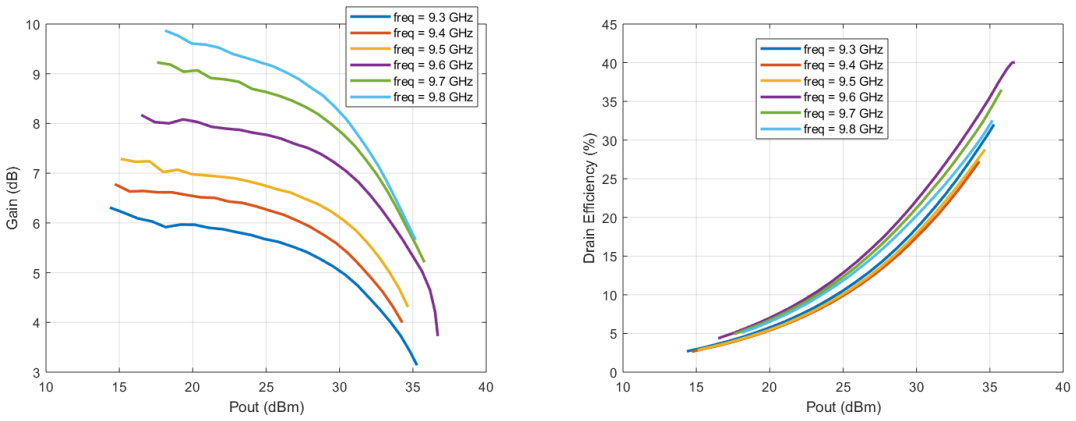


Figure 4.34: Small-signal gain of the multiple frequency PA - from 9 to 10GHz.

The measured curve has a confined band and lower gain when compared with the simulation. Besides that, and as expected, there is a shift of about 400MHz to the right.

After small-signal test, a power-sweep was performed from 9.3GHz to 9.8GHz. The results of gain and drain efficiency as a function of output power are in the following figures, 4.35.



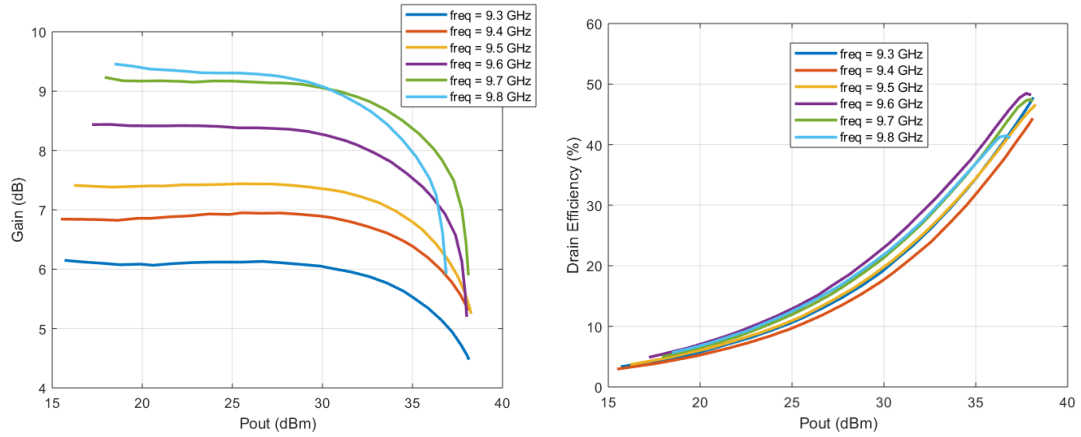
(a) Gain (b) Drain Efficiency

Figure 4.35: Gain and drain efficiency versus output power from 9.3 to 9.8GHz.

Through the previous graphics, it is possible to conclude that for the frequency band of 9.3-9.8GHz a gain between 6.3-9.9dB and a drain efficiency of 27-40% is achieved.

Pulsed Characterization

The gain and drain efficiency curves under pulsed operation are shown in figure 4.36.

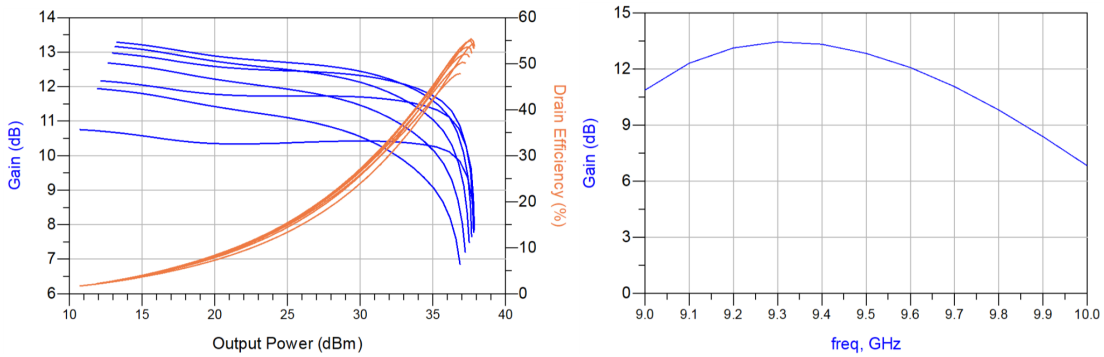


(a) Gain (b) Drain Efficiency

Figure 4.36: (a) Gain and (b) drain efficiency curves versus output power from 9.3-9.8GHz.

Similar to what was observed in the single frequency amplifier: the small-signal gain has similar values on pulsed and CW measurements, but the measured drain efficiency in pulsed mode is much higher than in CW. For a bandwidth of 500MHz (9.3-9.8GHz) it is achieved 6.2-9.5dB and 41.4-48.5% of gain and drain efficiency, respectively.

In order to be able to state that the transistor model is not adequate, the S-parameters of the PA matching networks were measured. With these measurements, a HB simulation was performed, and the results for the frequencies 9-9.6GHz are in the following figure 4.37.



(a) (b)

Figure 4.37: Gain and drain efficiency curves versus output power from 9-9.6GHz (a) and small-signal gain versus frequency (b) - with the measured s-parameters of the MN.

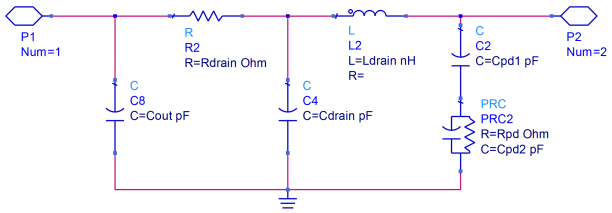
Since the results of figure 4.37 and 4.33 are similar it is now possible to affirm that the transistor model is the cause of the shift in the small-signal gain, and therefore is not correct. Besides this, through the CW and pulsed measurements of the previous amplifiers it can be concluded that the transistor model does not represent well the thermal phenomena. This problem leads us to next section: PA design based on S-parameters.

4.4 PA Design Based on S-Parameters

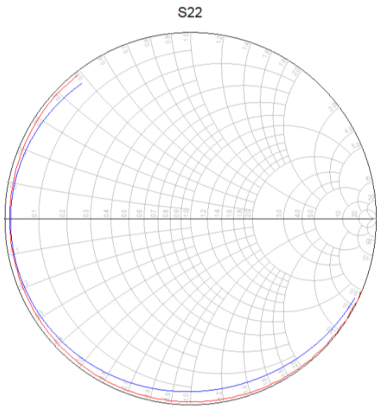
As mentioned before, the transistor model given by the manufacturer is not accurate enough, resulting in different performance when compared with the measurements. Due to time limitation, extracting a complete non-linear model was not an option. Instead, with the help of the RF group modelling experts, it was possible to extract the output device's extrinsic elements (including the output capacitance, Cout, which is the representation of the C_{ds} in parallel with C_{gd}). With this we can move from the extrinsic to the device's intrinsic reference plane, determining the optimum impedance for the PA design.

The equivalent circuit of the extrinsic elements is depicted in figure 4.38(a). To extract their values a set of S-parameters were measured from the device for several bias points: V_{GS}=-5V (i.e., cut off zone) with V_{DS} = 0, 1, 2, 3, 6, 10, 20, 30, 40 V and, by fitting the S_{22} of the circuit when the port one is open to the measured S_{22}, considering that Cout is the only element that is changing with the bias. Fig 4.38(b) shows the obtained fit for the bias V_{GS} = -5V and V_{DS} = 40V. The several measurements made for different V_{DS} were intended to check if the Cout profile is reasonable, giving more confidence in the extraction process.

In fact, a better approach as the one proposed in [51] would lead to a better model. There, two-port measurements are used, in which the FET is biased with a V_{GS} much higher than V_T (producing a virtual short-circuit in the channel) and a V_{GS} lower than V_T (where the channel is an open) with V_{DS} = 0. This gives extra information, being possible to extract better the series and parallel elements independently. Despite this, the model proved to be a good estimate, since it allowed (as we shall see further) to obtain satisfactory results.



(a)



(b)

Figure 4.38: (a) Extrinsic model created, which the values of its components were obtained by (b) fitting the S_{22} of the circuit (at blue) to the S_{22} measurements (at red) for a V_{GS} = -5V and V_{DS} = 40V.

With this circuit, the OMN was projected in order to achieve the efficiency optimum loads between 9-9.6GHz and at the same time to ensure stability between 1-2.5GHz (which as seen previously is the problematic range).

The IMN was projected with the measured S-parameters of the transistor for the used bias point. The IMN was optimized to achieve a gain of about 11.5dB with a ripple lower than 1dB for the frequency band considered. After that, some adjustments were made on the resistor of the bias network to ensure stability.

Then, the layout was created in order to proceed to implementation, figure 4.39.

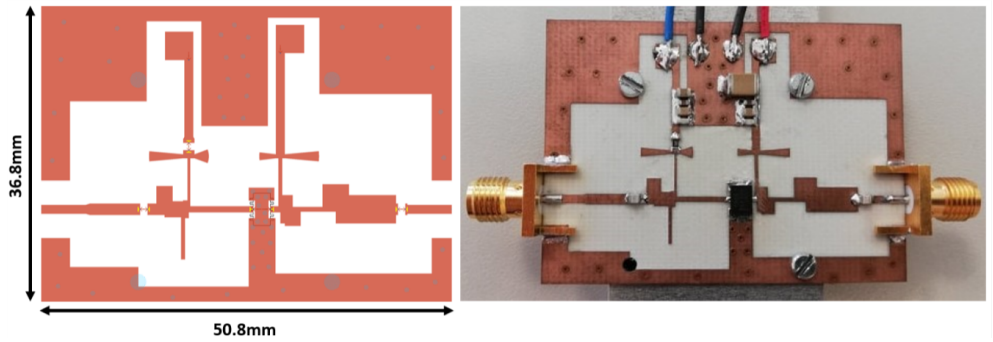


Figure 4.39: PA layout and its implementation.

4.4.1 Experimental Validation

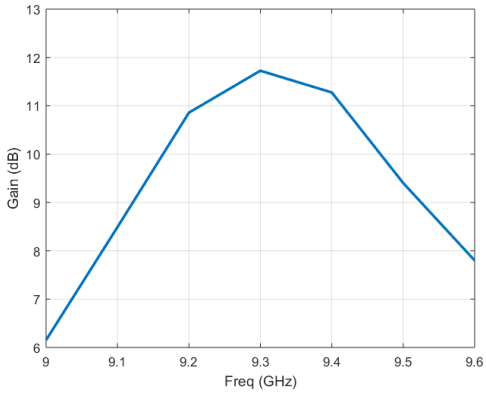
Finally, it was necessary to verify the veracity of the used method to design a PA, therefore pulsed measurements were performed in order to characterize it. In figure 4.40(a) it is possible to observe the small-signal gain is in accordance with the simulations, in frequency terms, which means that there is no shift as before. However, the values obtained are lower than the projected ones, mainly for the edge frequencies (9GHz and 9.6GHz). These lower values may be the consequence of differences between simulation and implementation.

In figure 4.40(b) it can be seen that the maximum drain efficiency is always above 50%, except for 9.5-9.6GHz frequencies because it was not possible to guarantee the optimum impedance, as desired. At 9.3GHz are reached the best results: it is achieved a drain efficiency of 55%, while the small-signal gain is 11.7dB.

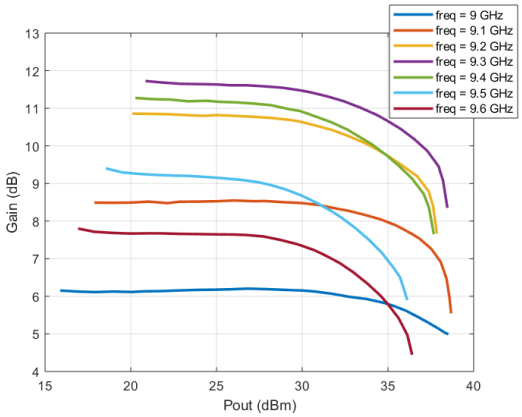
Comparing these results with the previous multiple frequency amplifier, a performance improvement is notorious, in all aspects, which can be observed in figure 4.41. Besides the fact that simulation and measurements are now consistent (in frequency), it is also concluded that:

- The bandwidth of the PA increased 100MHz - being now 600MHz;
- The small-signal gain increased from 6.2-9.5 dB to 6.2-11.7 dB;
- Maximum drain-efficiency increased from 41-49 % to 41-55%.

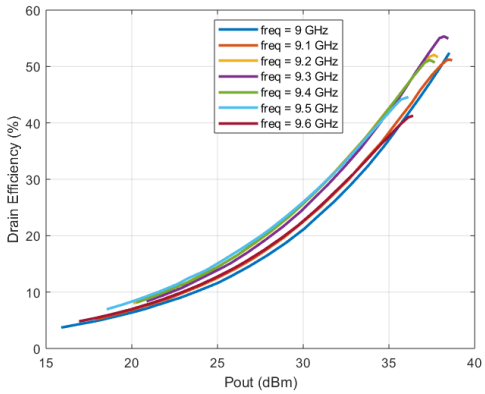
The great improvement in PA performance compared to the previous one allow to conclude that the created circuit is suitable for the PA design.



(a) Small-signal Gain Comparison



(b) Gain



(c) Drain Efficiency

Figure 4.40: (a) Small-signal gain versus frequency; (b) Gain and (c) drain efficiency curves versus output power from 9-9.6GHz.

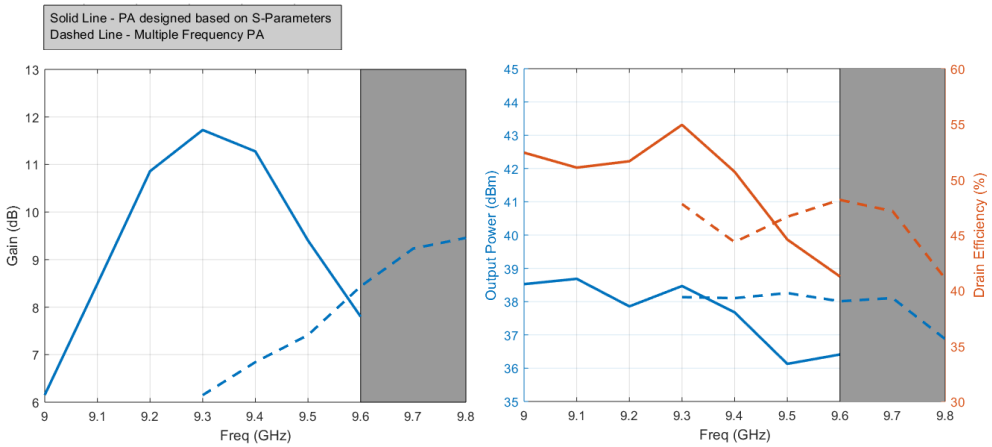


Figure 4.41: Comparison of small-signal, drain efficiency and Pout between PA designed based on the S-parameters and the multiple frequency PA. 9 to 9.6GHz is the desired frequency band.

Chapter 5

Conclusions

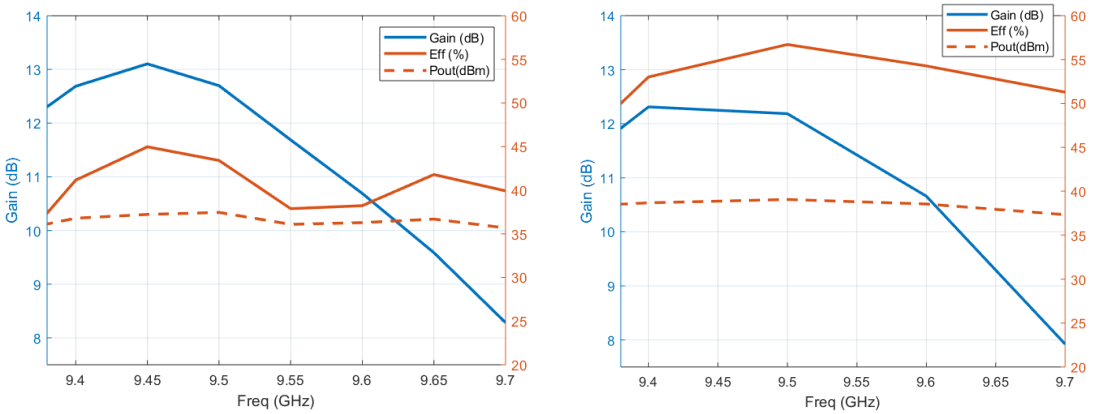
5.1 Discussion and Final Remarks

The focus of this work was to study, design and implement a power amplifier for frequencies in the X band, specifically, for the frequency range of 9 to 9.6GHz. To accomplish this objective, the first step was to understand the behaviour of some passive elements at these frequencies. For this, several test boards were implemented in order to characterize the substrate, via holes, connectors and capacitors. This first approach to high frequencies, although simple, allowed to tune the simulation process to the measurements and to conclude that passive elements will not be the main cause of problems for a power amplifier design around 9GHz. After this analysis, two PAs were projected and implemented: a single frequency (central frequency: 9.5GHz) and a multiple frequency (9-9.6GHz) PA.

When designing the single frequency PA it was verified that a RC circuit was required to guarantee unconditional stability. However, due to the fact that there were some suspicions about the behaviour of the resistor at the considered frequencies, a second PA (multiple frequency) without the RC was projected. In this case, the matching networks were carefully optimized in order to ensure (conditional) stability. For time constraints reasons the PAs had to be simultaneously implemented.

In the end, it was verified that the RC of the IMN had impact on the results, but this was not the only flaw detected: the transistor model also proved to be inaccurate.

Despite the shortcomings of the IMN and the transistor model, these two problems were mutually cancelled, and therefore the obtained results for the single frequency PA were coherent with the ones projected. In figure 5.1, it can be seen the gain, output power and drain efficiency versus frequency, for CW and pulsed mode operation.

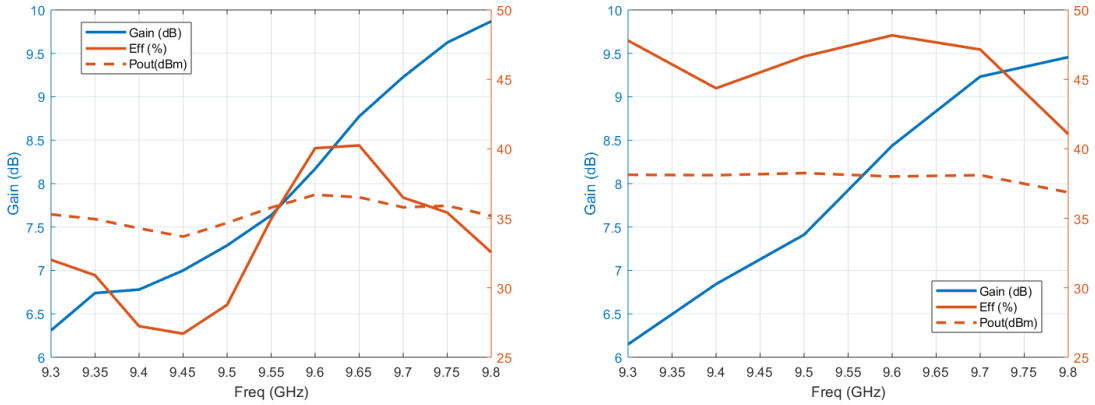


(a) CW operation (b) Pulsed operation

Figure 5.1: Results of drain efficiency, gain and output power versus frequency for the "single frequency" amplifier - under CW and pulsed signal.

Through the two graphics, it is observed that pulsed mode operation allows to achieve a higher output power, contributing to a greater efficiency. In fact, there is an increase of more than 10% in pulsed measurements efficiency comparing to the CW operation. For 300MHz of bandwidth a drain efficiency between 51.5-56.5% is achieved (pulsed measurements).

The multiple frequency amplifier was projected without the RC circuit and with the original model, therefore the implementation of this amplifier allowed to make important conclusions: verify that the problem of the IMN was on the RC circuit; confirm that the transistor model is not accurate; and to improve the design and simulation process at high frequencies. Although it is not possible to quantitatively compare the measured results with simulation, since there is a shift in frequency of about 400MHz (due to the inaccuracy of the transistor model), it was achieved, for 500MHz of bandwidth, a gain of 6.3-9.9dB and a drain efficiency between 27-40% and 41-48.5% for CW and pulsed signal, respectively, figure 5.2.



(a) CW operation (b) Pulsed operation

Figure 5.2: Results of drain efficiency, gain and output power versus frequency for the multiple frequency amplifier - under CW and pulsed signal.

The fact that the transistor model is not accurate enough led to make a new approach to design an amplifier. It was extracted the output device's extrinsic elements (based on S-parameters measurements), thus it was possible to move from the extrinsic to the device's intrinsic reference plane, determining the optimum impedance for the PA design. With this circuit, a new PA was projected for the frequency band of 9-9.6GHz.

The results of this amplifier in pulsed mode operation are in figure 5.3 as a function of frequency. As we can see, there is agreement, in frequency terms, between simulation and measurements. Although the IMN was designed so that the amplifier had a small-signal gain around 11.5dB for the frequency band considered, the results mainly for the "edge" frequencies are considerably lower. Differences between simulation and measurements of the matching networks may be the cause of lower gain.

In this amplifier, the lines of the MNs are much wider (as we could see in figure 4.39) than in the previous PAs. Despite this, it was made the same analysis to the matching networks, which may have been an error, since there are more discontinuities that can lead to greater differences between simulation and implementation, and therefore, may be the cause of lower gain. In this way, the analysis of the MNs should have been more detailed in order to understand if the increase of the line widths causes problems or not.

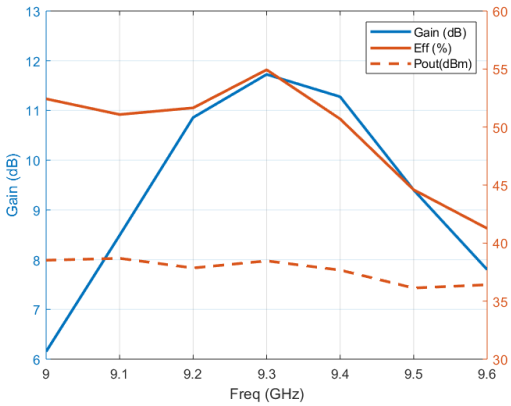


Figure 5.3: Results of drain efficiency, gain and output power versus frequency for PA designed with an extrinsic model - under pulsed signal.

Nevertheless, for 600MHz of bandwidth it is achieved a drain efficiency between 41-55% and a small-signal of 6.2-11.7dB. With these results and comparing with the ones obtained for the "Multiple Frequency" PA it is possible to conclude that there is a considerably improvement of the performance, besides there is no longer frequency deviation in the small-signal gain.

Despite the detected problems, the initial goal of this dissertation was fulfilled, therefore the final step is to compare the obtained results with the state-of-the-art. For this purpose, table 5.1 was elaborated:

	BW (GHz)	**Gain (dB)**	**η/PAE (%)**	**Operation**	**Transistor**
This Work,4.2	9.4-9.8	8-13 8-12.3	38-45 / 21-38 51-57 / 33-49	CW pulsed	CGHV1F006S
This Work,4.3	9.3-9.8	6-9.8 6.2-9.5	27-40 / 16-27 41-49 / 29-37	CW pulsed	CGHV1F006S
This Work,4.4	9-9.6	6.5-12 6.2-11.7	26-44 / 14-34 41-55 / 27-48	CW pulsed	CGHV1F006S
[38]	8.5-9.6	14.5	52 / x	pulsed	CGHV1F006S
[52]	8.7-10.2	x	x / 35	x	CGHV1F006S
[53]	4-8.4	7.6-9.4	x / 26-43	CW	CGHV1F006S
[54]	9.3-9.4	10	x / 44.4	CW	FSX027WF

Table 5.1: Comparison of the produced power amplifiers with other works in literature.

Analysing the previous table we can conclude that the performance of the developed amplifiers is highly competitive in comparison to the work of others.

All the work done throughout the semester, from the theoretical study, schematic simulations, implementation, laboratory test to the final results analysis, allowed to acquire, progressively, a great amount of knowledge and to conclude the following points, that can be understood as advice for those who wish to design PAs using ADS at high frequencies:

- The (total) schematic simulation at frequencies above 9GHz is not trustable, since the equivalent circuit of some components such as *mtaper*, *mcros* and *mtee* differ considerably from the layout. To solve this, the referred components were EM simulated and then, a new optimization was done adjusting the line lengths - This adopted strategy proved to be effective;
- Resistors should be avoided (in the RF path) due to their associated parasites that are often not well contemplated in simulation;
- The model of the used transistor proved not be accurate and besides that, it is necessary to take into account the source inductance underneath the pad;
- The used transistor suffers of thermal effects, which affect significantly the amplifier performance. For this reason PAs should be characterized under pulsed operation, instead of CW.

5.2 Future Work

In an attempt to continue this work, which means, using the same frequency range and the same transistor, in the author's perspective, the first step to take would be to carefully analyse the matching networks of the last PA in order to investigate the cause of lower gain. Solved this problem, there are some suggestions as future work, that would make sense to be carried out in the following order:

1. Study how variations of the layout in which the transistor is placed affect the model and the performance of the PA. For example, increase the number of via holes underneath the transistor and check its behaviour. In this way, the implementation could not be done locally, in the Instituto de Telecomunicações, due to the limitations of the printing machine.

2. Extract a complete non-linear model of the transistor. For this, besides all the theoretical study required, a great amount of measurements would have to be made to the transistor, namely: S-parameters, IV-curves and large signal measurements.

3. Move to an architecture that could improve efficiency, such as Doherty architecture. This would be a challenging choice at these frequencies.

Bibliography

[1] Jeffrey G Andrews, Stefano Buzzi, Wan Choi, Stephen V Hanly, Angel Lozano, Anthony CK Soong, and Jianzhong Charlie Zhang. What will 5g be? *IEEE Journal on selected areas in communications*, 32(6):1065–1082, 2014.

[2] Ltd Huawei Technologies Co. 5g network architecture - a high-level perspective. Available: `https://www.huawei.com/minisite/hwmbbf16/insights/5G-Nework-Architecture-Whitepaper-en.pdf`. Accessed: 2019-06-12.

[3] IMT-2020 (5G) Promotion Group. 5g concept. 2015.

[4] Qorvo. Getting to 5g: Comparing 4g and 5g system requirements. Available: `https://www.qorvo.com/design-hub/blog/getting-to-5g-comparing-4g-and-5g-system-requirements`. Accessed: 2019-06-12.

[5] IMT-2020 (5G) Promotion Group. 5g wireless technology architecture. 2015.

[6] PIC Wire & Cable. Pic micromates x and ku band cable assemblies. Available: `https://www.picwire.com/cables/micro-mates/`. Accessed: 2019-04-26.

[7] L. Liu, S. Men, M. Liu, and B. Zhou. An energy saving solution for wireless communication equipment. In *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, pages 1–3, Sep. 2014.

[8] David M Pozar. *Microwave Engineering: Microwave Amplifier Design*. John Wiley & Sons, Inc, 2012.

[9] J.C. Pedro and N.B Carvalho. *Intermodulation Distortion in Microwave and Wireless Circuits*. Artech House, 2003.

[10] Herbert L Krauss, Charles W Bostian, and Frederick H Raab. *Solid State Radio Engineering*. John Wiley & Sons Inc, 1980.

[11] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge. The class-e/f family of zvs switching amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 51(6):1677–1690, June 2003.

[12] E. Frank. *Radio Frequency Integrated Circuits and Technologies*. Springer, 2 edition, 2008.

[13] S. C. Cripps. *RF Power Amplifiers for Wireless Communications*. Artech House, 2006.

[14] Elisa Cipriani, Paolo Colantonio, Franco Giannini, and Rocco Giofre. *The Switched Mode Power Amplifiers*. 03 2010.

[15] M.K. Kazimierczuk. *RF Power Amplifiers*. John Wiley & Sons, 2 edition, 2015.

[16] Frederick H Raab, Peter Asbeck, Steve Cripps, Peter B Kenington, Zoya B Popovic, Nick Pothecary, John F Sevic, and Nathan O Sokal. Power amplifiers and transmitters for rf and microwave. *IEEE transactions on Microwave Theory and Techniques*, 50(3):814–826, 2002.

[17] P. Reynaert and M. Reynaert. *RF Power Amplifiers for Mobile Communications*. Springer, 2006.

[18] Qorvo. Model-based gan pa design basics: What's in an i-v curve? Available: `https://www.qorvo.com/design-hub/blog/model-based-gan-pa-design-basics-whats-in-an-iv-curve`. Accessed: 2019-05-13.

[19] John Hoversten, Michael Roberg, and Zoya Popović. Harmonic load pull of high-power microwave devices using fundamental-only load pull tuners. In *75th ARFTG Microwave Measurement Conference*, pages 1–4. IEEE, 2010.

[20] Agilent Technologies. Understanding the fundamental principles of vector network analysis. Available: `http://anlage.umd.edu/Microwave%20Measurements%20for%20Personal%20Web%20Site/Agilent%20Fundamentals%20of%20Network%20Analysis%205965-7707E.pdf`. Accessed: 2019-05-29.

[21] ISO 17511 International Organization for Standardization. In vitro diagnostic medical devices - measurement of quantities in biological samples - metrological traceability of values assigned to calibrators and control materials. Available: `https://www.sis.se/api/document/preview/904066/`. Accessed: 2019-05-13.

[22] Anritsu. Understanding vna calibration. Available: `http://anlage.umd.edu/Anritsu_understanding-vna-calibration.pdf`. Accessed: 2019-03-11.

[23] Keysight Technologies. Trl calibration. Available: `http://na.support.keysight.com/vna/help/latest/S3_Cals/TRL_Calibration.htm#4Port`. Accessed: 2019-05-09.

[24] J.C. Pedro. Rf power amplifier linearity and efficiency enhancement techniques. 2013.

[25] L. R. Kahn. Single-sideband transmission by envelope elimination and restoration. *Proceedings of the IRE*, 40(7):803–806, July 1952.

[26] Chi-Tsan Chen, Yi-Chieh Lin, Tzyy-Sheng Horng, Kang-Chun Peng, and Chien-Jung Li. Kahn envelope elimination and restoration technique using injection-locked oscillators. In *2012 IEEE/MTT-S International Microwave Symposium Digest*, pages 1–3. IEEE, 2012.

[27] Frederick H Raab. High-efficiency linear amplification by dynamic load modulation. volume 3, pages 1717–1720. IEEE, 2003.

[28] William H Doherty. A new high efficiency power amplifier for modulated waves. *Proceedings of the Institute of Radio Engineers*, 24(9):1163–1182, 1936.

[29] Henry Chireix. High power outphasing modulation. *Proceedings of the Institute of Radio Engineers*, 23(11):1370–1392, 1935.

[30] W. Zhancang. *High Efficiency Load Modulation Power Amplifiers for Wireless Communications*. Artech House, 2017.

[31] Bumman Kim, Youngoo Yang, Jaehyok Yi, Joongjin Nam, Young Yun Woo, and J Cha. Efficiency enhancement of linear power amplifier using load modulation technique. In *Int. Microwave and Optical Technology Symp. Dig*, pages 505–508, 2001.

[32] Harold M. Edwards. *Linear Algebra*. Birkhäuser Basel, 1995.

[33] I. Bahl. *Fundamentals of RF and Microwave Transistor Amplifiers*. John Wiley & Sons, 2009.

[34] G. Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design*. E. Svendsen, R. Kernan, and K. Cassino, Eds. Upper Saddle River, New Jersey: Prentice-Hall, 2 edition, 1996.

[35] Marion Lee Edwards and Jeffrey H Sinsky. A new criterion for linear 2-port stability using a single geometrically derived parameter. *IEEE Transactions on microwave theory and techniques*, 40(12):2303–2311, 1992.

[36] Rogers Corporation. Ro4000 series high frequency circuit materials. Available: `http://www.rogerscorp.com/documents/726/acs/RO4000-Laminates-RO4003C-and-RO4350BData-Sheet.pdf`. Accessed: 2019-02-10.

[37] Anritsu. Universal test fixture 3680 series. Available: `https://dl.cdn-anritsu.com/en-us/test-measurement/files/Brochures-Datasheets-Catalogs/datasheet/11410-00024F.pdf`. Accessed: 2019-02-26.

[38] Cree. Cghv1f006s, 6w, dc-15ghz, 40v, gan hemt. Available: `https://www.wolfspeed.com/media/downloads/421/CGHV1F006S.pdf`. Accessed: 2019-01-23.

[39] FM Ghannouchi and MS Hashmi. Load-pull techniques and their applications in power amplifiers design. In *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pages 133–137. IEEE, 2011.

[40] American Technical Ceramics (ATC). Atc 800 a series npo ceramic, high rf power ultra-low esr multilayer capacitors. Available: `http://www.atceramics.com/UserFiles/800a.pdf`. Accessed: 2019-05-29.

[41] Multicomp. Surface mount resistor kit 0603 case size. Available: `http://www.farnell.com/datasheets/1895129.pdf?_ga=2.103667077.465644510.1559304483-1385427558.1559304483`. Accessed: 2019-05-29.

[42] Keysight EEsof EDA. Recommendations for port setup when using ads momentum and modelithics models. Available: `http://literature.cdn.keysight.com/litweb/pdf/5992-0415EN.pdf`. Accessed: 2019-03-10.

[43] Rhode and Schwartz. Microwave signal generator - operating manual. Available: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_manuals/gb_1/s/smr_1/smr_20-40.pdf. Accessed: 2019-04-30.

[44] Keysight Technologies. N6700 modular power system family. Available: https://literature.cdn.keysight.com/litweb/pdf/5992-1880EN.pdf?id=2798814. Accessed: 2019-04-30.

[45] Mini-Circuits. Coaxial high power amplifier zve-3w-183+. Available: https://ww2.minicircuits.com/pdfs/ZVE-3W-183+.pdf. Accessed: 2019-03-15.

[46] Pasternack. Isolator with 20db isolation from 7ghz to 12.4ghz, 50watts and n female. Available: https://www.pasternack.com/images/ProductPDF/PE8313.pdf. Accessed: 2019-06-14.

[47] HP Hewlett Packard. Hp435a, hp436a, hp437a, hp438a power meters. Available: http://www.testequipmentdepot.com/usedequipment/pdf/430seriesnp.pdf. Accessed: 2019-05-25.

[48] Keysight Technologies. M8190a arbitrary waveform generator. Available: http://literature.cdn.keysight.com/litweb/pdf/5990-7516EN.pdf. Accessed: 2019-06-8.

[49] Keysight Technologies. E8267d psg vector signal generator. Available: https://literature.cdn.keysight.com/litweb/pdf/5989-0697EN.pdf?id=473817. Accessed: 2019-06-8.

[50] Keysight Technologies. Uxa x-series signal analyzer, multi-touch n9041b. Available: https://literature.cdn.keysight.com/litweb/pdf/5992-1822EN.pdf?id=2792918. Accessed: 2019-06-8.

[51] Gilles Dambrine, Alain Cappy, Frederic Heliodore, and Edouard Playez. A new method for determining the fet small-signal equivalent circuit. *IEEE Transactions on microwave theory and techniques*, 36(7):1151–1159, 1988.

[52] Cai Wei-bo, Zhang Xiao-fa, and Yuan Nai-chang. Design of an x-band gan high power amplifier. In *2016 IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, volume 1, pages 147–149. IEEE, 2016.

[53] Stefan May, Daniel Maassen, Felix Rautschke, and Georg Boeck. Two stage 4–8 ghz, 5 w gan-hemt amplifier. In *2017 47th European Microwave Conference (EuMC)*, pages 136–139. IEEE, 2017.

[54] LiXia Hu, Kewei Qian, and Boming Wang. Research of high efficiency x-band power amplifier. In *2015 8th International Symposium on Computational Intelligence and Design (ISCID)*, volume 1, pages 129–132. IEEE, 2015.