A 0.45 V low power high PSRR subthreshold CMOS voltage reference

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Abstract

Voltage references are broadly used in analog and digital systems to generate a DC voltage independent of process, supply voltage and temperature (PVT) variations. Conventional band gap references (BGR) add the forward bias voltage across a PN junction with a voltage that is proportional to absolute temperature to produce an output that is insensitive to changes in temperature. BGRs generate a nearly temperature independent reference, of about 1.25 V, and therefore they require a higher supply voltage, which might not meet the low voltage constraints for low-power applications such as passive RFID's, wearable and implantable medical devices. Also, BGRs use resistors that need more area on silicon. One possible solution to meet the low power requirement is to operate MOSFETs in subthreshold region. Most often, forward biased PN-junctions of BGRs are substituted with MOSFETs biased in the subthreshold region and achieves a supply voltage down to 0.6 V.

This paper presents a sub-1V voltage reference circuit that has only MOS transistors, all working in subthreshold region with a supply voltage down to 0.45 V and a supply current of 1nA at room temperature for ultra-low power applications. The circuit is designed and simulated in 0.13um technology.

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Symbols	Definitions
μ_n, μ_p	Carrier mobility of electrons and holes respectively
ϵ	Permittivity
D_n, D_p	Diffusion coefficients of electrons and holes, respectively
E_G	Bandgap energy
k	Boltzmann constant
L_n, L_p	Minority carrier electron and hole diffusion length respectively
N_D, N_A	Donor and acceptor concentrations at the n side and p side, respectively
q	Elementary charge
n_i	Intrinsic carrier concentration in the semiconductor material
n_p	Equilibrium concentration of electrons in p-type material
p_n	Equilibrium concentration of electrons in n-type material
T	Absolute temperature

Chapter 1

Introduction

Reference circuits are ubiquitous in modern circuit design. Ranging from regulators to analog-to digital converters, it is hard to find a block that does not use a reference voltage or current to set up its operating point [1]. The major goal of any reference circuit is to provide as constant a voltage and/or current as possible, irrespective of changes in the process or environment. Most metrics, such as line sensitivity and variation with process depend strongly on circuit implementation, and thus must be discussed in the context of a particular implementation. However, temperature variation is much more fundamentally related to the choice of topology, and less so with the exact implementation.

With multiple circuit blocks on a modern System on Chip (SoC) circuit, it becomes valuable to build a separate reference block that supplies references to all the other blocks on the chip. This way, the power and area cost of generating an accurate reference voltage is restricted to a single block.

However, with the recent advent of massive SoC designs, this has become harder and harder to do. The largest systems have many different circuit blocks, each with some combination of specifications, which may be mutually incompatible. There can be multiple modes of operation, each with a different set of requirements. Therefore, it

has become valuable to develop a reference block that can accommodate many different sets of specifications, and has multiple power/operation modes.

In this thesis, to address the need of low voltage and low power operation demanded by battery powered circuits, we propose a topology that generates a reference voltage based on the difference in threshold voltage of two transistors. The proposed reference uses a unique two stage architecture, with the first stage acting as a power supply for the second stage by functioning as a coarse reference. This helps us achieving high power supply rejection ratio (PSSR). Rest of the thesis is structured as follows:

- Chapter 2 starts with the first known voltage reference in the history followed by bandgap circuit concept published by Hilbiber, where the voltage variation of a silicon diode as function of temperature was obtained. Afterwards, following the evolution of the bandgap references, the most efficient circuit configurations demonstrated by Widlar and Brokaw are explained. Then, different elements were used in the same circuit to realize the effects in terms of area, power consumption, stability and factors referred. Finally, two actual models of bandgap references will be presented, each one with different structures and using different elements.

- In chapter 3, the implementation of each part of the proposed circuit is explained. Firstly, the fundamental part of the circuit (Reference Voltage Generator), then the self-biasing structure is added to the circuit to obtain a current generator and then the simulation results are shown. Finally, the complete proposed circuit which includes a pre-regulator block with simulations results are presented.

- In chapter 4, we outline the key specifications and the advantages of the proposed voltage reference over traditional architectures. After the conclusion, it is possible to consider a couple of improvements to modify the circuit configuration to obtain a better performance in a future work.

- Chapter 5 concludes our experimental results and shows future enhancements.

Chapter 2

Background and Motivation

This chapter covers the history of voltage references. We begin with describing earliest known voltage reference then how it's evolved over time.

2.1 Origin of Voltage Reference

The earliest voltage references were wet-chemical cells such as the Clark cell and Weston cell, which are still used in some laboratory and calibration applications.

The Clark cell was invented by English engineer Josiah Latimer Clark in 1873. It is basically a bettery and produced a highly stable voltage [2]. It was later supplanted by Weston cell which produced a constant voltage output of 1.019 volt and was virtually independent of temperature change.

With the advent of semiconductor devices, voltage references started taking a new form: the first milestone for a semiconductor-based reference was the introduction of the zener diode in the late 1950s [5]. Then, in 1964 Hilbiber described the evolution of a new reference voltage source with magnitude and stability comparable to the Weston standard cell. He built a prototype system that showed a nominal ouput of 1.2567 volt and maintained with a 10 μV envelope for over 12,000 hours [6].

Hilbiber's circuit works as follows: For an ideal p-n junction, the forward voltage,

V_F, and its temperature dependence, dV_F/dT, are a function of current density and the junction impurity profile. This is given by Shockley's equation:

$$p_n \simeq \frac{n_i^2}{N_D} \text{ and } n_p \simeq \frac{n_i^2}{N_A}$$

$$I = I_s \left[exp\left(\frac{qV}{kT}\right) - 1 \right] \tag{2.1}$$

Where I_s is the junction saturation current given by

$$I_s = q\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right) \tag{2.2}$$

Where V is the applied voltage and other parameters have their usual meanings. The temperature dependence of I_s is given by

$$I_s = qn_i^2 \tag{2.3}$$

$$= q\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right) \tag{2.4}$$

$$\text{where } n_i^2 = C_oT^3 exp\left(\frac{-E_G}{kT}\right) \tag{2.5}$$

$$\tag{2.6}$$

Thus,

$$I_s \simeq C_1T^{\beta_p} exp\left(\frac{-E_G}{kT}\right) \tag{2.7}$$

for a p^+n junction, and

$$I_s \simeq C_2T^{\beta_n} exp\left(\frac{-E_G}{kT}\right) \tag{2.8}$$

for an n^+p junction. β is a constant that takes into consideration the approximate temperature dependence of the diffusion coefficients and diffusion lengths. Unfortunately, the ideal behavior is not observed for single Ge or Si junctions at normal temperatures. It has been observed, however, that Equation 2.1 accurately describes the base-emitter voltage of a transistor as a function of collector current [6].

Then from Equations 2.1 and 2.2, it is possible to express V_{BE} in a Taylor's series expansion, as shown in Equation 2.9

$$V_{BE} = \frac{kT_o}{q}\left\{ ln\frac{I_C}{I_S(T_o)} + \left[ln\frac{I_C}{I_S(T_o)} - \left(\beta + \frac{E_{Go}}{kT_o}\right)\right]\left(\frac{T}{T_o} - 1\right) \right.$$
$$\left. - \frac{\beta}{2}\left(\frac{T}{T_o} - 1\right)^2 + ... + \frac{\beta(-1)^{n-1}}{n(n-1)}\left(\frac{T}{T_o} - 1\right)^n + ...\right\} \quad (2.9)$$

$$V_{BE} > \frac{4kT}{q} \text{ and } T < 2T_o$$

This equation 2.9 provides a considerable insight into the low-frequency, low-level behavior of V_{BE}. It is seen that as junction doping density is increased, V_{BE} increases and dV_{BE}/dT becomes less negative. An increase of current density also has the same effect. The curves of Figure 2.1 and Figure 2.2 demonstrate this behavior for the 2N917 and 2N1893 transistors from Fairchild. Although V_{BE} and dV_{BE}/dT are shown as a function of emitter current, if the current gain is sufficiently high, $I_B << I_C$, and the series expansion can be used with I_E substituted for I_C. The circuit of the reference voltage source is shown in Figure 2.3.

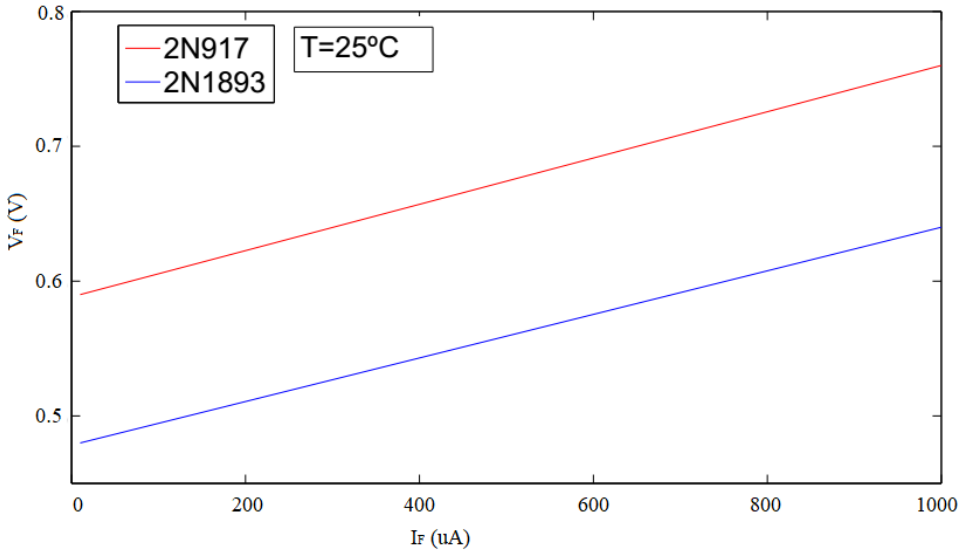

Figure 2.1: Forward voltage Vs current for the transistor quasi-diode [6]

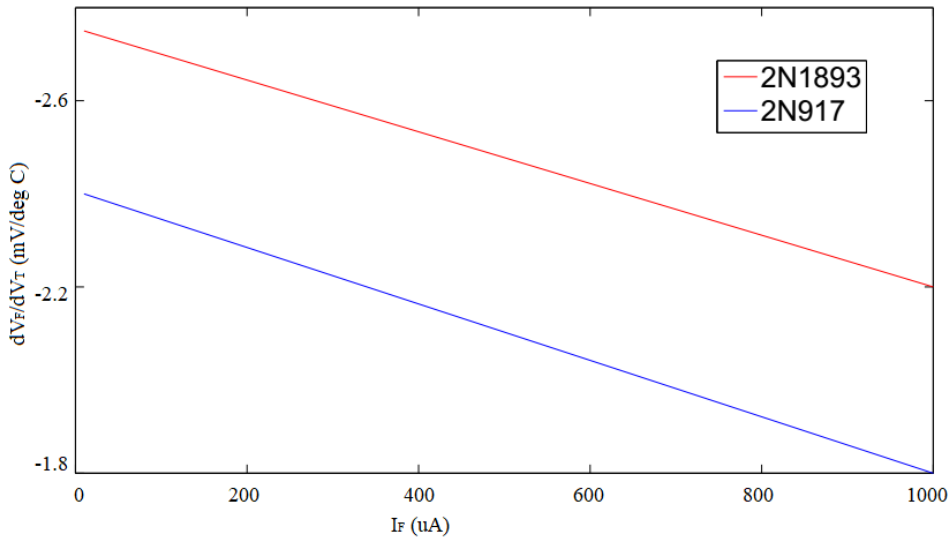

Figure 2.2: The temperature dependence of forward voltage Vs current for the quasi-diode [6]

if m quasi-diodes of type I and r of type II are used, and r-m=1, then the general output voltage is given by the equation 2.10 and equation 2.11 shows the output voltage with the first order temperature dependence eliminated.

$$V_{OUT} = \frac{kT_o}{q}\left[\theta + \left(\theta - \phi - \frac{E_{G0}}{kT_o}\right)\left(\frac{T}{T_o} - 1\right) - \frac{\phi}{2}\left(\frac{T}{T_o} - 1\right)^2\right] \tag{2.10}$$

$$\theta = r.ln\frac{I_{C2}}{I_{S2}(T_o)} - m.ln\frac{I_{C1}}{I_{S1}(T_o)}$$

$$\phi = r\beta_{II} - m\beta_I$$

$$V_{OUT} = E_{G0} + \phi\frac{kT_o}{q}\left[1 - \frac{1}{2}\left(\frac{T}{T_o} - 1\right)^2\right] \tag{2.11}$$

Here, the third and higher order terms are not included, since for $|T - T_o| < 50^oC$, their contribution to the output voltage is less than 20 μV. By choosing the relationship

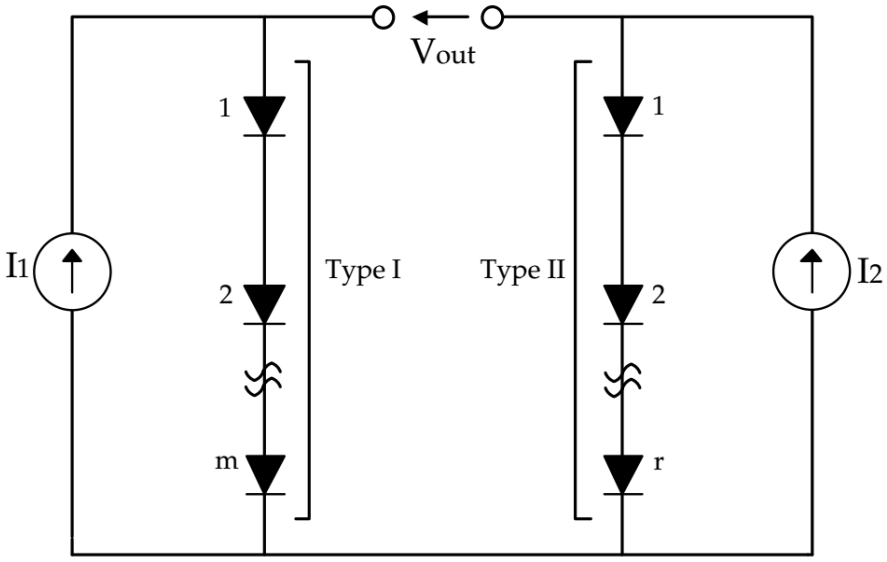

Figure 2.3: The basic circuit of Hilbiber′s reference voltage source [6]

between θ and ϕ as shown in equation 2.12, It is possible to eliminate the main source of temperature dependence.

$$\theta = \phi + \frac{E_{GO}}{kT_o} \tag{2.12}$$

The long-term stability of the voltage source using the 2N917 and the 2N1893 is of the order of 3 to 5 ppm. This figure arises primarily from variations of the zener diode in the current source network, which has a stability of about 150 to 200 ppm. Many variations of the basic circuit are possible, including the use of diodes fabricated from other semiconductors such as germanium or gallium arsenide. However, it has not been possible to demonstrate long term stability with devices other than npn silicon planar transistors.

Thus Hilbiber attempted to find a relationship between V_{OUT} and the bandgap potential of silicon at zero Kelvin, but found that it was primarily a function of the semiconductor material used in the two different transistors. He got what he was after, a much better long-term stability, and stopped at that. Nothing happened for six years,

when Bob Widlar put in the missing pieces. He recognized that the difference in diffusion profiles was only a secondary effect and the idea would work better if the two transistors were made by identical processes [4].

2.2 Widlar's Bandgap Reference Circuit

If we plot the diode voltage (V_{BE}) over temperature we will notice that it points at the bandgap potential at absolute zero. This is not strictly a straight line; it is slightly convex below about 150^{o}C and concave above (it asymptotically approaches zero volts) [4]. The line in red on the figure below shows the negative temperature dependency generated by the V_{BE} voltage. With $V_{BE} \approx 750mV$ and T=300K, $\partial V_{BE}/\partial T \approx -1.5mV/K$ [7].

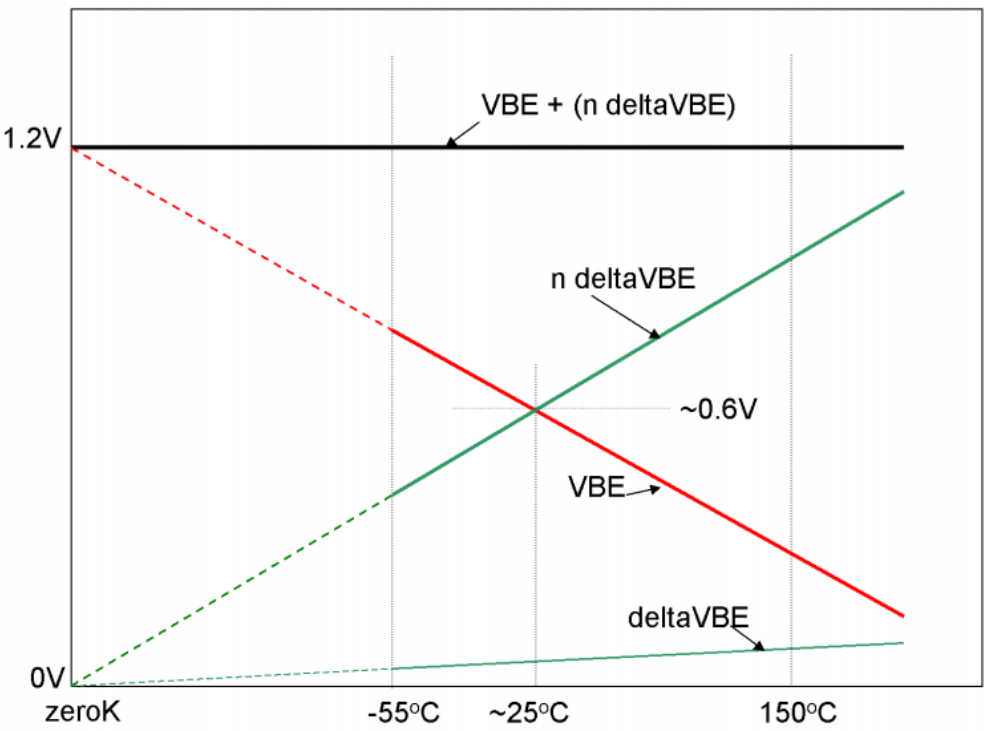

Figure 2.4: The principle of a bandgap reference [4]

If two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature. For example, as shown in Figure 2.5, if two identical transistors ($I_{S1} = I_{S2}$) are biased at collector currents of nI_0 and I_0 and their base currents are negligible, then

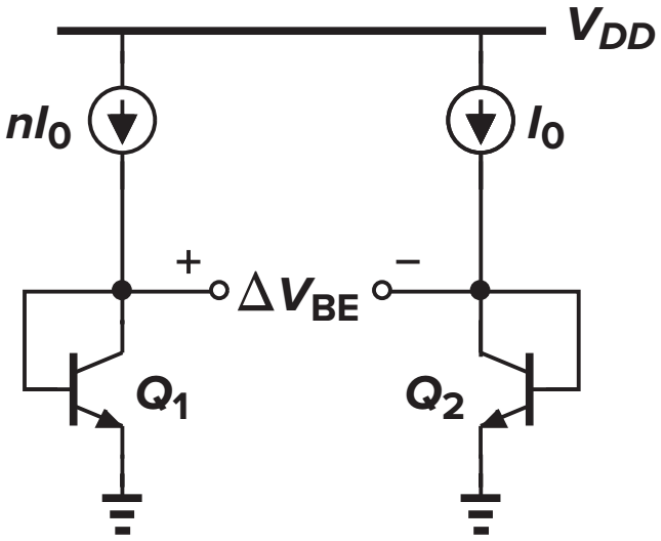

Figure 2.5: Generation of PTAT voltage [7]

$$\begin{aligned}\Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T ln\frac{nI_0}{I_{S1}} - V_T ln\frac{I_0}{I_{S2}} \\ &= V_T ln(n)\end{aligned}$$

Thus, the V_{BE} difference exhibits a positive temperature coefficient.

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} ln(n) \tag{2.13}$$

It can be noticed that, this Temperature Coefficient (TC) is independent of the temperature or behavior of the collector currents.

Figure 2.6 shows the conceptual circuit that depicts how a basic bandgap voltage reference is built.

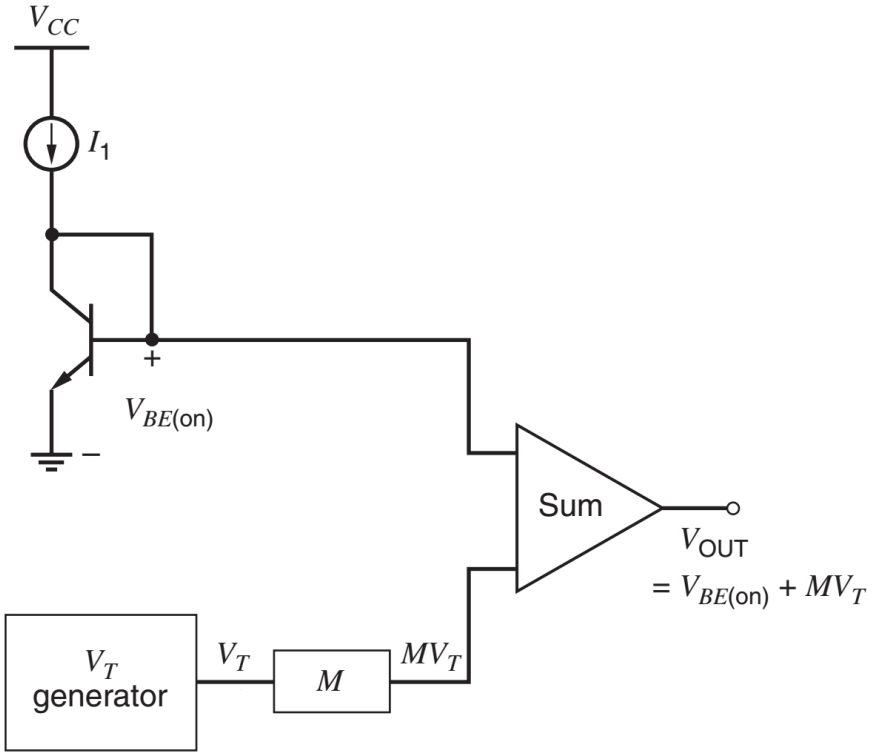

Figure 2.6: Hypothetical bandgap reference circuit [8]

Thus, by using the negative temperature coefficient of emitter-base voltage in conjunction with the positive temperature coefficient of emitter–base voltage differential of two transistors operating at different current densities, Widlar proposed a voltage reference that can be made at voltages as low as the extrapolated energy band-gap voltage of the semiconductor material, which is 1.205 V for silicon.

A simplified version of this reference is shown in Figure 2.7. In this circuit, Q_1 is operated at a relatively high current density, the current density of Q_2 is about 10 times lower and the emitter–base voltage differential ΔV_{BE} between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be

proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter-base voltage plus the drop across R_2

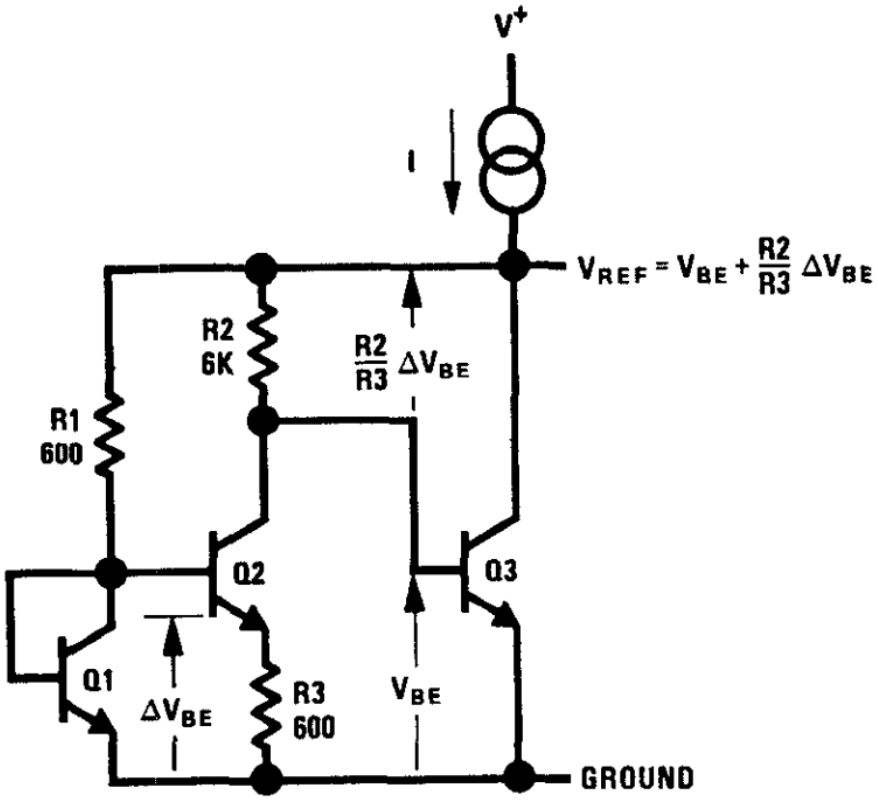

Figure 2.7: Widlar′s low voltage bandgap reference in one of its simpler forms [9]

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor, which is [10]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q} ln\left(\frac{T_0}{T}\right) + \frac{kT}{q} ln\frac{I_c}{I_{C0}} \tag{2.14}$$

where V_{g0} is the extrapolated energy band-gap voltage for the semiconductor material at absolute zero, n is a constant that depends on how the transistor is made

(approximately 1.5 for IC transistors), I_C is collector current, and V_{BE0} is the emitter-base voltage corresponding to I_{C0} at T_0

Further, the emitter–base voltage differential between two transistors operated at different current densities is given by [11]

$$\Delta V_{BE} = \frac{kT}{q} ln \frac{J_1}{J_2} \tag{2.15}$$

where is J is the current density. Referring to 2.14, the last two terms are quite small and can be made even smaller by making I_C vary as absolute temperature. At any rate, the terms can be ignored because they are of the same order as errors caused by nontheoretical behavior of the transistors that must be determined empirically. If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE} the output voltage is obtained by adding 2.14 in its simplified form to 2.15:

$$V_{ref} = V_{g0} \left(1 - \frac{T}{T_0}\right) + V_{BE0} \left(\frac{T}{T_0}\right) + \frac{kT}{q} ln \frac{J_1}{J_2} \tag{2.16}$$

Differentiating the expression for V_{ref} with respect to temperature gives us

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{k}{q} ln \frac{J_1}{J_2} \tag{2.17}$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BE0} + \frac{kT_0}{q} ln \frac{J_1}{J_2} \tag{2.18}$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy bandgap voltage of the semiconductor, the reference will be temperature compensated.

In practice, for minimum drift, it is necessary to make the output voltage somewhat higher than was theoretically determined. This tends to compensate for various low-order terms that could not be included in the derivation. The typical performance of a

circuit set for minimum temperature drift is shown in Figure 2.8. It should be possible to get even lower drift as more and more non-idealities of devices are accounted while designing circuit.

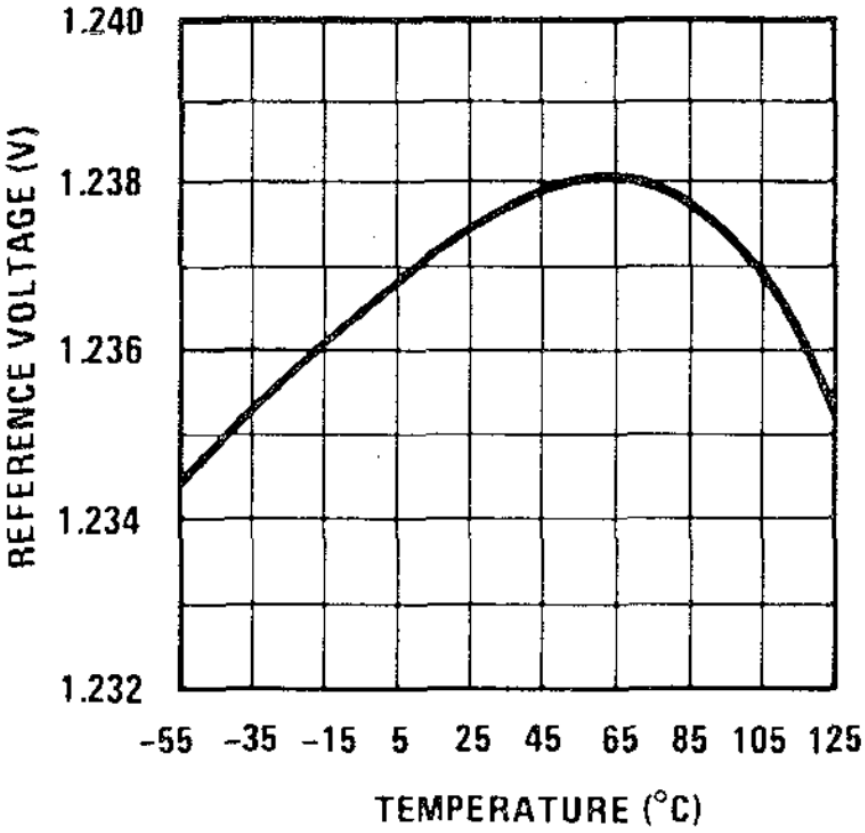

Figure 2.8: Typical temperature characteristic of the low voltage reference [9]

Some of the advantages of this reference that have not been pointed out are that the emitter–base voltage of n-p-n transistors is the most predictable and well understood parameter in an integrated circuit. And the generation of the ΔV_{BE} component depends only on matching, which is easily accomplished in a monolithic circuit. That is why the initial accuracy of the reference can be controlled easily, eliminating the need of trimming individual samples for many applications.

2.3 Brokaw's Bandgap Reference Circuit

The conventional bandgap circuits then, based on [9] used parallel current paths with voltage sensing connections between the paths. The parasitic currents exchanged between the parallel paths are not accounted for in the theory and give rise to beta-dependent voltage errors and temperature drift [12]. Also, to generate higher voltages with the conventional circuit, it is necessary to stack junctions to produce a multiple of the bandgap or use a second amplifier, to multiply the separately stabilized bandgap voltage, that would in turn worsen the temperature coefficient depends on the multiplication factor. To overcome these limitations, Paul Brokaw proposed a design in his paper entitled "A Simple Three Terminal IC Bandgap Reference" published in 1974. The operating principle of the circuit is as below:

In this circuit shown in Figure 2.9, the emitter area of Q_2 is made larger than that of Q_1 (by a ratio of 8-to-1 in the example given). When the voltage at their common base is small, so that the voltage drop across R_2 is small, the larger area of Q_2 causes it to conduct more of the total current available through R_1. The resulting imbalance in collector voltages drives the op-amp so as to raise the base voltage. Alternatively, if the base voltage is high, forcing a large current through R_1, the voltage developed across R_2 will limit the current through Q_2 so that it will be less than the current in Q_1. The sense of the collector voltage imbalance will now be reversed, causing the op amp to reduce the base voltage. Between these two extreme conditions is a base voltage at which the two collector currents match, toward which the op amp drives from any other condition. Assuming equal α or common base current transfer ratio for Q_1 and Q_2, this will occur when the emitter current densities are in the ratio 8-to-1, the emitter area ratio.

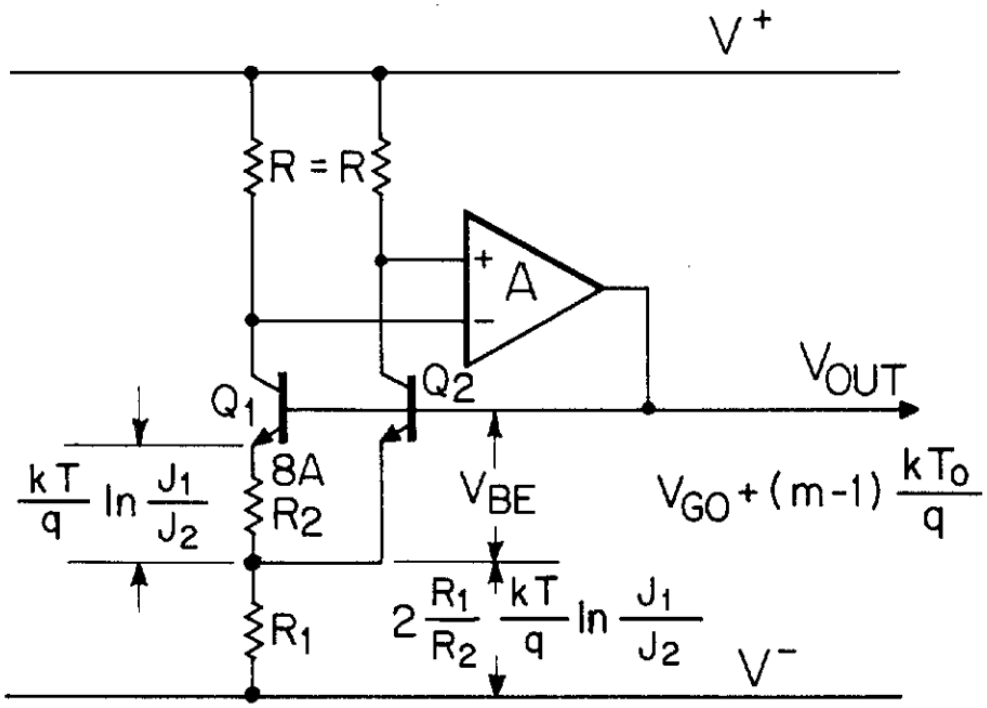

Figure 2.9: Idealized circuit illustrating Brokaw's two-transistor bandgap cell [12]

When this difference in current density has been produced by the op amp, there will be a difference in V_{BE}, between Q_1 and Q_2, which will appear across R_2. This difference will be given by the expression

$$\Delta V_{BE} = \frac{kT}{q} ln \frac{J_1}{J_2} \tag{2.19}$$

Since the current in Q_1 is equal to the current in Q_2, the current in R_1 is twice that in R_2 and the voltage across R_1 is given by

$$V_1 = 2\frac{R_1}{R_2}\frac{kT}{q} ln \frac{J_1}{J_2} \tag{2.20}$$

Assuming that the resistor ratio and current density ratio are invariant, this voltage varies directly with temperature T. This is the voltage which is used to compensate the negative temperature coefficient of V_{BE}.

The voltage at the base of Q_1 is the sum of the V_{BE} of Q_1 and the temperature-dependent voltage across R_1. This is analogous to the output voltage of the conventional bandgap circuit and can be set, by adjustment of R_1/R_2, to a temperature stable value.

2.4 Other circuit approaches to building BGR

The bandgap reference (BGR) circuits discussed so far basically made up of bipolar junction transistors that need bipolar IC technology to fabricate. When complementary metal oxide semiconductor (CMOS) became the technology of choice for digital circuits in early 70s for various advantages, designers started looking to implement BGR in CMOS technology. In this section, we will discuss the various changes the bandgap circuit has undergone to make it viable on CMOS technology and to reduce the minimum supply voltage requirement, power consumption and area demanded by various applications especially the battery powered ones.

2.4.1 CMOS Bandgap References

A bandgap reference is basically a bipolar concept. It needs a diode and the difference between two diodes. And the only diodes good enough are diode-connected bipolar transistors [4].

Fortunately the PN junction formed by the source-drain (emitter) and n-well (collector) region of p-type MOSFET can be used as a diode.

Such a device had limitations. First, the collector is permanently tied to the lower supply voltage. Second, the gain (h_{FE}) is very low. To address these limitations the CMOS substrate were made larger for higher gain and architecture of conventional bandgap voltage reference was modified as shown in the Figure 2.10.

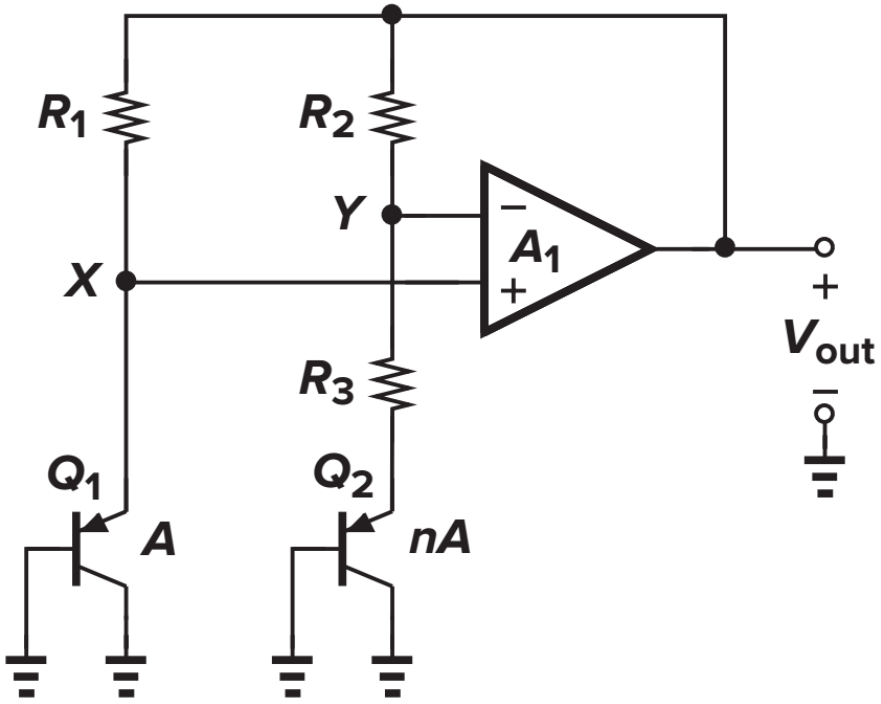

Figure 2.10: A self-biased bandgap reference in n-well cmos [7]

Assume that a stable operating point exists for this self-biased circuit and that the op amp is ideal. Then the differential input voltage of the op amp must be zero and the voltage drops across resistors R_1 and R_2 are equal. Thus the ratio of R_2 to R_1 determines the ratio of I_1 to I_2. These two currents are the collector currents of the two diode-connected transistors Q_2 and Q_1, assuming base currents are negligible. The voltage across R_3 is

$$\begin{aligned} V_{R3} = \Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T ln \frac{I_1}{I_2} \frac{I_{S2}}{I_{S1}} \\ &= V_T ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \end{aligned} \tag{2.21}$$

Since the same current that flows in R_3 also flows in R_2, the voltage across R_2 must be

$$\begin{aligned} V_{R2} = \frac{R_2}{R_3} V_{R3} &= \frac{R_2}{R_3} \Delta V_{BE} \\ &= \frac{R_2}{R_3} V_T ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \end{aligned} \tag{2.22}$$

This equation shows that the voltage across R_2 is proportional to absolute temperature (PTAT) because of the temperature dependence of the thermal voltage. Since the op amp forces the voltages across R_1 and R_2 to be equal, the currents I_1 and I_2 are both proportional to temperature if the resistors have zero temperature coefficient [8]. The output voltage is the sum of the voltage across Q_2, R_3, and R_2:

$$\begin{aligned} V_{OUT} &= V_{BE2} + V_{R3} + V_{R2} \\ &= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) \Delta V_{BE} \\ &= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) V_T ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \\ &= V_{BE2} + M V_T \end{aligned} \tag{2.23}$$

The circuit thus behaves as a bandgap reference, with the value of M set by the ratios of R_2/R_3, R_2/R_1, and I_{S2}/I_{S1}.

2.4.2 Sub-1 V CMOS Bandgap Reference

In the BGR circuits discussed so far, the output voltage V_{ref} is the sum of the built-in voltage of the diode V_f and the thermal voltage V_T of kT/q multiplied by a constant. Therefore, V_{ref} is about 1.25 V, which limits a low supply-voltage operation below 1 V.

Conversely, in the circuit proposed by Banba et al [13], V_{REF} has been converted from the sum of two currents; one is proportional to V_f and the other is proportional to V_T. It produced a V_{ref} of 518 mV.

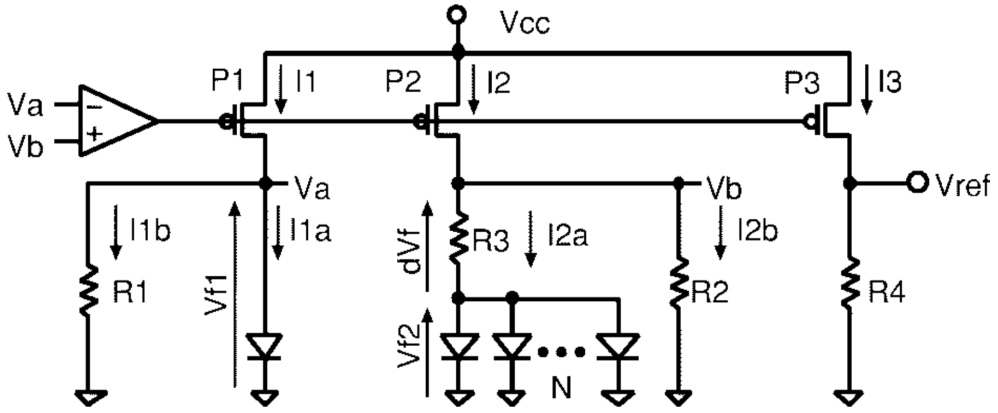

Figure 2.11: Sub-1 V CMOS BGR proposed by Banba et al [13]

The circuit works as follows: The two currents that are proportional to V_f and V_T, are generated by only one feedback loop as shown in Figure 2.11. The PMOS transistor dimensions of p_1, p_2 and p_3 are the same, and the resistance of R1 and R2 is same

$$R1 = R2 \tag{2.24}$$

The op-amp is so controlled that the voltages of V_a and V_b are equalized

$$V_a = V_b \tag{2.25}$$

Therefore, the gates of p_1, p_2 and p_3 are connected to a common node so that the current I1, I2 and I3 becomes the same value due to the current mirror

$$I1 = I2 = I3 \tag{2.26}$$

$$\text{In this case, } I1a = I2a \text{ and } I1b = I2b \tag{2.27}$$

$$dV_f = V_{f1} - V_{f2} = V_T ln(N) \tag{2.28}$$

$I2a$ is proportional to V_T

$$I2a = \frac{dV_f}{R3} \tag{2.29}$$

$I2b$ is proportional to V_{f1}

$$I2b = \frac{V_{f1}}{R2} \tag{2.30}$$

Here, I2 is the sum of I2a and I2b, and I2 is mirrored to I3

$$I3 = I2 = I2a + I2b \tag{2.31}$$

Therefore, the output voltage V_{ref} becomes

$$V_{ref} = R4\left(\frac{V_{f1}}{R2} + \frac{dV_f}{R3}\right) \equiv V_{ref\_prop} \tag{2.32}$$

$$\text{where, } V_{ref\_prop} = \frac{R4}{R2}V_{ref\_conv} \tag{2.33}$$

Therefore, V_{ref_prop} can be freely changed from V_{ref_conv} of 1.25 V and V_{ref} is determined by the resistance ratio of R2, R3 and R4 and little influenced by the absolute value of the resistance. The transistors $p1$, $p2$ and $p3$ are required to operate in the saturation region, so that their drain-to-source voltages can be small when the drain-to-source currents are reduced. Therefore, V_{cc} can be theoretically lowered to V_f if V_{ref} is set below V_f [13].

2.4.3 Sub-1 V Low Power Low Area BGR

In 2012, Annema and Goksun proposed a circuit that circumvents the power-area trade off of conventional sub-1 V BGR. In this architecture shown in Figure 2.12, to break the power-area trade-off, no resistive averaging or subdivision nor any opamps, high ohmic resistor or multiple diodes were used.

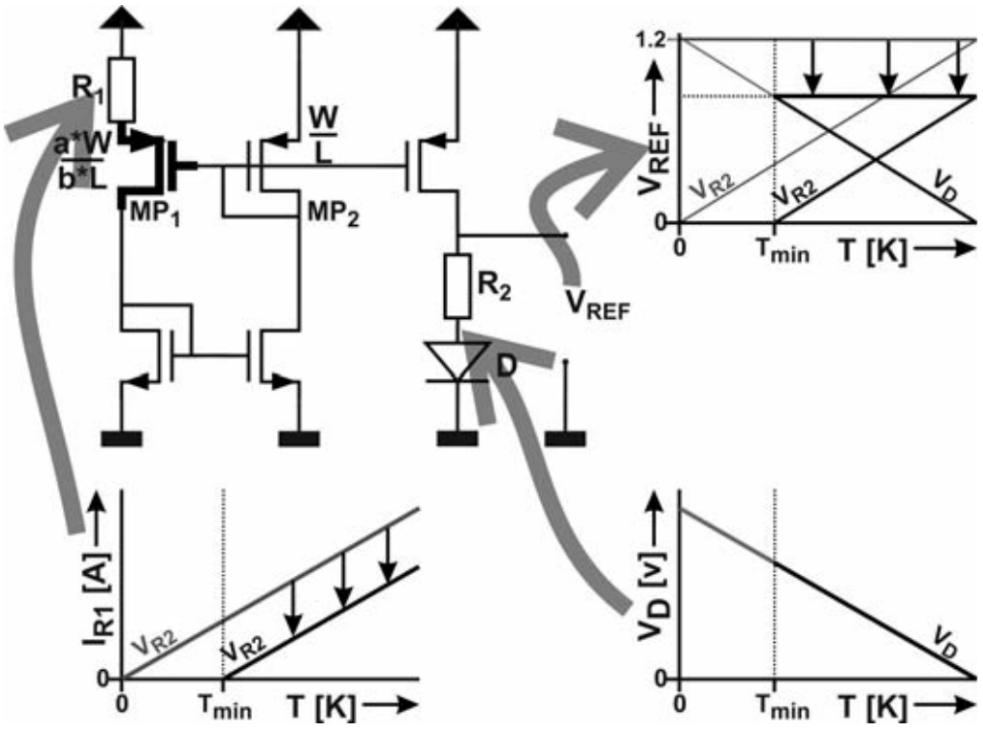

Figure 2.12: Schematic of sub-1 V low power BGR proposed by Annema and Goksun [14]

In this topology, the PMOS transistors MP_1 and MP_2 operate in subthreshold region with an exponential behavior (The theory behind the MOSFETs operating in subthreshold region and related equations will be discussed in next chapter). Then the generated reference voltage (V_{REF}) is given by

$$V_{REF} = \frac{kT}{q} N ln(A) + \frac{kT}{q} ln\left(\frac{I_c(T)}{I_{C,0}T^{\eta}}\right) + V_{gap,0} \approx 1.2V \tag{2.34}$$

In this relation the faction N equals the ratio between resistors R_2 and R_1, the factor A equals the ratio of the current factors of transistors MP_1 and MP_2, $I_C(T)$ is the diode current as a function of temperature T, η is a technology and topology dependent factor typically around 4.

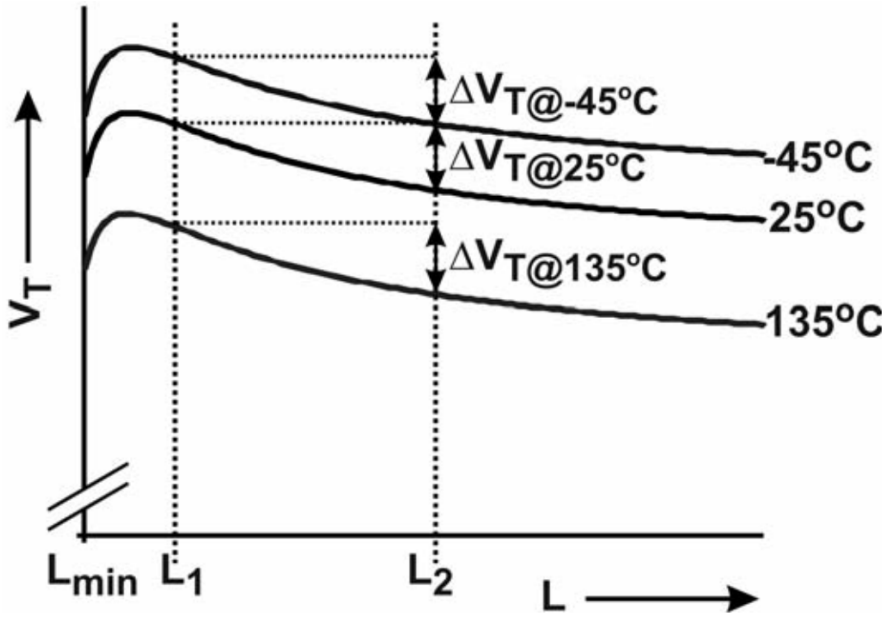

Figure 2.13: Typical threshold-voltage (V_T) dependency on transistor length in modern CMOS technologies for 3 temperatures [14]

To get a sub-1V output, an almost temperature independent offset between MP1 and MP2 was introduced, using the dependency between threshold voltage V_T and transistor length L. A typical $V_T(L)$ relation for three temperatures is given in Figure 2.13. On the x-axis in this figure is the transistor length, starting at minimum length. With increasing length the V_T first increases and then decreases, due to short channel effects. For the current circuit we selected transistor lengths L1 and L2 for transistors MP1 and MP2 respectively, yielding an almost temperature independent offset voltage ΔV_T. The results is that now

$$V_{REF} = N\left[\frac{kT}{q}ln(A) - \Delta V_T\right] + \frac{kT}{q}ln\left(\frac{I_C(T)}{I_{C,0}T^{\eta}}\right) + V_{gap,0} \approx 1.2V - N\Delta V_T \qquad (2.35)$$

Table 2.1 shows the measurements on silicon.

Table 2.1: Performance summary [14]

Parameters	**Value**
Technology	0.16 μm CMOS
V_{DD}	$\geq$ 1.1 V
V_{REF}	944 mV
Temp. Range	-45^{o}C to 135^{o}C
TC	30 ppm/^{o}C
I_{DD} @ 27^{o}C	1.4 μA
Area	0.0025 mm^2

2.4.4 Voltage reference with no resistor

Here comes an another CMOS BGR circuit with MOSFETs operating in subthreshold and doesn't use any resistor. It generates two voltages having opposite temperature coefficients and adds them to produce an output voltage with a near-zero temperature coefficient. The resulting voltage is equal to the extrapolated threshold voltage of a MOSFET at absolute zero temperature, which was about 745 mV for the MOSFETs used [15].

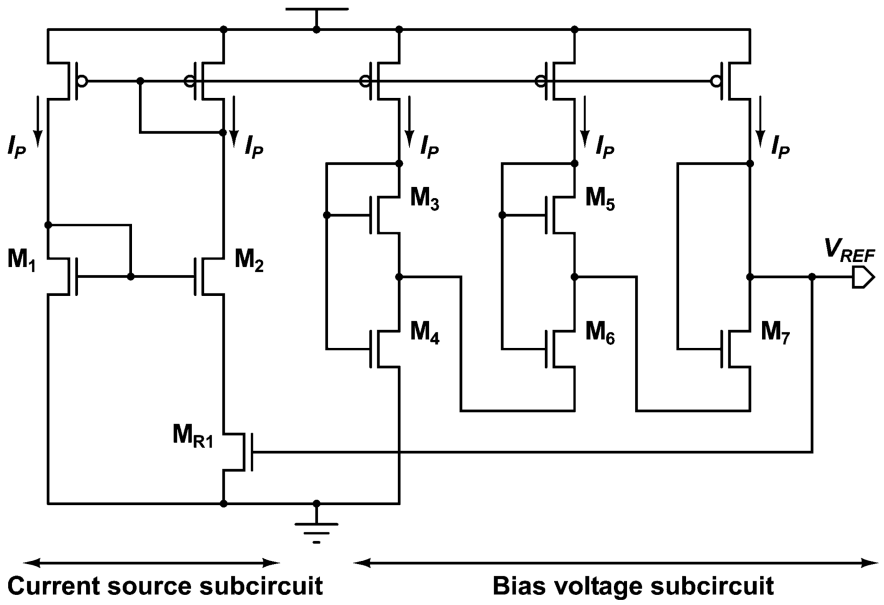

Figure 2.14: Schematic of the circuit proposed in [15]

The circuit shown in Figure 2.14 consists of a current source sub-circuit and a bias-voltage sub-circuit. The current source sub-circuit is a modified β multiplier self-biasing circuit that uses a MOSFET operating in strong inversion triode region acting as a resistor. It generates a current I_P which is mirrored to bias-voltage sub-circuit that produces an output voltage V_{REF} given by the equation 2.36

$$\begin{aligned} V_{REF} &= V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \\ &= V_{GS4} + \eta V_T ln\left(\frac{2K_3K_5}{K_6K_7}\right) \\ &= V_{TH} + V_{GS4} + \eta V_T ln\left(\frac{3I_P}{K_4I_0}\right) + \eta V_T ln\left(\frac{2K_3K_5}{K_6K_7}\right) \end{aligned} \tag{2.36}$$

Where, K is the aspect ratio (W/L) of corresponding transistor. Temperature compensation in this circuit is accomplished by adding PTAT voltage - 2nd and 3rd term in the equation 2.36 - of suitable slope with V_TH of CTAT nature. The performance summary of this circuit is shown in the table 2.2.

Table 2.2: Performance summary [15]

Parameters	**Value**
Technology	0.35 μm CMOS
V_{DD}	1.4 - 3 V
V_{REF}	745 mV
Temp. Range	-20^{o}C to 80^{o}C
TC	7 ppm/^{o}C
I_{DD} @ 27^{o}C	214 nA
Area	0.055 mm^2

Thus, we have discussed the history of voltage reference started as Clarke cell then superseded by bandgap voltage reference that evolved as a modern voltage reference circuit implemented with MOSFETs operating in subthreshold region to operate with sub-1 V supply and consume very low power.

Chapter 3

The Proposed Design

This section starts with introduction to the theory behind the subthreshold operation of MOSFETs followed by the development of concept, design and simulation of the proposed design.

3.1 Transistors Operating in Subthreshold Region

Its important to understand the behavior of MOSFET operating in subthreshold beforehand since all the MOSFETs in our proposed circuit operate in subthreshold region. In this section we will explore the concepts and equations pertaining to subthreshold, also known as weak inversion regime where the channel is weakly inverted. This will allow us to design circuits that can operate with small gate voltages much lesser than the threshold voltage of the transistor.

The Figure 3.1 shows the exponential relationship between the gate voltage and the channel charge in different region of operation namely, Weak, Moderate and Strong inversion.

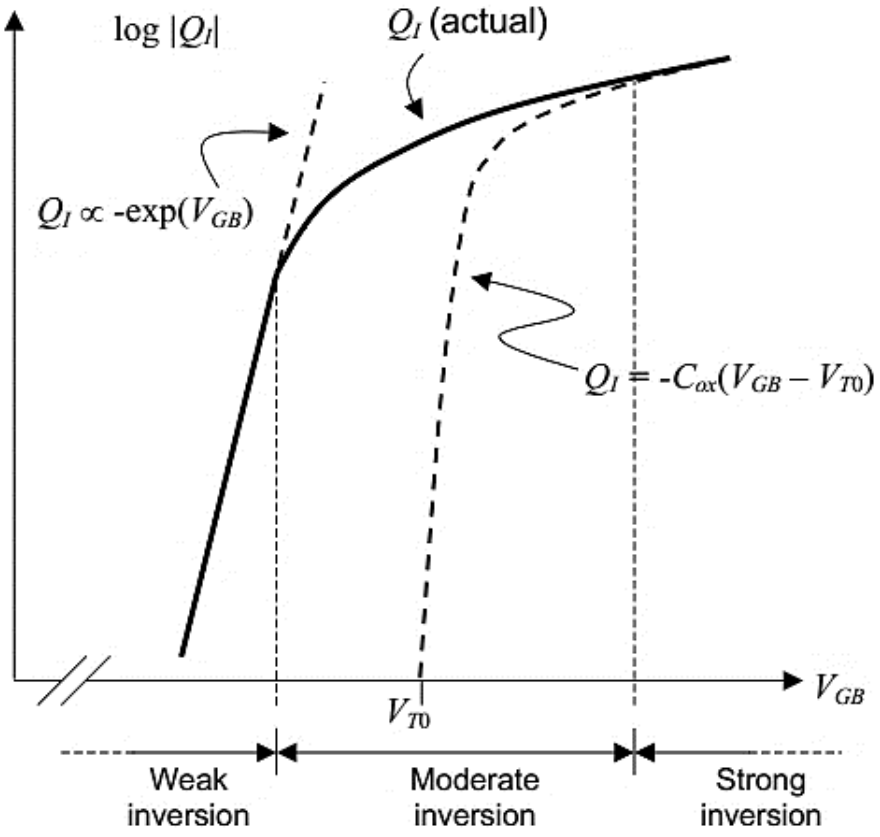

Figure 3.1: Channel charge Vs gate voltage; V_{T0} – Threshold voltage [17]

We can think of weak inversion as the region where Q_I is an exponential function of gate voltage, strong inversion as the region where Q_I is a linear function of gate voltage, and moderate inversion as a transition region between the two. In weak inversion, the inversion layer charge is much less than the depletion region charge:

$$Q_I << Q_B \text{ in weak inversion}$$

Since the substrate is weakly doped, Q_B is small, and there is not enough charge in the channel to generate a significant electric field to pull electrons from the source to the drain. Current flows by diffusion, not drift. Considering diffusion of charge carriers and concentration gradient in the channel, we can derive the expression for the drain

current as below:

$$I_D = I_o \frac{W}{L} exp\left(\frac{\kappa V_G}{V_T}\right) . \left[exp\left(\frac{-V_S}{V_T}\right) - exp\left(\frac{-V_D}{V_T}\right)\right] \tag{3.1}$$

Where, W, L – Width and Length of the transistor

V_G, V_S, V_D – Gate, Source and Drain voltages with reference to bulk terminal respectively. V_T is thermal voltage:

$$V_T \equiv \frac{kT}{q} \cong 26 \text{ mV at room temperature}$$

Where, T is absolute temperature and I_o is a process-dependent constant.

For an n-channel MOSFET:

$$I_{on} \equiv \frac{2\mu_n C'_{ox} V_T^2}{\kappa} . exp\left(\frac{-\kappa V_{T0n}}{V_T}\right) \tag{3.2}$$

Where C_{ox} is the gate oxide capacitance per unit area, V_{T0n} is threshold voltage of n–channel MOSFET and κ is the gate coupling coefficient that represents the coupling of the gate to the surface potential:

$$\kappa = \frac{C_{ox}}{C_{ox} + C_{dep}} \tag{3.3}$$

The depletion capacitance C_{dep} stays fairly constant over the subthreshold region, and kappa (κ) is usually considered to be constant, although it increases slightly with gate voltage.

Typical values of I_{0n} range from 10^{-15}A to 10^{-12}A. The subthreshold gate coupling coefficient κ is rarely reported in process data. Sometimes, people will report the subthreshold slope V_T/κ. If it is not given, κ can be calculated by:

$$\kappa = \left(1 + \frac{\gamma}{2\sqrt{(1+\alpha)\phi_F}}\right)^{-1} \tag{3.4}$$

Where, $\gamma = \dfrac{\sqrt{2q\varepsilon N_{sub}}}{C'_{ox}}$

$$\phi_F = \frac{kT}{q} ln \frac{N_{sub}}{n_i}$$

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

The α parameter should be set between zero – for extreme weak inversion, near depletion mode – and one – for the boundary between weak and moderate inversion – to account for the slight change in depletion capacitance. Usually, $\alpha = 0.5$ is a good value to use for general-purpose use. So all we really need to know is the oxide thickness (to determine $C_{ox}{}'$) and the channel doping (N_{sub}) to estimate kappa. In SPICE models, oxide thickness is called T_{OX} (units = m) and the channel doping is called NSUB or NCH (units = cm^{-3}).

We can rearrange the terms and rewrite the expression for drain current as:

$$I_D = I_o \frac{W}{L} exp\left(\frac{\kappa V_G - V_S}{V_T}\right) . \left[1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right] \tag{3.5}$$

Where, V_{DS} – Drain to source voltage

For ease of calculation and understanding, let us replace κ with $1/m$, assume $V_S = 0$ and grouping of variables differently, then we get the expression below,

$$I_D = S\mu V_T^2 exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right) . \left[1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right] \tag{3.6}$$

Where, $S = \left(\dfrac{W}{L}\right) C_{ox}$

m – subthreshold slope parameter

V_{GS} – gate to source voltage

If we are able to keep the voltage V_{DS} greater than $4V_T$, then I_D becomes almost independent of V_{DS} since $exp(-V_{DS}/V_T) << 1$ so the last term is approximately equal to one, and can be ignored. The expression for drain current then simplifies to:

$$I_D = S\mu V_T^2 exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right) \tag{3.7}$$

3.2 Proposed Circuit

In the previous chapters, starting with the basic zener type voltage reference to more sophisticated voltage reference that can work with the voltage down to 0.6 V and still can produce temperature coefficient less than 15 ppm/^{o}C have been discussed. In this chapter let's look into the proposed circuit which can work with the supply voltage as low as 0.45 V and consume power in nano watt range. To achieve a low voltage below 0.5 V operation, the transistors need to be operated in subthreshold regime and as a consequence, the supply current get reduced to nano ampere range. The development of the proposed circuit is divided into three different parts:

- Threshold-voltage-difference based reference voltage generator
- Reference voltage generator with start-up circuit and simulation results
- Pre-regulator with start-up circuit and simulation results of complete circuit

3.2.1 Reference Voltage Generator

The reference voltage (V_{REF}) generating architecture is based on [18] that generates PTAT voltage but with one difference that the transistors have different threshold voltages as proposed in the [19]. In this section core of the voltage reference circuit will be presented. The basic concept of our topology is shown in Figure 3.2. In this circuit, the two transistors M2 and M3 are in the same p-well, which may be connected to the

source of M2 as body effect is very negligible on M3 since its source terminal is the one which generates V_{REF}.

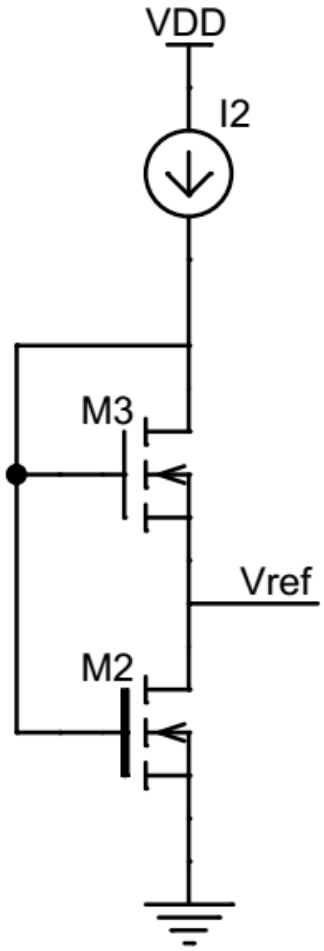

Figure 3.2: Reference voltage generating circuit

For $V_{DS} > 4V_T$, I_D becomes almost independent of V_{DS}, the transistor is said to be in saturation and the drain current of MOSFET as shown in the equation 3.6 in section 3.1 simplifies to

$$I_D = S\mu V_T^2 exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right) \tag{3.8}$$

Thus, the gate to source voltage V_{GS},

$$V_{GS} = V_{th} + mV_T ln\left(\frac{I_D}{S\mu V_T^2}\right) \tag{3.9}$$

Let us note that, at a first approximation, $V_T(T)$, $V_{th}(T)$ and $\mu(T)$ introduce dependence on temperature. As shown in equation 3.10, it is usually assumed that V_{th} decreases linearly with temperature

$$V_{th} = V_{th}(T_0) + (k_{t1} + k_{t2}V_{BS})\left(\frac{T}{T_0} - 1\right) \tag{3.10}$$

where $V_{th}(T_0)$ is the threshold voltage at the reference temperature ($T_0 \approx 300.15^oK$). V_{BS} is the body-to-source voltage of the transistor. Temperature coefficients k_{t1} and k_{t2} have negative values.

Applying Kirchhoff' voltage law (KVL) on the circuit shown in the Figure 3.2, we get,

$$\begin{aligned} V_{REF} &= V_{GS2} - V_{GS3} \\ &= V_{th2} + m_2 V_T ln\left(\frac{I_2}{S_2\mu_2 V_T^2}\right) - V_{th3} + m_3 V_T ln\left(\frac{I_2}{S_3\mu_3 V_T^2}\right) \\ &= (V_{th2} - V_{th2}) + V_T ln\left(\frac{(S_3\mu_3 V_T^2)^{m3}}{(S_2\mu_2 V_T^2)^{m2}} I_2^{(m_2-m_3)}\right) \end{aligned} \tag{3.11}$$

Thus the reference voltage is the sum of difference between the threshold voltage of the MOSFETs and the second term that is proportional to absolute temperature (V_{PTAT}). Also, the reference voltage value depends only on the difference in threshold voltage of M_2 and M_3 since the value of (V_{th2}–V_{th3}) is much larger than the second term V_{PTAT}. A simpler expression for V_{REF} can be obtained considering that, the m parameters of different regions have similar values then,

$$m_2 = m_3 = m$$

And $\mu_2 = \mu_3 = \mu$, then

$$V_{REF} = (V_{th2} - V_{th3}) + V_T ln\left(\frac{S_3}{S_2}\right) \tag{3.12}$$

For the given current, as the temperature rises, the threshold voltage of the MOSFET decreases with a slope of 1 – 3 mV/^{o}C depending on the fabrication process. Since M2 and M3 have different threshold voltages by fabrication, they may not have equal temperature coefficient as shown in the Figure 3.3. So, it's required to modify the slope dV_{th}/dT so that $(V_{th2} - V_{th3})$ stays at constant value for all temperature. This is achieved by choosing appropriate proportionality factor for V_{PTAT} term in equation 3.12

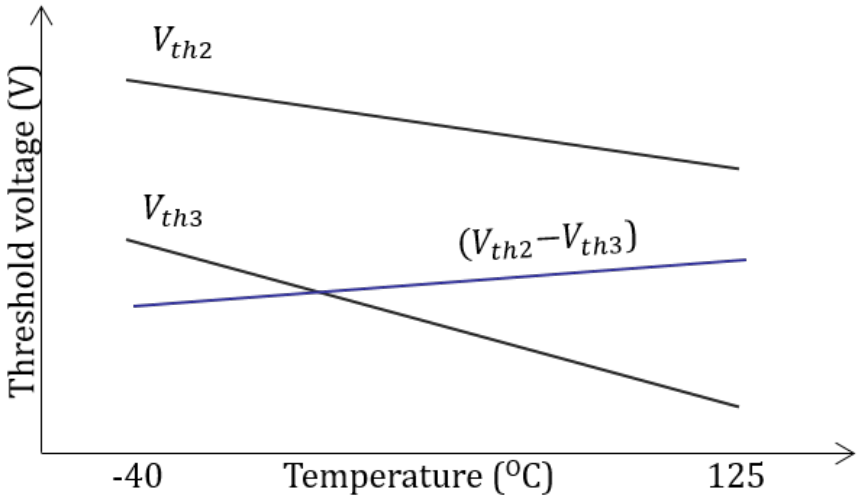

Figure 3.3: V_{th} V_S Temperature curve of MOSFET for a constant drain current

It can be noticed that, this generated voltage V_{REF} is independent of the current I_2 flowing through the transistors and it holds good as long as this current is smaller than the weak inversion limit and much larger than the leakage currents through gate oxide and parasitic PN junctions in the MOSFETs. Furthermore, as mentioned before, the drain to source potential of the transistors must exceed by $4V_T$ in order to maintain them in saturation. To achieve this, the dimension and threshold voltage of the transistors need to be chosen appropriately.

3.2.2 Reference Voltage Generator with Self-biasing

Traditionally we use resistors to bias the current source but, as proposed in [19], M2 and M3 transistors of reference voltage generator can be made self-biased by addition of one NMOS transistor M1 operating in subthreshold region as shown in the Figure 3.4.

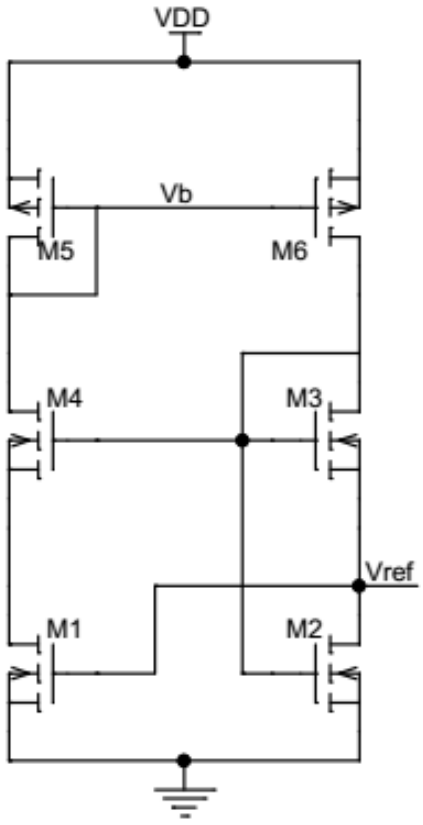

Figure 3.4: Reference voltage generator with self-bias

The transistor M1 converts V_{REF} applied at it's gate to a current that is mirrored to reference voltage generating leg. This self-biased configuration is analyzed as follows: Applying KVL on the loop formed by the MOSFETS M1, M2 and M3 in the Figure

3.4, we get,

$$V_{GS2} = V_{GS1} + V_{GS3}$$

$$V_{th2} + m_2 V_T ln\left(\frac{I_2}{S_2\mu_2 V_T^2}\right) = V_{th1} + m_1 V_T ln\left(\frac{I_1}{S_1\mu_1 V_T^2}\right) + V_{th3} + m_3 V_T ln\left(\frac{I_2}{S_3\mu_3 V_T^2}\right) \quad (3.13)$$

Let $\Delta V_{th} = V_{th1} + V_{th3} - V_{th2}$

and $\Sigma_m = m_1 + m_3 - m_2$

then solving for I_1 we get,

$$I_1 = \left(\frac{S_1^{m1} S_3^{m3}}{S_2^{m2}}\right)^{\frac{1}{\Sigma_m}} \mu V_T^2 exp\left(\frac{-\Delta V_{th}}{\Sigma_m V_T}\right) \quad (3.14)$$

If we assume $m_1 = m_2 = m_3 = m$ then

$$I_1 = \left(\frac{S_1 S_3}{S_2}\right) \mu V_T^2 exp\left(\frac{-\Delta V_{th}}{m V_T}\right) \quad (3.15)$$

The self-biased structure, which can also be considered as a current generator, is to provide a current, as given by the equation 3.15, as independent as possible of supply voltage variations, which compensates temperature effects on V_{REF}. All the transistors in the proposed solution are Standard V_{th}(SVT) MOSFETs, except for M2 and M19, which are High V_{th}(HVT) MOSFETS. The stability of V_{REF} with VDD variations mainly depends on the current generator′s insensitivity to supply voltage variations. This characteristic is achieved by means of the self-biased current source architecture, where the high impedance elements per branch (M7 and M1) are capable of absorbing the supply voltage variations leaving their current almost unchanged. Significant improvement of the reference voltage line sensitivity can be obtained by using an additional current mirror, in the self-biased current reference circuit. The use of additional current mirrors in the current generator that add transistors in stack, increases the minimum achievable VDD were avoided.

Figure 3.5 shows the self-biased voltage reference with start-up circuit that ensures the main circuit to be biased in the desired state. The dimensions of transistors M19-M25 are chosen in such a way, under normal operating condition, they consume negligible amount of current.

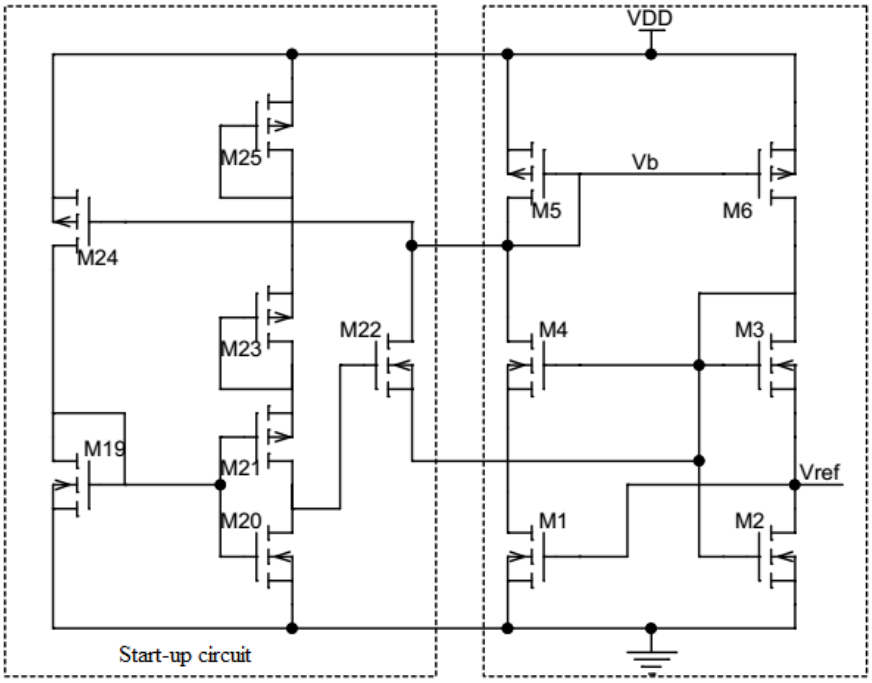

Figure 3.5: Voltage reference circuit with start-up circuit

3.2.3 Minimum Current Consumption

The minimum current consumption is not limited by the operating region of transistors in the proposed configuration. All $|V_{GS}|$ values are at least 100 mV smaller than the absolute value of MOSFET threshold voltages. Recalling equation 3.9, it can be stated that, in principle, there is no lower limit for the current supplied in the subthreshold voltage reference of Figure 3.5. Nevertheless, the proposed temperature compensation technique imposes a lower bound for the generated current, as explained below. The ratio of the dimensions of the transistors M2 and M3 are chosen such a way that the

negative temperature coefficient of $(V_{th2} - V_{th1})$ slope gets compensated by the positive temperature coefficient of V_{PTAT} by second terms in the equation 3.12. Moreover, the technology has a limitation on W_{MIN}/L_{MAX}. Thus the value on minimum current consumption is imposed.

3.2.4 Minimum Supply Voltage

Considering the voltage reference configuration in the Fig 3.5, the supply voltage will redistribute as a sum of a V_{DS} and a V_{GS} in both voltage reference generating branch and the self-biasing branch. Although subthreshold operation does not limit the minimum V_{GS} achievable, in order to generate a current and hence a reference voltage, as independent as possible of VDD variations, the high impedance transistors, M1 and M7 should absorb at least V_{DS} of $4V_T$. The maximum working temperature of the proposed circuit is 125^oC, therefore, the minimum V_{DS} value to ensure proper operation, even at that temperature, becomes $4V_T = 137$ mV. Consequently, by generating a current given by the equation 3.15 so that, in each branch, $V_{GS} << 4V_T$, a minimum supply voltage of $4V_T$ can be achieved with a similar voltage reference architecture regardless of the process technology chosen. In our specific case, the gate-to-source voltage of M2 need to be 274 mV at least which means VDD needs to be 411 mV at least and the same rule applies to self-biasing branch as well. So, the minimum VDD that ensures $|V_{DS}| > 4V_T$ for M1, M4 and M5, will be

$$VDD_{MIN} > 12V_T \tag{3.16}$$

It can be noticed that the simulations results shown in the Figure 3.7 follows the equation 3.16.

3.2.5 Analyzing the effect of process variations

The generated voltage given by equation 3.12 is a linear combination of threshold voltages parameters shown in eqnuation 3.10. As usually happens in low-power CMOS

integrated voltage, the reference voltage is process dependent. Thus, neglecting matching errors, the accuracy of the output voltage is mainly due to the accuracy of threshold voltages of transistors M2 and M3. Process variations are generally distinguished in WIthin Die (WID or intra-die) variations and Die to Die (D2D or inter-die) variations [19]. The first type of variations causes mismatch between transistors of the same chip and influences the relative accuracy of transistor parameters. Careful layout techniques [3] and large transistor W/L [7], can help to reduce those effects. D2D variations, instead, influence the absolute accuracy of transistor parameters and their effects are not compensated in the proposed configuration. Expressing V_{REF} as the threshold voltage difference between an HVT – NMOS and an SVT – NMOS , the standard deviation of V_{REF} can be approximated with:

$$\sigma_{VREF} = \sqrt{\sigma_{HVT}^2 + \sigma_{SVT}^2} \tag{3.17}$$

Where σ_{HVT} and σ_{SVT} are the V_{th} standard deviations of an HVT – NMOS and an SVT – NMOS, respectively. In equation 3.17, it has been implicitly assumed that the variation process of the two V_{th}s are independent. i.e., their covariance is zero. Moreover, assuming that $\sigma_{HVT} = \sigma_{SVT} = \sigma_{Vth}$, it is easy to evaluate the standard deviation of the voltage reference as [19]

$$\sigma_{VREF} \approx \sqrt{2\sigma_{Vth}} \tag{3.18}$$

The equation 3.18 confirms that the initial accuracy of voltage reference is mainly affected by the threshold voltage variations of the M2 and M3. On the other hand, since the threshold voltage dependence of temperature, $\Delta V_{th}/\Delta T$ has small dependence on process variations, as demonstrated in [19], even the temperature coefficient of the reference voltage will benefit from a similar behavior with process variations.

3.2.6 Line Sensitivity

A common parameter used for the evaluation of the reference voltage sensitivity to VDD variations is the line sensitivity. It is defined as

$$LS = \frac{\left(\frac{\Delta V_{REF}}{\Delta VDD}\right)}{V_{REF}} \text{x} 100\% \tag{3.19}$$

where ΔVDD is the VDD range of operation: 2 V - 0.45 V = 1.55 V for the proposed circuit, ΔV_{REF} is the absolute variation of the reference voltage, in the range considered, and V_{REF} stands for the mean output value. The line sensitivity optimization starts from the minimization of ΔV_{REF}. Neglecting the effect of the term in square brackets in equation 3.6 (i.e., considering a $V_{DS} \geq 4V_T$), we can write the expression for V_{REF} derived from small signal analysis on the circuit shown in the Figure 3.2. This expression shows how the drain voltage of M3 has an effect on V_{REF} when there is a finite resistance across the drain source terminals of the MOSFETs.

$$V_{REF} = \frac{V_{D3}}{1 + \frac{r_{o3}}{r_{o2}} + g_m r_{o3}} \tag{3.20}$$

Where, g_m is the small signal transconductance and is same for both the MOSFETs as the current through them is same. r_{o2} and r_{o3} are small signal resistance between the source and drain terminals which can be calculated as

$$r_o = \frac{mV_T}{\lambda_D I} \tag{3.21}$$

Where λ_D is the Drain-Induced Barrier Lowering factor (DIBL). Here, r_o is not same as the one due to the effect of channel length modulation when the transistor operates with strong inversion. Subthreshold operated MOSFETs do not suffer from channel length modulation, therefore, for $V_{DS} \geq 4V_T$, I_D will depend on only because of the DIBL effect. As is well known, the DIBL effect significantly decreases with increasing channel length [19].

It can be noticed from the equation 3.21 that, to have better line sensitivity, r_{o3} has to be kept as high as possible but it comes at a cost – higher the channel length, higher the area of the MOSFET. It also should be noted that, though the equation 3.21 gives an idea about the importance of keeping r_o as high as possible to have better line sensitivity, this small signal model can not be used for calculating the line sensitivity of the whole circuit as the VDD varies from 0.45 V to 2 V which needs large signal analysis. So we resort to simulation results entirely to measure the line sensitivity. Qualitatively, considering the whole circuit, for line sensitivity minimization, the high impedance transistors M1 and M7 should also be as along as possible, in order to improve the stability of the generated current.

This result not only gives a quick evaluation of the expected line sensitivity of the proposed voltage reference configuration, but can also be extended to every voltage reference architecture operated in subthreshold region, where only one high impedance transistor per branch is present. Such architectures are very common in ultra-low voltage solutions, where the reduction of transistor stacks helps in lowering the minimum achievable. In [16], where a two-transistor stack per each branch is present, a minimum of 0.9 V was attained.

3.2.7 Simulation Results

Cadence – Virtuoso was used for making the circuit schematic and Spectre was used for simulation. Figure 3.6 and 3.7 show the simulation results from typical corner and supply voltage VDD set to 450 mV

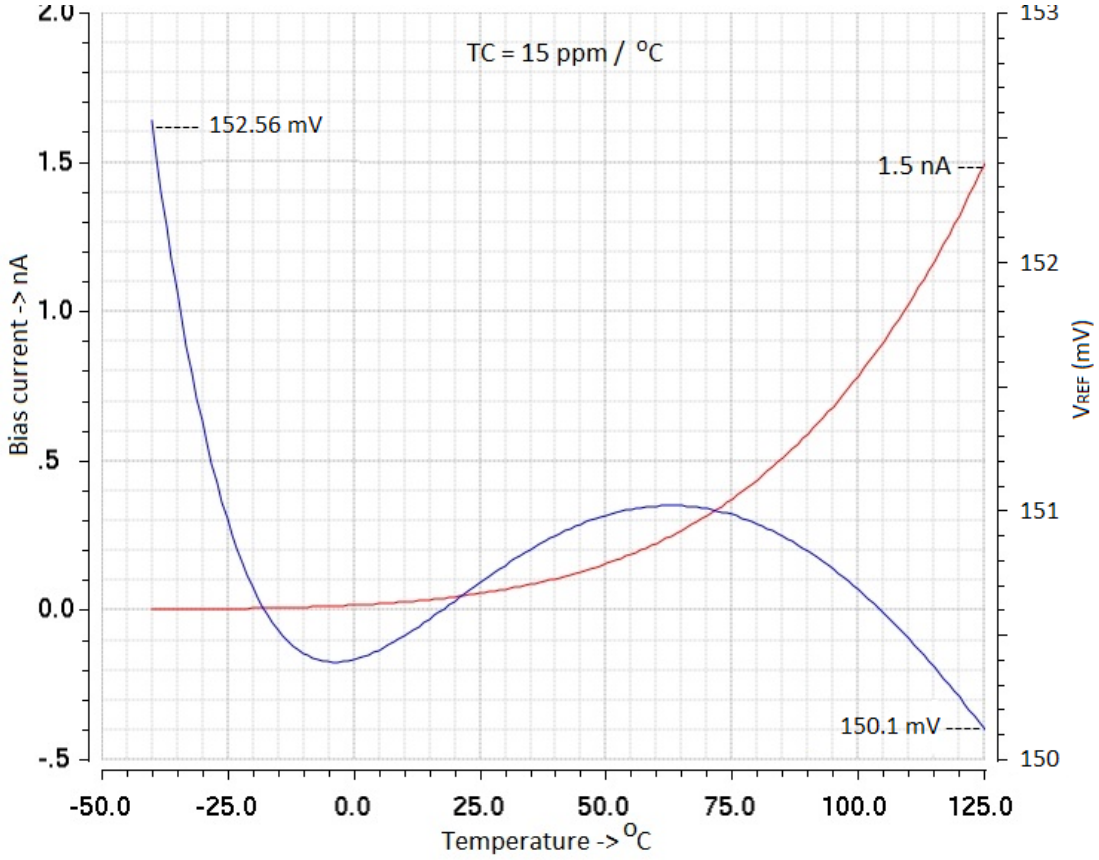

Figure 3.6: Bias current, V_{REF} Vs Temperature. VDD = 450 mV

Figure 3.6 shows that the bias current rises exponentially as the temperature is increased from -40^{o}C and reaches as high as 1.5 nA at 125^{o}C. The V_{REF} versus Temperature curve shows a temperature coefficient of 15 ppm/^{o}C for the same temperature range.

Figure 3.7 shows how do V_{REF} and bias current change when supply voltage VDD changes. Here the temperature is kept constant at 27^{o}C. As long as the supply voltage is lesser than 450 mV which is the minimum voltage required to keep all the transistors in saturation, the bias current generated by the current generator circuit is not enough

to create $4V_T$ V across M2 and M3 thereby causing V_{REF} less than the targeted value of 150 mV. The non-zero line sensitivity and the change in bias current are due to the DIBL effect when the supply voltage is increased beyond 450 mV as shown in the Figure 3.7.

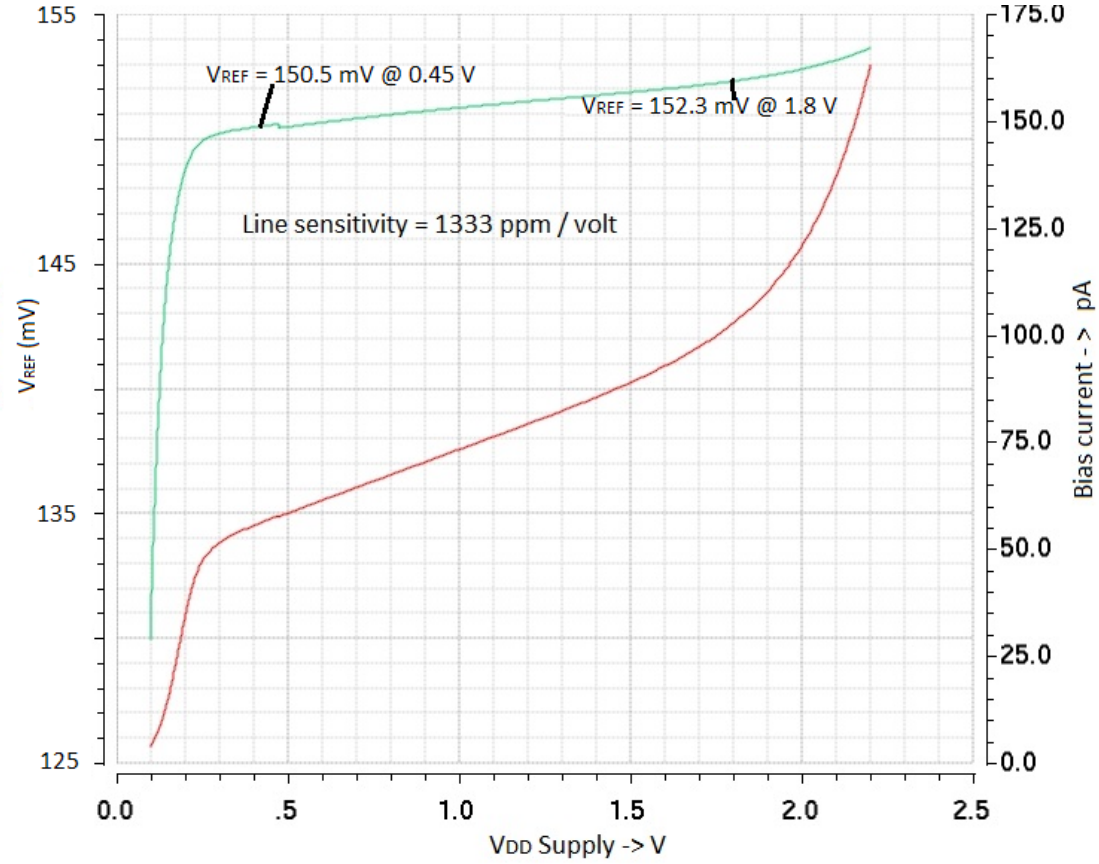

Figure 3.7: Bias current, V_{REF} Vs Supply Voltage (VDD) at 27^{o}C

3.2.8 Pre-regulating circuit

The pre-regulating circuit shown in Figure 3.8, is to improve line sensitivity by absorbing the change in VDD and keeps Va almost constant. It consists of M7 – M18

MOSFETs and all of them operate in the subthreshold region. When supply voltage VDD fluctuates, the variation of I_A can be written as

$$i_a = g_{ds17}(v_{dd} - v_a) \tag{3.22}$$

Where v_{dd} and v_a are the variation of VDD and V_A, and g_{ds17} is drain-source conductance of M17. Meanwhile, the variation of I_E is

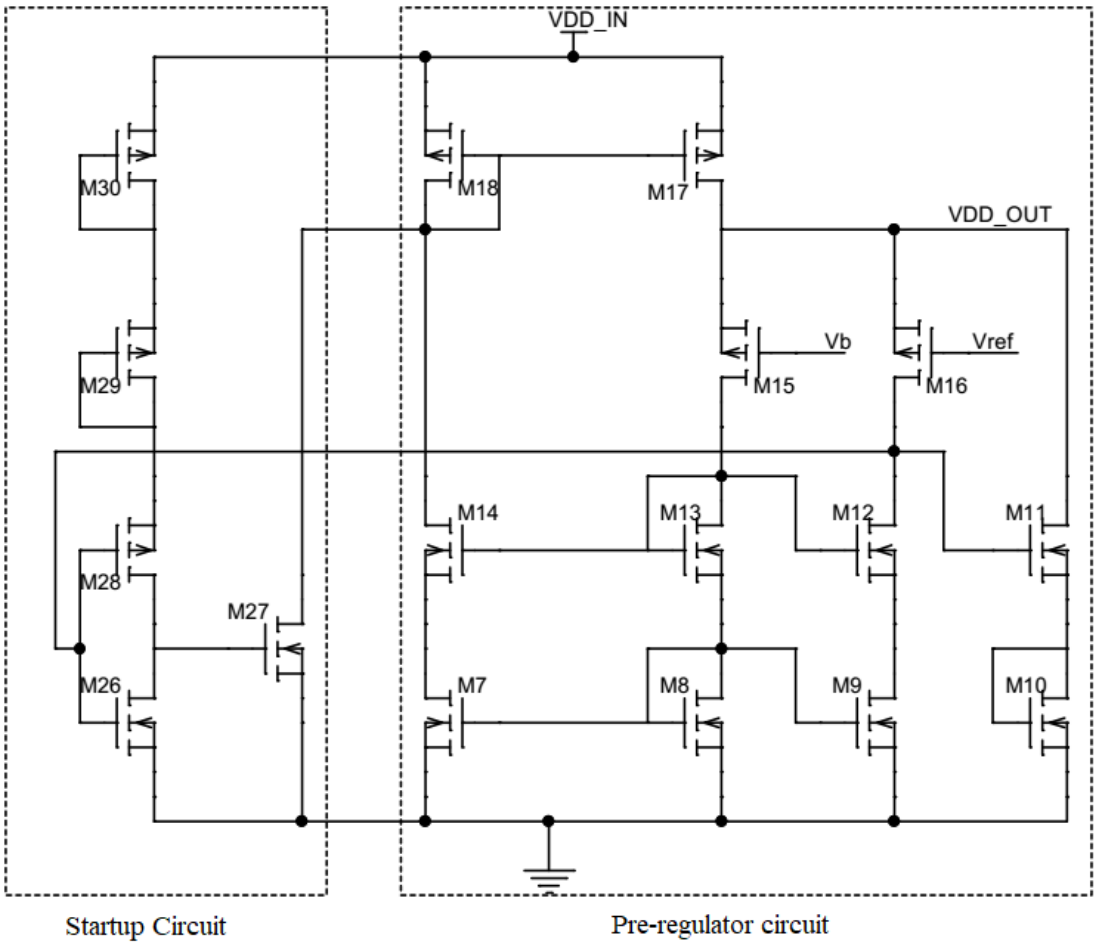

Figure 3.8: Pre-regulator circuit with startup circuit

$$i_e = \frac{v_a}{r_{eq}} \tag{3.23}$$

Where $r_{eq} \approx \frac{g_{m11} r_{011} g_{m16} r_{o9} g_{m12} r_{012} g_{m10}}{g_{m11} r_{011} + g_{m10} r_{011}}$ (3.24)

Where r_{eq} is the equivalent ground impedance of M9-M12. Since I_D is almost constant and I_B, I_C, I_D and I_P are nearly unchanged when VDD fluctuates, i_a should be equal to i_e according to krchhoff's current law.

$$i_e = i_a \tag{3.25}$$

From equation 3.22 and 3.25, we get,

$$\frac{v_{dd}}{v_a} = \frac{1}{r_{eq} g_{ds11}} + 1 = k \tag{3.26}$$

Where r_{eq} and g_{ds11} are very small values and k is a relatively large value.

$$v_a = \frac{v_{dd}}{k} \tag{3.27}$$

Therefore, the variation of V_A is much smaller than that of VDD.

In the Figure 3.8, the start-up circuit consists of M26-M30, and its aspect ratio should be chosen carefully to satisfy the power requirement.

As shown in the Figure 3.8, the transistor M16 in the pre-regulating circuit is biased by the V_{REF}. Cascoding transistors M7 M8 and M9 are to increase the equivalent ground impedance for lower line sensitivity. The W/L ratio of M17 is chosen larger to have higher regulated voltage (V_{DD_OUT}) and M11 should be chosen carefully to make sure that M12 and M16 operate in saturation region.

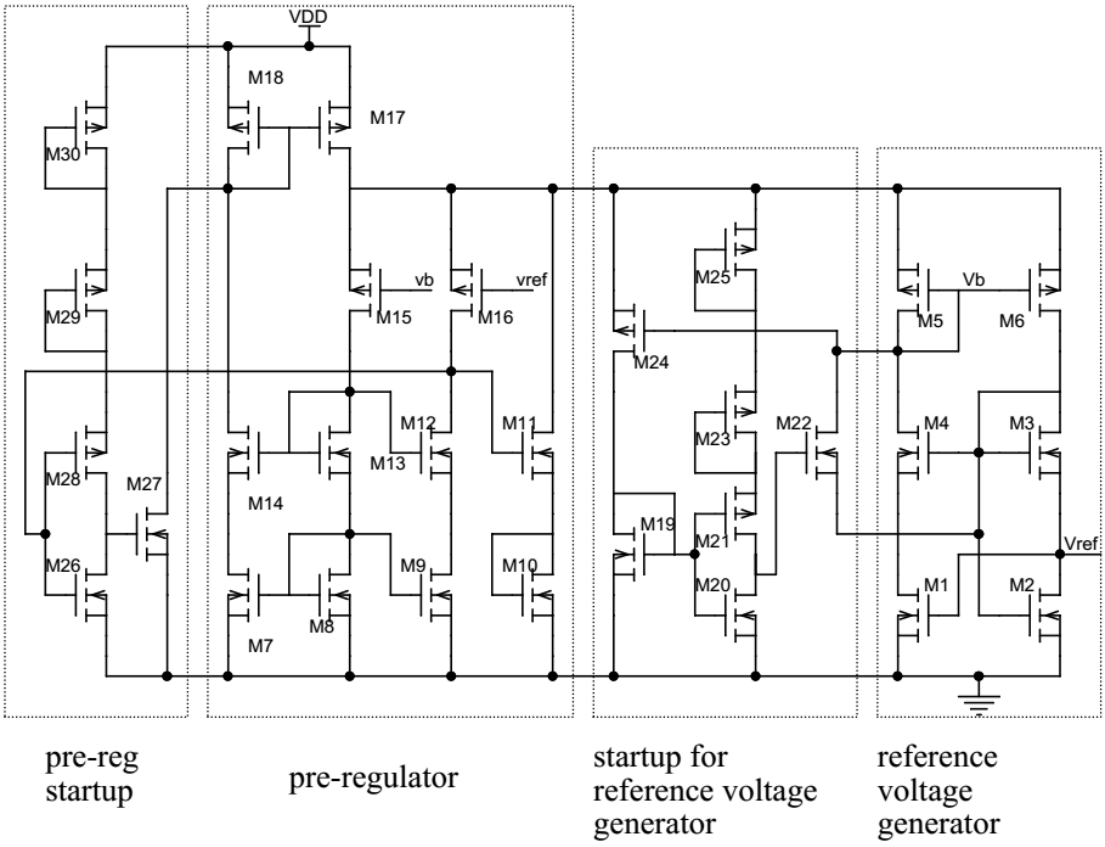

Figure 3.9: Complete Proposed Circuit

3.2.9 Simulation results

Figure 3.10 and 3.11 show the simulation result of the entire proposed voltage reference. Comparing the Figure 3.7 and 3.10 reveals us that the pre-regulator circuit has improved the line sensitivity substantially from 1333 ppm/volt to 25 ppm/volt. From the graph 3.7, it can be noticed that the pre-regulator circuit takes a head room of only 79 mV.

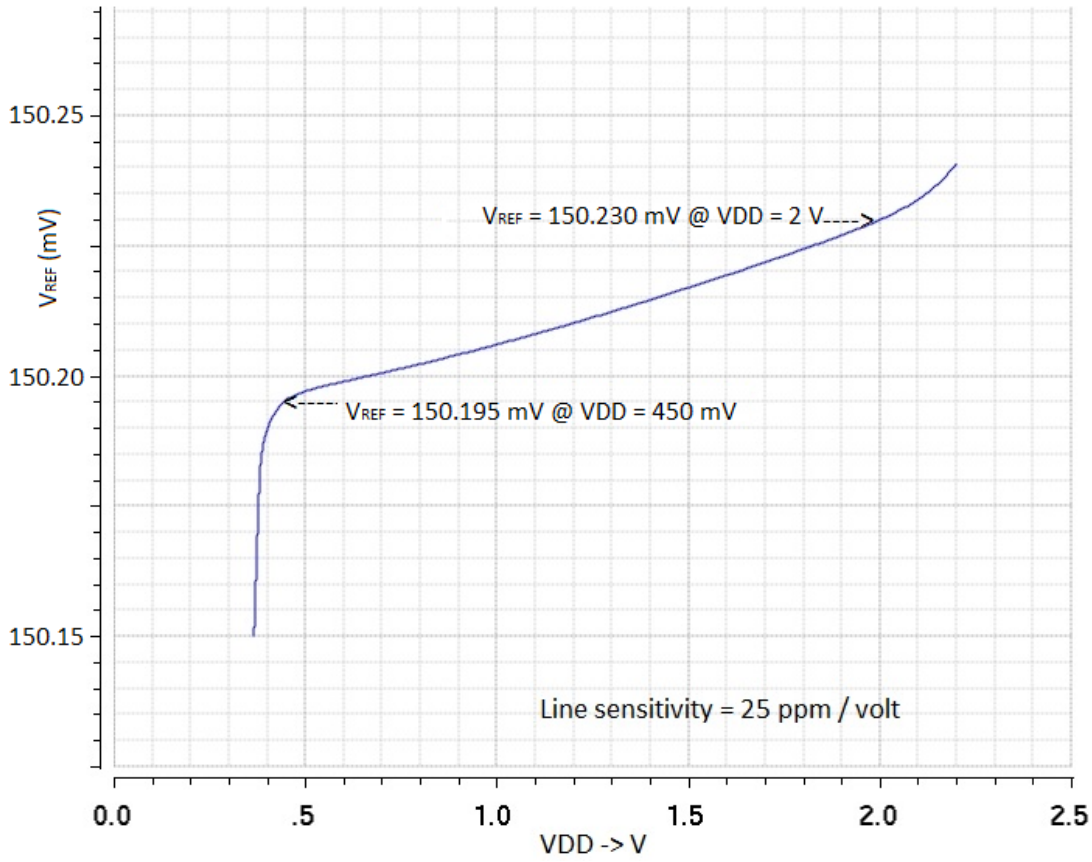

Figure 3.10: V_{REF} Vs VDD at Temperature = 27^oC

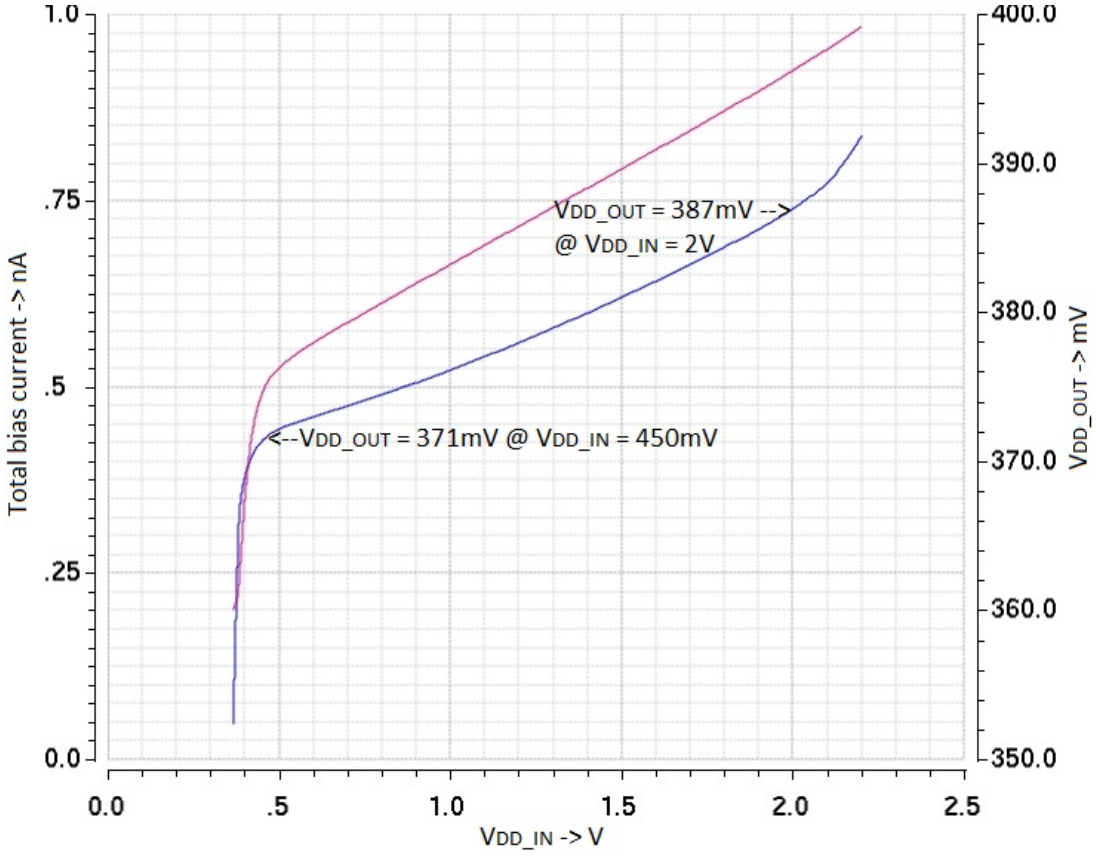

Figure 3.11: Total bias current, V_{DD_OUT} Vs V_{DD_IN} at Temperature = 27^oC

Chapter 4

Conclusion

4.1 Summary

A low voltage, ultra low power voltage reference circuit designed and simulated in IBM 0.13 μm CMOS process, is presented. The circuit works with all transistors in subthreshold region, thus allowing a remarkable reduction of minimum supply voltage and power consumption while keeping the temperature coefficient as low as 15 ppm/^{o}C. In this sense, the proposed solution represents a significant advance in low power low voltage reference circuit design: the average power dissipation is only 2 nW, which is about one order of magnitude lower than that of the best results found in the literature, and the minimum supply voltage for correct operation falls to 0.45 V. In addition, a temperature compensation technique and a simple model for line sensitivity prediction in subthreshold-operated voltage reference circuits is presented and demonstrated. The ultra low power and low voltage features of the proposed circuit make it very attractive for battery-operated electronic applications.

4.2 Future Enhancement

As discussed in the section 3.2.5, the generated voltage is a linear combination of threshold voltages parameters. Thus, the accuracy of the output voltage is mainly due to the accuracy of threshold voltages of transistors M2 and M3. Since these MOSFETs belong to different device type, both intra-die variations and inter-die variations affect the initial accuracy of V_{REF}. In this case, a trimming circuit is required to increase the initial accuracy. As the loading effect has direct impact on initial accuracy of V_{REF} and its temperature coefficient, it should always be connected to gate terminal of a MOSFET in the next stage. Alternatively, an opamp circuit can permanently be added to the output of the voltage reference. By doing so, in addition to buffering, scaling of V_{REF} is also possible.

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