An Improved DC fault Protection Algorithm for MMC HVDC Grids based on Modal Domain Analysis

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***Abstract*— To detect the DC faults for MMC based DC grids using overhead line transmission, many protection methods in phase-domain have been proposed. These existing protection methods suffer from incomplete function, weak theoretical basis and sensitivity to fault resistance and noise disturbance. To overcome these shortcomings, this paper proposes an improved DC fault protection algorithm using the modal-domain approach for the MMC based overhead DC grids, which decouples interaction between positive and negative poles and mitigates the strong frequency-dependency of the characteristic impedance in phase-domain. The DC fault equivalent circuits are established in modal-domain and the fault characteristics during the initial stage are analysed. Based on the modal-domain analysis, the line-mode reactor voltage which combines fault characteristics of negative and positive reactor voltages, is employed to identify the internal faults. The zero-mode reactor voltage which enlarges the differences between faulty and healthy poles, is employed to select the faulted pole. This method is robust to fault resistance and noise with high detection speed. In addition, it is not affected by power reversal, AC faults and DCCB operation, which are validated and evaluated by simulations in PSCAD/EMTDC.**

***Index Terms*— MMC-HVDC grids, DC fault detection, modal-domain analysis, phase-modal transformation, anti-noise.**

I. Introduction

The modular multilevel converter (MMC) based DC grids have been a preferred solution to integrate bulk renewable energy over long distance [1]-[3]. Recently, the State Grid Corporation of China (SGCC) is constructing the ±500 kV *Zhangbei* DC grid, which transmits large-scale wind power using the overhead lines (OHL) [4]. Comparing with the point-to-point HVDC transmission systems, each converter of DC grids will feed current to the fault point during DC faults, leading to higher fault current [5]. To avoid damage of power electronic devices and guarantee reliable power supply for healthy parts, DC circuit breakers (DCCB) are implemented to isolate the faulted lines [6]. Taking *Zhangbei* project as an example, the DCCBs are required to interrupt 25kA DC fault current within 6ms [7], which puts forward stringent speed requirements for the DC fault protection algorithm.

With regard to the protection design of MMC based DC grids, the traveling-wave (TW) methods in time-domain are mostly employed to identify internal and external faults, such as the rate of change of current (ROCOC) [8], the rate of change of voltage (ROCOV) [9], the wave peak [10] methods and so on. As pointed out in [11], the amplitudes of the traveling-waves will attenuate under large fault resistance, particularly for pole-to-ground (PTG) faults. Besides, the initial wave front and wave peak are difficult to be detected encountering noise disturbance. To improve the robustness to fault resistance, the wavelet transform (WT) in the time-frequency domain can be adopted to extract the high-frequency components [7][11].

When a DC fault occurs, the sharp wave front of traveling wave induced from the fault point will be smoothed at the current-limiting reactors (CLR). Considering this boundary effect, some boundary protection approaches taking advantage of DC current-limiting reactors are proposed. Reference [7] proposes a transient voltage based DC fault detection method on the basis of the high-frequency characteristics difference between the converter and line sides of CLRs. References [12] and [13] propose protection methods based on DC reactor voltage change rate (RVCR) and DC reactor voltage of faulted pole (RVOFP) respectively. The voltages across the CLRs are employed as an indicator.

According to [14], the aforementioned protection methods can be classified into phase-domain methods. The advantages and disadvantages of them are listed in Table 1 (some methods may belong to multiple categories). As can be seen, the traveling wave methods are sensitive to fault resistance. The WT methods may bring about additional calculation delay and burden when the decomposition layer is high. The DC reactor based methods suffer from incomplete functions. In addition, due to the strong frequency-dependency of the characteristic impedance in overhead lines, these phase-domain methods are difficult to conduct a comprehensive fault analysis, especially under asymmetrical PTG faults, which makes them lack of theoretical basis.

To address the shortcomings of phase-domain methods, the phase-modal transformation (PMT) is employed to decouple the dependency of the poles of transmission lines and the fault analysis under modal-domain is carried out to design the protection schemes. In [15][16], modal-domain is selected to improve the performance of fault detection algorithms, such as the capability of the faulted pole selection and the robustness to fault resistance. In [15], the line-mode backward travelling-wave voltage associated with WT modulus maximum (WTMM) is adopted. However, a sampling frequency as high as 1MHz is required. A lifting WT based protection is proposed in [16]. The line-mode travelling-wave voltage with four decomposition layers is calculated to detect the arrival of wave fronts accurately. However, due to the four decomposition layers of WT, the time delay and computational burden is high. The analysis of these existing

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modal-domain methods is also concluded in Table 1.

To overcome the challenges of the aforementioned methods, a fast and reliable protection scheme based on modal-domain analysis is proposed for MMC based DC grids using overhead line transmission. The contributions of the proposed method are as follows:

1) The PTG and PTP fault analysis under modal-domain are conducted respectively, which mitigates the dependency of positive and negative poles of overhead lines in phase-domain and improves the capability of the faulted pole selection and endurance to fault resistance. Compared with the phase-domain methods, this paper provides a solid theoretical foundation for the PTG faults.

2) The modal components of reactor voltages are selected to design the fault detection algorithm. The line-mode reactor voltage is employed to identify the external and internal faults. The zero-mode reactor voltage is employed to select the faulted pole. This method can reduce the computational burden greatly compared with the WT based methods and the existing modal-domain methods.

The remainder of the paper is structured as follows. Section II derives the equivalent fault network of DC grid under modal-domain. Fault analysis under modal-domain is conducted in section III. Then, the overall protection scheme is proposed in section IV. Finally, the effectiveness and robustness of the proposed method are verified under extensive cases in section V and VI.

Table 1 Overall comparison of typical protection schemes and the improvement in the proposed method

Protection methods		Advantages	Disadvantages
Phase-domain based methods	The traveling-wave methods based on time-domain analysis (for instance [8][9][10])	1. Simple concept and widely implemented. 2. Almost no computation is required.	1. The sharp wave front will attenuate with large resistance, particularly for PTG faults. 2. Difficult to detect the initial wave front and wave peak under noise disturbance.
	The WT methods based on time-frequency domain analysis (for instance [7][11])	1. WT is employed to extract the high-frequency components efficiently.	1. High computational burden and long time delay due to the cascaded filtering and multi-scale decomposition [8]. 2. Weakness to noise.
	DC reactor based methods (for instance [12][13])	1. Simple implementation and low computational burden. 2. Work well for faults with high resistance [12] or different fault types [13].	1. Sensitivity to fault type or resistance. 2. Lack of detailed fault characteristic analysis for PTG faults. 3. Impacts of noise are not discussed in detail.
Existing modal-domain based methods	The line-mode backward voltage TW based on WTMM (for instance [15][16])	1. WT is employed to detect arrival of wave fronts accurately. 2. Robustness to noise. 3. Work well for faults with high resistance and different fault types.	1. High computational burden with four decomposition scales of WT. 2. High sampling frequency (1MHz) is required [15].
Improvement in the proposed modal-domain based method		1. Endurance to fault resistance. 2. Robustness to noise. 3. Able to select the faulted pole. 4. High speediness for fault detection. 5. Low computational burden with lower sampling frequency. 6. Strong theoretical basis for both PTP and PTG faults.	

II. Equivalent Fault Network of MMC based DC Grid under Modal-domain

Fig. 1 shows a typical topology of half-bridge MMC based DC grid [16]. The hybrid DCCBs are implemented to interrupt the DC fault current. To suppress the rise rate of fault current, the current-limiting reactors are installed on the overhead lines (OHL) [17]. This system adopts the symmetric monopole structure and the OHL adopts the frequency-dependent model.

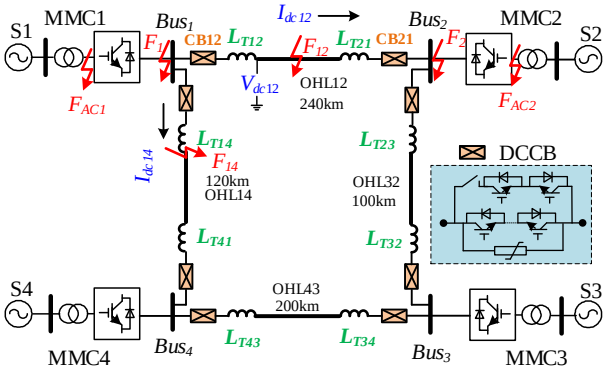


Fig. 1. The topology of MMC based DC grid.

A. Equivalent Model of Half-bridge MMC

During fault initial stage, the discharge current of MMC capacitors dominates fault current. The impact of AC source on fault current can be ignored [18]. Referring to [19], the simplified equivalent model of MMC can be obtained, as shown in Fig. 2.

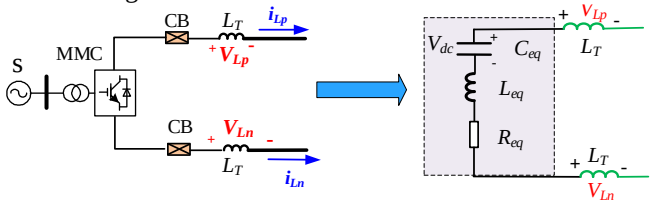


Fig. 2. The MMC equivalent model.

In Fig. 2, C_{eq}=6C/N, L_{eq}=2/3L, R_{eq}=2/3R. Where C, L and R represent the sub-module capacitance, arm inductance, arm resistance respectively. N and L_T denote the sub-module number per arm and the current-limiting reactor.

B. The Overhead Transmission Line Equivalent Model

Fig. 3 shows the distributed parameter model of OHL [20]. C_{g0} and C_{l0} denote the grounding capacitor and phase

capacitor per unit length respectively. And L_{0mn}, R_{0mn}, and M_{0mn} denote the self-inductance, resistance and mutual inductance of line *mn* per unit length respectively.

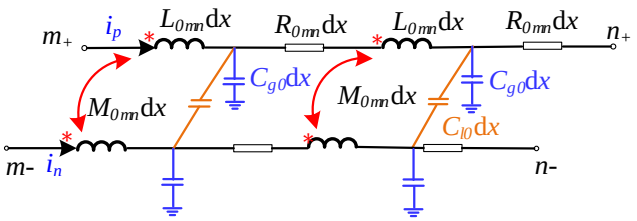


Fig. 3. The detailed distributed parameter model of overhead line.

The typical value of line capacitance (grounding capacitor and phase capacitor) and sub-module equivalent capacitance are 0.01μF and 1×10^2μF respectively [21]. Thus, the discharge current from sub-module capacitors is much larger than that of line capacitor. Hence, the line capacitor can be ignored and the OHL model is simplified to a *RL* series circuit, as shown in Fig. 4.

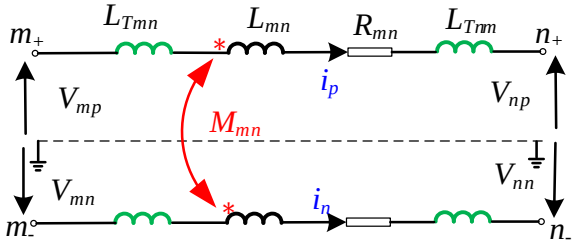


Fig. 4. The simplimplified equivalent model of overhead transmission line.

In Fig. 4, L_{mn}, R_{mn}, and M_{mn} denote the self-inductance, resistance and mutual inductance of line *mn* respectively. The subscripts "*m*" and "*n*" represent node *m* and node *n*; subscripts "*p*" and "*n*" represent positive and negative pole. According to KVL, it can be obtained:

$$\begin{bmatrix} V_{mp} \\ V_{mn} \end{bmatrix} = \begin{bmatrix} L_{Tmn}+L_{mn}+L_{Tnm} & M_{mn} \\ M_{mn} & L_{Tmn}+L_{mn}+L_{Tnm} \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_p \\ i_n \end{bmatrix} + \begin{bmatrix} R_{mn} & 0 \\ 0 & R_{mn} \end{bmatrix}\begin{bmatrix} i_p \\ i_n \end{bmatrix} + \begin{bmatrix} V_{np} \\ V_{nn} \end{bmatrix} \quad (1)$$

In order to decouple the dependency of the poles of transmission lines under PTG faults, phase-modal transformation is employed, as shown in equation (2) [22].

$$\begin{bmatrix} x_1 \\ x_0 \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} x_p \\ x_n \end{bmatrix} \quad (2)$$

where x_p and x_n represent the positive and negative pole values. x_0 and x_1 represent the zero-mode and line-mode values. Applying the phase-modal transformation to equation (3), it can be obtained:

$$\begin{cases} \begin{bmatrix} V_{m1} \\ V_{m0} \end{bmatrix} = \begin{bmatrix} L_{Tmn}+L_{mn1}+L_{Tnm} & 0 \\ 0 & L_{Tmn}+L_{mn0}+L_{Tnm} \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_1 \\ i_0 \end{bmatrix} \\ \quad + \begin{bmatrix} R_{mn} & 0 \\ 0 & R_{mn} \end{bmatrix}\begin{bmatrix} i_1 \\ i_0 \end{bmatrix} + \begin{bmatrix} V_{n1} \\ V_{n0} \end{bmatrix} \\ L_{mn1} = L_{mn} - M_{mn};\ \ L_{mn0} = L_{mn} + M_{mn} \end{cases} \quad (3)$$

where subscripts "*1*, *0*" represent the line-mode and zero-mode components respectively. Equation (3) demonstrates that an asymmetric coupled equivalent network can be decomposed into two symmetric decoupled networks by the phase-modal transformation. The line-mode and zero-mode equivalent model of OHL under modal-domain are shown in Fig. 5.

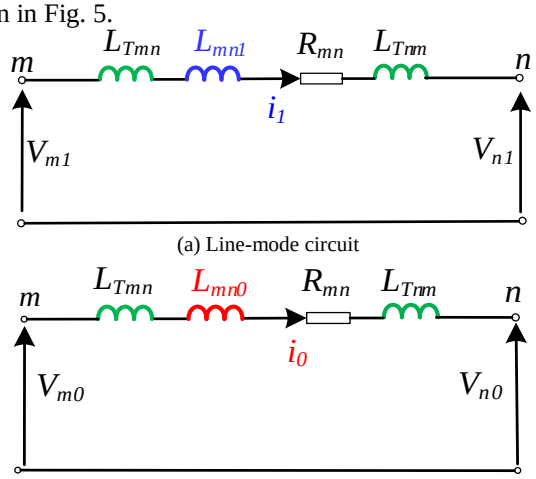


Fig. 5. The line-mode and zero-mode circuit of overhead transmission line.

C. Fault Network of DC Grid in Modal-domain

Based on the equivalent models of MMC and OHL, the model of four-terminal DC grid can be obtained, as shown in Fig. 6. Suppose a fault happen at *n* of OHL12 (F_{12}) (0<*n*<1). During the fault wave propagation stage, the CLR and line inductance provide higher impedance characteristics, comparing with line resistances. Thus, the line resistance and arm resistance are ignored [12]. The un-faulted OHL14 and OHL23 are equivalent to two voltage sources with the voltage of V_{14} and V_{23}, where C_{eq14} and C_{eq23} are the equivalent capacitances of the terminal of OHL14 and OHL23 respectively, as shown in Fig. 7[12]. Thus, the simplified equivalent fault network during fault initial stage can be obtained, as shown in Fig. 7(a). The line-mode and zero-mode networks under modal-domain are depicted in Fig. 7 (b) and Fig. 7 (c) respectively.

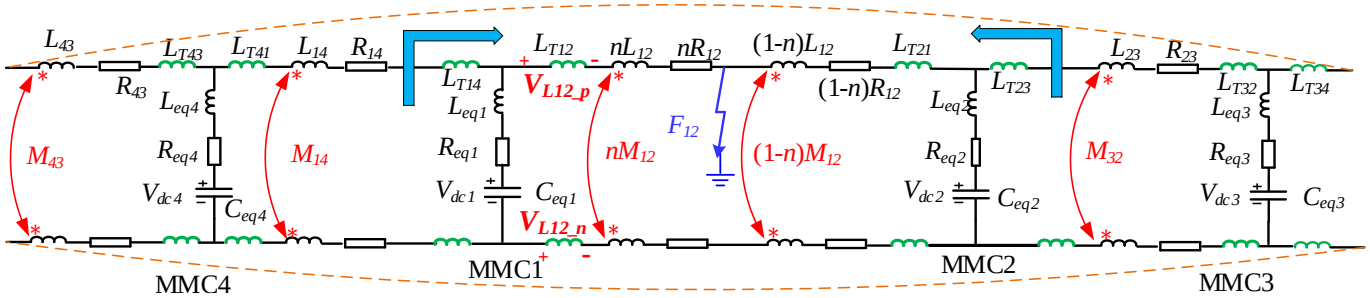
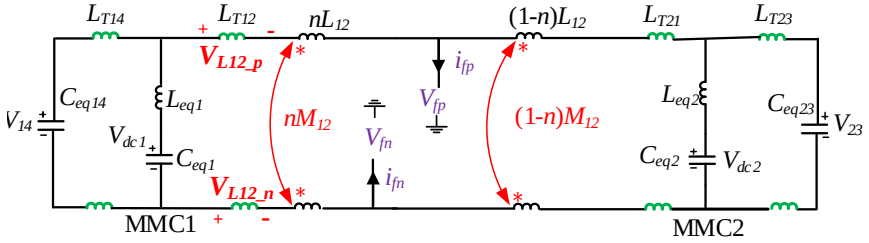
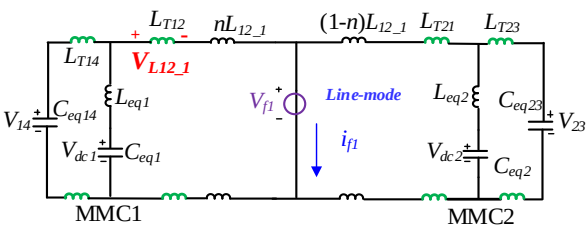


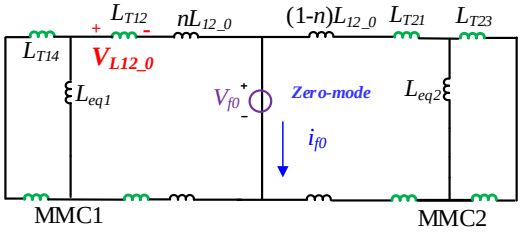
Fig. 6. The fault equivalent network of the symmetric monopole system under PTP faults.



(a) Simplified system equivalent network at F_{12}



(b) Line-mode equivalent network at F_{12}



(c) Zero-mode equivalent network at F_{12}

Fig. 7. The simplified equivalent network of system with a fault at F_{12}.

III. Fault Analysis of MMC based DC Grid under Modal-domain

A. PTG Fault Analysis under Modal-domain

1) *Fault Analysis under Internal PTG Faults*

Taking CB12 for an example, applying a positive PTG (P-PTG) fault at F_{12}, the fault boundary condition is i_{fn}=0, V_{fp}=0. Based on the phase-modal transformation, the fault boundary condition can be re-written as:

$$\begin{cases} V_{f1}+V_{f0}=0 \\ i_{f1}=i_{f0} \end{cases} \tag{4}$$

It can be seen from the above fault boundary condition that the zero-mode network is connected with the line-mode network in series. Thus, the composite mode network under modal-domain can be obtained, as shown in Fig. 8.

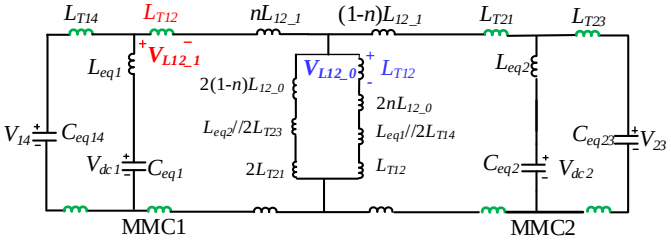


Fig. 8. The composite mode network under internal P-PTG faults.

Assuming the value of each CLR is V_T and the instantaneous MMC DC terminal voltages at fault instant are V_{dcn} (the rated DC voltage). Thus, the instantaneous values at fault instant of line-mode and zero-mode voltage across L_{T12} ($V^0_{L12\_1}$ and $V^0_{L12\_0}$) can be calculated (the reference direction of positive and negative reactor voltage is shown in Fig. 2):

$$\begin{cases} V^0_{L12\_1}=\dfrac{L_T V_{dcn}}{L_1+L_2//L_3//L_4}+\dfrac{-L_T V_{dcn}}{L_2+L_1//L_3//L_4}\times\dfrac{L_1//L_3//L_4}{L_1} \\ V^0_{L12\_0}=\dfrac{L_T V_{dcn}}{L_1+L_2//L_3//L_4}\times\dfrac{L_2//L_3//L_4}{L_3} \\ \qquad\qquad +\dfrac{L_T V_{dcn}}{L_2+L_1//L_3//L_4}\times\dfrac{L_1//L_3//L_4}{L_3} \end{cases} \tag{5}$$

where the inductances L_1, L_2, L_3 and L_4 can be expressed as:

$$\begin{cases} L_1=L_{eq1}//2L_T+2L_T+2nL_{12\_1} \\ L_2=L_{eq2}//2L_T+2L_T+2(1\text{-}n)L_{12\_1} \\ L_3=L_{eq1}//2L_T+2L_T+2nL_{12\_0} \\ L_4=L_{eq2}//2L_T+2L_T+2(1\text{-}n)L_{12\_0} \end{cases} \tag{6}$$

From equations (5)-(6), it can be concluded:

a) $V^0_{L12\_1}$ is positive and large under internal P-PTG faults.

b) $V^0_{L12\_0}$ is positive under internal P-PTG faults.

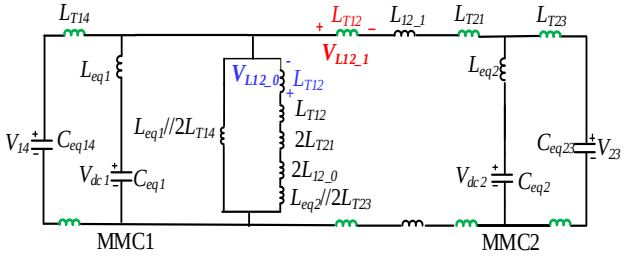
Similarly, for internal N-PTG faults, $V^0_{L12\_1}$ and $V^0_{L12\_0}$ can also be calculated as:

$$\begin{cases} V^0_{L12\_1}=\dfrac{L_T V_{dcn}}{L_1+L_2//L_3//L_4}+\dfrac{-L_T V_{dcn}}{L_2+L_1//L_3//L_4}\times\dfrac{L_1//L_3//L_4}{L_1} \\ V^0_{L12\_0}=\dfrac{-L_T V_{dcn}}{L_1+L_2//L_3//L_4}\times\dfrac{L_2//L_3//L_4}{L_3} \\ \qquad\qquad +\dfrac{-L_T V_{dcn}}{L_2+L_1//L_3//L_4}\times\dfrac{L_1//L_3//L_4}{L_3} \end{cases} \tag{7}$$

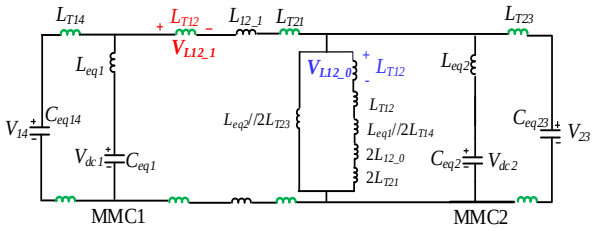
Equation (7) indicates that $V^0_{L12\_0}$ is negative under internal N-PTG faults.

2) *Fault Analysis under External PTG Faults*

Apply P-PTG faults at F_1 (backward external fault) and at F_2 (forward external fault) respectively. The composite mode networks under modal-domain at F_1 and F_2 are presented in Fig. 9.



(a) The composite mode network at F_1



(b) The composite mode network at F_2

Fig. 9. The composite mode networks under external P-PTG faults.

For F_1 and F_2, $V^0_{L12\_1}$ and $V^0_{L12\_0}$ can be obtained:

$$\begin{cases} V^0_{L12\_1}(F_1)=\dfrac{-L_TV_{dcn}}{L_5+\dfrac{L_6}{2}//L_7}+\dfrac{L_TV_{dcn}}{L_6+L_5//L_6//L_7}\times\dfrac{L_5//L_6//L_7}{L_5} \\ V^0_{L12\_0}(F_1)=\dfrac{-L_TV_{dcn}}{L_5+\dfrac{L_6}{2}//L_7}\times\dfrac{\dfrac{L_6}{2}//L_7}{L_7} \\ \qquad\qquad +\dfrac{-L_TV_{dcn}}{L_6+L_5//L_6//L_7}\times\dfrac{L_5//L_6//L_7}{L_7} \\ V^0_{L12\_1}(F_2)=\dfrac{L_TV_{dcn}}{L_8+\dfrac{L_9}{2}//L_{10}}+\dfrac{-L_TV_{dcn}}{L_9+L_8//L_9//L_{10}}\times\dfrac{L_8//L_9//L_{10}}{L_8} \\ V^0_{L12\_0}(F_2)=\dfrac{L_TV_{dcn}}{L_8+\dfrac{L_9}{2}//L_{10}}\times\dfrac{\dfrac{L_9}{2}//L_{10}}{L_{10}} \\ \qquad\qquad +\dfrac{L_TV_{dcn}}{L_9+L_8//L_9//L_{10}}\times\dfrac{L_8//L_9//L_{10}}{L_{10}} \end{cases} \tag{8}$$

where the inductances L_5-L_8 can be expressed as:

$$\begin{cases} L_5=L_{eq2}//2L_T+4L_T+2L_{12\_1} \\ L_6=L_{eq1}//2L_T \\ L_7=L_{eq1}//2L_T+4L_T+2L_{12\_0} \\ L_8=L_{eq1}//2L_T+4L_T+2L_{12\_1} \\ L_9=L_{eq2}//2L_T \\ L_{10}=L_{eq1}//2L_T+4L_T+2L_{12\_0} \end{cases} \tag{9}$$

From equations (5)-(9), it can be concluded:

a) $V^0_{L12\_1}$ under backward external fault (F_1) is negative while $V^0_{L12\_1}$ under forward external fault (F_2) is positive.

b) $V^0_{L12\_1}$ under internal PTG faults (F_{12}) is larger than that under internal PTG faults (F_2).

B. PTP Fault Analysis under Modal-domain

For PTP faults, the fault boundary condition is V_{fn}=V_{fp}, i_{fp}+i_{fn}=0. Using the phase-modal transformation, it can be re-written as:

$$\begin{cases} V_{f1}=0 \\ i_{f0}=0 \end{cases} \tag{10}$$

Based on the above fault boundary condition, the composite mode network under internal PTP faults can be obtained, as shown in Fig. 10.

$V^0_{L12\_1}$ and $V^0_{L12\_0}$ under internal PTP faults are:

$$\begin{cases} V^0_{L12\_1}=\dfrac{L_TV_{dcn}}{L_1} \\ V^0_{L12\_0}=0 \end{cases} \tag{11}$$

Equation (11) indicates that the $V^0_{L12\_0}$ is equal to zero under internal PTP faults. For external PTP faults, such as F_1 and F_2, $V^0_{L12\_1}$ can also be calculated by the composite mode network. The conclusion can be obtained:

a) $V^0_{L12\_1}$ under backward external fault (F_1) is negative while $V^0_{L12\_1}$ under forward external fault (F_2) is positive.

b) Due to the boundary effect of CLR on the change rate of fault current, the amplitude of $V^0_{L12\_1}$ under F_2 is smaller than that of $V^0_{L12\_1}$ under F_{12}.

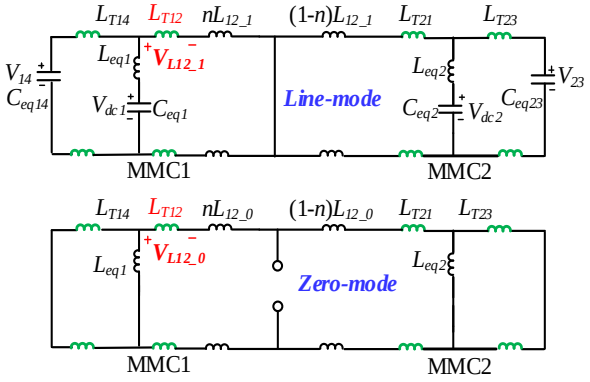


Fig. 10. The composite mode network under internal PTP faults.

IV. The Overall Protection Scheme based on Line-mode and Zero-mode Reactor Voltage

A. Fault Detection based on Line-mode Reactor Voltage

Based on above modal-domain analysis, the characteristics of $V^0_{Lmn\_1}$ under different faults can be obtained, as shown in Table 2.

Table 2 The characteristics of $V^0_{Lmn\_1}$ under different faults

Fault position		$V^0_{Lmn\_1}$	
		Polarity	Amplitude
internal faults		Positive	Large
external faults	reverse	Negative	/
	forward	Positive	Small

During fault initial stage (within 0.5ms subsequent to DC faults), though voltages of sub-module capacitors decrease, line-mode reactor voltages under backward external faults are always negative but positive under forward faults. Meanwhile, line-mode reactor voltages under forward external faults are always smaller than those under internal faults, due to the boundary effect of CLR. Thus, the fault detection criterion for relay CB*mn* can be designed using the line-mode reactor voltage of line *mn* (V_{Lmn_1}):

$$V_{Lmn\_1}>V_{set} \tag{12}$$

where V_{set} is the threshold for fault detection. As can be seen from equation (2), the line-mode reactor voltage combines the fault characteristics of negative and positive reactor voltages. For PTG faults, negative and positive reactor voltages under internal faults are both larger than those under external faults. Thus, line-mode reactor voltage enlarges the differences between internal and external faults, therefore improving the robustness for fault detection.

B. Faulted Pole Selection based on Zero-mode Reactor Voltage

Table 3 represents the characteristics of voltage $V^0_{L12\_0}$ based on modal-domain analysis for internal faults. As can be seen,

the polarity of $V^{0}_{L12\_0}$ for each fault type is unique and it will remain constant during fault initial stage. Thus, the faulted pole selection criterion for relay CB*mn* can be designed using the zero-mode reactor voltage of line *mn* (V_{Lmn_0}):

$$\begin{cases} V_{Lmn\_0} > \lambda & \Rightarrow P-PTG \quad faults \\ -\lambda < V_{Lmn\_0} < \lambda & \Rightarrow PTP \quad faults \\ V_{Lmn\_0} < -\lambda & \Rightarrow N-PTG \quad faults \end{cases} \tag{13}$$

where λ is a positive coefficient and the specified value can be obtained by the simulations.

Table 3 The characteristics of $V^{0}_{L12\_0}$ for internal faults

Fault type	$V^{0}_{L12\_0}$	
	Amplitude	Polarity
PTP faults	0	/
P-PTG faults	$\frac{L_T V_{dcn}}{L_1+L_2//L_3//L_4}\times\frac{L_2//L_3//L_4}{L_3}+\frac{L_T V_{dcn}}{L_2+L_1//L_3//L_4}\times\frac{L_1//L_3//L_4}{L_3}$	positive
N-PTG faults	$\frac{-L_T V_{dcn}}{L_1+L_2//L_3//L_4}\times\frac{L_2//L_3//L_4}{L_3}+\frac{-L_T V_{dcn}}{L_2+L_1//L_3//L_4}\times\frac{L_1//L_3//L_4}{L_3}$	negative

C. The Modified Criteria with Anti-Noise Capability

Noise is an interference source signal generated from the equipment or system. Signal noise ratio (SNR) is commonly employed to represent the relationship between original signal and noise signal:

$$SNR = 10\lg\frac{P_s}{P_{noise}}(\text{db}) \tag{14}$$

where P_s is the power of original signal and P_{noise} is the power of noise.

For DC grid system shown in Fig. 1, the waveform of DC voltage V_{dc12} with 20db noise is shown in Fig. 11.

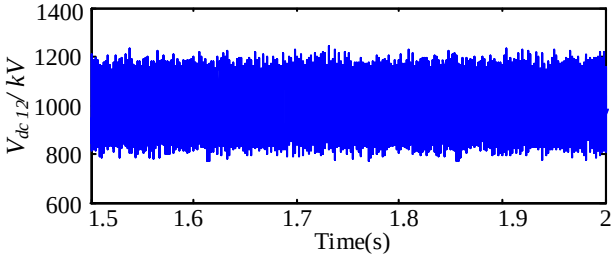


Fig. 11. The waveform of DC voltage added 20db noise.

In Fig. 11, the measurement of the original DC voltage signal will be affected by noise.

As pointed out by [23], the mean value of white noise is zero. To mitigate the impact of noise, the integral method is employed to modify the criterion:

$$\int V_{Lmn\_1(0)} = \int_0^{T_w} V_{Lmn\_1(0)}dt \tag{15}$$

where T_w is the time window for integral process. To guarantee the reactor voltage constantly rise during the integral process, T_w is selected as 0.5ms in this paper.

The waveforms of integration of voltage V_{L12_1} ($\int V_{L12\_1}$) without noise and with 20db noise are shown in Fig. 12. As can be seen, the integral method can be adopted to improve the robustness to noise.

$$\int V_{Lmn\_1(0)} = \int_0^{T_w} V_{Lmn\_1(0)}dt \tag{16}$$

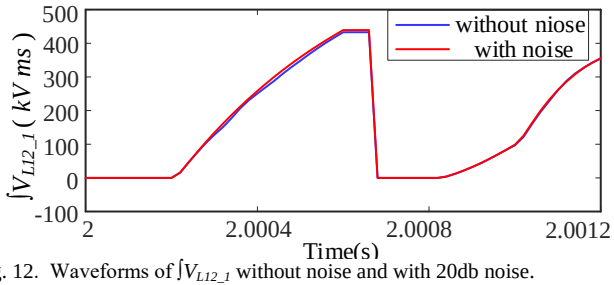


Fig. 12. Waveforms of $\int V_{L12\_1}$ without noise and with 20db noise.

The modified criterion for the selection of the faulted pole using the integral method is expressed as:

$$\begin{cases} \int V_{Lmn\_0} > \lambda_{set} & \Rightarrow P-PTG \quad faults \\ -\lambda_{set} < \int V_{Lmn\_0} < \lambda_{set} & \Rightarrow PTP \quad faults \\ \int V_{Lmn\_0} < -\lambda_{set} & \Rightarrow N-PTG \quad faults \end{cases} \tag{17}$$

where λ_{set} is the threshold for the faulted pole selection and the determination of λ_{set} will be conducted in section V.A.

To determine the beginning time of the integral process, the rate of change of DC voltage (ROCOV) is employed as the fault start-up element. The subsequent protection will be activated when the following equation holds true:

$$dV_{dc}/dt < D_{Vdc} \tag{18}$$

where D_{Vdc} is the setting threshold of the start-up element and the determination of D_{Vdc} will be conducted in section V.A.

D. The Flow Chart of the Overall Protection Scheme

Based on the above analysis, the overall protection scheme can be obtained, as shown in Fig. 13.

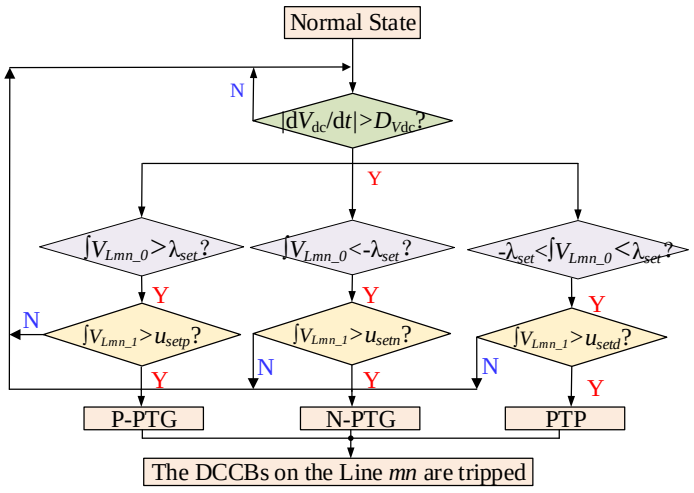


Fig. 13. The flow chart of the proposed protection method.

Once the criterion (18) holds true, the fault start-up element will be activated and the subsequent protection scheme will be conducted. In Fig. 13, $u_{setp(n)}$ and u_{setd} represent the setting thresholds of $\int V_{Lmn\_1}$ under PTG and PTP faults respectively. Considering that there exist different setting thresholds for fault detection under different fault types, such as $u_{setp(n)}$ and u_{setd}, the faulted pole will be selected first. On detecting $\int V_{Lmn\_0} > \lambda_{set}$ and $\int V_{Lmn\_1} > u_{setp}$, an internal P-PTG fault is

identified. On detecting $\int V_{Lmn\_0} < -\lambda_{set}$ and $\int V_{Lmn\_1} > u_{setn}$, an internal N-PTG fault is identified. On detecting $-\lambda_{set} < \int V_{Lmn\_0} < \lambda_{set}$ and $\int V_{Lmn\_1} > u_{setd}$, an internal PTP fault is identified.

V. Simulation and Verification

In order to verify the feasibility and effectiveness of the proposed method, a ±500kV four-terminal MMC based DC grid shown in Fig. 1 is built in PSCAD/EMTDC. The current-limiting reactor is selected as 0.15H [6]. The other converter parameters are listed in Table 4. MMC1 controls the DC link voltage while other converters control the transmitted power.

Table 4 Parameters of each converter station

Converter	MMC1	MMC2	MMC3	MMC4
arm inductance / mH	96	144	115	192
sub-module capacitor / mF	15	10	12.5	8
sub-module number / *N*	200	200	200	200
rate power / MW	3000	2000	2500	1500

A. Determination of Setting Value

Taking the relay of CB12 as an example, the threshold setting calculation will be conducted as follows.

1) *Threshold Setting for Start-up Element*

To determine the beginning time of the integral process ($\int V_{Lmn\_1}$), the rate of change of DC voltage (dV_{dc}/dt) is employed as the fault start-up element. The fault start-up element can be activated when $dV_{dc}/dt < D_{Vdc}$. The principle to select the D_{Vdc} is as follows:

D_{Vdc} should be selected to avoid activation during normal operation and it should be activated during DC fault conditions. Thus, to cover all internal faults, D_{Vdc} should be larger than the observed maximum value of dV_{dc}/dt during internal faults. However, to enable fast detection, the selection of D_{Vdc} should leave a margin so that the protection scheme can be activated as soon as possible.

Based on the above principle, taking DCCB 12 as an example, scan different DC bus faults and line faults along OHL12 and OHL 41. Then, the voltage derivatives dV_{dc}/dt under DC faults are obtained in Table 5.

In Table 5, the R-PTP and R-PTG represent the PTP fault with 200Ω fault resistance and PTG fault with 200Ω fault resistance respectively. As shown in Table 5, for internal faults, the maximum value of dV_{dc}/dt is -1200kV/ms. Based on the above principle, D_{Vdc} should not exceed -1200kV/ms. Besides, to activate the following protection scheme as fast as possible, D_{Vdc} is selected as -200 kV/ms.

2) *Threshold Setting for Faulted Pole Selection*

According to (17), the positive coefficient λ_{set} should satisfy the following requirements to select the faulted pole: For PTP faults, $|\int V_{Lmn\_0}|$ should be much smaller than λ_{set}. In addition, $\int V_{Lmn\_0}$ should be much larger than λ_{set} for P-PTG faults but much smaller than $-\lambda_{set}$ for N-PTG faults, as illustrated in Fig. 14.

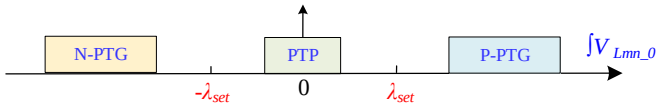


Fig. 14. The principle to select the positive coefficient λ.

Based on the above principle, taking DCCB12 as an example, scan different DC line PTP and P-PTG faults along OHL12 respectively. Then, $\int V_{L12\_0}$ under different DC faults are obtained in Table 6.

Table 5 Measured values of dV_{dc}/dt under different DC faults(kV/ms)

Faults	F_1				The head of OHL14				The end of OHL14			
	PTP	R-PTP	PTG	R-PTG	PTP	R-PTP	PTG	R-PTG	PTP	R-PTP	PTG	R-PTG
dV_{dc}/dt (kV/ms)	-1117	-612	-210	-170	-2103	-600	-200	-100	-1174	-121	-68	-30
Faults	The head of OHL12				The end of OHL12							
	PTP	R-PTP	PTG	R-PTG	PTP	R-PTP	PTG	R-PTG				
dV_{dc}/dt (kV/ms)	-7000	-5014	-2543	-1577	-4044	-3132	-1899	**-1200**				

Table 6 the simulation values of $\int V_{L12\_0}$ under different DC faults

Location	$\int V_{L12\_0}$			
	Metallic PTP faults	PTP faults with 200Ω resistance	Metallic PTP faults	PTP faults with 200Ω resistance
The head of OHL12	-0.00353	-0.00351	102	62
1/4 of OHL12	-0.00384	-0.00183	106	64
1/2 of OHL12	0.00393	0.00396	124	60
3/4 of OHL12	0.00752	0.00755	110	63
The end of OHL12	0.01085	0.01087	110	68

As can be seen from Table 6, $|\int V_{Lmn\_0}|$ under PTP faults are very close to zero. In addition, $\int V_{Lmn\_0}$ under P-PTG faults with 200Ω resistance are around 60 *kV*ms*. Thus, λ_{set} can be obtained: $\lambda_{set} = k_{rel} \times 60$. In this paper, k_{rel} is selected as 1/3. Finally, λ_{set} can be calculated as 20 *kV*ms*.

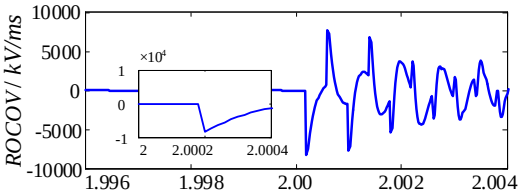
3) *Threshold Setting for Fault Detection*

V_{set} should be smaller than the minimum value under internal faults but larger than the maximum value under external faults. For relay CB12, the maximum value under external faults can be obtained under F_2 fault. Applying metallic PTP and P-PTG faults at F_2 respectively, the simulation values of $\int V_{L12\_1}$ are 239 *kV*ms* (for PTP faults) and 45 *kV*ms* (for P-PTG faults) respectively. Considering 200Ω resistance and a certain margin, V_{setd} (for PTP faults) and $V_{setn(p)}$ (for P-PTG faults) are selected as 275 *kV*ms* and 68 *kV*ms*.

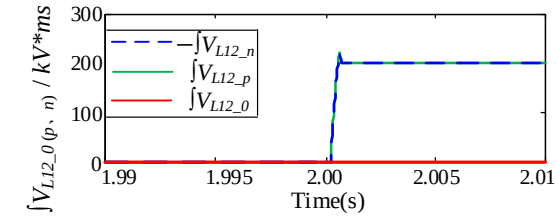
B. Simulation Analysis for Different Faults

1) *Simulation Analysis under PTP Faults*

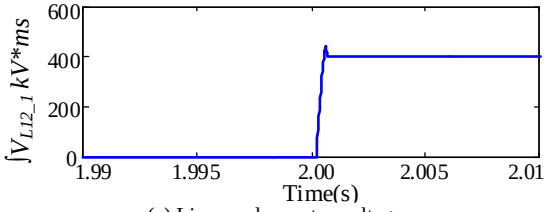
At 2.0s, a metallic PTP fault is applied at 25% of OHL12 and the simulation waveforms are shown in Fig. 15.



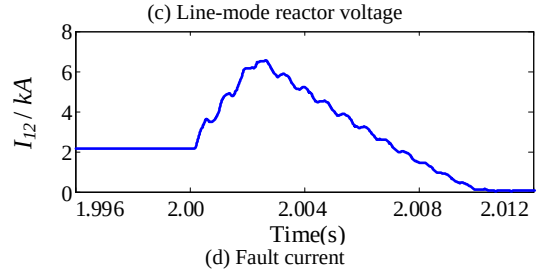
(a) ROCOV



(b) Zero-mode and negative and positive reactor voltages



(c) Line-mode reactor voltage



(d) Fault current

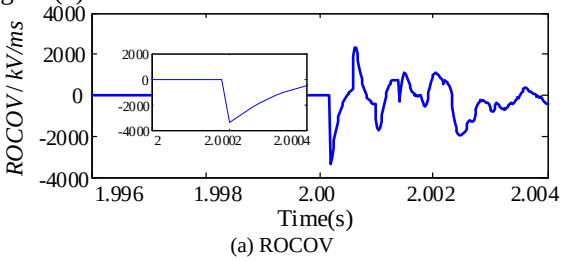
Fig. 15. Simulation waveforms of voltage and current under a metallic PTP fault.

As shown in Fig. 15 (a), the ROCOV is smaller than -200 *kV/ms*. Thus, the start-up element is activated. In Fig. 15 (b) and Fig. 15 (c), -20 *kV*ms* < $\int V_{L12\_0}$ < 20 *kV*ms*, and $\int V_{L12\_1}$>275 *kV*ms*. Hence, it is deemed to be an internal PTP fault. In Fig. 15 (d), the fault current I_{12} rapidly rises to around 6kA. Subsequent to trip of DCCB12, the current I_{12} begins to decrease and decays to zero within 8ms.

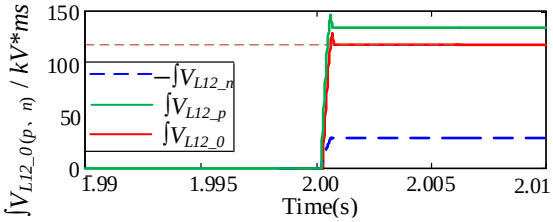
2) *The Simulation Analysis under P-PTG Fault*

At 2.0s, a metallic P-PTG fault is applied in the middle of OHL12 and the simulation waveforms are shown in Fig. 16.

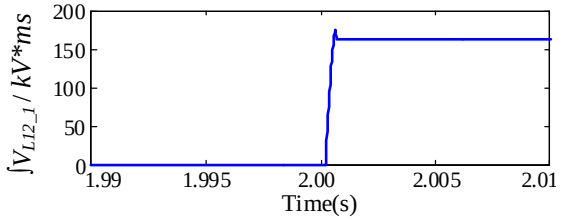
As shown in Fig. 16(a), the ROCOV is smaller than -200 *kV/ms*. Thus, the start-up element is activated. In Fig. 16(b) and Fig. 16(c), $\int V_{L12\_0}$ > 20 *kV*ms* and $\int V_{L12\_1}$>68 *kV*ms*. Hence, it is deemed to be an internal P-PTG fault. The fault current I_{12} rises to around 3kA. Subsequent to trip of DCCB12, I_{12} begins to decrease and decays to zero within 6ms, as shown in Fig. 16(d).



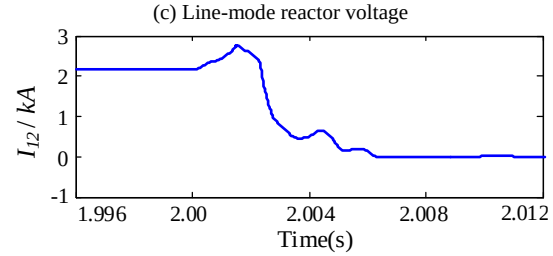
(a) ROCOV



(b) Zero-mode and negative and positive reactor voltages



(c) Line-mode reactor voltage

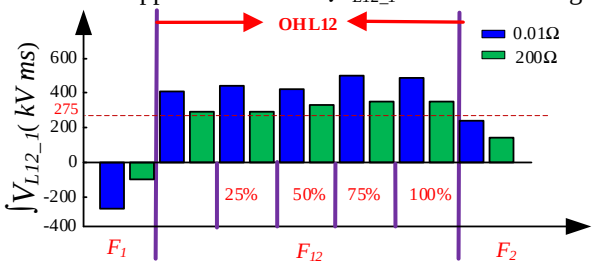


(d) Fault current

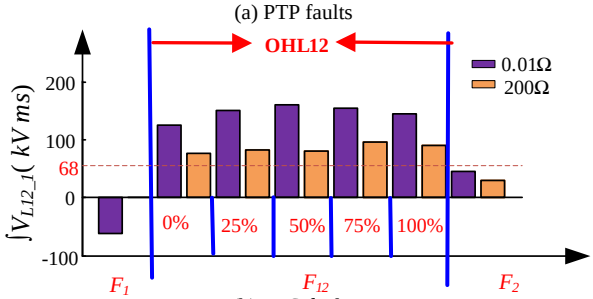
Fig. 16. Simulation waveforms of voltage and current under a metallic P-PTG fault.

C. Influence of Fault Resistance

To verify the influence of fault resistance on the proposed method, PTP and P-PTG faults with different locations and resistances are applied. Values of $\int V_{L12\_1}$ are shown in Fig. 17.



(a) PTP faults



(b) PTG faults

Fig. 17. The values of $\int VL12\_1$ under faults with different resistances.

As shown in Fig. 17, $\int V_{L12\_1}$ decreases with the increase of fault resistance. However, when the fault resistance is no more than 200Ω, $\int V_{L12\_1}$ under internal faults are always larger than the threshold while $\int V_{L12\_1}$ under external faults are still smaller than it. Thus, the proposed method can identify faults with 200Ω resistance.

D. Detection Time

Traveling wave induced from fault point takes some time to arrive at the measurement position. Meanwhile, high-resistance faults require longer time to activate the start-up element and exceed the threshold for fault detection. Thus, a P-PTG fault with 200Ω resistance at the end of OHL12 is applied to obtain the longest detection time at 2.0s. The result is shown in Table 7 and the state of DCCB12 is shown Fig. 18 ("*1*" represents the tripping of DCCBs). The simulation results demonstrate that the longest detection time

is less than 1.1ms. Thus, the scheme is fast for fault detection.

Table 7 The detection time of the different protection

Parameter		Value
Fault resistance		200Ω
Fault position		at the end of OHL12
Start-up	Propagation time of traveling-wave	0.8*ms*
	Total delay for fault start-up element	0.82*ms*
Total Detection Delay		1.04*ms*

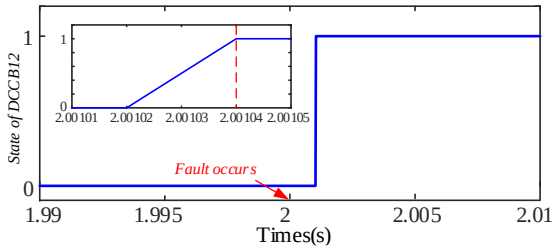


Fig. 18. The state of DCCB12 under P-PTG fault with 200Ω resistance at the end of OHL12.

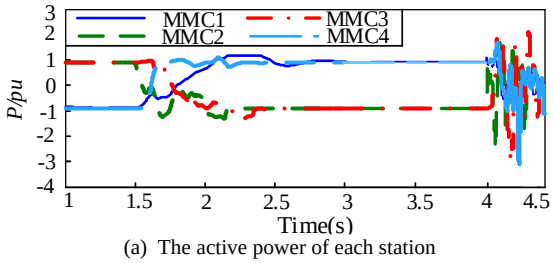
VI. Robust Analysis

A. Influence of Change of Operation Mode

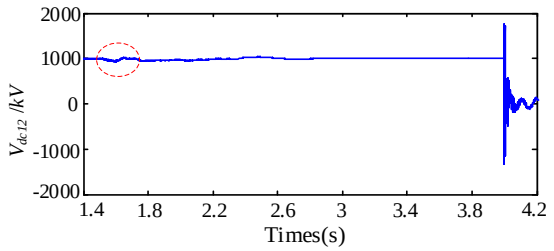
Further studies are conducted to test the impact of change of operation mode on the proposed protection strategy. At 1.5s, active power of each converter reverses. At 2.0s, the system power recovers to steady state, as shown in Fig. 19(a). At 4s, a metallic PTP fault is applied in the middle of OHL12.

In Fig. 19(b), although power reversal causes a large power fluctuation, the fluctuation of DC line voltage is small and the start-up element is not activated. After power reversal, a PTP fault occurs in the middle of OHL12. The DC voltage drops rapidly and the start-up element is activated. Since $\int V_{L12\_1}$ is larger than 275*kV*ms*, the fault can be identified to be internal correctly, as shown in Fig. 19 (c).

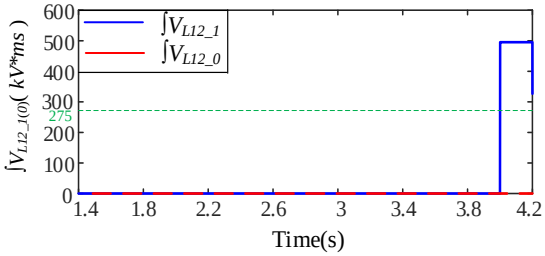
To be concluded, power reversal has no influence on the proposed scheme.



(a) The active power of each station



(b) The DC line voltage V_{dc12}



(c) Zero-mode and line-mode reactor voltages

Fig. 19. The simulation waveforms under power reversal.

B. Influence of Noise

To test the influence of noise, a 10db white noise is added into the measured signals and a metallic PTP fault is applied at F_2. The waveform $\int V_{L12\_1}$ is shown in Fig. 20.

As can be shown, $\int V_{L12\_1}$ is always smaller than 275 *kV*ms*. Thus, the fault is identified to be external.

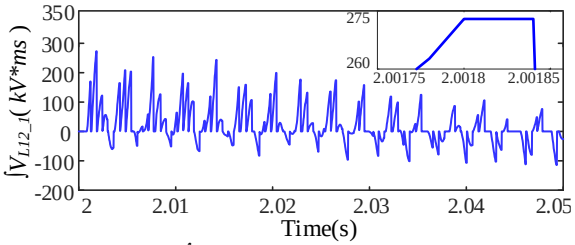


Fig. 20. The waveform of $\int V_{L12\_1}$ when the SNR is 10db.

More simulation cases with 10db, 20db, and 30db noise are conducted and the simulation results are shown in Table 8. To be concluded, the protection scheme has strong anti-noise ability and can achieve fault detection under 10db noise disturbance.

Table 8 Influence of noise with different SNR on the proposed protection

SNR (db)	The situation of protection
10	No action
20	No action
30	No action

C. Influence of DCCB Operation

At 2s, a metallic PTP fault is applied in the middle of OHL14, and tripping orders are issued to DCCB14 and DCCB41 at 2.0005s. To test the influence of DCCB14 and DCCB41 operation on relay CB12, $\int V_{L12\_1}$ is measured, as shown in Fig. 21.

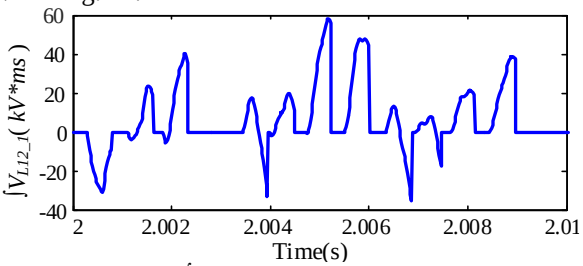


Fig. 21. The waveform of $\int V_{L12\_1}$ when DCCB14 and DCCB41 are tripped.

During the trip of DCCB14 and DCCB41, $\int V_{L12\_1}$ is always smaller than 275 *kV*ms*, which will not bring about the false operation of relay CB12. Thus, DCCB operation has no impact on the relay CB12.

D. Influence of the Size of CLR

Voltage of C LR is proportional to the size of CLR. Thus, small CLR will lead to difficulty of threshold setting. Meanwhile, the smaller the CLR, the less obvious the

boundary characteristics. For further study on influence of the size of CLR, reactors vary from the 100mH to 200mH, and internal PTP faults with 200Ω resistance and external metallic PTP faults are applied respectively. Simulation results are shown in Fig. 22, where the fault position -0.25 represents the F_2 fault.

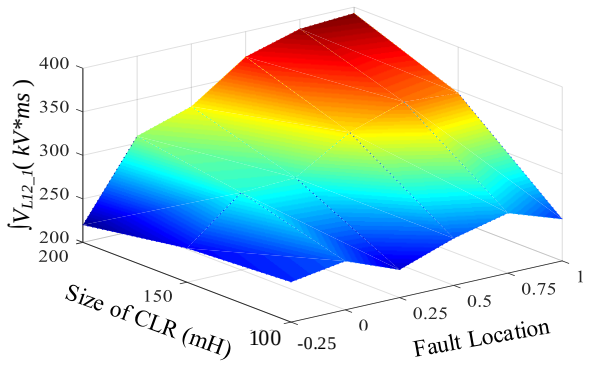


Fig. 22. The value of $\int V_{L12\_1}$ under different faults with different reactors.

In Fig. 22, when CLR is 100mH, the difference of $\int V_{L12\_1}$ between external and internal faults is small, leading to the decreased detection accuracy to fault resistance. With the increase of CLR size, difference of $\int V_{L12\_1}$ becomes more obvious and the robustness of the protection scheme enhances.

E. Response to AC Faults

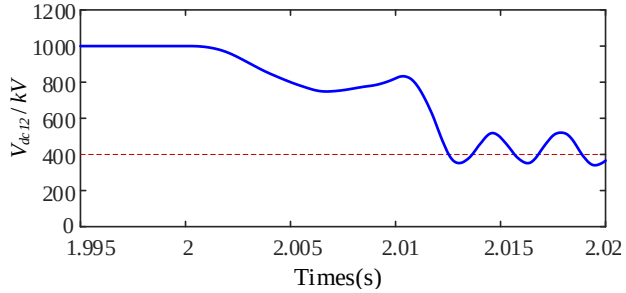
To test the impacts of AC faults on DC fault protection, a metallic three-phase AC fault F_{AC1} is applied at the secondary side of power transformers close to AC system S1 at 2.0s, as shown in Fig. 23.

In Fig. 23(a) and (b), the DC line voltage V_{dc12} drops slowly during initial stage of AC fault and the rate of change of DC voltage dV_{dc12}/dt is less than -200 *kV/ms* at 2.012s, thereby triggering the fault start-up element. The integral of the change of DC line voltage ($\int|\Delta V_{dc12}|$) under this circumstance is 186 *kV*ms*, which is larger than that under the PTG DC fault with 200Ω resistance at the end of OHL12. The specific comparison is presented in Fig. 23(c) and Fig. 24 (b), which demonstrates that $\int|\Delta V_{dc12}|$ cannot identify the internal DC faults and AC faults.

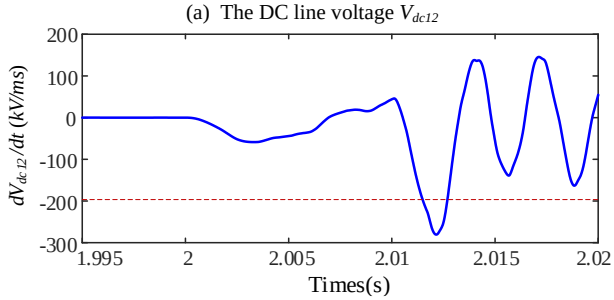
In addition, in Fig. 23(a), the minimum value of DC line voltage V_{dc12} is 352kV under AC fault while it is larger than 400kV under DC fault, as shown in Fig. 24 (a). Thus, the low-voltage criterion is also sensitive to AC faults.

However, the measured $\int V_{L12\_1}$ under AC fault F_{AC1} is negative, as shown in Fig. 23(b). Hence, the AC fault F_{AC1} will be deemed to be external and it will not lead to the false operation of the proposed method.

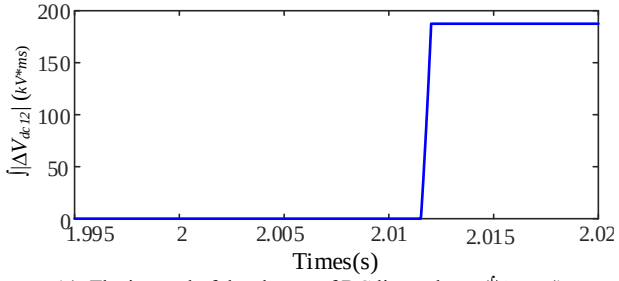
To further verify the robustness of the proposed method to AC faults, a metallic three-phase AC fault F_{AC2} is tested at AC system S2. When the AC short circuit fault F_{AC2} occurs, the DC line voltage will have a small fluctuation and not activate the start-up element. Thus, the proposed protection scheme is not affected by AC faults.



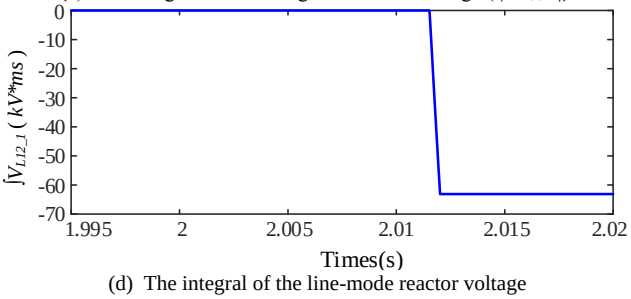
(a) The DC line voltage V_{dc12}



(b) The rate of change of DC voltage dV_{dc12}/dt

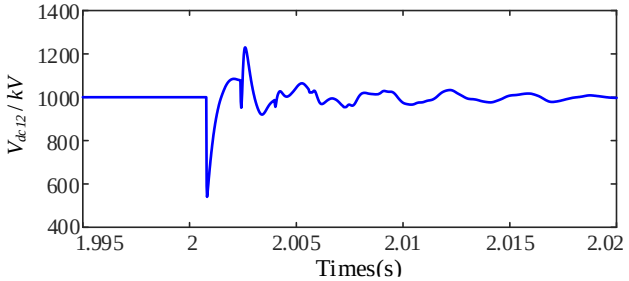


(c) The integral of the change of DC line voltage ($\int|\Delta V_{dc12}|$)

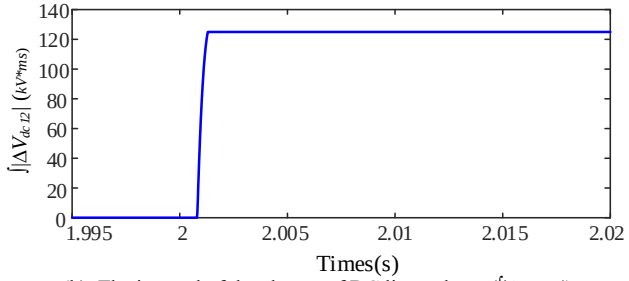


(d) The integral of the line-mode reactor voltage

Fig. 23. The simulation waveforms under a metallic AC fault at S1.



(a) The DC line voltage V_{dc12}



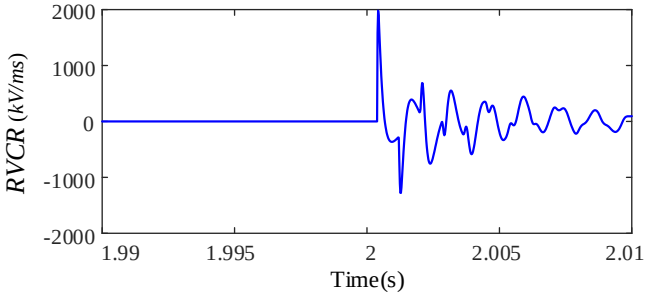
(b) The integral of the change of DC line voltage ($\int|\Delta V_{dc12}|$)

Fig. 24. The simulation waveforms under a PTG fault with 200Ω resistance at the end of OHL12.

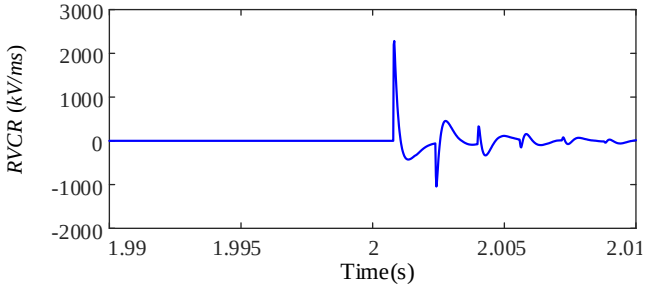
F. Comparison with Other Protection Methods

1) *The DC Reactor Voltage Change Rate (RVCR) Method in [12]*

The topology for the simulation is shown in Fig. 1 and the specific parameter is shown in Table 4. Taking DCCB 12 as an example, apply a P-PTG fault with 200Ω resistance in the middle of OHL12 (F_{12}) at 2s. The measured RVCR is 2000kV/ms, as shown in Fig. 25 (a). Apply a metallic P-PTG fault at F_2 at 2s. The measured RVCR is 2284kV/ms, as shown in Fig. 25 (b). It can be seen that the RVCR during an external fault F_2 is higher than that during an internal fault (F_{12}). Thus, the RVCR cannot be applied to the P-PTG faults.



(a) RVCR during internal fault (F_{12})

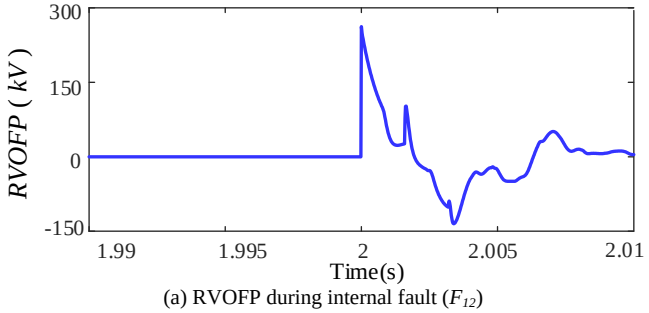


(b) RVCR during external fault (F_2)

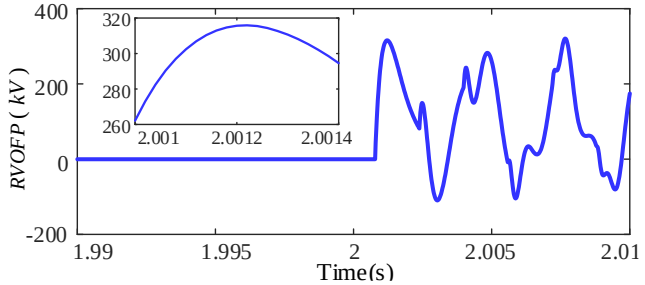
Fig. 25. Simulation results using RVCR method.

2) *The DC Reactor Voltage Method in [13]*

Taking DCCB 12 as an example, apply a PTG fault with 100Ω resistance at the head of OHL12 (F_{12}) at 2s. The measured reactor voltage of faulted pole (RVOFP) is smaller than 300kV, as shown in Fig. 26 (a). Apply a metallic PTP fault at F_2 at 2s. The measured RVOFP exceeds 300kV, as shown in Fig. 26 (b). It can be seen the RVOFP during an external fault F_2 is higher than that during an internal fault (F_{12}). Thus, using the RVOFP criterion, the internal faults with high fault resistance cannot be identified.



(a) RVOFP during internal fault (F_{12})

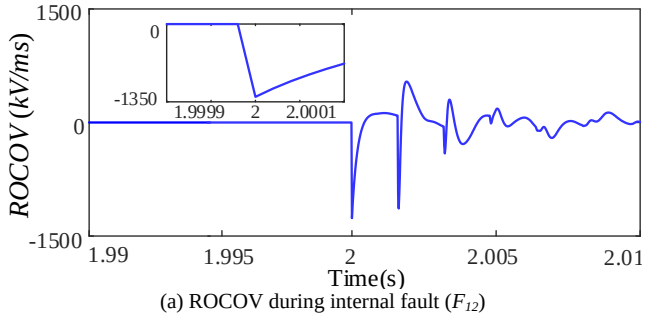


(b) RVOFP during external fault (F_2)

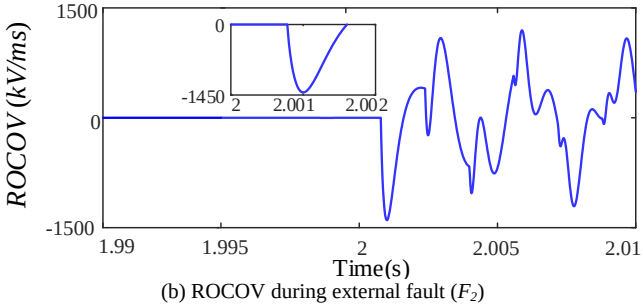
Fig. 26. Simulation results using RVCR method.

3) *The Rate of Change of Voltage (ROCOV) Method in [9]*

Taking DCCB 12 as an example, applying a PTG fault with 200Ω resistance at the head of OHL12 (F_{12}) and a metallic PTP fault at F_2 at 2s respectively, the measured ROCOVs are shown in Fig. 27.



(a) ROCOV during internal fault (F_{12})

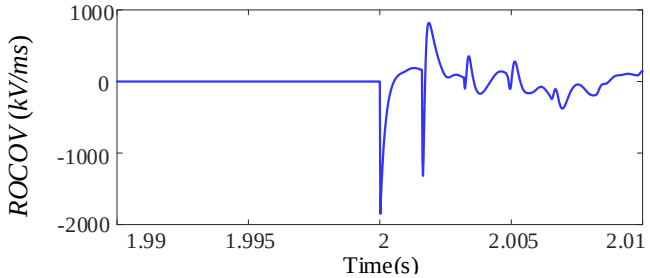


(b) ROCOV during external fault (F_2)

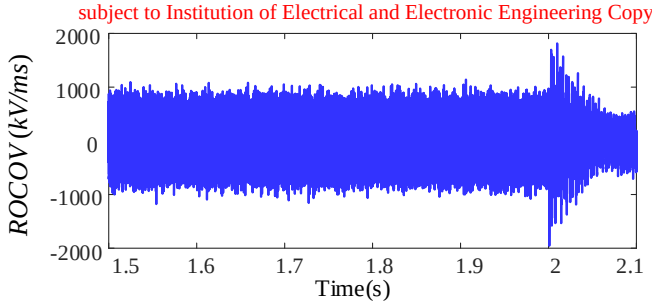
Fig. 27. Simulation results using ROCOV with different fault resistances.

It can be seen that measured ROCOV at F_{12} is larger than that at F_2, which demonstrates that the ROCOV based method cannot work under high fault resistance.

Applying a metallic P-PTG fault at head of OHL12 (F_{12}) and a metallic PTP fault with 20db noise at F_2 respectively, the measured ROCOVs are shown in Fig. 28. It can be seen that measured ROCOV at F_{12} is larger than that at F_2, which demonstrates that the ROCOV based method is vulnerable to noise.



(a) ROCOV during internal fault (F_{12})



(b) ROCOV during external fault (F_2)

Fig. 28. Simulation results using ROCOV with noise.

VII. Conclusion

A fast and selective protection scheme based on modal-domain analysis for overhead MMC based DC grids is proposed in this paper. Using the modal-domain analysis, the dependency of positive and negative poles of overhead lines is decoupled. From the theoretical analysis and simulations, it can be concluded that,

1) The PTG and PTP fault analysis under modal-domain are conducted respectively, which provides the theoretical basis for the design of protection algorithm.

2) The derivative of DC line voltage (dV_{dc}/dt) is adopted as the start-up element. Then, the zero-mode reactor voltage ($\int V_{L12\_0}$) is employed to select the faulted pole. The line-mode reactor voltage ($\int V_{L12\_0}$) is employed to identify the internal and external faults.

3) The proposed method can identify faults with fault resistance as high as 200Ω and it is immune to noise with 10dB. By only using local measurements, the proposed protection scheme is fast, no more than 1.1ms. In addition, the method is not affected by DCCB interruptions, operating conditions and AC faults. Quantities of simulation results demonstrate that the smaller current-limiting reactor will reduce the sensitivity to fault resistance and the protection can work well when the CLR is larger than 100mH.

4) In comparison with similar schemes, such as RVCR, RVOFP and ROCOV, the proposed method has advantages over the capability of the faulted pole selection, the robustness to high-resistance and noise disturbance.

References

[1] W. Xiang, R. Yang, C. Lin, et al., "A Cascaded Converter Interfacing Long Distance HVDC and Back-to-Back HVDC Systems," *IEEE Journal of Emerging and Selected Topics in Power Electron*., early access, doi: 10.1109/JESTPE.2019.2913915.

[2] X. Li, Q. Song, W. Liu, et al., "Experiment on DC-fault ride through of MMC using a half-voltage clamp submodule," *IEEE Journal of Emerging and Selected Topics in Power Electron*., vol. 6, no. 3, pp. 1273-1279, Sept. 2018.

[3] W. Xiang, W. Lin, T. An, et al, "Equivalent Electromagnetic Transient Simulation Model and Fast Recovery Control of Overhead VSC-HVDC Based on SB-MMC," *IEEE Trans. Power Del*., vol. 32, no. 2, pp. 778-788, Apr. 2017.

[4] T. An, G. Tang, W. Wang, "Research and application on multi-terminal and DC grids based on VSC-HVDC technology in China," *IET High Voltage*, vol. 2, no. 1, pp. 1-10, Jun. 2017.

[5] G. Liu, F. Xu, Z. Xu, et al, "Assembly HVDC breaker for HVDC grids with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 931–941, Feb. 2017.

[6] M. Zhou, W. Xiang, W. Zuo, W. Lin, J. Wen, "A novel HVDC circuit breaker for HVDC application," *Int. J. Elect. Power Energy Syst.*, Vol. 109, pp. 685-695, 2019.

[7] W. Xiang, S. Yang, L. Xu, et al, "A transient voltage based DC fault line protection scheme for MMC based DC grid embedding DC breakers," *IEEE Trans. Power Del*., vol. 34, no. 1, pp. 334-345, Feb. 2019.

[8] N. Geddada, Y. M. Yeap, A. Ukil, "Experimental Validation of Fault Identification in VSC-Based DC Grid System," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4799-4809, June 2018.

[9] J. Sneath, A. Rajapakse, "Fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid DC breakers," *IEEE Trans. Power Del.*, vol.31, no.3, pp. 973-981, Jun. 2016.

[10] Q. Huang, G. Zou, X. Wei, et al., "A non-unit line protection scheme for MMC-based multi-terminal HVDC grid," *Int. J. Elect. Power Energy Syst.*, vol. 107, pp. 1-9, 2019.

[11] Q. Yang, S. L. Blond, R. Aggarwal, et al, "New ANN method for multi-terminal HVDC protection relaying," *Electr. Power Syst. Research*, vol. 148, pp. 192-201, 2017.

[12] R. Li, L. Xu, L. Yao, "DC fault detection and location in meshed multi-terminal HVDC systems based on DC reactor voltage change rate," *IEEE Trans. Power Del.*, vol.32, no.3, pp. 1516-1626, Jun. 2017.

[13] C. Li, A. M. Gole, C. Zhao, "A fast DC fault detection method using DC reactor voltages in HVdc Grids," *IEEE Trans. Power Del.*, vol. 33, no. 5, pp. 2254-2264, Oct. 2018.

[14] W. Leterme, S. Pirooz Azad, D. Van Hertem, "HVDC grid protection algorithm design in phase and modal-domains," *IET Renewable Power Gener*., vol. 12, no. 13, pp. 1538-1546, Sept. 2018.

[15] L. Tang, X. Dong, S. Shi, et al., "A high-speed protection scheme for the DC transmission line of a MMC-HVDC grid," *Elect. Power Syst. Research*, vol. 168, pp. 81-91, 2019.

[16] M. Kong, X. Pei, H. Pang, et al, "A lifting wavelet-based protection strategy against DC line faults for Zhangbei HVDC Grid in China," *19th European Conf. on Power Electron. and Applica. (EPE'17 ECCE Europe)*, Warsaw, Poland, Sept. 2017, pp. 1-11.

[17] E. Kontos, R. T. Pinto, S. Rodrigue, et al, "Impact of HVDC transmission system topology on multiterminal DC network faults," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp.844-852, Apr. 2015.

[18] J. Yang, J. E. Fletcher, J. O. Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827-3837, Oct. 2012.

[19] C. Li, C. Zhao, J. Xu, et al, "A pole-to-pole short-circuit fault current calculation method for DC grids," *IEEE Trans. Power Syst.*, vol. 32, no. 6, pp. 4943–4953, Nov. 2017.

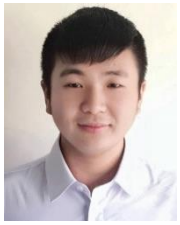
[20] T. Wang, G. Song, L. Wu, et al., "Novel reclosure scheme of MMC-HVDC system based on characteristic signal injection," *The Journal of Engineering*, vol. 2019, no. 16, pp. 1153-1157, Mar. 2019.

[21] H. Li, Z. He, J. Yang, et al, "Switching overvoltage analysis for modular multilevel converters," *High Voltage*, vol. 43, no. 4, pp. 1144-1151, Apr. 2017.

[22] E. D. Kimbark, "Transient overvoltages caused by monopolar ground fault on bipolar DC line: theory and simulation," *IEEE Trans. Power Appar. Syst.*, vol. 89, no. 4, pp. 584-592, Apr. 1970.

[23] J. Zhang, C. Y. Chung and L. Guan, "Noise Effect and Noise-Assisted Ensemble Regression in Power System Online Sensitivity Identification," *IEEE Trans. Ind. Informat.*, vol. 13, no. 5, pp. 2302-2310, Oct. 2017.

Biographies



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