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Structural and electrical properties of Si/Ge heterostructures with various surface orientations

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Submitted By

Mohammad Mahfuz Alam

Student ID No. : 1691303

Department of Electrical and Electronic Engineering

Tokyo City University
Japan

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Declaration

This thesis is submitted to the Tokyo City University in support of my application for the degree of Doctor of Philosophy. All experimental data presented was carried out by the author, or by specialists under the author’s direction.

Abstract

Strained Ge and Ge-rich $Si_{1-x}Ge_x$ on a Si platform with (111) surface orientation has been attracting intensive attentions due to the superiority to enhance mobility for n-type channel MOS than other plane orientations and also highly applicable to spintronic devices owing to the epitaxial growth of high-quality ferromagnetic materials on Ge(111) and SiGe(111). For this purpose, their strain states and thermal stabilities are systematically evaluated and critical thickness (t_c) of Ge-rich $Si_{1-x}Ge_x$ on Ge-on-Si(111), Ge(111) and Ge(100) substrates are precisely determined. For precise determination of t_c, an initial stage of the strain relaxation of $Si_{1-x}Ge_x$ layers is systematically investigated in detail in terms of strain states together with surface morphologies. It was found that t_c of $Si_{1-x}Ge_x$/Ge-on-Si(111) is much lower than that of $Si_{1-x}Ge_x$/Ge(111) for the higher Ge concentrations in SiGe while t_c becomes equivalent for the lower Ge concentrations, origins of which was discussed in terms of dislocation nucleation and surface ridge formation. On the other hand, t_c of $Si_{1-x}Ge_x$/Ge(100) is much higher than that of $Si_{1-x}Ge_x$/Ge(111) and $Si_{1-x}Ge_x$/Ge-on-Si(111) because of different dislocation generation mechanism depending on lattice plane orientations. The critical thickness of strained $Si_{1-x}Ge_x$ with no surface roughness study provides critical design parameters for strained SiGe(111) based devices, such as high-mobility channels and spintronic devices on a Si platform.

However, though electron mobility of strained Ge(111) channel superior compared to other orientations for n-MOSFETs, still now it is a challenging issue to fabricate a high-quality compressively strained Ge(111) channel for enhancing hole mobility for p-MOSFETs. Therefore, compressive strained Ge channel grown on Si(111) substrate was investigated with a comparative sample grown simultaneously on Si(100) substrate. A large compressive strained Ge channels with very low RMS roughness were fabricated on high-quality reverse graded $Si_{1-x}Ge_x$ (111) and $Si_{1-x}Ge_x$ (100) buffer layers. The phosphorous doping was attempted in the SiGe buffer for the purpose of suppression of parallel conduction and very abrupt doping was realized without very little diffusion. This highly compressively strained Ge (111) is expected to open possibilities of high-performance Ge(111) based devices. On the other hand, a high-quality strained Ge surface channel was fabricated on a Si(111) substrate by combining low temperature growth method and reverse graded method. A high-quality Al_2O_3/ strained Ge interface was observed where Al_2O_3 can confine the hole in the channel and as a result, high hole mobility of 1650 cm^2/Vs is obtained at room temperature. The high-quality Al_2O_3/strained Ge interface is a promising template for high-performance surface channel Ge-based devices.

Publications and Presentations

Refereed Publications

1. **Md. Mahfuz Alam,** Youya Wagatsuma, Kazuya Okada, Yusuke Hoshi, Michihiro Yamada, Kohei Hamaya, and Kentarou Sawano, *"Critical thickness of strained $Si_{1-x}Ge_x$ on Ge(111) and Ge-on-Si(111)"* Applied Physics Express (Accepted)

2. **Md. Mahfuz Alam,** Yusuke Hoshi, K. Sawano, *"Structural properties of compressive strained Ge channels fabricated on Si(111) and Si(100)"* Semicond. Sci. Technol. 33, 124008 (2018)

3. Shunya Sakane, Takafumi Ishibe, Tatsuhiko Taniguchi, Nobuyasu Naruse, Yutaka Mera, Takeshi Fujita, **Md. Mahfuz Alam**, Kentarou Sawano, Nobuya Mori, Yoshiaki Nakamura, *"Thermoelectric power factor enhancement based on carrier transport physics in ultimately phonon-controlled Si nanostructures"* Materials Today Energy 13, 56-63 (2019)

Conference Presentations

1. **Md. Mahfuz Alam** and Kentarou Sawano, *"Si/Ge Heterostructures with Various Surface Orientations"* EMN Epitaxy 2019, Amsterdam, Netherlands, June 2019

2. **Md. Mahfuz Alam,** Kazuya Okada, Yuya Wagatsuma, Yusuke Hoshi, Michihiro Yamada, Kohei Hamaya and Kentarou Sawano *"Strain states and critical thickness of $Si_{1-x}Ge_x$ epitaxial layers on Ge-on-Si(111)"* ISTDM / ICSI 2019 Conference, Madison, USA, June 2019

3. **Md. Mahfuz Alam,** K. Sato, Y. Sakamoto, K. Sawada, K. Sawano, *"Structural and electrical properties of compressive strained Ge channels fabricated on Si (111) and Si (100)"* ISTDM / ICSI 2018 Conference, Potsdam, Germany, May 2018

4. Kaoru Okamoto, Ryoji Yanagisawa, **Md. Mahfuz Alam,** Kentarou Sawano, Masashi Kurosawa, Masahiro Nomura, *"Quasi-ballistic heat transport in Si_{1-x} Ge_x nanowires depending on temperature and composition"*,66th Annual Meeting of The Japan Society of Applied Physics, Tokyo Institute of Technology, Tokyo, Japan, March 2019

5. Tatsuhiko Taniguchi, Takashi Ishibe, **Md. Mahfuz Alam,** Kentarou Sawano, Yoshiaki Nakamura *"Further high thermal conductivity of Si-rich SiGe / Si superlattice"*, 66th Annual Meeting of The Japan Society of Applied Physics, Tokyo Institute of Technology, Tokyo, Japan, March 2019

6. Kaoru Okamoto, Ryoji Yanagisawa, **Mr. Mahfuz Alam,** Kentarou Sawano, Masahiro Nomura *"Considerations on Heat Transport in SiGe Nanowires at Low Temperature",*79th Fall Meeting of the Japan Society of Applied Physics, Nagoya International Conference Place, Nagoya, Japan, September 2018

7. Kaoru Okamoto, Ryoji Yanagisawa, **Mr. Mahfuz Alam,** Kentarou Sawano, Masahiro Nomura *"Ballistic Heat Transport in SiGe Nanowires",*65th Annual Meeting of The Japan Society of Applied Physics, Waseda University, Japan, March 2018

8. Shunya Sakane, Watanabe Kentaro, Naruse Nobuyasu, **Md. Mahfuz Alam,** Sawano Kentarou, Mori Shinya, Nakamura Yoshiaki, *"Output Factor Determination Mechanism in Nanostructured Si Thin Film",* 65th Annual Meeting of The Japan Society of Applied Physics, Waseda University, Japan, March 2018

9. Taniguchi Tatsuhiko, Watanabe Kentarou, **Md. Mahfuz Alam,** Sawano Kentarou, Nakamura Yoshiaki, *"Output Factor Manipulation of Si / SiGe Superlattices by Interface Control",* 65th Annual Meeting of The Japan Society of Applied Physics, Waseda University, Japan, March 2018

10. Taniguchi Tatsuhiko, Okuhata Ryo, Watanabe Kentarou, **Md. Mahfuz Alam,** Sawano Kentarou, Fujita Takeshi, Nakamura Yoshiaki, *"Output factor increase of SiGe / Si superlattice by composition control",* 78th Fall Meeting of the Japan Society of Applied Physics, Fukuoka International Conference Place, Fukuoka, Japan, September 2017

11. Shunya Sakane, Watanabe Kentaro, Fujita Takeshi, **Md. Mahfuz Alam,** Sawano Kentarou, Nakamura Yoshiaki, *"Influence of Heat Treatment on Thermoelectric Properties of Nano Dot Containing Si Thin Film",* 78th Fall Meeting of the Japan Society of Applied Physics, Fukuoka International Conference Place, Fukuoka, Japan, September 2017

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List of Contents

1 Introduction

1.1 Introduction to semiconductor industry

Group –IV semiconductor material silicon (Si) has been widely used in the electronics industry as a material of electronic devices because of its abundance on the earth as a resource. The development of the microelectronics was achieved when Julius Edgar Lilienfeld proposed the basic principle of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) early in 1925 and the world of electronics revolutionized when scientists invented the transistor in 1947. After achieving a device quality SiO_2 in the late 1950s, it was realized that development could be made with the research of semiconductor for enhancing the performance of the transistor and leading to the demonstration of the first functional Si MOSFET in 1960.[1] In 1960s, the first epitaxial Si transistor was also demonstrated [2] and significant developments were achieved on the epitaxial growth of group IV materials, which was fundamental concept for realizing high quality heterostructures.

Performance of Si based semiconductor devices can be improved by enhancing the performance of very large scale integrated (VLSI) circuits. Performance improvements in metal-oxide-semiconductor field-effect transistors (MOSFETs) was acquired by reducing device dimensions such as the gate length and gate oxide thickness. As a result, the promoting miniaturization of the gate structure had reached its limit and it was realized that further miniaturization of device structure will increased the probability of leakage current. It has also been observed that improvement of device performance not only depend on miniaturization of device structure but also depend on the enhancement of material properties, which is essential for next generation electronics devices. However, the industrial benefit of scaling is declining as economical limits is approached. In these circumstances, in order to continue higher performance without relying on miniaturization, development of devices incorporating new structures and new materials was attracted interest. Compound semiconductors (group III-IV) such as GaN and GaAs etc. based electronic devices have been developed to overcome this problem. Due to the low cost of conventional Si based devices, research have been done to develop different methods to enhance the performance of Si based devices. On the other hand,

germanium (Ge) and carbon (C) which are also group-IV semiconductor materials are expected to contribute to further improvement of the performance of the devices by fabricating alloy with Si.

In view of the fact that the enhancement of the performance of Si based devices, the first method was the incorporation of Ge as a channel material. Since hole effective mass of Ge is lower than that of Si, this method is effective to enhance the hole mobility of the channel. During the 1980's, SiGe epitaxial films on Si growth technique was developed which enabled various key discoveries about the band alignments in SiGe heterostructures. At the same period, SiGe with full range alloy compositions was successfully grown on Si at AT&T Bell Laboratories by using molecular beam epitaxy (MBE) [3, 4]. People et al. observed a two-dimensional hole gas (2DHG) in modulation-doped strained SiGe films fabricated on Si substrates [5, 6]. In 1992, Welser J.J et al was first demonstrated the operation of n-type strained-Si MOSFET [7] and subsequently p-type strained-Si MOSFET was realized by Nayak D.K et al [8]. It was observed that carrier mobility of the conventional MOSFET can be increased by manufacturing devices using Ge and SiGe as a channel materials that lead to improve the performance of the devices. Since the carrier mobilities for both electron and hole of Ge is higher due to low effective mass than that of Si, and in particularly, high hole mobility than that of compound semiconductors, Ge is attracting attention as a high mobility semiconductor materials with good crystallinity on Si platform. In addition, by using high-quality GeO_2 as a gate insulating film, Ge-MOSFET was fabricated and significant enhancement of carrier mobility was observed compared to Si-MOSFET. Therefore, achieving performance improvement using semiconductor materials, it was realized that Ge and SiGe is important channel materials to enhance the performance of the next generation CMOS devices due to extremely low hole effective mass and subtraction of the alloy scattering. For further improvement of SiGe and Ge channel devices, SiGe-on-insulator (SGOI) and Ge-on-insulator (GOI) were proposed [9-12].

Another important method is so-called "local strain technology" i.e lattice stress is uniformly introduced over the entire film so that it become tensile or compressive strained film depending on the lattice mismatch with underneath layer. The mechanism of this method is band engineering such as strained Ge can significantly enhance the hole mobility due to the low effective mass and the suppression of the interband phonon scattering by the splitting of light-hole and heavy-hole bands [13-15]. In last decades, it has been realized that lattice plane orientation is important issue to enhance the mobility and reported that mobility of Si p-

MOSFETs fabricated on (110) plane orientation is higher than that of Si p-MOSFETs fabricated on (100) plane orientation [16].

Ge and $Si_{1-x}Ge_x$ with high Ge contents epitaxial layers on a Si platform have attracted increasing interest for recent years because of their promising applications in the microelectronics field, such as high mobility channels for complementary metal oxide semiconductors (CMOS) [17-21] and light emitting devices for optoelectronics [22-24]. So far, most researches have been focused on Ge and SiGe with (100) surface orientation. Recently, however, the (111) surface orientation of Ge and SiGe has been attracting renewed attentions since it is not only superior for n-type channel MOS [25, 26] but also highly applicable to spintronic devices owing to the epitaxial growth of high-quality ferromagnetic materials on Ge(111) and SiGe(111) [27-29]. Particularly, pure-spin-current transport was recently reported in a SiGe alloy by using (111)-oriented channel layers [30]. Furthermore, because the spin relaxation mechanism is related to the *L*-valley structures of the conduction band in Ge and SiGe [28,31,32], it is quite important for improvement of the spin lifetime to induce the strain in Ge and SiGe on a Si platform. To realize such various strained SiGe based devices, an issue of the most importance is the crystal growth of high quality strained SiGe layers on Ge(111). Partial strain relaxation involving dislocation generation, which drastically degrades the quality of the strained SiGe layer, should be avoided whereas the sufficiently thick channel layer in devices is needed to effectively confine carriers in the SiGe. In addition, the top most surface of the SiGe can be consumed during device fabrication processing. Therefore, the fully strained SiGe layer as thick as possible is highly demanded. To fabricate and design high performance SiGe heterostructure devices, therefore, one of the most important physical properties that we have to know is critical thickness (t_c), at which partial relaxation of the layer begins via generating dislocations. Although t_c of $Si_{1-x}Ge_x$ on Si(100) has been intensively studied both theoretically and experimentally [33-39], there is no report on t_c of strained SiGe grown on Ge(111). Moreover, for practical device applications, the strained SiGe has to be formed on Si substrates. A Ge-on-Si(111) is useful templates since it has been shown that high quality Ge layers can be grown on Si(111) substrates by means of two-step growth method [40-44]. Whilst such Ge-on-Si enables us to fabricate strained Si/Ge heterostructures on the Si platform, neither t_c nor strain stability of the strained SiGe on Ge-on-Si in comparison with that on a Ge substrate has not been systematically explored. In this study, experimental critical thickness (t_c) of Ge-rich strained $Si_{1-x}Ge_x$ layers on Ge(111), Ge-on-Si(111) and Ge(100). For precise

determination of t_c, an initial stage of the strain relaxation of $Si_{1-x}Ge_x$ layers is systematically investigated in detail in terms of strain states together with surface morphologies.

Till now it is, however, the challenging issue to fabricate high-quality strained Ge(111) on Si platform due to large lattice mismatch between Si and Ge. For achieving high-quality Ge-rich SiGe epitaxial layers on Si(100), graded virtual substrates (GVSs) were fabricated, in which the Ge content linearly varies from zero to the desired final composition [45, 46]. On the other hand, reverse graded relaxed buffer for Ge-rich SiGe virtual substrates were investigated by V.A Shah et al. [47, 48]. These SiGe virtual substrates is not beneficial for practical device application due to their excessive thickness and low thermal conductivity. Therefore, this research focus on the investigation of the development of strain techniques to elucidate the mechanism of the mobility enhancement of the strained Ge(111) channel fabricated on the Si platform. For this purpose, high-quality strained Ge channels were fabricated on Si(111) and Si(100) substrates. A high-quality $Si_{1-x}Ge_x$ buffers for these strained Ge channels were fabricated by combining low temperature growth method and reverse graded method. As a results, a high compressive strained Ge channels with small surface roughness were observed which provide novel methods for further improvement of transport properties of Ge(111) based devices.

1.2 Purpose of this research

The structural and electrical properties of semiconductor devices strongly depend of the lattice plane orientation. The enhancement of mobility of the channel in n-MOSFETs and applicability in spintronics devices, Ge(111) play an important role for enhancing the performance of the semiconductor devices. This thesis is a general investigation of the structural and electrical properties of a high-quality compressive strained Ge(111) channel fabricated on Si platform. The strain states and surface morphology of Ge-rich $Si_{1-x}Ge_x$(111) layers are investigated which are used to fabricate a high-quality strained Ge(111) channel. The reverse graded buffer method and low temperature buffer method are used to fabricate a high-quality relaxed Ge-rich $Si_{1-x}Ge_x$(111) virtual substrate by using MBE. Unlike conventional virtual substrate on (100) lattice plane the fabricated virtual substrate on (111) lattice plane is relaxed under tensile strain and obtained the similar relaxation ratio. For comparative study, a sample is grown on (100) lattice plane simultaneously with the sample grown on (111) lattice plane.

1.3 Chapter summaries

Chapter 2: All theoretical aspects for this research are explained. First, the band structure of strained heterostructure of Si based semiconductor material are described. Then the growth method for the fabrication of relaxed buffer layer are explained. Finally, lattice plane oriented properties are described for Ge with (111) lattice plane orientation compare to other orientations.

Chapter 3: All the experimental techniques used in this research are explained. Molecular beam epitaxy is used for sample fabrication. The Raman spectroscopy and X-ray diffraction are used to determine the composition, the relaxation and strain state observation. For the surface morphology investigation, atomic force microscopy (AFM) and a laser microscopy are used. Lastly, secondary ion mass spectroscopy (SIMS) is used to investigate doped element segregation in the buffer layer and the thickness of the channel layer.

Chapter 4: The strain states of Ge-rich $Si_{1-x}Ge_x$ layer grown on a Si (111) substrate are presented based on XRD profiles. The surface morphology of the Ge-rich $Si_{1-x}Ge_x$(111) layers with wide range of the surface are investigated and reported. The change in strain states and the surface morphology are observed for thermal treatment. Similar investigations are performed for Ge-rich $Si_{1-x}Ge_x$/Ge(100) and Ge-rich $Si_{1-x}Ge_x$/Ge(111) samples. Finally, the critical thickness for strain relaxation and ridge free surface of the Ge-rich $Si_{1-x}Ge_x$ layers are reported.

Chapter 5: The characteristics of a compressive strained Ge(111) channel fabricated on a Si(111) substrate and a comparative sample grown on Si(100) substrate are presented. The strain states and surface roughness of the strained Ge(111) channel is compared with the strained Ge(100) channel. Finally the electrical properties of the strained Ge(111) channel are reported.

Chapter 6: Conclusions of this research.

Chapter 7: References used are listed.

2

Discussion of Si/Ge heterostructure

The fundamental principles of all aspects of Si/Ge heterostructure will be described in this chapter. The physical properties of silicon and germanium with band engineering due to strain induced in the silicon and germanium are described. After that, strained Si, Ge and SiGe are described with the strain relaxation mechanism of SiGe and its growth method.

2.1 Physical properties of silicon and germanium

The physical properties of silicon (Si), germanium (Ge) and silicon-germanium (SiGe) alloys at room temperature which are used for this study are presented as shown in Table 2.1 [49, 50]. In this table, m_t and m_l represent the transverse and longitudinal effective masses of electrons respectively and m_{hh} and m_{lh} represent the effective masses of heavy holes and light holes respectively. Silicon (Si) and Germanium both have a face centered diamond cubic crystal structure. The lattice constant of Ge is 4.17% larger than the lattice constant of Si. The minimum indirect energy gape for both Si and Ge is lower than the minimum direct energy gape. Kasper-corrected-Vergard's law (equation 2.1) can determine the lattice constant of any relaxed Si1-xGex alloy where a_{si} and s_{Ge} are the lattice constant of Si and Ge respectively [51, 52].

$$a_{SiGe} = (1 - x)a_{si} + xa_{Ge} - 0.02733x + 0.02733x^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.1)$$

2.2 Strain effect in semiconductor

The enhancement of carrier mobility contribute the significant enhancement of the transport performance of the semiconductor devices where electrons and holes are used as the complementary carriers in semiconductors. The mobility (μ) is correlated with drift velocity (v) of the carrier and applied electric field (E) by the equation of $\mu = v/E$. Therefore, high carrier mobility material is required to achieve higher drift velocity of the carrier as well as higher performance for low applied electric field. On the other hand, the mobility can be defined by another relation with electronic charge (e), effective mass of carrier (m^*) and mean free time between scattering events (τ): $\mu = e\tau/m^*$. In this relation, it is seen that mobility increase for decreasing effective mass of the carrier. It can be accomplished by introducing

strain in the suitable semiconductor material. In table 2.1, it is observe that Ge has high carrier mobility for both hole and electron compared to Si. Therefore, Ge is an attractive channel material for MOS devices and it has been reported that hole mobility significantly enhanced due to the compressively strained Ge [53]. A lot of research have been done for introducing strain into Si and Ge to realize higher motilities by modulating band structure. Therefore, it is important to understand about band modulation by strain induce in semiconductor materials.

Properties	Ge	$Si_{0.25}Ge_{0.75}$	$Si_{0.5}Ge_{0.5}$	$Si_{0.75}Ge_{0.25}$	Si
Atoms/cm³	4.42×10^{22}	4.415×10^{22}	4.61×10^{22}	4.805×10^{22}	5.0×10^{22}
Crystal Structure	Diamond	Diamond	Diamond	Diamond	Diamond
Lattice Constant (A)	5.6575	5.5960	5.5373	5.4825	5.4310
Minimum Indirect Energy Gap (eV) at 300K	0.66	0.804	0.945	1.05	1.12
Minimum Direct Energy Gap (eV)	0.7	1.6	2.5	3.1	3.4
Intrinsic carrier concentration (cm-3)	2.4×10^{13}	1.8×10^{13}	1.2×10^{13}	0.6×10^{13}	1.45×10^{10}
Melting point (°C)	937	1056.5	1176	1295.5	1415
Effective Mass, m^*/m_0 Electrons Holes	m^*_l= 1.64 m^*_t= 0.082 m^*_{lh}=0.044 m^*_{hh}= 0.28				m^*_l= 0.98 m^*_t= 0.19 m^*_{lh}= 0.16 m^*_{hh}= 0.49
Mobility (drift) (cm2/V-s)	3900 (electron) 1900 (hole)	3300 (electron) 1537.5 (hole)	7700 (electron) 1175 (hole)	2100 (electron) 812.5 (hole)	1500 (electron) 450 (hole)
Linear coefficient of thermal expansion, ΔL/LΔT ($°C^{-1}$)	5.8×10^{-6}	5.0×10^{-6}	4.2×10^{-6}	3.4×10^{-6}	2.6×10^{-6}
Elastic constant ($x10^{10}$) (N/m^2)	C_{11}=12.4 C_{12}=4.13				C_{11}=16.577 C_{12}=6.393

Table 2.1: Physical properties of Si, Ge and SiGe alloys.

The band gap of the SiGe alloy and the band offset of the heterojunction have been theoretically and experimentally investigated, and have been clarified in almost all Ge composition regions [54-57]. Ge composition dependence energy gap of strained and unstrained $Si_{1-x}Ge_x$ alloys are shown in Fig.2.1 [58]. For the unstrained state of SiGe, the band gap linearly decreases with the increase of the Ge composition x, but a kink occurs around x = 0.85. This is because the Ge composition of x <0.85, the bottom of the conduction band exists at the Δ point near X point and the bandgap of $Si_{1-x}Ge_x$ alloys become more like Si, but when x> 0.85, it moves to the L point and becomes like Ge. On the other hand, when SiGe is epitaxially grown on a Si substrate, biaxial compressive strain is induced to SiGe due to the lattice mismatch between Si and SiGe. In this case, the bottom of the conduction band is always present at the Δ point, and the change of the band gap with respect to the the unstrained state as a function of Ge composition. These facts indicate that band engineering can be performed by inducing strain in the SiGe alloy.

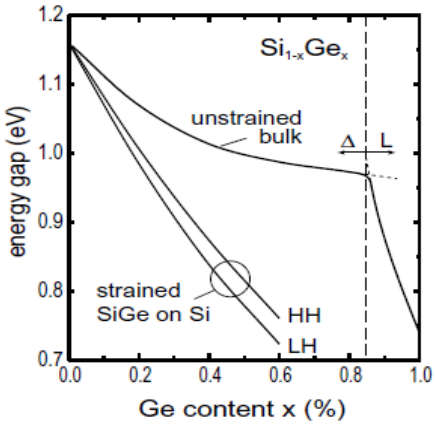

Figure 2.1 Ge composition dependence energy gap of strained and unstrained $Si_{1-x}Ge_x$ alloys. [26]

The valley of the conduction band of the unstrained Si is degenerated sixfold at the Δ point near the X point, and the valley of the conduction band of the unstrained Ge degenerate fourfold at the L point. When Si or Ge is grown on unstrained SiGe, biaxial tensile strain is introduced in Si and compressive strain is introduced in Ge, depending on the lattice parameter difference with SiGe as shown in Fig. 2.2. A constant energy surface of the conduction band for biaxial tensile strained Si as shown in Fig. 2.2 (c). Since the symmetry of the crystal is lost due to the strain, the valley which are degenerated sixfold, is split into two valleys such as Δ_2 valley in the z axis in k space and Δ_4 valley on the x and y axes respectively. The subband energy of Δ_2 valley is lower than the energy of Δ_4 valley, and an energy difference formed between two valleys. The transition of electrons between the Δ_2 and Δ_4 valleys occurs via phonons.

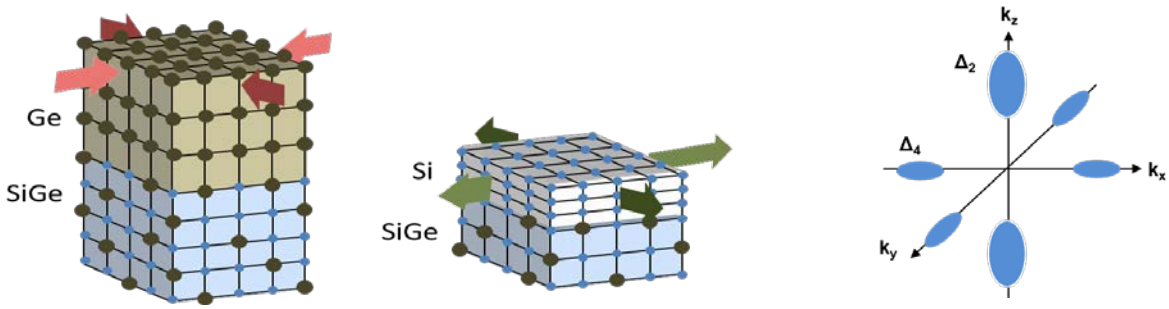

Figure 2. 2: Schematic of (a) compressive strained Ge on relaxed $Si_{1-x}Ge_x$ buffer (b) tensile strained Si on relaxed $Si_{1-x}Ge_x$ buffer and (c) constant energy surface of the conduction band in strained Si.

Phonon scattering is suppressed by reducing the transition probability of electrons between the Δ_2 and Δ_4 valleys. It has been reported that energy difference between the Δ_2 and Δ_4 valleys increases with increase the strain and therefore the transition probability between

valleys decrease. The longitudinal effective mass (m_l) and the transverse effective mass (m_t) for the unstrained Si are 0.92 m_0 and 0.19 m_0, respectively (see Table 2.1). For the Δ_2 valley, only the lateral effective mass contributes in the xy in-plane direction i.e m_c = 0.19 m_0. On the other hand, for the Δ_4 valley, the effective mass of both longitudinal and transvers components contribute, and from 1 / m_c = 1/2 (1 / m_l + 1 / m_t), m_c = 0.315 m0. Therefore, the conduction effective mass is smaller in the Δ2 valley. When biaxial tensile strain is introduced into Si, valley splitting increases the electron occupancy of Δ_2 valley. Although the change of each effective mass m_l and m_t due to the effect of strain is small, an increase of electron mobility can be expected by the reduction of the average effective mass of electrons.

The Ge composition dependence of each band energy in the Ge/relaxed SiGe structure is shown in Fig. 2.3 [59]. The solid line indicates the band energy of Si and Ge, and the dash line indicates the relaxed SiGe band energy. It is clearly observed that the valance band is split due to compressive strain where HH band becomes the top of the valence band. The effective mass of is significantly reduced by compressive strain that contributes to the increase in mobility together with the suppression of interband scattering due to band splitting.

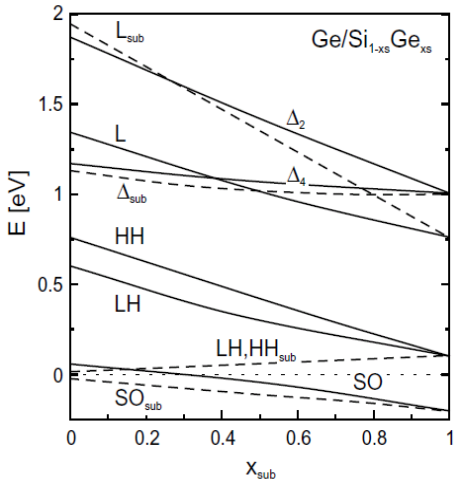

Figure 2. 3: The Ge composition dependence of each band energy in the Ge / relaxed SiGe.[59]

2.3 Strain relaxed SiGe buffer

A high-quality SiGe buffer layer is necessary for the realization of high mobility 2DEGs in strained Si and Ge. In this section, the strain relaxation mechanism of the SiGe layer will be briefly described.

2.3.1 Strain relief mechanism

Due to the lattice constant different between SiGe film and Si substrate, biaxial compressive strain formed in a SiGe at the initial stage of crystal growth. The accumulated strain can be relieved by introducing misfit dislocation at the heterointerface between SiGe film and Si substrate. When the SiGe film thickness exceeds the critical film thickness, elastic strain energy is release by creating misfit dislocation at the SiGe/Si heterointerface leading the formation of relaxed SiGe buffer.

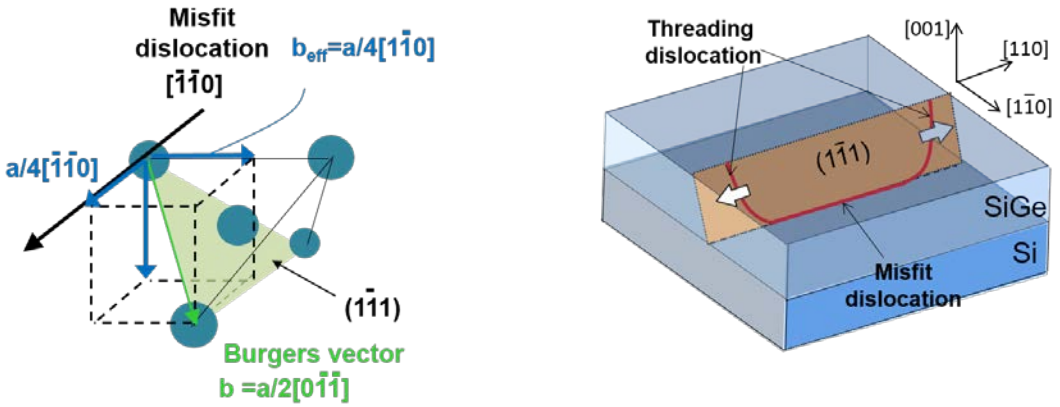

Figure 2.4: (a) The direction of the misfit dislocation and Burgers vector with atomic structure of Si (b) A schematic view of the propagation behavior of dislocations at the SiGe/Si interface. White arrow indicates the sliding direction of the threading dislocation arm.

The direction of the misfit dislocation and Burgers vector with atomic structure of Si are shown in Fig. 2.4. The misfit dislocations are created along $[\bar{1}\bar{1}0]$ direction where the slip plane is in the $(1\bar{1}1)$ plane and b is in the $a/2$ $[0\bar{1}\bar{1}]$ direction. A dislocation cannot end in the interior of a crystal where it either end at a surface or is closed as a dislocation loop. In unstrained states the dislocation follows the <111> directions. 60° dislocation is created between each direction of b and misfit dislocation. Dislocations may easily glide along the {111} slip planes and have two threading dislocation arms on the {111} planes at both ends (FIG. 2). Misfit dislocations are extended by sliding the arms along the direction of the arrow on the {111} plane. Therefore, low misfit dislocation glide velocity is responsible for the high density of threading dislocations in the layer. Since the dislocation glide velocity increases with temperature, it is possible to promote the dislocation glide velocity by increasing growth temperature or performing heat treatment after crystal growth [60].

2.3.2 Relaxed SiGe layer fabrication method

A high-quality relaxed SiGe buffer with significantly low surface roughness and threading dislocation densities play important role for fabrication of the strained Si, SiGe and Ge on the silicon platform. In this section, several relaxed SiGe buffer layer fabrication method will be briefly described.

2.3.2.1 Graded buffer method

A high quality relaxed SiGe buffer was achieved by demonstrating compositional graded buffer method [61, 62]. In this method, the Ge composition is gradually increased to the desired final composition in successive graded layers and a constant Ge composition final layer is grown on the graded layers. The strain relaxed SiGe graded buffer with low defect density depend on two important factors such as minimizing dislocation nucleation rates while simultaneously maximizing dislocation glide velocity. Low dislocation nucleation rates can be accomplished by slowly increasing the Ge content over some thickness of the successive SiGe films. The highest dislocation glide velocities and lowest defect densities are acquired by increasing growth temperature, typically 750˚C or higher for SiGe with $x \leq 0.5$. Once threads are created, subsequent layers can be relaxed by the glide of preexisting threads. Since the strain in the growing film is applied slowly by gradually increasing the Ge content and the dislocation gliding velocity is high for the high growth temperature, a low mismatch defect density can be expected throughout growth [63]. The threading dislocation densities lower than 10^6 cm^{-2} has been reported for relaxed SiGe with x=0 to 0.5 [64]. In practice, dislocation pileup is the initial obstacle to the glide of the threads in the SiGe graded buffer [65]. The dislocation pileup is responsible for creating crosshatch surface roughness in the mismatched epitaxy at high temperature [66]. However, the accumulation of threads in a pileup not sufficient to strain relief. A new dislocation must nucleate for relax successive graded layers resulting the defect density of the final film increases. A low threading dislocation density, lower surface roughness by minimizing dislocation pileup formation was demonstrated by Currie et al. [65] They also reported that intermediate CMP steps can be incorporated into grading process for achieving a high-quality SiGe buffer with small surface roughness. By using compositional graded SiGe buffer, a high quality strained Si and Ge are fabricated for obtaining high carrier mobility. [67, 68].

2.3.2.1 Reverse graded buffer method

Recently, a reverse graded buffer layer has been developed where the Ge composition gradually decrease from highest to the lowest desired Ge composition [69-71]. In this method, first, a high-quality Ge epilayer is fabricated by two temperature growth method where a thin Ge seed layer is grown on Si substrate at low temperature after that a thick Ge layer is grown at relatively high temperature. Next, successive compositional reverse graded SiGe films are grown on Ge epilayer and finally a thick constant composition SiGe layer is grown on graded layer. The misfit dislocations are generated in the reverse graded layer, which are needed to relax the constant composition layer. These misfit dislocations are confined into the reverse graded layer as like as the linear forward graded structure as shown in Fig. 2.5 [70]. The crosshatch pattern is formed in the graded layer due to strained field created by misfit dislocation and propagating along orthogonal directions during growth of the graded layer [72]. V. A. shah et al. demonstrated a high-quality reverse grade SiGe buffer on Si(100) substrate with high Ge content where a high degree of relaxation with low TDD of $4x10^6$ cm^{-2} are obtained compared to forwarded graded structure with TDD of 10^6-10^8 cm^{-2} and also reported that the surface roughness is remarkably lower than the forward grading structure [70].

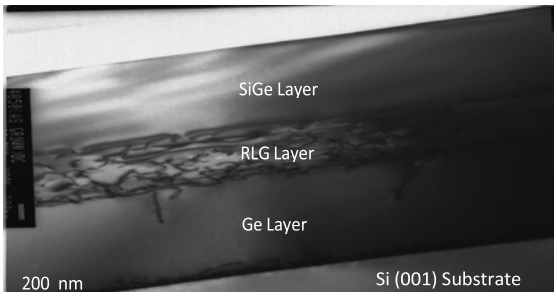

Figure 2.5: A cross-sectional TEM image in the 220-diffraction condition. Shown are dislocations confined to the RLG region but not penetrating upwards.[39]

2.3.2.3 Low temperature buffer method

The low-temperature buffer method has been demonstrated as a method for fabricating a high quality relaxed SiGe buffer layer with low surface roughness and is thinner film compared to the compositional graded buffer [73, 74]. In this method, first, a thin Si buffer layer is fabricated on a Si substrate at low temperature of less than 400°C and then a thick SiGe layer is grown on Si buffer at relatively high temperature. The point defects are created in LT-Si layer acts as a dislocation source, which is, contribute to promote the relaxation of the next fabricated SiGe layer. The dislocations are confined in the LT-Si layer due to point defects. In addition, LT-Si layer become tensile strained which reduce the lattice mismatch between SiGe

layer and Si buffer layer [75] leading the relaxation of the SiGe layer by suppressing the dislocation nucleation. By using this method, it is possible to fabricate a high-quality relaxed SiGe buffer with high Ge content whereas the graded layer thickness significantly increased for fabricating the relaxed forward graded SiGe buffer layer with high Ge content. However, the surface roughness increases with the increase of the Ge composition, and in the case of 90% Ge composition, the roughness becomes more than 5 nm [76]. Since it is necessary to form a low temperature layer, the greatest drawback of this method is that the low temperature layer is difficult to grow by gas source MBE or CVD methods.

For this research both reverse graded buffer method and low temperature buffer method are used to fabricated a high-quality relaxed Ge-rich SiGe buffer layer on (111) lattice plane orientation by using MBE.

2.4 Importance of Ge with (111) plane orientation

Ge with a lattice orientation of (111) is attractive due to its two times higher electron mobility for n-type channel MOS applications compared to the (100) orientation [25]. This high electron mobility observed due to (111) surface orientation relies upon two factors: first, lower the density of interface traps (D_{it}) for the (111) lattice plane orientation in the upper half of the bandgap than the (100) lattice plane orientation and second, higher transport properties for the (111) orientation reported by simulation [77]. In addition, Ge n-channel MOSFETs fabricated on (111) lattice pale provides enhanced electron mobility due to largest quantization mass and smallest conductivity mass in the L valley. For the (111) orientation, strong inversion and most of the electrons occupy in the central L valleys leads to the highest electron mobility because of the smallest conductivity effective mass. Y. –J. Yang et al. reported that unstrained mobility to be significantly dependent on substrate orientation Ge (111) > Ge (110) > Ge (001) [69]. Usually, the mobility of the uniaxial strained channel depend on the channel direction. For uniaxial tensile strain, the highest mobility was obtained in the channel direction at [$\bar{1}$10], [$\bar{1}$10] and [110] with Ge(111), Ge(110) and Ge(001) lattice plane orientation respectively. The achievement of the enhance electron mobility mainly for electrons repopulate from large conductivity mass valleys to small conductivity mass valleys resulting the reduction of average conductivity of mass. However, biaxial strain is independent of the stress direction. The mobility as a function of strain for uniaxial and biaxial strain is shown in Fig 2.6. It is observe that the mobility is highest for (111) lattice plane orientation either uniaxial or biaxial tensile strain.

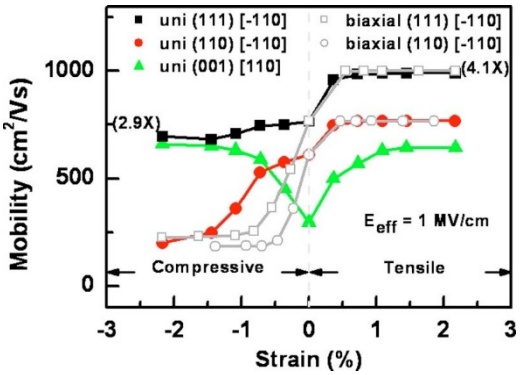

Figure 2.6: (Color online) Mobility as a function of strain under different stress conditions, channel directions with notation of [ ], and substrate orientations with notation of ( ). [17]

On the other hand, Ge with a surface orientation of (111) is also attractive due to applicability to spintronic devices via lattice-matched epitaxial growth of high-quality ferromagnetic materials. The contact resistance at the metal/Ge interface reduction by reducing Schottky barrier height (SBH) at the interface is the challenging issue. It has been reported that the SBH at the germanide/Ge interface is significantly dependent on the Ge surface orientation, and the ohmic characteristics was observed at germanide/n-Ge(111) junction as shown in Fig. 2.7[78].

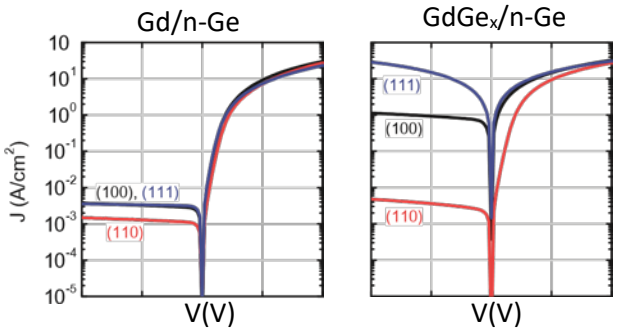

Figure 2.7: Typical I–V characteristics of (a) Gd/n-Ge and (b) $GdGe_x$/n-Ge junctions fabricated on Ge(100), (110), and (111) substrates. The I–V characteristics of $GdGe_x$/Ge are significantly dependent on surface orientation, and ohmic characteristics are observed at the $GdGe_x$/n-Ge(111) junction.[48]

In addition, a reduced surface roughness of Ge(111) fin LEDs wae fabricated by a combination of anisotropic wet etching and Ge-condensation techniques because the etching rate strongly depends on crystal orientation. The PL and EL spectra has been reported for tensile-strained Ge(111) fins which indicates direct band-gap recombination and optical interference [79]. By considering the advantage of Ge with (111) lattice plane orientation over (110) and (100) orientations this research is focused on the high quality strained Ge (111) fabrication and characterization.

3

Experimental techniques

In this chapter, the operating principles of the experimental techniques used in this thesis are illustrated with fundamental theory of each technique. First, solid source molecular beam epitaxy (SSMBE) technique is described which is used for all samples preparation and then structural characterization techniques are described. Finally, electrical conductivity measurement systems and other evaluation methods are described successively.

3.1 Molecular beam epitaxy (MBE)

The MBE method allow the epitaxial growth of very thin crystalline layer with well-defined dopants at low growth temperature. There are two types of MBE systems depending on source condition such as solid source molecular beam epitaxy (SSMBE) and gas source molecular beam epitaxy (GSMBE). The descriptions given below is for SSMBE, which is used for this study.

3.1.1 Basic principle and requirements of SSMBE

In epitaxial growth process, growing layer follows the orientation of the substrate and a single crystalline film grow on a substrate. For avoiding polycrystalline or amorphous growth by disordering lattice orientation, a clean substrate is necessary for epitaxy. The generated molecular beams of matrix material such as silicon or germanium and doping species interact with the substrate surface without colliding with impurity atoms in the vacuum chamber to form a single crystal deposit under an ultra-high vacuum (UHV) condition is the basic concept of SSMBE. The molecular fluxes of elemental constituents are evaporated in special electron beam evaporators (EBEs) or in radiative heated effusion cells and the flux of the deposition materials are measured directly by a flux monitor. The purity of constituent fluxes and ultra-high vacuum conditions are important for the MBE because semiconductor properties are sensitive to impurities. Therefore, the essential features of the MBE system are

1. Ultra-high vacuum (UHV) condition during growth
2. Pure source of molecular beams

3. Clean substrate
4. Precisely monitoring deposition rate

3.1.2 UHV chambers

MBE needs at least to chambers, a growth chamber and a preparation chamber. Figure 3.1 shows a schematic diagram of the SSMBE system (VG Semicon V80M) used for this research. It consists of two independently pumped UHV chambers connected with a UHV gate valve. At the left side, there is the entry lock with the wafer-transfer mechanism. The entry lock is pumped rapidly with a cry-pump so that its pressure reached in the range of 10^{-8} mbar within 90 min. The preparation chamber has a parking stage and a high temperature heating stage (HTHS) and maintain UHV condition by ion-pump. The growth chamber accommodates all the installations necessary for MBE growth such as substrate holder, substrate heater and substrate rotator; evaporation sources for matrix materials and dopants; and evaporation rate monitor system. The growth chamber is always under UHV pumping by turbo-molecular pump. Under growth conditions, cooling water pipes welded to the chamber walls effectively reduce outgassing.

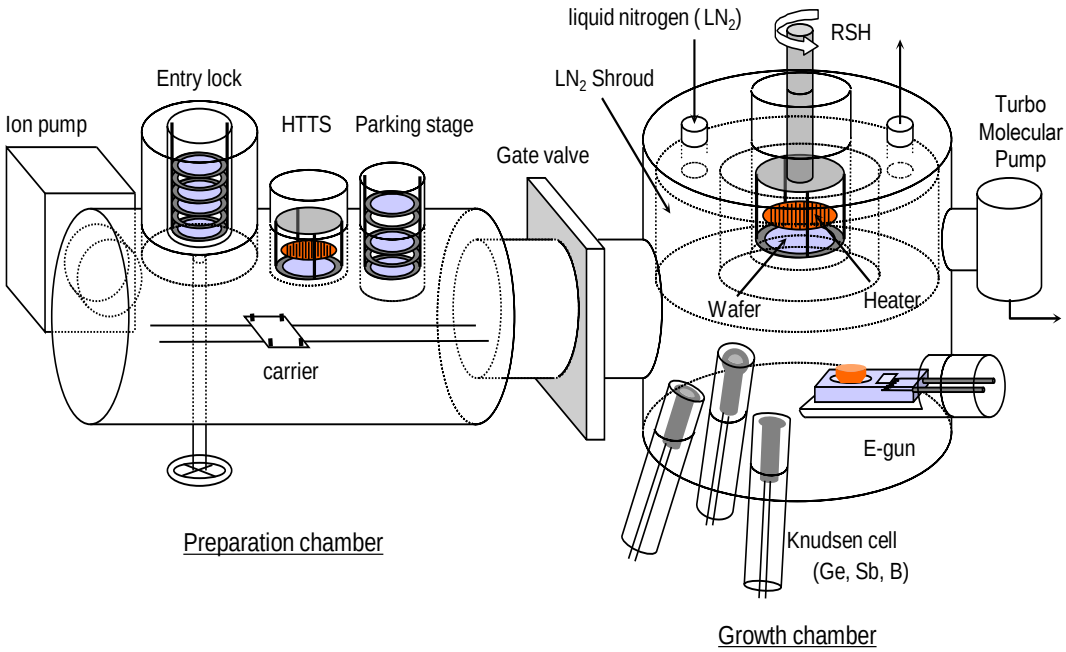

Figure 3.1: Schematic illustration of a typical solid source molecular beam epitaxy (SSMBE)

3.1.3 Source of molecular beams

Si cell temperatures around 1700°C are necessary for Si growth rates of the order of nanometers per second. These rates are generated by evaporation from Si-source distance of about 30 cm from the substrate. At such temperature, molten Si is very reactive and it would cause excessive contamination from the crucible material. To overcome such type of problems, Si is heated by electron beam. Figure 3.2 shows a schematic diagram of the major component of a Si electron beam evaporator (EBE). Tungsten filament emits electrons and these are accelerated in an electric field with 7KeV energies. To avoid contamination produced by tungsten filament, the emitted electrons are deflected by magneto static field to an angle 270°. The high energy electron impinge on a single crystal, high purity Si ingot, which is placed in a water-cooled Cu-crucible. Due to the thermal properties of Si, molecular beam is created by electron beam.

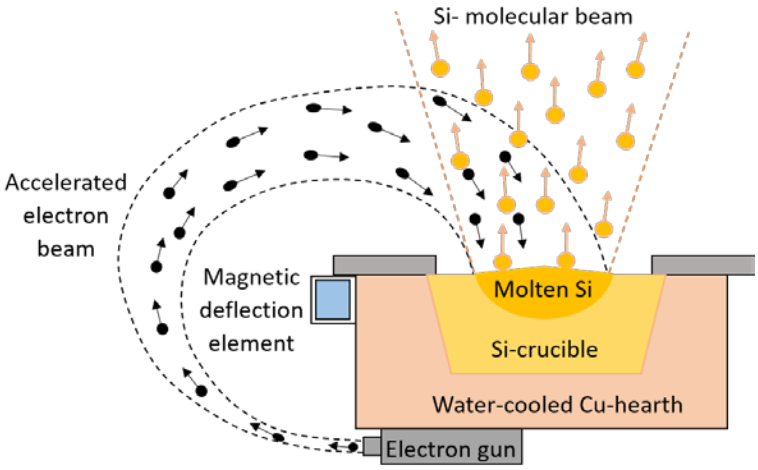

Figure 3.2: Schematic diagram of the major component of a Si electron beam evaporator.

A single effusion cell is used for the evaporation of Ge. The particular properties of this cell is the co-evaporation of Ge and carbon with a flux ration of roughly 1000, because Ge is melted in a graphite crucible with large area opening which is specially designed to withstand the strong tensile forces exerted by the increase of Ge volume during solidification. The electrical current heater surrounds the crucible; the outward heat flux is shielded by a graphite cage, tantalum and Si-shields and a cold wall. A thermocouple is mounted near the bottom of the crucible as shown in fig. 3.3.

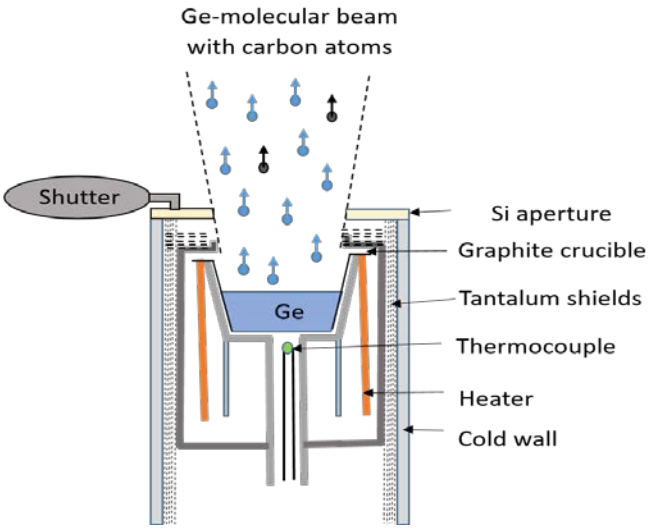

Figure 3.3: Schematic diagram of the major components of an effusion cell for Ge evaporator.

In MBE system, several doping techniques are used for p-type and n-type doping over a wide range of concentration. Boron is commonly used for p-type doping as it has large equilibrium solid solubility and a very low surface segregation. In modern MBE system, boron is evaporated using a high-temperature source with special graphite crucible. N-type doping during MBE growth is problematic because of low sticking coefficients and surface segregation. Usually antimony (Sb) and phosphorous (P) are used for n-type doping. For this research work, phosphorous is used for n-type doping layer fabrication by using GaP dopant source.

3.1.4 Substrate cleaning and heating

High-quality epitaxial growth needs substrate surface with low contamination levels before MBE growth. For this research, cleaning the Si substrate or SiGe where Ge composition is less than 70% , first step of H_2SO_4 + H_2O_2 solution is used for 5minutes and then rinsed with deionized water for 3 minutes and finally immersed into HF solution for one minute and this cycle was performed for twice. On the other hand, for Ge substrate or SiGe where Ge composition is greater than 70%, a solution of NH_4OH + H_2O is used for 5 minutes and then rinsed with deionized water for 3 minutes and finally immersed into HF solution for one minutes and this cycle was performed for twice. After HF treatment, the substrate surface is well hydrogen-terminated and immediately loaded into the MBE chamber. A clean surface is obtained by desorbing hydrogen by in situ heat treatment at 700 to 800 °C before epitaxial growth.

3.2 Ion implantation technique

Ion implantation systems are widely used industrially as a technique of impurity doping in semiconductor devices. Figure 3.4 shows a schematic diagram of the ion implantation system (ULVAC IM-200M-RD) used in this study. The ion implantation system consist of three main parts: ion source (IS), beamline (BL) and end station (ES). IS evacuated by oil diffusion pump, and the other main parts BL and ES are evacuated by a cryopump. The steady-state pressure of IS is approximately 1×10^{-6} Torr. The injected gas into the IS is ionized by the thermionic electrons emitted from the tungsten filament and extracted by the 25 keV voltage. The pressure of the IS is 1 to 5×10^{-5} Torr during ionization. The extracted ions are passed through mass spectroscope system for the specific ion species and then enter the accelerating tube. The ion beam is then accelerated to 25-100 keV, scanned longitudinally and laterally by a quadrupole lens, and then injected into the sample placed at ES. The injection beam current is set to 5 to 30 μA to suppress the heating of the substrate.

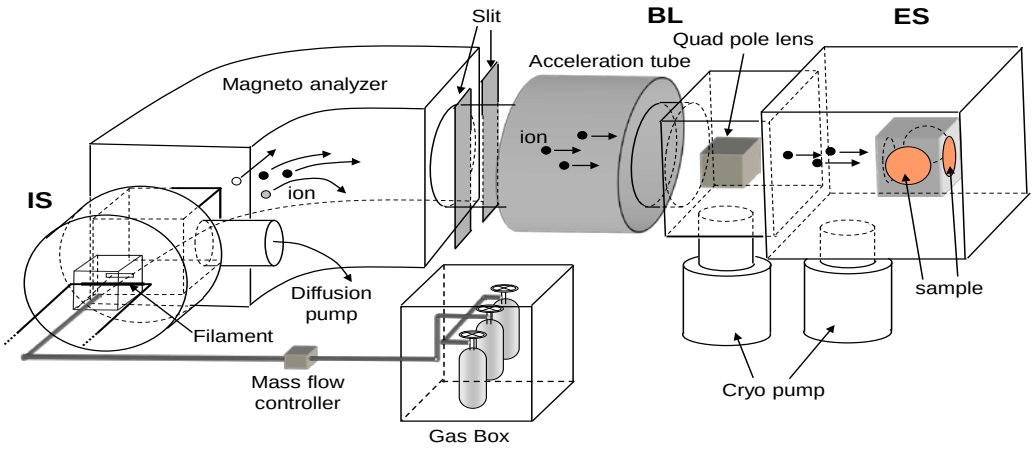

Figure 3.4: Schematic diagram of the major components of Ion implantation

3.3 X-ray diffraction

The X-ray diffraction (XRD) is widely used in order to determine crystal structure and states of strain. In particular, the XRD rocking curve (RC) is a useful technique to analyze composition and layer thickness of crystal film and two-dimensional reciprocal space mapping (RSM) is used for analysis of semiconductor heterostructures including composition and strain analysis by determining in-plane and out-plane lattice constant. In this study, a Philips X-Pert

MRD was used for X-ray diffraction measurement. Cu is used as the target of the X-ray source which was operated at 45KeV and 40mA to produce CuKα_1 radiation (wavelength 1.5406 Å) This x-ray beam was then passed through 4 bounce asymmetric Ge(220) crystal monochromator and then incident of the sample. The sample stage is moveable in four axes of freedom such as ω and 2θ depended to the beam adjustment to the sample so that highest possible diffraction count is detected. The other two rotation axes are phi (φ) and psi (ψ) as shown in figure 3.4. The count per second (cps) of diffracted X-ray was recorded by an analyzer with asymmetric Ge (220) crystals can be inserted in front of the detector to increase resolution.

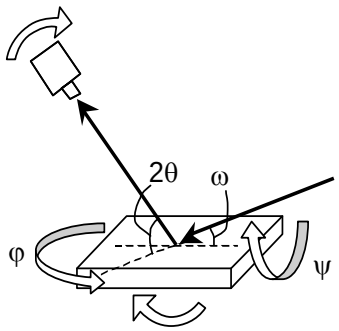

Fig. 3.4 X-ray diffraction measurement system.

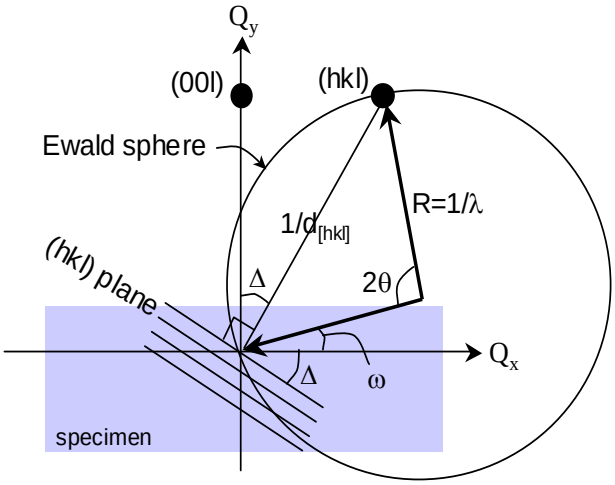

Fig. 3.5 Reciprocal lattice space in X-ray diffraction measurement

RSM is generated by converting angles to coordinates in the reciprocal lattice space. The principle of the conversion is described in the following. Figure 3.5 shows the reciprocal lattice space in X-ray diffraction measurement. In this case ω and 2θ satisfy the Bragg law (n = 0) of (hkl) reciprocal lattice point

$$2R\sin\theta = 1/d_{[hkl]}$$

Here, the radius of the Ewald sphere $R = {}^{1}/_{\lambda}$ (λ denotes the wavelength of the X-ray) and $d_{[hkl]}$ is the spacing of the (hkl) plane. The angle θ represents the following equations

$$\theta = \omega + \Delta\,;\ \cos\Delta = \frac{l}{\sqrt{h^2 + k^2 + l^2}}$$

Here, Δ is the angle between [001] reciprocal vector and [hkl] reciprocal vector.

The plane of the incident and diffracted X-ray (Q_x- Q_y plane) is referred to as the scattering plane and the wave vector difference $\vec{Q} = \vec{K} - \overrightarrow{K_0}$ is called the scattering vector. It is straightforward to derive the coordinates of the end point of the scattering vector in this space:

$$Q_x = 1/d_{[hk0]} = R\ \{\cos\omega - \cos(2\theta - \omega)\}$$

$$Q_y = 1/d_{[00l]} = R\ \{\sin\omega + \sin(2\theta - \omega)\}$$

Here, d [hk0] is the spacing of the (hk0) plane, and d [00l] is the spacing of the (001) plane. By converting angles ω and 2θ to coordinates in the reciprocal lattice space and using these relationships, a reciprocal lattice space-mapping image can be obtained. In addition, a rocking curve is obtained by keeping the angle ω at constant and ω/2θ is scanned around a specified reflection. In this research, the crystal structure of the pseudomorphic and relaxed SiGe layers were characterized by using these two methods.

3.4 Strain and relaxation evaluation method

The strain is introduced in the fabricated layer due to the lattice mismatch between the epitaxial layer and substrate. The in-plane strain ($\varepsilon_{//}$) is created along parallel direction to the layer plane and the out-plane strain ($\varepsilon_{\perp}$) is created along vertical direction to the layer plane. These strains can be defined by the following equations.

$$\mathcal{E}_{\perp} = \frac{a_{\perp} - a}{a}$$

$$\mathcal{E}_{//} = \frac{a_{//} - a}{a}$$

Here, $a_{//}$, $a_{\perp}$ and a are the in-plane lattice constant of the epitaxial layer, out-plane lattice constant of the layer and lattice constant of the substrate respectively. The induced strain in the SiGe layer is evaluated by using the elastic constants c_{11} and c_{12}:

$$\mathcal{E}_{\perp} = -\frac{c_{12}}{c_{11}}(\mathcal{E}_{//x} + \mathcal{E}_{//y})$$

Where $\mathcal{E}_{//x}$ and $\mathcal{E}_{//y}$ are the in-plane strain along the direction of x-axis and y-axis respectively. Therefore, using above equation we get

$$a_{\perp} = a_{SiGe}\{1 - \frac{c_{12}}{c_{11}}\left(\frac{a_{//x} + a_{//y} - 2a_{SiGe}}{a_{SiGe}}\right)\}$$

Here, a_{SiGe} represents the lattice constant of completely relaxed SiGe layer. $a_{//x}$ and $a_{//y}$ are in-plane lattice constants of the strained SiGe in the x-direction and y-direction respectively. If the SiGe layer experienced biaxial strain, we get $a_{//x} = a_{//y}$.

The elastic constant of the SiGe layer can be calculated by using elastic constants of Si and Ge which are presented in table 2.1.

$$c_{ij}^{SiGe} = \frac{(1-x)a_{Si}c_{ij}^{Si} + xa_{Ge}c_{ij}^{Ge}}{a_{SiGe}}$$

In addition, the relaxation ratios R_x and R_y of the SiGe layer grown on the Si substrate in the x and y directions are:

$$R_x(\%) = \frac{a_{//x} - a_{Si}}{a_{SiGe} - a_{Si}} \times 100$$

$$R_y(\%) = \frac{a_{//y} - a_{Si}}{a_{SiGe} - a_{Si}} \times 100$$

In general, the relaxation ratio of a layer:

$$R = \frac{a_{substrate} - a_{layer}}{a_{substrate} - a_{layer\,(bulk)}} \times 100\%$$

3.5 Raman spectroscopy

Raman spectroscopy is a spectroscopic technique where the frequency of photons in incident monochromatic light changes after interaction with a sample i.e inelastic scattering of monochromatic light is the basic principle of the Ramman spectroscopy. Laser is widely used as a source of monochromatic light. When photons of the laser light are absorbed by the sample, frequency of the reemitted photons is shifted up or down compared to the incident photons frequency, which is called the Raman effect. This shift provides information about vibrational, rotational and other low frequency transitions in molecules.

The laser beam can be considered as an oscillating electromagnetic wave with electrical vector E. When the laser light interact with the sample, it induces electric dipole moment P = αE which deforms molecules. The molecules start vibrating with characteristic frequency υ_m due to periodical deformation of the molecules. In addition, incident monochromatic laser light

with frequency υ_0 excites molecules and transforms the molecules into oscillating dipoles that emit light with three different frequencies when:

(a) A molecule with no Raman-active modes absorbs the incident photon with the frequency υ_0, the excited molecule with no Raman-active modes returns back to the same basic vibrational state and emits photon with the same frequency as an incident photon frequency. This type of interaction is known as elastic Rayleigh scattering.

(b) A molecule with Raman-active modes absorbs the incident photon with the frequency υ_0, which is in the basic vibrational state. A part of the photon's energy is transferred to the Raman-active mode with frequency υ_m and the resulting frequency of scattered light is reduced to $\upsilon_0 - \upsilon_m$. This Raman frequency is called "Stokes".

(c) A molecule with Raman-active modes absorbs the incident photon with the frequency υ_0, which is already in the excited vibrational state. Excessive energy of excited Raman-active mode is released, molecule returns to the basic vibrational state resulting the frequency of scattered light increase to $\upsilon_0 + \upsilon_m$. This Raman frequency is called "Anti-Stokes".

It can be noted that, about 99.999% of all incident photons in spontaneous Raman undergo elastic Rayleigh scattering. This type of signal is useless for practical purposes of molecular characterization. Only about 0.001% of the incident light produces inelastic Raman signal with frequencies $\upsilon_0 \pm \upsilon_m$. Spontaneous Raman scattering is very weak and special measures should be taken to distinguish it from the predominant Rayleigh scattering. Instruments such as notch filters, tunable filters, laser stop apertures, double and triple spectrometric systems are used to reduce Rayleigh scattering and obtain high-quality Raman spectra.

The space microscopic Raman spectrometer (JOBIN YVON / HORIBA T64000) is used for this research. An Ar laser (wavelength: 514.5 nm) are used as an excitation light where the laser intensity is 5 to 20 mW. The sample is placed in a back scattering arrangement, and the excitation laser light is focused and irradiated to about 1 μm by an objective lens. A very weak spontaneous Raman scattering is distinguished from the predominant Rayleigh scattering by using a notch filter, dispersed by a spherical mirror and a diffraction grating, and finally detected by a CCD.

The phonon modes of Si are degenerate in threefold and split into singlet and doublet by applying stress. When the sample is placed in the backscattering configuration as in the

apparatus used in this research, the Raman spectrum can be observed only in singlet, so the optical phonon energy ω is defined by [79]

$$\omega = \omega_0 + \frac{1}{\omega_0}\left(q - \frac{c_{12}}{c_{11}}p\right)\varepsilon_{//} = \omega_0 + b\varepsilon_{//}$$

Here, ω_0 is the phonon energy in an unstrained state, p and q are constants, and b is a strain shift coefficient. From the Raman spectrum of SiGe, three optical phonon modes Si-Si, Si-Ge, and Ge-Ge are observed. The phonon energy ω_0 in the unstrained state of SiGe depends on the Ge composition x, and strain state of SiGe. The magnitude of strain shift coefficient b and the phonon energy ω_0 have been reported.[80-83].

The Si-Si phonon mode is investigated by Nakashima et al. [83], and Si-Ge mode and Ge-Ge modes are investigated by Tsang et al. [82]. Below, the formula of the phonon energy in each mode is shown.

$\omega_{Si-Si} = 521 - 61.7x - 732\varepsilon_{//}$

$\omega_{Si-Ge} = 400.5 - 14.2x - 575\varepsilon_{//}$

$\omega_{Ge-Ge} = 282.5 - 16x - 385\varepsilon_{//}$

Here, $\omega_{\text{Si-Si}}$, $\omega_{\text{Si-Ge}}$, and $\omega_{\text{Ge-Ge}}$ represents the phonon energy of Si-Si, Si-Ge, and Ge-Ge, phonon modes respectively.

3.6 Atomic Force Microscopy (AFM)

In this study, a Digital Instruments NanoscopeIIIa tapping-mode AFM was used where the results are analyzed by using NanoScope software to investigate the surface morphology of the sample. This experiment allows quantification of the surface roughness by using root mean square (RMS) roughness with height range. The operation of a tapping-mode AFM is described below.

Principle of tapping-mode AFM

The tapping-mode AFM scans the sample surface by intermittently touching or tapping on the sample with a very tiny and sharp tip fixed at flexible cantilever. The cantilever is

mounted to a piezoelectric actuator. During oscillation, the tip goes through both the attractive and the repulsive regions of the tip–sample force field. The laser beam incident on the end of cantilever and reflected laser beam received by a position sensitive photo detector to provide cantilever deflection feedback. During the scan of the tip over the sample surface with feedback mechanisms, PZT scanners enable to maintain the tip at a constant force or a constant height. Therefore, the tip is moved up and down with the contour of the surface and the laser beam deflected from the cantilever provides measurements of the difference in light intensities between the upper and lower photo detectors. The frequency of oscillation is fixed near the resonance of the tip and the oscillation amplitude is monitored. Starting from free oscillation amplitude, the sample is approached to the tip until its amplitude is reduced to the set point value, which is selected to reduce damage to the sample. The variations of the z-position of the tip during scanning are plotted as a function of the xy position of the tip to create the height image, in which color contrast is used to show the z-variations.

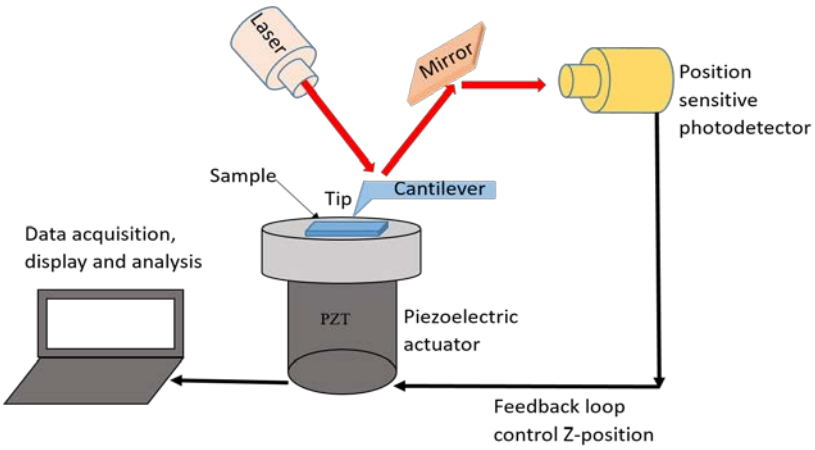

Figure 3.7: Schematic diagram of the major components of tapping-mode AFM.

3.7 Hall measurement system

Hall measurement system is used to measure the drive carrier sheet density and carrier mobility at the temperature range of 3K to room temperature by using cryostat. For this hall measurement, hall bar was fabricated by using photolithography system and AuGa (Ga 1%) was deposited on hall bar for the formation of metal contact by using metal deposition system as shown in figure 3.8. A current (I_{AB}) is applied between the electrodes A and B and voltage

drop (V_{CD}) is measured between C and D. The hall voltage (V_{DE}) was found when a magnetic field is applied in perpendicularly to the conductive surface. Using these values, the sheet carrier density (p_H) and the hall hole mobility (μ_H) are evaluated by the following equations.

$$\rho_H = \frac{BI_{AB}}{eV_{DE}}$$

$$\mu_H = \frac{V_{DE}}{BV_{CD}}\frac{L}{W}$$

Here, e is an electron charge, and W and L are the channel width and length of the hall bar, which are 200 μm and 400 μm, respectively. In addition, the magnitude of the applied magnetic field was 0.4 T, and 1 to 10μA was used for the constant current (I_{AB}) flow.

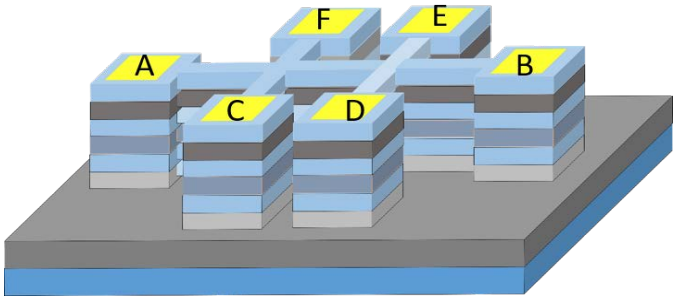

Figure 3.8: Schematic diagram of a hall bar.

4

Strain states of Ge-rich $Si_{1-x}Ge_x$ layer and its thermal stability

4.1 Introduction

$Si_{1-x}Ge_x$ epitaxial layers on Si platform with high Ge contents have attracted massive interest for last few decades because of their several applications in the microelectronics industry. Strained $Si_{1-x}Ge_x$ is an attractive channel material for enhancing the hole mobility of the channel [80, 81] and also attractive in optoelectronics due to their high potential for efficient light emission via direct band transition [21, 22]. SiGe with an orientation of (111) is also attractive for n-type channel MOS applications [25] and applicability to spintronic devices via lattice matched epitaxial growth of high-quality ferromagnetic materials [27, 28]. Additionally, a high-quality Ge-rich $Si_{1-x}Ge_x$ buffer layer as well as virtual substrate on a Si platform play an important role for the formation of a high-quality strained Ge channel in conventional CMOS processes [82, 83]. Due to the 4.2% lattice mismatch between Si and Ge, still now it is a challenging issue to grow high-quality Ge-rich $Si_{1-x}Ge_x$ layers on the Si platform. Moreover, it has been shown that high-quality Ge epilayer can be formed on the Si substrate by two-step growth method [41-44]. Whilst such Ge-on-Si enables us to fabricate strained Si/Ge heterostructures on Si platform, the strain stability on Ge-on-Si in comparison with that on a Ge substrate has not been systematically studied. However, critical thickness for plastic relaxation of $Si_{1-x}Ge_x$ on Si(100) was studied both theoretically and experimentally by several researchers [33-39] and showed that for the lower growth temperature, higher the experimental critical thickness due to the dislocation formation in the layer.

A high-quality $Si_{1-x}Ge_x$ layer with smooth surface play crucial roles for enhancing the performance either it is used as a channel layer or a buffer layer in the conventional CMOS processes. Due to the importance of (111) lattice plane orientation, results are presented in this chapter by successfully characterization of $Si_{1-x}Ge_x$ layers fabricated on (111) lattice plane for explaining strain states and other structural parameters. All the samples, characterized in this chapter are fabricated at low temperature. Since the growth temperature is strongly influences all adatom process, the surface roughness, the crystallinity and the relaxation processes in

heterostructure. The thermal stability of strain states and other parameters of $Si_{1-x}Ge_x$ after post annealing condition are also presented in the chapter. In this study, we experimentally determine critical thickness (t_c) of Ge-rich strained $Si_{1-x}Ge_x$ layers on Ge(111), Ge-on-Si(111) and Ge(100) substrates. For precise determination of t_c, an initial stage of the strain relaxation of $Si_{1-x}Ge_x$ layers is systematically investigated in detail in terms of strain states together with surface morphologies. As a result, we find that t_c for strained $Si_{1-x}Ge_x$ with $x > 0.75$ on the epitaxial Ge-on-Si is much lower than that on the Ge substrate while t_c for strained $Si_{1-x}Ge_x$ with $x < 0.75$ does not show obvious difference between the two Ge substrates. This tendency can be explained by nucleation of dislocations and resultant initial strain relaxation occurring locally in surface ridged areas. To the author's knowledge, the critical thickness of $Si_{1-x}Ge_x$ layers on (111) lattice plane have not been studied elsewhere.

4.2 Base layer for Ge-rich $Si_{1-x}Ge_x$ on Ge-on-Si(111)

To reduce the large lattice mismatch between Si substrate and Ge-rich $Si_{1-x}Ge_x$ layer, a high quality Ge layer as a base layer is necessary prior to the epitaxial $Si_{1-x}Ge_x$ layer grown on a Si substrate. The development of a high quality Ge layer directly grown on a Si substrate with (111) plane orientation using two-step growth method have already been reported. In this section, two-step growth method for base layer fabrication and its structural properties are presented.

4.2.1 Base layer structure and growth parameters

The growth parameters for fabricating Ge layer directly on the Si substrate is different for MBR and CVD growth systems, where MBR system is used for this research. Figure 4.1 shows the Ge epilayer that was used as the base underlying Ge layer for the Ge–rich $Si_{1-x}Ge_x$ layers grown on the Si(111) substrate. The purpose of the low temperature (LT) Ge layer deposited directly on wafer is to reduce the lattice mismatch by generating dislocations so that relaxed thin Ge epitaxial layer is formed. K. Sawano et al.[10] reported that the optimized growth temperature and thickness for LT layer are 400°C and 40 nm respectively based on RMS roughness and FWHM of Ge(333) peak. On the other hand, relatively high temperature (HT) thicker Ge layer reduce threading dislocation to reach the surface of buffer. For a high-quality Go-on-Si(111), a 40 nm thick LT-Ge layer was grown at 400°C and followed by the growth of a 650nm thick HT-Ge layer was grown at 700°C and then annealed at 800°C for 10 min in same vacuum condition in order to reduce the threading dislocation density in the Ge epilayer.

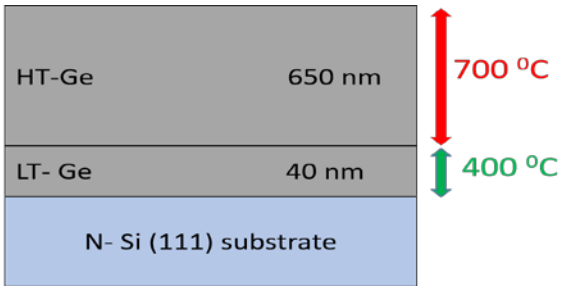

Figure 4.1: Structure of the base Ge layer on a Si(111) substrate for fabricating SiGe layers on it.

4.2.2 Structural characterization of the base Ge layer

The base Ge layer is characterized by using XRD reciprocal space mapping (RSM) and Raman spectroscopy. The XRD RSM was performed to investigate relaxation ratio of Ge epilayer. Figure 4.2 shows a RSM image around the asymmetrical (153) reciprocal space point for Ge epilayer. It is clearly seen that Ge (153) peak is slightly deviated from relaxation line with respect to Si(153) peak. The relaxation ratio of the Ge layer was calculated compare to Si(111) substrate to be 104% indicates that Ge layer is experienced a little tensile strain.

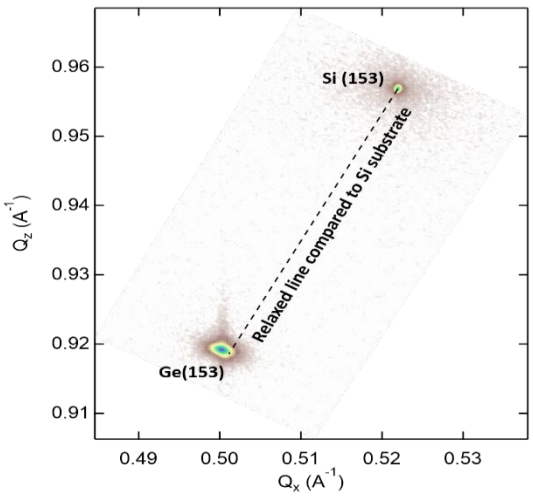

Figure 4.2: XRD reciprocal space mapping (RMS) image of the base Ge layer around the asymmetrical (153) reciprocal space point.

Raman spectroscopy was used to examine the strain states of HT Ge layer. The Ge layer peak is shifted towards the lower wavenumber compared to a bulk Ge peak as shown in Fig. 4.3, meaning that the HT Ge layer have the tensile strain. The in-plane tensile strain of the HT Ge layer was evaluated by using a following equation $\omega = 300.5 - 400\varepsilon_{11}$ where ω is a Raman shift wavenumber of the Ge-Ge mode and ε_{11} is the in-plain strain. Obtained amounts of the strains is 0.22% for the HT-Ge grown on the Si(111). The tensile strain in Ge epilayers

originates from the difference of thermal expansion co-efficient between Ge and Si. During the cooling of the Ge epilayers, which are grown on the Si at high temperatures and almost fully strain-relaxed, thermal shrinkage of the Ge is suppressed by the underneath Si substrate with the lower thermal expansion coefficient.

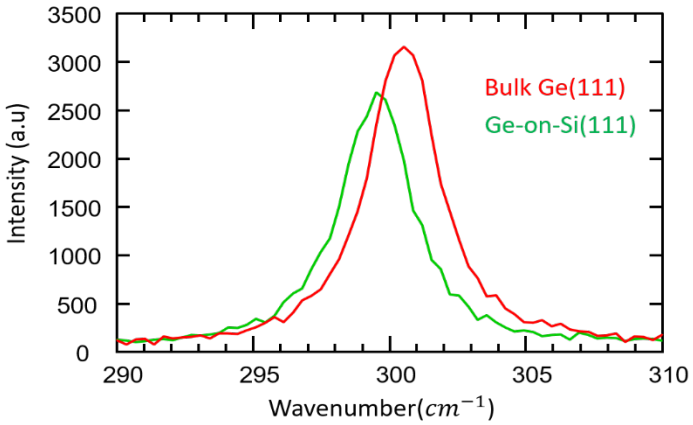

Figure 4.3: Raman spectra for a 650nm thick Ge layer grown on a Si(111) substrate and for bulk Ge.

4.2.3 Roughness of the base Ge layer

The higher dislocation density of a layer is responsible for higher surface roughness. Figure 4.4 shows the AFM image of the base Ge layer that is used in this study to fabricate the $Si_{1-x}Ge_x$ layer on it. It is clearly observe that RMS roughness of the base Ge layer is 0.33 nm that is significantly low surface roughness compare to the reported RMS roughness until now typically several nm. It is speculated that after annealing the Ge-on-Si(111), dislocation density reduced by melting surface and redistributed threading dislocations in Ge layer resulting the lower RMS surface roughness.

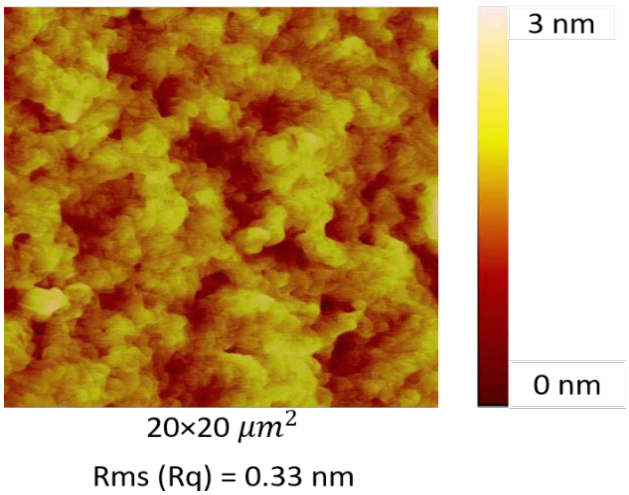

Figure 4.4: AFM image for a 650nm thick Ge layer grown on a Si(111)

4.3 Fabrication of Ge-rich $Si_{1-x}Ge_x$ layer

The epitaxial growth process and growth parameters are presented in this investigation. The composition of the $Si_{1-x}Ge_x$ layer was analyzed using XRD and SIMS profiles for investigation of composition profiles depending on (111) and (100) lattice plane orientation.

4.3.1 Structure of $Si_{1-x}Ge_x$ layer with growth parameter

To investigate the critical thickness for strain relaxation of Ge-rich $Si_{1-x}Ge_x$ layers, all samples were grown by using solid-source molecular beam epitaxy (MBE). First, a 50nm thick pure Ge buffer layer was grown on the substrates for starting from atomically smooth Ge surface. After that, various thickness of $Si_{1-x}Ge_x$ ($0.7 \leq x \leq 0.9$) layers were grown simultaneously on the Ge(111), Ge(100) and Ge-on-Si(111) substrates at 350°C for comparative investigation as shown in Fig. 4.5. The samples are annealed at 500°C for 3 minutes by using rapid thermal annealing system (RTA) for observing the thermal stability of strain states of post-annealed samples.

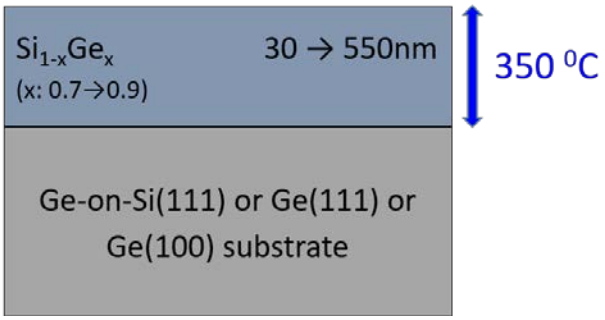

Figure 4.5: $Si_{1-x}Ge_x$ layer structure for investigating strain states.

4.3.2 SIMS profiles of $Si_{1-x}Ge_x$ layer grown on (111) and (100) lattice planes

In this section an investigation of composition profiles of Si and Ge in $Si_{1-x}Ge_x$ layer fabricated on (111) and (100) lattice plane orientations are presented. The thickness and composition of the fabricated layers are obtained from SIMS profiles of the individual samples. A series of samples were grown for this study where only partial relaxed samples were characterized by using RSM images and the rest of strained samples were characterized by using rocking curves. The compositions and thickness of all strained $Si_{1-x}Ge_x$ samples were quantified from reliable simulation by fitting thickness fringes of $Si_{1-x}Ge_x$ samples . In

simulation results, a discrepancy was observed between the compositions of the $Si_{1-x}Ge_x$ layers fabricated on (111) and (100) lattice plane orientations. As a result, an experimental uncertainty was arise to obtain accurate compositions of the $Si_{1-x}Ge_x$ layer on (111) and (100) lattice plane, which are quantified accurately by performing secondary ion mass spectrometry (SIMS) measurement on a selected sample. The SIMS profiles were also used to observe the diffusion of atoms in the interface region between epitaxial $Si_{1-x}Ge_x$ layer and prior Ge buffer. Figure 4.6 shows Si and Ge SIMS profiles for simultaneously grown 50nm thick $Si_{0.24}Ge_{0.76}$ on Ge(111) and Ge(100) substrates. It is observe that Si and Ge diffusion completely suppressed with very abrupt defect-free SiGe/Ge interfaces. The concentrations of Si and Ge are 0.24 & 0.76 respectively for $Si_{0.24}Ge_{0.76}$ /Ge(111) and 0.241 & 0.759 respectively for $Si_{0.24}Ge_{0.76}$ /Ge(100) are obtained. Therefore, it is clear that epitaxial growth in MBE is independent of lattice plane orientation.

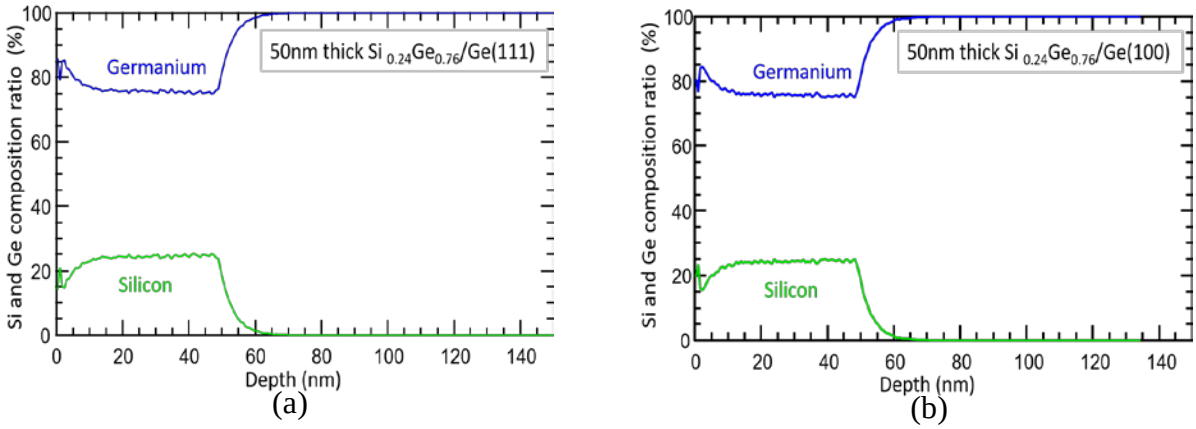

Figure 4.6: Si and Ge SIMS profiles for the 50nm thick $Si_{0.24}Ge_{0.76}$ layer on (a) Ge(111) and (b) Ge(100) substrates.

The Ge contents x of the $Si_{1-x}Ge_x$ pseudomorphic layers were evaluated using the following equations, whereas reciprocal space mapping (RSM) was used for partial relaxed layer. The simulated and evaluated values of Si and Ge compositions are same.

$$a_{SiGe}^{\perp} = \frac{\lambda\sqrt{h^2+k^2+l^2}}{2\sin\omega} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

$$a_{SiGe}^{\perp} = a_{SiGe} + \left(\frac{2\nu}{1-\nu}\right)(a_{SiGe} - a_{Si}) \dots\dots\dots\dots\dots (2)$$

$$a_{SiGe} = 5.43105 + 0.1988x + 0.028x^2 \dots\dots\dots (3)$$

Where, ω is SiGe peak value (obtained from XRD rocking curve), $a_{SiGe}^{\perp}$ is perpendicular lattice parameter of the layer, a_{SiGe} is the bulk lattice parameter of the layer, a_{Si} is the lattice parameter of bulk Si and ν is the Poisson ratio (obtained from Ref. 21).

4.4 Properties of $Si_{1-x}Ge_x$ layers fabricated on Ge (111) substrate

The strain states, surface roughness and thermal stability of strain states of the Ge-rich $Si_{1-x}Ge_x$ layer grown on Ge (111) are investigated and presented in this section. The experimental error of the values of compositions, which are reported within ± 0.005. Relaxation of the layer is accurate to within ± 0.005, root mean square roughness are accurate up to ± 0.3 and height ranges are within ± 2.

4.4.1 Strain states of $Si_{1-x}Ge_x$ on Ge (111) substrate

In this section, the strain states of the $Si_{1-x}Ge_x$ layers on a Ge (111) substrate are observed by using XRD profiles. Omega-2Theta (ω-2θ) scans of (333) diffraction orders for (111) lattice planes orientation was performed to examine the strain states of $Si_{1-x}Ge_x$ layers grown on the Ge (111) substrate with various thickness. Figure 4.7 shows the XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on the Ge(111) substrate with various thickness before and after annealing. The thickness fringes appear on both sides of the layer peak and angular spacing decreases in the 50 to 160nm range meaning that 40 to 160nm thick layers are fully pseudomorphic and the strain relaxation takes place for the 180nm thick layer because the thickness fringes disappear as shown in Fig. 4.7(a). The relaxation of the 180nm thick $Si_{0.24}Ge_{0.76}$ layer was calculated by using RSM to be 3%. The thermal stability of the strain states of the $Si_{0.2}Ge_{0.8}$ layers are observed by annealing the layers grown on the Ge(111) substrate. For the 130nm thick layer, the thickness fringes clearly observe on both sides of the layer peak before annealing as shown in Fig. 4.7(a), but the fringes disappear and the layer peak intensity decreases after annealing as shown in Fig. 4.7(b). The less intense and broad peak indicates that strain relaxation takes place for the 130nm thick layer after annealing, whereas the 90nm thick layer remains pseudomorpic after annealing as shown in Fig. 4.7(b).

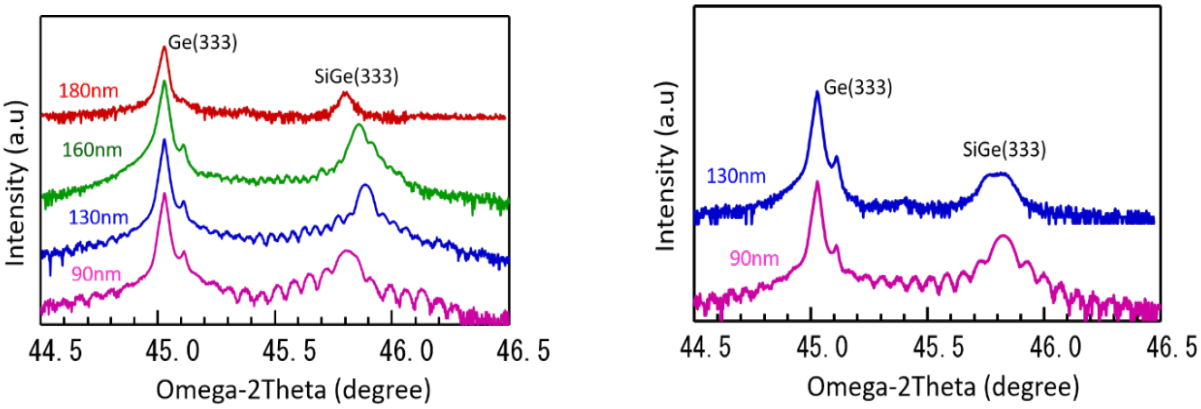

Figure 4.7: XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on Ge(111) substrate for the various thickness (a) before annealing and (b) after annealing.

The thermal effect of the strain states of the 130nm thick $Si_{0.25}Ge_{0.75}$ layers before and after annealing are precisely observed by using XRD reciprocal space mapping (RSM) image. Figure 4.8 shows RSM image around asymmetrical (153) reciprocal space point for the 130nm thick $Si_{0.25}Ge_{0.75}$ layers before and after annealing. The thickness fringes clearly observe in RSM image for the $Si_{0.25}Ge_{0.75}$ layer before annealing as shown in Fig. 4.8(a) indicating that the layer is completely pseudomorphic. On the other hand, the $Si_{0.25}Ge_{0.75}$ layer peak shifts away from the strained line compared to Ge substrate as shown in Fig. 4.8(b), meaning that after annealing relaxation takes place and the relaxation of the 130 nm thick $Si_{0.25}Ge_{0.75}$ layer after annealing was evaluated compared to Ge to be 29%.

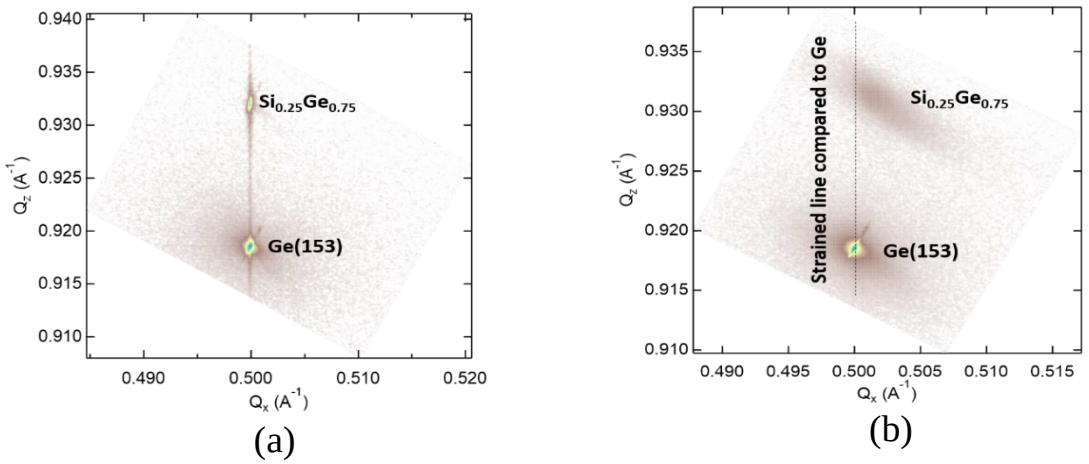

Figure 4.8: XRD for asymmetric (153) RSM of the 130 nm thick $Si_{0.25}Ge_{0.75}$ layer grown on the Ge (111) substrate for (a) before annealing and (b) after annealing.

4.4.2 Surface roughness of $Si_{1-x}Ge_x$ on Ge (111) substrate

Figure 4.9 shows Laser Microscope (LM) images of various thickness SiGe layers grown on the Ge (111) substrates before annealing. Relaxation ratios in mm scale wide areas measured by x-ray diffraction (XRD) analyses (not shown here) are indicated in each image. For the 50 nm thick $Si_{0.25}Ge_{0.75}$ (Fig. 4.9(a)), the relaxation ratio is 0 % and the surface exhibits no roughness. For the 130 nm thick $Si_{0.25}Ge_{0.75}$ (Fig. 4.9(b)), it is observed that line-shaped ridges are created on the SiGe surfaces although the relaxation ratio is ~ 0 %. It was confirmed that the ridge lines are aligned on intersections of equivalent (111) planes and the surface. For the 180 nm thick $Si_{0.24}Ge_{0.76}$ (Fig. 4.9(c)), the number of the ridges increases and the relaxation ratio also increases to 3 %, indicating that this thickness exceeds t_c. From observation of other samples, it was found that the density of the ridges gradually increases as the layer thickness increases. Figure 4.9(d) shows an AFM image of the selected region of the LM image in Fig. 4.9(c). The line-shaped ridge is very clearly seen and its height and width are estimated to be around 10 nm and 1-2 μm, respectively. It is also found that outside of the ridge the SiGe surface is very flat. Values of mean surface roughness (Ra) obtained by AFM are 0.07-0.10 nm for the 50 nm thick layer and 0.1-0.3 nm for the 130 and 180 nm thick layers.

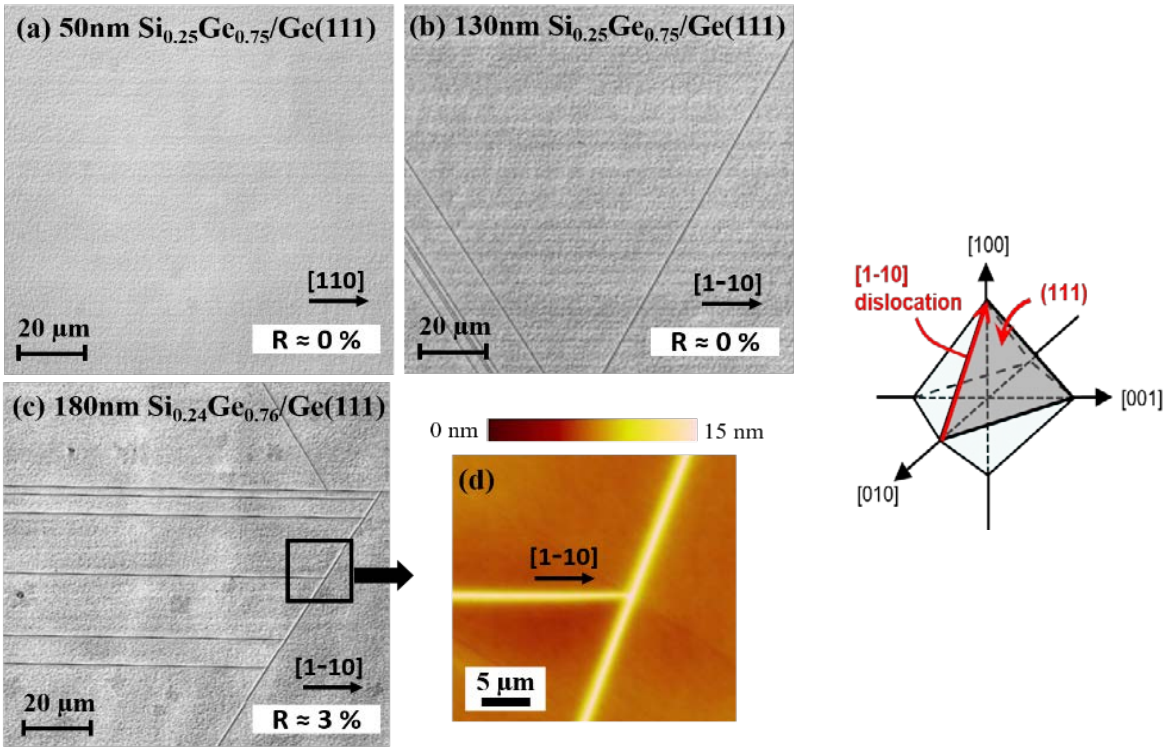

Figure 4.9: Laser microscopic images before annealing for (a) 50 nm thick $Si_{0.25}Ge_{0.75}$, (b) 130 nm thick $Si_{0.25}Ge_{0.75}$, (c) 180 nm thick $Si_{0.24}Ge_{0.76}$ layers grown on Ge(111) substrates. (d) An AFM image for the selected area of (c).

Atomic force microscope (AFM) images were used for clear observation of the surface morphology of the SiGe layer grown on Ge (111) substrate as shown in Fig. 4.10. The root mean square (RMS) surface roughness and height range are mentioned where these values depend on the density and height of the ridge in the scanning area.

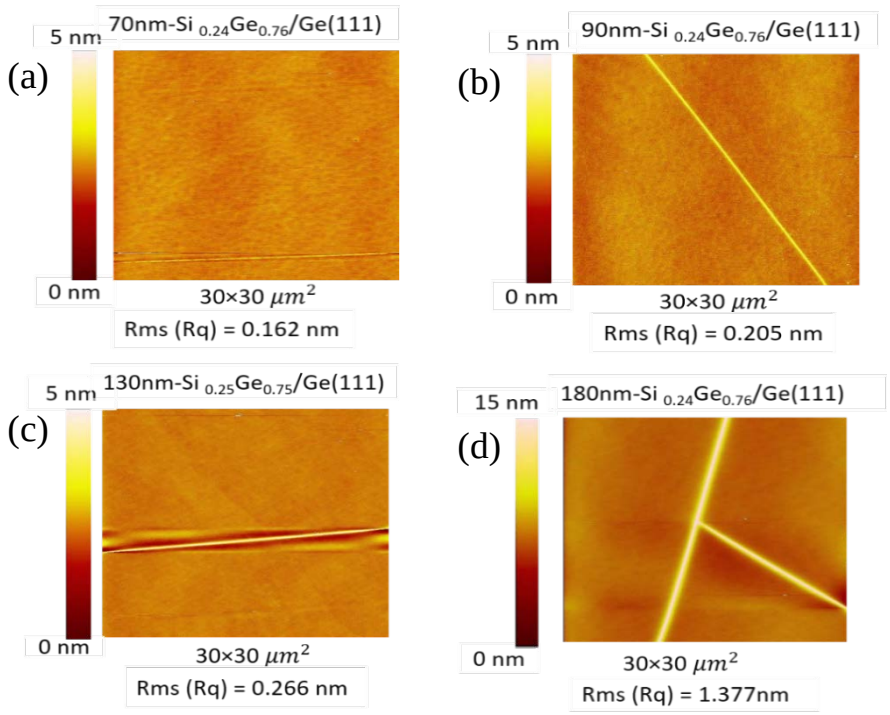

Figure 4.10: AFM images of the surface of SiGe layers grown on the Ge (111) substrate before annealing for the (a) 70nm thick $Si_{0.24}Ge_{0.76}$ layer, (b) 90nm thick $Si_{0.24}Ge_{0.76}$ layer, (c) 130nm thick $Si_{0.25}Ge_{0.75}$ layer & (d) 180nm thick $Si_{0.24}Ge_{0.76}$

Next we investigated changes in the surface morphologies after annealing. It was confirmed by LM measurements (Figures 4.11(a) and (b)) that the distribution as well as the density of the ridges appearing before annealing remain unchanged after annealing. Figures 4.11(c) and (d) show AFM images in ridge-free areas of the 130 nm thick $Si_{0.25}Ge_{0.75}$ on the Ge(111) substrate before and after annealing, respectively. While the surface has no roughness before annealing, a number of trenches are generated after annealing. Their directions are along [10-1], [-110] and [0-11], that is, the intersections of equivalent (111) planes and the surface, which is the same as the ridges observed in Fig. 4.9. High density trenches with those directions are clearly forming partial triangle shapes. These results imply that the trenches are formed due to misfit dislocation gliding towards the surface during the annealing. Strain relaxation ratio obtained by XRD from the wide-area significantly increases from 0 to 29% after annealing. By characterizations for other SiGe samples, it was confirmed that the density of the dislocation-

related trenches increases as the layer thickness increases, leading to the larger relaxation ratios. It is observed that the density and depth of the additional dislocation-related trenches increase as the layer thickness as well as relaxation ratio increases.

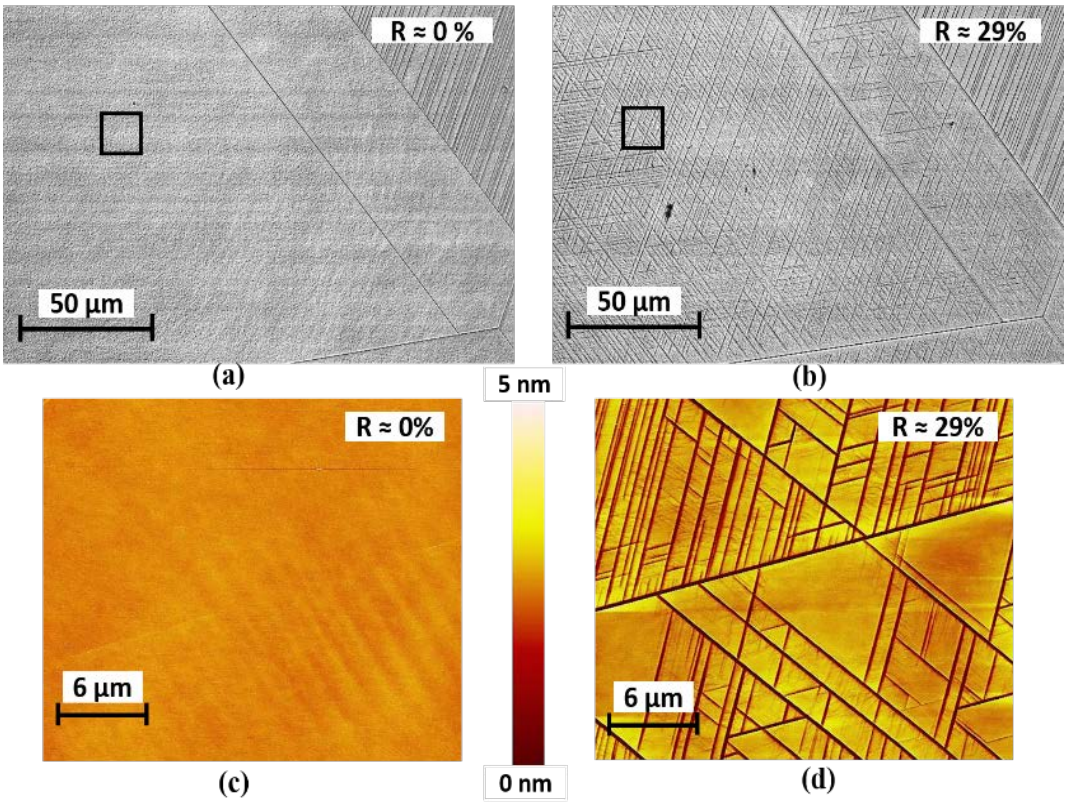

Figure 4.11: Laser microscopic images for 130 nm thick $Si_{0.25}Ge_{0.75}$/Ge(111) (a) before and (b) after annealing. AFM images for 130 nm thick $Si_{0.25}Ge_{0.75}$/Ge(111) (c) before and (d) after annealing. AFM scan area is ridge-free surface region indicated by a square in Fig. (a) & (b).

4.4.3 Ridge formation mechanism

An origin of the ridge formation can be considered as follows. First, due to the strain energy accommodated in the strained SiGe film, misfit dislocations are nucleated at an interface between the SiGe and Ge and glide through equivalent (111) slip planes. The tensile strain in the SiGe is locally relieved along the dislocations, leading to laterally inhomogeneous strain distribution. Due to this the growth rate of the SiGe is locally modified and the SiGe growth thickness is enlarged around the dislocations, forming the surface ridges. Similarly to the dislocations, the directions of the ridges correspond to intersections of the equivalent (111) planes and the surface (111) plane as seen in Fig. 4.9. From the derived relaxation ratios (~ 50%), a number of dislocations are speculated to be generated and accumulated after gliding within the ridge region, and detailed observation of the dislocations is underway. These line-

shaped ridges were observed also for $Si_{1-x}Ge_x$ layers grown on the Ge-on-Si(111) and Ge(100) substrates with various thicknesses and compositions whereas the conditions are quite different depending on the substrates, which will be discussed next sections.

Strain states in and out of the ridge regions are investigated by micro Raman measurements. Since the width of the ridge is 1-2 μm, the laser beam can be focused within the ridge and spectrum only from the ridge region can be obtained. Figure 4.12 shows Raman spectra in and out of the ridge for 180 nm thick $Si_{0.24}Ge_{0.76}$ on Ge(111). The Ge-Ge, Si-Ge and Si-Si phonon mode peaks in the ridge are observed to shift to higher wavenumbers from those out of the ridge. Here, peak shifts $\Delta\omega_{Ge\text{-}Ge}$ and $\Delta\omega_{Ge\text{-}Si}$ are defined as differences in Raman peak values between in and out-of ridge regions for Ge-Ge and Si-Ge phonon modes, respectively, as shown in Fig. 4.12. In general, such phonon mode peaks shift due to the modification of strain and/or Ge contents in SiGe layer [84, 85]. On the other hand, it is expected that the Ge-Ge and Si-Ge mode peaks shift to higher wavenumbers whereas the Si-Si mode peak shifts to lower wavenumbers with increasing Ge contents in a SiGe layer. Therefore, considering the observation of the peak shifts (Fig.4.12), it can be concluded that the tensile strain in the ridge region is partially relaxed and the Ge content modification is negligible. A relaxation ratio in the ridge region is estimated to be approximately 60 % from the obtained $\Delta\omega_{Ge\text{-}Ge}$ ($2.3cm^{-1}$). Inset shows $\Delta\omega_{Ge\text{-}Ge}$ and $\Delta\omega_{Ge\text{-}Si}$ as a function of the SiGe thickness. As the thickness increases, the peak shifts also increase, which means the strain relaxation proceeds with the thickness locally in the ridge. On the other hand, the relaxation hardly takes place on the ridge-free areas, resulting in averaged wide-area relaxation ratio as low as 3% obtained by XRD in mm scale.

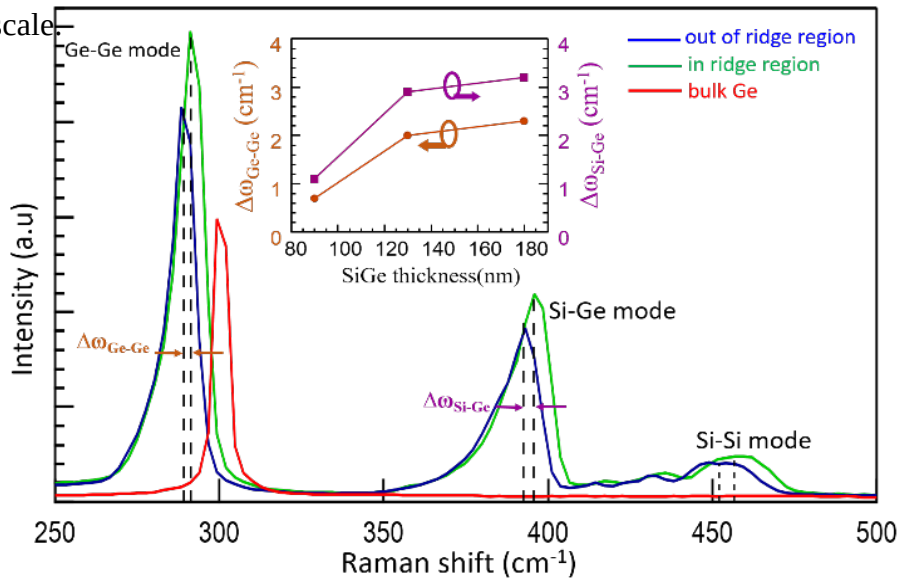

Fig. 4.12: Raman spectra in and out of the ridge for 180 nm thick $Si_{0.24}Ge_{0.76}$ on the Ge(111) substrate. Inset shows the peak shifts $\Delta\omega_{Ge\text{-}Ge}$ and $\Delta\omega_{Ge\text{-}Si}$ as a function of the SiGe thickness.

4.4.4 Ridge height

Figure 4.13 shows the ridge height with the thickness of $Si_{0.2}Ge_{0.8}$ grown on Ge(111), Ge-on-Si(111) and Ge(100) substrates. It is observe that the ridge height increases as the layer thickness increase as well as the strain relaxation in the ridge area increases. Since the strain relaxations are different for 130nm thick $Si_{0.2}Ge_{0.8}$ layer grown on Ge(111), Ge-on-Si(111) and Ge(100) substrates, the ridge heights are different for different substrates (Fig. 4.13). It is observed that the ridge height changes as the strain states of the layer changes.

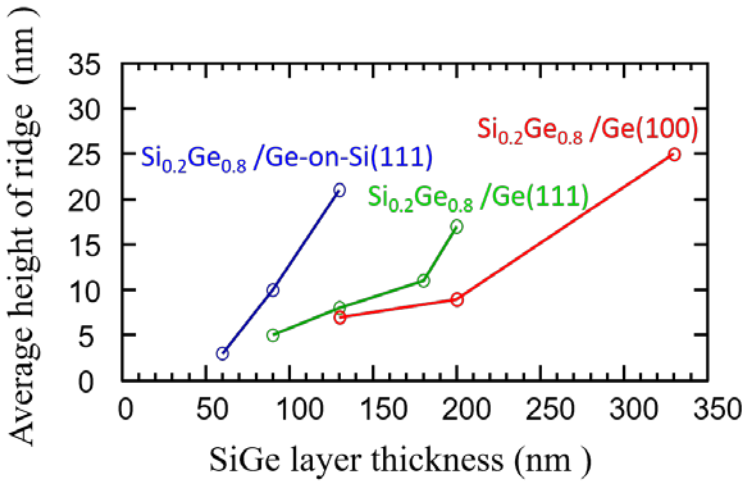

Fig. 4.13: Average height of the ridge formed on the surface of $Si_{0.2}Ge_{0.8}$ layer grown on Ge(111), Ge-on-Si(111) and Ge(111) substrates as a function of the $Si_{0.2}Ge_{0.8}$ layer thickness.

4.5 Properties of $Si_{1-x}Ge_x$ layers fabricated on Ge-on-Si (111)

In this section an investigation of the individual properties of strain states, surface roughness and thermal stability of strain states of the Ge-rich $Si_{1-x}Ge_x$ layer grown on Ge-on-Si (111) are reported. The base layer which was presented in section 4.2 used underneath of $Si_{1-x}Ge_x$ layer. The experimental error of the values of compositions, which are reported within ± 0.005. Relaxation of the layer is accurate to within ± 0.005, root mean square roughness are accurate up to ± 0.3.

4.5.1 Strain states of $Si_{1-x}Ge_x$ on Ge-on-Si (111)

The strain states of the $Si_{1-x}Ge_x$ layers on Ge-on-Si (111) examine by using XRD profiles are presented in this section. Omega-2Theta (ω-2θ) scans of (333) diffraction orders for (111) lattice planes orientation was performed to examine the strain states of $Si_{1-x}Ge_x$ ($0.7 \leq x \leq 0.9$) layers grown on the Ge-on-Si(111) with various thickness. Figure 4.14(a) shows the XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on the Ge-on-Si(111) with various thickness before annealing. The SiGe layers peak become narrower and more intense as the thickness increases in the range of 40 to 110nm (all XRD profiles not shown in Fig.4.14), where the layers peak are not at same incident angle because of slightly difference of Ge concentrations in the SiGe layers (75.7 to 77.6%). The thickness fringes appear on both sides of the layer peak and angular spacing decreases with the thickness increases, which indicates that 40 to 110nm thick layers are fully pseudomorphic. On the contrary, thickness fringes completely disappear and the intensity of the layer peak decreases for the 130nm thick layer, which indicates that partial strain relaxation takes place. The relaxation ratio estimated from XRD reciprocal space mapping (RSM) was 7%.

The thermal stability of the strain states of the $Si_{0.2}Ge_{0.8}$ layers are observed by annealing the layers. It was investigated that pseudomorphic condition changes with change in anneal temperature and time. Figure 4.14(b) shows the XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on the Ge-on-Si(111) with various thickness after annealing at 500°C for 3 minutes. Clear thickness fringes was observe until 60 nm thick layers. For the 70nm thick $Si_{0.24}Ge_{0.76}$ layer, the thickness fringes are clear before annealing as shown in Fig.4.14(a) whereas after annealing the thickness fringes are completely disappear and the layer peak intensity decreases with angular shift towards the substrate peak as shown in Fig.4.14(b). It reveals that after annealing, the strain relaxation takes place for the 70nm thick layer. On the other hand, the 60nm thick SiGe layer remains pseudomorphic even after annealing the layer as shown in Fig.4.14(b).

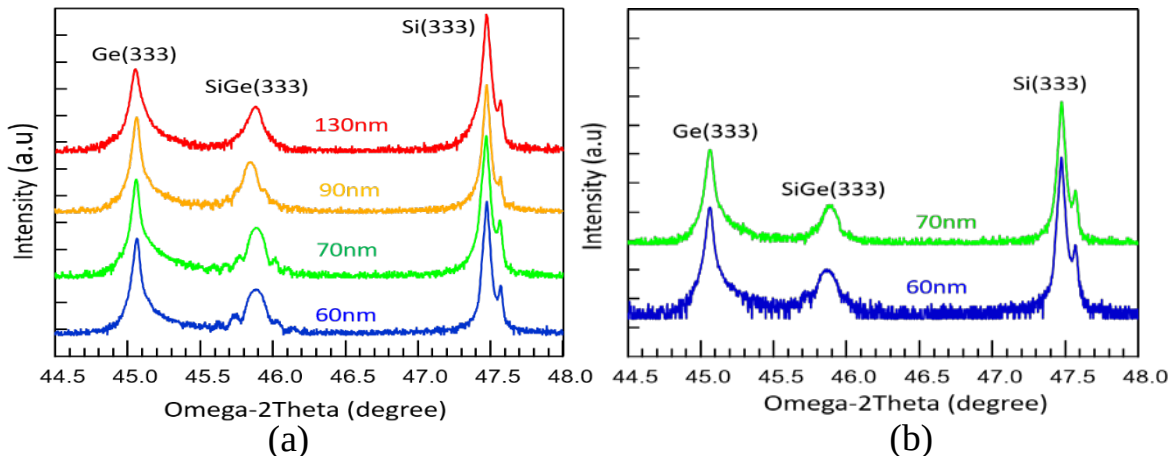

Figure 4.17: XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on Ge-on Si(111) for the various thickness (a) before annealing and (b) after annealing.

The strain states of the 70nm thick $Si_{0.24}Ge_{0.76}$ layers before and after annealing are precisely observed by using RSM image. Figure 4.8 shows RSM image around asymmetrical (153) reciprocal space point for the 70nm thick $Si_{0.24}Ge_{0.76}$ layers before and after annealing. The $Si_{0.24}Ge_{0.76}$ peak is align with the strained line compared to Ge as shown in Fig. 4.15(a), whereas the peak is slightly shifts away from the strained line as shown in Fig. 4.15(b), meaning that after annealing relaxation takes place. The relaxation of the $Si_{0.24}Ge_{0.76}$ layer after annealing was evaluated compared to the base Ge layer to be 9%.

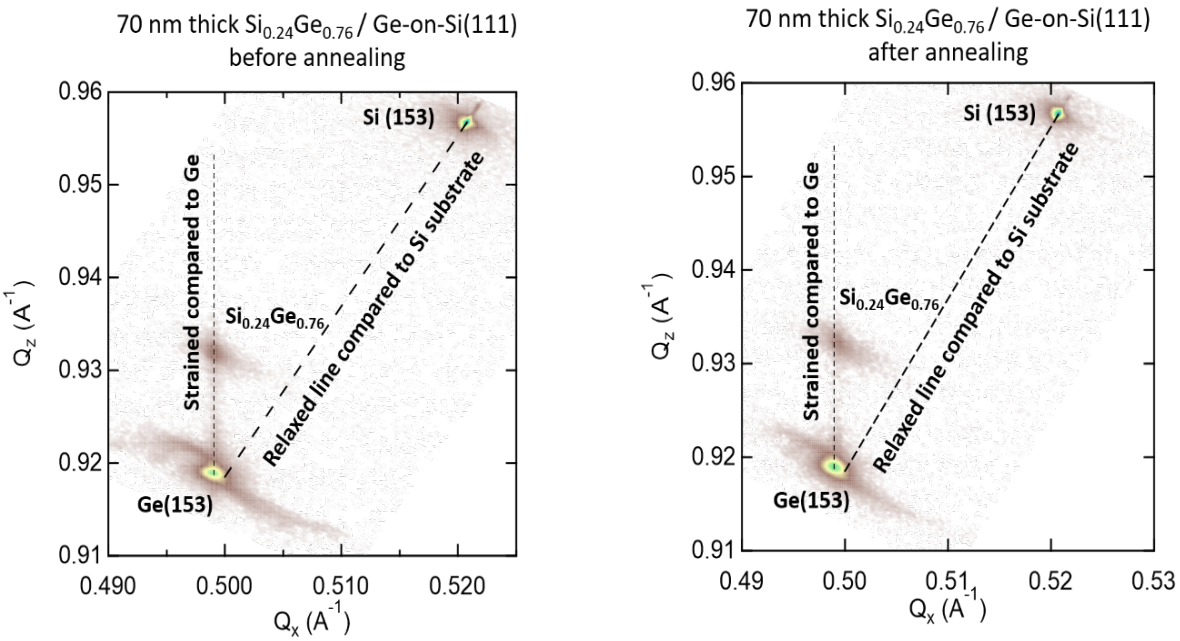

Figure 4.15: XRD for asymmetric (153) RSM of the 70 nm thick $Si_{0.24}Ge_{0.76}$ layers grown on Ge-on Si(111) (a) before annealing and (b) after annealing.

Investigation of strain states depend on base layer parameter such as thickness and/or growth temperature of the base layer are also presented. For this investigation, various thick SiGe layers with same concentration are fabricated simultaneously on the various base Ge layers that are grown with different growth temperature and thickness. Figure 4.16 shows that XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on Ge-on Si(111) simultaneously at 350°C where Ge-on-Si(111) thickness and growth temperature are different to each other. In this study, three types of Ge-on-Si(111) are used that are: 650nm thick Ge-on-Si(111) grown at 700°C,

1000nm thick Ge-on-Si(111) grown at 700°C and 800nm thick Ge-on-Si(111) grown at 750°C. It is observe that thickness fringes are appear for 100 nm thick $Si_{0.2}Ge_{0.8}$ layer, whereas fringes disappear for 130 nm thick layer even the base layers conditions are different. This reveals that the strain states remain unchanged and independent of the base layer condition.

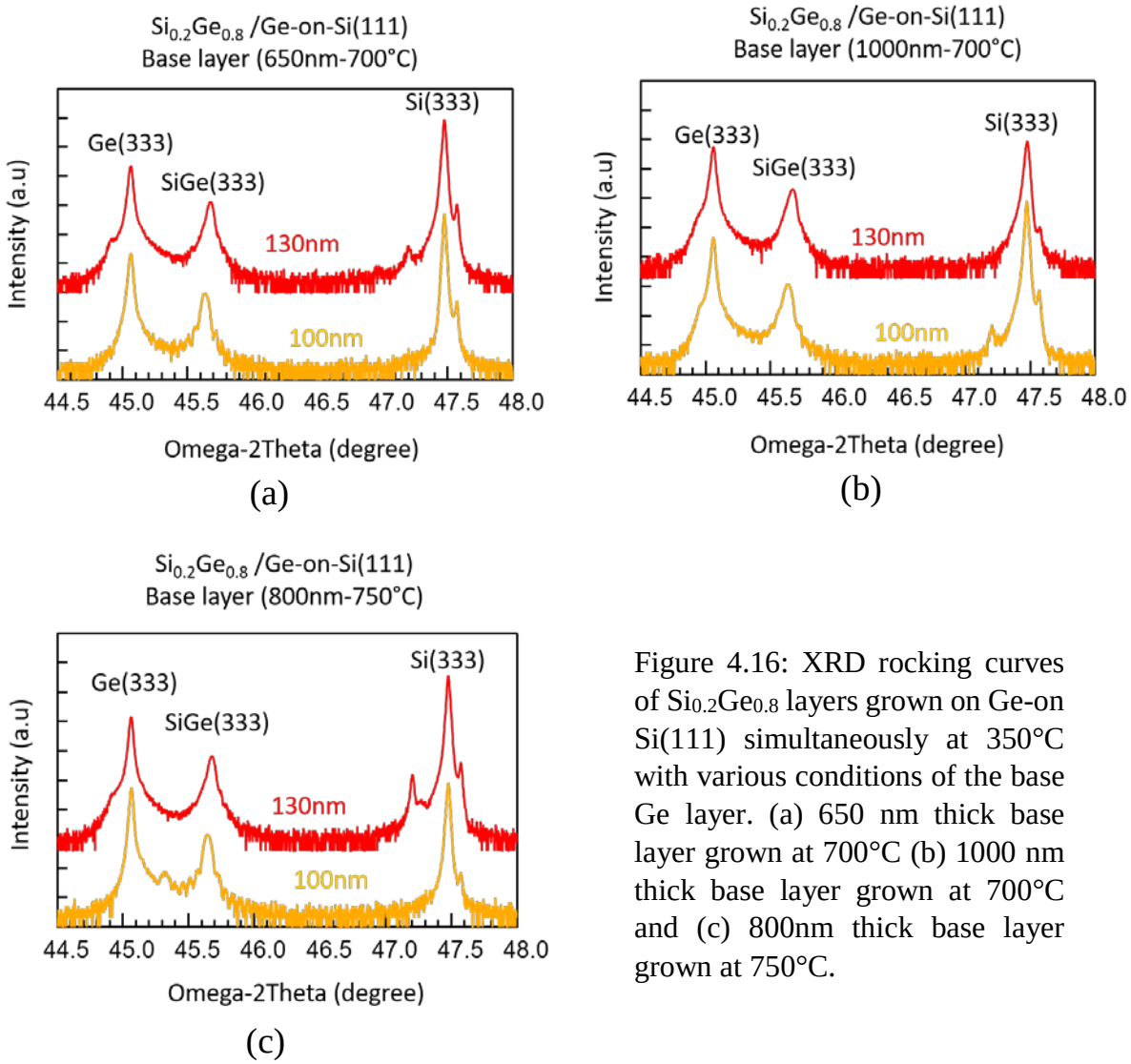

Figure 4.16: XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on Ge-on Si(111) simultaneously at 350°C with various conditions of the base Ge layer. (a) 650 nm thick base layer grown at 700°C (b) 1000 nm thick base layer grown at 700°C and (c) 800nm thick base layer grown at 750°C.

4.5.2 Surface roughness of $Si_{1-x}Ge_x$ on Ge-on-Si (111)

The surface morphology of the $Si_{1-x}Ge_x$ layers grown on Ge-on-Si(111) are investigated by using AFM for small surface area and microscopic image for wide surface area that are presented in this section.

A laser microscope was used to investigate wide-area surface morphologies of the $Si_{1-x}Ge_x$ layers particularly for observation of initial stages of strain relaxation. Figure 4.17 shows laser microscopic images of the $Si_{1-x}Ge_x$ layers fabricated on the Ge-on-Si(111). It is observe that thin-line ridges were created on the SiGe surfaces with the thickness over 60nm even though the thickness fringes appeared clearly as shown in Fig. 4.17 (b)& (c). Figure 4.17(d) shows the partial relaxed layer morphology with such ridges. These ridges are not created uniformly over the surface due to inhomogeneity of strain on the surface and the density of the ridges gradually increases as the strain or the layer thickness increases. On the other hand, ridges were not found for very thin SiGe layers below 50nm thickness as shown in Fig. 4.17(a). The density of ridge evaluation accurately is almost impossible due to its inhomogeneity on the surface.

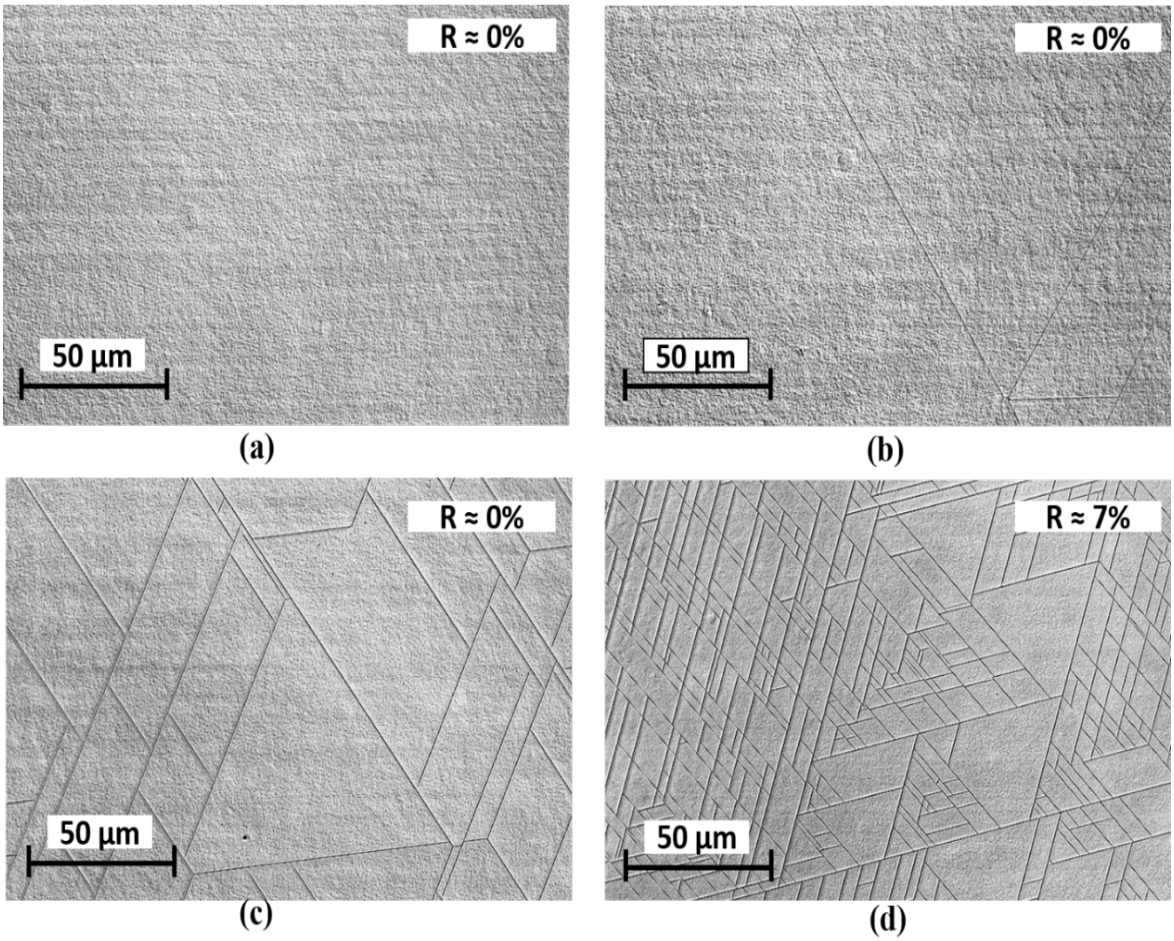

Figure 4.17: Laser microscopic images of the surface of SiGe layers grown on the Ge-on-Si(111) substrate before annealing for the (a) 50nm thick $Si_{0.25}Ge_{0.75}$ layer, (b) 60nm thick $Si_{0.24}Ge_{0.76}$ layer, (c) 70nm thick $Si_{0.24}Ge_{0.76}$ layer & (d) 130nm thick $Si_{0.25}Ge_{0.75}$ layer.

AFM measurement was performed for clear observation of surface morphology of the SiGe layer grown on Ge-on-Si(111) as shown in Fig. 4.18. The root mean squared (RMS) surface roughness and height range are mentioned with image though these values depend on the density and height of the ridge in the scanning area.

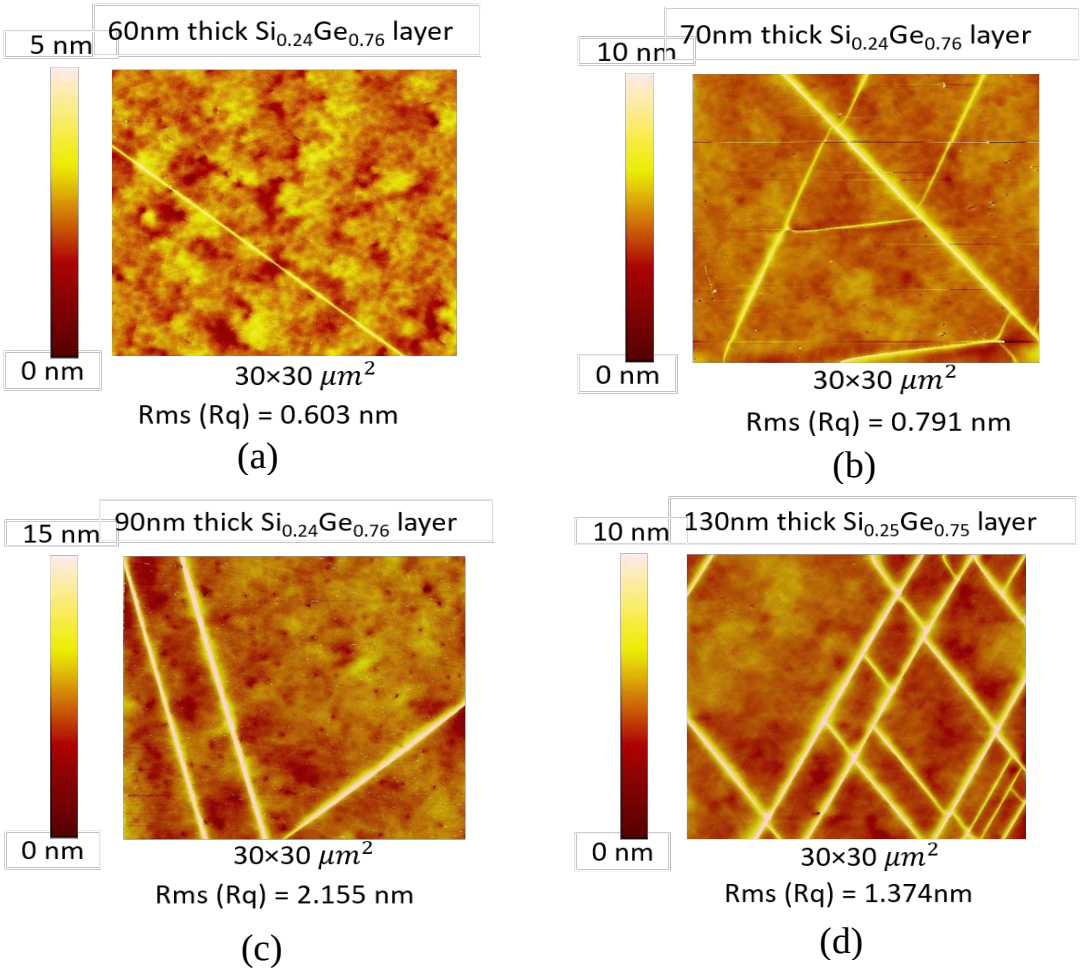

Figure 4.18: AFM images of the surface of SiGe layers grown on the Ge-on-Si(111) substrate before annealing for the (a) 60nm thick $Si_{0.24}Ge_{0.76}$ layer, (b) 70nm thick $Si_{0.24}Ge_{0.76}$ layer, (c) 90nm thick $Si_{0.24}Ge_{0.76}$ layer & (d) 130nm thick $Si_{0.25}Ge_{0.75}$ layer.

The ridge remain same density even the samples are annealed at higher temperature than the layer growth temperature. Figures 4.19 (a) & (b) show the microscopic images of the 70 nm thick $Si_{0.24}Ge_{0.76}$ layer for before and after annealing respectively. It is observe that density of ridge neither increases nor decreases after annealing the 70 nm thick $Si_{0.24}Ge_{0.76}$ layer. Tapping-mode AFM images are used to investigate the surface morphology for next stages of relaxation. Figures 4.19 (c) & (d) show the AFM images of the 70nm thick $Si_{0.24}Ge_{0.76}$ layer grown on the Ge-on-Si(111) before and after annealing respectively. In

addition to the ridges, a number of trenches appear after annealing presumably due to misfit dislocation glides towards the surface during the annealing, whereas very few trenches are observed before annealing. These additional dislocation-related trenches largely contribute to increase the strain relaxation of the layer, resulting in disappearance of fringes in XRD as seen in Fig.4.14(b). It is observed that the density and depth of the additional dislocation-related trenches increase as the layer thickness as well as relaxation ratio increases.

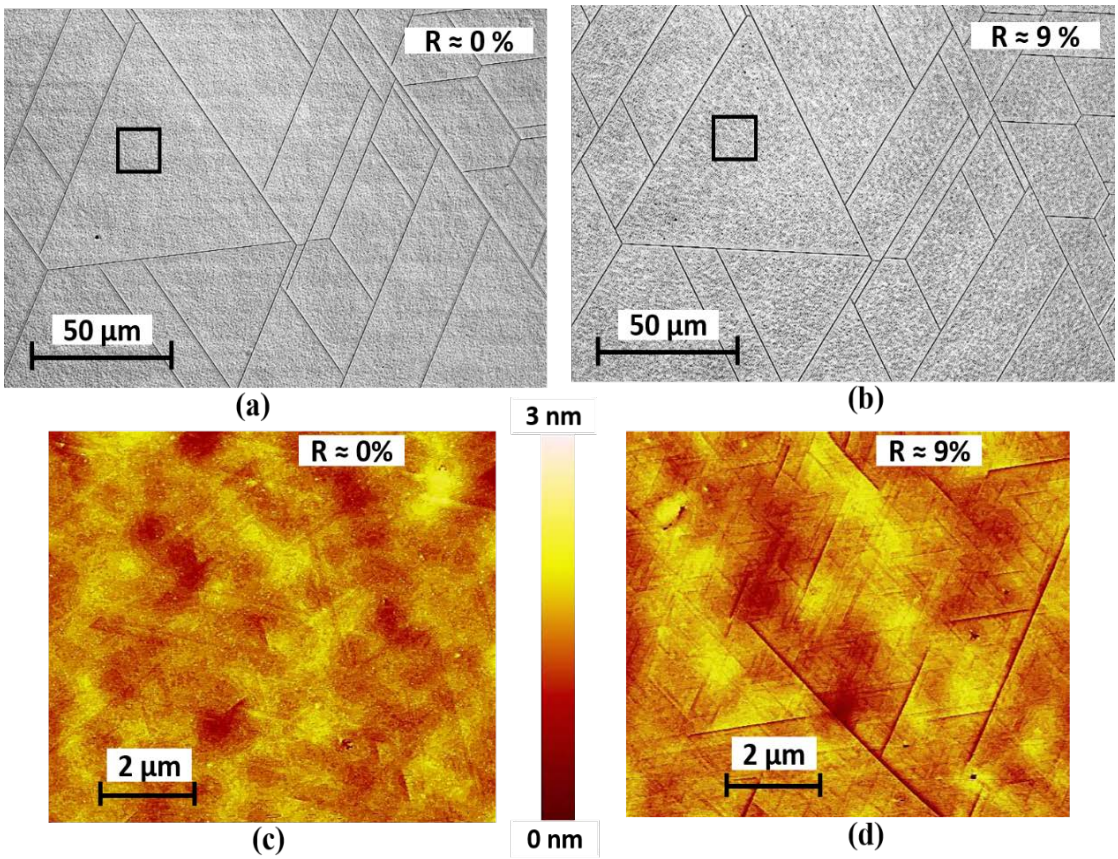

Figure 4.19: Laser microscopic images for 70 nm thick $Si_{0.24}Ge_{0.76}$/Ge-on-Si(111) (a) before and (b) after annealing. AFM images for 70 nm thick $Si_{0.24}Ge_{0.76}$/Ge-on-Si(111) (c) before and (d) after annealing. AFM scan area is ridge-free surface region indicated by a square in Fig. (a) & (b).

4.6 Properties of $Si_{1-x}Ge_x$ layers fabricated on Ge (100) substrate

For investigation of change in strain states due to the lattice plane orientation, the strain states, surface roughness and thermal stability of strain states of the Ge-rich $Si_{1-x}Ge_x$ layer grown on Ge (100) are presented in this section. The experimental error of the values of compositions, which are reported within ± 0.005. Relaxation of the layer is accurate to

within$\pm$0.005, root mean square roughness are accurate up to $\pm$0.3 and height ranges are within$\pm$2.

4.6.1 Strain states of $Si_{1-x}Ge_x$ on Ge (100) substrate

For the comparative study of the strain states of the $Si_{1-x}Ge_x$ layers fabricated on (100) lattice plane are investigated and reported in this section. Omega-2Theta (ω-2θ) scans of (004) diffraction orders for (100) lattice planes orientation was performed to observe the strain states of $Si_{1-x}Ge_x$ layers grown on the Ge (100) substrate with various thickness. Figure 4.20 shows the XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on the Ge(100) substrate with various thickness before and after annealing.

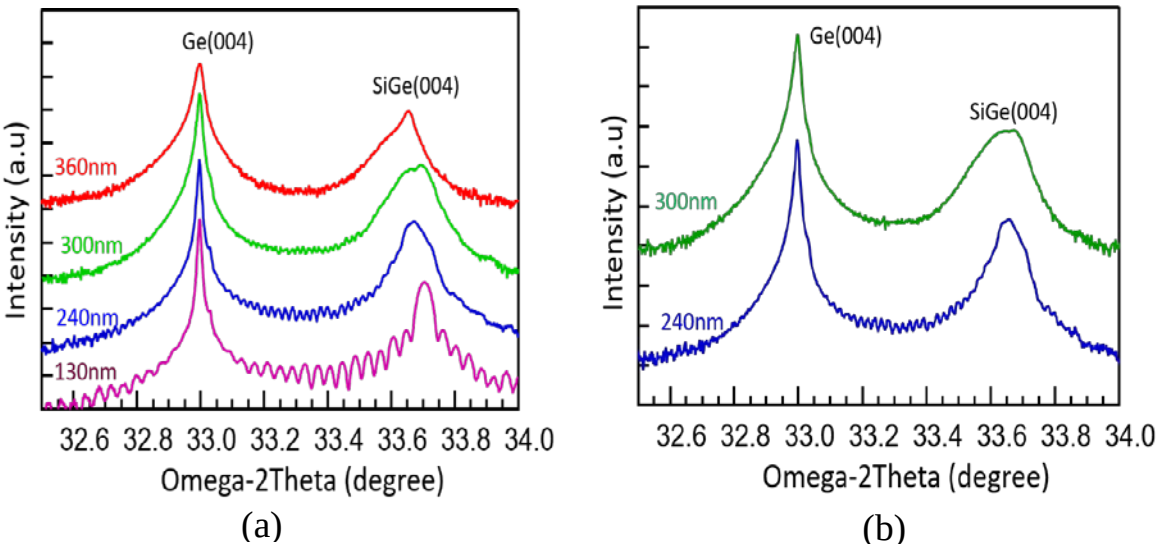

Figure 4.20: XRD rocking curves of $Si_{0.2}Ge_{0.8}$ layers grown on the Ge(100) substrate with the various thickness for (a) before annealing and (b) after annealing.

In the range of 40 to 300 nm thick $Si_{0.2}Ge_{0.8}$ layers are pseudomorphic because the thickness fringes appear on both sides of the layer peak and angular spacing decreases. The strain relaxation takes place for the 360nm thick layer because the thickness fringes disappear as shown in Fig. 4.20 (a). The relaxation of the 360nm thick $Si_{0.24}Ge_{0.76}$ layer was calculated by using RSM to be 2%. The thermal stability of the strain states of the $Si_{0.2}Ge_{0.8}$ layers are observed by annealing the layers grown on the Ge(100) substrate. For the 300nm thick layer, the thickness fringes appear before annealing as shown in Fig. 4.20 (a) whereas the fringes

disappear and the layer peak intensity decreases after annealing as shown in Fig. 4.20 (b) meaning that strain relaxation takes place after annealing. On other hand, the 240nm thick layer remains pseudomorpic after annealing as shown in Fig. 4.20(b).

The XRD RSM was performed to investigate the strain states of the 300nm thick $Si_{0.24}Ge_{0.76}$ layer after annealing. Figure 4.21 shows RSM image around asymmetrical (224) reciprocal space point for the 300nm thick $Si_{0.24}Ge_{0.76}$ grown on the Ge (100) substrate after annealing. The shape of the $Si_{0.24}Ge_{0.76}$ layer peak indicates that a small amount of relaxation takes place in the $Si_{0.24}Ge_{0.76}$ layer and the relaxation of the 300 nm thick $Si_{0.25}Ge_{0.75}$ layer after annealing was evaluated compared to Ge to be 2%.

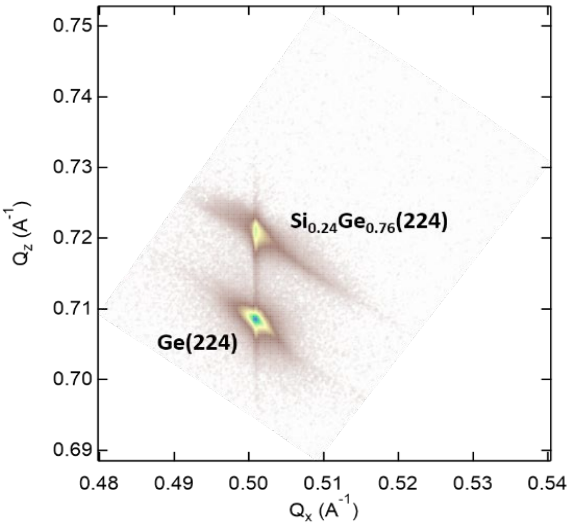

Figure 4.21: XRD for asymmetric (224) RSM of the 300 nm thick $Si_{0.24}Ge_{0.76}$ layer grown on the Ge (100) substrate after annealing.

4.6.2 Surface roughness of $Si_{1-x}Ge_x$ on Ge (100) substrate

An investigation of surface morphology of the $Si_{1-x}Ge_x$ layers grown on Ge (100) substrate by using a laser microscope and AFM measurements are presented in this section. Figure 4.22 shows laser microscopic images of the $Si_{1-x}Ge_x$ layers fabricated on the Ge (100) substrate. Like the 50 nm thick layer grown on (111) lattice plane, ridges were not created on the 50 nm thick $Si_{0.25}Ge_{0.75}$ layer grown on the Ge (100) substrate as shown in Fig. 4.22(a). In addition to the thin-line ridges, a number of thin-line trenches line also created on the surface before annealing with the thickness over 100nm even though it is pseudomorphic or partial relaxed. On the other hand, such ridges and trenches were not found below 90nm thickness.

These ridges and trenches are not created uniformly over the surface due to inhomogeneity of strain on the surface and the density of the ridges gradually increases as the strain or the layer thickness increases. The ridges with trenches are clearly observed by using AFM images for the SiGe layers grown on Ge (100) substrate as shown in Fig. 4.23.

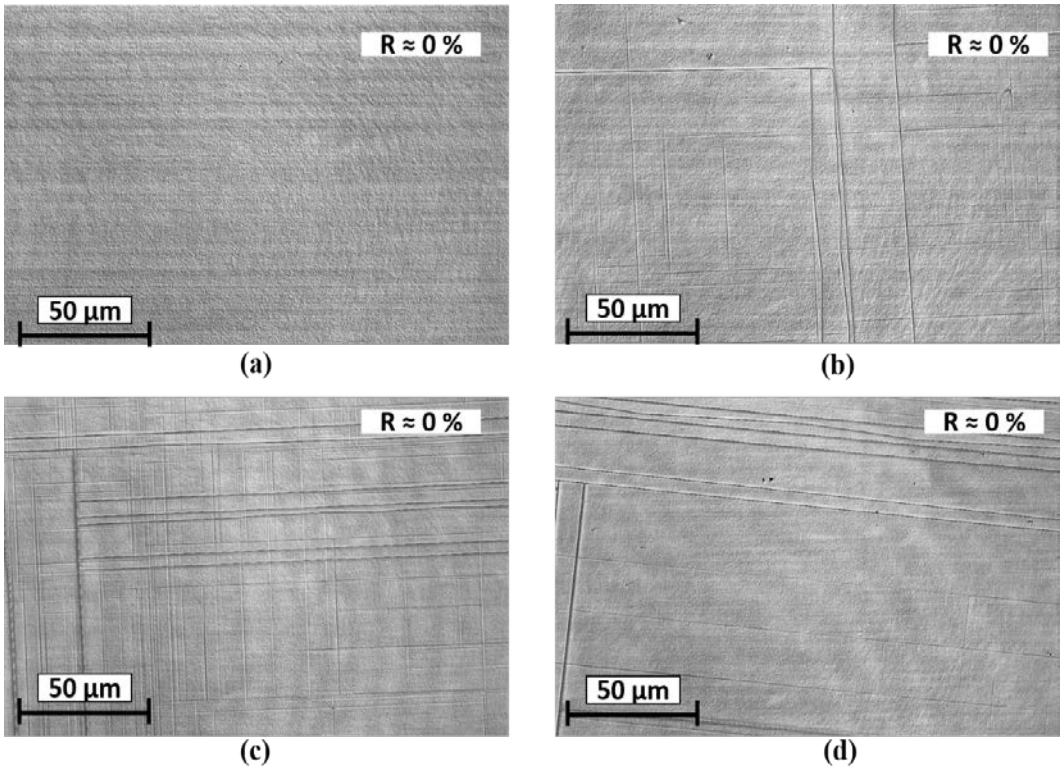

Figure 4.22: Laser microscopic images of the surface of SiGe layers grown on the Ge(100) substrate before annealing for the (a) 50nm thick $Si_{0.25}Ge_{0.75}$ layer, (b) 240nm thick $Si_{0.23}Ge_{0.77}$ layer, (c) 300nm thick $Si_{0.24}Ge_{0.76}$ layer & (d) 330nm thick $Si_{0.21}Ge_{0.79}$ layer.

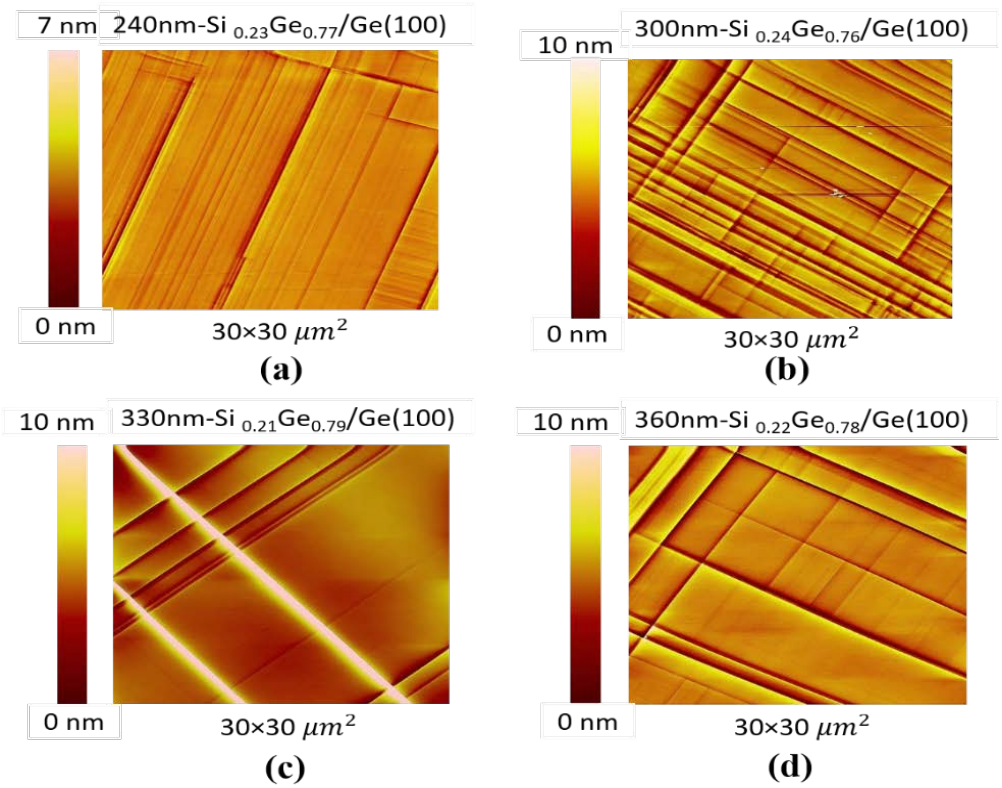

Figure 4.23: AFM images of the surface of SiGe layers grown on the Ge (100) substrate before annealing for the (a) 240nm thick $Si_{0.23}Ge_{0.77}$ layer, (b) 300nm thick $Si_{0.24}Ge_{0.76}$ layer, (c) 330nm thick $Si_{0.21}Ge_{0.79}$ layer & (d) 360nm thick $Si_{0.22}Ge_{0.78}$

Laser microscopic images are used to compare the ridges and trenches states of the 300nm thick $Si_{0.24}Ge_{0.76}$ layer grown on the Ge (100) substrate before and after annealing as shown in Fig. 4.24 (a) & (b) respectively. It is observe that additional dislocation-related trenches are created on the surface with thin-line trenches that are not observed before annealing, whereas ridges remain same as before annealing. These additional dislocation-related trenches are found to contribute to increase the strain relaxation of the SiGe layers It is observed that the density and depth of the additional dislocation-related trenches increase as the layer thickness as well as relaxation ratio increases.

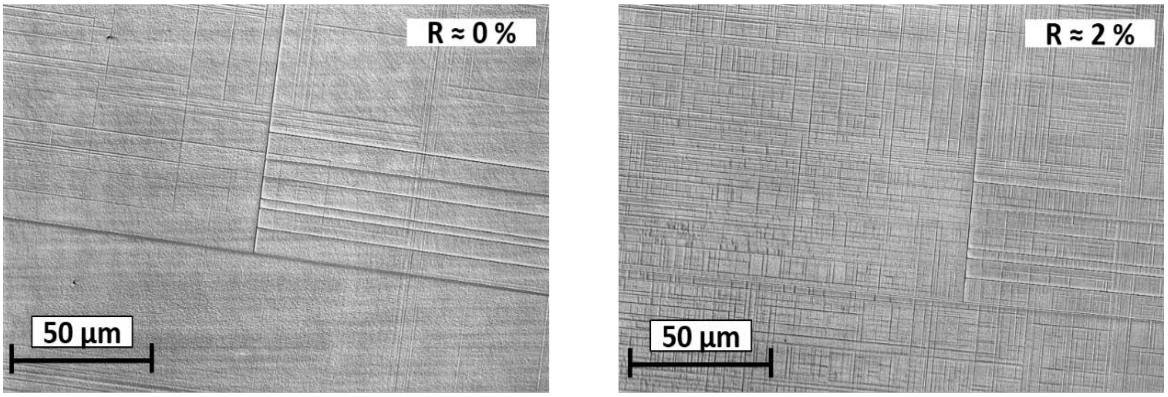

Figure 4.24: Laser microscopic images for 300 nm thick $Si_{0.24}Ge_{0.76}$/Ge(100) (a) before and (b) after annealing.

4.7 Critical thickness for strain relaxation of $Si_{1-x}Ge_x$ layer

The summarized results for this study are shown in Table 4.1. Figures 4.25 show summarize results of all SiGe samples fabricated in this study, i.e. various thickness $Si_{1-x}Ge_x$ layers on the Ge(111), Ge-on-Si(111) and Ge(100) substrates in the top, middle and bottom graphs, respectively. One plot corresponds to one sample in each graph, where x and y axes represent Ge concentrations in SiGe and the SiGe thickness, respectively. Red square plots represent samples which were partially relaxed after the growth. Green triangle plots represent samples which were fully strained after the growth but partially relaxed after annealing. Blue circle plots represent samples which were fully strained even after annealing. For these plots,

XRD results were used for judging whether the SiGe is fully strained or partially relaxed. In contrast, from observations of surface morphologies, filled plots are used for samples which exhibited very flat surface without any ridges after the growth while open plots correspond to samples where the surface ridges clearly appeared before annealing. Boundaries of blue and green plots represent equilibrium t_c curves while those of green and red do meta-stable t_c curves as shown with dashed lines. Also, we can write another curves (solid line) at boundaries of open and filled plots, which mean t_c for growth of ridge-free surfaces. It is clearly seen in those three graphs that t_c rapidly decreases with the decrease in Ge contents, that is, the increase in the tensile strain. This behavior is almost the same as reports on SiGe/Si(100) system and theoretically predictable. However, it is remarkable that the values of t_c depends strongly on the Ge substrates, which has not been reported in detail so far.

It is noticeable that t_c of $Si_{1-x}Ge_x$ layers on the Ge-on-Si(111) is much lower than that on the Ge(111) substrate especially Ge contents higher than 75%. For example, at the Ge content of 90 % t_c is 110 and 260 nm for $Si_{0.1}Ge_{0.9}$ layers on the Ge-on-Si(111) and Ge(111), respectively. This difference is presumably because threading dislocations in the Ge epilayer on Si work as sources for misfit dislocation nucleation and facilitate the strain relaxation of the $Si_{1-x}Ge_x$ layers on the Ge-on-Si(111) substrate. Additionally, the Ge layer grown on Si(111) has 0.2 % tensile strain due to difference of thermal expansion coefficients between Ge and Si [24]. This tensile strain in Ge-on-Si is added to the tensile strain of over-grown SiGe layers, leading to the higher probability of the dislocation nucleation and resultantly the lower t_c. By contrast, for Ge concentrations lower than 75%, t_c is equivalent between the Ge(111) and Ge-on-Si(111) substrates. For example, for $Si_{0.3}Ge_{0.7}$ layers both on the Ge-on-Si(111) and Ge(111), t_c determined by the ridge formation, which is slightly lower than equilibrium t_c determined by XRD, is about 35 nm. In this Ge content range, the above mentioned effects do not play roles for relaxation for both structures. In other words, the Ge-on-Si fabricated here has sufficiently high quality for the strained SiGe growth with several tens nm, which is thick enough for device channel formation. On the other hand, t_c of $Si_{1-x}Ge_x$ layers on Ge(100) is higher than that on Ge(111) substrates. This is presumably attributable to different dislocation generation mechanisms. For SiGe/Ge(111), the hetero-interface is (111) plane and can become the slip plane for dislocations. Therefore, nucleation of dislocations in SiGe/Ge(111) is much more likely than that in SiGe/Ge(100), resulting in the lower t_c for SiGe/Ge(111). It is also noticeable that the solid curves (t_c for ridge-free surface) are close to but do not correspond to equilibrium t_c (dashed lines). Since the strained SiGe with a ridged surface cannot be employed

for device channels, it can be said that acceptable conditions are below both the solid and dashed curves, which has been firstly indicated.

Table 4.1: Summarization of all results of $Si_{1-x}Ge_x$ grown on Ge(111), Ge-on-Si(111) and Ge(100) substrates.

Layer	Sample No.	Layer thickness (nm)	Ge concentration in SiGe (%)	$Si_{1-x}Ge_x$/Ge-on-Si(111)						$Si_{1-x}Ge_x$/Ge(111)						$Si_{1-x}Ge_x$/Ge(100)					
				Ridge of the surface	Average ridge height (nm)	Thickness fringes		Relaxation ratio (%)		Ridge of the surface	Average ridge height (nm)	Thickness fringes		Relaxation ratio (%)		Ridge of the surface	Average ridge height (nm)	Thickness fringes		Relaxation ratio (%)	
						Before annealing	After annealing	Before annealing	After annealing			Before annealing	After annealing	Before annealing	After annealing			Before annealing	After annealing	Before annealing	After annealing
$Si_{0.3}Ge_{0.7}$	18115	30	68.86	×		*	*			×		*	*	0		×		*			
	18062	40	70.98	*		*	*			×		*	*			×		*			
	18058	50	68.00	*		*	×			*		*	×			×		*			
	18061	70	67.75	*		*	×	6		*		*	×			*		*			
	18071	90	65.97	*		*		11		*		*	×			*		*			
	18057	100	68.49	*		×				*		*	×			*		*	*		
	18063	130	68.16							*		*				*		*	*		
	18064	150	67.93							*		×				*		*	×		
	18070	170	67.18													*		×			
$Si_{0.2}Ge_{0.8}$	18013	40	74.88	×		*	*			×		*				×		*			
	18018	50	75.86	×		*	*	0		×		*		0		×		*			
	18019	60	76.02	*	3.5	*	*	0		×		*				×		*			
	18033	70	76.26	*		*	×	0	9	*		*				×		*			
	18034	90	77.67	*	10.5	*		4		*	5	*	*			×		*			
	18090	110	75.99	*		*		1.2		*		*	*			*		*			
	18023	130	75.78	*	21	×		7		*	8.5	*	×	0	29	*	6.5	*		0	
	18024	140	75.49							*		*	×			*		*			
	18048	160	76.42							*		*				*		*			
	18051	180	76.25							*	11	×		3		*		*			
	18094	200	77.86							*	15	×				*	8.5	*	*		
	18098	240	76.99													*		*	*		
	18106	300	76.23													*		*	×	0	1.3
	18113	330	79.03													*	25	*			
	18117	360	77.57													*		×		1.3	
$Si_{0.1}Ge_{0.9}$	18079	50	88.50	×		*				×		*				×		*			
	18075	70	88.34																		
	18066	90	88.04	×		*	*			×		*				×		*			
	18067	110	88.44	×		*	×			×		*				×		*			
	18076	130	88.76	×		*		-3		×		*				×		*			
	18083	150	86.12	*		*		0		×		*				×		*			
	18089	170	87.95	*		×		5		×		*				×		*			
	18078	200	88.81							×		*	*			×		*			
	18081	230	88.02							×		*	*			×		*			
	18088	260	89.66							×		*	×			×		*			
	18091	300	88.64							×		*				×		*	*		
	18097	330	87.82							*		*				×		*	*		
	18099	350	87.18							*		×				×		*	*		
	18114	400	89.48													×		*	×		
	18116	450	87.86													*		*	×		
	18157	550	89.70													*		×		3	

* Appeared
× Disappeared

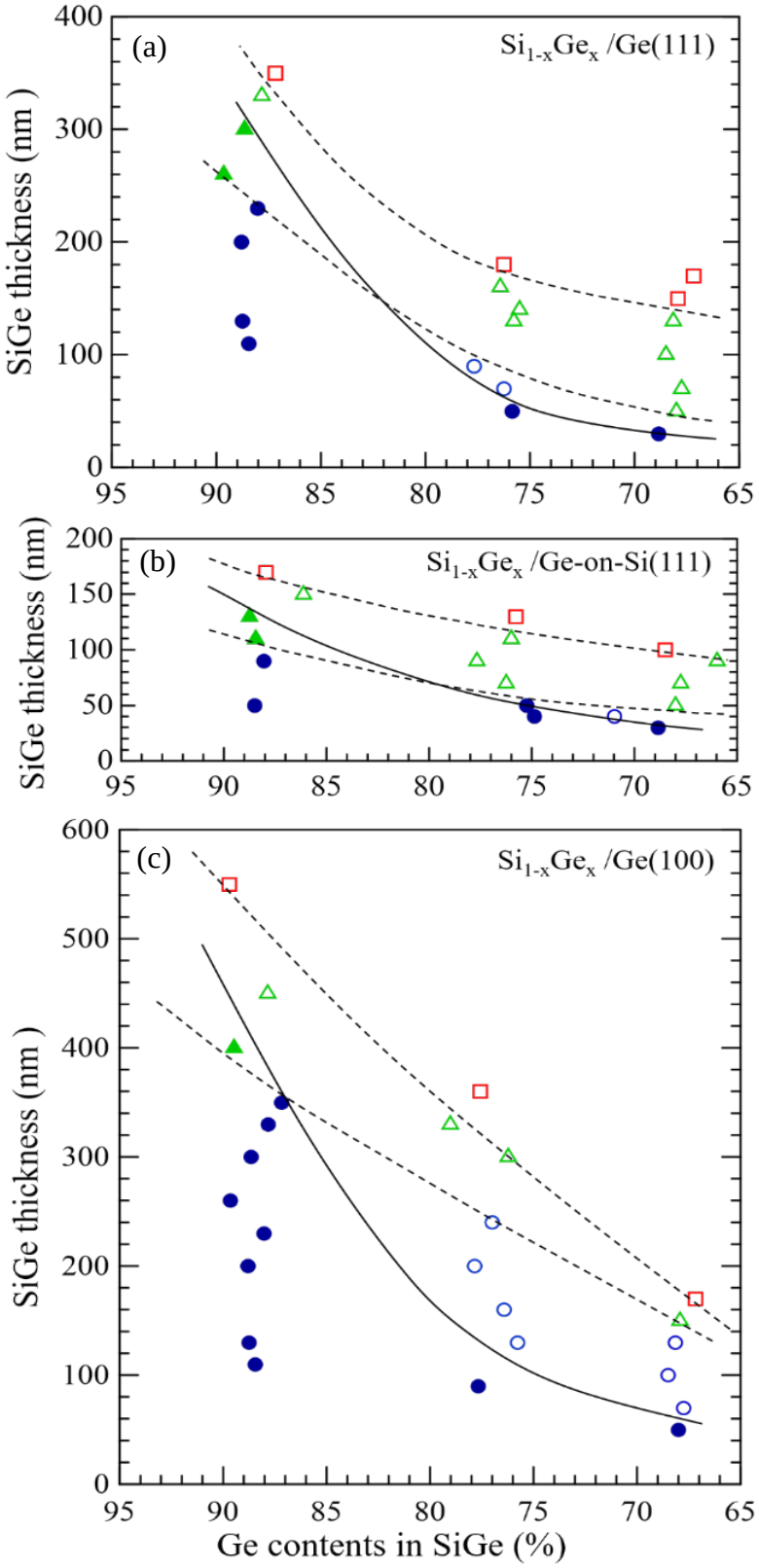

Figure 4.25: Summary of results of all SiGe samples in graphs of SiGe thickness vs Ge concentrations in SiGe for (a) SiGe/Ge(111), (b) SiGe/Ge-on-Si(111) and (c) SiGe/Ge(100) substrates. See the text for each plot and curve.

4.8 Comparison of critical thickness

The experimental critical thickness (t_c) for strain relaxation of the strained $Si_{1-x}Ge_x$ layers grown on the Ge(111), Ge-on-Si(111) and Ge(100) substrates (solid lines in Fig. 4.25) compared with the critical thickness of strained $Si_{1-x}Ge_x$/Si(100) (Van der Merwe et. al.[33], J. W. Matthews et. al.[34], R. People et. al.[36, 37]) and strained Si/ $Si_{1-x}Ge_x$(100) (S. B. Samavedam et. al.[86]) as shown in figure 4.26. J. W. Matthews et. al. calculated the critical thickness by using mechanical equilibrium whereas R. People et. al. obtained the critical thickness by assuming interfacial misfit dislocation. It is observe that critical thickness of the strained $Si_{1-x}Ge_x$/Ge(100) has good agreement with R. People et. al. results (Fig. 4.26). On the other hand, critical thickness of the strained $Si_{1-x}Ge_x$/Ge(111) and $Si_{1-x}Ge_x$/Ge-on-Si(111) are lower than that of R. People et. al. results due to the different dislocation generation mechanism for (111) plane orientation.

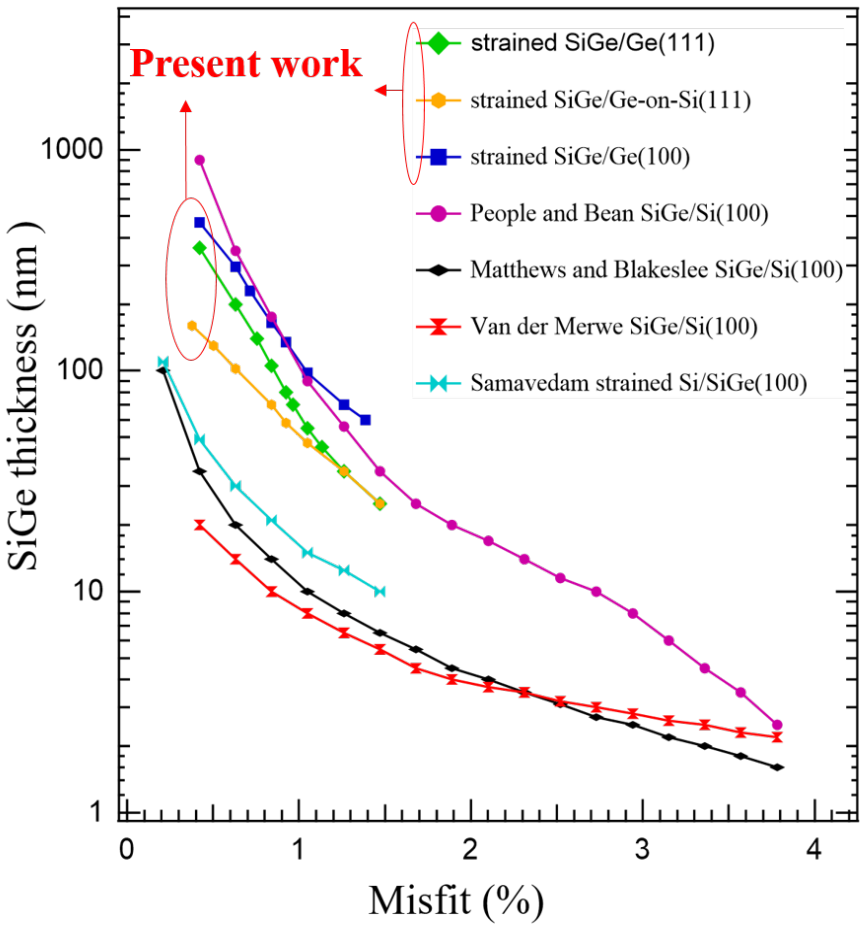

Figure 4.26: The critical thickness of strained $Si_{1-x}Ge_x$ layers fabricated on various substrates as a function of misfit between the layer and substrate.

4.8 Summary

In summary, experimental critical thickness (t_c) of the strained $Si_{1-x}Ge_x$ layers grown on the Ge-on-Si(111) and Ge(111) substrates were studied. To determine t_c, initial stages of strain relaxation of the $Si_{1-x}Ge_x$ layers were investigated in detail, where strain states together with surface morphologies were systematically evaluated by x-ray diffraction (XRD), micro-Raman, laser microscope and atomic force microscope. As a result, experimental t_c curves as a function of Ge concentrations have been firstly obtained both from XRD measured relaxation ratios and the surface morphology. It was found that t_c of $Si_{1-x}Ge_x$/Ge-on-Si(111) is much lower than that of $Si_{1-x}Ge_x$/Ge(111) for the lower Ge concentrations in SiGe while t_c becomes equivalent for the higher Ge concentrations. For example, t_c is 35 nm for $Si_{0.3}Ge_{0.7}$ layers both on Ge(111) and Ge-on-Si(111) substrates. This different behavior of t_c is thought to come from different dislocation nucleation probabilities and related surface ridge formation. We can say that the highly substrate-dependent t_c found in this comparative study has to be considered carefully for applications of strained Si/Ge heterostructures on Ge-on-Si to various devices.

5

Compressive strained Ge channel fabricated on Si (111)

5.1 Introduction

Germanium (Ge) has attracted extensive interests as a promising channel material for next generation CMOS circuits due to high intrinsic mobilities of both holes and electrons and compatibility with conventional CMOS processes, with higher performances and lower power consumption. Ge with a surface orientation of (111) is attractive due to its higher electron mobility for n-type channel MOS applications [25] and applicability to spintronic devices via lattice-matched epitaxial growth of high-quality ferromagnetic materials [27, 87]. Introduction of the lattice strain can significantly increase the mobility in Ge channels [20, 88] because of reduction in effective mass and the band/valley splitting [89]. It has been experimentally demonstrated that the hole mobility increases with increasing compressive strain up to ~ 2% for the strained Ge(100) channels formed on SiGe(100) virtual substrates [13]. Similarly for the Ge(111) channel, hole mobility improvement by the compressive strain has been predicted by numerical simulations [90]. It has also been reported that valley degeneracy splitting by the strain or quantum confinement can largely increase the spin lifetime [91]. Hence, the Ge(111) thin channel layer with strain is appropriate for spintronic devices with long spin lifetime. However, to date, there are still few reports on fabrication and characterization of detailed structural properties of compressively strained Ge(111) thin layers [92]. It is the great challenge to grow a smooth and high quality strained Ge channel layer on the strained relaxed $Si_{1-x}Ge_x$ buffer layer on a Si(111) substrate due to the generation of threading dislocations and stacking faults. The compositionally graded buffer layer is one of the most common methods to gradually reduce the misfit strain and to largely reduce the threading dislocations [93, 94]. Moreover, this method is not suitable for SiGe(111) particularly with high Ge concentrations because it has been shown that very slow grading rates (e.g. 1% Ge/μm) are mandatory in order to obtain high quality SiGe(111) graded buffer layer [95]. As a result, thickness of the graded buffer layer significantly increases, which is not favorable for practical device applications from viewpoints of low thermal conductivity of SiGe, huge time and material consumptions. Also, high electrical conductivity of SiGe buffers leads to parallel conduction and off-leak current. On the other hand, a high quality Ge can be grown directly on a Si (Ge-

on-Si) by two–step growth method. Based on the Ge-on-Si, the reverse graded buffer method has been proposed and high Ge composition $Si_{1-x}Ge_x$ /Si(100) with low threading dislocation density (TDD) of $4.2 \times 10^6 cm^{-2}$ and a high degree of relaxation of 107.3% was reported [70].

In this chapter, an investigation of compositionally reverse graded buffer layer fabrication on Si(111) substrate with a high structural quality and high quality strained Ge channel on the buffer and a comparative sample was grown simultaneously on a Si(100) substrate are presented . Still there are few reports on the fabrication and detailed structural properties of strained Ge(111) thin layer. In addition, since large amounts of holes are generated in the buffer layer due to the presence of dislocations and defects, the suppression of parallel conduction is issue of critical importance. For this purpose, insertion of phosphorus (P)-doped thin layer in the buffer layer and observation of the P diffusion behavior are also reported in this chapter. Finally, electrical properties of compressively strained Ge(111) thin layer grown on reverse graded buffer are presented.

5.2 Base layer for strained Ge channel

The growth parameters, strain states, relaxation and surface roughness of the base Ge layer fabricated on Si(111) and Si (100) are reported in this section.

5.2.1 Structure and growth parameters of the base Ge layer

Two-step growth method of the base Ge layer fabricated on a Si(111) substrate by using MBE already have been described in section 4.2. The low temperature (LT) Ge seed layer generate a high density of dislocations to reduce the lattice mismatch and formed relaxed thin Ge layer. The high temperature (HT) layer reduce the surface roughness by annihilating threading dislocation glide to the buffer surface. A post anneal is responsible to reduce the threading dislocation density (TDD). For fabricating the Ge(111) base layer on which reverse graded buffer layer was grown, first, a 40 nm thick LT-Ge layer was grown at 400°C and followed by the growth of a 800 nm thick HT-Ge layer was grown at 800°C and then annealed at 800°C for 10 min in same vacuum condition in order to reduce the threading dislocation density in the Ge film. The different growth parameters was used to fabricate the Ge(100) base layer, a 40 nm thick LT-Ge layer was grown at 400°C and a 800 nm thick HT-Ge layer was

grown at 600°C and then annealed at 800°C for 10 min in same vacuum condition. The structure of the base Ge layer as shown in figure 5.1.

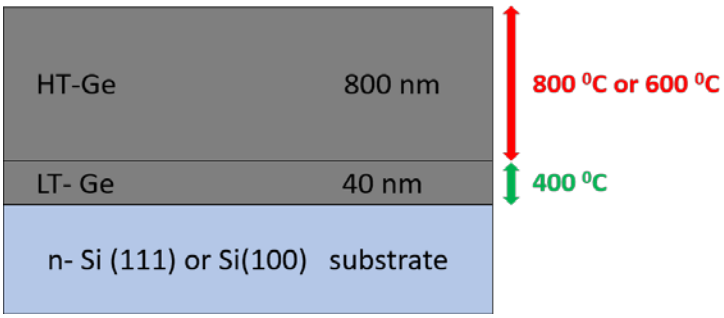

Figure 5.1: Structure of the base Ge layer on a Si(111) or Si(100) substrates for fabricating reverse graded buffer layers on it.

5.2.2 Structural characterization of the base Ge layer

The strain states of HT-Ge layers grown on Si substrates were characterized by Raman spectroscopy as shown in Fig.5.2. Amounts of in-plain strain of the Ge epilayers were derived by using a following equation $\omega = 300.5 - 400\varepsilon_{11}$ where ω is a Raman shift wavenumber of the Ge-Ge mode and ε_{11} is the in-plain strain. As seen in Fig.5.2, peaks of the HT-Ge epilayers are redshifted compared to a bulk Ge peak, meaning that the HT-Ge epilayers have the tensile strain. Obtained amounts of the tensile strains are 0.28 and 0.20% for the HT-Ge grown on the Si(111) and Si(100) substrates, respectively. The larger tensile strain in Ge(111) than Ge(100) is interpreted as follows. The tensile strain in Ge epilayers originates from the difference of thermal expansion co-efficient between Ge and Si. During the cooling of the Ge epilayers, which are grown on the Si at high temperatures and almost fully strain-relaxed, thermal shrinkage of the Ge is suppressed by the underneath Si substrate with the lower thermal expansion coefficient. It should be noted that if the strain relaxation of the Ge is not sufficient, the induced tensile strain decreases. Although the post-growth annealing temperature is the same (800°C) for both Ge epilayers on Si(100) and Si(111), the discrepancy of growth temperatures between the two is considered to lead to a slight difference in the strain relaxation of the HT-Ge. As a result, the induced tensile strain of the HT-Ge fabricated on the Si(111) is slightly higher than that on the Si(100). However, the relaxation of the HT-Ge grown on the Si(111) and Si(100) substrates was evaluated using Raman spectroscopic data to be 107% and 105% respectively.

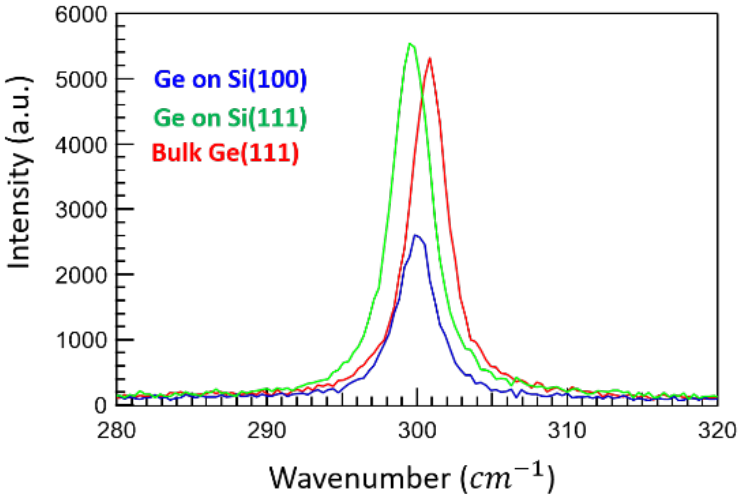

Figure 5.2: Raman spectra for the Ge epilayer grown on Si (111) and Si (100).

Reciprocal space mapping (RSM) image around the asymmetrical (153) reciprocal space point was used to examine the relaxation ratio of base Ge layer grown on the Si(111) substrate and the evaluated value is 105%. On the other hand, similar observation along asymmetrical (224) orientation for the base Ge layer grown on the Si(100) substrate was performed and evaluated the relaxation ratio is104%.

5.2.3 Surface roughness of the base Ge layer

The base Ge layer surface morphology was observed by performing AFM measurements in $10 \times 10\ \mu m^2$ area for the Ge layers formed on the Si(100) and Si(111) substrates as shown in Figs. 5.3 (a) and (b), respectively. The RMS roughness of the base Ge layer fabricated on Si(100) is 0.44 nm despite of the 4% lattice mismatch between Ge and Si, indicating that the low temperature Ge nucleation aids in maintaining a smooth, two-dimensional (2-D) surface reconstruction throughout the growth. On the other hand, the RMS rough of the base layer grown on Si(111) is 3.6 nm. Since dislocation density is strongly related to the surface, it is speculated that dislocation nucleation and gliding are higher in the base layer grown on Si(111) substrate resulting the higher surface roughness. If roughness of the base Ge layer is higher, a thicker buffer layer is required to suppress the dislocation nucleation within the buffer layer grown on the base Ge layer.

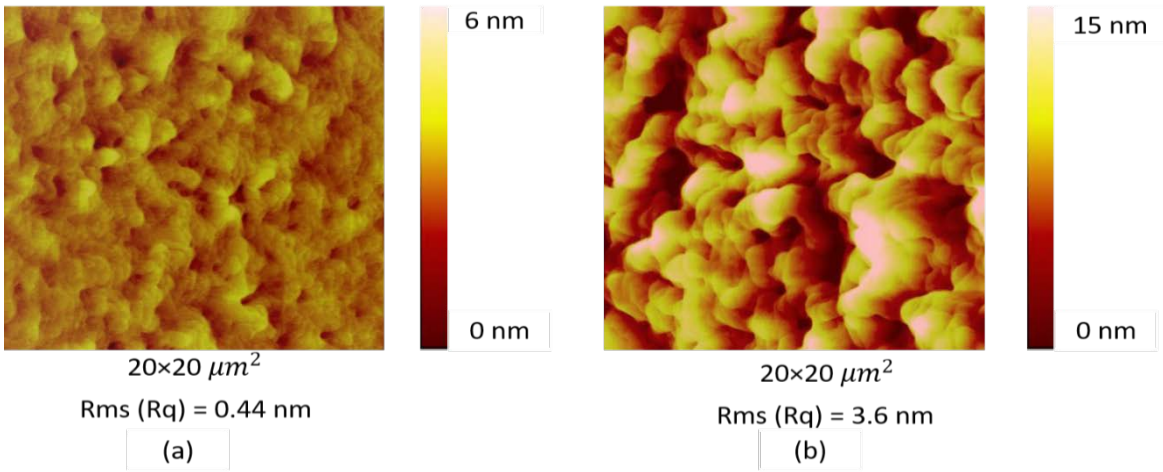

Figure.5.3: AFM image of th base Ge layer fabricated on (a) Si(100) substrate and (b) Si(111) substrate.

5.3 Structure and fabrication parameters for strained Ge channel

In the section, the strained Ge channel fabrication process using base Ge layer are presented. A compressive strained Ge channel was fabricated on Si(111) substrate and a comparative sample was grown simultaneously on a Si(100) substrate. For fabrication relaxed buffer layer, reverse grade technique is used.

5.3.1 Reverse graded buffer layer for strained Ge channel

Reverse graded SiGe buffer layer formed by grading the Ge composition from higher to desired lower values. The novel idea of reverse graded thin SiGe buffer on Si(100) substrate has been introduced by Lui et al. [98] and linearly reverse graded thin SiGe buffer on Si(100) substrate with low threading dislocation density has been reported by V. A. Shah et al. [70, 99]. However, for fabricating high-quality strained Ge channel, a relaxed SiGe buffer layer is necessary. A high-quality buffer layer directly deposition on a Si substrate would be subject to strain based surface segregation due to the growth kinetics and large misfit dislocation. Additionally dislocation density increases when the layer thickness over than the critical thickness due to homogeneous and heterogeneous nucleation. Ge epilayer on Si substrate used to reduce the surface segregation due to low mismatch between the Ge epilayer and the Ge-rich SiGe buffer reported by Huang L. et al.[48] The buffer layer presented here, starting with a base Ge layer on Si substrate and then fabricate SiGe layer with reverse grade down to a

composition of $Si_{0.26}Ge_{0.74}$. The initiative behind this process is to fabricate Ge-rich graded buffer layer on the Si(111) or Si(100) substrates.

5.3.2 Fabrication parameters for strained Ge channel

The strained Ge channel was fabricated on a Si(111) substrate by using solid-source molecular beam epitaxy (MBE) and a comparative sample was grown simultaneously on a Si(100) substrate as shown in Fig.-5.4. A reverse graded relaxed SiGe buffer layer was grown on the base Ge epilayer at 500°C with grading Ge compositions from 100% to 74%. After that, 20 nm thick P-doped layer was grown at 500°C to suppress the parallel conduction and then 50 nm thick spacer, the 20 nm thick Ge channel layer, 10 nm thick spacer and a cap layers were successively grown at 300°C.

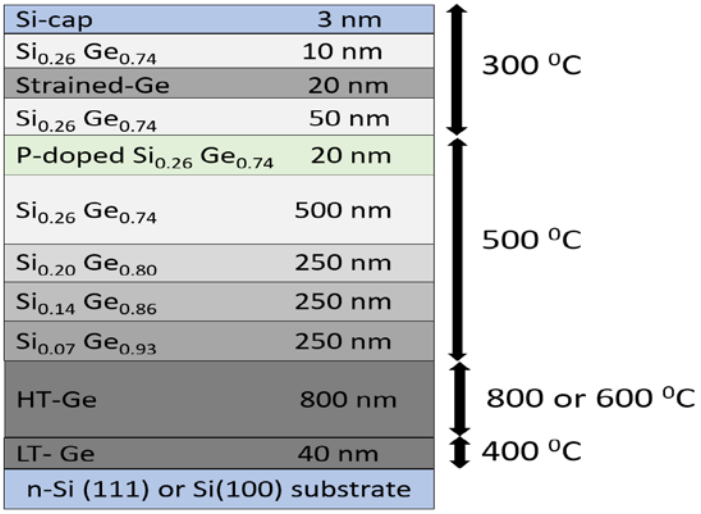

Figure 5.4: Strained Ge/$Si_{0.26}$ $Ge_{0.74}$ /Ge on Si(111) or Si(100) structures with P-doped layer.

5.4 Structural properties of strained Ge channel

An investigation of the structural properties of compressive strained Ge channels fabricated on Si (111) and Si (100) are presented in this section. The relaxation of the buffer layer, composition of the buffer layer, strain states of the strained Ge channel layer, top surface roughness, phosphorous dopant diffusion and thermal stability of strained Ge channel are investigated.

5.4.1 Relaxation of buffer layer

X-ray diffraction (XRD) measurements were performed to examine relaxation ratios and Ge compositions of the buffer layers. Figure 5.5(a) shows a reciprocal space mapping (RSM) image around the asymmetrical (153) reciprocal space point for the strained Ge/SiGe/Ge on Si(111). The relaxation of the constant composition $Si_{0.26}Ge_{0.74}$ layer was evaluated compared to the Si(111) substrate to be 107%. Figure 5.5(b) shows the similar observation along asymmetrical (224) orientation for the strained Ge/SiGe/Ge on Si(100), where the relaxation of $Si_{0.26}Ge_{0.74}$ buffer layer compared to the Si(100) substrate is 112%, indicating both $Si_{0.26}Ge_{0.74}$ buffer layers are slightly tensile-strained. The relaxation ratios of $Si_{0.26}Ge_{0.74}$ buffer layers compared to Ge(111) and Ge(100) epilayers are evaluated to be 86% and 74% and those compared to unstrained Ge(111) and Ge(100) to be 83% and 70% respectively. Though the $Si_{0.26}Ge_{0.74}$ buffer layers fabricated on (111) and (100) simultaneously under the same growth conditions, the relaxation of the buffer layer on the Ge(100) is lower that on the Ge(111). It is speculated that formation of 60^0 dislocations is responsible for lower relaxation i.e slightly higher residual tensile strain of the $Si_{0.26}Ge_{0.74}$ (100) buffer layer.

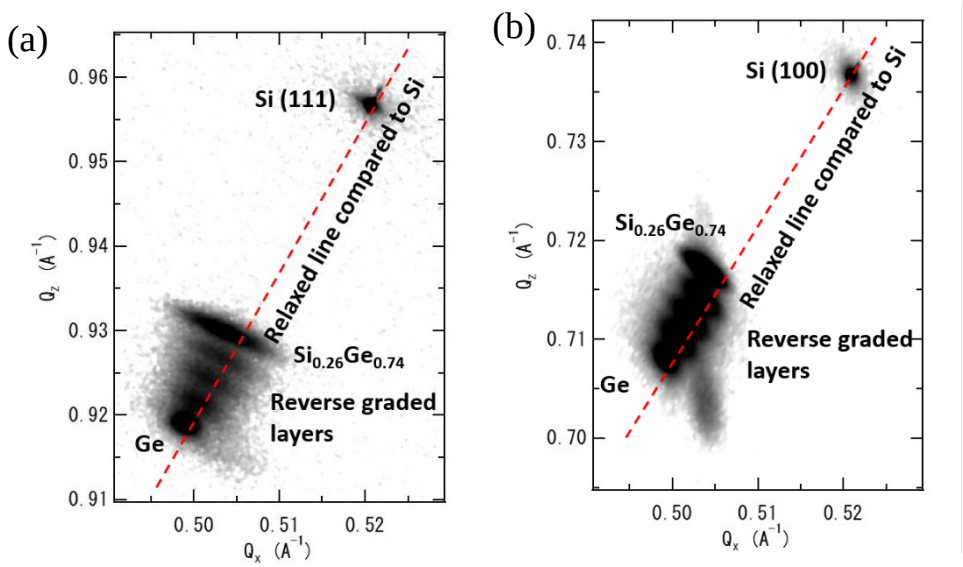

Fig.5.5 XRD for (a) asymetric (153) RSM of strained Ge fabricated on Si(111) and (b) asymetric (224) RSM of strained Ge fabricated on Si(100).

It is also clear from (224) and (153) RSM images that Ge layers also have slight tensile strain and the relaxation ration was evaluated to be 104.5% and 105% compared to Si (100) and Si(111) substrates respectively. By the contrast, the relaxation ratio of the Ge-on-Si(100)

and Ge-on-Si(111) was 104% and 105% respectively before buffer layer grown on these Ge epilayers. The relaxation ratio of the Ge-on-Si(100) slightly changed when the buffer layer grown on it. It can be speculated that during the longtime growth of reverse graded buffer layer on Ge epilayer, additional dislocation nucleation occurred in Ge/Si(100) interface due to the growth temperature difference between the Ge epilayer(600°C)and the buffer (500°C). Therefore, the relaxation ratio of the Ge-on-Si(100) slightly increased after buffer layer grown on it. On the other hand, the dislocation nucleation is saturated due to the high growth temperature (800°C) of the Ge epilayer on Si(111) substrate. That is why, the relaxation of the Ge-on-Si(111) remains same even buffer layer grown on it.

5.4.2 Strain states of strained Ge channel

Raman spectra were used to investigate strain states of the strained Ge channels grown on (111) and (100) are shown in Fig. 5.6. Peaks are observed around 292 cm^{-1} and 302 cm^{-1} corresponding to the Ge-Ge phonon modes originated from the SiGe buffer layer and the strained Ge channel layer grown on Si(100), whereas, peaks are observed around 293 cm^{-1} and 303 cm^{-1} corresponding to the Ge-Ge phonon modes originated from the SiGe buffer layer and the strained Ge channel layer grown on Si (111). It is clearly observed that the peak wavenumber for the Ge channel grown on the Si (111) is higher than the one on Si (100), indicating that the Ge channel on Si (111) is more compressively strained than Si (100). The compressive strains were calculated to be -0.92% and -0.58% for the Ge channel grown on Si (111) and Si (100) respectively. Since the relaxation of $Si_{0.26}Ge_{0.74}$(100) compared to the Si substrate is higher than $Si_{0.26}Ge_{0.74}$ (111), the in-plane lattice constant of $Si_{0.26}Ge_{0.74}$(100) is larger than $Si_{0.26}Ge_{0.74}$(111), which is the reason for the larger compressive strain of Ge on $Si_{0.26}$ $Ge_{0.74}$(111) than strained Ge on $Si_{0.26}$ $Ge_{0.74}$(100).

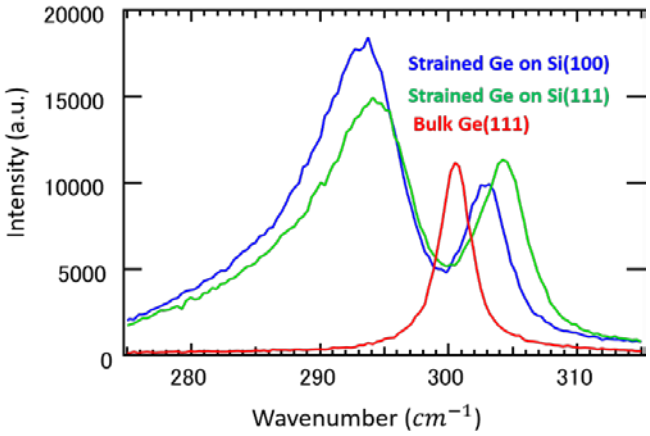

Fig.5.6 Raman spectra for the strained Ge channels grown on SiGe buffer layers on Si(111) and (100).

5.4.3 Thermal stability of strained Ge channel

The thermal stability of the strained Ge channels are observed after annealing the samples for one minute at various temperatures by using RTA. The compressive strains were evaluated from Raman spectra and plotted against temperatures as shown in Fig.5.7. The compressive strain of the channel decreases with increase annealing temperature. It was observed that after annealing at 800°C the strain of the channel layer became zero. The Ge atoms in underneath SiGe layer are diffused to the interface of the channel layer due to the high anneal temperature. For this reason, strain of the channel decreases with increase annealing temperature and for specific high temperature the strain become zero.

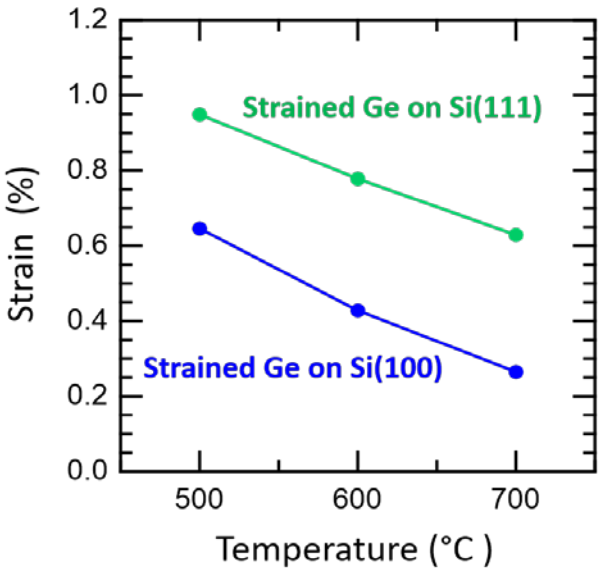

Figure 5.7: Temperature dependence compressive strain calculated from Raman spectra.

5.4.4 Surface roughness of strained Ge channel

Surface roughness can play a key role in device applications due to the surface scattering-induce mobility degradation. AFM measurements in $10 \times 10\ \mu m^2$ area were performed for the strained Ge samples formed on the Si(100) and Si(111) substrates as shown in Figs. 5.8 (a) and (b), respectively. A so-called cross-hatch pattern clearly appears for the strained Ge(100) sample, whereas no such pattern is found for the strained Ge(111) sample. This is presumably attributed to different dislocation generation mechanisms in both reverse-graded SiGe buffer layers and Ge-on-Si between (100) and (111). For (100), intersections of (100) surface and (111) slip planes create [110] directional orthogonal misfit dislocations,

leading to the cross-hatch surface. By contrast, for (111), intersections of (111) surface and (111) equivalent slip planes are expected to create triangle shape. However no such morphology is clearly seen in Fig. 5.8 (b) presumably due to short distance gliding of dislocations. Additionally, generation of stacking faults can be another reason. Obtained RMS roughness is 0.34 nm and 1.7 nm for the strained Ge (100) and Ge (111), respectively. It should be noted that the both samples show very flat surface below 2 nm without CMP compared to conventional graded buffers whose roughness usually exceed several tens of nm [65, 96]. In general, the surface roughness becomes larger for the higher growth temperature due to enhanced surface migration. The difference in amplitudes of the roughness between the strained Ge(100) and (111) is considered to come from the different growth temperatures of the Ge-on-Si.

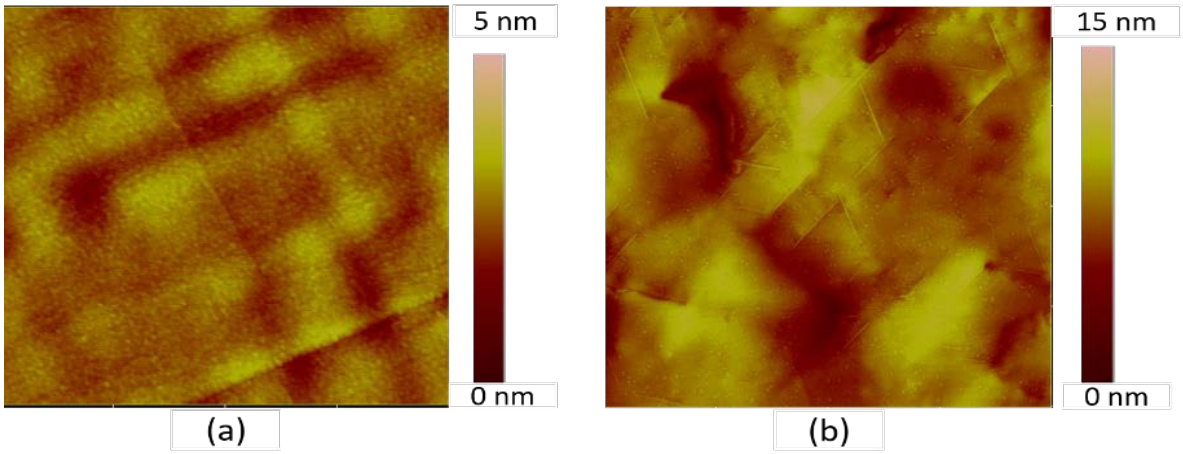

Figure.5.8: Top surface AFM image of strained Ge fabricated on (a) Si(100) substrate and (b) Si(111) substrate.

5.4.5 Doped layer profile

Since we know that a large number of holes are generated in the SiGe buffer layer due to the presence of dislocations and defects, it is necessary to suppress the parallel conduction in the buffer layer. Phosphorous (P) doped thin layer is inserted in the buffer layer due to the suppression of parallel conduction through buffer layer [97]. The thickness of the phosphorous doping layer and strained Ge channel layer grown on (100) were measured to be 13.75nm and 15.1nm respectively from SIMS profile as shown in fig.5.9 (a). The average phosphorous concentration in this doping layer is $1.31 \times 10^{20} \mathrm{cm}^{-3}$ and clearly seen that P-doped layers effectively isolate from the Ge channel. Figure 5.9 (b) shows the SIMS profile for strained Ge

grown on (111) where the thickness of the doping and channel layers are calculated to be11.87nm and 14.95nm respectively and the average doping concentration of $1.64 \times 10^{20} cm^{-3}$.

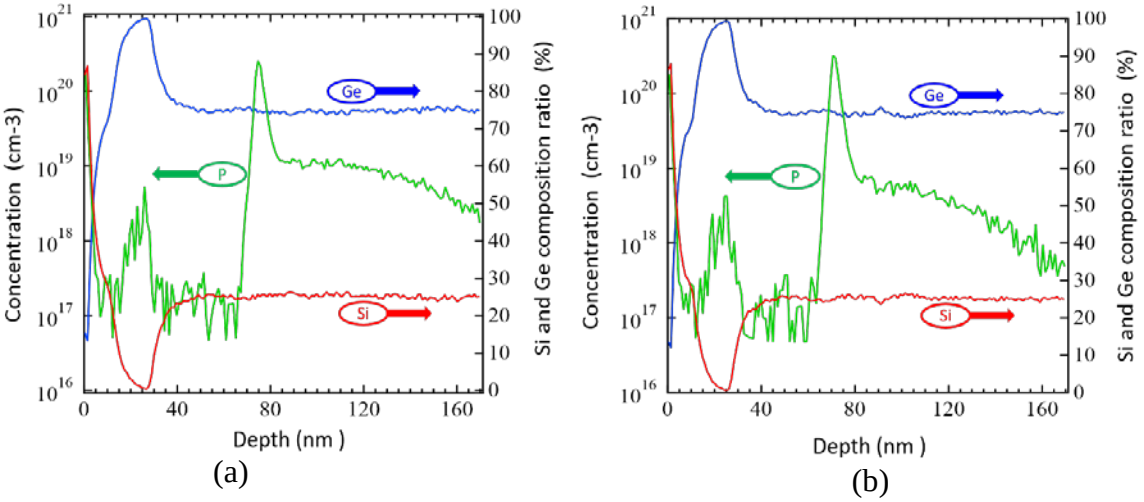

Figure 5.9: **(a)** Si, Ge and P SIMS profiles for the strained Ge on Si(100) substrate. **(b)** Si, Ge and P SIMS profiles for the strained Ge on Si(111) substrate.

It is clearly observed that the P concentration peak on (111) is higher than the peak on (100) and the tail of the peak on (100) is much broader towards the substrate than the peak on(111) as shown in fig.6 (c). On the other hand, peak tail towards the channel is very short indicates that diffusion of P atoms to the channel is suppressed due to the low growth temperature. The presence of dopant atoms in the channel on (111) is negligible than (100) also confirmed the purity of the channel on (111).

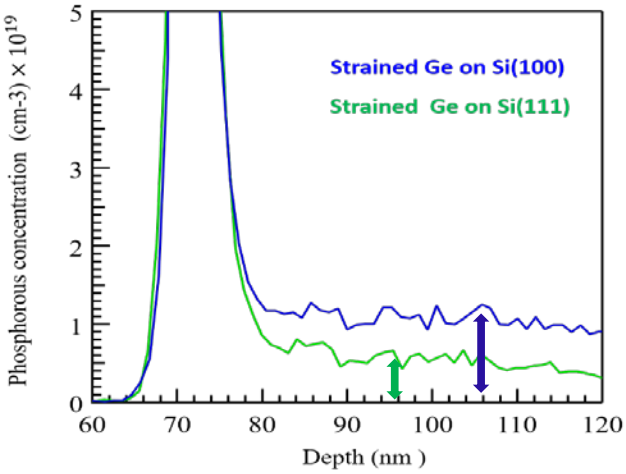

Figure 5.10: Phosphorous SIMS profile for the strained Ge on Si(100) & Si(111) substrate.

5.5 Surface channel strained Ge MOS

In this section, an investigation of the surface channel strained Ge fabricated on a Si(111) substrate is reported. For fabrication of the $Si_{0.67}Ge_{0.33}$ (111) buffer layer, low temperature buffer technique is used.

5.5.1 SiGe buffer layer

The low-temperature buffer method (LT buffer) is a method that can suppress both the roughness and threading dislocation density with a thin film rather than the graded compositional method [100, 101]. The point defects are formed in the LT-Si layer and promotes relaxation to the SiGe layer by confining the dislocation in the LT-Si layer. Low temperature buffering has already been applied to device structures and high mobility has been obtained and strained Ge channel modulation doped structures [102, 103].

For this investigation, a $Si_{0.67}Ge_{0.33}$ (111) buffer layer was fabricated by using low temperature buffer method to obtain the benefit of this method for (111) orientations. In this study, a LT-layer was used before each different composition layer deposit one each other. As a result, it can be expected that dislocation is confined in each LT layer.

5.5.2 Structure and growth parameters for the surface channel strained Ge

The surface channel strained Ge MOS sample was grown on a Si(111) substrate by using MBE as shown in Fig. 5.11. First, an 840 nm thick Ge base layer was formed on a Si(111) substrate with two-step growth method, where a thin Ge layer was grown on a Si substrate at relatively low temperatures and followed by the growth of a thick Ge layer at higher temperatures and then annealed at 800 °C for 10 min in ultra-high vacuum in order to reduce threading dislocation density in the Ge film. After that, the SiGe strain-relaxed buffer layers with Ge composition from 70% to 40% and a 60 nm thick P-doped layer were grown successively at various temperatures. A 20nm thick channel layer was grown on the $Si_{0.67}Ge_{0.33}$ (111) buffer layer at 300°C. Finally, an Al_2O_3 film with the thickness of 10 nm was directly deposited on the strained Ge channel by using ALD.

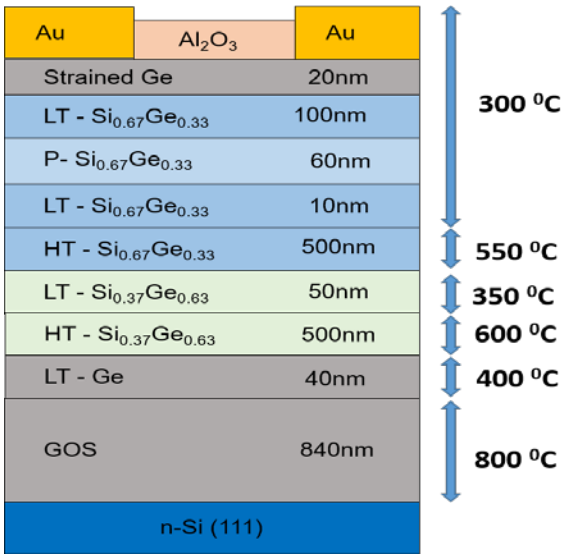

Figure 5.11: Surface channel strained Ge/$Si_{0.67}Ge_{0.33}$ /Ge on Si(111) structures with P-doped layer.

5.5.3 Relaxation of SiGe buffer layer

X-ray diffraction (XRD) measurements were performed to examine relaxation ratios and Ge compositions of the buffer layers. Figure 5.12 shows a reciprocal space mapping (RSM) image around the asymmetrical (153) reciprocal space point for the strained Ge/SiGe/Ge on Si(111). The relaxation ratios of the $Si_{0.37}Ge_{0.63}$ and $Si_{0.67}Ge_{0.33}$ layers were evaluated compared to the Si(111) substrate to be 111% and 128% respectively, indicating both $Si_{0.26}Ge_{0.74}$ layers are slightly tensile-strained. The relaxation ratios of the $Si_{0.37}Ge_{0.63}$ and $Si_{0.67}Ge_{0.33}$ layers compared to Ge(111) epilayers are evaluated to be 87% and 83% . It is speculated that formation of 60^0 dislocations is responsible for slightly higher residual tensile strain of the buffer layer.

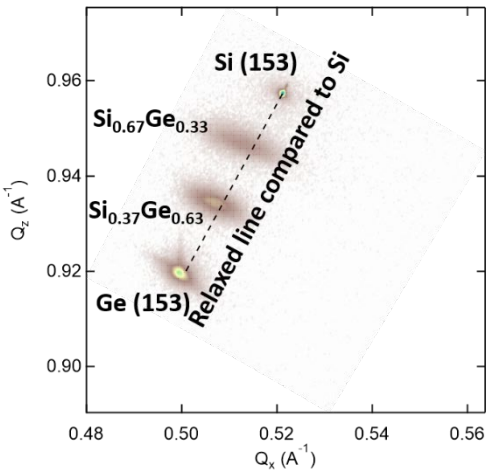

Fig.5.12: XRD for asymetric (153) RSM of strained Ge fabricated on Si(111) .

5.5.4 Hole mobility of surface channel strained Ge MOS

A high quality buffer layer with low surface roughness is an important issue for a high-quality channel as well as high hole mobility of the channel. During the growth of the buffer layer, a large number of holes are generated unintentionally in the buffer layer due to some defects in the buffer layer. Therefore, phosphorous (P) doped layer is necessary to suppress the parallel conduction through the buffer layer. Figure 5.13 shows the temperature dependence of the hole mobility and hole sheet density for a strained Ge channel grown on the Si(111) with the P-doped layer. It can be speculated that the holes are confined in the strained Ge surface channel grown on the SiGe (111) buffer layer and a high hole mobility of 1650 cm^2/Vs is obtained at room temperature (300K). Figure 5.14 shows the SiGe buffer layer mobilities (green line) and hole sheet density as a function of temperature with the channel layer mobilities (blue line) and hole sheet density. It is observe that below 150K, there is no mobility for SiGe buffer layer because of at low temperature the carriers of the buffer layer are frizzed and can't move. On the other hand, confined hole in the channel contribute to obtain the mobility even at low temperature reveal that two-dimensional hole gas (2DHG) is formed in the channel. The enhancement of the hole mobility is also indicating effective suppression of parallel conduction through the SiGe buffer layers by the P-doped isolation layer. Without the Al_2O_3 film top on the channel, holes are not confined in the channel, resulting in no 2DHG behavior. This indicates that the Al_2O_3 film on the strained Ge channel can effectively confine holes in the channel. And as a result, very high hole mobility is obtained, indicating that the Al_2O_3/Ge interface-related scattering is sufficiently low.

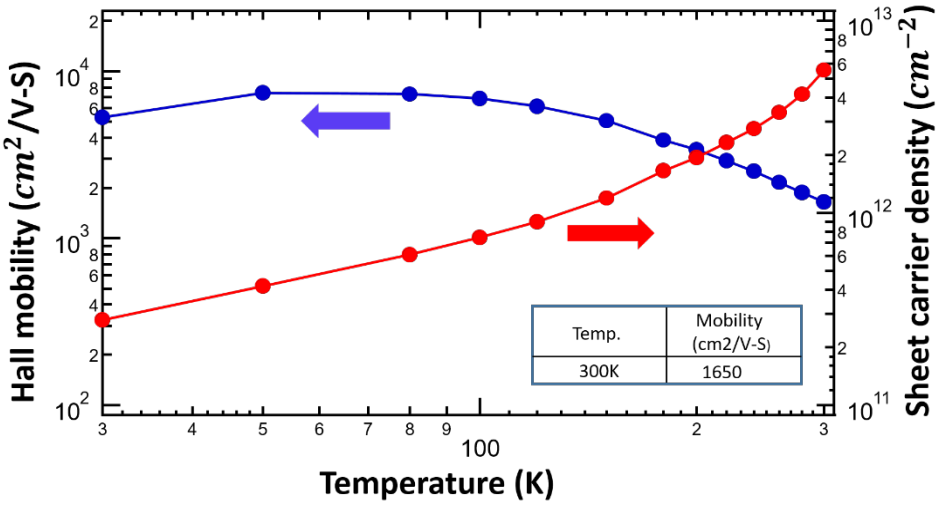

Figure 5.13: Temperature dependence of hole Hall mobility and sheet density for strained Ge MOS structure fabricated on Si(111) substrate.

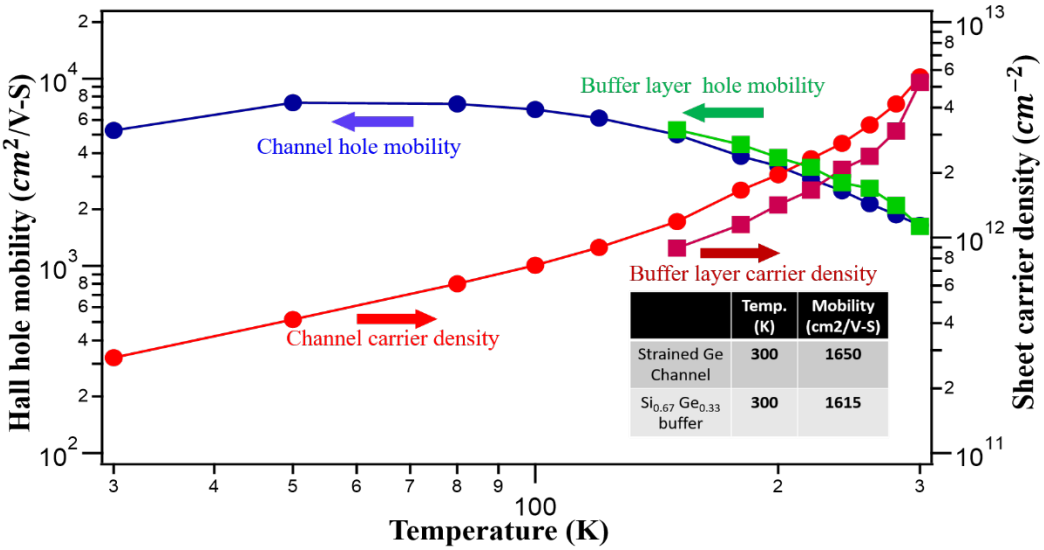

Figure 5.14: Temperature dependence of hole Hall mobility and sheet density for strained Ge MOS structure and SiGe buffer layer fabricated on Si(111) substrate.

5.6 Summary

Strained Ge channel thin layers were fabricated on Si(100) and Si(111) and structural properties were studied. Using reverse graded method, SiGe buffer layers with high Ge concentrations were formed on a Si(100) and (111) substrates, and relaxation ratios of 107 and 112 % were obtained. On the SiGe buffers, high-quality strained Ge channel layers were fabricated with the compressive strain -0.58 and -0.92 % with low RMS roughness. P doping in the SiGe buffer layer was examined and it was found that the P diffusion is completely suppressed in SiGe(111) compared to SiGe(100) and well controlled abrupt P doping was realized, which is expected to enable to suppress the parallel conduction in the buffer. This highly compressively strained Ge (111) is expected to open possibilities of high-performance Ge(111) based devices. Electrical properties of strained Ge surface channel MOS fabricated on Si(111) substrates was studied. The significant enhancement of hole Hall mobility with high-quality Al_2O_3/ strained Ge interface was observed. The high hole mobility (1650 cm^2/Vs) of the strained Ge surface channel at room temperature is remarkable and opening possibilities of high performance Ge(111) based devices.

6

Conclusions and Further work

6.1 Conclusions

The strain states and thermal stability of strain for the Ge-rich $Si_{1-x}Ge_x$ layers fabricated on a Ge(111), Ge-on-Si(111) and Ge(100) substrates were investigated to achieve the critical thickness for strain relaxation. The surface morphology of the Ge-rich $Si_{1-x}Ge_x$ layers were observed and presented the critical thickness for ridge free surface of the Ge-rich $Si_{1-x}Ge_x$ layers which will contribute to fabricate strained Si/Ge heterostructures on Si platform with small surface roughness.

A base Ge layer was fabricated on the Si(111) substrate by using two-temperature growth method for fabrication of the Ge-rich $Si_{1-x}Ge_x$ layers on Si(111). The relaxation ratio of the Ge epilayer was observed 104% compare to the Si(111) substrate which indicate that the base layer became slightly tensile strained layer. This residual tensile strain created in the Ge epilayer because of the difference of thermal expansion co-efficient between Ge and Si. The tensile strain of the HT-Ge layer was calculated to be 0.22. Since, the surface roughness of the base Ge layer influence the structural and electrical properties of the next epitaxial layer grown on it, a significantly low 0.33 nm RMS roughness was observed for the base Ge layer compare to the present reported RMS roughness of several nanometers. The relaxed Ge-on-Si(111) with very small surface roughness enable the fabrication of the next epitaxial layer on it with small surface roughness.

The strain states of the Ge-rich $Si_{1-x}Ge_x$ layers grown on the Ge-on-Si(111), Ge(111) and Ge(100) substrates at 350°C were investigated based on XRD profiles. Thickness fringes were clearly observed for the small thick strained $Si_{1-x}Ge_x$ layers. For the pseudomorphic $Si_{1-x}Ge_x$ layers, it was observed that the thickness fringes appear on both sides of the layer peak and angular spacing decreases with the thickness increases whereas the layer peak become narrow and intensity increases with the thickness of the layer increases. On the other hand, the thickness fringes disappear and the layer peak become broad and less intense for the partial relaxed $Si_{1-x}Ge_x$ layer. The thermal stability of the strained $Si_{1-x}Ge_x$ layers were examined after annealing the layers at 500°C for 3 minutes which is the higher temperature than the layers

growth temperature350°C. For the investigation of surface morphology of the Ge-rich $Si_{1-x}Ge_x$ layers, a wide surface area typically 200x200µm was used. It was observed that thin line ridges created on the surface of the Ge-rich $Si_{1-x}Ge_x$ layers for both pseudomorphic and relaxed layers. Their directions are along [10-1], [-110] and [0-11], that is, the intersections of equivalent (111) planes and the surface. For a very thin pseudomorphic layer, such type of ridges was not observed. The density of the thin line ridges increases with either the layer thickness or the strain increases. On the other hand, the density of the ridges remain same even the layers are post annealed at higher temperature than the growth temperature of the layers. Additional trenches with ridges were observed after annealing the layers which are responsible for making relaxed layer after annealing. It was also observed that after annealing the layer, the ridges remain same density as before annealing even the layer became relaxed after annealing, which indicates that the thin line ridges not contribute to the relaxation of the layer.

The strain states of the $Si_{1-x}Ge_x$ layers based on XRD results were summarized by plotting the thickness of the $Si_{1-x}Ge_x$ layers as a function of Ge contents of the SiGe layers to obtain experimental critical thickness for strain relaxation of the $Si_{1-x}Ge_x$ layers fabricated on Ge-on-Si(111), Ge(111) and Ge(100)substrates. It was observed that the critical thickness of $Si_{1-x}Ge_x$ layers on Ge-on-Si(111) is lower than that on Ge(111) substrate. The threading dislocations and stacking faults are created in the base Ge layer during HT-Ge layer growth. These threading dislocations extend to the next SiGe layer and contribute to the strain relaxation of the $Si_{1-x}Ge_x$ layers on the Ge-on-Si(111) substrate. On the other hand, the critical thickness of $Si_{1-x}Ge_x$ layers on Ge(100) is higher than that on Ge-on-Si(111) and Ge(111) substrates was observed due to the different dislocation generation mechanism and stacking faults depending on lattice plane orientation.

The critical thickness for ridge free surface was obtained by separating the thin line ridge free $Si_{1-x}Ge_x$ layers and plotted the thickness of the $Si_{1-x}Ge_x$ layers as a function of Ge contents of the $Si_{1-x}Ge_x$ layers fabricated on Ge-on-Si(111), Ge(111) and Ge(100)substrates. The critical thickness for the ridge free surface of the strained SiGe/Ge(100) is matched with the critical thickness calculated by assuming interfacial misfit dislocations for strained SiGe on Si(100). This comparative study can be contributed to enhance the performance the strained SiGe based devices.

The strained Ge channel was fabricated on a Si(111) substrate with a comparative sample grown on a Si (100) substrate. The high temperature Ge layer (HT-Ge) was grown on the Si(111) and Si(100) substrates at 800°C and 600°C respectively for fabricating base Ge layer where the relaxation ration of the base Ge layer on (111) and (100) planes was calculate to be 105 and 104% respectively. The tensile strains 0.28 and 0.20% were obtained for the HT-Ge grown on the Si (111) and Si(100) substrates respectively. For the fabrication of the strained Ge channels by using these base Ge layers, reverse graded buffer method was used to fabricate a high-quality relaxed $Si_{0.26}Ge_{0.74}$ buffer as a virtual substrate on (111) and (100) lattice plane orientations. The relaxation ratio of the $Si_{0.26}Ge_{0.74}$ buffer layer compared to the Si(111) and Si (100) was evaluated to be 107 and 112% while the relaxation ratio of the $Si_{0.26}Ge_{0.74}$ buffer layer compared to the base layer Ge(111) and Ge(100) was evaluated to be 86 and 74% respectively. Formation of 60^0 dislocations is responsible for slightly different residual tensile strain between the $Si_{0.26}Ge_{0.74}$ (111) and $Si_{0.26}Ge_{0.74}$ (100) buffer layers. Phosphorous (P) doped thin layer was inserted in the buffer layer due to the suppression of parallel conduction through buffer layer and well controlled abrupt P doping was realized from SIMS profiles.

The compressive strains of the strained Ge channels grown on Si (111) and Si (100) were calculated to be -0.92% and -0.58% respectively. Since the relaxation ratio of the $Si_{0.26}Ge_{0.74}$(100) is lower than that of the $Si_{0.26}Ge_{0.74}$(111) buffer layer compare to base Ge layer, the tensile strain of the $Si_{0.26}Ge_{0.74}$(100) is higher than that of the $Si_{0.26}Ge_{0.74}$(111) buffer layer. As a result, the compressive strain of the strained Ge channel grown on $Si_{0.26}Ge_{0.74}$(100) is smaller than that of the $Si_{0.26}Ge_{0.74}$(111). For investigating the thermal stability of compressive strain for the strained Ge channel, the samples were annealed at various temperatures for one minute. It was observed that the compressive strain decreases with the increasing temperature. However, RMS roughness was obtained 0.34 nm and 1.7 nm for the strained Ge(100) and Ge(111) respectively. The difference RMS roughness between the strained Ge(100) and (111) is considered to come from the different growth temperatures of the Ge-on-Si. The strained Ge was formed on the SiGe (111) relaxed buffer layer and larger compressive strain was found to be obtained in Ge(111) compared to Ge(100), opening possibilities of high performance Ge(111) based devices.

For realization of the high hole mobility of the strained Ge(111), a strained Ge surface channel was fabricated on a Si(111) substrate. The combination of reverse grade with low temperature buffer method was used to fabricate a thin buffer layer compare to the reverse

graded buffer layer by using base Ge layer. The relaxation ratios of the $Si_{0.67}Ge_{0.33}$ (111) constant composition layer compared to Ge(111) epilayer was evaluated to be 87% indicates that buffer layer is slightly tensile-strained. A thin Phosphorous (P) doped layer was inserted in the buffer layer due to the suppression of parallel conduction through buffer layer. Electrical properties of strained Ge(111) channel were studied. High hole mobility 1650 cm^2/Vs at room temperature of the surface channel strained Ge(111) MOS with high-quality Al_2O_3/ strained Ge interface was obtained. Moreover, mobility enhancement was observed by suppressing parallel conduction caused by defect-originated holes in the buffer layer by means of inserting a P-doped layer. The high-quality Al_2O_3/ strained Ge interface is a promising template for high-performance surface channel Ge-based devices.

6.2 Further work

There are some aspects depending on this research work which are described as follows

1. Since the top most surface of the SiGe can be consumed during device fabrication processing. Therefore, for practical device applications, the fully strained SiGe layer as thick as possible is highly demanded. For this purpose, the critical thickness of strained SiGe on Ge-on-Si(111) needed to increase as thick as possible from current critical thickness which are precisely determined in this research by considering partial relaxation of the layer begins via generating dislocations.

2. High compressive strained Ge channel on Si(111) with low surface roughness and high hole mobility can be applied in practical device applications by fabricating p-MOSFET.

3. The strained Ge and Ge-rich SiGe on (111) surface orientation with very low surface roughness studies can be contributed to fabricate next generation devices such as spintronics.

7
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