Temperature Dependent Thermal Capacitance Characterization for SOI-MOSFETs

Benito González, Beatriz Aja, Eduardo Artal, *Life Member, IEEE*,
Antonio Lázaro, *Senior Member, IEEE,* Antonio Núñez

***Abstract*—Thermal capacitances are required to describe fast dynamic thermal behavior in SOI devices. This paper presents a physical model based on the AC technique, together with the characteristic thermal frequency determination through the frequency response of the output conductance, for calculating the thermal capacitance of single-finger and multi-finger SOI-MOSFETs. The model accounts for total gate width and substrate temperature, making evident the augmented thermal coupling when multi-fingers are used. Thermal capacitances and corresponding time constants, extracted from a variety of gate widths and number of fingers, are correctly predicted up to a substrate temperature of 150°C.**

Index Terms—**electrothermal characterization, model, SOI-MOSFET, substrate temperature, thermal capacitance.**

I. Introduction

Silicon-on-insulator (SOI) MOSFETs, having a buried oxide layer thicker than 100 nm, suffer from obstruction of the heat flow towards the substrate [1], [2]. This, together with the ultra-thin internal layers used at nanometer length scales, with a reduced thermal conductivity [3], [4], results in a remarkable self-heating effect, particularly in DC operation/biasing with relevant electrical power levels involved (as from dozens of mW [5]). This makes the design and configuration of terminals, acting as heat sinks, critical in SOI-MOSFET performance [1], [6].

The typical thermal model for the temperature rise in devices, induced by self-heating effects, consists of the equivalent circuit shown in Fig. 1, with the thermal resistance, R_{th}, and capacitance, C_{th}, being connected in parallel. This model is based on the following analogy between electrical and thermal magnitudes: The temperature rise in the device channel, ΔT_c, above the substrate temperature, T_{sub}, is actually the "voltage drop" when the "current" flowing through the circuit is the electrical power dissipated, P, in the device (i.e. $\Delta T_c = Z_{th}P$, with $1/Z_{th} = 1/R_{th} + j\omega C_{th}$). Making use of more sophisticated thermal networks [7], hot spots could be even localized (i.e. not only the average device temperature can be determined). Nevertheless, our thermal model maintains a higher degree of simplicity, to be useful in the context of compact model development for circuit simulators.

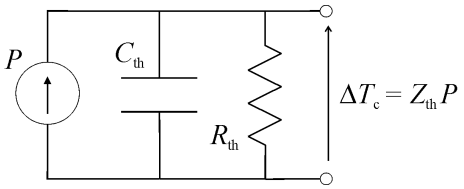


Fig. 1. Equivalent circuit for self-heating effects in devices.

For DC response, the SOI-MOSFET thermal resistance has been extensively investigated in the literature [8–11]. Regarding characterization, several well-established techniques have been used for obtaining the thermal resistance, such as the AC/RF conductance method [8], pulsed characteristics [9], [10], or with impedance analyzers [11]. Regarding modeling, precise and simple enough compact models for circuit simulation purposes have been developed, including thermal coupling in case of multi-finger devices [12–17].

With respect to the thermal capacitance, it is necessary to describe the fast dynamic thermal behavior in SOI devices subjected to abrupt changes in power generation [7], which was also demonstrated in [9], with the decrease of drain current as SOI-MOSFETs heat up after being turned on. Despite this, too few studies concerning this thermal capacitance issue have been published, and more advancement in both measurement techniques and modeling is required.

Small-signal equivalent circuit analysis has been used for investigating heat flow paths in SOI-MOSFETs [18]. Nevertheless, empirical approaches are needed, such as fitting

This work was supported by the Spanish MEC under Project GREENSENSE–TEC2015-67883-R and RTI2018-096019-B-C31.

B. González and A. Núñez are at the Institute for Applied Microelectronics, Universidad de Las Palmas de Gran Canaria, Campus Universitario de Tafira, Las Palmas, CO 35017 Spain (e-mail: benito@iuma.ulpgc.es and nunez@iuma.ulpgc.es).

B. Aja and E. Artal are at the Department of Communications Engineering of the University of Cantabria, Edificio Ingeniería de Telecomunicación-Prof. José Luis García, Plaza de la Ciencia s/n, Santander, CO 39005 Spain (e-mail: beatriz.aja@unican.es and eduardo.artal@unican.es).

A. Lázaro is at the Departament of Electronic, Electrical and Automatic Engineering, Universitat Rovira i Virgili, Escola Tècnica Superior d'Enginyeria, Av. Dels Països Catalans 26, Tarragona, CO 43007 Spain (e-mail: antonioramon.lazaro@urv.cat).

of the elements of the electrical/thermal circuit or the use of multiple-pole RC networks for the thermal part [6], [15].

Other studies are based on the transient response to pulsed measurements and the determination of the thermal time constant, τ_{th} ($\tau_{th} = R_{th}C_{th}$) [19]. This method has been applied to high-voltage MOSFETs, when a resistance connected to the drain is enough to measure the drain current transient (with the voltage drop across the resistance). However, in case of SOI-MOSFETs this is a non-viable methodology, due to their small thermal time constant (hundreds of nanoseconds) [5], [11]. In addition, it is relatively easy to introduce errors in the result, since the temperature is derived from complicated fittings in the model as in [19] (or even for a pulsed *I*–*V* system fully capable of pulsing gate/drain bias in a submicrosecond time scale [10]).

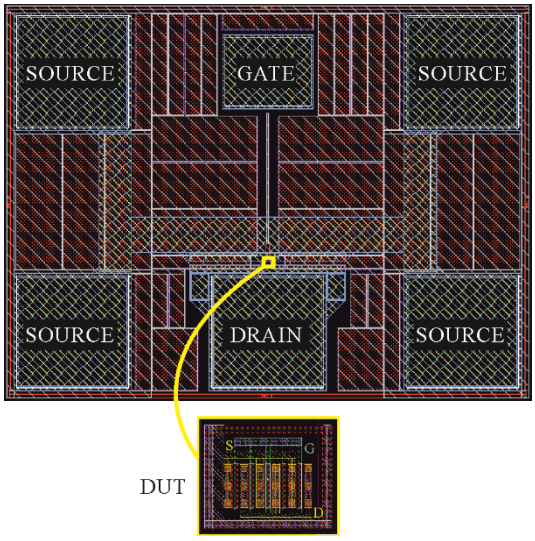


Fig. 2. Layout of GSG on-wafer test structure and DUT (with $N_f = 5$).

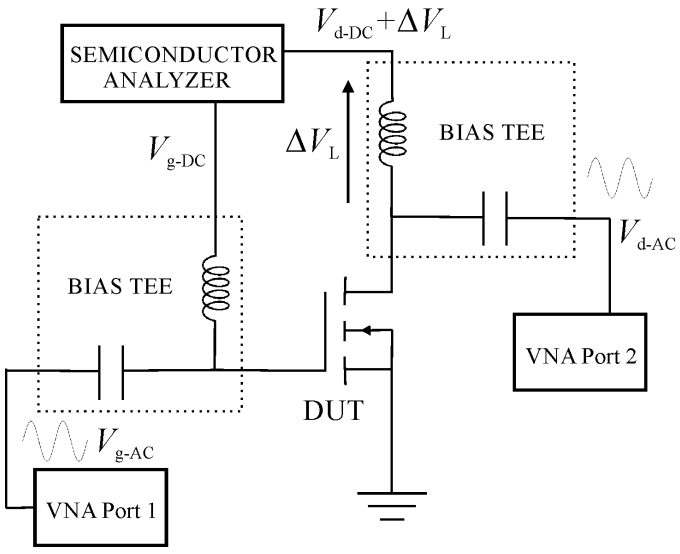


Fig. 3. Schematic of the AC measurement system for the DUT.

The AC/RF technique has also been applied previously to measure complex thermal impedances, but in the case of the thermal capacitance a frequency response for the imaginary part of the conductance parameter (Y_{22}), when the dynamic self-heating is avoided, was just assumed [5], [20]. Alternatively, the thermal capacitance has been extracted by using an underestimated thermal frequency, f_{th} ($\omega_{th} = 2\pi f_{th} = 1/\tau_{th}$), once the thermal resistance has been obtained [11].

On the other hand, SOI-MOSFET thermal capacitance has been numerically simulated [21]. In this case, when applying the AC/RF technique, the resulting drain-to-source capacitance shows a constant value at low frequencies that, as far as we know, cannot yet be experimentally assessed.

In this paper, the thermal capacitance of single-finger and multi-finger SOI-MOSFETs is obtained in a straightforward and simple form with a methodology based on the AC technique and the thermal frequency determination, through the output conductance frequency response [21]. In addition, a model for the thermal capacitance is proposed, to be implemented in circuit simulators, which is valid when the thermal coupling increases by the use of multi-finger devices [12], and that includes the substrate temperature and total gate width dependencies. Regarding the channel length, it has an impact that is less significant on SOI-MOSFET self-heating than compared to channel width, as usually the change of channel width is much greater than that of channel length [6].

Thus, the SOI-MOSFETs under consideration, varying the gate width and number of fingers, are described in Section II, where heat dissipation is also analyzed through numerical simulations. The experimental set-up used for their temperature dependent thermal capacitance characterization is detailed in Section III. Section IV is devoted to thermal capacitance determination, measurement and modeling. Finally, some conclusions are discussed in Section V.

II. Fabricated Devices

Eight SOI N-channel MOSFETs, partially depleted, with 180 nm gate length, were fabricated using XT018 0.18 µm HV SOI-CMOS technology (by XFAB). The transistors were body-tied to prevent the floating-body effect and embedded in ground–signal–ground (GSG) on-wafer test structures. The corresponding layout is shown in Fig. 2, together with that of the device-under-test (DUT).

Thus, four single-finger transistors, 10, 20, 40, and 60 µm (W) wide, were made. The four remaining ones, to enhance self-heating, were multi-finger devices with the same total gate width ($W = N_f W_f$), composed of 5, 10, 20, and 30 parallel fingers (N_f), each finger being 2 µm wide (W_f).

Numerical simulations with Sentaurus Device [22] have been performed as in [17], for the single-finger device 40 µm wide, as example, and demonstrate that 12% of the generated heat is escaping from the Silicon body through the gate, and 34% and 54% through the source and drain contacts, respectively, which points out the relevance of the access resistances in self-heating, mainly the drain terminal (as the hot spot of the device is located by the drain side). A deeper study would be required to account

for the heat propagation physical properties of the materials in detailed, which could be object of future works.

III. Experimental Set-up

On-wafer measurements were performed with a Cascade Summit 9000 probe station. A thermal chuck set the substrate temperature, T_{sub}, from 30 to 150°C, in 20°C increments.

As indicated in Fig. 3 for the experimental set-up, *S*-parameters were measured from 30 kHz to 1.2 MHz with the Agilent N9913A Vector Network Analyzer and Cascade GSG microprobes, for all temperatures. Moreover, *ad-hoc* designed bias tees were used for the frequency range under consideration. The Agilent B1500A Semiconductor Analyzer made the devices operate in saturation regime, with a DC gate and drain voltages of 2 V ($V_{g\text{-}DC}$) and 1.8 V ($V_{d\text{-}DC}$), respectively, to enhance self-heating effects [16].

In addition, it must be pointed out that, for the DC drain voltage setting, the voltage drop through the corresponding DC path (ΔV_L in Fig. 3) must be overcome, for every transistor and substrate temperature. This was evaluated as the DC resistance of the inductor (68.9 Ω) times the DC drain current at the bias considered ($V_{g\text{-}DC}$ = 2 V, $V_{d\text{-}DC}$ = 1.8 V), obtained in [16].

In order to calibrate the measurement system, the short-open-load-through method was implemented in a previous step, and the pad-to-device parasitic elements are de-embedded with the open-short-thru de-embedding technique [23]. When more sophisticated thermal networks are used [7], the corresponding parasitic elements would need to be also de-embedded and evaluated for the thermal circuit, which is not the case.

IV. Thermal Capacitance

A. Characterization

Accounting for the thermal network of Fig. 1, the real part of the equivalent thermal impedance, Z_{th}, is given by

$$\mathrm{real}(Z_{th}) = \frac{R_{th}}{1+\omega^2 R_{th}^2 C_{th}^2} \tag{1}$$

On the other hand, according to the AC conductance technique for MOSFETs [8], the real part of the thermal impedance can be written as

$$\mathrm{real}(Z_{th}) = \frac{\Delta g_{dd}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT} + I_d\right)} \tag{2}$$

where $\Delta g_{dd} = g_{dd} - g_{ddT}$, g_{dd} is the output conductance at the angular frequency ω, g_{ddT} is the conductance at high frequency (with dynamic self-heating removed), I_d is the drain current, and V_d is the drain voltage. Therefore, equating (1) and (2), as in [21], results in

$$\frac{R_{th}}{1+\omega^2 R_{th}^2 C_{th}^2} = \frac{\Delta g_{dd}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT} + I_d\right)} \tag{3}$$

Thus, at low frequency ($\omega \approx 0$), the following expression for the thermal resistance is derived,

$$R_{th} = \frac{\Delta g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT} + I_d\right)} \tag{4}$$

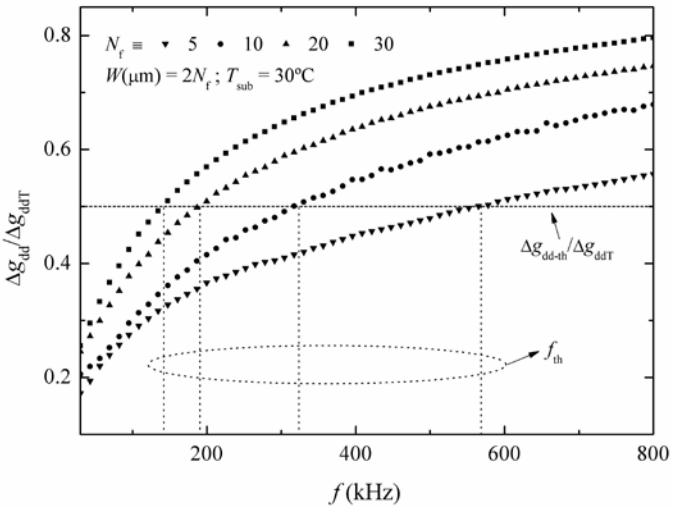
with $\Delta g_{ddT} = g_{ddo} - g_{ddT}$, g_{ddo} being the DC conductance. Alternatively, at the characteristic thermal frequency, f_{th} ($\omega_{th} = 2\pi f_{th} = 1/\tau_{th}$), it is found that

$$\frac{R_{th}}{2} = \frac{\Delta g_{dd\text{-}th}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT} + I_d\right)} \tag{5}$$

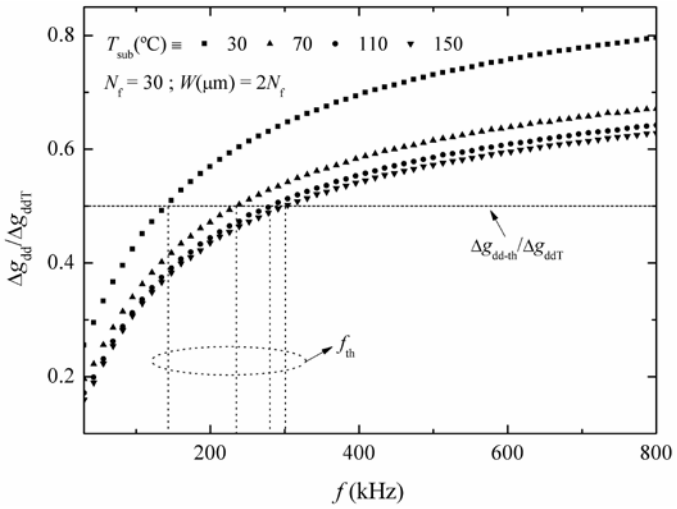
where $\Delta g_{dd\text{-}th} = g_{dd\text{-}th} - g_{ddT}$, with $g_{dd\text{-}th} = g_{dd}(\omega_{th})$. Therefore, dividing (5) by (4), at the characteristic thermal frequency it results that

$$\left.\frac{\Delta g_{dd}}{\Delta g_{ddT}}\right|_{\omega_{th}} = \frac{\Delta g_{dd\text{-}th}}{\Delta g_{ddT}} = \frac{1}{2} \tag{6}$$

The required parameters, g_{ddo} and g_{ddT}, for having the $\Delta g_{dd}/\Delta g_{ddT}$ frequency response were obtained in [16] at the bias considered ($V_{g\text{-}DC}$ = 2 V, $V_{d\text{-}DC}$ = 1.8 V), for all devices and substrate temperatures.



(a)



(b)

Fig. 4. $\Delta g_{dd}/\Delta g_{ddT}$ frequency response: (a) at 30°C for multi-finger transistors and (b) for a multi-finger transistor (with N_f = 30) at different substrate temperatures; $V_{g\text{-}DC}$ = 2 V, $V_{d\text{-}DC}$ = 1.8 V.

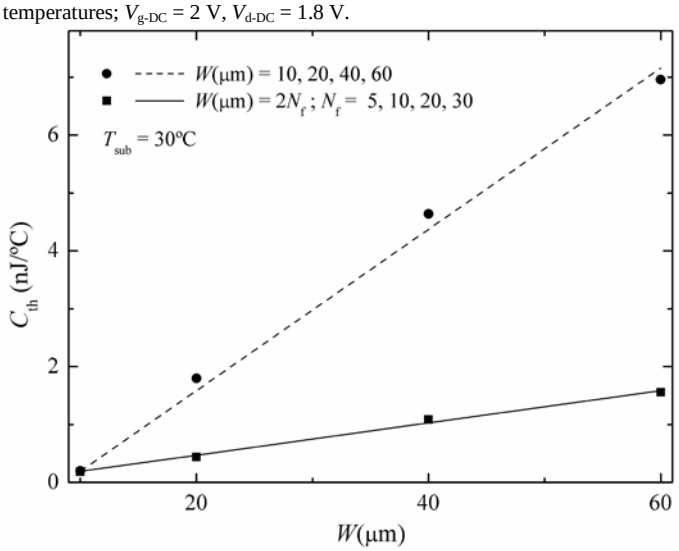


Fig. 5. Thermal capacitance as a function of gate width, extracted and modeled for single-finger transistors (with circles and dashed line, respectively), and multi-finger transistors (with squares and solid line, respectively); T_{sub} = 30°C.

TABLE I
PARAMETERS FOR THE SUBSTRATE TEMPERATURE DEPENDENCY

Parameter	m_{sf}	m_{mf}	$<C_{tho}>$
α (×10^{-10})	1.39 (J/°C-μm)	0.28 (J/°C-μm)	1.87 (J/°C)
β	–0.91	–0.55	–0.66

The resulting measured $\Delta g_{dd}/\Delta g_{ddT}$ frequency response, for a substrate temperature of 30°C, is represented by symbols in Fig. 4(a) for multi-finger transistors, with the characteristic thermal frequency that is obtained when $\Delta g_{dd}/\Delta g_{ddT}$ = 1/2 (6), and it is indicated with vertical lines. Notice that the narrower the transistor is, the higher the f_{th} results. Additionally, the characteristic thermal frequency increases with the substrate temperature, as Fig. 4(b) shows for a multi-finger transistor (with N_f = 30), where the measured $\Delta g_{dd}/\Delta g_{ddT}$ frequency response is similarly represented.

Analogous dependencies on both gate width and substrate temperature were observed for the characteristic thermal frequency in all single-finger and multi-finger devices. Once the characteristic thermal frequency has been extracted for all SOI-MOSFETs, at the different temperatures, the corresponding thermal capacitance is obtained through (7),

$$C_{th} = \frac{1}{2\pi f_{th} R_{th}} \tag{7}$$

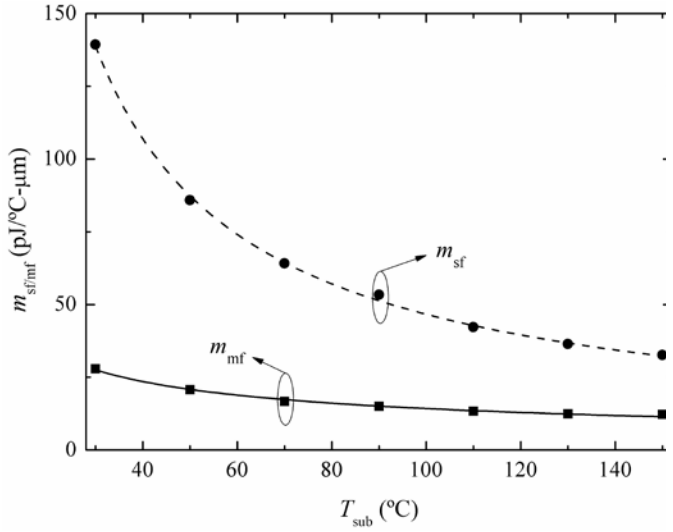
with the thermal resistance measured in [16]. Finally, when using the proposed method for high scaled devices, accesses resistances, which need to be extracted for a proper electrical characterization, must be accounted (not de-embedded) for a correct thermal characterization, as proposed.

B. Modeling

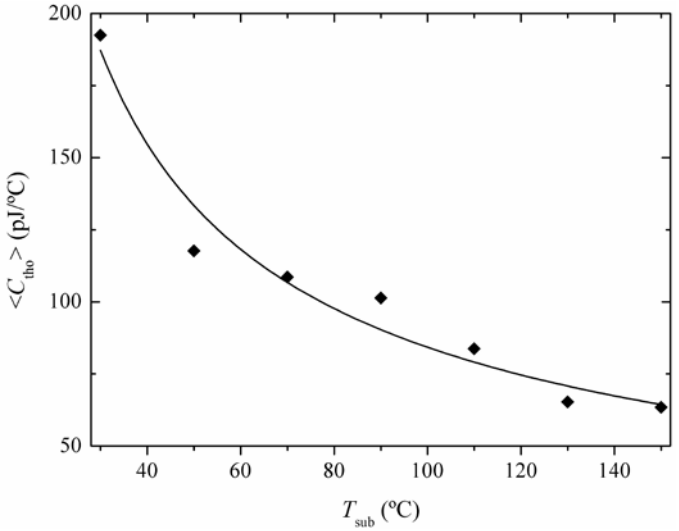
Regarding the gate width, W, the thermal capacitance for single-finger and multi-finger SOI-MOSFETs, at a substrate temperature of 30°C, shows an expected linear dependency as indicated in Fig. 5, where circles and squares represent the respective measured data. Notice that for the narrower total gate width (W = 10 μm), the thermal capacitances of single-finger and multi-finger devices practically coincide. However, superior thermal capacitances result for the single-finger SOI-MOSFETs, when the gate width rises, which could be attributed to having much fewer number of terminal contacts than those in multi-finger devices, through which the heat flow is spread out. Thus, the thermal capacitance, C_{th}, for all transistors can be modeled as a function of the total gate width, W (in μm), using the following linear expression:

$$C_{th} = m_{sf/mf}(W - 10) + <C_{tho}> \tag{8}$$

where $<C_{tho}> \approx 0.2$ nJ/°C represents the average thermal capacitance of those transistors for the narrower single-finger and multi-finger devices (W = 10 μm), and m_{mf} = 28 pJ/°C-μm and m_{sf} = 14 pJ/°C-μm are the slope of the linear dependency for multi-finger and single-finger SOI-MOSFETs, respectively. The modeled thermal capacitance is plotted in Fig. 5 for single-finger (with dashed line) and multi-finger (with solid line) devices, showing a good agreement with measured data.

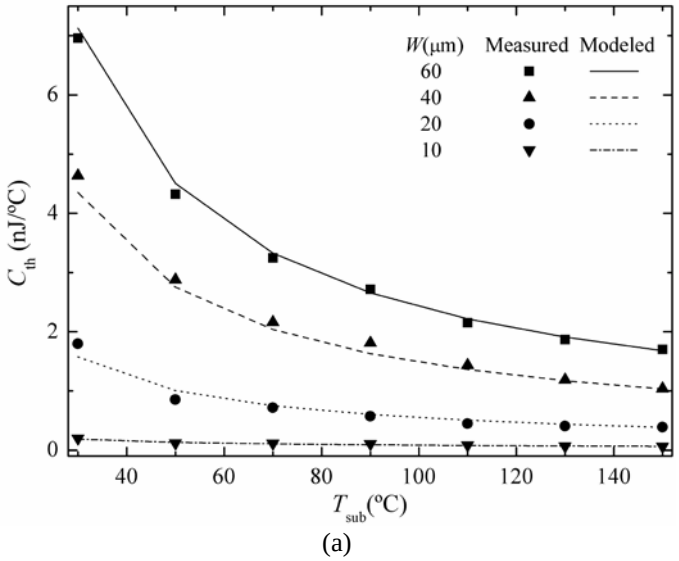


(a)

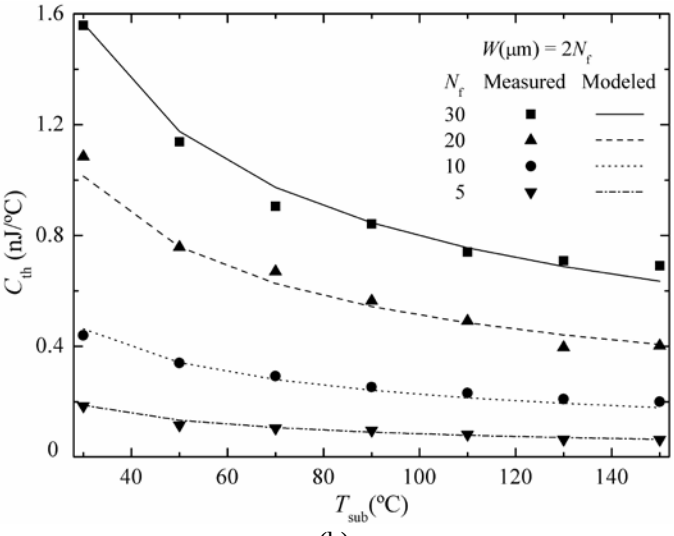


(b)

Fig. 6. Slope of the thermal capacitance linear dependency on the gate width, m_{sf} (single-finger devices) and m_{mf} (multi-finger devices) (a), and the average of the thermal capacitances for the narrower single-finger and multi-finger devices (W = 10 µm), $<C_{tho}>$ (b), as a function of the substrate temperature, extracted from measurements (scattered) and modeled (lines).



(a)



(b)

Fig. 7. Thermal capacitance extracted from measurements (scattered) and modeled (lines), as a function of the substrate temperature, for (a) single-finger devices, and (b) multi-finger devices.

Similar results are obtained for the remaining substrate temperatures, with m_{sf} and m_{mf}, and $<C_{tho}>$ diminishing as the substrate temperature increases, as Fig. 6(a) and 6(b) show, respectively, with symbols. These three parameters for the substrate temperature dependency can be modeled, with lines in Fig. 6(a) and 6(b), using the power function $\alpha(T_{sub}/30)^{\beta}$. Results for α and β are summarized in Table I in all cases.

The measured and modeled thermal capacitances are represented, as a function of the substrate temperature, with symbols and lines, respectively, in Fig. 7(a) for single-finger transistors and Fig. 7(b) for multi-finger ones. The observed linear and power dependences of the thermal capacitance on

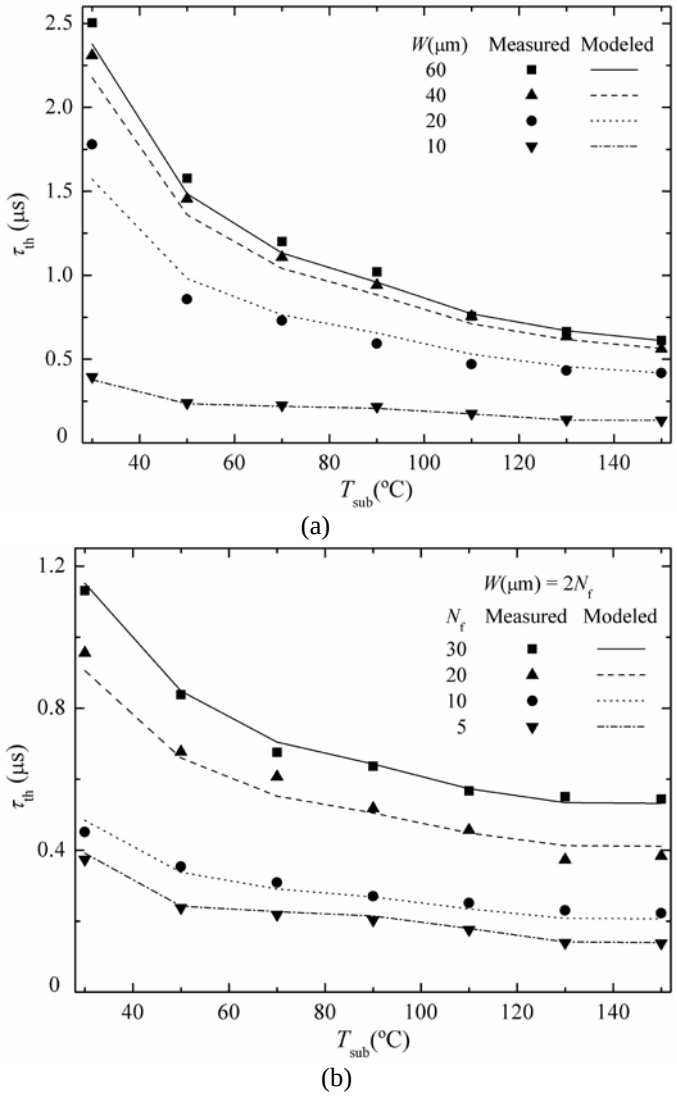


Fig. 8. Thermal time constant extracted from measurements (scattered) and modeled (lines), as a function of the substrate temperature, for (a) single-finger devices, and (b) multi-finger devices.

the total gate width and substrate temperature, respectively, were previously obtained in [6] and [19]. Furthermore, thermal capacitances of the same order of magnitude ($0.1–5\times10^{-9}$ J/°C) were measured in [6] for RF SOI-MOSFETs and [24] for FinFETs.

Finally, accounting for the thermal impedances in [16], Fig. 8(a) and 8(b) show the resulting measured (with symbols) and modeled (with lines) thermal time constant, $\tau_{th} = R_{th}C_{th}$, for single-finger and multi-finger devices, respectively, as a function of the substrate temperature. Comparable results, from hundreds of nanoseconds to microseconds, were obtained in [5], [11], [21], and [24] and modeled in [18] with multiple-pole thermal RC networks. Notice that, for a given total gate width, the thermal time constant is larger in single-finger devices than in multi-finger ones, tending to be similar as the number of fingers is reduced. Furthermore, in contrast to [19], the thermal time constant diminishes as the substrate temperature rises, this dependence being more intense in single-finger devices and when the total gate width increases.

The average relative error for the thermal capacitance and thermal time constant, between measured and modeled data, in the substrate temperature range considered, is lower than 9% in all transistors, with a maximum absolute error of 18%.

Finally, it can be highlighted that confinement due to gate length scaling results in smaller thermal capacitances; a linear dependency of the thermal capacitance on channel length is also expected [6]. In this scenario, as (4) indicates, the increment observed for Δg_{ddT} when the gate length is reduced [25], is balanced with a superior drain current, resulting on a constant minimum thermal capacitance (maximum thermal resistance [26]) for ultra-short devices, when extrinsic elements determine the device thermal performance (as contacts do not scale with gate length).

V. Conclusions

The thermal capacitance of single-finger and multi-finger SOI-MOSFETs has been successfully measured using the AC conductance method, together with the determination of the thermal frequency, once the thermal resistance has been obtained. The expected linear and power dependences of the thermal capacitance on the total gate width and substrate temperature (up to 150°C), respectively, were determined and modeled for circuit-design purposes. Multi-finger devices show a minor influence of the total gate width on the thermal capacitance, which results in lower thermal capacitances than those of single-finger devices. This could be attributed to thermal coupling, when a superior number of terminals in the case of multi-finger SOI-MOSFETs results in a higher heat flow spread outside the devices. Finally, corresponding thermal time constants were also correctly predicted, showing a reverse dependence with the substrate temperature, which is more intense for large total gate widths and single-finger devices.

References

[1] M. Shrivastava *et al.*, "Physical insight toward heat transport and an improved electro-thermal modeling framework for FinFET architectures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1353–1363, May 2012, doi: 10.1109/TED.2012.2188296.

[2] B. González, B. Iñiguez, A. Lázaro, and A. Cerdeira, "Numerical dc self-heating in planar double-gate MOSFETs," *Semicond Sci. Technol.*, vol. 26, no. 9, pp. 095014, Sep. 2011, doi: 10.1088/0268-1242/26/9/095014.

[3] M. von Arx, O. Paul, and H. Baltes, "Process-dependent thin-film thermal conductivities for thermal CMOS MEMS," *J. Microelectromech. Syst.*, vol. 9, no. 1, pp. 136–145, Jan. 2000, doi: 10.1109/84.825788.

[4] S. M. Lee and D. G. Cahill, "Heat transport in thin dielectric films," *J. Appl. Phys.*, vol. 81, no. 6, pp. 2590–2595, Mar. 1997, doi: 10.1063/1.363923.

[5] S. Makovejev, S. H. Olsen, V. Kilchytska, and J. P. Raskin, "Time and frequency domain characterization of transistor self-heating," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1844–51, Jun. 2013, doi: 10.1109/TED.2013.2259174.

[6] Z. Chen , L. Sun, J. Liu , G. Su, and W. Zhou, "Investigation of geometry dependence of thermal resistance and capacitance in RF SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4232–7, Oct. 2018, doi: 10.1109/TED.2018.2863022.

[7] J. Lin, M. Shen, M.-C. Cheng, and M. L. Glasser, "Efficient thermal modeling of SOI MOSFETs for fast dynamic operation," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1659–66, Oct. 2004, doi: 10.1109/TED.2004.835994.

[8] N. Rinaldi, "Small-signal operation of semiconductor devices including selfheating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, doi: 10.1109/16.902734.

[9] K. A. Jenkins, J. Y. C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997, doi: 10.1109/16.641362.

[10] J. Joh, J. A. del Alamo, T. M. Chou, H. Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, Dec. 2009, doi: 10.1109/TED.2009.2032614.

[11] W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C., "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 730-736, Apr. 2001, doi: 10.1109/16.915707.

[12] B. Swahn and S. Hassoun, "Electro-thermal analysis of multi-fin devices," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol.16, no. 7, pp. 816–829, July 2008, doi: 10.1109/TVLSI.2008.2000455.

[13] S. Hniki *et al.*, "Thermal effects modeling of multi-fingered MOSFETs based on new specific test structures," *in Proc. IEEE ESSDERC*, Athens, Greece, 2009, pp. 296–299, doi: 10.1109/ESSDERC.2009.5331544.

[14] F. Nasri, M. Fadhel, B. Aissa, and H. Belmabrouk, "Nonlinear electrothermal model for investigation of heat transfer process in a 22-nm FD-SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1461–1466, Ap. 2017, doi: 10.1109/TED.2017.2666262.

[15] J. S. Brodsky, R. M. Fox, D. T. Zweidinger, and S. Veeraraghavan, "A physics-based, dynamic thermal impedance model for SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 957–964, Jun 1997, doi: 10.1109/16.585551.

[16] B. González, R. Rodríguez, and A. Lázaro, "Thermal resistance characterization for multifinger SOI-MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3626–3632, Sep. 2018, doi: 10.1109/TED.2018.2853799.

[17] B. González, J. B. Roldán, B. Iñiguez, A. Lázaro, and A. Cerdeira, "DC self-heating effects modelling in SOI and bulk FinFETs," *Microelectron. J.*, vol. 46, pp. 320–326, Ap. 2015, doi: 10.1016/j.mejo.2015.02.003.

[18] B. M. Tenbroek, W. Redman-White, M .S. L. Lee, R. J. T. Bunyan, and M .J. Uren, "Characterisation of geometry dependence of SOI MOSFET thermal resistance and capacitance parameters," *in Proc. IEEE SOI Conf.*, Fish Camp, CA, USA, 1997, pp. 114–5, doi: 10.1109/SOI.1997.634959.

[19] C. Anghel, R. Gillon, and A. M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141–143, March 2004, doi: 10.1109/LED.2003.821669.

[20] A. J. Scholten, G. D. J. Smit, R. M. T. Pijper, L. F. Tiemeijer, H. P. Tuinhout, J.-P. J. van der Steen, A. Mercha, M. Braccioli, and D. B. M. Klaassen, "Experimental assessment of self-heating in SOI FinFETs," *in Proc. IEEE IEDM*, Baltimore, MD, USA, 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424362.

[21] U. S. Kumar and V. R. Rao, "A Novel TCAD-Based Thermal Extraction Approach for Nanoscale FinFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1404–7, March 2017, doi: 10.1109/TED.2017.2657626.

[22] Version N-2017.09 Synopsys TCAD suite.

[23] I. Gutiérrez, J. Meléndez, J. García, I. Adin, G. Bistue, and J. de No, "Reliability Verification in a Measurement System of Integrated Varactors for RF Applications," *IEEE Lat. Am. Trans.*, vol. 3, no. 4, pp. 15–20, Oct. 2005, doi: 10.1109/TLA.2005.1642424.

[24] S. Makovejev, S. Olsen, and J.-P. Raskin, "RF extraction of self-heating effects in FinFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, doi: 10.1109/TED.2011.2162333.

[25] S. Makovejev *et al.*, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs," *Solid-State Electron.*, vol. 71, pp. 93–100, May 2012, doi: 10.1016/j.sse.2011.10.027.

[26] P. Kushwaha *et al.*, "Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG," *Microelectron. J.*, vol. 56, pp. 171–176, Oct. 2016, doi: 10.1016/j.mejo.2016.07.014.