Fault-Tolerant Space Vector Modulation for Modular Multilevel Converters With Bypassed Faulty Submodules

Mohsen Aleenejad, *Member, IEEE*, Hamid Mahmoudi, *Student Member, IEEE*, Seyyedmahdi Jafarishiadeh, *Student Member, IEEE*, and Reza Ahmadi, *Member, IEEE*

***Abstract*—This paper develops a modulation based fault-tolerant (FT) strategy for restoring the operation of three-phase modular multilevel converters (MMCs) with faulty switches. This FT strategy is based on a proposed modified space vector modulation (SVM) technique that generates balanced line-to-line (line) voltages even in the case of a fault occurrence. In the postfault operation, the proposed strategy is able to restore the fundamental amplitude of the line to the neutral (load) voltages to that of the normal operation condition with a slightly increased voltage stress over the switches in the faulty phase. In this paper, first a brief background about MMCs and SVM technique is provided. Then, the proposed FT strategy and the modified SVM technique are presented. Finally, several simulation and experimental results are provided to validate operation of the proposed strategy.**

***Index Terms*—Fault-tolerant (FT) strategy, modular multilevel converters (MMCs), space vector modulation (SVM).**

I. Introduction

MODULAR multilevel converters (MMCs) are an attractive solution for applications [1], [2]. They feature superior characteristics, such as high modularity [3], high efficiency [4], higher voltage level availability [5], low total harmonic distortion (THD) [6], and high power quality [7]. However, these admirable aspects come at the price of a more complicated structure with an increased number of power electronic devices. Thus, the chances of fault occurrence increase [8]. High reliability is a critical attribute for the power converters in the industry [9], [10]. Thus, proposing fault-tolerant (FT) methods for multilevels converters (MLC) has been a subject of importance for researchers in the field of power electronics [11].

Manuscript received September 15, 2017; revised January 16, 2018, April 6, 2018, and June 20, 2018; accepted June 30, 2018. Date of publication August 1, 2018; date of current version October 31, 2018. *(Corresponding author: Reza Ahmadi.)*

M. Aleenejad is with the Department of Electrical and Computer Engineering, New York University, Brooklyn, NY 11201 USA (e-mail: aleenejad@nyu.edu).

H. Mahmoudi, S. M. Jafarishiadeh, and R. Ahmadi are with the Department of Electrical Engineering and Computer Science, the University of Kansas, Lawrence, KS 66045 USA (e-mail: mahmoudi@ku.edu; jafari@ku.edu; ahmadi@ku.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2018.2860518

Recently, several FT control methods have been presented for the MLC, however, only a few of them are suitable for MMCs [8], [12]. In [13], various fault modes of an MMC are discussed. Usually, after detecting the location of the fault, the defective submodules (SMs) are bypassed and an FT strategy is applied [14]. However, this leads to the generation of unbalanced line-to-line (line) voltages. The conventional answer to this problem is to bypass one additional SM in the opposite leg of the faulty phase and two corresponding operative SMs in the healthy phases [15]. This results in balanced operation; however, it renders six SMs nonoperational, resulting in a significant reduction of converter's capacity [16]. To overcome this problem, a number of auxiliary SMs are incorporated in each phase [17]–[19]. In [17], these auxiliary SMs are not engaged in the normal operation of the converter. The main drawback is that the auxiliary SMs' start-up performance suffers from long charging time and transient issues. In [18], a strategy was developed to initiate these SMs during the normal operation by charging their capacitors. It is worth mentioning that the auxiliary SMs used in [18] are not permanently used during the normal operation of the converter. In [20], however, the reserved SMs are often employed. This strategy controls the MMC with some hot redundant SMs based on the carrier based pulsewidth modulation (CB-PWM). All of the SMs work in the operating and standby modes in a specific order.

The MMCs are well-suited for hardware-based techniques due to their modular topology [16]–[19]. However, not much effort is made to modify the modulation technique to exploit some of the inherent merits of MMCs [21]. The works in [22] and [23] are a few examples of FT methods, which modify the modulation. In [23] and [24], FT methods based on the CB-PWM are reported. In these papers, the references are modified to generate balanced phase voltages. In [25], an FT scheme based on fundamental phase compensation (FPSC) PWM is presented. The space vector modulation (SVM) is another widely used modulation technique for MLC [26]. However, there are few studies for MMCs controlled by the SVM [26]–[30]. In [28] and [29], an SVM method with capacitor voltage balancing and circulating current suppression (CCS) is presented; however, the implementation of this method is very complicated. In [27], a dual-SVM method for the MMC is proposed; however, this work does not employ any current suppression and capacitor

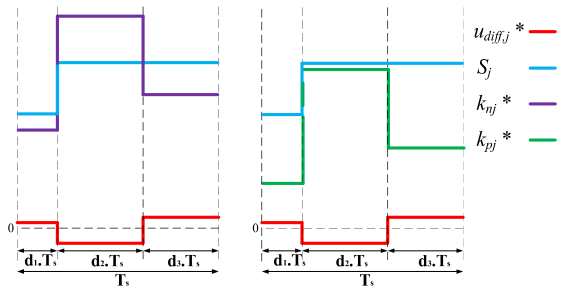


Fig. 1. CCS of phase *j* by using the modified switching states generated for an example difference voltage.

voltage control. Another work [30] maximizes the achievable voltage levels, which leads to better control of the capacitor voltage, circulating current, and common-mode voltage reduction. Although researchers have developed some valuable SVM methods for the MMCs, no effort has been made to control the converter in a faulty condition by adopting the SVM technique. For the other ML topologies however, a few FT strategies based on SVM have been reported [31]–[33]. The strategy proposed in [32], for instance, bypasses the faulty cell and utilizes the redundant switching states via SVM to generate balanced converter voltages. In [33], the idea of FPSC has inspired the authors to define a new space vector diagram for the SVM by introducing a new *abc* set of axes with arbitrary phase shifts.

The purpose of this paper is to propose a new control-based FT strategy for an MMC with bypassed faulty SMs. The proposed FT strategy generates balanced line voltages without employing auxiliary SMs or bypassing any SMs in the healthy phases, makes better use of the converter capacity, and generates line to the neutral (load) voltages with the same fundamental amplitude of normal operation.

II. Background

A. Modular Multilevel Converter

The circuit topology of the MMC used in this paper is illustrated in [19, Fig. 1]. As pictured, each leg of the MMC is comprised of an upper arm (*p*) and a lower arm (*n*), each made up of *N* SMs. The middle point of the upper and lower arms (V_a point in [19, Fig. 1]) is connected to the load. Each arm also incorporates an inductor ($L_{\rm arm}$) with an equivalent internal resistance ($R_{\rm arm}$). Each SM is comprised of a standard half-bridge and a capacitor (*C*). The capacitor can be placed in the circuit or bypassed using the half-bridge switches. Accordingly, by labeling the input terminal voltage of each SM as u_c, the output terminal voltage of each SM can be made equal to zero (SM is said to be OFF) or u_c (SM is said to be ON). In almost all applications, if the voltage drops in the circuit are neglected, the voltage of all SM capacitors are regulated ideally to $u_c = V_{\rm dc}/N$, where *N* is the number of SMs per arm. Therefore, the upper arm voltages ($u_{\rm pa}$, $u_{\rm pb}$, $u_{\rm pc}$) and lower arm voltages ($u_{\rm na}$, $u_{\rm nb}$, $u_{\rm nc}$) can be controlled by controlling the number of ON SMs in each arm. For simplicity, all of the converter voltages are normalized to $V_{\rm dc}$ and the voltage values are given in per unit (p.u.) terms. According to this convention, the voltage levels generated by phases of the converter (0, $V_{\rm dc}/N$, $2V_{\rm dc}/N$, ..., $V_{\rm dc}$) are normalized to 0, 1/*N*, 2/*N*, ..., 1 in p.u. terms.

B. Conventional SVM

The SVM method generates the switching signals based on the instantaneous position of a rotating reference vector in the voltage vector space of the converter. The space vector diagram of the $(N+1)$-level converter is illustrated in Fig. 2. Each dot in this figure represents a voltage vector [33]. The voltage vectors are related to converter phase voltages. The relationship in the *a-b-c* and stationary α-β reference frames is [33]

$$\vec{V} = V_{\rm ag} + V_{\rm bg}e^{j\frac{2\pi}{3}} + V_{\rm cg}e^{-j\frac{2\pi}{3}} = V_{\alpha g} + jV_{\beta g} \tag{1}$$

where $V_{\rm ag}$, $V_{\rm bg}$, and $V_{\rm cg}$ are the phase voltages of the converter in the *a-b-c* reference frame and $V_{\alpha g}$ and $V_{\beta g}$ are the phase voltages in a stationary α-β reference frame. These voltages are related to the switching states (S_a, S_b, S_c) according to [33]

$$\begin{bmatrix} V_{\rm ag} \\ V_{\rm bg} \\ V_{\rm cg} \end{bmatrix} = \left(\frac{1}{N}\right) \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{2}$$

$$\begin{cases} V_{\alpha g} = \frac{1}{3N}(2S_a - S_b - S_c) \\ V_{\beta g} = \frac{1}{N\sqrt{3}}(S_b - S_c) \end{cases}. \tag{3}$$

The switching states S_a, S_b, and S_c are defined for the "a," "b," and "c" phases, respectively. Since the voltage levels generated by phases of the converter in p.u. are 0, 1/*N*, 2/*N*, ..., 1, then, according to (2) each switching state has the possible values of 0, 1, 2, ..., *N* in order to represent the switching levels. Note that some switching states are redundant meaning that they produce the same vectors. The rotating reference vector is illustrated in [33, Fig. 1] in red color. This vector can be defined as

$$\vec{V}^* = \frac{3}{2}Me^{jwt} \tag{4}$$

where *M* is the modulation index and *wt* is the phase angle of the phase voltages. According to (4), in conventional SVM the reference vector follows a circular path as illustrated in [33, Fig. 1]. The SVM algorithm finds the three nearest voltage vectors to the reference vector ($\vec{V}_x$, $\vec{V}_y$, and $\vec{V}_z$ in [33, Fig. 1]) in each step and switches between the three identified voltage vectors during one switching period ($T_{\rm sw}$). The amount of time spent at each vector (T_x, T_y, T_z) is found from [33]

$$\begin{bmatrix} {\rm Re}\{\vec{V_x}\} & {\rm Re}\{\vec{V_y}\} & {\rm Re}\{\vec{V_z}\} \\ {\rm Im}\{\vec{V_x}\} & {\rm Im}\{\vec{V_y}\} & {\rm Im}\{\vec{V_z}\} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} T_x \\ T_y \\ T_z \end{bmatrix} = \begin{bmatrix} T_{\rm sw} \times {\rm Re}\{\vec{V^*}\} \\ Tsw \times {\rm Im}\{\vec{V^*}\} \\ T_{\rm sw} \end{bmatrix}. \tag{5}$$

Finally, SVM algorithm decides on the sequence of switching between the three voltage vectors and chooses one switching state among the redundant states for generating each voltage vector. In this paper, the switching sequence selection is based on generating symmetrical phase voltages for the CCS purposes.

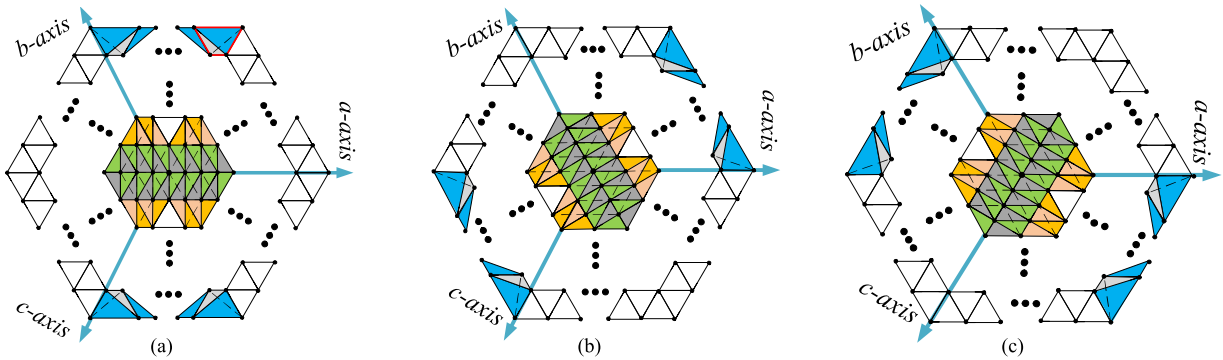


Fig. 2. Elaborated space diagram and all of its possible space vectors for a four-level converter one faulty cell in (a) phase "a," (b) phase "b," and (c) phase "c."

C. Circulating Current Suppression

The circulating current in MMC is caused by the variations of the SM capacitor voltages. These current has almost no effect on ac-side of the MMC and should be suppressed to have a higher efficiency. In [28] and [29], Deng *et al.* proposed an SVM scheme for MMC that features a CCS method. The following section is a modified adaptation of the CCS method in [28], applied to the $(N+1)$-level MMC of [19, Fig. 1]. According to the Kirchhoff's voltage law (KVL), converter's voltage in phase j can be defined as

$$\begin{aligned} V_j &= 1 - U_{\rm pj} - \frac{L_{\rm arm}}{V_{\rm dc}}.\frac{di_{\rm pj}}{dt} - \frac{R_{\rm arm}.i_{\rm pj}}{V_{\rm dc}}V_j \\ &= U_{\rm nj} + \frac{L_{\rm arm}}{V_{\rm dc}}.\frac{di_{\rm nj}}{dt} - \frac{R_{\rm arm}.i_{\rm nj}}{V_{\rm dc}} \end{aligned} \tag{6}$$

where $U_{\rm pj} = u_{\rm pj}/V_{\rm dc}$ and $U_{\rm nj} = u_{\rm nj}/V_{\rm dc}$ are the upper and lower arm voltages in the p.u. system. From (6) and from [19, Fig. 1] where $i_j = i_{\rm pj}$–$i_{\rm nj}$, V_j is derived as

$$\begin{aligned} V_j &= V_j^* - \frac{L_{\rm arm}}{2V_{\rm dc}}.\frac{di_j}{dt} - \frac{R_{\rm arm}.i_j}{2V_{\rm dc}} \\ V_j^* &= \frac{1 - U_{\rm pj} + U_{\rm nj}}{2} \end{aligned} \tag{7}$$

where V_j^* is called the modulation voltage in phase j. By substituting the modulation voltages in (1), the rotating reference of the SVM method can be calculated. Defining $I_{{\rm diff},j} = (I_{\rm pj} + I_{\rm nj})/2$, the upper and lower arm currents can be found by adding $I_{,j}/2$ to $I_{{\rm diff},j}$ and subtracting $I_{,j}/2$ from $I_{{\rm diff},j}$. Then, based on KVL, the $I_{{\rm diff},j}$ can be calculated by [34]

$$\frac{L_{\rm arm}}{V_{\rm dc}}.\frac{di_{{\rm diff},j}}{dt} + \frac{R_{\rm arm}.i_{{\rm diff},j}}{V_{\rm dc}} = \frac{1 - (U_{\rm pj} + U_{\rm nj})}{2} = U_{{\rm diff},j} \tag{8}$$

where $U_{{\rm diff},j}$ is called the difference voltage of phase j in p.u. system. By controlling this difference voltage in this equation, the $I_{{\rm diff},j}$ is restrained in phase j. The circulating current in phase j is $I_{zj} = I_{{\rm diff},j} - I_{\rm dc}/3$. Therefore, to suppress the circulating current in each instant, $I_{{\rm diff},j}$ should be driven to $I_{\rm dc}/3$. By careful manipulation of the previous relations, we can reach $I_{{\rm p},j} = I_j/2 + I_{zj} + I_{\rm dc}/3$, and $I_{n,j} = -I_j/2 + I_{zj} + I_{\rm dc}/3$. On the other hand, the purpose of circulating current control method is to set $I_{zj} = 0$ by eliminating I_{zj}, $I_{\rm pj} = I_j/2 + I_{\rm dc}/3$ and $I_{\rm nj} = -I_j/2 + I_{\rm dc}/3$. It must be noted that $I_{\rm pj}$ and $I_{\rm nj}$ contain two different ac components $(\pm I_j/2)$ on top of a common dc component $(I_{\rm dc}/3)$. Thus, if the circulating current is successfully eliminated, $I_{\rm pj}$ and $I_{\rm nj}$ will be two currents with the same average value $(\widehat{I}_{\rm pj} = \widehat{I}_{\rm nj})$, and maximum $(I_{pj_{\rm maximum}} = I_{nj_{\rm maximum}})$ and minimum $(I_{pj_{\rm minimum}} = I_{nj_{\rm minimum}})$ values. Otherwise (if the current suppression method is not employed), these currents will have the same average value but the maximum and minimum values will not be the same anymore. As a result, without the CCS method, the currents in the upper and lower arms will be significantly different. This means that the currents through the capacitors in the lower and upper arms charge the capacitors with different rates; however, the average of the capacitor voltages is still the same. Thus, the FT strategy still can be implemented without the circulation current suppression method: however, the THD quality of the generated waveforms will be negatively affected by the circulating current. In addition, without CCS, the ratings of the MMC components and converter losses are increased significantly [7], [35].

By denoting the number of ON SMs in the upper/lower arms as $k_{\rm pj}/k_{\rm nj}$, the voltage across the upper arm can be formulated as $U_{\rm pj} = k_{\rm pj}/N$, while the voltage across the lower arm is $U_{\rm nj} = k_{\rm nj}/N$. Then, the modulation voltage in (1) and (7) can be rewritten as

$$V_j^* = \frac{1}{N}S_j; \quad \text{and} \quad V_j^* = \frac{1}{2} - \frac{k_{\rm pj}}{2N} + \frac{k_{\rm nj}}{2N}. \tag{9}$$

Moreover, adding $U_{\rm nj} = k_{\rm nj}/N$ to the both sides of (8) yields

$$U_{{\rm diff},j} + \frac{k_{\rm nj}}{N} = \frac{1 - (U_{\rm pj} + U_{\rm nj})}{2} + U_{\rm nj} = V_j^* = \frac{1}{N}S_j. \tag{10}$$

Thus, the revised number of ON SMs in the upper and lower arms to suppress the circulating current can be calculated from

$$k_{\rm nj}^* = S_j - N.U_{{\rm diff},j}^*; \quad k_{\rm pj}^* = N - S_j - N.U_{{\rm diff},j}^*. \tag{11}$$

Fig. 1 shows the implementation of (11) for generating the switching voltages in the MMC arms.

D. Voltage Balancing

Once the voltages *Vx*, *Vy*, and *Vz* ([33, Fig. 1]) and the duty cycles *dx*, *dy*, and *dz* are determined by (5), specific set of

SMs should be chosen to be turned ON to maintain the voltage balance of the capacitors. The capacitor voltage of SMs and the arm currents can be measured in each sampling time and then a sorting algorithm can be used to choose the proper SMs to be turned ON [2], [35]. In this paper, a sorting algorithm is used for voltage balancing of the MMC [35]. In order to select the proper SM with the highest or lowest voltage, all of the SM voltages in one arm have to be sorted. The basic principles of the voltage-balancing algorithm are as follows [2], [35].

1) According to the generated voltage states (*Vx*, *Vy*, and *Vz*) in the previous part, the number of required ON SMs per the upper and lower arms must be calculated to keep the number of ON SMs equal to *N* SMs.
2) Considering the arm current direction, during the capacitors charging (or discharging) period the required number of SMs (three in our case) with the lowest (or highest) u_c must be ON.

The sorting method ensures the capacitor voltages in each arm to be identical. Together with the current control loops, it makes the capacitor voltages of different arms to be also balanced, without requiring large capacitors.

III. Proposed FT SVM Method

In this section, an SVM-based FT technique for an unbalanced MMC with bypassed SMs is proposed. The proposed SVM technique uses a reformed space vector diagram to generate phase voltages with equal amplitudes that have different number of levels. The reformed space vector diagram for the proposed method is structured according to the modified switching states of the faulty MMC using (1). As mentioned, the voltage levels generated by the converter are 0, 1/*N*, 2/*N*, ..., 1 p.u. In the event of a fault in one of the phases, the defective SM is bypassed using the bidirectional SCR switch between SM terminals A and B (shown in [19, Fig. 1]). In this case, the faulty arm of that phase consists of $N-1$ operative SMs, while the healthy arm consists of *N* operative SMs. In this condition, the faulty phase of the MMC fails to operate as normal condition and cannot generate one of the *N* feasible voltage levels. The $(N-1)$ voltage levels in faulty phase along with *N* voltage levels in healthy phases are substituted in (1) to shape the space vector diagram of the faulty converter. Then, the generated space vector diagram is not symmetric around the faulty phase axis, which results in an asymmetrical phase voltage containing a large undesirable dc-offset component in the faulty phase. Thus, unlike some of the PWM-based FT methods [16], [35], the number of operative SMs in the upper and lower arms must be equal in SVM methods to generate symmetrical waveforms. As a result, one operative SM in the healthy arm must be bypassed. In this condition, the faulty phase is not able to generate all the normal voltage levels (0, 1/*N*, 2/*N*, ..., 1) anymore. As a result, the possible switching states for the faulty phase will be limited to (0, 1/(*N* − *1*), 2/(*N* − *1*), ..., 1). To generate the new space vectors, all the possible switching states (S_a, S_b, and S_c) in the faulty condition are substituted in (2) to find all the possible voltage states (V_{ag}, V_{bg}, and V_{cg}) in the faulty condition. Then, these voltages are substituted in (1) to find the new space vectors. For the event of a faulty SM in phases a, b, or c of the MMC, the restructured space vector diagrams created using (1) are shown in Fig. 2(a), (b), and (c), respectively. As illustrated in Fig. 2, the space vector diagrams for the faulty converter no longer resemble the conventional space vector diagram used by traditional SVM algorithms as depicted in [33, Fig. 1].

There are three key distinctions to the new space vector diagrams. First, comparing to the conventional space vectors (dots in [33, Fig. 1]), the location of some new space vectors (dots in Fig. 2) have been altered. This is because fewer voltage levels are generated by the faulty phase of the MMC. Second, since the distances of most of these new space vectors from each other are no longer equal (unlike the conventional MMC), some of the shaped triangles in the new space vector diagrams are not equilateral triangles anymore [the colored triangles in Fig. 2(a)–(c)]. There are some dashed lines in the space vector diagrams of Fig. 2(a)–(c). These dashed lines make-up more nonequilateral triangles that cannot be easily highlighted in Fig. 2 since their positions overlap with colored ones. For example, in Fig. 2(a), one quadrilateral is marked by its four red sides. Two of the triangles within this quadrilateral are colored cyan and light gray. Besides these two triangles, we can imagine two more triangles, which are separated by the dashed line. But, this does not affect the selection of the three nearest vectors to the tip of rotating reference. Indeed, by (5), the three nearest vectors can be calculated in the same procedure. Third, unlike the conventional case, some of the redundant states are mapped to several distinct space vectors. It means for some redundant states, several distinct space vectors are generated using (1). Namely, in Fig. 3(a) that shows a standard space vector diagram for a four-level converter, seven space vectors are identified along the *a*-axis with dots. Considering the redundancies, 16 switching states exist that could be used to generate these seven space vectors. These switching states are also shown in Fig. 3(a) in parenthesis. However, using (1) to generate new space vectors in faulty phase "a" leads to 11 vectors along the *a*-axis, identified by dots in Fig. 3(b). The corresponding switching states to the new voltage vectors are also shown in Fig. 3(b) in parenthesis. As illustrated in this figure, each voltage vector is only realizable using one switching state. The number of switching states is reduced from 16 to 12 due to missing voltage level in the faulty phase "a."

The external vertices of the hexagonal space vector diagram are shown by the red dots in Fig. 3(a) and (b) for the normal and faulty conditions. As pictured, in the event of a fault, the coordination of these vertices remains the same. Thus, the areas of the two hexagonal space vectors remain equal, which means compared to the healthy MMC, the faulty MMC will be able to deliver the same amount of power to the load. The new path for the rotation of the reference vector is found by transforming the desired three-phase voltages in the faulty condition to the stationary α-β reference frame. Considering the previous example of one bypassed SM per arms in phase "a" for a certain fault scenario, one might assume the amplitude of voltage of phase "a" will be reduced. However, in reality after a transient phase and charging up the SM capacitors, the amplitude of the voltage generated by phase "a" will converge to the same value as the healthy phases but with reduced voltage levels. Therefore, the

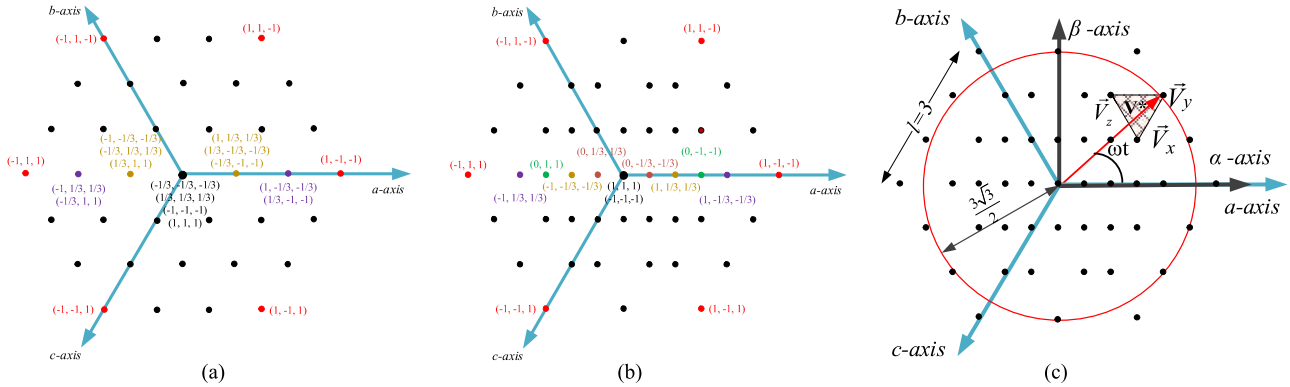


Fig. 3. Space vectors of the MMC and switching states of some of these vectors. (a) In normal operation of the MMC. (b) In the event of a fault in phase "a." (c) Phase "a" with its circulating path and three nearest vectors in one sampling instance.

desired three-phase voltages that the converter needs to generate in the faulty condition are (normalized to $V_{\rm dc}$)

$$\begin{cases} V^*_{\rm ag} = M \times \cos(wt) \\ V^*_{\rm bg} = M \times \cos(wt - \alpha) \\ V^*_{\rm cg} = M \times \cos(wt + \alpha) \end{cases}. \tag{12}$$

An *abc* to α-β transformation is required to transform the set of three-phase voltages in (12) to the stationary α-β reference frame. The standard α-β transformation is used for this purpose

$$\begin{bmatrix} V^*_{\alpha g} \\ V^*_{\beta g} \\ V^*_{0g} \end{bmatrix} = \begin{bmatrix} 1 & 0.5 & 0.5 \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V^*_{\rm ag} \\ V^*_{\rm bg} \\ V^*_{\rm cg} \end{bmatrix}. \tag{13}$$

Substituting (13) in (12) yields the desired voltages in the stationary α-β reference frame

$$\begin{cases} V^*_{\alpha g} = \frac{3}{2} M \cos(wt) \\ V^*_{\beta g} = \frac{3}{2} M \sin(wt) \end{cases} \tag{14}$$

which are same as the voltage reference of (4) in a normal converter. This equation describes a circular path in the stationary α-β axes, which is shown in Fig. 3(c) in red. Other than restructuring the space vector diagram, the rest of the modified SVM implementation remains the same as the conventional SVM. As illustrated in Fig. 3(c), the modified SVM algorithm needs to find the three nearest voltage vectors to the reference vector in each step and switch between the three identified voltage vectors during one switching period ($T_{\rm sw}$). The amount of time spent at each space vector can be found from (5) similar to conventional SVM. As mentioned previously, by using (1), some of the redundant states generate distinct space vectors for the faulty converter. Consequently, the three identified nearest voltage vectors can be realized each with a unique converter switching state; meaning that the SVM algorithm is no longer required to choose an appropriate switching state among the redundant states for a space vector. In fact, in the proposed method, the state redundancy capacity of the converter is leveraged for the FT operation of the converter to squeeze more voltage vectors along the circular path of the reference vector. Using the proposed method, in some cases, the three nearest voltage vectors no longer shape equilateral triangle. However, the shape of

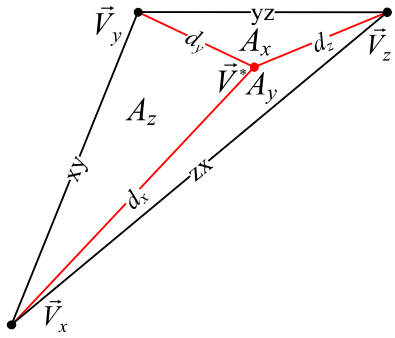


Fig. 4. Three nearest space vectors to the reference vector.

these triangles is not important for calculating the time spent at each of the vector. As mentioned above, the procedure for calculating the time spent at each vector is the same as conventional SVM. In (5), the coordinates of three nearest vectors ($\vec{V}_x$, $\vec{V}_y$, and $\vec{V}_z$), which are not necessarily vertices of an equilateral, are used in the coefficients matrix and the coordinates of the reference vector is used in the constant matrix of the system. As long as the reference vector is located inside this triangle, this system of equations has a valid solution that satisfies the practical constraints ($0 \le T_i \le T_s, \quad i = x, y, z$). Additionally, the time spent at each vector can be calculated using the distances of each space vector to the other vectors and the reference vector

$$T_i = \frac{A_i}{A_x + A_y + A_z} \times T_{\rm sw} \quad \text{where} \quad i = x, y, z \tag{15}$$

where A_x, A_y, and A_z are the areas shaped from the distances of $\vec{V}_x$, $\vec{V}_y$, and $\vec{V}_z$ to the reference vector. These areas can be seen in Fig. 4. These areas can be easily calculated by using the distances shown in Fig. 4. For example, A_x is equal $\sqrt{p(p-d_x)(p-d_y)(p-yz)}$, where p is half the perimeter ($p = (d_x + d_y + yz)/2$). From this engineering solution, it can be concluded that finding a set of solutions does not depend on the shape of triangle.

Finally, it is worth mentioning that since the space vectors in the faulty MMC lose their inherent redundancies in the vector diagram that is constructed by the modified FT strategy, each

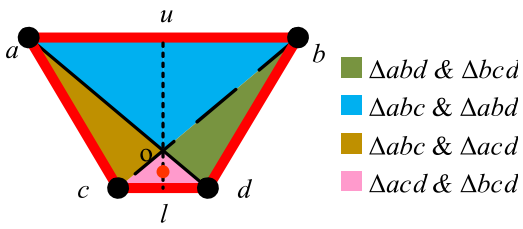


Fig. 5. One example of the triangular redundancy that is achieved by the proposed FT SVM method.

of the previously redundant switching states is now mapped to a unique switching vector. This results in more space vectors comparing with the traditional space vectors in the balanced operation of the converter. The more space vectors shape more triangles in the converter's space diagram. As mentioned before, some of these triangles overlap together and this causes the redundancy of triangles. For instance, consider the quadrilateral of the previous example, which is demonstrated with more detail in Fig. 5. In this quadrilateral, four distinct parts are distinguished by four colors. Every single point in any of the parts is located within two overlapping triangles. As an example, if the tip of the rotating reference vector is located in the Δodb, the three nearest vectors to this point shape either Δabd or Δbcd triangles. In this case, by using (5) the exact coordination of three nearest vectors can be found. However, in some cases, the locations of these three vectors are not unique anymore. The red point in Fig. 5 shows an example of this situation. This point is located within Δacd and Δbcd triangles. Thus, the space vectors "c" and "d" are two nearest vectors and the third one can be one of the "a" and "b" vertices. This is because of equal distances of vectors "a" and "b" from the red point. Based on the desired switching strategy, one of these vectors can be selected as the third vector.

At the end of this part, a flowchart for systematic implementation of the proposed method is given in Fig. 6.

IV. Investigation of New FT Strategy

In this section, the performance of the proposed SVM algorithm is evaluated using investigations on two MMCs with different numbers of SMs in each arm. In the first investigation, several simulations have been carried out on a 10-level 3-phase MMC (nine series connected SMs in [19, Fig. 1]). In the second investigation, the proposed fault tolerant strategy is utilized to revamp the performance of a prototype 4-level MMC ($N = 3$) in the event of a fault in phase "a" (see Fig. 7). In this setup, the dc-side terminal voltage of converter is equal to 400 V and the output terminals of the MMC are connected to the three-phase inductive load. The proposed method is implemented using TMS320F28335 digital signal processor. The parameters of the system under the test are listed in Table I.

In the first investigation, the waveforms for the normal operation of the MMC in Fig. 8 are provided to offer a reference for comparison of the results. By comparing the phase voltages in Fig. 8(a), it can be inferred that these voltages are not balanced.

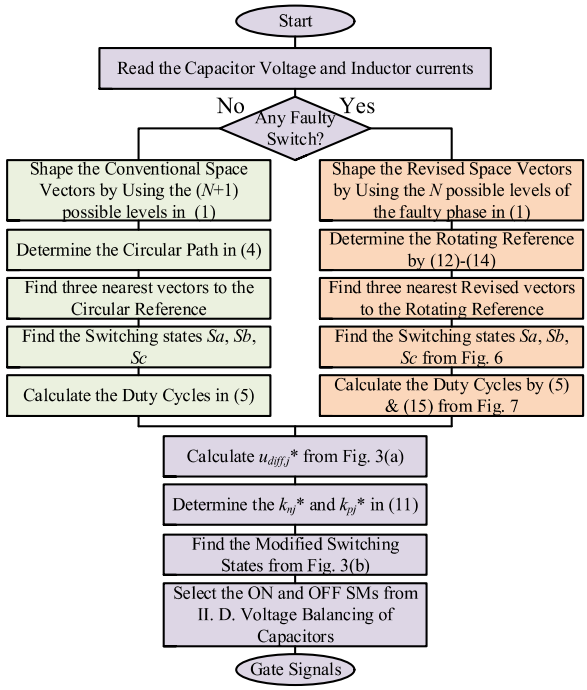


Fig. 6. Flowchart for systematic implementation of the proposed method.

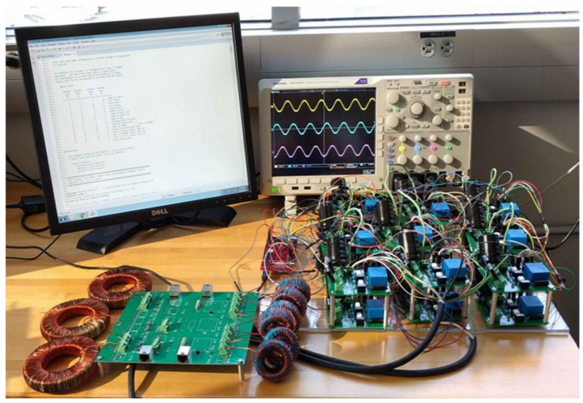
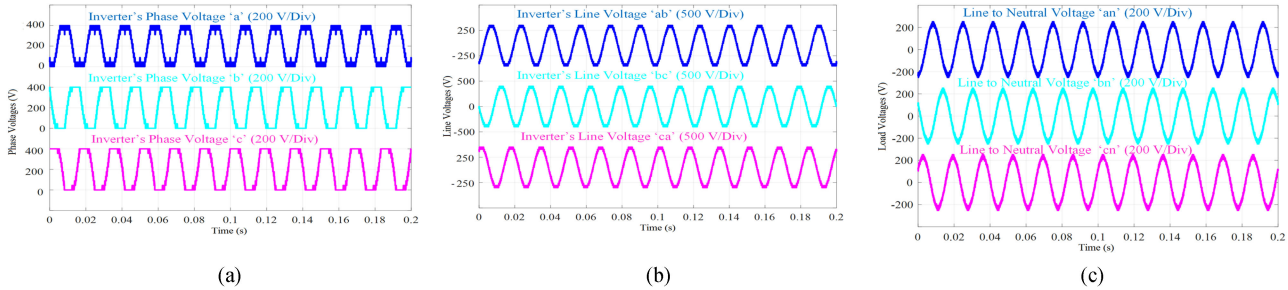


Fig. 7. Prototype of three-phase, MMC, and TMS320F28335 controller.

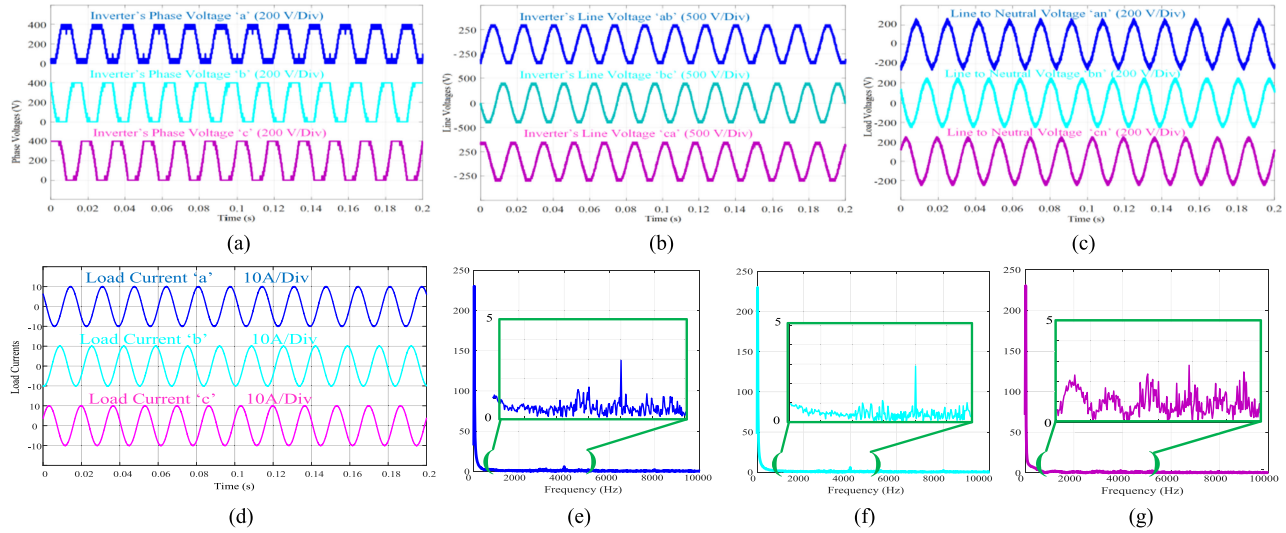
TABLE I
System Parameters

Description	Parameter	Value	Unit
Arm inductance	L_{arm}	1	mH
Arm resistance	R_{arm}	0.2	Ω
SM capacitor	C	1.2	mF
Capacitor Rated Voltage	u_C	250	V
Load inductance	L_{load}	8.6	mH
Number of SMs per Arm	N	3	-
Load resistance	R_{load}	22.8	Ω
DC side voltage	V_{dc}	400	V
Fundamental frequency	F	60	Hz
Rated Power	P_{out}	3.5	kW
DC side voltage	$V_{L\text{-}L}$	400	V
SVM sampling time	T_{s_SVM}	250	μs



(a) (b) (c)

Fig. 8. 10-level MMC voltages during normal (healthy) operation of the converter. (a) Phase voltages. (b) Line voltages. (c) Load voltages $V_{\rm an}$, $V_{\rm bn}$, and $V_{\rm cn}$.



(a) (b) (c) (d) (e) (f) (g)

Fig. 9. Operation of the MMC with nine SMs during faulty condition. (a) Converter phase voltages. (b) Line voltages. (c) Load voltages $V_{\rm an}$, $V_{\rm bn}$, and $V_{\rm cn}$. (d) Load currents. (e) $V_{\rm an}$ harmonic spectrum. (f) $V_{\rm bn}$ harmonic spectrum. (g) $V_{\rm cn}$ harmonic spectrum.

In normal operation, the amplitude of the fundamental component of the converter's phases "a," "b," and "c" are calculated from Fig. 8 as 219.3, 237, and 237 V, respectively. However, all three load and line voltages are 230.8 and 399.8 V, respectively. According to the harmonic spectrum of the load and line voltages, the THDs of the voltages are 6.7% and the phase shifts are 120°. The generated phase voltages of the converter after activating the proposed FT method are shown in Fig. 9. In the postfault condition, due to bypassing of one SM per each arm in phase "a," this phase generates nine voltage levels, while the healthy phases keep generating all ten voltage levels. To verify generation of balanced line voltages in the postfault condition, the line voltages are plotted in Fig. 9(b). Additionally, the load voltages are shown in Fig. 9(c). According to Fig. 9(e)–(g), all three load and line voltages are 399.8 and 230.8 V. According to the harmonic spectrum of the load and line voltages, the THDs of the voltages are slightly increased to 7.1%; however, the phase shifts are exactly 120°. To get a better idea about the converter operation, the load currents in the event of a single faulty phase are given in Fig. 9(d). As pictured, the amplitude of the three waveforms in the postfault operation are equal (10 A) and the phase shifts are exactly 120°. However, the THD of the current is slightly increased from 0.05% to 0.07% due to fault.

In the second investigation, the waveforms for the normal operation of the MMC with three series-connected SMs in each arm are provided in Fig. 10 to provide a reference for comparison. The amplitudes of the fundamental component of the converter's phases "a," "b," and "c" are calculated from Fig. 10 for normal operation as 218.13, 236, and 237 V, respectively. However, all three load and line voltages are 230.8 and 399.9 V, respectively. From analyzing the harmonic spectrums of the waveforms, the THD of the load voltages are 19% and the phase shifts are 120°. The generated phase voltages of the converter after activating the proposed FT method are shown in Fig. 11. In the postfault condition, due to the bypassed SMs in phase "a," this phase generates three voltage levels. According to Fig. 11, however, the amplitude of voltage of phase "a" is still equal to 218 V, although the number of the voltage levels in this phase is reduced. According to harmonic spectrum given in Fig. 11(e)–(g), the amplitudes of the load and line voltages are all equal to 230.8 and 399.8 V, respectively. From analyzing the harmonic spectrums, the THD of the load voltages are 21%, 19%, and 21%, respectively, and the phase shifts are 120°. Again, the load currents in the event of a single faulty phase are given in Fig. 11(d). As pictured, the amplitude of the three waveforms in the postfault operation are equal (10 A) and the

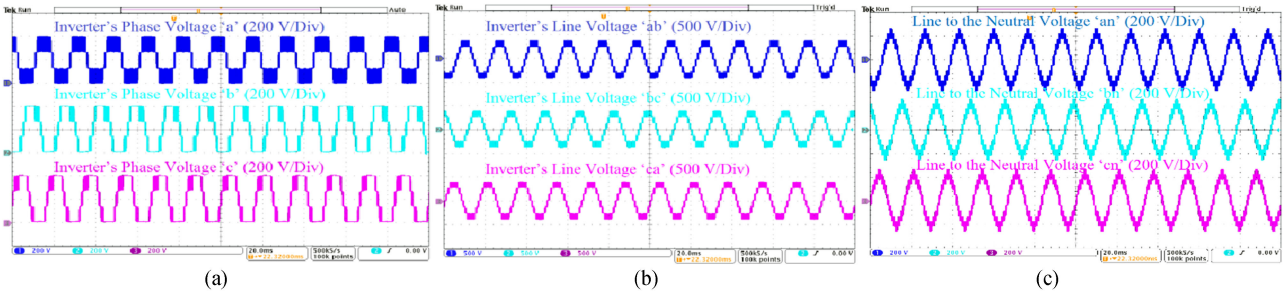


Fig. 10. Four-level MMC voltages during normal (healthy) operation of the converter. (a) Phase voltages. (b) Line voltages. (c) Load voltages $V_{\rm an}$, $V_{\rm bn}$, and $V_{\rm cn}$.

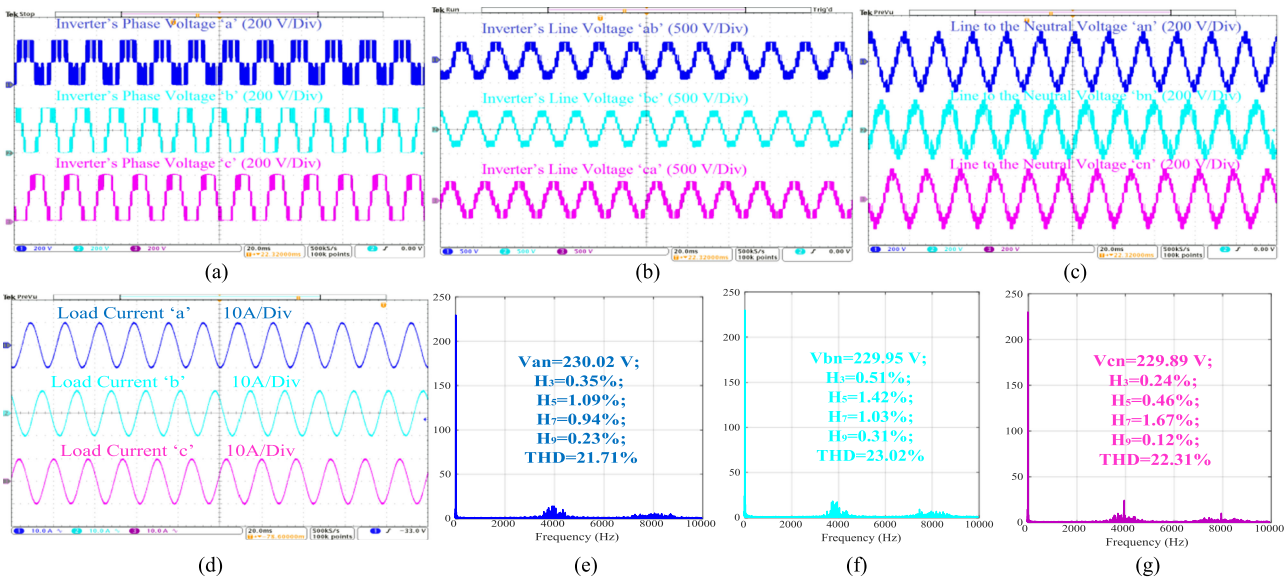


Fig. 11. Operation of the prototype MMC with three SMs during faulty condition. (a) Converter phase voltages. (b) Line voltages. (c) Load voltages $V_{\rm an}$, $V_{\rm bn}$, and $V_{\rm cn}$. (d) Load currents. (e) $V_{\rm an}$ harmonic spectrum. (f) $V_{\rm bn}$ harmonic spectrum. (g) $V_{\rm cn}$ harmonic spectrum.

phase shifts are exactly 120°. However, the THD of the current is slightly increased from 1.3% to 1.5% due to fault occurrence.

Finally, Fig. 12 analyzes the operation of the current suppression and voltage balancing methods. According to Fig. 12(f), the circulating currents in phases "a," "b," and "c" are respectively decreased to 10%, 15%, and 20% with the current suppression control. Before applying the CCS method, V_j^* is not revised based on Section II-C. Thus, the reference is generated regardless of the CCS goal and three nearest vectors are selected. Unlike the PWM methods, the generated phase voltages are different in the SVM method. If the CCS method is not employed, these different voltages result in different amplitudes of circulating currents, particularly, in the faulty phase that includes less operative SMs. Fig. 12(a)–(e) illustrates capacitor voltages of the upper arms and lower arms while the current suppression method is triggered. The rated dc voltage of capacitors in phase "a" of the converter is 200, while these voltages in two other phases are 133 V. By comparing the capacitors voltages of the lower and upper arms, it is observed that the charging and discharging rates are slightly different. This is due to the small circulating currents in the phases of the converter.

Note that the devices must be overdesigned in this approach. However, as the number of SMs increases, the percentage of needed overdesign decreases. For instance, in an MMC with N number of SMs per arm, the rated voltage for the switches and capacitors is $1/N$. In the event of a fault, the faulty cell is bypassed and $N-1$ SMs remain operative. So, the rated voltage in this case is increased to $1/(N-1)$. To find the increment in overdesign ratio we can write

$$\text{Overdesign Increment}\% = \left[\frac{1}{N-1} - \frac{1}{N}\right] / \left[\frac{1}{N}\right] = \frac{1}{N-1}\%. \quad (16)$$

Due to these overrated devices, the cost of using the proposed method is different from the conventional solution. In an MMC with a redundant SM for the fault tolerant purposes, the voltage of each SM capacitor is set to $V_c = 133.3$ V. For the safety concerns, the voltage rating of the capacitor is chosen as $1.25 * V_c = 166.6$ V, as provided in Table II. The voltage rating of the MOSFET is twice the rating of capacitors, equal to 330 V. In this design, each SM includes one voltage sensor, one gate

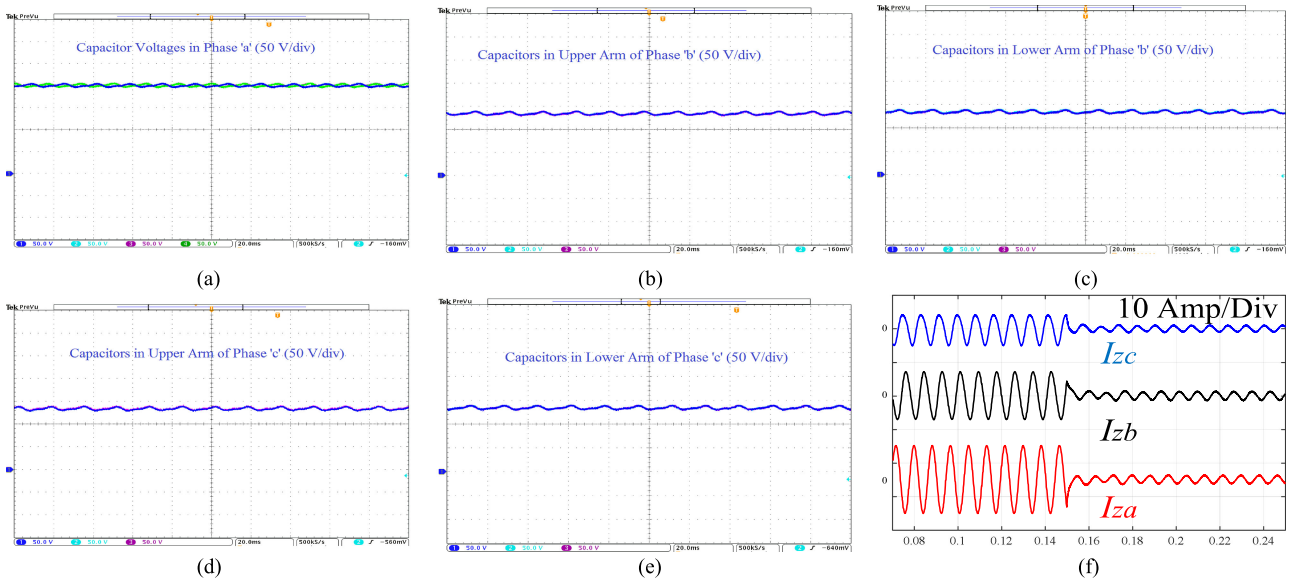


Fig. 12. Voltage over each SM's capacitor and the circulating currents in each phase. (a) Capacitors in phase "a." (b) Capacitors in upper arm of phase "b." (c) Capacitors in lower arm of phase "b." (d) Capacitors in upper arm of phase "c." (e) Capacitors in lower arm of phase "c." (f) Circulating currents.

TABLE II
REQUIRED PARTS FOR THE MMC WITH PROPOSED AND CONVENTIONAL METHODS

				Quantity per arm	
variable	**Part name**	**Price ($)**	**Description**	**Proposed**	**Conventional**
y_1	Voltage sensor	45.5	LV 20-P (LEM)	3	4
y_2	Gate driver circuit	25.5	-	3	4
y_3	Conditioning circuit	20	-	3	4
y_4	PCB	10	-	3	4
y_5	SM capacitor	3.3	CAP ALUM 1200UF 20% 160V (Nichicon)	0	4
y_6	SM capacitor	5.14	CAP ALUM 1200UF 20% 250V (Nichicon)	3	0
y_7	MOSFET N-CH	5.15	FKP330C-ND (Sanken)	0	8
y_8	MOSFET N-CH	9.56	FDH50N50-F133 (on-semiconductor)	6	0
y_9	inductor	20		1	1
y_{10}	Current sensor	24.8	LA 55-P (LEM)	1	1
y_{11}	Others	2	-	3	4

driving circuit, one signal conditioning circuit, one PCB, one SM capacitor, and two power MOSFETs.

Each arm contains one inductor and one current sensor. The conventional MMC includes three SMs plus one redundant SM for each arm. Hence, the cost for one arm is $4 \times (y_1 + y_2 + y_3 + y_4 + y_5 + 2y_7 + y_{11}) + y_9 + y_{10}$. In proposed method, if a fault occurs the remaining capacitor and power switches should withstand the dc-link voltage of 400 V. Hence, the voltage of the healthy SM capacitors will be equal to 200 V, and required rating of capacitor voltage is 250 V. This will also cause increment in rating of power switches accordingly. This trend is shown in Table II. The cost for one arm of MMC in the proposed method is $3 \times (y_1 + y_2 + y_3 + y_4 + y_6 + 2y_8 + y_{11}) + y_9 + y_{10}$. By using these two cost functions, a comparison has been performed for the prototype MMC with three SMs per arm. In MMC with one SM redundancy, although the rating of capacitor and power switches are less, but there is a need for four cells. The total cost for one arm in MMC with the conventional solution ($3068) is $512 (20%) more than the cost in the proposed method ($2556). In addition, the size of the system in the conventional solution is (4/3) 33.3% bigger than the proposed method. Finally, although the cost and size of the MMC converter with proposed method is less, the conventional solution may be preferred in the applications with no cost and size limitation. In these applications, since there is one redundant SM per arm, the proposed method can be employed to revamp the event of the double fault in one phase of the converter.

V. CONCLUSION

In this paper, a new FT strategy based on a modified SVM technique for improving the performance of an MMC converter under faulty conditions was proposed. Using the proposed method, the converter generated balanced line voltages, even with one or more faulty switches. Using the conventional FT strategy, the maximum achievable line voltages for a four-level MMC in the normal and faulty operations were the same. The proposed strategy can easily be implemented on various types of MMCs without limitation on the number of voltage levels.

REFERENCES

[1] B. Novakovic and A. Nasiri, "Modular multilevel converter for wind energy storage applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8867–8876, Nov. 2017.

[2] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[3] B. Li, Y. Zhang, G. Wang, W. Sun, D. Xu, and W. Wang, "A modified modular multilevel converter with reduced capacitor voltage fluctuation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6108–6119, Oct. 2015.

[4] A. Christe and D. Dujic, "Virtual submodule concept for fast semi-numerical modular multilevel converter loss estimation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5386–5294, Jul. 2017.

[5] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[6] A. Dekka, B. Wu, V. Yaramasu, and N. R. Zargari, "Dual-stage model predictive control with improved harmonic performance for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6010–6019, Oct. 2016.

[7] L. Ben-Brahim, A. Gastli, M. Trabelsi, K. A. Ghazi, M. Houchati, and H. Abu-Rub, "Modular multilevel converter circulating current reduction using model predictive control," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3857–3866, Jun. 2016.

[8] F. Deng, Y. Tian, R. Zhu, and Z. Chen, "Fault-tolerant approach for modular multilevel converters under submodule faults," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7253–7263, Nov. 2016.

[9] J. Mei *et al.*, "Balancing control schemes for modular multilevel converters using virtual loop mapping with fault tolerance capabilities," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 38–48, Jan. 2016.

[10] P. T. Lewis, B. M. Grainger, H. A. A. Hassan, A. Barchowsky, and G. F. Reed, "Fault section identification protection algorithm for modular multilevel converter-based high voltage DC with a hybrid transmission corridor," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5652–5662, Sep. 2016.

[11] A. Ghazanfari and Y. A. R. I. Mohamed, "A resilient framework for fault-tolerant operation of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2669–2678, May 2016.

[12] Q. Yang, J. Qin, and M. Saeedifard, "A postfault strategy to control the modular multilevel converter under submodule failure," *IEEE Trans. Power Del.*, vol. 31, no. 6, pp. 2453–2463, Dec. 2016.

[13] L. Hui, L. Poh Chiang, and F. Blaabjerg, "Review of fault diagnosis and fault-tolerant control for modular multilevel converter of HVDC," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 1242–1247.

[14] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *Proc. IEEE/PES Transmiss. Distrib. Conf. Expo*. 2008, pp. 1–16.

[15] P. Hu, D. Jiang, Y. Zhou, Y. Liang, J. Guo, and Z. Lin, "Energy-balancing control strategy for modular multilevel converters under submodule fault conditions," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5021–5030, Sep. 2014.

[16] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.

[17] G. T. Son *et al.*, "Design and control of a modular multilevel HVDC converter with redundant power modules for noninterruptible energy transfer," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1611–1619, Jul. 2012.

[18] G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Active redundant submodule configuration in modular multilevel converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2333–2341, Oct. 2013.

[19] G. Liu, Z. Xu, Y. Xue, and G. Tang, "Optimized control strategy based on dynamic redundancy for the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 339–348, Jan. 2015.

[20] K. Li, L. Yuan, Z. Zhao, S. Lu, and Y. Zhang, "Fault-tolerant control of MMC with hot reserved submodules based on carrier phase shift modulation," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6778–6791, Sep. 2017.

[21] Q. Yang, J. Qin, and M. Saeedifard, "Analysis, detection, and location of open-switch submodule failures in a modular multilevel converter," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 155–164, Feb. 2016.

[22] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug. 2005.

[23] P. W. Hammond and M. F. Aiello, "Multiphase power supply with series connected power cells with failed cell bypass," US5986909A, Google Patents, 2001.

[24] E. C. dos Santos and S. Sajadian, "Fault-tolerant DC-AC converter with split-wound coupled inductors," in *Proc. Brazilian Power Electron. Conf.*, 2013, pp. 30–35.

[25] P. Lezana and G. Ortiz, "Extended operation of cascade multicell converters under fault condition," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[26] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, 2003, vol. 3, pp. 1–6.

[27] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A space-vector PWM-based voltage-balancing approach with reduced current sensors for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2734–2745, May 2016.

[28] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "Space vector modulation method for modular multilevel converters," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, 2014, pp. 4715–4721.

[29] Y. Deng, M. Saeedifard, and R. G. Harley, "An optimized control strategy for the modular multilevel converter based on space vector modulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 1564–1569.

[30] Y. Deng, Y. Wang, K. H. Teo, M. Saeedifard, and R. G. Harley, "Optimized control of the modular multilevel converter based on space vector modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5697–5711, Jul. 2017.

[31] M. Aleenejad, H. Iman-Eini, and S. Farhangi, "Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters," *IET Power Electron.*, vol. 6, pp. 742–751, 2013.

[32] L. G. G. P. de Castro and M. B. R. Correa, "A fast space-vector algorithm for cascaded H-bridge converters under faulty conditions," in *Proc. 10th IEEE/IAS Int. Conf. Ind. Appl.*, 2012, pp. 1–7.

[33] M. Aleenejad, H. Mahmoudi, and R. Ahmadi, "Unbalanced space vector modulation with fundamental phase shift compensation for faulty multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7224–7233, Oct. 2016.

[34] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.

[35] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

Mohsen Aleenejad (S'15–M'17) received the B.S. degree in electrical engineering from Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 2010, the M.S. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2013, and the Ph.D. degree in electrical engineering from the Department of Electrical Engineering and Computer Science, The University of Kansas, Lawrence, KS, USA, in 2017.

He is currently a Postdoctoral Researcher with the Electrical and Computer Engineering Department, New York University, New York City, NY, USA. His research interests include power electronics and its applications in power grid systems.

Hamid Mahmoudi (S'15) was born in 1989. He received the B.Sc. degree in electrical engineering from Noshirvani University of Technology, Mazandaran, Iran, in 2011, and the M.Sc. degree in electrical engineering from Iran University of Science and Technology, Tehran, Iran, in 2014. He is currently working toward the Ph.D. degree in electrical engineering with the University of Kansas, Lawrence, KS, USA.

His research interests include design and control of power electronic converters, motor drives, multilevel converters, and solar energy systems.

Seyyedmahdi Jafarishiadeh (S'16) received the B.Sc. degree from Amirkabir University of Technology, Tehran, Iran, in 2010, and the M.Sc. degree from K. N. Toosi University of Technology, Tehran, Iran, in 2013, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical and computer engineering with the University of Kansas, Lawrence, KS, USA.

His research interests include power electronics, electric machines, storage systems, and renewable energy sources.

Reza Ahmadi (M'09) received the B.S. degree in electrical engineering from Iran University of Science and Technology, Tehran, Iran, in 2009, and the Ph.D. degree in electrical engineering from Missouri University of Science and Technology, Rolla, MO, USA, in 2013.

He is currently an Assistant Professor of Electrical and Computer Engineering with the University of Kansas, Lawrence, KS, USA. His research interests include modeling, design, and control of power electronic converters, electric-drive vehicles, and solar energy systems.