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Low-Noise Speed-Optimized Large Area CMOS Avalanche Photodetector for Visible Light Communication

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Abstract

Mean-gain and excess-noise measurements are presented for a 350 × 350 μm^2 P+/N-well/P-sub and a 270 × 270 μm^2 N-well/P-sub avalanche photodetectors fabricated using 0.13-µm CMOS technology. The active area of the P+/N-well/P-sub device was divided into multiple subsections to decrease transit time and increase speed. For the P+/N-well structure, remarkably low excess-noise factors of 4.1 and 4 were measured at a mean gain of 16 corresponding to a k value of approximately 0.1, using a 542 (633) nm laser. For a variant N-well/P-sub structure, excess-noise factors of 6.5 and 6.2 were measured at a mean-gain of 16 corresponding to a k value of approximately 0.3. The proposed CMOS APDs with high gain, low noise, low avalanche breakdown voltage (below approximately 12 V) and low dark-currents (approximately nA) would be attractive for low-cost optical receivers in visible-light communication systems.

SECTION I. Introduction

Silicon photonics is a promising technology for the realization of low-cost, low-noise, high-speed and high-sensitivity photodetectors in visible-light communication (VLC) systems. The VLC system is gaining momentum as a solution to provide gigabit-class (up to 3 Gb/s) connectivity of electronic devices in home and office environments [1]–[3]. Silicon avalanche photodiodes (APDs), with their inherent internal amplification mechanism and the resulting high-sensitivity, can offer an excellent photodetector choice for high path-loss VLC systems [3]. In addition, Si APDs with their low-noise characteristics can provide improved signal-to-noise ratio (SNR) in the VLC receiver. Specifically, Si is a very attractive material for APDs due to its low k value (<0.1), which results in a low excess-noise factor, F [4] –[18]. Additionally, careful device design and fabrication process can further improve the noise properties of Si APDs by reducing the thickness of the avalanche region [19]–[22].

More specifically, since VLC systems are an integral part of emerging smart-lighting concepts, there is a need for cost-effective and compact optical devices that enable VLC in such scenarios. The rapid advances in solid-state lighting and high-speed (∼5 GHz for 30 meters of distance) plastic optical fiber (POF) technology have been paving the way toward a low-cost and high-speed implementation of VLC optical transmitters [1]. Si APDs implemented on standard complementary-metal–oxide–semiconductor (CMOS) process can offer a low-cost, compact, and high-yield fabrication solution to VLC receivers for smart-lighting systems [23] –[26]. Additionally, a large-area CMOS APD can substantially ease the coupling of light from the wide-diameter step-index POF (typically with a core diameter of 1 mm), which normally requires bulky concentrators and optical alignment setups [2].

Although linear-mode speed-optimized CMOS APDs have been developed in the recent years, one of the main challenges in them is that they require high operating voltages (e.g., 35.25, 68.25, 83.5, 119.25 V) [2], [27]. While high-voltage (HV) CMOS process can also be utilized to implement integrated receivers including HV-APDs, the technology choice for high-speed receiver implementation is moving toward smaller gate length with low-

voltage (LV) CMOS nodes that offer optimized performance to analog/digital circuitry. A possible solution to retain the advantages of both technologies is to fabricate the APD in high-voltage process while the receiver circuits in LV-CMOS nodes. However, interfacing such high-voltage systems with low-voltage optical receiver circuitry increases implementation complexity. Therefore, it is beneficial to fabricate APDs in similar CMOS technology, as the receiver itself, to reduce implementation complexity of the entire system. Modern sub-micron CMOS processes employ increasingly higher doping concentration to achieve constant field scaling and thinner oxide layers in smaller device features for better performance. As a result, the highest voltage that can be applied without running into reliability issues in such technology also scales down. Since the allowed voltage levels in such CMOS-technology are low (e.g., ∼11 V in 0.13 -μm CMOS), special biasing circuitry must be utilized to operate such aforementioned high voltage APDs. In addition, low breakdown voltage APD benefits from low power operation and simple electrical bias circuitry. Therefore, it would be desirable to have a low-bias CMOS APD in a range compatible with the voltages allowed by CMOS circuitry. In this regard, a low operating-voltage (<11 V) P+/N-well APD was designed and fabricated using a 0.35-µm CMOS process [10] . However, the design yielded a high k value of 0.47, which resulted in a high excess-noise factor (e.g., F = 5.2 at 480/560/650 nm, and F = 3.9 at 380 nm, at a mean gain of 16). The APD also suffered from high dark currents (∼1 µA at the breakdown voltage of 10.8 V).

Recently, we have reported a speed-optimized, large-area P+/N-well/P-sub APD fabricated in 0.13-µm CMOS technology for the VLC applications [3]. This device was based on an earlier design, reported in [3], which helped overcome the speed limitation associated with a large active area [26]. The total area (350 × 350 μm^2) of the device reported in [3] was sub-sectioned into 20 × 20 μm^2 identical P+ regions inside an N-well. The outputs of the subsections were connected in parallel in order to achieve large bandwidth (6 GHz). The detection speed was increased as a result of the reduced transit time of diffusive carriers in the large-area CMOS APD. Measured dark-current, photo-current, simulated frequency response as well as the calculated mean-gain and excess-noise factor were reported for the P+/N-well/P-sub APD device [3].

In this work, we further investigate N-well/P-sub APD as well as the P+/N-well/P-sub APD device structures of the type reported in [3]. Specifically, we report here the measured dark-currents, capacitances, as well as the calculated and measured spectral responsivity, avalanche breakdown voltage, mean-gain, and excess-noise factor for both of the devices. The reported APDs exhibit low dark currents (in the range of nA) for a linear-mode avalanche breakdown voltage below 11 V. The investigated P+/N-well APD devices offer very low excess noise factors (4.1 and 4.0 using a 542 nm laser and a 633 nm laser, respectively, both at a mean gain of 16) with a low k value of 0.1. The reported excess-noise measurements are the lowest as compared to those for other reported CMOS APDs in the visible regime of the electromagnetic spectrum [7], [9]– [10], [12],[14]–[16].

SECTION II. Device Structure

The P+/N-well/P-sub and N-well/P-sub APD device structures considered here have been fabricated using IBM 0.13 -µm standard CMOS technology. Fig. 1(a) shows the die micrograph of the photodiode and the zoomed-in layout view is shown in Fig. 1(b) . Fig. 1(c) shows the large-area P+/N-well/P-sub APD. Note that this structure features sub-sectioned regions of P+ diffusion interlaid in a meshed configuration [3]. The advantage of such structure is the reduced diffusion distances of minority carriers that results in a smaller transit time and higher optical bandwidth [3], [26].

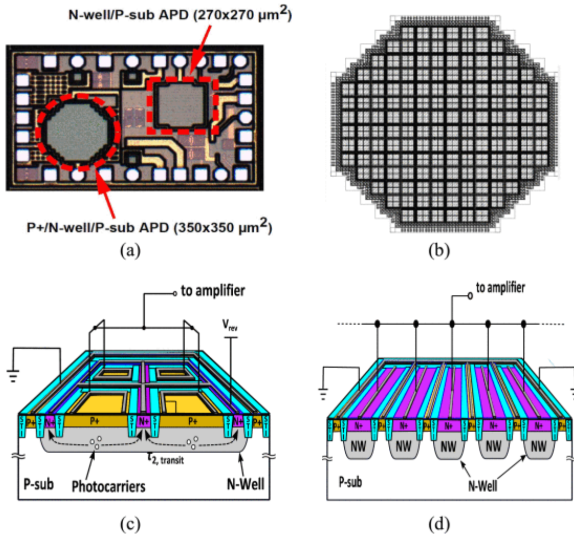


Fig. 1. Investigated silicon APDs fabricated in 0.13-µm CMOS technology: (a) die micrograph, (b) layout view showing 20×20 µm^2 sub-sections, (c) P+/N-well/P-sub structure (350×350 µm^2) with reduced transit time and (d) N-well/P-sub structure (270×270 µm^2). (a)–(c) are reproduced from [3].

Due to the large number of substrate and cathode contacts interlaced in such meshed structure, the substrate resistance for the photo-carriers also decreases. However, as described in [3] , the overall junction capacitance of the sub-divided structure remains almost the same as its conventional counterpart due to the equivalency of total active area. The P+/N-well/P-sub structure consists of a p-substrate (5×10^{15} cm^{-3}) layer, a 1.5-µm thick N-well (5×10^{17} cm^{-3}) layer, a 0.3-µm thick P+ (5×10^{19} cm^{-3}) layer and a 0.3-µm thick N+ (5×10^{19} cm^{-3}) layer. It is also assumed that the impurity concentrations follow a Gaussian profile at the edges of the specified regions, both in horizontal and vertical directions. The total area of the device is 350×350 µm^2, which is sub-sectioned into 20×20 µm^2 identical P+ regions inside an N-well. The active area is divided into a meshed array of P+ islands and the cathode electrode is inserted in-between for uniform distribution of bias voltage. A different type of N-well/P-sub APD structure is shown in Fig. 1(d) , which is comprised of N-well stripes inside P-substrate in an area of $\sim 270 \times 270$ µm^2 . The purpose of the striped structure is to pass metal density rules in this sub-micron technology and to reduce contact resistance of N-well and P-sub contacts. However, the opaque metal contacts resulting from the plurality of the N-well stripes cause partial shading of light. The structure consists of a p-substrate (5×10^{15} cm^{-3}) layer, a 1.5-µm thick N-well (5×10^{17} cm^{-3}) layer, a 0.3-µm thick P + (5×10^{19} cm^{-3}) layer and a 0.3-µm thick N+ (5×10^{19} cm^{-3}) layer. An N-well width of ~ 15 µm is chosen as a compromise between terminal resistance, parasitic capacitance and fill-factor. The shallow-trench-isolation (STI) is used around the P+ and N+ regions for both of the APD devices to prevent premature edge breakdown.

SECTION III. Modeling and Simulation Results

The dead-space multiplication theory (DSMT) [4], [5] was used to calculate the avalanche breakdown voltage, mean-gain and excess-noise factor for the APD devices. In the DSMT analytical model, the depletion region of the APD is assumed to be extended from $x = 0$ to $x = W$, where W is the depletion-region width. It is further assumed that the avalanche multiplication process is initiated by the photogenerated electron at the high field, P+/N-well junction ($x = 0$) for the P+/N-well/P-sub device structure [see Fig. 2(a)]. Electrons travel in the positive x-direction within the depletion region. For the N-well/P-sub device structure, avalanche multiplication is initiated by the photogenerated electron at the low field, N-well/P-sub junction ($x = W$). Electrons travel in the negative x-direction within the depletion region.

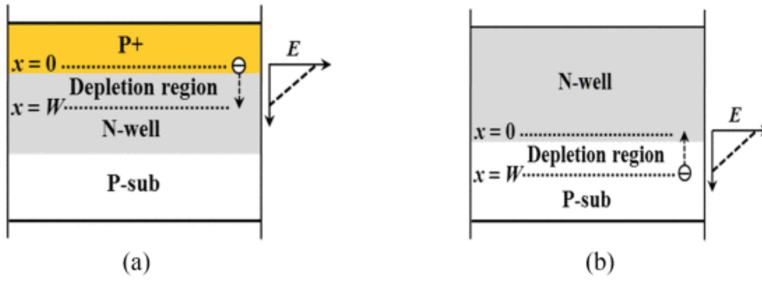


Fig. 2. P+/N-well/P-sub APD structure showing direction of electron injection (a) and N-well/P-sub structure showing the direction of electron injection (b).

In addition to the electron-initiated avalanche multiplication process, hole injection and mixed-carrier injection were taken into account in the recursive DSMT model while taking into account the absorption profile of each device. Consider an electron and a hole are located at position *x* within the multiplication region. Assume that *Z*(*x*) is the random sum of electrons and holes produced by the electron including the initiating electron itself. Similarly, *Y*(*x*) is the random number of all electrons and holes produced by the hole and its offsprings, including the hole itself. Note that $Z(W) = 1$ and $Y(0) = 1$. Consider, $z(x) = \langle Z(x) \rangle$ and $y(x) = \langle Y(x) \rangle$ are the means of $Z(x)$ and $Y(x)$, respectively. Similarly, $z_2(x) = \langle Z^2(x) \rangle$ and $y_2(x) = \langle Y^2(x) \rangle$ are the second moments of $Z(x)$ and $Y(x)$, respectively. Here, bracket denotes ensemble average. The electron and hole probability densities (he and hh), the first moments ($z(x)$ and y(x)) and the second moments ($z_2(x)$ and $y_2(x)$) are calculated using the equations expressed in [5]. The gains for an electron-initiated avalanche *G*′, a hole-initiated avalanche *G*″, and a mixed-carrier initiated avalanche *G* ‴ are calculated from the quantities *z*(*x*) and *y*(*x*) as follows. In particular, the mean of *G*′, *G*″ and *G* ‴ are

$$\langle G' \rangle = \frac{1}{2}(1 + z(0)), \quad (1)$$

$$\langle G'' \rangle = \frac{1}{2}(1 + y(w)) \quad (2)$$

and

$$\langle G''' \rangle = C \int_0^W \frac{1}{2}[z(x) + y(x)]e^{-rx}dx\,. \quad (3)$$

And the total mixed-injection mean-gain is calculated using

$$\langle G \rangle = p_e\langle G' \rangle + p_h\langle G'' \rangle + \langle G''' \rangle, \quad (4)$$

where p_e and p_h are the probability of photon absorption above and below the depletion region, respectively, τ is the absorption coefficient in Si, and *C* is a constant chosen so that $C\int_0^W e^{-rx}\,dx = p_m$ is the probability that an incident photon is absorbed in the depletion region.

Next, the second moment of the gain in the cases of an electron-initiated, a hole-initiated and a mixed-carrier initiated avalanches are given by

$$\begin{aligned} \langle G'^2 \rangle &= \quad 0.25(1 + 2z(0) + z_2(0)) \\ \langle G''^2 \rangle &= \quad 0.25(1 + 2y(w) + y_2(w)) \end{aligned} \quad (5)(6)$$

and

$$\langle G'''^2 \rangle = C \int_0^w \frac{1}{4} [z_2(x) + 2z(x)y(x) + y_2(x)] e^{-rx} dx \,. \quad (7)$$

The second moment of the mixed-injection gain is therefore

$$\langle G^2 \rangle = p_e \langle G'^2 \rangle + p_h \langle G''^2 \rangle + \langle G'''^2 \rangle. \quad (8)$$

Finally, the mixed-injection excess-noise factor F is

$$F = \frac{\langle G^2 \rangle}{\langle G \rangle^2} \,. \quad (9)$$

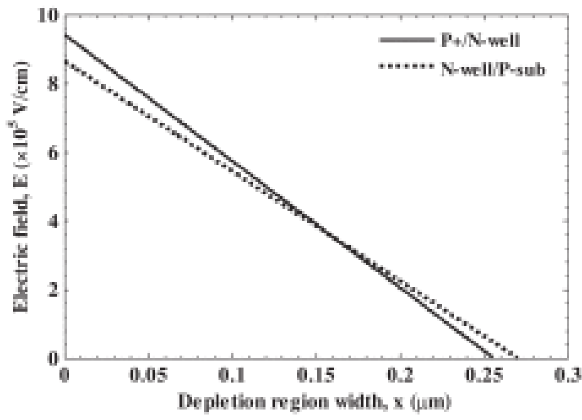
The electric field and depletion width were calculated using Technology Computer Aided Design (TCAD) Sentaurus software tool. Note that Sentaurus Device takes into account physics models like Poisson's equation and carrier continuity in calculating electric fields. The electric-field profile in the multiplication region were extracted from TCAD simulation as shown in Fig. 3(a). The electric-field dependent ionization coefficients for electrons (α) and holes (β) are calculated using Chynoweth's formula [29]

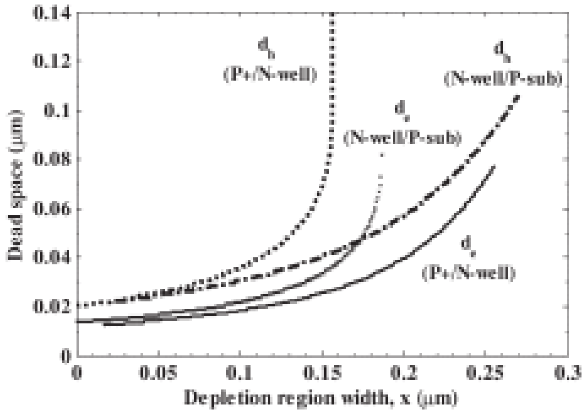
$$\alpha(E) = A_e exp \left[- \left(\frac{B_e}{E} \right)^{m_e} \right] \quad (10)$$

and

$$\beta(E) = A_h \left[exp - \left(\frac{B_h}{E} \right)^{m_h} \right], \quad (11)$$

where E is the electric field and the A, B, and m are material dependent parameters (listed in Table I) chosen from experimental [28] and fitted [8] data.





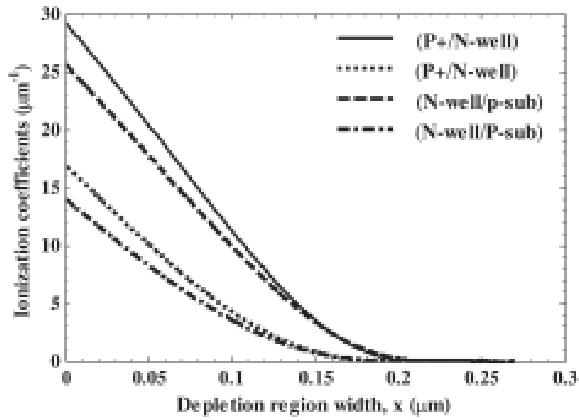


Fig. 3. Calculated electric-field profile as a function of x in the depletion region (a), calculated dead spaces for electron (d_e) and hole (d_h) (b), and calculated electron and hole ionization coefficients, α and β (c).
View All

TABLE I Ionization Parameters for Silicon [28]

	A [cm^{-1}]	B [V/cm]	m	E_{th} [eV] [8]
Electron	1.286×10^6	1.40×10^6	1.0	1.1
Hole	1.438×10^6	2.02×10^6	1.0	1.8

	A [cm^{-1}]	*B* [V/cm]	*m*	E_{th} [eV] [8]
Electron	1.286×10^6	1.40×10^6	1.0	1.1
Hole	1.438×10^6	2.02×10^6	1.0	1.8

The electric field within the depletion region, electron and hole dead spaces, d_e and d_h in conjunction with the ionization coefficients, α and β, as shown in Fig. 3(a)– (c), were used in the DSMT analytical model to predict the avalanche breakdown voltage, mean-gain, and the excess-noise factor.

The enabled ionization parameters $\alpha^*(\beta^*)$ are calculated from the experimentally determined values α (β) by equating the mean ionizing lengths from the DSMT and local model by using the formula [30]

$$\alpha = \frac{1}{\frac{1}{\alpha^*}+2d_e}, \quad (12)$$

where d_e (d_h) is the dead space for electron (hole).

In addition, McIntyre's classical noise model formula [31], as shown below

$$F(M) = kM + \left(2 - \frac{1}{M}\right)(1-k), \quad (13)$$

is used to evaluate the equivalent hole-to-electron ionization ratio, k. A small value of k represents a low excess-noise factor for an electron-initiated multiplication process.

The absorbed photon density as a function of device depth is shown in Fig. 4 for the front-side illuminated P+/N-well and N-well/P-sub APDs. Simulations were performed using TCAD software tool with 460, 542, and 633 nm excitations having a constant illumination of 1.46 mW/cm^2. The absorbed photon density is at its maximum value at the top of the APD and it decreases with the device depth. For the P+/N-well/P-sub APD, approximately 65%, 26% and 11% of the incident light are absorbed in the P+ region for 460, 542, 633 nm excitations, respectively. However, higher percentage of light absorption in P+ layer yields low values of excess noise factor (see Fig. 10) for the dominant electron initiated multiplication process in the avalanche region. Note that approximately 21%, 17% and 8% of the light are absorbed in the multiplication region for 460, 542, and 633 nm wavelengths, respectively, giving rise to mixed-injection multiplication process. In addition, reduced excess-noise factor is observed in going from 460 to 633 nm excitations. This is due to the reduced amount of mixed-injections in the multiplication region for long wavelengths.

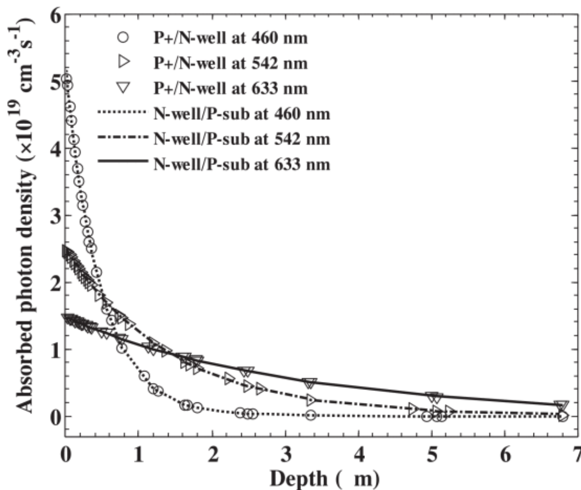


Fig. 4. Simulated absorbed photon density as a function of device depth for the P+/N-well/P-sub and the N-well/P-sub APD devices. Simulations were performed using Sentaurus TCAD software tool.

For a variant N-well/P-sub structure, approximately 0.5%, 22% and 57% of the light are absorbed in the P-sub region. This results in relatively higher excess noise factors due to the injection of holes in the multiplication region. Additionally, increased excess-noise factor is observed in going from 633 to 460 nm excitations (see Fig. 10). This is due to the increased amount of hole injections in the multiplication region for short wavelengths. Note that approximately 0.3%, 5% and 6% of light are absorbed in the multiplication region for 460, 542, and 633 nm wavelengths, respectively, giving rise to mixed-injection multiplication process.

The wavelength dependent mean-gain and excess-noise factors (see Figs. 9 and 10) are calculated using non-local DSMT analytical model taking into account 460, 542, and 633 nm excitations. Note that (4) and (8) represent first and second moments of the mixed-injection mean avalanche gain used in the DSMT model. These equations, in turn, require knowledge of the probability of photon absorption at each location along the device depth. For example, see the exponential terms in (3) and (7), which are used in (4) and (8). Now the probability of photon absorption at each location is calculated from Fig. 4, as calculated by the Sentaurus TCAD software tool.

SECTION IV. Measurement Results

Measured dark-current characteristics for the fabricated CMOS APDs are shown in Fig. 5. The current voltage characteristics were recorded with a Keithley 237 source-meter. In the linear avalanche regime, the P+/N-well (P+/N-well/p-sub) and the N-well/P-sub APD devices exhibit low dark currents of ∼93 and ∼0.86 nA at the breakdown voltages of ∼11 V and ∼10.5 V, respectively. However, the N-well/P-sub APD (270 × 270 μm^2) exhibits low dark currents as compared to the P+/N-well (350 × 350 μm^2) APD. The large difference in dark currents may be due to the difference in peak electric field in each of the APD device structures. This may not be related to the area of the device where the dark current increases linearly with the device active area [34]. We believe that the high field required for the avalanche multiplication process gives rise to strong band-to-band-tunneling, resulting in a high dark current (∼nA) for both of the APDs. The comparably low breakdown voltage of the N-well/P-sub APD is due to the proximity of P+ substrate contacts in between the plurality of N-well fingers. The shallow-trench-isolation guard-ring (STI GR) around the P+ and N+ regions prevents premature edge breakdown at the APD periphery. The dark currents are comparable to the reported values in [9] , [16] and are low as compared to the high dark currents of 1 µA at 10.8 V as in [10], and 3 µA at 8.41 V as in [14]. The reported CMOS APDs in [16] exhibit low dark currents in the range of ∼pA before avalanche breakdown occurs. The amplified dark current (due to the tunneling effect at the edges of p+ regions in n-well and n+ regions in p-well) was significantly reduced by using lightly doped p-sub or STI around the p+ and n+ regions.

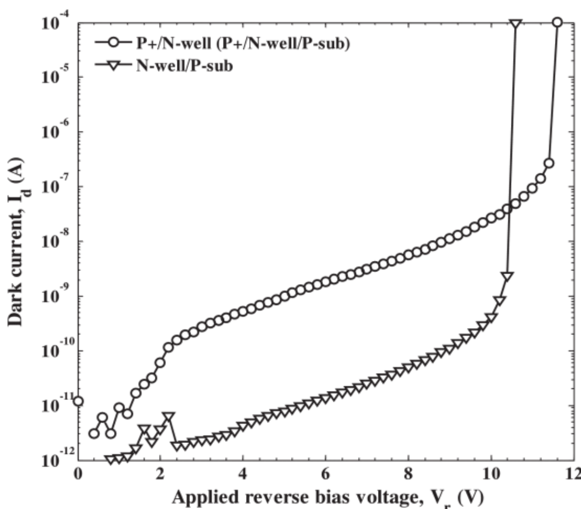


Fig. 5. Measured dark current versus applied reverse bias voltage for the P+/N-well (P+/N-well/P-sub) and the N-well/P-sub APD devices.

Measured spectral-responsivity characteristics for the P+/N- well and N-well/P-sub APD devices are shown in Fig. 6(a) and (b), respectively. Spectral measurements were performed using a single grating monochromator with a 100 W tungsten light source. A supervisory-control-and-data-acquisition (SCADA) system was also used in a desktop computer for automatic measurement. In order to modulate the optical signal, the monochromatic light from the exit slit of the monochromator was chopped at a frequency of 180 Hz. The optical beam was subsequently focused on the optical window of the device-under-test (DUT) by using a microscope objective. A Keithley 236 SMU was used for bias voltage requirements across the device and the resultant photocurrent was measured using a SR830 lock-in amplifier (LIA).

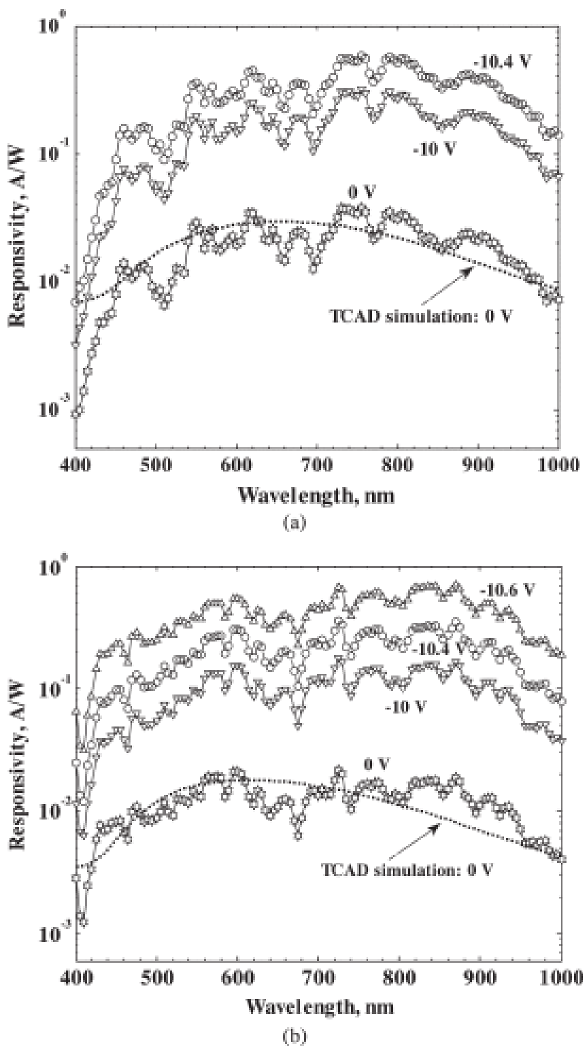


Fig. 6. Measured spectral responsivity as a function of wavelength for the P+/N-well (a) and the N-well/P-sub (b) APD devices.

Measured responsivity curves in Fig. 6(a) and (b) show peaks due to the optical interference in the dielectric stack atop the silicon surface. Note that IBM 0.13-µm CMOS technology considered here to fabricate P+/N-well/P-sub and N-well/P-sub APDs consists of 8 metal layers and 8 dielectric layers. There is also a final passivation layer on top of the last metal layer, which adds up to the total stack. As a result, there are multiple

reflections and refractions as well as attenuation through the stack of materials. This, in turn, exhibits very irregular transmission characteristics [32]–[33]and spectral response [14] as a function of the wavelength. In addition, there is a ±20% process variation in thickness of dielectric layers. This process variation causes deviation in transmission coefficient through the dielectric stack [32]– [33], which has significant impact on the APD responsivity.

For the P+/N-well APD, the unity-gain responsivities are 0.014, 0.022 and 0.024 A/W for 460, 542, and 633 nm excitations, respectively. For a variant N-well/P-sub APD, unity-gain responsivities are 0.007, 0.011, and 0.014 A/W. Both of the APDs exhibit very low values of responsivity which result from the aforementioned optical interferences in the dielectric stack and un-optimized CMOS process for APD devices. However, responsivity can be improved by using optimized CMOS process which can replace dielectric stack with an antireflection coating [14]. The spectral responsivity can also be improved with increased reverse bias voltage which results widening of the depletion region. In addition, avalanche multiplication occurs for higher bias voltage which in turn increases responsivity. The zero-bias spectral responsivities were calculated using transmission matrix method (TMM) optical solvers in conjunction with the complex-refractive-index model embedded in Sentaurus TCAD. The calculated responsivity curves are slightly off from the measured responsivity for both of the APDs. This may be due to the presence of dielectric stack atop the Si surface.

Fig. 7 shows the measured capacitance as a function of applied reverse bias voltage for the APD devices. The C-V measurements were carried out using an HP 4275A LCR meter, and the testing frequency was 1 MHz with an AC amplitude of 0.05 V. The measured capacitances for the P+/N-well (P+/N-well/P-sub) and the N-well/P-sub APD devices are below 25 pF under operating bias voltages. The transimpedance-amplifier (TIA) based measurement system, as reported in [35], can measure the excess-noise factor reliably on a wide variety of materials and APD devices, with a capacitance value up to ∼50 pF. Therefore, the mean-gain and excess-noise measurements have been performed for both of the P+/N-well (P+/N-well/P-sub) and N-well/P-sub APDs.

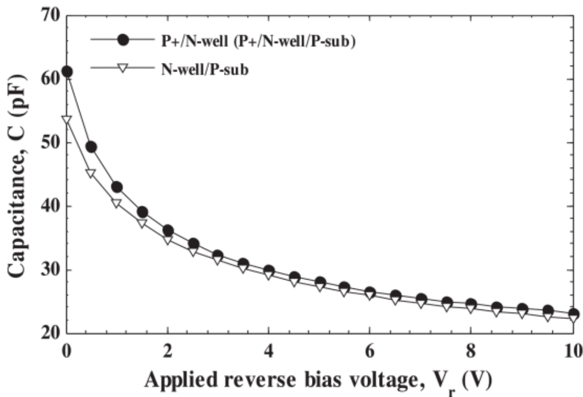


Fig. 7. Measured capacitance versus applied reverse bias voltage for the P+/N-well (P+/N-well/P-sub) and the N-well/P-sub APD devices.

The mean-gain and excess-noise measurement system is shown in a block diagram in Fig. 8. A Thorlabs 460 nm LED (LED470L), a Uniphase 542 nm He-Ne laser, and a Lambda Photometrics 633 nm He-Ne laser were used to illuminate the device with a mechanical chopper having chopping frequency at around 180 Hz. In addition, a TIA (an AD9631 high speed operational amplifier with feedback capacitance and resistance) was used to convert photodiode current into a proportional voltage. This output voltage consists of a noisy, square waveform at the chopper frequency. The peak-to-peak value of a noise-free version of this waveform (difference between the photocurrent and dark current) is proportional to the mean photocurrent. The output voltage representing the photocurrent was buffered through a unity gain voltage follower to smooth the signal and was fed to a Stanford

Research SR830 LIA. The LIA output voltage was converted to a value of stimulated photocurrent by using the known TIA gain of 1100 V/A. The mean-gain was calculated using the definition for multiplication given by

$$M = \frac{i_{ph}}{i_{pr}}, \quad (14)$$

where i_{ph} and i_{pr} are the measured output photocurrent and the unmultiplied primary photocurrent, respectively.

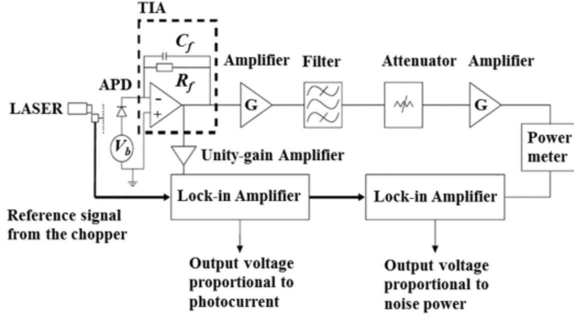


Fig. 8. Block diagram of the mean-gain and excess-noise measurement system. The TIA consists of an op-amp with a feedback resistor R_f and capacitor C_f. This block diagram is reproduced from [35].

The output of the TIA, photocurrent and its multiplied noise, was amplified by a low-noise amplifier (Mini-Circuits ZFL-500LN+). In order to extract noise information from the TIA output, the photocurrent signal must be removed. This can be done by passing the signal through a bandpass filter (Mini-Circuits SBP-10.7+). The photocurrent signal associated with the 180 Hz fundamental and its harmonics were attenuated by passing only the noise pass-band frequency, ranging from 9.5 to 11.5 MHz with a center frequency of 10.7 MHz. The output of the bandpass filter contains only the information of the noise signal (associated with the avalanche gain process which multiplies the photocurrent), which resembles an amplitude modulated noise waveform. The noise signal was then amplified by a low-noise cascaded amplifier (an HP355D attenuator with three Mini-circuits amplifiers: 500LN, 1000LN and AD9618) giving a total gain of around 78 dB. The attenuator was used in the cascade to cope with the wide range of noise amplitudes and to avoid the risk of saturating the output stages for large noise signals. The output noise voltage of the cascaded amplifier was fed into a power meter (a squaring-and-averaging circuit) to obtain the noise-power output. The noise-power was then measured using a second SR830 lock-in amplifier. The excess-noise factor is obtained using the expression [35], [36]

$$F(M) = \frac{N_{DUT}}{aMI} \times \frac{B_{eff}(C_{Si})}{B_{eff}(C_{DUT})}, \quad (15)$$

where N_{DUT} is the measured noise power of the device under test, a is a correction factor, I is the multiplied photocurrent, $B_{eff}(C_{Si})$ is the effective noise bandwidth at the calibrating Si photodiode's capacitance (C_{Si}) and B_{eff} (C_{DUT}) is the effective noise bandwidth at the device under test's capacitance. The excess-noise measurement system was calibrated against a commercial Si photodiode at unity gain. The effect of the shot noise measurement in the investigated P+/N-well/P-sub and N-well/P-sub CMOS APDs was assumed to be contributed from the multiplied excess-noise. In addition, calibration tests were performed with devices with known excess noise to ensure the absolute F measured in CMOS APDs under test are within the acceptable range.

The mean-gain and excess-noise factor depend on the applied reverse bias voltage as well as the incident wavelength onto the active area of the APD. The electron-hole pair generation (from photon absorption)

depends on the penetration depth: long wavelength light penetrates silicon deeper than the light with short wavelength. For low-noise operation, it is expected to have electron initiated avalanche multiplication process since electrons have higher ionization coefficients than holes.

The measured mean-gain, as a function of the applied reverse bias voltage, is shown inFig. 9. In the linear avalanche regime, the P+/N-well APD exhibits a mean-gain of ∼16, at a reverse bias voltage of 10.53 V, resulting from the use of a 460 nm LED, and 542 nm and 633 nm lasers, respectively. For the N-well/P-sub device structure, the linear-mode mean-gain of ∼16 was measured at a reverse bias voltage of 10.4 V using 460 nm LED, and 542 and 633 nm lasers, respectively. The wavelength dependent mean-gains were calculated using non-local DSMT analytical model with 460, 542 and 633 nm excitations. The measured breakdown voltages and mean-gain show excellent agreement with the calculated results using the DSMT, as evidenced by Figs. 5 and 9 .

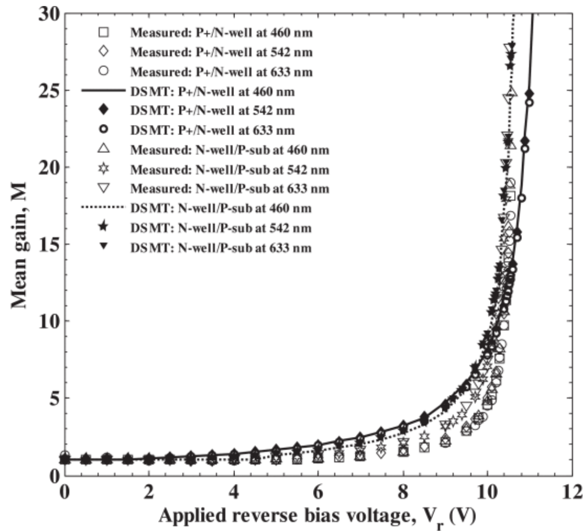


Fig. 9. Measured mean-gain versus reverse bias voltage for the P+/N-well (P+/N-well/P-sub) and the N-well/P-sub APD devices, respectively, using a 460 nm LED, and 542 and 633 nm lasers. Wavelength dependent mean-gains are calculated using non-local DSMT analytical model.

The measured excess-noise factor, as a function of the mean gain, is shown in Fig. 10 for 542 and 633 nm excitations, respectively. At a mean-gain near and below 2, however, the photocurrent was quite low (∼1 μA). In addition to the inherently low excess- noise in the P+/N-well devices, the noise-power was too weak to be measured accurately, being below the noise of our measurement setup. This results in error when calculating the excess noise near unity. Our measurement error is around ±5% in the excess-noise factor, *F*, values of unity. Nevertheless, the measurement error decreases with higher multiplication values ($M > 2$). Note that we could not measure excess-noise factor at the 460 nm excitation due to the low amount of photocurrents.

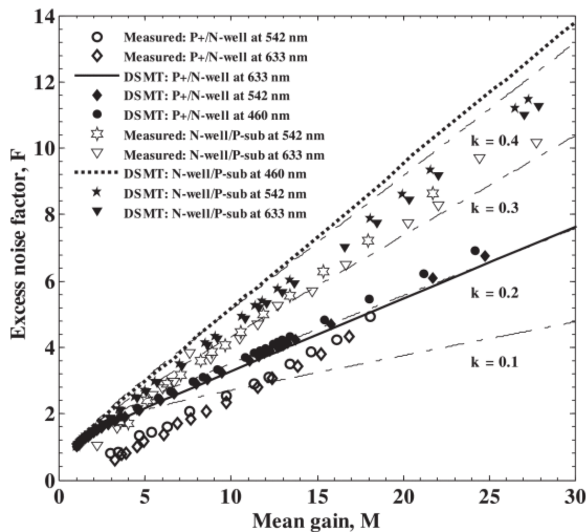


Fig. 10. Measured excess-noise factor versus mean-gain for the P+/N-well (P+/N/well/P-sub) and the N-well/P-sub APD device, respectively, using 542 and 633 nm lasers. Wavelength dependent excess noise factors are calculated using non-local DSMT analytical model. McIntyre's curves are denoted with *k* = 0.1, 0.2, 0.3, and 0.4.

The P+/N-well APD exhibits very low excess-noise factors of 4.1 and 4 at a mean gain of 16 using 542 and 633 nm lasers, respectively, as compared to the measured excess-noise factors in the visible regime of wavelength, as summarized in Table II. The low excess noise factor is due to the presence of dead space in the thin depletion region and the initiation of avalanche multiplication process by the dominant photogenerated electron in the depletion region [4], [5]. The measured excess-noise factor falls close to the *k* = 0.1 curve, as calculated from McIntyre's noise model.

TABLE II Performance Comparison With Different Silicon APDs

References	Technology node	Breakdown voltage, V_{br} (V)	Dark current, I_d	Wavelength (nm)	Excess noise factor, F (M = 16)	Ionization ratio, $k = \beta/\alpha$
Pauchard *et al.* 2000 [7]	custom	15	n.d.	600	6.2	0.47
				380	3	
Rochas *et al.* 2002 [9]	0.8-μm CMOS	19.5	0.2 nA	400	5.8	n.d.
Pancheri *et al.* 2008 [10]	0.35-μm CMOS	10.8	1 μA	380	3.9	0.47
				480/560/650	5.2	
Betta *et al.* 2011 [12]	0.35-μm CMOS	n.d.	n.d.	560	5.1	0.2
	0.7-μm HVT CMOS	20.8	n.d.	650	70	
Atef *et al.* 2013 [14]	40-nm CMOS	8.41	3 μA	520	12 (M = 27)	n.d.
Pancheri *et al.* 2014 [15]	0.15-μm CMOS	23.1	n.d.	415	3.5	n.d.
				850	5	
Lee *et al.* 2014 [16]	0.25-μm CMOS	12.4	0.1 nA	850	13	0.47
This work	0.13-μm CMOS	11	93 nA	542	4.1	0.1
				633	4	

References	Technology node	Breakdown voltage, V_{br} (V)	Dark current I_d	Wavelength (nm)	Excess noise factor, F (M = 16)	Ionization ratio, $k = \beta/\alpha$
A. R. Pauchard *et al.*, 2000 [7]	custom	15	n.d.	600 380	6.2 3	0.47
A. Rochas *et al.*, 2002 [9]	0.8-μm CMOS	19.5	0.2 nA	400	5.8	n.d.
L. Pancheri *et al.*, 2008 [10]	0.35-μm CMOS	10.8	1 μA	380 480/560/650	3.9 5.2	0.47
G.-F. D. Betta *et al.*, 2011 [12]	0.35-μm CMOS 0.7-μm HVT CMOS	n.d. 20.8	n.d. n.d.	560 650	5.1 70	0.2
M. Atef *et al.*, 2013 [14]	40-nm CMOS	8.41	3 μA	520	12 (M = 27)	n.d.
L. Pancheri *et al.*, 2014 [15]	0.15-μm CMOS	23.1	n.d.	415 850	3.5 5	n.d.
M.-J. Lee *et al.*, 2014 [16]	0.25-μm CMOS	12.4	0.1 nA	850	13	0.47
This work	0.13-μm CMOS	11	93 nA	542 633	4.1 4	0.1

For the N-well/P-sub device structure, excess-noise factors of 6.5 and 6.2 were measured at a mean-gain of 16 using 542 and 633 nm lasers, respectively. The high excess noise appears as a result of the injection of holes in the multiplication region. The measured excess-noise factor falls close to the calculated DSMT curve as well as the McIntyre's noise curve at $k = 0.3$. The measured excess-noise with 542 nm was slightly higher than that with 633 nm for both of the P+/N-well and N-well/P- sub APD devices. The wavelength dependent excess-noise factors are also calculated using DSMT model with 460, 542 and 633 nm excitations. The calculated excess-noise factors using recursive DSMT analytical model were slightly higher than measured values for both of the APDs. This could be due to the presence of non-uniform electric fields in the multiplication region.

SECTION V. Conclusion

Modeling and measurements for the speed-optimized, large-area CMOS compatible P+/N-well/P-sub and N-well/P-sub APDs were presented. Remarkably low excess-noise factor values were reported for the P+/N-well APD in the visible wavelength regime. The reported devices benefit from high-speed operation, low-voltage biasing and low cost. The large-area CMOS Si APDs with subsections are potential devices for the realization of low-noise, multi-gigabit visible-light communication systems.

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