This project is submitted to the Faculty of Computer Science and Information Technology
University Of Malaya
Impartial fulfillment of the requirement of the Bachelor of Computer Science

Fax Modem System-
Analysis in Concept,
Design & Implementation Using VHDL

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ABSTRACT

This graduation project is entitled Designing Fax Modem using VHDL. This project is indeed the starting point the way of exploring secret of embedded system. It is actually a practice with the knowledge and hardware and software in computer organization and design. At first stage the architecture of fax modem will be analyzed and studied. Then the architecture of the fax modem is redesigned using hardware prototyping. The hardware prototyping is method that used to test and evaluate the design of a particular fax modem. Coding or programming with VHSIC Hardware Description Language (VHDL) undertakes this approach.

Finally the completed programs and codes will be simulated using the Xilinx Foundation Software. This report is a description of analysis and design of the modem. For the implementation and simulation it will conducted continuously from this stage. This report including books, web pages articles. The implication of this report is the understanding of the hierarchical and parallel nature of the fax modem that is the most important thing in order to design processor.

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Chapter 1
Introduction

1.0 Introduction

This project should be understood by anyone to control fax modem. In chapter 2, I introduce about modem first because a fax modem is like a regular modem except it is designed to transmit document to a fax machine or to another fax modem. Some but not t all fax modem can be do double either duty as regular modems. As regular m fax modem can be either internal or external. Internal fax modems are often called fax board. What important thing in my project I focus on modem control. Modem control is designed in UART.UART is a controlled chip that process data coming in and going out of the modem. So to more detail about modem control will be conducted in chapter 4.

1.1 Scope

Chapter 2: It covers about modem, explanation what is modem, how it work and used, standard for modem, types, classifying and how learning process can be made in modem.

Chapter 3: Brief explanation on how programming is done by using VHDL will be carried in this chapter.

Chapter 4: It covers the analysis and designing process.

Chapter 5: The result of every simulation and synthesis process and the explanation of every module will be presented.

Chapter 6: The conclusion and suggestion for future enhancement are discussed here.

1.2 Objective

The main objective of this project is to design, coding and simulate the modem control as core of central processing unit using VHSIC (Very High Speed Integrated Circuitry Hardware Description Language and Xilinx Software).

After designing, coding and testing will be done to implement the instructions using VHDL and then simulate it using a Xilinx Software. In fact, this project consists of a research in both computer software and hardware. Therefore it requires the understanding and knowledge in computer science especially programming and modem control architecture.

The output of this project will be a prototype of modem control using hardware description language. By using simulation program with appropriate simulation data, the result of all design stages can be verified, waveforms, timing diagram. It provides the user an overview of how modem working.

1.3 Modeling tools

In this research the modem control is used as test case to implement a typical simulated modem control using Xilinx Software. This approach allow the application of the existing high – quality software development environment and focuses on processor development.

More over ,the modem control core will be described using the VHDL (VHSIC Hardware Description Language).VHDL is an industry standard language used to

describe hardware from abstract to concrete level. It is rapidly being embraced as the universal communication medium of design. Computer aided engineering workstation vendors throughput the industry are standardizing on VHDL as input and output from their tools. These tools include simulation tools, synthesis tools, layout tools , etc.

1.4 Project Schedule.

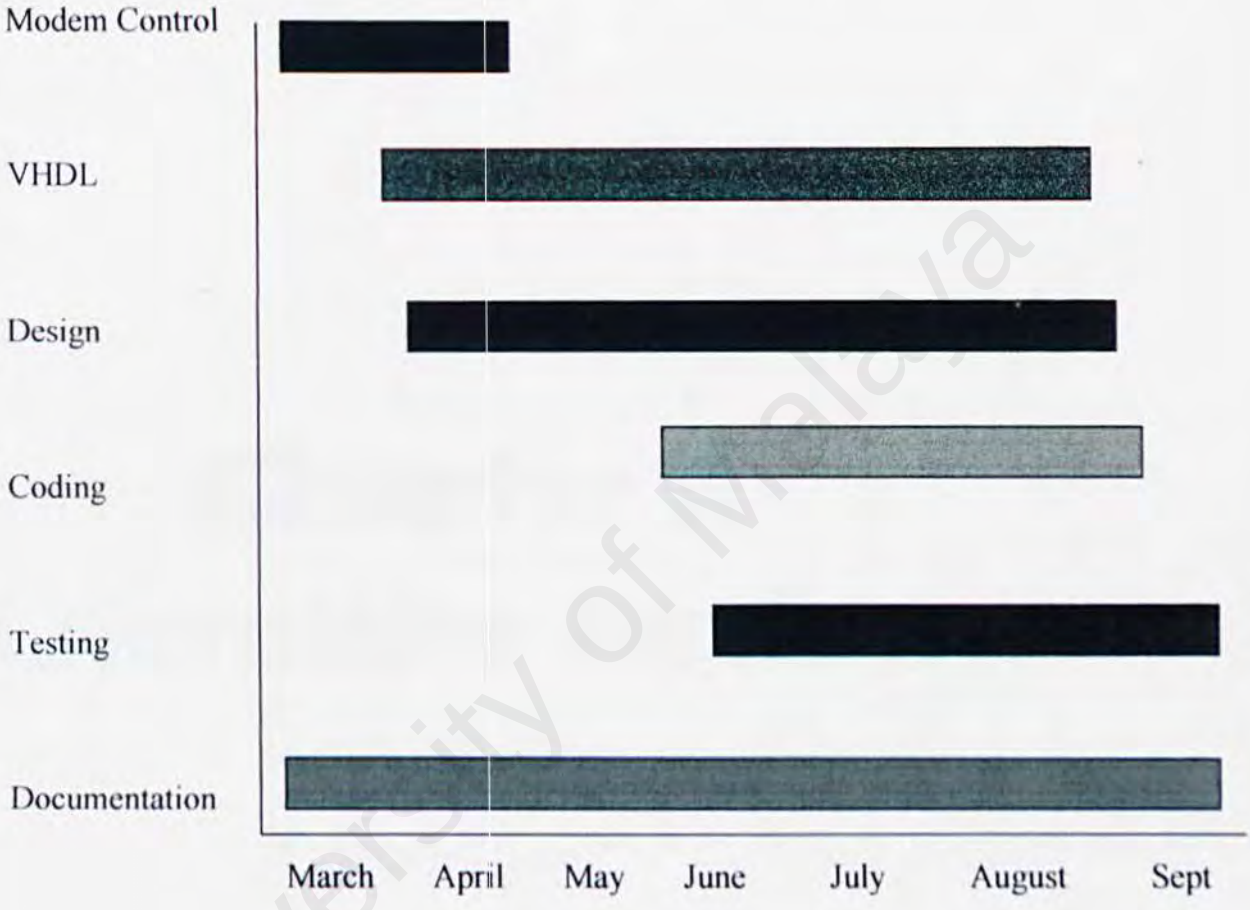


Figure 1 : Graf Schedule for Project

Chapter 2
Literature Review

2.0 History Modem

It was in the 1950s that the first modems were being developed. There was a need to transmit data for North American air defense, so efforts were made to accomplish the goal of data transfer across the existing telephone wires. The air defense was using modems by the end of the 1950s, but the first commercial device was not available until 1962. It was called the Bell 103, by AT&T. This first modem allowed full-duplex transmission, and boasted data rates up to 300 bits per second. Shortly after the Bell 103, there came the Bell 212, which reached speeds of 1200 bits per second. It also employed a method of modulation called phase-shift keying (PSK). This was a step up from the frequency-shift keying (FSK) method that the Bell 103 employed.

Over the next fifteen years, the efforts were to make the modems transmit data at a higher rate. In order to accomplish this, the telephone system required some improvement. As it was, due to mutual interference of signals being attenuated at various rates through the system, there was smearing of data symbols. To compensate for this, equalizers needed to be applied to the telephone lines. The automatic adaptive equalizer was invented in 1965 at Bell Laboratories by Robert Lucky. While equalizers had been used for some time, they required human intervention to be adjusted appropriately. With the advent of the automatic adaptive equalizer, data could be transmitted at high rates, as was desired. Modem technology also improved in this time, and by 1980, there existed modems that could transmit up to 14.4 kilobits per second over four-wire leased lines.

By 1984, modems were to the point of transmitting 9.6 kilobits per second over a single-pair circuit on the telephone system. To make this a reality, advances were made in echo cancellation, which keeps the sending modem from picking up its transmitted signal on its own receiver. This problem, of course, only presented itself when trying to send high speed data over a single circuit. Additionally, a new coded modulation with error correcting codes was developed. This integral error correction made the signal less susceptible to noise.

Using the same sort of technology, modem speeds were increased to 14.4 kilobits per second by 1991. Then, in 1994, it doubled to 28.8 kilobits per second. Soon after, there came 33.6, which was thought to be an upper limit for phone line transmisions. But along came the 56k modem, and a new set of standards, so the speeds continue to push the envelope of the capacity of the telephone system.

2.1 WHAT MODEMS ARE.

A modem (short for Modulate Demodulate) is a digital communications device that enables data from computer to be transmitted over regular (i.e. analog), telephone line. Computers transmit data in digital format discrete" on" and "off" pulses. Telephone lines, designed for voice communication, transmit data in analog format continuous sound waves that vary in strength and frequency, depending on the volume and pitch of the sound. A modem converts (i.e. modulates) digital pulses from the computer into analog waves that can be sent overt the phone line, and it also converts (i.e. demodulates) analog waves from the phone line into digital pulses that the computer can understand.

(Actually, the telephone company lines are analog only between the telephone company's switching station and the end user: between switching stations, signals are converted and transmitted in digital format.)

A modulator converts a digital signal to an analog signal. A demodulator converts an analog signal to a digital signal

2.2 MODEM CONCEPT

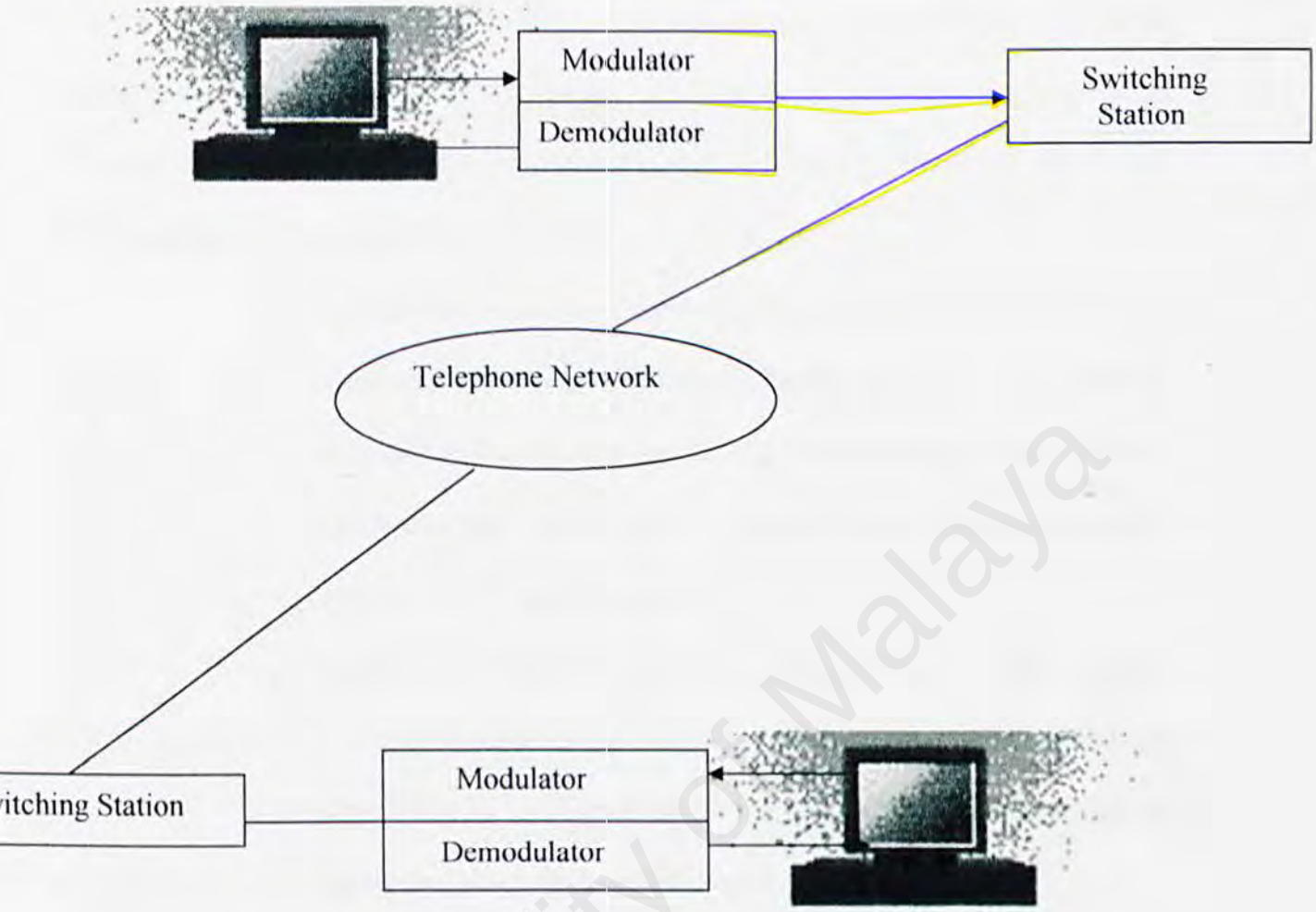


Figure 2 : Modem Concept

Figure show the relationship of modems to a communication link. The two PCs at the end are the DTEs: the modem are the DCEs .The DTE create a digital signal and relays it to the modem via an interface (like the EIA-232) The modulated signal is received by the demodulation function of the second modem .The demodulator takes the ASK,FSK,PSK or QAM signal and decode it into whatever its format computer can accept. It then relays the resulting digital signal to the receiving computer via interface. Each DCE must be compatible with both its own DTE and with other DCEs.

2.3 WHEN MODEMS ARE USED

Modems are employed when a library decides to use the public phone system (sometimes referred to as POTS plain old telephone service)as a means of communicating between its LAN and remote computers. They provide both dial in and out capability. A library may use modems to:

- Provide dial in access ("remote access service") to its LAN. This might enable patrons to access the catalog and CD-ROM databases and staff to access files on the LAN server from home. Remote access can also enable the LAN administrator to access the LAN from home when problems arise.
- Connect to on line services or the internet .Modems can be used by staff to dial out to online services as Dialog or can provide the LAN with a dial up connection to an Internet Services Provider(ISP) for e-mail and access to the World Wide Web.
- Connect to LAN, allowing computers on the library LAN to access files from the remote LAN allowing computers of the library LAN to access files from the remote LAN of the library's parent organization.

Using modems to connect a LAN to voice grade telephone lines is recommended mainly when occasional access is needed for a relatively small number of users. However ,phone lines have narrow bandwidth(i.e are slow) are subject to noise and can

only accommodate one user at time LAN that has multiple user requiring full time access and accommodate multiple users.

2.4 HOW MODEMS ARE USED.

There are two way to connect to LAN to the phone system using modems. One is to set up a communications server (essentially a LAN workstation with one or several modems plus modems software) to act as an agent on behalf of the remote user. In this method, the remote user remote user dialing in to the LAN does not become a LAN client(i.e. does not have direct access to the LAN);rather the remote user only has access to communication server, which in turn has access to the LAN. To load files onto the file server, for example, the remote user first must load the files (trough modem connection) onto the communication server, and from there to the files server.

The second method is to set up a communication server for Point-to –Point (PPP) connections. PPP is a communication protocol that allows the remote computer to become an actual "node" on the LAN, so that it can access the LAN directly and function as though it were actually on the network. Running PPP requires that the both the communication server and the remote computer have PPP software.(AN older protocol called Serial Line Internet Protocol (SLIP) can also be used, but it is more limited)

When communications server need to provide access to a large number of a remote users, a large number of modems can be rack mounted to form **modem bank**, with each modem connected to telephone line. All the phones lines can be set up to respond to a single number ,so that a single number so that the library can provide remote access with only one phone number.

2.5 HOW DOES MODEMS WORK

Modems have the following internal components:

- Power supply to provide steady regulated source of power.
- Subscriber interface which contains the telephone jacks to connect to phone line.
- Central processing unit which controls all the other components and is responsible for processes such as data compression and error detection.
- Memory including both Read Only Memory (to store the modem software)and Random Access Memory(for temporary storage of data being processed).
- Modem circuitry including the modem chip which converts digital signal to analog and vice versa.

To connect to a remote host via modem a computer (using modem software such as ProComm or PC anywhere)first establishes communication with its attached modem, the modem establishes communication with the remote host's modem and that modem establishes communication with the actual remote host. Establishing this channel of communication and setting its parameters is a processed called **handshaking.** When communicating the sending modem modulates the digital signals from the attached computer into analog audio signals, converting them back into digital signals which it sends to attached computer. High speed modem are able to transfer more data over a phone line at given time by using data compression. The modem at the other end however must be able to decompress data. Modems used methods of error detection and control to ensure that signals are transmitted accurately when an error is detected the signals is retransmitted.

2.6 EXTERNAL / INTERNAL MODEMS

There are two basics physical types of modems: Internal and External modems. External modems sit next to the computer and connect to the serial port using a straight through serial cable.

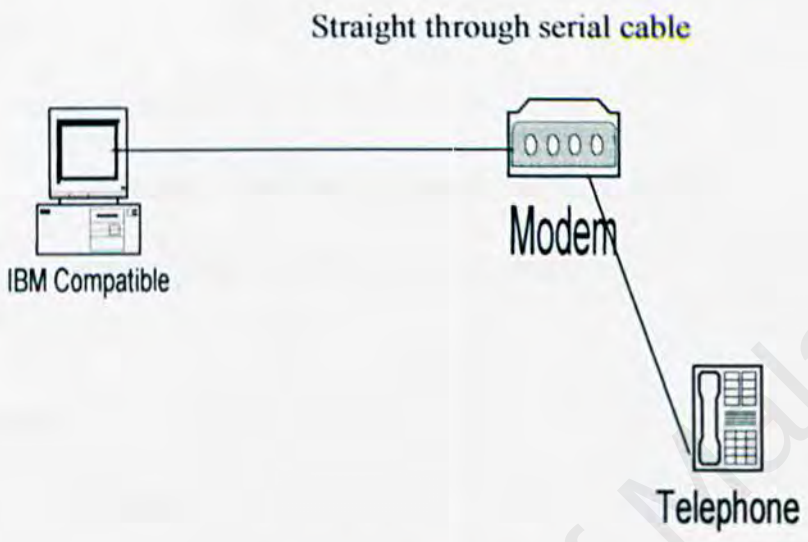


Figure 3: External Modem

An internal modem is a plug in circuit board that site inside the computer. It incorporates the serial port on board. They are less expensive than external modem because they do not requires case, power supply and serial cable. They appear to the communication programs as if they were an external modem for all practical purposes.

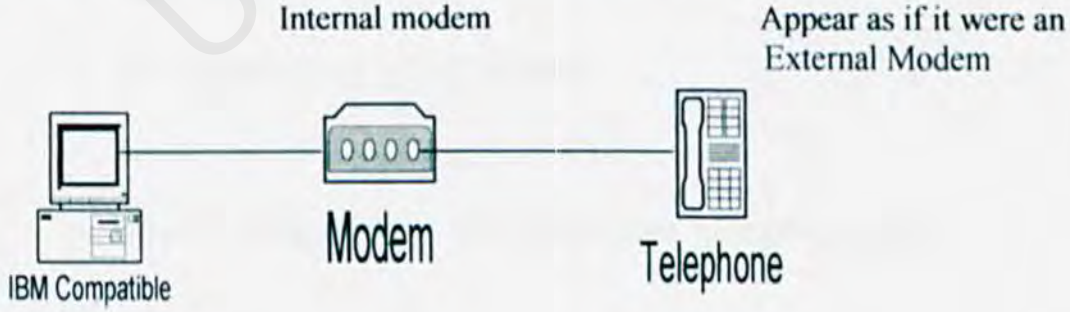


Figure 4 : Internal modem

2.7 ADVANTAGES AND DISADVANTAGES FOR INTERNAL/EXTERNAL MODEM

External Modem

Advantages:

- Easier to installation
- Can be shared return multiple machines(IBM or Mac)
- Has indicator light to show status connection

Disadvantages:

- More expensive
- External power supply requires
- Requires extra cabling

Internal Modem

Advantages:

- Less expensive
- No external power supply required
- Some are configuration by software
- Avoid cabling problem(loose connection incorrection cable)

Disadvantages:

- Installation and services more difficult(pc must be opened)
- No indicator light to show status of modem
- Harder to share modem between multiple machine.

2.8 Modem Architecture Description

- Coding structure for downstream link
  - Concatenated coding with interleave
  - Inner convolution code
  - Outer Reed-Solomon code

- Advantages
  - High coding gain
  - Supports long block lengths
  - Supports multiple coding strategies in the channel
  - Well-known complexity for subscriber terminal
  - Additional complexity is concentrated at hub

- Downstream FDD transmission
- Dynamic variation in modulation format
  - Code rate / type (coding strategy)
  - Modulation order
- Supports multiple codes in the channel
  - Code assignment is partitioned by service requirement
  - Supports variability in block lengths
- Coding gain improvement for all codes
- Low-latency applications

Modulator Architecture Description

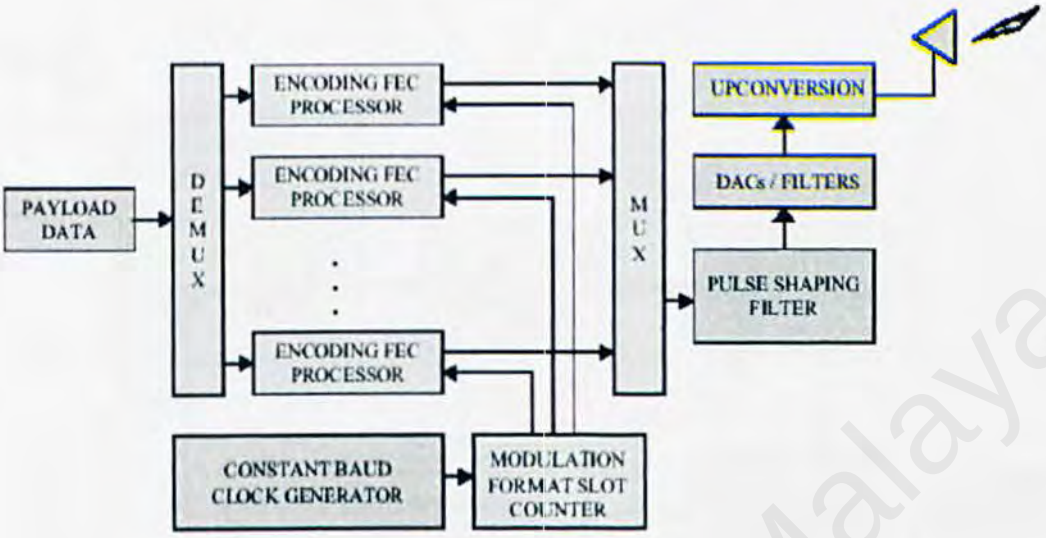


Figure 5 : Modulator Architecture Description

Demodulator Architecture Description

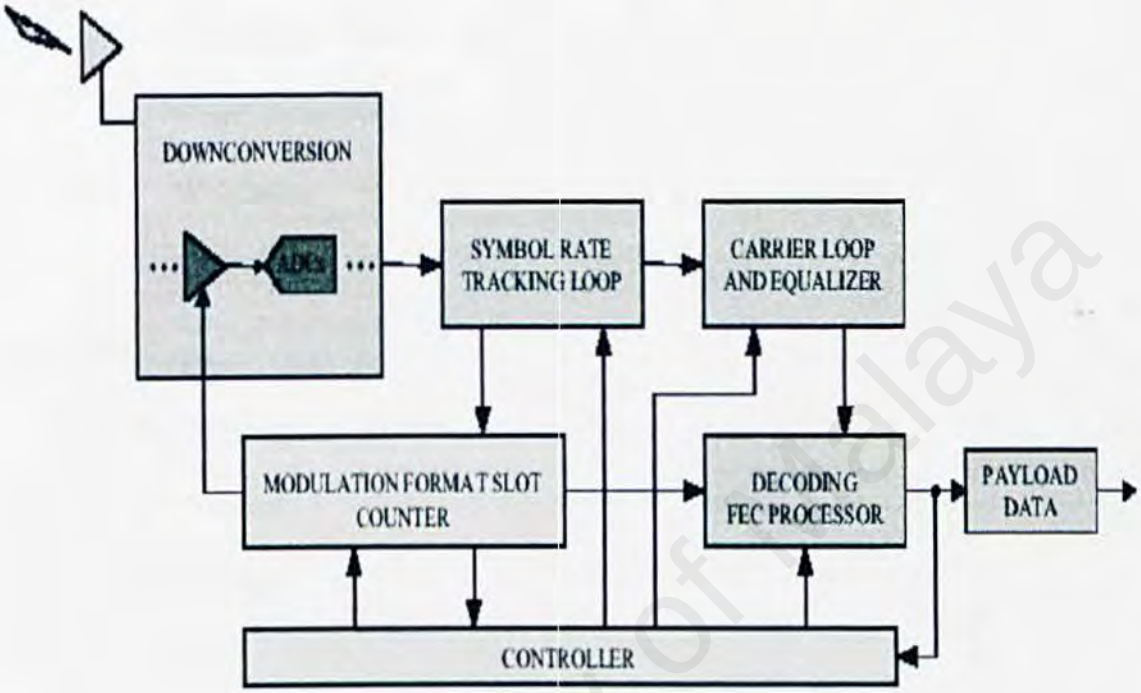


Figure 6 : Demodulator Architecture Description

2.9 CLASSIFICATION OF MODEMS

The modems can be classified according to their characteristics:

- Range
    - Short Haul
    - Voice Grade(VG)
    - Wideband
- Line Type
    - Dial-up
    - Leased
    - Private
- Synchronization
    - Asynchronous
    - Synchronous
- Modulation
    - AM
    - FM/FSK
    - PM
    - TCM
- Data Rate

2.9.1 Classifying Modems according to :Range

- **Short Haul**

Short Haul modems are cheap solution to system of short ranges (up to 15km),which use private lines are not part of a public system. Short haul modems can also can be used, even if the end-to-end length of the direct connections longer than 15 km, when both end of lines are served by the same central office in the telephone system. These lines are called "local loop". Short haul modem are distance sensitive, because signal attenuation occurs as the signal travels through the lines. The transmissions rate must be lowered to ensure consistent and error free transmission on longer distances.

Short haul modems tend to be cheaper than other modem for two reason:

- No circuitry is included in them to correct for differences between the carrier frequency of the demodulator and the frequency of the modulator.
- Generally no circuitry is included to reduce/correct for noise rejection which is less of problem over short distances than over long distances.

There two main types of short haul modems:

1. Analog modems using a simple modulation method, without sophisticated devices

for error or equalizers. These modems usually operates at a maximum rate of 9600bps,but there are some which support higher rates(up to 64 000bps)

2. Line drivers increase the digital signal which transmit to the communication Channel and to the not transmit the carrier signal, as conventional modems. Line driver are very cheap and tiny and connect to the RS232 connector of the terminal (since the lack of power supply, they use the signal voltage of the DTE-DCE interface for DC power supply).

❖ **Voice Grade(VG)**

Voice Grade modems are used for unlimited destination, using moderates to high data rate. This modems are expensive and their maintenance and tuning are sophisticated. Communication channels are leased line s and dial-up.

Voice band telephone network is used for data transmissions. A user to-user connection may be either dedicated or dialed. The links in the connection are the same two cases, and the only differences for the user is that for some impairments (particularly attenuation and delay distortion) a dedicated (private or leased)line is guaranteed to meet certain specifications, whereas a dialed connection can only be described statistically

❖ **Wideband**

Wideband modem are used in large volume telephone line multiplexing, dedicated computer-to- computer link .These modems exceed high data rates.

2.9.2 Classifying Modems according to: Line Type

❖ **Leased, Private**

Leased, private or dedicated lines (usually 4-wires)are for the exclusive use of "leased line" modems either pair (in simple point-to-point connections) or several (on multi drop network for a polling of connection system).If the medium is the telephone network, their transmissions characteristics are usually guaranteed to meet certain specification, but if the link include any radio transmission, the quality of it may be as variable as that of a switched (i.e. no dedicated)line

❖ **Dial up**

Dial up modem can be establishes point-to-point connections on the PSTN by any combination of manual or manual or automatic dialing or answering. The quality of the circuit is not guaranteed, but all phone companies establish objectives. The link established almost always 2-wire because 4 –wire dialing is tedious and expensive.

Two- and Four –Wires Lines

A four –wire (4W) line is pair of two-wire (2w) lines, ones for transmitting and one for receiving, in which the signals in the two directions are to be kept totally separate. Perfect separation can be maintained only if the four-wire configuration is two sustained from transmitter to receiver. The line may be combined in 4W/2W network (often called *hybrid* or *a hybrid transformer*) at any point in the signal path. In this cases impedance mismatches will causes reflections and interference between two signal.

2.9.3 Classifying Modems according to: Operation Mode

- **Half duplex**

Half duplex means that signal can be passed in either direction but not in both simultaneously. A telephone channel often includes an echo- suppressor ,allowing transmission in only one direction this renders the channel half duplex. Echo suppressors are slowly being replaced by echo cancellers. which are theoretically full-duplex devices.

When a modems is connected to a two-wire line, its output impedances cannot be matched exactly to the input impedances of lines and some part of its transmitted signal(usually badly distorted)will always be reflected back. For this reason half – duplex receivers are disabled (received data is clamped)when their local transmitter operative.

Half- duplex modems can work full-duplex mode.

❖ **Full Duplex**

Full duplex means that signal can be passed in either direction, simultaneously. Full duplex operation on two –wire line requires the ability separate a receive signal from the reflection of transmitted signal. This is accomplished by either FDM(frequency division multiplexing) in which the signals in the two directions occupy different frequency band and are separated by filtering ,or by Echo Canceling (EC).

The implication of the modems term full-*duplex* is usually that the modems can transmit and receive simultaneously at full speed. Modems that provide a low –speed reverse channel are sometimes called *split-speed* or *asymmetric* modems.

Full duplex modems will not work on half –duplex channels.

❖ **Simplex**

Simplex means that signals can be passed in one direction only. A remote modem for a telemeter system might and 2-wire line with a common unidirectional amplifier is simplex.

❖ *Echo Suppressor and Echo Canceller*

At the junction between the local loop which usually a 2 wire circuit and the trunk which is a 4 wire circuit echoes can occur. The effect of the echo is that a person speaking on telephone hears his own words after a short delay.

Physiologies studies have shown that this is annoying to many people often making them stutter become confused. To eliminate the problem of echoes, echo suppressor are installed on line longer than 200km (On short lines the echoes come back so fast that

people cannot detect them .An echoes suppressor is a device that detect humans speech coming from one end of the connection and suppresses all signal going the other ways .The device compares the levels at its two input port and it if decides for example that the other end is talking it inserts an attenuator in the return (echo path) and vice versa.

Echo suppressors have several properties that are undesirable for data communication. First they prevent full duplex data transmission, which would otherwise be possible, even other two wire local loop (by allocating part of the bandwidth to the forward channel and part to the reverse channel).Even if half duplex transmission is adequate, they are a nuisance because the time required to switch directions can be substantial. Double talking totally confuses them, and the attenuation may be switched in and out repeatedly. Furthermore they are designed to reverse upon detecting human speech not digital data.

To reduce these problems, when echo suppressors detect a specific tone they shut down and remain shut down as long as the carrier is present(this is an example of *in band signaling* where control signals that activate and deactivate internal control carrier function lie within the band accessible to the user)This disabling is usually done during initial handshaking by one modem transmitting an answer tone in either 2100Hz (CCIT standard) or 2225 Hz(modems following the old Bell 103 standard)

Echo suppressors are slowly being replaced by ECs, which allow a certain amount of double talking and do not require "capture" timwe for any one talker to assume control of the connection.

2.9.4 Classifying Modems according to: Synchronization

❖ **Asynchronous Modems**

Most of modems that operates in slow and moderate rates up to 1800bps are synchronous (using asynchronous data).Asynchronous modems operates in FSK modulation and use two frequencies for transmission and another two for receiving .Asynchronous modems can be connected in different options to the communication media.

- Using 2-wire or 4-wire interface
- Using switched lines or leased lines.
- Using interface to call unit/automatic answer when dialing up
-

In a 2-wire line full duplex operation can be achieved by splitting the channel into two sub channels.

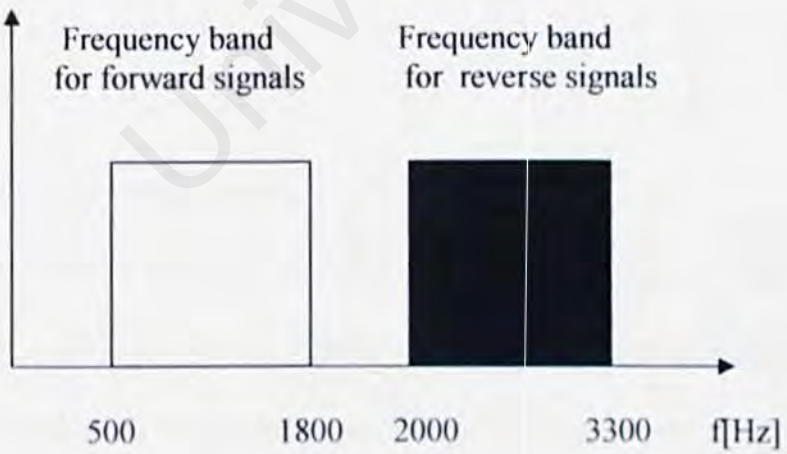


Figure 7: Graph or Frequencies Transmission

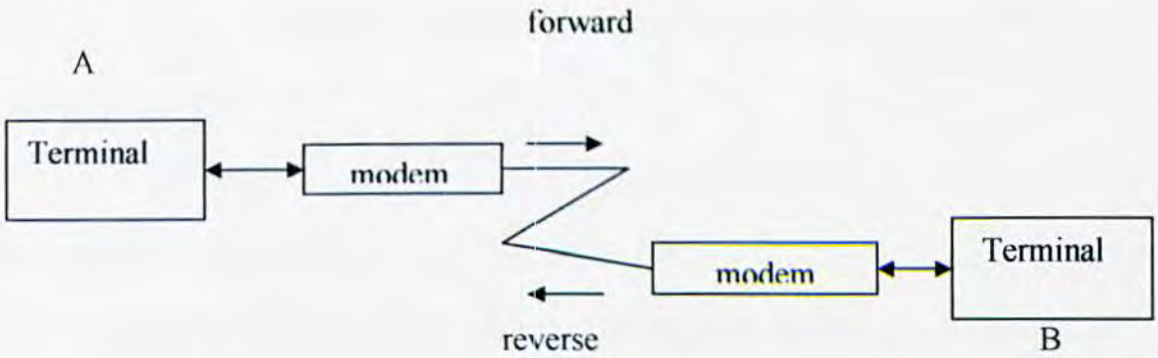


Figure 8: Operating Asynchronous Modem in 2-Wire Line.

❖ Asynchronous data

Asynchronous data is not accompanied by any clock, and the transmitting and receiving modems know only the nominal data rate. To prevent slipping of the data relative to the modems' clocks this data always grouped in very short blocks(characters) with framing bits (starts and stops bits).The most common code used for this is seven-bit ASCII code with even parity.

❖ Synchronous Modems

Synchronous modems operates in the audio domain at rates up to 28800bps in audio lines used in telephones system (using synchronous data).The usual modulation methods are the phase modulation and integrated phase and amplitude (at higher rates than 4800bps).

In synchronous modems, equalizer are used, in order to offset the misfit of the telephone lines. This equalizer are inserted in addition to equalizers, that sometimes already exists in the telephone lines.

These equalizers can be classified into three main groups:

1. *Fixed/statically equalizer*-these equalizer offset the signal according to the average of the known attenuation in each frequency. Tuning the equalizer is sometimes done in the factory and stays fixed, usually they are used to operate at low rates in a dial up line.
2. *Manually adjusted equalize*r- these equalizer can be tuned to optimal performance to given line. These equalizers should be re-tuned when the line is replaced and periodically. Specially, it should be tuned frequently when the line is low quality and it's parameters are changed frequently. Tuning is done using a button inside the modem(or on the external board).
3. Automatic equalizer-these equalizers are tuned automatically when the connection is established. Depending on the line quality in a specific moment, in process of about 1.5ms to2.5ms,after the first tuning, the equalizer samples the line continually and adjusts itself to the changed conditions, so the modems operates at each moment under optimal conditions. The fitness process operates some modems, at rates of 2400 times in a second.

Synchronous modems operate in same manner asynchronous modems. However synchronous modems operate at higher rates and since requirements to transmit at these rates in increasing, most of the innovations are implemented for synchronous modems.

In synchronous modems the channel can be spilt for several consumer at variations speeds. Modems who have this ability are called SSM –Split System Modem. These modems can be use a simple split or using multipoint connection.

Synchronous data is accompanied by a clock signal. Synchronous data is almost always grouped in blocks and it is the responsibility of the data source to assemble those blocks with framing codes and any extra bits needed for error detecting and/or correcting according to one of many different protocols (BISYNC, HDLC, SDLC, ETC).The data source and destination expect the modem to be transparent to this type data, conversely, the modems can be ignore the blocking of the data.

2.9.5 Classifying Modems according to: MODULATION

Communication channels like telephone lines are usually analog media. Analog media is a bandwidth limited channeling the case of telephone lines the useable bandwidth frequencies is in the range of 300 Hz to 3300Hz.

Data communication means moving digital information from one place to another through communication channels. These digital information signals have the shape of square waves and the meaning of "0" and "1".

Modulation

Modulation is a technique of modifying some basic analog signal in a known way in order to encode information in that basic signal. Any measurable property of an analog signal can be used to transmit information by changing this property in some known manner and then detecting those changes at the receiver end. The signal that is modulated is called the carrier signal, because it carries the digital information from one end of the communication channel to the other end.

The device that changes the signal at the transmitting end of the communication channel is called the ***MODULATOR***. The device at the receiving end of the channel, which detects the digital information from the modulated signal, is called the ***DEMODULATOR.***

A basic analog signal is a sinusoidal wave which can be written in mathematical form as follows:

S(t) = A * SIN (2* PI * F * T + PHI)

were A is the peak amplitude, F is the signal frequency and PHI is the phase of the signal . Modulation can use any of these three measurable and changeable properties of the sine wave for encoding purposes.

There are three modulation techniques, each of them changes one of the properties of the basic analog signal.

2.9.5.1 * AM - amplitude modulation

This technique changes the amplitude of the sine wave. In the earliest modems, digital signals were converted to analog by transmitting a large amplitude sine wave for a "1" and zero amplitude for a "0". The main advantage of this technique is that it is easy to produce such signals and also to detect them. This technique has two major disadvantages. The first is that the speed of the changing amplitude is limited by the bandwidth of the line. The second is that the small amplitude changes suffer from unreliable detection. Telephone lines limit amplitude changes to some 3000 changes per second. The disadvantages of amplitude modulation causes this technique to no longer be used by modems, however, it is used in conjunction with other techniques .

2.9.5.2. * QAM - quadrate amplitude modulation

This technique is based on the basic amplitude modulation . This technique improves the performance of the basic amplitude modulation. In this technique two carrier signals are transmitted simultaneously. The two carrier signals are at the same frequency with a 90 degrees phase shift. The mathematical form of the transmitted signal will be as follows:

S(t) = A* SIN (Wc* t) + B* COS (Wc* t)

A, B, are the amplitude of the two carrier signals. Each of them can get a value from a known set of values. In this way a few bits can be transmitted in the period of one symbol time. For example consider the set of values {1 , 2 , 3 , 4 }. In this example 4 different values can represent 2 bits. During one symbol time 4 bits will be transmitted, "A" will represent 2 bits and another 2 bits will be represented by "B".

2.9.5.3 * FM - frequency modulation

In this technique the frequency of the carrier signal is changed according to the data. The transmitter sends different frequencies for a "1" than for a "0" .This technique is also called FSK - frequency shift keying. The disadvantages of this technique are that again (as it was with amplitude modulation) the rate of frequency changes is limited by the bandwidth of the line, and that distortion caused by the lines makes the detection even harder than amplitude modulation. Today this technique is used in law rate asynchronous modems up to 1200 baud only.

2.9.5.4 * CPM - continuous phase modulation

A modern technique which derives from basic frequency modulation. The only difference is that in the transition from one symbol to another the phase is continuously changed, there are no phase steps. Continuous phase means that the transmitted signal bandwidth is limited and faster data rates can be achieved for the same bandwidth.

2.9.5.5 * PM - phase modulation

In this modulation method a sine wave is transmitted and the phase of the sine carries the digital data. For a "0", a 0 degrees phase sine wave is transmitted (PHI = 0). For a "1", a 180 degrees sine wave is transmitted (PHI = 180) . This technique, in order to detect the phase of each symbol, requires phase synchronization between the receiver's and transmitter's phase. This complicates the receiver's design

A sub method of the phase modulation is ***DIFFERENTIAL PHASE MODULATION***. In this method, the modem shifts the phase of each succeeding signal in a certain number of degrees for a "0" (90 degrees for example) and a different certain number of degrees for a "1" (270 degrees for example) .This method is easier to detect than the previous one. The receiver has to detect the phase shifts between symbols and not the absolute phase. This technique is also called *PSK - phase shift keying*. In the case of two possible phase shifts the modulation will be called BPSK - binary PSK. In the case of 4 different phase shifts possibilities for each symbol which means that each

symbol represents 2 bits the modulation will be called QPSK, and in case of 8 different phase shifts the modulation technique will be called 8PSK.

2.9.6 Data Rate

The number of signal changes transmitted per unit of time is called the *data rate* of the modem. That rate is usually expressed in terms of a unit known as a baud. The baud is the

number of times per second the line condition can switch from "1" to "0". Data rate and transmission speed , which is expressed in terms of bits per second, usually are not the same, as several bits may be transmitted through the channel by the modem in each signal change (a few bits can be transmitted as one symbol).

Claude Shannon showed, in 1948, that the maximum capacity (bit rate) of a bandwidth limited transmission line with limited signal to noise ratio is:

$C = W * log (1 + S/N) / log (2)$

Where C is the maximum capacity, W is the limited bandwidth and S/N is the power of the signal to noise ratio.

A telephone line, for example, has a bandwidth of 3000 Hz and maximum S/N of about 1000 (30db). Thus the theoretically maximum data rate that can be achieved is about 30 K bps (bits per second). Earliest modems that work through telephone lines had 1.2 K bps. Today's modems reach data rates of 28.8 K bps.

2.10 HOW MODULATION IS USED FOR DATA TRANSFER ?

Any technique of the various modulation methods discussed previously or even any combination of these methods (integrated modulation method) can be used for data transfer.

For example we shall look at the following table:

relative amplitude	phase shift	bit meaning	symbol value
1	45	0 0 0	"0"
1	135	0 0 1	"1"
1	225	0 1 0	"2"
1	315	0 1 1	"3"
2	45	1 0 0	"4"
2	135	1 0 1	"5"
2	225	1 1 0	"6"
2	315	1 1 1	" 7"

Table 1: Data transfer

In this example a combination of differential phase modulation and amplitude modulation is used. Each symbol is represented by a certain amplitude and phase shift. The transmitting modem is combining 3 succeeding bits in to one transmitted symbol. The receiving modem interprets each detected symbol to 3 succeeding bits. For the data sequence 10100101011001010, the transmitted symbol' sequence will be: 6 4 5 1 2.

Chapter 3
VHDL

VHSIC Hardware Description Language

3.1 Introduction

VHDL is an acronym which stands for VHSIC Hardware Description Language. VHSIC is another acronym which stands for Very High Speed Integrated circuits. Hardware description language can be used as an alternative way of representing a circuit diagram foe a digital circuits[Perry,1991,P1-2].In other world VHDL can be used to describe circuits for simulation and synthesis [Accolade,1996,p1].Structural behavioral representation of VHDL are two of describing a model of a digital system.

VHDL can be used for documentation, verification, modeling, simulation and synthesis of large digital design. This is actually one of the key features of VHDL, since the same VHDL code can archive all these goals, this saving a lot of effort and reducing the introduction of the error between translate a specification into an implementation in additions to being used for each these purpose, VHDL can be used to take three different approaches to describes hardware. These three approaches to describe are the structural, date flow, and behavior methods of hardware description. Most of the time during this project, a mixture of the three methods are employed and complete design will have different section expressed in different ways. The term RTL (Register Transfer Large) is sometimes used for behavioral/data flow.

A language capable of such diverse applications has a lot of keyboards by this project only use a small subset of the full language. it also means that there is often have then are way of designing in VHDL, software tools that compile, simulate and synthesis the VHDL module will work with the entire language as defined in official Language Reference Normal (LRN) but there will be some specialist tools that require contains

subsets on a particular methodology to be adhered to. This is most often seen in synthesis tools(synopsis used in this project) that try automate the conversion of behavioral to structural. Implementation tools that are targeted to a particular type of hardware such as synopsis may well have we restriction and some of the less expensive VHDL tools ways completely core the language.

Peak VHDL for instance is a VHDL compiler and simulator tool that runs on PC it has several restrictions. In practice such tool will still allow useful work to be done, within their target environment so the restrictions are rarely too severs.

3.2 Advantages

VHDL offer the following advantages for digital design:

- **Standard**: VHDL is EKE standard. Just like any standard (such as graphic X-window standard, bus communication interface standard high level programming language and so on, it reduce confusion and make interface between tools, companies product easier Any development the standard would here better chances of lasting longer and have less chance of becoming absolute due to incompatibility with others.
- **Industry support.** With the advent of more powerful and effective VHDL tool has come the growing support of the industry companies use VHDL tools not only with regard to defense contracts but also for their commercial design.
- **Portability:** The same VHDL code can be simulated and used in many design tools and not different design stage of the design process. This reduce depend on a

set on a set of design tools whose limited capability may not be competitive in late market. The VHDL standard also transforms design data much easier trak a design database of a proprietary design tool.

- **Modeling capability:** VHDL was developed to model all level of design from electronic boxes to transistor. VHDL can accommodate behavioral constructs and mathematical routines that describes complex models, such as queuing networks and analog circuits. It allows use of multiple architecture and associates with the same design during various stages of the design process.
- **Reusability:** certain common design cab be described verified and modified lightly in VHDL for future use. This eliminate reading /marking changes to schematics pages, which the consuming and subject to error .For example, a parameterized multiplier VHDL code can be reused easily by changing to width parameter so that the same VHDL code can be do either 16 by 16 or 12 by 8 multiplication.
- **Technology and Foundry Independence:** The functionality and behaviors of the design can be described with VHDL and verified making foundry and technology independent. This frees the designer to proceed without having to wait for the foundry and technology to be selected.
- **Documentation:** VHDL is design description language which allows documentation to be located in a single place by embedding in it the code. The combining of comments and that actually dictates what the design should be reduces the ambiguity between specification and implementation.

- **New Design Methodology :** Using VHDL and synthesis creates a new methodology that increases the design productivity ,shortens the design cycles and lower costs .It amounts to revolution comparable to that introduced by automatic semi-atoms layout synthesis tools of the last for years

3.3 New Design Methodology

Introducing VHDL and synthesis enables the design community to explore a new design methodology. The traditional design approach starts with drawing schematics and then perform functional and timing simulation based on the same schematic. If there is any design error, the process iterates back to up date schematics. After the layout, functions and back –annotated timing are verified again with that same schematics. The design is functionality described using VHDL.

VHDL simulation is used to verify the functionality of the design. In general modifying VHDL source code is much faster than changing schematics. The allow designer make faster functionality correct design, to explore more architecture trade offs and to have more impact on the design. After the function match the requirements that VHDL code is synthesis to generate schematics (or equivalents halt list).The nets list can be used to layout the circuit and to verify the timing requirement (both before and after the layout. The design changes can be made by modifying VHDL code on changing the contains (timing, area and soon) in the synthesis. The new design approach and methodology has improved the design process by shortening design time, improved the

design process by shortening design time, reducing the number of design iterations and increasing the design complexity. That designer can be change.

3.4 Hardware Abstraction

VHDL is used to describe a model for digital hardware device. This model specifies the external view of the device an one or more internal views. The internal view of the device specifies the functionality or structure, while the external view specifies the interfaces or device through which it communicates with the other models in its environments.

The device-to-device model mapping is strictly one to many. That is a hardware device may have many device models, for example, a device modeled at high level of abstractions may not have a clock as one of its inputs, since the clock may not here been used in description. Also data transfer at the interface may be treated in terms of for example integer value instead of logical values. In VHDL each device model is treated as a digital representation of a unique device, called an entity in the text.

3.5 Element

Construct of VHDL language are designed for describing hardware components, packing parts and utilities and used of libraries. Besides it is also designed for specifying design libraries and parameters .In the simplest form the description and architecture of

component in VHDL consists of an interfaces specification and an architecture specification.

- *Interface specification* begin with the entity keyword and contains the inputs – output parts of the component. The external characteristic of a component such as time and temperature dependencies can also be included in the interface description.
- *Architectural specification* begins with the ARHITECTURE keyword, which describe the functionality of component. This functionality depend on the input-output signal and other parameters that are specified in the interface description several architectural specification with the difference identifiers can exists for one component with a given interface description.

3.6 Basic Concept

Because VHDL is language foe hardware description .It has features which are conceptually different from those of the software language. These features are representing the special characteristic of hardware component and carries.These main features of hardware description language are timing and cancurrency.

3.6.1 *Timing*

Timing is associated with values that are designed to hardware carries.Signal in VHDL represent the real wires ,where the delays associated with transfer of values through wire are concern, thus the assignment to signal in VHDL involved timing, consider the assignment in software as shown below

a = x;

b = c;

These is only consider the value transfer from k to a and b and ignore the timing of such transfer.

3.6.2 *Concurrency*

Concurrency refers to the simultaneous operation of various hardware components. The VHDL has constructs that allows a virtually concurrent environment to be created. These constructs satisfy concurrency required for the description of hardware. Through the use of concurrent constructs, timing of inter connecting signals and under of simulation construct or component a VHDL simulator names is think that the execution is being done concurrently.

3.7 Object and Classes

An entity that has a value of a given type is object, port signals, loops index variables, signal for interconnecting components,temporary variables and files are some of the VHDL objects.There are for class begin VHDL

- Signal
- Variable
- Constant
- File

An object may be one of these classes:

- *Objects of the signal class* represent the hardware wire and more timing associated with them. Values assigned to a signal are placed on the signal after a specified delay value.
- *Object of the variables class* **are** for storage of temporary values and here no hardware significance. Variable can only be declared on have values assigned to them in sequential bodies of VHDL.
- *Objects of the constants class* represent the values of a given type. They can be declared and used in concurrent and sequential bodies. The value given to the constants cannot be changed.
- *Object of the files class* contains data of the same type. They can also be declared and used in both concurrent and sequential bodies.

3.8 Signal Assignment

Assignment of values to signals in sequential and concurrent bodies is an important issues in VHDL .It its simplest form a signal assignment consists a targets signal on the left hand side of a left arrow and an expression for defining a value term on the right hand side be assigned to the left –hard side after a delta time. An assignment can include an after clause specifying that a physically fine delay occurs before the assignment for the left hand side takes places. Signal assignment can have inertial with reject and transport mechanism.

3.9 Signal Driver

A signal has driving value and there are may be several pending timing action on this signal wanting to become correct .When a transaction become current, its value become the driving value of the signal. Assignment to a signal in multiple concurrent bodies create multiple drivers to the signal. Such a signal must be resolved and a resolution function must exist to are solve the value from multiple driving values.

3.10 Packages

Often in a hardware design environment it because necessary to group component or utilities used for description of components. Examples of VHDL constructs for describing utilities and environments are type definitions and subprogram. Components such utilities can be grouped by used of packages.

Chapter 4
Analysis and Design

4.0 Fax Modem Design

In typically industrial processing Fax Modem design there are several steps of designing digital system. Initially the design stars with a design idea. A more complete definition of the intended hardware must then developed from the initial design idea. Therefore it is necessary to generate a behavioral definition of the system under the design. In this stage the overall functionality the input output mapping and the functionality specification will be decided. The next phase is to design the data path of the system. The data path of the interconnected components is developed.

Then the logic design will takes place where implementation of the hardware blocks using primitive gates is conducted using the VHSIC Hardware Description Language. Finally the central fax modem design will be tested and simulated to perform waveform using the Xilinx Software.

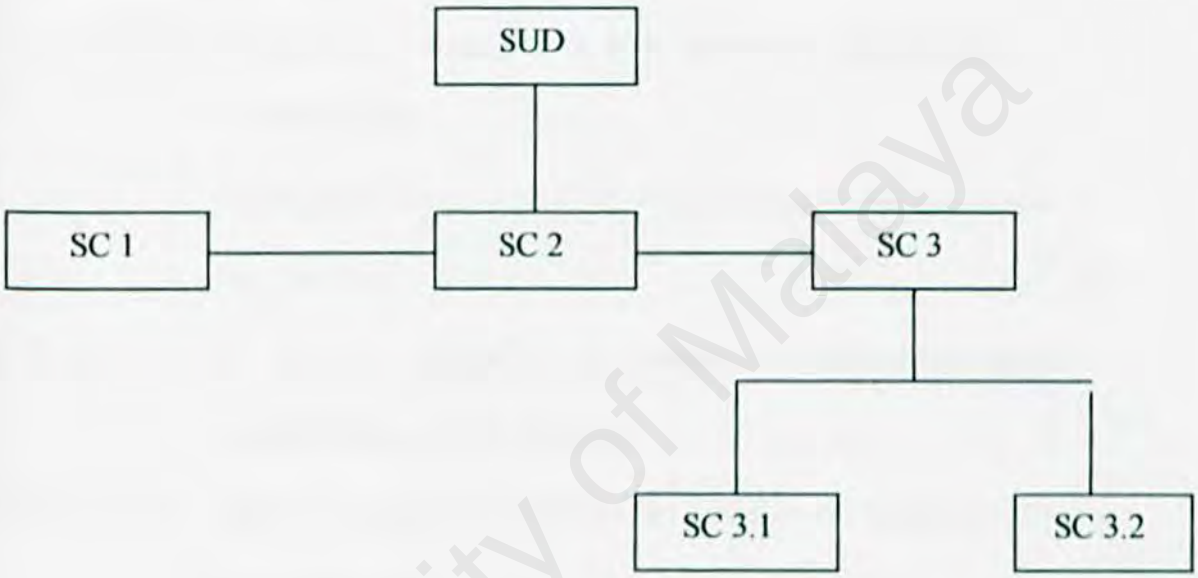
4.1 Design Analysis

In this processing unit fax modem design, there are two methodologies that will be used to make the design a success. These methodologies are typically digital system as mentioned above and top down design together with VHSIC Hardware Description Language.

4.1.1 Top Down Design

A top down design is a design technique that recursively partitions a system into its sub-components until all sub- components become manageable design part.

Mapping to hardware depends on target technology available libraries and tool. Generally a system can be partitioned into its simpler components. Figure 4.1 show the top design and bottom up implementation



SUD : System Under Design

SC : System Component / System Sub-Component

Shaded area designate sub- component with hardware

Figure 9: Top- Down design and bottom –up implementation.

4.1.2 Planning A Program

The first step in writing a program is to derive an overall plan of attack.This should be envisioned as a step-by- step procedure, such a functional description of task is called algorithm. It is also similar to a cook recipe but more precisely defined. In particular, an algorithm has five properties:

1. **Finiteness** : An algorithm must terminate after a finite number of steps.
2. **Definiteness :** Each step of the algorithm must be precisely defined and unambiguous.
3. **Input** : An algorithm may or may not require some initial qualities to be specified.
4. **Output** :An algorithm has one or more outputs which related to input or characteristics of the algorithm.
5. **Effectiveness** : The out come of an algorithm has a predictable result which has an application.

4.1.3 Flow Charts

Flow charts are a schematic representation of the flow information through the component of processing system. At some point in the program development, it is desirable to construct flow chart of the program.

4.1.4 Design with VHDL

In real design environment, synthesis tools, complex library elements and a set of configurable part are available as to manageable parts.

Synthesis tools : Present synthesis tools are capable of translating high level hardware description into an interconnection of logic cells of FPGA layout. Example of synthesis tools is combinatorial circuits.

Libraries : Prepackaged libraries are available in most technologies. In fact libraries consist of pre-designed, tested and commonly used functional units. Example of library element are multiplexer, flip-flop and IC.

Interface Description : At the top level, a system can be described by its interface description, which can be characteristic of the system.

Architecture Description : The functionality of the component is described in VHDL architecture bodies. This description can be in term of other components on in the form of definition that specifies the from data form input to the output the circuit (input –output mapping)

Dataflow : Data flow is referred to the description where functionality of hardware is mainly described in term of data flow through buses ,logic units and registers.

Behavioral Description : At this description, the concern is on assigning appropriate value to circuit output. The structures of the circuits and the details of the hardware in which the data flow are out of concern. At this level of abstraction ports of model correspond to the actual input and output of the actual circuit .

Configurable Ports : Pre –designed part in the previous design can be used in the current design by reconfigured them.

4.1.5 Design Scenario

Analyzing The Requirement : The design begins with analyzing the requirement and developing a simulatable model of the system. The interface description and behavioral description are developed in this stage. Before taking the next step, the behavioral description is simulated.

Design Implementation: After verifying the behavioral description by simulating it, the code must be studied for generating the general layout the design. Specifying for the be implemented by a correspondence hardware. After identity the available components, the VHDL description will be developed to study the way of designing them.

Final Implementation : The VHDL source code will then be test simulated using the Xilinx Foundation Software.

4.2 Design Idea

The aim is to design and implement fax modem of the following :

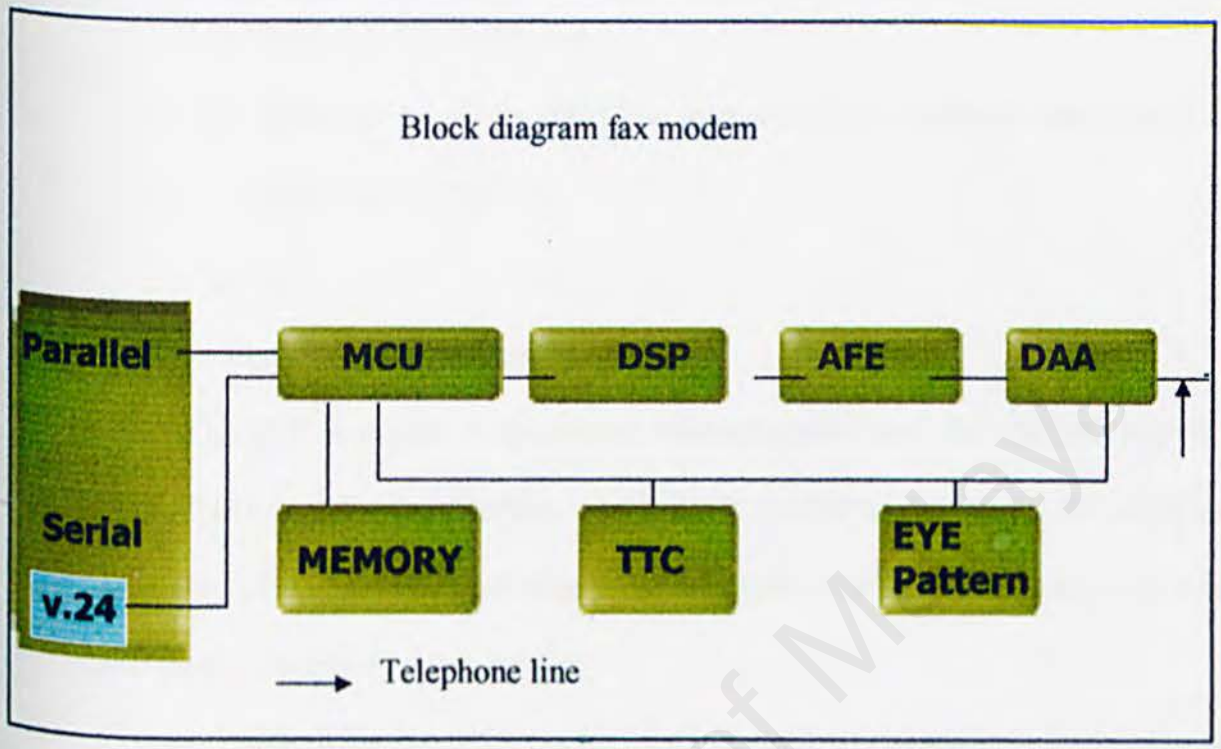


Figure 4.2 Block diagram fax modem

Functionality of module in fax modem :

- **Mcu (microcontroller unit)**

  Some modem contain a dedicated microcontroller interface to RS 232.The microcontroller perform the following functions :

  - At parsing and execution.
  - Call progress monitoring such as monitoring for the presence of dial, busy answer and facsimile calling tone. The microcontroller detection does not perform tone detection. Detecting tone is DSP function. The DSP report the tone detection results to microcontroller that take suitable action.

- Handshaking. The DSP perform the signal processing function that form handshaking. The microcontroller monitors the progress of handshake and makes decisions on moving to the next or previous state of a state machine.
- Data link layer protocols.
- Sending / receiving data: The microcontroller retriever data from Pc and Pc send data to DSP.

• DSP – Digital Signal Processing

The DSP is usually a specialized microprocessor and that perform high complex math functions. In the modem world, DSP techniques improve the accuracy and reliability of digital communication sometime called modem data pump. It is where the real magic is performed in a modem.

A DSP is able differentiate between orderly data signals and noise, which is in herently croatic. Noise is hence of communication engineers. DSP dramatically improves the sensitivity of a receiving unit if an incoming signal is analog (for example a standard modem) the signal it first converted to digital form by the AFE. The resulting digital signal has two or more levels. Ideally these level are always predictable, exact voltages or current.

However because the incoming signal contains noise, the levels are not always at standard values. The DSP circuit adjust the level so they are at the correct values, which practically eliminate the noise.

DSP techniques are also used to modulate data onto carrier signal and demodulate that data from the carrier signal.

• **AFE – Analog Front End**

The Analog Front End (AFE) perform both analog to digital (ADC) and digital –to-conversion DAC.AFE is some the called the modem codec- coder/decoder. Particular data protocol and data rates (speed) of the modem signal determine the precession or signal resolution characteristic of the AFE.

• **DAA –Data Access Arrangement**

The Data Access Arrangement interfaces the modem to phone networks. This interface is required by the FCC and PTT through the world to provide safety protection both to end user and to telephone switching lines. DAA's usually consist of discrete components and provide many features, including voltage isolation detect caller ID signal detect ring and perform an –hook and off hooks function.

These solid state DAA's typically reduce component count board and power conception but may be too expensive for cost sensitive low speed modem application.

• **EYE PATTERN OR CONSTELATION**

The modem signal can be represented on an X-Y oscilloscope as dots which fall into four quadrants (+/+ , - / + , -/- , and + / -).Each dot represent an amplitude and a phase of the signal at a given point in time.

The resultant display is called the constellation, eye pattern. The eye pattern is used a visual way of determining the quality of a modem is signal. Sharp steady dots on an oscilloscope represent " clean " modem signal. A modem signal that is less than ideal

may be seen a fuzzy dots that have move around quite a bit and a constellation may be rotated.

- **TTC – Timing , Trigger, Control.**

TTC is interface between all the data acquisition sub system control element and global trigger sub –system. The clocking and trigger information for all those sub – system is provided through their connection to TTC.

The TTC sub – system provides also the means foe data acquisition sub system control elements to generate commands and data to be transmitted to front end electronics controller. It provides the fast controller for all the data acquisition sub –system (broad cost commands).It can also used to transmit individual parameter (addressed command).

- **MEMORY (RAM ,ROM)**

RAM – for temporary storage of data being processed.

ROM - to store the modem software.

- **V.24 / RS 232**

Converters are used for potential separation between two devices with RS 232 interfaces. The high quality potential separation improver the immunity to interface interference and doubles the transmission distance at the same time. The plug modules differ by the type of RS 232 connector (male/female).

- **Telephone Line**

The connection to the phone line is through a RJ – 11 jack.

4.2.2 Overview of fax modem chip

The main operation of fax modem chip are :

- Modulator / Demodulation
- Filtering
- Error control
- Data Compression
- D/A and A/D conversion for transmitting and receiving data.

4.2.3 Operation flow of modem card

Transmit Path	PC > UART > MCU > DSP > AFE > Interpolator > DAC > DAA.
Receive Path	DAA > ADC > Decimator > AFE > DSP > MCU > UART > PC.

Table 2 :Operation flow of fax modem card.

Interpolation.

Interpolation is used also in codes to creates a high performance DAC. This basically increase the output frequency of low resolution analog output.

Decimation

The process of converting short words at high frequency to longer words at slower rate with input signal over sampling at a very high rate reducing the final output code frequency will make the computations more manageable. This reduce the effective the effective sampling at the ADC output.

4.3 Structural Design

In structural design the description lists the ports of the system and their interconnections. The functionally of the components is not parts of the description.

Advantages:

- When synthesizing the design all of the VHDL blocks are flattened (collapsed into one blocks and it is possible that the resulting logic may be more efficient.
- The structural VHDL code is more portable to other design system than a schematic.

Disadvantages:

- Writing structural VHDL code can be none error prone than creating a schematic. This is because the possibility to misplace a net when there is no' picture' to go with.
- The resulting flattered net list can be more difficult to debug.

4.4 Modem Control Logic

Modem control logic has mainly two functions. Firstly, it purpose is to perform handshaking with RS 232 input. Subsequently it is second function is able to provide the state or status of the device that connecting to the UART. This module will operate based on two important register that is modem control register (mcr) and modem status register (msr).

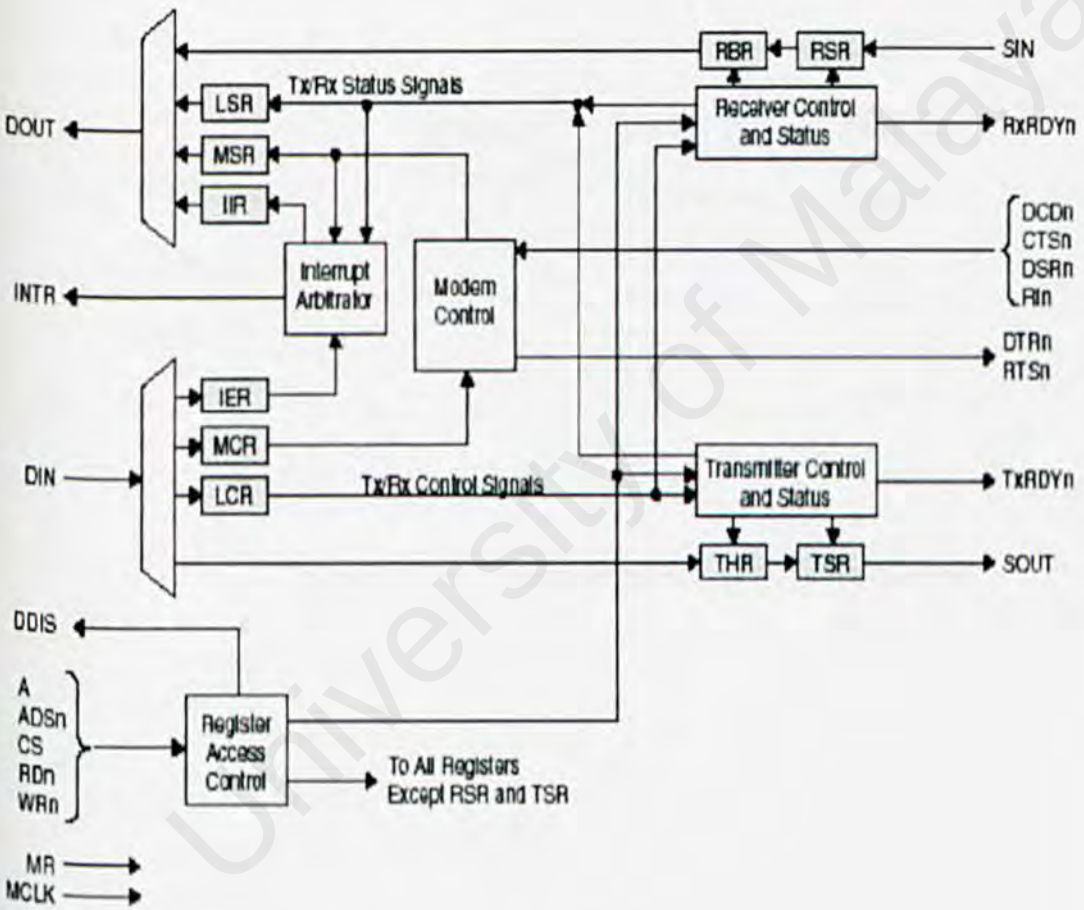


Figure 11 : UART Block Diagram

4.5 Modem Control Logic Module

In this module, there are two register involved in the implemented. They are MCR and MSR. This module special function that is handshaking with external device that connected to RS 232 port for communication with a workstation. Here we shall see the implementation of this module.

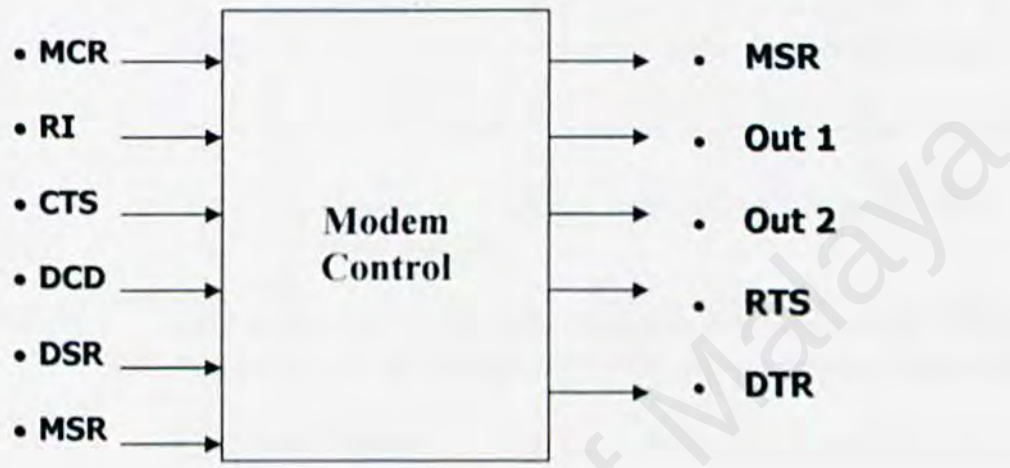


Figure 12 : Block diagram of Modem Control

Pin description Modem Control

CTS	One bit input. This signal active low based on RS 232 protocols. It is used to indicate that transmission can begin.
CLK	One bit input port. It is global clock signal. It determine the speed of the system in UART
DCD	One bit input port. This signal is active low based on RS 232 protocol. It used to indicate the determine of the data arrived at received line.
DSR	On bit input port. This signal is active low based on RS 232 protocol. It used to indicate the received data is ready to be sent to receiver of UART
MSR	One bit input port. It used to acknowledge the processor has read the MSR
RESET	One bit input port. It is global reset signal it is active most register and output signal are cleared.
RI	One bit input port. This signal is active low based on RS 232 protocol. It is used to attempt the communication between external device and PC
MCR	8 bit input register. It contains command from processor in order to communicate with external device.
DTR	One bit input port. This signal is active low based on RS 232 protocol.
RTS	One bit input port. This signal is active low based on RS 232 protocol.
MSR	8 bit output register. It contains the status from external device in order to communicate with processor

Table 3 : Pin Description

MODEM Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	RTS	DTR

Table 4 : Modem control Register

Loopback mode for testing (Bit 4), Auxiliary user-defined output Out2 (Bit 3) and Out1(Bit 2) are removed, because it can be implemented with in-system programmability (ISP)

DTR:

This bit controls the Data Terminal Ready (DTRn) output.

DTR=0: force DTRn output to a logic 1 (normal default)

DTR=1: force DTRn output to a logic 0

RTS:

This bit controls the Request to Send (RTSn) output

RTS=0: force RTSn output to a logic 1 (normal default)

RTS=1: force RTSn output to a logic 0

MODEM Status Register (MSR)

Modem Status Register (MSR) provides maodem status information of a control line.

Bit	Description
0	**Delta Clear To Send (delta_cts)** '1'= The CTS line has changed its state
1	**Delta Data Set Ready (delta_DSR)** **'1'**= The DSR line has changed its state
2	**Delta Ring Indicator (delta_RI)** '1'=The RI line has changed its state (from low to high)
3	**Delta Data Carrier Detect (delta_DCD)** '1'= The DCD line has changed its state
4	**Complement of Clear To Send (comp_Cts)** Complement of CTS or Equals to RTS in loop back mode
5	**Complement of Data Set Ready (comp_DSR)** Complement of DSR or equals to DTR in loop back mode
6	Complement of Ring Indicator (comp_RI) Complement of RI or equal to OUT 1 in loop back mode
7	**Complement of Data Carrier Detect (comp_DCD)** Complement of DCD or equal to OUT2 in loop back mode

Table 5 : Modem Status Register Description

Flow Chart Modem Control

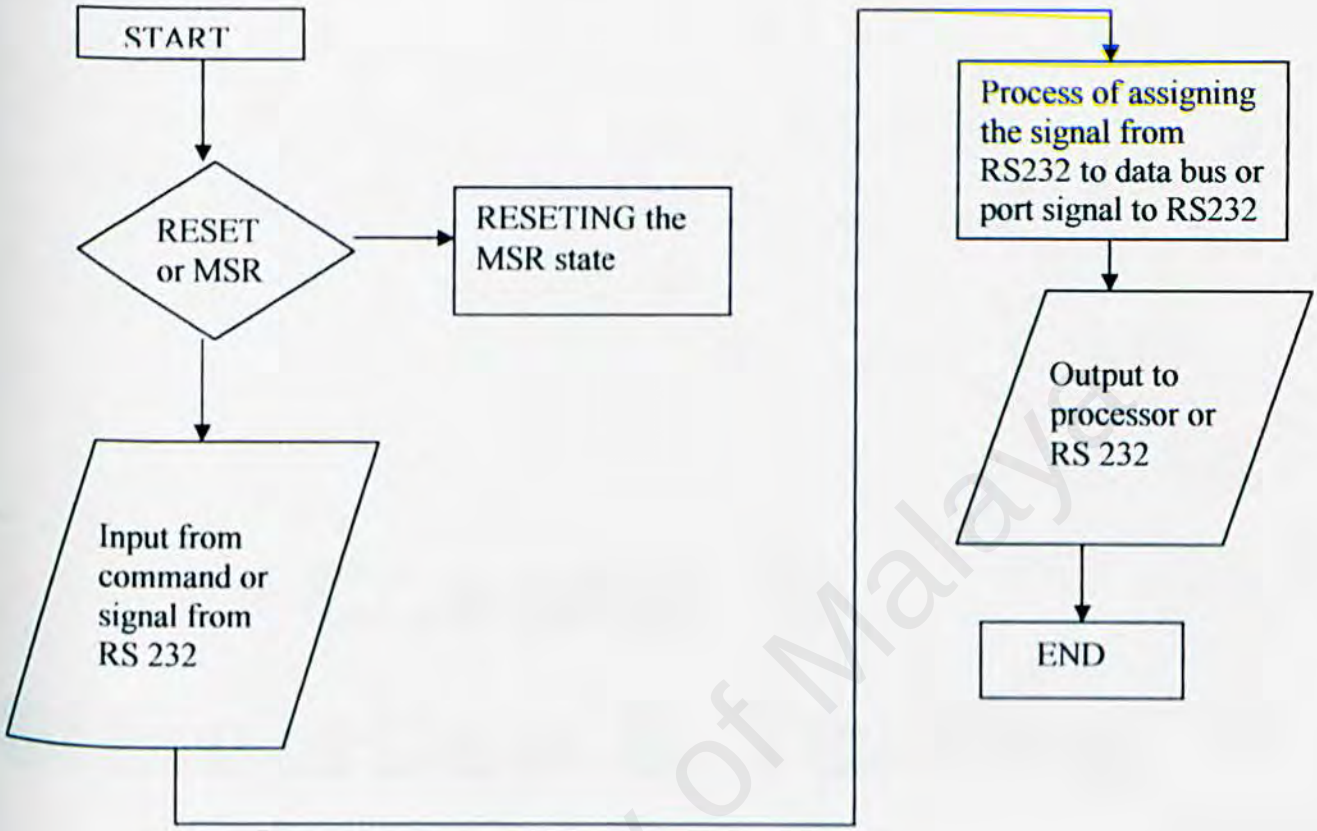


Figure 13: Flow chart of Modem Control Logic

Chapter 5
Simulation & Testing

5.0 Development and Testing

5.1 Introduction

In this phase the design will be used to develop the module control modem. The design will develop using the Field Programmable Gate Array Gate (FPGA) software. From the design the modules will be developed. By using the software we can develop, compile simulate and test the design A test bench provided by " Logic Simulator" simulation tools will be used to feed inputs to the designed logic gates and generate the output waveforms to verify the theoretical characteristics of the designed modem control.

5.2 Module Development

Figure 14: Module Control

5.2.1 Signal (Pin Decriptions)

Pin Name	Type	Pin Description
CTSn	In	Clear to Send, low active. Indicates that the modem is ready exchanged data
DSRn	In	Data Set Ready low active. Indicates that the MODEM is ready to establish the communication link with the UART
DCDn	In	Data Carrier Detect, low active. Indicates that the data carrier has been detected by MODEM
RIn	In	Ring Indicator, low active. Indicate telephone ringing signal has been received by the MODEM
RESET	In	One bit input port. It is global reset signal. When it is active high, most register and output signal are cleared.
MCR	In	2 bit input register. It commands from processor in order communication between with external device.
MSR	Out	8 bit output register. It contain the status from external device in order to communication with processor
DTR	Out	Data Terminal Ready. When low this informs the MODEM that UART is ready to establish a communication link
RTSn	Out	Request to Send. When low, this informs the MODEMS that the UART is ready to exchange
CLK	In	One bit input port. It is global clock signal. It determines the speed of the system in UART.

Table 6 : Pin Description

5.2.2 Output Modem Control

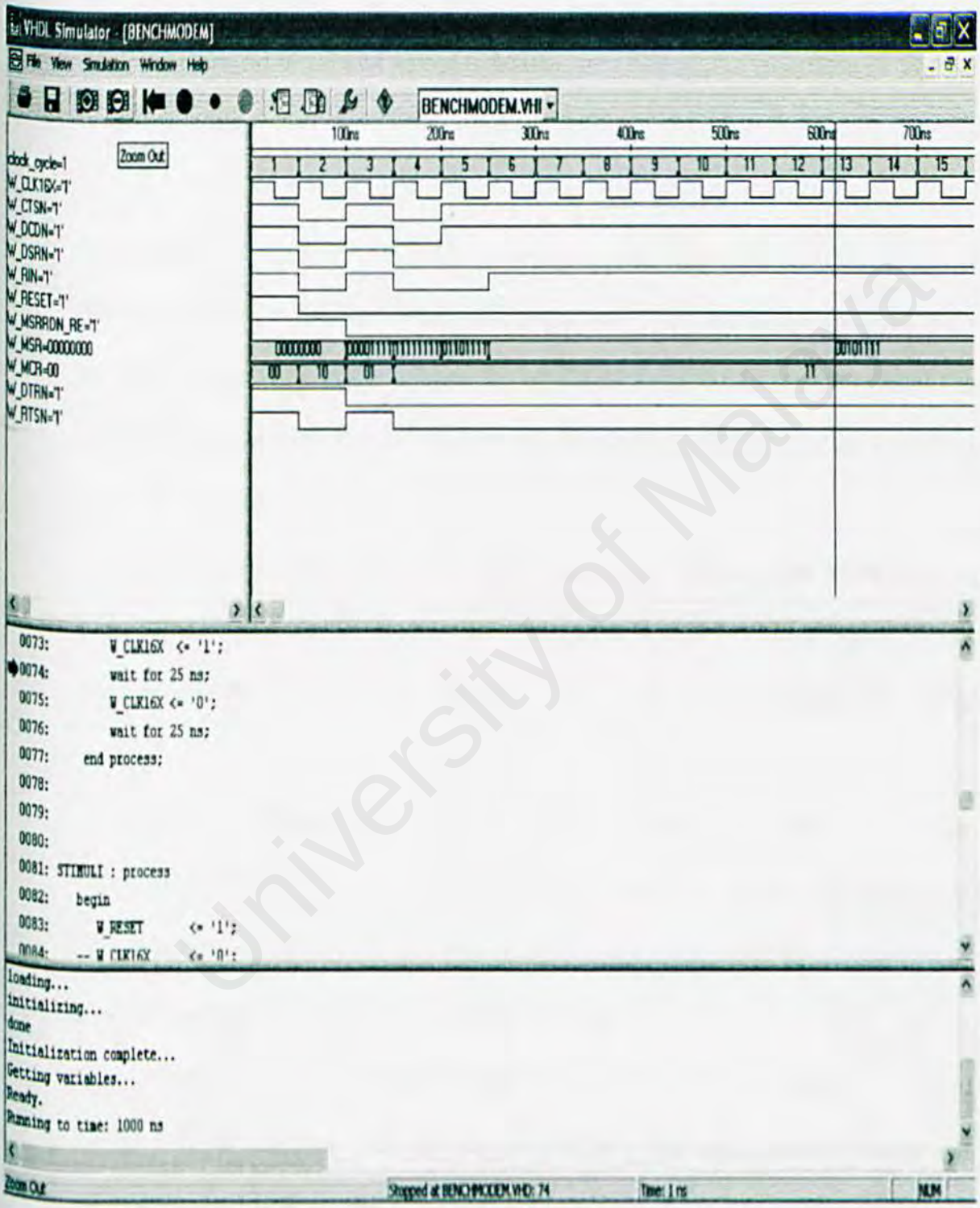


Figure 15 : Output Modem Control

5.2.3 Brief Explanation

Modem, MCR (modem control register) control the outputs state of DTRn and DTRn.The lines status of DCDn,CTSn,DSRn, and RIn are monitored by the MODEM control block and stored in MSR.

MCR is set :

DTRn <= not MCR (0)

RTSn <= not MCR (1)

Thus,MCR [1:0] = "00" the output will come out = "11" which is it stand for RTS and DTR.When DTR low it informs the MODEM that UART is ready to establish a communication link. When RTS low it informs the MODEM that the UART is ready to exchange data.

For MSR when RESET = 1 it clears register and control logic when input is high. When input for W_CTS,W_DCD,W_DSR,W_RIN = 1111_b"input it not changed and get W_MSR[7:0] "0000000_b" this is because MSRRDN_RE = '1'at 100ns.

When MSRRDN_RE = '0' data input for "W_CTS,W_DCD,W_DSR,W_RIN = "1111_b" and the output will come out W_MSR[7:0]="0001111_b"after 100ns .This is because bit 3-0 is set to 1 and bit 4-7 as complement forCTSn, DCDn,DSRn,RIn input.

When MSRRDN_RE = '0' data input for"W_CTS,W_DCD,W_DSR,W_RIN = '$0000'_b$, the out put will come out W_MSR [7:0] = "11111111" at 150ns,for input "W_CTS,W_DCD,W_DSR,W_RIN = "1100_b" the output is W_MSR [7:0] =

"01101111_b" and when input for"W_CTS,W_DCD,W_DSR,W_RIN = "1101_b" the output is W_MSR [7:0]="00101111"

CTSn,active low it indicates that the MODEMS is ready to exchange data.DCDn, active low it indicates that the data carrier has been detected,DSRn active low indicates that the MODEM is ready to establish the communication link with the UART.RIn, active low indicates that a telephone ringing signal has been received by the MODEM.

If the processor ready to receive data it would reply by set MCR (1) to logic 1.Then DTR is set.UART is ready to receive and wait for signal that is DSR and DCD..So we are able to see hand shaking process. For more detail for output MSR,we refer to the MSR,MCR description,

MODEM Status Register (MSR)

Modem Status Register (MSR) provides modem status information of a control line.

Bit	Description
0	**Delta Clear To Send (delta_cts)** '1'= The CTS line has changed its state
1	**Delta Data Set Ready (delta_DSR)** **'1'**= The DSR line has changed its state
2	**Delta Ring Indicator (delta_RI)** '1'=The RI line has changed its state (from low to high)
3	**Delta Data Carrier Detect (delta_DCD)** '1'= The DCD line has changed its state
4	**Complement of Clear To Send (comp_Cts)** Complement of CTS or Equals to RTS in loop back mode
5	**Complement of Data Set Ready (comp_DSR)** Complement of DSR or equals to DTR in loop back mode
6	Complement of Ring Indicator (comp_RI) Complement of RI or equal to OUT 1 in loop back mode
7	**Complement of Data Carrier Detect (comp_DCD)** Complement of DCD or equal to OUT2 in loop back mode

Table 7 : Modem Status Register Description

MODEM Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	RTS	DTR

Table 8 : Modem control Register

Loop back mode for testing (Bit 4), Auxiliary user-defined output Out2 (Bit 3) and Out1 (Bit 2) are removed, because it can be implemented with in-system programmability (ISP)

DTR:

This bit controls the Data Terminal Ready (DTRn) output.

DTR=0: force DTRn output to a logic 1 (normal default)

DTR=1: force DTRn output to logic 0

RTS:

This bit controls the Request to Send (RTSn) output

RTS=0: force RTSn output to a logic 1 (normal default)

RTS=1: force RTSn output to a logic 0

5.3 Development of the Top Level Design.

After the modules are tested the development of the top level design are initiated. The comprised of listening the module together to form one working top level module and compiling it so there will be no syntax error or what development stage of the control. The layout of the top level design can be in the appendices section.

5.4 Synthesis

After the modules or entities are described, the next step is to synthesis the entities. It is a process translation and optimization in digital design. For example, layout synthesis is from of data that facilities placement and routing, resulting in optimizing timing and or chip size. Logic synthesis, in other hand is the process of taking a form of input (VHDL),translating it into a form a Boolean equations and synthesis tools specifies and then optimizing in propagation delay and or area.

After the VHDL code is translated the optimization process can be performed based on constraints such as speed area power and go on. After the synthesis process completed the whole module will be simulated to testify that behavior of modem control is correct. Simulation and test done will be discussed in this section.

5.5Test and Simulation

5.5.1 Introduction

Test and simulation are carried out in the next stage of development. Test is conducted on module control to determine the workability according to their code. The test comprised of few steps which is syntax checking functional simulation and timing verification.

5.5.2 Error Checking and Syntax Checking

The coding is check for any syntax error, starting from the design entry which in form of HDL (Hardware Description Language).This checking is done with all the modules by using FPGA series HDL editor. After syntax checking return no error the HDL code then being added to the project. From this we can conclude the steps and more on to the next step of development that is synthesizing

5.5.3 Functional Simulation

This simulation is done after the synthesis process is completed. The simulation test at the functional level to testify the behavior of the control is correct. Thus simulation is done by using event driven stimulator.

5.5.4 Implementation

In the implementation stage phase verification of timing accuracy is done by using static timing analysis tool and this is important at gate level timing stage

5.6 VHDL Design Verification

The next step is simulation and it done after the model description is successfully compiled. A simulation can be done on either one of the following.

- An entity declaration and architecture body pair
- A configuration

Then actual simulation commence on two phase.

i) Elaboration Phase

The entity expanded and linked according to its hierarchy, component are bounded to entities in library and the top – level is built as network af behavioral models is ready to be simulated.

ii) Initialization Phase

Driving and effective values for all explicitly declared signals are computed, implicit signal are signed values, process are executed until they suspend and simulation time is set to 50 ns.

In this design step the VHDL description for each module of the control had been created and ready to be simulated to insure proper logic functionality. By using script file that can be generated from FPGA script editor in order to do the simulation. It is uses

text file as input which contains the header information for the VHDL file such as port maps.

5.7 Testing

In order to determine that the hardware developed really works a set of test were done to each module or entities that involves. To get the expected result a set of data were chosen to be assign as the inputs values.The data will determine whether the entity working as it should be or not.

Chapter 6
Discussion

6.1 Problems

During the development stage of the project there are several problems faced and each will be described as below:

1) Learning Process

The problem faced here is learning VHDL the languages will take time to familiarize with syntax and so on. Thus learning VHDL took much of time expected in developing the control. Much time spent on referring to manual on coding VHDL instead starting writing the codes. The causes of this problem lack of time to study the languages properly ,limited references available that time and not having the good foundation in programming language also contributes to this problem.

2) Coding Problems

Because of many modulates that involve, some time syntax error always occurs during writing the codes. This is due to the lacks of VHDL programming knowledge and references. One major syntax error that occurs is net list loaded with warning. This is cause by type mismatch of entity name with the declared name in component part of other entity. This problem easily solved by changing the name so it is identical.

3) Limited Resources and References

As well all know that VHDL is a new language that getting much support from the industry. It is a tool makes modeling hardware much simpler and easier. Thus resources are very limited on the limited on the VHDL and its standard. There are much references book that available in store and library .If it available the user level are for the advance user. This cause problem for beginner user. Besides that VHDL are taught in faculty syllabus their although now the faculty just made we it as one of the compulsory subject for the student.

4) Hardware and Software

From the experience that I've been through develop VHDL require much, firstly I suggest to used Xilinx Software.But due to Xilinx Software I changed the use software to FPGA because of it easy usage and understanding

6.2 Solutions and Recommendations

To solves the problem faced, several of these solutions and recommended should be should be considered.

a) Making VHDL as a tolls foe developing hardware in faculty encourage students to developed hardware using this tools for broadens their know ledges of computer hardware.

b) Improve the facilities of the laboratory or set –up a proper laboratory for hardware development in near future so there will be no shortage in skilled computer engineering computer students in future come.

c) Lecturer should always encourage students to involves in computer hardware project then move to software side because it proven that nearly half student doesn't know that the computer hardware and architecture very well.

d) Improve the implementation gathering systems so finding resource much easier such having own family library instead of a small document room

e) Try to buy a new VHDL tolls so the development not limited to a certain constrains buying software like Aldec Active HDL would be an advantage because this software can do simulation and synthesis much faster than the FPGA

6.3 Future Enhancement

The design of this controller is not perfect. For future enhancement the are few feature can be added such as

i) Move compatible for other hardware also such as thumb reader.

ii) Modify the controller so it can support other hardware peripherals so it can function as one.

iii) Clean up the coding so there will be no delays created due to their prefect codes.

iv) Try to implementing it by downloading into FPGA chip and test it to determine the functionally of the chip.

However, future development of the controller should not only constraints to this design only but depend on the needs.

Chapter 7
Conclusion

7.0 Conclusion

In conclusion the project had taught me a lot starting with the proposal of such project and managing in now to conduct the project so it cover all the objectives within the given time. Second time management without proper time management this project would never be completed on time but I've made it with little trouble.

Experiencing the use of VHDL in modeling a controller leaves me with much benefit for the future come. The languages are tool that made the simulation of model behavior much easier for user through the graphical output, which easier to face any fault in the design.

With help of friends that always around, every problem encountered being resolve through discussion. This problem will be discussed in the next section with solution and recommendations for future use.

Here I've learned that developing source code for certain hardware are more complex then software such as multimedia package because it involve every situation that involve an electronic circuit. Though the result from are true but not in real life. This is because it depends on the circuit in the hardware that can affect the output data.

In whole development modem control using VHDL gave me one useful experience for me. I've learned the technique of designing and developing hardware that I cannot

learn in majoring in general. With this I can apply the knowledge of electronic that I've learned in class to develop such hardware

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Case Study: Testing of IP based – "Mixed Signal Fax Modem System on Chip"

[15] http://www.quicklogic.com/support/anqn/uart.exe

Appendix

```
-- control.vhd

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity Modem is
 port (
   -- Global reset and clock
   Reset      : in  std_logic; -- Master reset
   Clk16X     : in  std_logic; -- UART internal clock

   -- Registers
   MSR        : out std_logic_vector(7 downto 0); -- Modem Status Reg
   MCR        : in  std_logic_vector(1 downto 0); -- Modem Control Reg

   -- Rising Edge of MSR Read Strobe
     MsrRDn_re  : in  std_logic; -- pulse indicating rising of MsrRDn_r

   -- Modem interface
   DCDn       : in  std_logic; -- Data Carrier Detect
   CTSn       : in  std_logic; -- Clear To Send
   DSRn       : in  std_logic; -- Data Set Ready
   RIn        : in  std_logic; -- Ring Indicator
   DTRn       : out std_logic; -- Data Terminal Ready
   RTSn       : out std_logic  -- Request To Send
 );
end Modem;

architecture Modem_a of Modem is

 signal MSReg   : std_logic_vector(7 downto 0);
 signal CTSn1   : std_logic; -- Delayed version of CTSn
 signal DSRn1   : std_logic; -- Delayed version of DSRn
 signal DCDn1   : std_logic; -- Delayed version of DCDn
 signal RIn1    : std_logic; -- Delayed version of RIn

begin

 DTRn <= not MCR(0);
 RTSn <= not MCR(1);

-------------------------------------------
--      Modem Status Register Setup
-------------------------------------------

 MSR <= MSReg;

 Modem_Stat_Proc: process(Reset, Clk16X)
 begin
   if (Reset='1') then
     MSReg <= "10101010";      ------(others=>'1');---- ubah dari 0 ke 10
     CTSn1 <= '1';
     DSRn1 <= '1';
     DCDn1 <= '1';
     RIn1 <=  '1';
   elsif rising_edge(Clk16X) then
     CTSn1 <= CTSn; -- Delay of CTSn
     DSRn1 <= DSRn; -- Delay of DSRn
     DCDn1 <= DCDn; -- Delay of DCDn
     RIn1 <= RIn;   -- Delay of RIn
     if (MsrRDn_re='1') then
       MSReg <= (others=>'0');  ---ubah macam atas
     else
       MSReg(0) <= MSReg(0) or (CTSn1 xor CTSn);     -- Indicate DCDn changes
       MSReg(1) <= MSReg(1) or (DSRn1 xor DSRn);     -- Indicate DSRn changes
       MSReg(2) <= MSReg(2) or ((not RIn1) and RIn); -- Rising edge of RI
       MSReg(3) <= MSReg(3) or (DCDn1 xor DCDn);     -- Indicate DCDn changes
       MSReg(4) <= not CTSn; -- Compliment of CTSn
       MSReg(5) <= not DSRn; -- Compliment of DSRn
```

```
      MSReg(6) <= not RIn;  -- Compliment of RIn
      MSReg(7) <= not DCDn; -- Compliment of DCDn
    end if;
  end if;
end process Modem_Stat_Proc;

end Modem_a;
```

```
-- This testbench was automatically generated

-- Filename          : tb_tmp.vhd
-- Modelname         : benchmodem
-- Title             :
-- Purpose           :
-- Author(s)         : zulianaz
-------------------------------------------------------------------------
-- Version  | Author | Date       | Changes made
-- ----------------------------------------------------------------------
-- 1.0      | zulianaz | 09.08.2003 | inital version

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity TB_MODEM is
end TB_MODEM;

architecture BEH of TB_MODEM is

  component MODEM
    port(RESET       : in std_logic ;
         CLK16X      : in std_logic ;
         MSR         : out std_logic_vector ( 7 downto 0 );
         MCR         : in std_logic_vector ( 1 downto 0 );
         MSRRDN_RE   : in std_logic ;
         DCDN        : in std_logic ;
         CTSN        : in std_logic ;
         DSRN        : in std_logic ;
         RIN         : in std_logic ;
         DTRN        : out std_logic ;
         RTSN        : out std_logic );

  end component;


  constant PERIOD : time := 50 ns;

  signal W_RESET       : std_logic ;
  signal W_CLK16X      : std_logic ;
  signal W_MSR         : std_logic_vector ( 7 downto 0 );
  signal W_MCR         : std_logic_vector ( 1 downto 0 );
  signal W_MSRRDN_RE   : std_logic ;
  signal W_DCDN        : std_logic ;
  signal W_CTSN        : std_logic ;
  signal W_DSRN        : std_logic ;
  signal W_RIN         : std_logic ;
  signal W_DTRN        : std_logic ;
  signal W_RTSN        : std_logic ;
  signal clock_cycle   : natural:=0;

begin

  DUT : MODEM
    port map(RESET       => W_RESET,
             CLK16X      => W_CLK16X,
             MSR         => W_MSR,
             MCR         => W_MCR,
             MSRRDN_RE   => W_MSRRDN_RE,
             DCDN        => W_DCDN,
             CTSN        => W_CTSN,
             DSRN        => W_DSRN,
             RIN         => W_RIN,
             DTRN        => W_DTRN,
             RTSN        => W_RTSN);
```

```
CLOCK: process
    begin
        Clock_cycle <= Clock_cycle + 1;
        W_CLK16X  <= '1';
        wait for 25 ns;
        W_CLK16X <= '0';
        wait for 25 ns;
    end process;


STIMULI : process
   begin
      W_RESET        <= '1';
   -- W_CLK16X       <= '0';
      W_MCR          <= "00";  --(others => '0');
      W_MSRRDN_RE    <= '1';
      W_DCDN         <= '1';
      W_CTSN         <= '1';
      W_DSRN         <= '1';
      W_RIN          <= '1';

Wait for PERIOD;
      W_RESET        <= '0';
     -- W_CLK16X      <= '0';
      W_MCR          <= "10";  --(others => '0');
      W_MSRRDN_RE    <= '1';
      W_DCDN         <= '0';
      W_CTSN         <= '0';
      W_DSRN         <= '0';
      W_RIN          <= '0';

Wait for PERIOD;

      W_RESET        <= '0';
   -- W_CLK16X       <= '1';
      W_MCR          <= "01"; --(others => '0');
      W_MSRRDN_RE    <= '0';
      W_DCDN         <= '1';
      W_CTSN         <= '1';
      W_DSRN         <= '1';
      W_RIN          <= '1';

 Wait for PERIOD;
      W_RESET        <= '0';
   -- W_CLK16X       <= '1';
      W_MCR          <= "11"; --(others => '0');
      W_MSRRDN_RE    <= '0';
      W_DCDN         <= '0';
      W_CTSN         <= '0';
      W_DSRN         <= '0';
      W_RIN          <= '0';

 Wait for PERIOD;
      W_RESET        <= '0';
   -- W_CLK16X       <= '1';
      W_MCR          <= "11"; --(others => '0');
      W_MSRRDN_RE    <= '0';
      W_DCDN         <= '1';
      W_CTSN         <= '1';
      W_DSRN         <= '0';
      W_RIN          <= '0';


 Wait for PERIOD;

      W_RESET        <= '0';
   -- W_CLK16X       <= '1';
      W_MCR          <= "11"; --(others => '0');
      W_MSRRDN_RE    <= '0';
      W_DCDN         <= '1';
```

```
    W_CTSN          <= '1';
    W_DSRN          <= '0';
    W_RIN           <= '1';

wait for PERIOD;


      wait;
  end process STIMULI;
end beh;
```