MULTIBAND LTE POWER AMPLIFIER FOR HANDSET APPLICATION

JAGADHESWARAN RAJENDRAN

THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENT FOR THE DEGREE OF DOCTOR OF PHILOSOPHY IN ENGINEERING

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2015

ABSTRACT

As wireless communication standard continues to evolve accommodating the demand of high data rate operation, the design of RF power amplifier (PA) becomes ever challenging. PAs are required to operate more efficiently while maintaining stringent linearity requirement. In this work, a new circuit to extend the linear operation bandwidth of a LTE (Long Term Evolution) power amplifier, while delivering a high efficiency is presented. The 950µm x 900µm monolithic microwave integrated circuit (MMIC) power amplifier (PA) is fabricated in a 2µm InGaP/GaAs process. The PA consists of three stages, which is the pre-driver, driver and main stages. The main stage is designed in class-J configuration in order to improve the efficiency of the PA. The optimum conduction angle method is employed to enable the PA to operate in bias condition which has the optimum operation for linearity and efficiency. A novel on-chip analog pre-distorter (APD) is designed and integrated into the driver stage to improve the linearity of the highly efficient PA further to meet the adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) specifications for LTE signal profile with 20MHz channel bandwidth. Experimental result verifies that the designed PA is capable to meet the ACLR specifications of -30dBc from 1.7GHz to 2.05GHz which encapsulates LTE Band 1,2,3,4,9,10,33,34,35,36,37 and 39 at maximum linear output power of 28dBm. The maximum EVM at 28dBm for 16-QAM scheme is 3.38% at 2050MHz.The corresponding power added efficiency (PAE) varies from 40.5% to 55.8% across band. With a respective input return loss of less than -15dB, the PA's maximum power gain is measured to be 35.8dB while exhibiting an unconditional stability characteristic from DC up to 5GHz. The proposed architecture serves to be a good solution to improve the linearity and efficiency of a PA for wideband LTE operation

without sacrificing other critical performance metrics. This will ultimately reach the goal to have single chip solution for handset LTE PA.

ABSTRAK

Sebagai wayarles komunikasi standard terus berkembang menampung permintaan operasi kadar data yang tinggi , reka bentuk RF penguat kuasa (PA) menjadi semakin mencabar. PA diperlukan untuk beroperasi dengan lebih cekap di samping mengekalkan keperluan kelinearan ketat. Dalam karya ini , litar baru untuk melanjutkan jalur lebar operasi linear daripada LTE (Long Term Evolution) penguat kuasa, manakala menyampaikan kecekapan yang tinggi dibentangkan. X 900μm mikro litar bersepadu monolitik 950μm (MMIC) amplifier kuasa (PA) adalah rekaan dalam 2μm InGaP / GaAs proses. PA ini terdiri daripada tiga peringkat , yang merupakan pra- pemandu, pemandu dan peringkat utama. Pentas utama direka dalam konfigurasi kelas -J untuk meningkatkan kecekapan PA tanpa perdagangan teruk off dalam keupayaan penghantaran linear . Novel A atas cip analog pra-distorter (APD) direka dan bersepadu ke peringkat pemandu untuk meningkatkan kelinearan PA yang sangat berkesan untuk memenuhi nisbah bersebelahan saluran kebocoran (PPHT) dan vektor magnitud ralat (EVM) spesifikasi untuk isyarat LTE profil dengan saluran jalur lebar 20MHz . Hasil eksperimen mengesahkan bahawa PA yang direka mampu untuk memenuhi spesifikasi PPHT of- 30dBc dari 1.7GHz untuk 2.05GHz yang merangkumi LTE Band 1,2,3,4,9,10,33,34,35,36,37 dan 39 pada kuasa output linear maksimum 28dBm . The EVM maksimum pada 28dBm untuk skim 16- QAM adalah 3.38 % pada 2050MHz.The kuasa sama menambah kecekapan (PAE) berbeza daripada 40.5% kepada 55.8 % di seluruh band. Dengan input kerugian pulangan masing-masing kurang daripada- 15dB , keuntungan kuasa maksimum PA adalah diukur untuk menjadi 35.8dB manakala mempamerkan satu ciri kestabilan tanpa syarat dari DC sehingga 5GHz . Seni bina yang dicadangkan bertujuan untuk menjadi satu penyelesaian yang baik untuk

meningkatkan kelinearan dan kecekapan PA untuk operasi LTE Wideband tanpa mengorbankan lain metrik prestasi kritikal. Ini akhirnya akan mencapai matlamat untuk mempunyai penyelesaian cip tunggal untuk telefon bimbit LTE PA.

ACKNOWLEDGEMENTS

I first would like to express my deepest gratitude to my supervisor, Dr Harikrishnan Ramiah for his dedicated supervision and invaluable guidance on my research project. His enthusiasm and motivation drove me throughout this project. His vision and strong technical knowledge is a major contributor to the successful completion of this project. Thank you very much Dr Hari.

I also would like to thank the Higher Education Ministry of Malaysia for providing me the financial support through the MyPhD Scholarship. This work would not have been possible without this support.

Finally, I would like to express my deepest gratitude to my wife Mrs Kavitha Jagadheswaran for her endless love and support throughout this project. I am also grateful to my parents Mr Rajendran Uthirajoo and Mrs Suppamah Govindasamy for their continuous encouragement during the tough times. Last but not least, I would like to thank my lovely daughter, Tharini Jagadheswaran for her smiles and laughter which encourages me to always stay positive and cheerful.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

ACLR	Adjacent Channel Leakage Ratio
APD	Analog Pre-Distorter
EVM	Error Vector Magnitude
IMD3	Third Order Intermodulation Product
LTE	Long Term Evolution
OFDMA	Orthogonal Frequency Division Multiple Access
PA	Power Amplifier
PAPR	Peak to Average Power Ratio
QAM	Quadrature Amplitude Modulation
SC-FDMA	Single Carrier Frequency Division Multiple Access

LIST OF APPENDICES

CHAPTER 1. INTRODUCTION

1.1 Overview of LTE System

Long Term Evolution (LTE) evolves from the Universal Mobile Telephone System (UMTS) which was initiated by the Third Generation Partnership Project (3GPP) to address the continuous demand for high data rates. Among the key specifications of LTE are (Rumney, LTE Introduction, 2009):

a) Increased downlink and uplink peak data rates.

b) Scalable channel bandwidths of 1.4MHz, 3.0MHz, 5MHz, 10MHz, 15MHz and 20MHz in both uplink and downlink.

c) Spectral efficiency improvements over Release 6 HSPA of 3 to 4 times in the downlink and 2 to 3 times in the uplink.

d) Sub- 5ms latency for small Internet Protocol (IP) packets.

e) Performance optimized for low mobile speeds from 0 to 15km/h supported with high performance from 15 to 120km/h; functional support from 120 to 350km/h.

f) Co-existence with legacy standards while evolving toward an all-IP network.

The LTE frequency bands as defined by the European Telecommunications Standards Institute (ETSI) and 3GPP are shown in Table 1.1 (3GPP TS 36.101 version 9.4.0 Release 9, 2010).

Table 1.1: LTE Frequency Bands

Band Number	Uplink		Downlink		Duplex Mode
	Low (MHz)	High (MHz)	Low (MHz)	High (MHz)	
1	1920	1980	2110	2170	FDD
2	1850	1910	1930	1990	FDD
3	1710	1785	1805	1880	FDD
4	1710	1755	2110	2155	FDD
5	824	849	869	894	FDD
6	830	840	875	885	FDD
7	2500	2570	2620	2690	FDD
8	880	915	925	960	FDD
9	1749.9	1784.9	1844.9	1879.9	FDD
10	1710	1770	2110	2170	FDD
11	1427.9	1447.9	1475.9	1495.9	FDD
12	698	716	728	746	FDD
13	777	787	746	756	FDD
14	788	798	758	768	FDD
15	Reserved		Reserved		FDD
16	Reserved		Reserved		FDD
17	704	716	734	746	FDD
18	815	830	860	875	FDD
19	830	845	875	890	FDD
20	832	862	791	821	FDD
21	1447.9	1462.9	1495.9	1510.9	FDD
……					
33	1900	1920	1900	1920	TDD
34	2010	2025	2010	2025	TDD
35	1850	1910	1850	1910	TDD
36	1930	1990	1930	1990	TDD
37	1910	1930	1910	1930	TDD
38	2570	2620	2570	2620	TDD
39	1880	1920	1880	1920	TDD
40	2300	2400	2300	2400	TDD

Allocations of the tabled bands above around the globe is illustrated in Figure 1.1.

Figure 1.1: LTE Bands around the globe (Amon, 2011)

From Table 1.1, it can be observed that LTE exists in a combinations of FDD and TDD mode. Therefore, the RF transmission specifications are the same for both modes, in contrary to UMTS standard (Rumney, LTE Introduction, 2009).

LTE supports three modulation modes, which are Quadrature Phase Shift Keying (QPSK), 16-Quadrature Amplitude Modulation (16-QAM) and 64-QAM. For uplink applications, QPSK and QAM are preferred choice, whereas for downlink application, 64-QAM is preferred. The multicarrier modulation schemes used in LTE are Orthogonal Frequency Division Multiple Access (OFDMA) for down link and Single Carrier Frequency Division Multiple Access (SC-FDMA) for uplink. The difference between

OFDMA and SC-FDMA is explained with the aid of Figure 1.2 (Rumney, Air Interface Concepts, 2009).

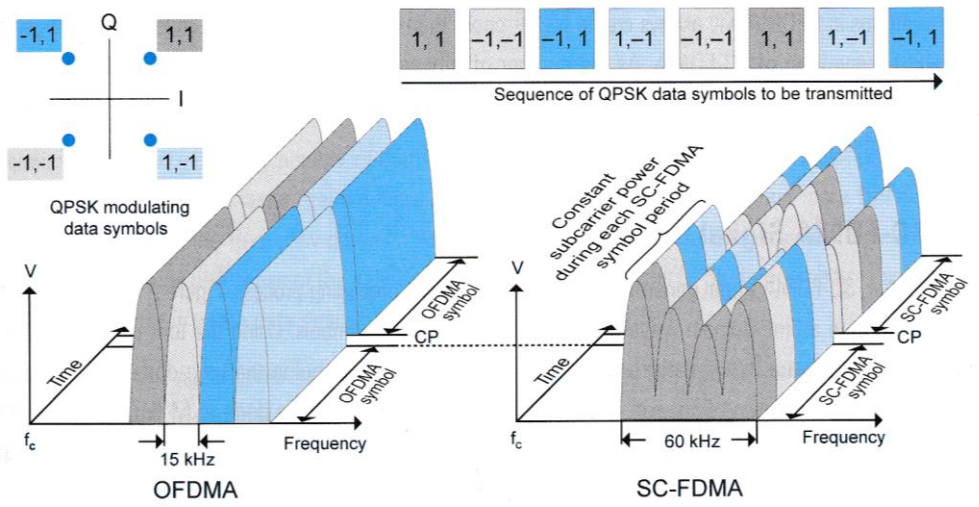


Figure 1.2: OFDMA and SC-FDMA comparison in transmitting QPSK symbols

In OFDMA transmission scheme, four subcarriers with 15kHz bandwidth each are modulated for the OFDMA symbol period of 66.7μs by one QPSK data symbol. For the four subcarriers, 4 symbols are taken in parallel. After one OFDMA symbol period has elapsed, the carrier prefix (CP) is inserted and the next four symbols are transmitted in parallel. To create the transmitted signal, an Inverse Fast Fourier Transform (IFFT) is performed on each subcarrier to produce M time-domain signals. These in turn are vector-summed to create the final time-domain waveform used for transmission.

In contrast to OFDMA, SC-FDMA signal generation begins with a special pre-coding process but then continues in a manner similar to OFDMA. The most obvious difference between the two schemes is that OFDMA transmits the four QPSK data symbols

in parallel, one per subcarrier, while SC-FDMA transmits the four QPSK data symbols in series at four times the rate, with each data symbol occupying a wider M x 15kHz bandwidth. This is well illustrated in Figure 1.2. The OFDMA signal clearly behaves as a multi-carrier with one data symbol per subcarrier, but the SC-FDMA signal appears to be more like a single-carrier with each data symbol being represented by one wide signal. It is the parallel transmission of multiple symbols that creates the undesirable high PAPR of OFDMA. By transmitting the M data symbols in series at M times the rate, the SC-FDMA occupied bandwidth is the same as multi-carrier OFDMA but, crucially, the PAPR is the same as that used for the original data symbols. In a nutshell, the PAPR of SC-FDMA is lower than OFDMA. For example, adding together many narrowband QPSK waveforms in OFDMA will always create higher peaks than would be seen in the wider bandwidth single carrier QPSK waveform of SC-FDMA. As the number of subcarriers increases, the PAPR of OFDMA with random modulating data approaches Gaussian noise statistics but, regardless the number of sub-carriers, the SC-FDMA PAPR remains the same as that used for the original data symbols.

1.2 Research Motivation

The setback of SC-FDMA carrier modulation scheme is the generation of non-constant amplitude signals. Therefore the transmitter circuits particularly power amplifier (PA) faces stiff challenge in meeting the linear transmission specifications, mainly the adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM). It's an uphill task to meet these specifications without trading off the PA's efficiency. This is because the PA needs to operate at certain back-off level from the 1dB compression point in order to transmit non-constant amplitude signals without clipping them (Raab, et al., 2002).

Efficiency is an important figure of merit to protect the battery life of the handset. ***The first motivation for this project is to reduce the tradeoff between linearity and efficiency of the PA so that it is suitable for handset application.***

Due to the trade-off between linearity and efficiency, a single band solution is often preferred. This is shown in Figure 1.3 which illustrates the tear down of a high end smart phone.

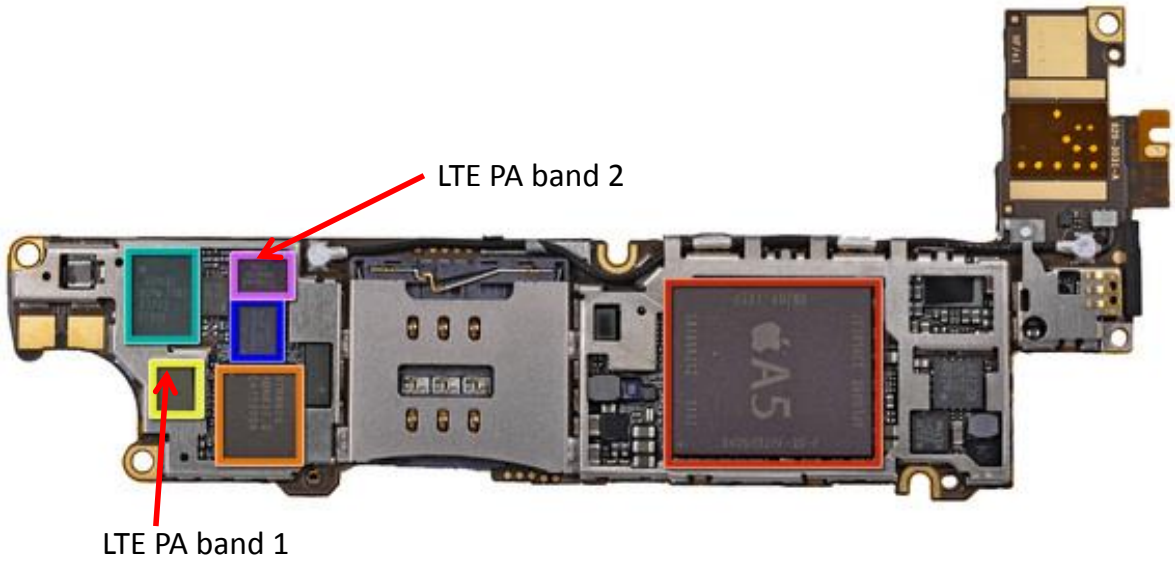


Figure 1.3: Tear down of a smart phone. The transmitter circuit contains two LTE power amplifiers to cover two different bands

This is due to the technique in existence till today in reducing the tradeoff prevails only for narrow bandwidth operation. The current available techniques have been discussed subsequently in Chapter 2. Therefore for global applications, more than one PA has to be integrated in the transmitter chain, which increases the cost and consumes larger board

space. ***Therefore, the second motivation is to design a multiband LTE PA, where several bands are integrated in single chip solution.***

The third research motivation is to design a high gain PA. This shall serve as an advantage to the baseband chip which is not designed to deliver high output power. A high gain PA also shall counter the antenna path loss on the phone board.

The fourth research motivation is to reduce the size of the active chip area of the PA, which helps in reducing the die manufacturing cost.

1.3 Research Objectives

In this project, the design of a monolithic microwave integrated circuit (MMIC) power amplifier (PA) for handset was intended. The first research objective was to reduce the trade-off between linearity and efficiency of the PA. In order to meet this requirement, the optimum conduction angle technique was used. A conduction angle which has the lowest third order inter-modulation product (IMD3) and optimum efficiency is chosen to bias the PA.

The second objective of this research is to improve the efficiency of the PA while meeting its linearity specifications. The class-J concept was explored to achieve this objective. The reactive harmonic termination concept is proposed to improve the efficiency of the PA instead of conventional practice of terminating the second harmonic.

The third objective of this research is to improve the linear operation bandwidth of the PA. A novel analog pre-distorter (APD) was integrated at the input of the main amplifier of the PA. The designed APD introduces IMD3 cancellation to improve the

adjacent channel leakage ratio (ACLR) which is crucial for linearity. The APD is integrated on the same chip as the PA.

The fourth objective is to increase the power gain of the PA. A pre-driver and driver amplifier is integrated in the chip to achieve this objective. This eliminates the need of external driver amplifier to counter the antenna path loss.

Finally, the fifth objective is to characterize the proposed topology with LTE signal. This test is essential to ensure PA meets the ACLR and Error Vector Magnitude (EVM) specifications, thus complying with the 3GPP specifications. Essential optimization was conducted to meet the stringent linearity requirement for several operating band to fulfill the multi-band operation objective.

1.4 Thesis Organization

The outline of this thesis is organized as follows. Chapter 2 summarizes the literature review on various published linearization and efficiency enhancement techniques. In Chapter 3, the design approach on the power cell, which is the main amplifier is described and analyzed. Mathematical analysis and lab experiments on choosing the optimum bias point for linearity and efficiency has also been presented. Chapter 4 presents the design methodology of the high efficiency wideband class-J PA. The design and implementation of the Analog Pre-distorter technique is described in Chapter 5. Subsequently, in Chapter 6 the mode of implementation and measurement results are presented. Finally, conclusion and suggestion for future works are given in Chapter 7.

CHAPTER 2. LITERATURE REVIEW OF POWER AMPLIFIER EFFICIENCY AND LINEARIZATION TECHNIQUES

2.1 Introduction

LTE employs single carrier frequency division multiple access (SC-FDMA) for uplink and orthogonal frequency division multiple access (OFDMA) for downlink, a multicarrier modulation scheme ensuring spectral efficiency (Rana, Islam, & Kouzani, 2010). This modulation scheme is subjected to high peak to average ratio (PAPR). SC-FDMA has a similar performance and complexity respective to OFDMA, in favor of lower PAPR (Akter, Islam, & Song, 2010). Typically, the PAPR of SC-FDMA signal is 7dB whereas OFDMA is 10dB, heavily depending on the modulation scheme adapted (QPSK, 16QAM or 64QAM) (Rumney, Air Interface Concepts, 2009). To amplify signals with high PAPR, the power amplifier (PA) needs to operate at a backed off output power satisfying the stringent linearity requirement, specified in terms of adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM). The drawback of this conventional technique is in the degradation in PA's power added efficiency (PAE). The relationship between backed off output power and efficiency for a multicarrier signal can be appreciated in the following equations (Cripps, Amplifier Classes, A to S, 2012):

$$\eta_{pbo-classA} = \frac{1}{2} \cdot \frac{P_{bo}}{P_{\max}} \tag{2.1}$$

$$\eta_{pbo-classB} = \frac{\pi}{4} \cdot \sqrt{\frac{P_{bo}}{P_{\max}}} \tag{2.2}$$

where P_{bo} and P_{max} represent backed off output power and maximum output power respectively. For example, if a PA which has P_{max} of 35dBm is transmitting LTE signal with PAPR of 7dB, the resultant efficiency at P_{bo} of 28dBm is only 9.9% and 30% in a respective operation of class A and class B mode.

The solution to improve the PAE of LTE PA lies in two techniques, which are the efficiency enhancement technique and linearization technique. The efficiency enhancement technique mandates in improving the efficiency of a linear PA, while linearization techniques improves the linearity of an efficient non-linear PA (Cripps, RF Power Amplifiers for Wireless Communications, 2006).

2.2 Efficiency Enhancement Techniques

2.2.1 Device Switching (DS)

Efficiency enhancement technique mandates in improving the efficiency of a linear PA, which is typically biased at class-AB mode of operation. The device switching approach is a simple methodology to improve the efficiency of WCDMA PA at P_{bo}. In this technique, the size of the power cells is varied respective to the output power. In other words, the power cells are smaller at P_{bo} as compared to P_{max}, resulting in a higher efficiency at backed off output power operation region. The switching of the power cells is executed at the base of the power cells (Deng, Gudem, Larson, Kimball, & Asbeck, A SiGe PA with Dual Dynamic Bias Control and Memoryless Digital Predistortion for WCDMA Handset Applications, 2006; Deng, Gudem, Larson, & Asbeck, A High Average Efficiency SiGe HBT Power Amplifier for WCDMA Handset Applications, 2005). A novel switching method is reported which utilizes the base-collector diode to improve the switching

efficiency (Han & Kim, 2008). Recent work also employs the switching technique integrating PHEMT process on a GaAs HBT power cell (Kim, Kwak, & Lee, 2011). Alternatively a dual output matching network is proposed instead of switching between two power cells. In this method, once the main amplifier is switched OFF, the secondary output matching network transforms the 50 ohm load to the driver's optimum output impedance to improve the P_{bo} transmission efficiency without degrading PA's overall linearity performance (Huang, Liao, & Chen, 2010). The conceptual operation principle of the switching PA is illustrated in Figure 2.1.

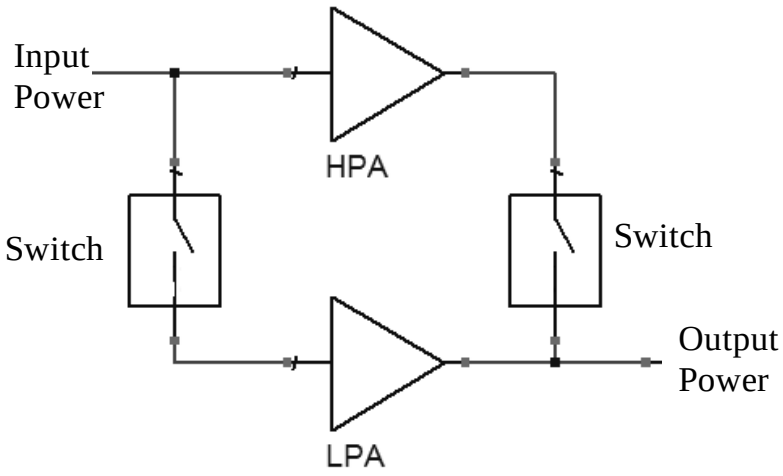


Figure 2.1: Switching PA topology

2.2.2 Doherty Power Amplifier (DPA)

Invented by W.H. Doherty in 1936 (Doherty, 1936), DPA consist of a carrier amplifier and a peaking amplifier where the combination of both delivers the total maximum output power of the PA. Below a certain input power level, the peaking amplifier is in off mode and the total output power of the PA is contributed by the carrier amplifier only. In this way, the efficiency at backed off output power can be improved. This is

usually achieved by varying the load impedance of the single carrier amplifier by applying another current source at its output terminal. In other words an active load pull is done at the output of the PA. This principle can be understood with the aid of Figure 2.2 and its following equations.

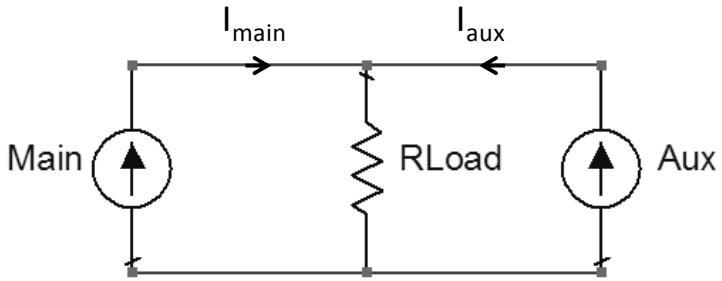


Figure 2.2: DPA concept

In Figure 2.2, *Aux* represents the peaking amplifier whereas *Main* represents the carrier amplifier. If *Aux* is inactive, *Main* will observe a load resistance of R_{Load}. Instead if *Aux* is active and supplies current I_{aux}, then the load impedance observed by *Main* is given by:

$$Z_{main} = R_{Load}\left(1+\frac{I_{aux}}{I_{main}}\right) \tag{2.3}$$

It can be observed from equation (2.3) that the source current from the *Aux* amplifier (I_{aux}) can be manipulated to change the load impedance of the *Main* amplifier to improve the efficiency at backed off output power. The practical implementation of DPA is shown in Figure 2.3.

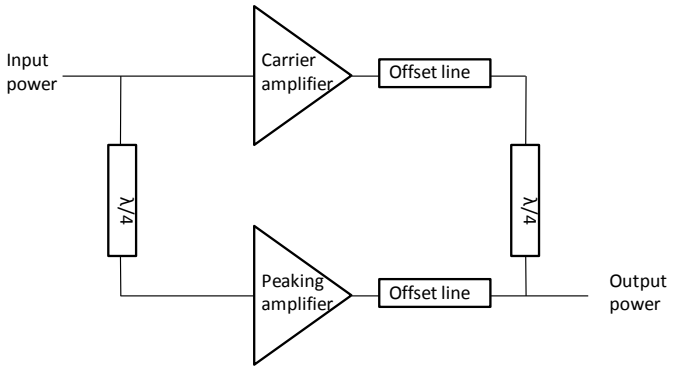


Figure 2.3: DPA topology

The output of the carrier amplifier is connected to the output of the peaking amplifier through an impedance transformer (quarter wave transmission line) prior terminating to the load. At P_{bo}, when the peaking amplifier is OFF, the carrier amplifier tends to observe an output impedance of $2R_{Load}$. As a result to this the efficiency of the PA is relatively high at P_{bo}. As the input power increases, the peaking amplifier begins to turn ON and generates its output power as depicted in Figure 2.4.

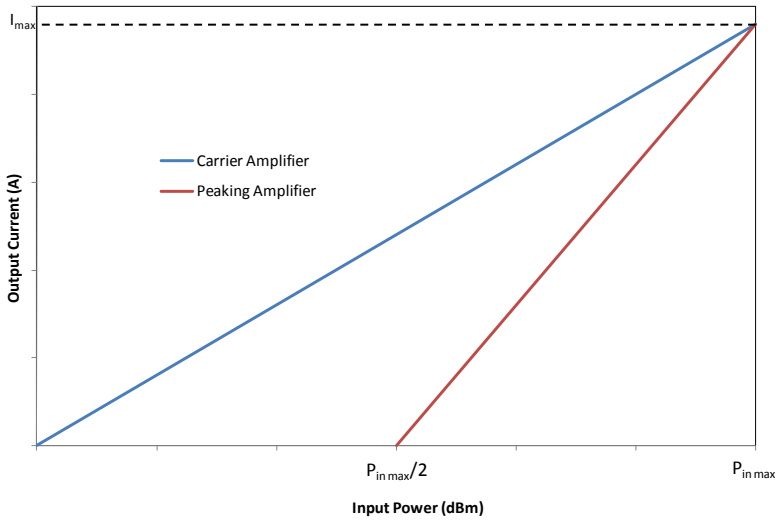


Figure 2.4: DPA profile

Accordingly, the load impedance of the carrier amplifier reduces. At P_{max}, the load impedance seen by both amplifiers is R_{Load}, which generates an equal output power of $P_{max}/2$ between the carrier and peaking amplifier.

Initial work on DPA in mobile wireless communications highlights a discrete solution, where the output network responsible for load modulation is integrated on printed circuit board (Iwamoto, et al., 2001), eventually evolving into a fully integrated approach (Kato, Yamaguchi, & Kuriyama, 2006). The concept of fully integrated chip using the HBT technology is extended up to 5 GHz operation (Yu, Kim, Han, Shin, & Kim, 2006).

An on-chip bias control circuit has also been introduced to reduce the tradeoff between linearity and efficiency at P_{bo} (Nam & Kim, 2007). Through the introduction of a third order harmonic control circuitry at the conventional DPA, further improvement in efficiency is achieved at P_{bo} (Kang, et al., 2008). Another proposed method is through optimizing the load modulation by designing an integrated optimum input power divider (Kang, et al., 2009). Recent work has also proposed wideband architecture for LTE application (Kang, et al., 2011), where the bandwidth is achieved through the aid of a phase compensation circuit, which ensures the load modulation is performed successfully across a wide range of frequency. In another work, switch load power mode technique has been designed to improve the DPA's backed off efficiency with the aid of an HEMT amplifier ((Cho, et al., 2014).

2.2.3 Average Bias Tracking (ABT)

The average bias tracking is another popular technique to improve the efficiency of the PA at P_{bo}. In this method, the biasing of the PA is adjusted respective to the output

power level. Instead of switching between two power devices, both supply voltage and bias current are dynamically adjusted for a single power cell. At P_{bo}, the supply voltage and bias current is low, thus improving the efficiency in this region of operation. The bias controller circuit is usually implemented on a CMOS platform. The penalty paid is in the inherit complexity as dual process is needed for the PA realization (Sahu & Rincon-Mora, 2007; Tombak, Baeten, Jorgenson, & Dening, 2006). There has been a continuous attempt to use an all CMOS process to reduce the design cost (Shameli, Safarian, Rofougaran, Rofougaran, & DeFlaviis, 2008). However the PAE and output power is still low as compared to GaAs based PAs.

2.2.4 Envelope Tracking (ET)

The envelope tracking method was given an immediate attention in the quest to design an efficient LTE PA. The construction is an evolution from the envelope elimination and restoration (EER) technique proposed by Kahn (Kahn, 1952). In EER, the phase modulation of the input signal is preserved, thus eliminating AM-PM distortion. Instead, the amplitude modulation of the input signal is used to modulate the supply voltage of the PA to improve the efficiency at P_{bo}. The improvement is obtained due to the reduction of the supply voltage in the PA accordingly. For EDGE application, this method is used to improve the power efficiency of a class-E PA at P_{bo} (Reynaert & Steyaert, 2005). On the other hand, the improvement in the bandwidth of the modulator without significantly degrading its efficiency is also proposed (Chu, Bakkaloglu, & Kiaei, 2008). In EER, the detection of the amplitude modulated supply voltage at the output of the PA needs to be accurate to ensure the linearity of the PA (in term of AM-PM distortion) is not jeopardized. This issue can be resolved by replacing the non-linear PA (class-E, Class-D) with an

equivalent linear PA (Class-AB). This method is known as the Envelope tracking (ET) which is illustrated in Figure 2.5.

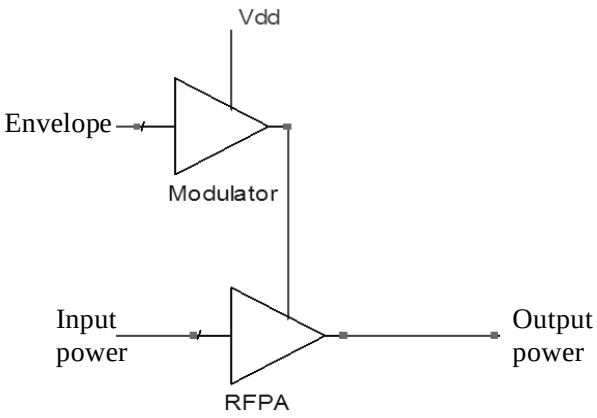


Figure 2.5: ET topology

At the initial stage of ET, the load resistance of the PA is matched to deliver a maximum linear output power. Then, as the output power is reduced, the supply voltage is decreased proportionally respective to the decreasing drive voltage. Hence, the efficiency at P_{bo} improves significantly. The reduction in supply voltage will not affect the linearity performance of the PA due to full rail to rail voltage swing contributed by the output matching network. The supply voltage is varied with the aid of a supply modulator. In WCDMA handset application, the supply modulator consist of a class-D switching amplifier, developed on a CMOS platform to improve the efficiency of a linear class-AB PA (Takahashi, Yamanouchi, Hirayama, & Kunihiro, 2008), where the Class AB PA is realized utilizing GaAs HFET process. Other reported work utilizes GaAs HBT process to develop the PA and CMOS process to realize the supply modulator (Choi, Kim, Kang, & Kim, 2009; Kang, et al., 2010). This dual chip integration is proven to work efficiently and linearly for high PAPR signals such as for the application of LTE, covering wideband

operation (Moon, Son, Lee, & Kim, 2011; Hassan, Larson, Leung, Kimball, & Asbeck, 2012). In the continuous effort to reduce the complexity and cost, RFPA and supply modulator is integrated as a single chip solution. For high power application, LDMOS is used to deliver an efficiency of up to 60% at backed off output power of 31dBm (Pinon, Hasbani, Giry, Pache, & Garnier, 2008). SiGe BiCMOS process is also well explored in the PA implementation (Li, Lopez, Wu, Wu, & Lie, 2011; Wang, Kimball, Lie, & Asbeck, 2007). The advantage of low voltage headroom operation in this technology adapts well into handset transmitter integration frame. However, the GaAs HBT based PA out shines the SiGe BiCMOS based PA in the linear output power performance. On the other hand, in the effort to reduce the sensitivity of the supply modulator to battery headroom variation, new integrated power management architecture is proposed (Choi, Kim, Kang, & Kim, A New Power Management IC Architecture for Envelope Tracking Power Amplifier, 2011).

An alternative method, known as the interlock operation is also proposed to enhance the efficiency of the ET PA. Through this method the output current waveform and the RF input signal is optimized to increase the efficiency of the PA. Optimization of the RF input signal is executed by increasing the amplitude of the modulated signal at low output power prior injecting it into the input of the PA, resulting the PA to operate in its saturated region at low output power, which in turn improves its efficiency (Kim, Son, Jee, Kim, & Kim, 2013). Recent research work reports on the utilization of the switching technique to further boost the efficiency of ET PA at P_{bo}. As an alternative for conventional series switching techniques, which places series switch at the input and output of the main amplifier, in current approach a shunt switched capacitor is used to toggle between the low

power and high power mode. This technique does not limit the bandwidth of operation in the PA, thus enables the PA to operate for multiband operation (Cho, et al., 2013).

2.2.5 Class-S

The class-S amplifier is gaining its popularity as a complementing efficient enhancement technique. Originally meant for audio applications, an improved efficiency can be achieved for modern RF applications with the aid of GaN process, which promises high breakdown voltage and fast switching (Rui, Zhancang, Yang, & Lanfranco, 2012; Maier, et al., 2011; Heinrich, Wentzel, & Melaini, 2010; Wentzel, Meliani, & Heinrich, 2010). Therefore it is a suitable application for high voltage transmitter circuits at current use.

2.3 Linearization Techniques

2.3.1 Hybrid Class PA

In conventional practice the class-AB PA is the preferred choice in obtaining a good efficiency performance abstaining the tradeoff on linearity. However for signal with high PAPR, class-AB is not an optimal solution. Hence, the solution matures into a hybrid integration of class AB and class-F PA in single chip realization (Kang, et al., A Highly Efficient and Linear Class-AB/F Power Amplifier for Multimode Operation, 2008). This solution is achieved by ensuring the fundamental load of the amplifier is sandwiched in between class F and class-AB loads highlighting an optimum load resistance for linearity and efficiency. However, the optimum load resistance is obtained only for a narrowband operation.

2.3.2 Feedforward Linearization Technique (FFL)

FFL is one of the early linearization techniques implemented since the era of vacuum tube days to minimize the higher order unwanted non-linear energy spurs which creates severe distortion to the adjacent channel bands. The generation of these spurs is due to high power operation. Figure 2.6 depicts the typical FFL transmitter block diagram.

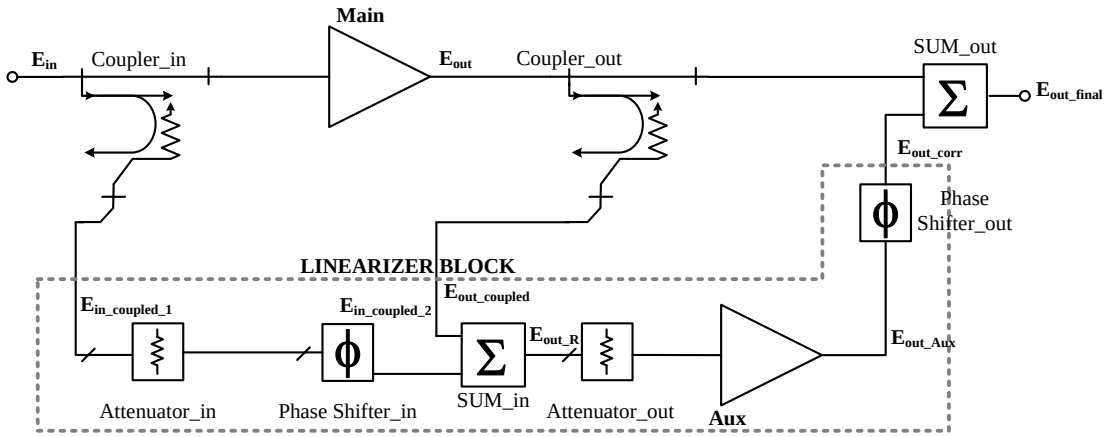


Figure 2.6: Feedforward transmitter block diagram

Basically, it consists of a main amplifier which transmits the RF energy and an auxiliary amplifier which is the part of the linearizer block. The linearizer block is responsible to eradicate the non-linear spurs. The output energy of the main amplifier is given by:

$$E_{out} = G_{main}E_{in} + G_{main}E_{HO} \tag{2.4}$$

$$E_{out\_coupled} = K_1\left(G_{main}E_{in} + G_{main}E_{HO}\right) \tag{2.5}$$

$$E_{in\_coupled\_1} = K_0E_{in} \tag{2.6}$$

where G_{main} is the gain of the main amplifier, E_{HO} is the higher order non-linear energy

spurs while K_0 and K_1 is the coupling coefficient of the input and output coupler, respectively. The amplitude and phase of the coupled undistorted input signal (no higher order energy) will be attenuated and reversed such that:

$$E_{in\_coupled\_2} = -E_{out\_coupled} = -A_{in}K_1E_{in} \tag{2.7}$$

where A_{in} is the input attenuation to cancel G_{main}.

Therefore, the resultant energy at the output of SUM_in is:

$$E_{out\_R} = E_{out\_coupled} - E_{in\_coupled\_2} = K_1G_{main}E_{HO} \tag{2.8}$$

The auxiliary amplifier will amplify E_{out_R} to generate E_{out_Aux}. With an aid of a phase shifter, the correction signal is produced, given as:

$$E_{out\_corr} = -G_{aux}K_1E_{HO} \tag{2.9}$$

where G_{aux} is the auxiliary amplifier's gain. With the aid of Attenuator_out and phase_shifter_out, the E_{out_corr} can be adjusted to generate an equal E_{HO} amplitude but with opposite phase response to achieve a perfect cancellation. Finally, the higher order energy free output signal is given as:

$$E_{out\_final} = E_{out} + E_{out\_corr} \tag{2.10}$$

The main design challenge in realizing FFL is the generation of the correction signal E_{out_corr}. In order to ensure perfect distortion cancellation, a good accuracy in coupling at the output of the PA and subsequently generate the correction signal is required in any transmission condition. A possible solution for the above mentioned constraint is to

use an adaptive control system to control the amplitude and phase response of the correction signal. This adaptive control system is realized with the aid of a digital controller (Suzuki, Ohkawara, & Narahashi, 2011; Legarda, et al., 2005; Kang, Park, Lee, & Hong, 2003). The controller is responsible to generate the amplitude and phase algorithm at various operating frequencies, to ensure broadband distortion cancellation is achieved.

The usage of coupler in this technique also causes some losses in the fundamental energy transmission. In order to minimize this losses, the feedforward technique is used as a pre-distorter where it is connected to the input of the main amplifier, rather than creating the conventional loop of operation (Kim, et al., 2006).

Due to the complexity of implementation and large board space consumption, the FFL approach is deemed more suitable for base station applications. Eventually, to improve on these drawbacks, pre-distortion technique is ventured upon.

2.3.3 Analog Pre-distortion Linearization (APD)

APD integration is the limelight of PA design due to its simplicity and capability to be integrated in single chip solution. The principle of operation in APD is through the generation of inverse phase and magnitude response of the third and fifth order nonlinearity respective to the corresponding output of the amplifier. In PA design, this reversal in phase and magnitude can be translated to its AM-AM and AM-PM characteristics as depicted in Figure 2.7. In other words, the coefficients of the generated non linearity from the APD cancel the intrinsic non linearity of the PA at the same order. Initial approach shows that a variable attenuator and phase shifter is used to manually compensate the IMD3 product generates by the non linear PA.

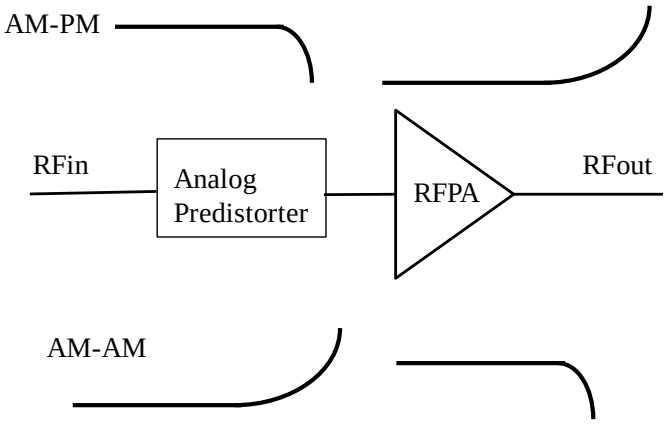


Figure 2.7: Analog Predistortion Technique

The variable attenuator generates an opposite AM-AM response whereas the phase shifter generates an opposite phase response (AM-PM) (Park, Baek, & Hong, 2000). Thereafter the APD is realized using the heterojunction FET (Hau, Nishimura, & Iwata, 2001). The opposite phase response is obtained by varying the biasing port of the FET. Other reported work outlays the usage of parallel Schottky diodes to generate IMD3 component to cancel out the IMD3 generated by a 4W PA for WCDMA base station application (Cha, Yi, Kim, & Kim, 2004). The generated IMD3 component is amplified through an amplifier prior being injected into the PA. The generated amplitude and phase response can be flexibly controlled using a vector modulator. A fully integrated APD implemented in GaAs HBT process is proposed to improve the adjacent channel leakage ratio (ACLR) confirming the WCDMA specifications. The APD consists of a single HBT transistor with an independent biasing circuit to generate an opposite third order response (Yamanouchi, et al., 2007).

2.3.4 Digital Pre-distortion Linearization (DPD)

The major disadvantage of APD techniques mentioned above is in its limited operation range in which the IMD3 and IMD5 cancellation is quite sensitive to the PA's output power and works only for narrow bandwidth. To improve on the bandwidth and to reduce the sensitivity, DPD is proposed. The DPD adaptation enables an accurate synthesis of the AM-AM and AM-PM coefficients to generate the 3^{rd} order, 5^{th} order and higher order cancellation. This improves the linearization dynamic range. Therefore, it can be used to linearize a highly non-linear PA such as the class-D (Landin, Fritzin, Moer, Isaksson, & Alvanpour, 2012) and Class-E configuration (Chen, Li, Horng, Jau, & Li, 2009). For extended application of wideband and high power, the DPD is also integrated together with envelope tracking technique (Jeong, et al., 2009). Another DPD method which uses the memory less predistorter techniques to reduce the sampling speed is proposed (Hammi, Kwan, Bensmida, & Morris, 2014). However, at this point of time the complexity of implementation and the consumption of larger board space serves are among the disadvantages DPD technique.

2.3.5 Other Linearization Techniques

As an alternative to the pre-distortion technique, other reported works also contributed in the effort to improve the linearity of the PA. As such is the bias linearizer circuit for WCDMA PA (Wen & Sun, 2006). The reverse biased diode maintains a constant base-emitter voltage (V_{be}) across input power, thus effectively improves the gain compression. The added advantage of this solution is in the reduced DC power consumption.

Another linearization method is the linear amplifications with nonlinear components (LINC). A novel technique is proposed to reduce the power dissipation at output combiner, which is achieved through a multi-level out-phasing transmitter scheme (Aref, Askar, Nafe, Tarar, & Negra, 2012).

The techniques mentioned in section 2.2 and 2.3 are compared in term of linear out power and corresponding efficiency in Table 2.1.

Table 2.1: Performance Comparison of Various Topologies

Ref	Concept	Process	Freq (GHz)	Linear Pout (dBm)	PAE (%)
(Huang, Liao, & Chen, 2010)	DS	GaAs HBT	1.95	28	34
(Kang, et al., 2011)	DPA	GaAs HBT	1.6-2.1	27.5	30
(Shameli, Safarian, Rofougaran, Rofougaran, & DeFlaviis, 2008)	ABT	0.18um CMOS	0.9	27.8	34
(Hassan, Larson, Leung, Kimball, & Asbeck, 2012)	ET	GaAs HBT + 0.15um CMOS	2.5	29	43
(Eswaran, Ramiah, Kanesan, & Reza, 2013)	APD	GaAs HBT	1.95	29	55
(Chen, Li, Horng, Jau, & Li, 2009)	DPD	GaAs PHEMT	1.95	22.7	48

2.4 Process Evolution in RFPA Design

An extensive amount of work has been published addressing PA design in CMOS process, leading to a positive transition from GaAs HBT to CMOS. The major mile stone is set upon when envelope tracking begins to gain its popularity. As highlighted, the current practice in ET realization is in the adaptation of dual process technology, CMOS and GaAs HBT platform, in constructing the PA encapsulating the RFPA and supply modulator. Favorably if the RFPA is realized in CMOS platform, a single chip solution is feasible resorting into a cost effective integration. The output power is improved through distributed active transformer in delivering an output power of more than 25dBm (Francois & Reyneart, 2012; Tuffery, et al., 2011). Alternately the output power could also be improved through the introduction of closed loop technique consisting of an amplitude and phase feedback (Kousai, Onikuza, Yamaguchi, Kuriyama, & Nagaoka, 2012), in which the operating bandwidth is also subjected to improve. On the other hand, a 90nm fully integrated CMOS power amplifier which improves the linear output power up to 27.3dBm is achieved through the couple L-Shape transformer design (Yang, Chen, & Chen, 2014).

Referring to the reviewed published works above, it can be concluded that the proposed solutions for LTE transmission are scattered around, in terms of linearization and efficiency improvements. Having said that, efforts on merging this two section as a single solutions has been lauded despite the higher cost, dual chip fabrications and board space consumption. Therefore, in this work a significant mileage has been taken to design a PA with both efficiency and linearization enhancement techniques integrated in one chip encapsulated to a single fabrication process.

CHAPTER 3. POWER CELL DESIGN

3.1 Introduction

In order to obtain the maximum output power for a particular device size, the optimum load line of the device plays an important role. The load-line determines the details of the transistor's collector matching network (Sweet, 1990). For LTE, the maximum linear output power allowed for reliable transmission by the transmitter system is 23dBm (3GPP TS 36.101 version 9.4.0 Release 9, 2010). Hence, the power amplifier (PA) needs to transmit at least 28dBm of linear output power to compensate the antenna path loss (Walsh & Johnson, 2009).

3.2 Power Cell Optimum Size

The optimum load resistance for a single HBT unit cell can be calculated with the following equation (Sweet, Designing Bipolar Transistor Radio Frequency Integrated Circuits, 2008):

$$R_{opt} = \frac{V_{cc} - V_k}{I_{\max}} \tag{3.1}$$

where V_{cc} is the desired operating voltage, V_k is the IV curve knee voltage and I_{max} is the maximum current obtained if the device is biased at class-A biasing point. The IV curve of a single HBT cell with an area of $80um^2$ is illustrated in Figure 3.1.

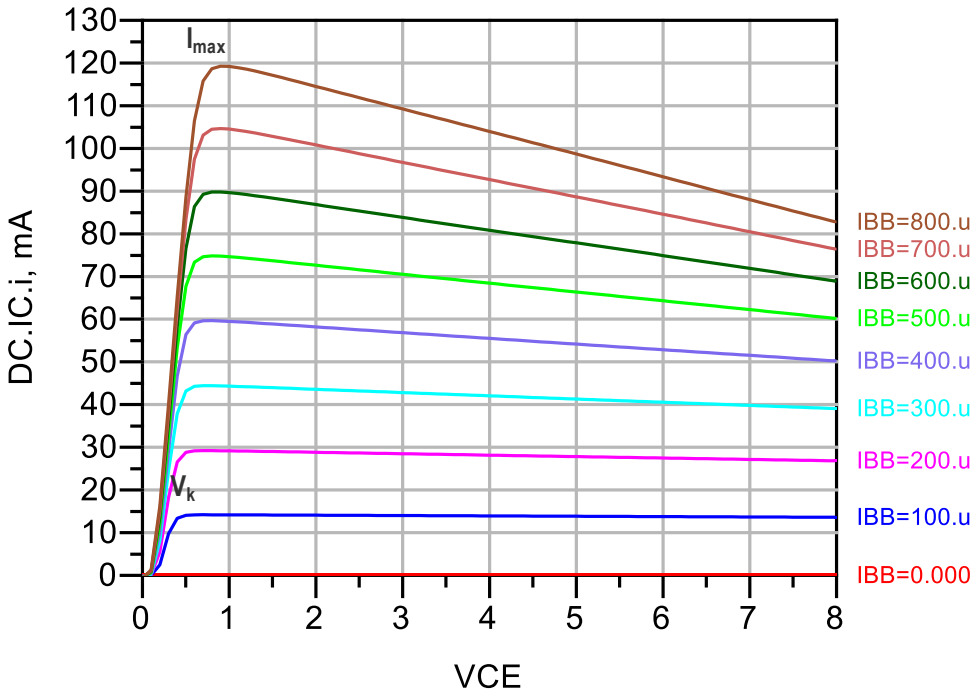


Figure 3.1: IV curves plot of a HBT with an area size of 80um^2

In Figure 3.1, it can be observed that the unit cell's DC IV curves show a negative slope due to its self-heating effect. Self-heating effect is caused by the increment of the bias point of a HBT unit cell in the saturation region (Ganesan, 1993). Therefore in order to protect the unit cell from this effect, in this work the power cells are designed in such a way that it comply the current density per unit HBT cell parameter. This is done by determining the unity gain frequency (f_T) of the device. Figure 3.2 illustrates the simulation setup to determine the unity gain frequency (f_T) across collector current for the 80um^2 unit cell. In this simulation, the collector current is increased gradually and the corresponding f_T of the device is determined. The resultant plot is depicted in Figure 3.3.

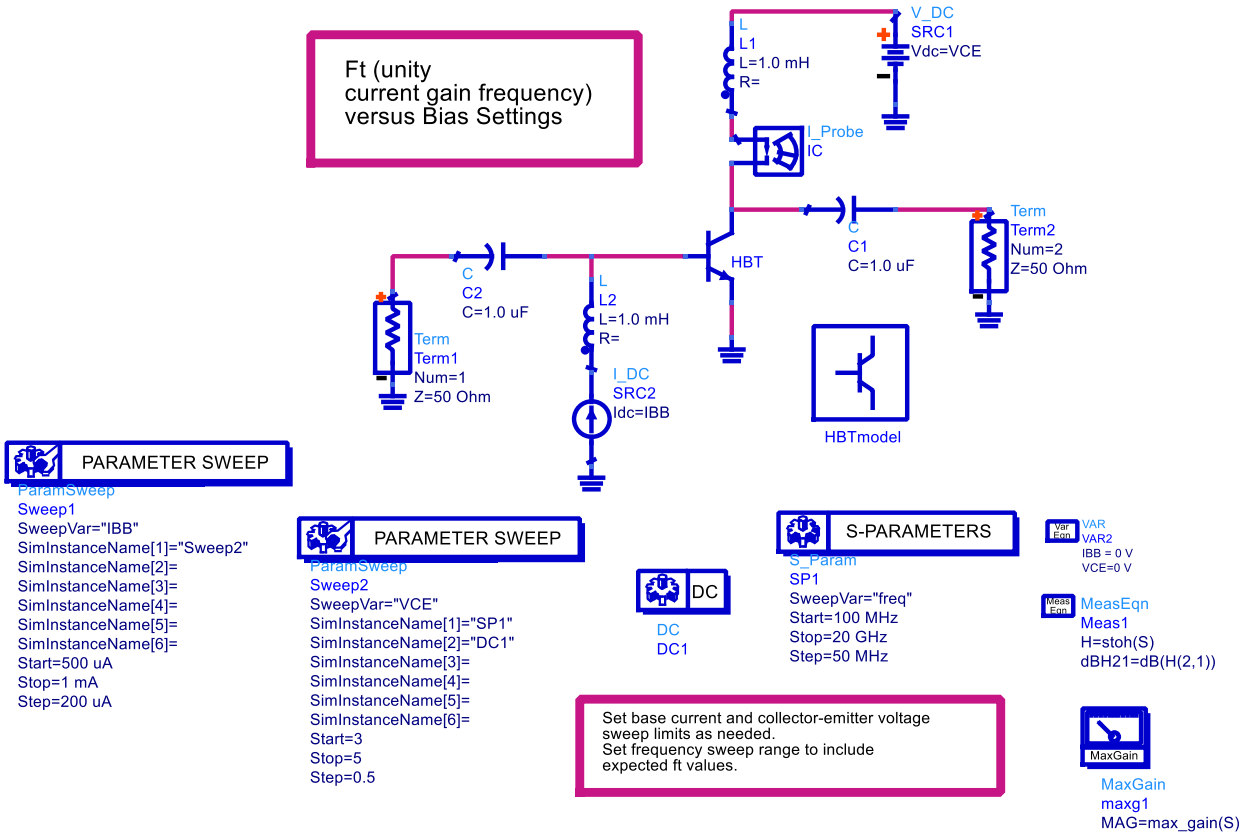


Figure 3.2: Simulation setup to determine the unity gain frequency, f_T

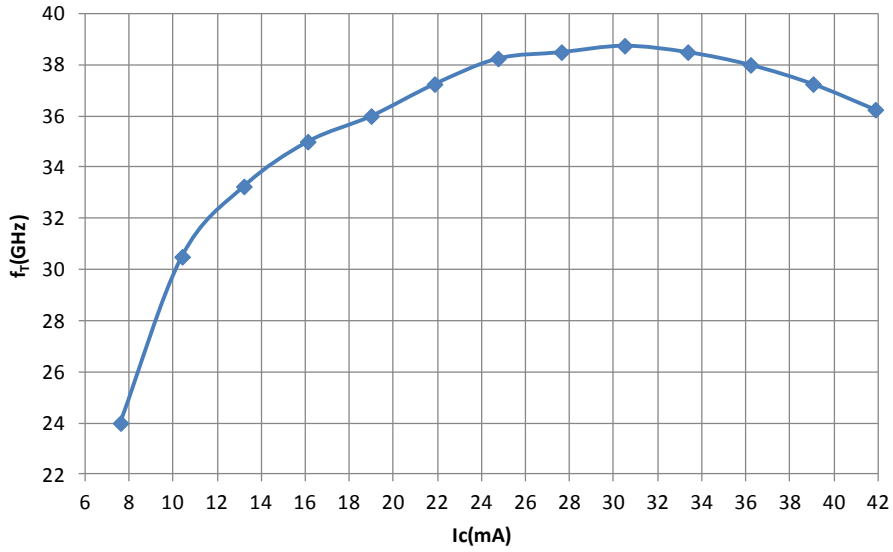


Figure 3.3: Unity gain frequency (f_T) across collector current I_c of a HBT with an area size of $80um^2$

It can be observed from Figure 3.3 that the f_T degrades when I_c is more than 30.5mA. With this the safe operating area (SOA) is defined as:

$$SOA = \frac{Max\, f_T\, I_c}{Area} \tag{3.2}$$

$$= \frac{30.5mA}{80um^2}$$

$$= 0.38\text{mA/um}^2$$

Therefore in this work the maximum current density per unit cell has been set to 0.38mA/um^2.

Since the targeted maximum linear output power is 28dBm, therefore the initial value for the maximum saturated output power of the amplifier is set to 32dBm. In other words, the back-off level is set to at least 4dB. This is an effort to optimize the efficiency of the PA with optimal device size. This can be viewed through equation (3.1) where smaller device will have larger R_{opt} and smaller I_{max} for the exact supply voltage headroom. The methodology to determine the power cell size is as follows:

1) Targeted maximum output power: 32dBm
2) Convert to Watt:

$$P_{out}(W) = \left(10^{\left(\frac{P_{out}(dBm)}{10} \right)} \right) \times 1mW \tag{3.3}$$

$$P_{out}(W) = \left(10^{\left(\frac{32}{10}\right)} \right) \times 1 \times 10^{-3}$$

$$= 1.58\text{W}$$

3) If the power cell is biased in class-A mode to obtain maximum output power where the efficiency, η is 50%, the DC supply power is then:

$$P_{DC} = \frac{100 \times P_{out}(W)}{\eta} \tag{3.4}$$

$$P_{DC} = \frac{100 \times 1.58}{50}$$

$$= 3.16\text{W}$$

4) For collector voltage V_{cc} of 3.5V, the maximum collector current, I_{ccmax} is:

$$I_{cc\max} = \frac{P_{DC}}{V_{cc}} \tag{3.5}$$

$$I_{cc\max} = \frac{3.16W}{3.5V}$$

$$= 900\text{mA}$$

5) Referring to Figure 3.1, I_{cc} of 15mA is selected as in this saturation region device is not severely affected by self-heating. Therefore the number of unit cells required:

$$N = \frac{I_{cc\max}}{I_{ccunitcell}} \tag{3.6}$$

$$N = \frac{900}{15}$$

$$N = 60$$

The number of unit cells required is 60.

6) The total device size is:

$$Total \text{ size (Q)} = N \times \text{ single unit size} \tag{3.7}$$

$$Q = 60 \times 80$$

$$= 4800um^2$$

Therefore the calculated power cell size is 4800um^2.

The load resistance of the power cell is calculated as following:

1) R_{load} of a single unit cell using equation (3.1):

$$R_{opt} = \frac{V_{cc} - V_k}{I_{\max}}$$

$$R_{opt} = \frac{3.5 - 0.5}{0.015}$$

$$= 200\Omega$$

2) The R_{load} of the power cell with size of 4800um^2 :

$$R_{load} = \frac{R_{opt}}{N} \tag{3.8}$$

$$R_{load} = \frac{200}{60}$$

$$= 3.33\Omega$$

The calculated load resistance of 3.33Ω delivers a maximum output power of 32dBm. The above calculated power cell size and its corresponding load resistance are verified in simulation. Figure 3.4 shows the schematic of the power cell.

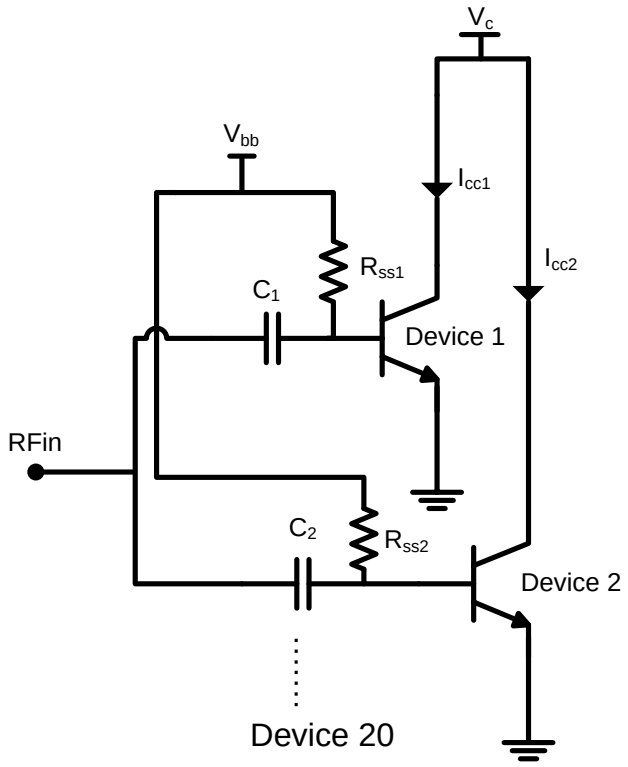


Figure 3.4: Power cell of the LTE PA. There are total 20 numbers of cells. R_{ss} is the ballasting resistor and C_1 and C_2 are the coupling capacitor

The size of each cell in Figure 3.4 is:

Cell size= Emitter width (µm) x Emitter Length (µm) x Number of emitter (3.9)

= 3 x 20 x 4

= 240um^2

The cells size is multiplied by 20 to achieve the overall size of 4800um^2. The simulation setup is illustrated in Figure 3.5.

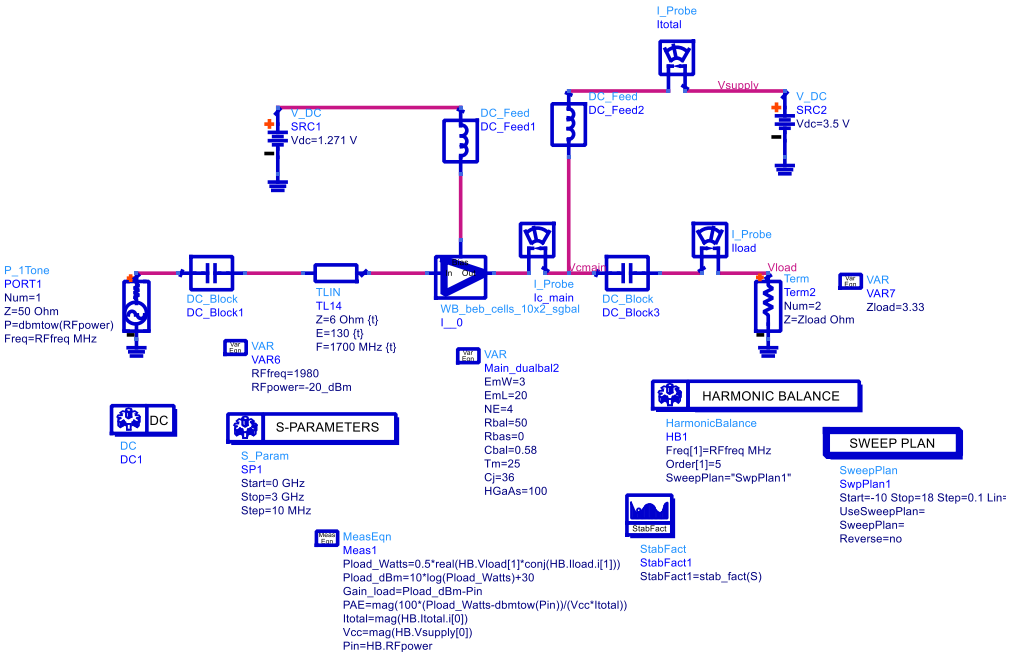


Figure 3.5: Simulation setup to verify the maximum output power and efficiency of the power cell

Based on the simulation setup in Figure 3.5, the maximum output power and its corresponding efficiency for load resistance of 3.33Ω are depicted in Figure 3.6. It can be seen that the maximum output power obtained is 33dBm with a power added efficiency (PAE) of 56.5%.

PAE is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{3.10}$$

where P_{out} is the output power, P_{in} represents the input power and P_{dc} is the DC power supplied to the PA.

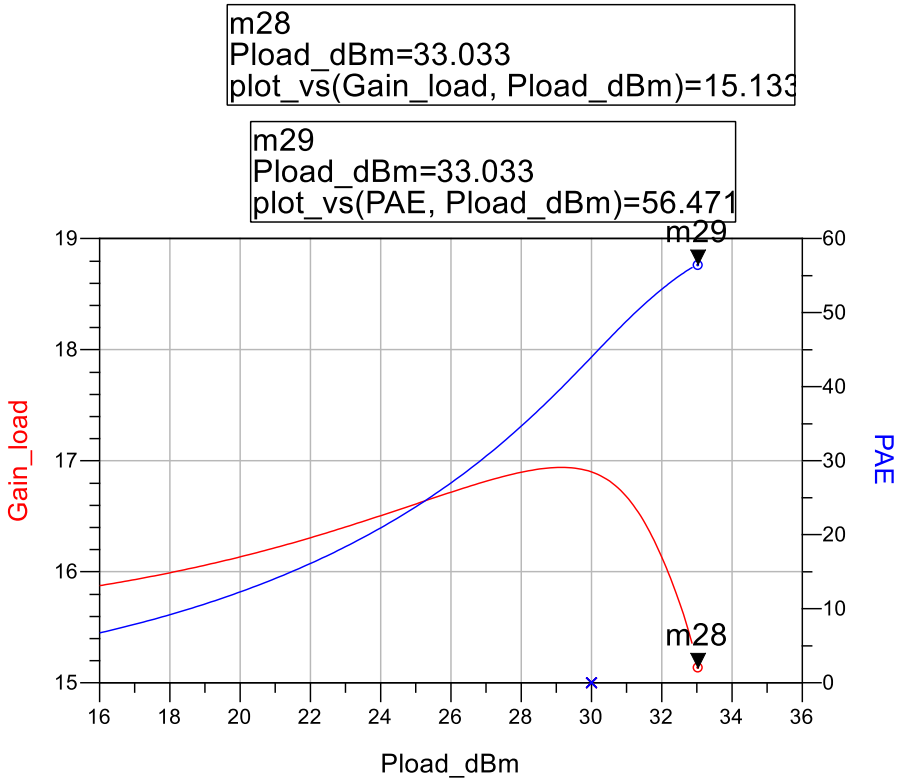


Figure 3.6: Simulation result for the 4800um^2 power cell with load resistance of 3.33Ω

In simulation, the maximum output power obtained is 33dBm, close to the calculated value. This shows a positive indication that the calculated power cell size is able to deliver the desired maximum output power when measured. Figure 3.7 depicts the load line swing of the power cell up to maximum output power.

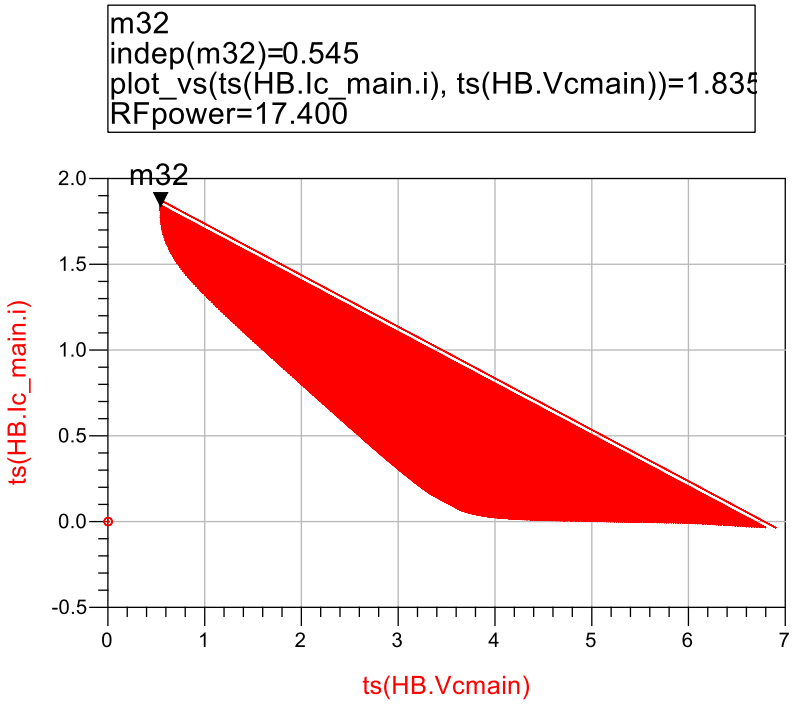


Figure 3.7: Load line swing across collector voltage of the power cell up to maximum output power of 33dBm

In Figure 3.7, the highest collector current simulated is 1.83A. Therefore the current density per area is 1.83A/4800um^2 which is **0.38mA/um^2**.

Since the simulated maximum output power delivered by the power cell is 33dBm with load resistance of 3.33Ω, a simple load pull is conducted then to observe the trade-off between the maximum output power and PAE when the load resistance is swept. This simulation is conducted with the PA being biased in class-AB mode. The result of the simulation is illustrated in Figure 3.8. With R_{load} of 5Ω, the maximum output power dropped to 32.5dBm with 1.6% improvement in maximum PAE. However, the PAE at backed off output power of 28dBm improves 8.6%. This result shows that if the power cell with the size of 4800um^2 is biased in class-AB mode only, R_{load} of 5Ω shall be able to

deliver PAE of 41% at backed off output power of 28dBm whereas R_{load} of 3Ω delivers a maximum output power of 34dBm. This shows there is enough room for maximum output power for the 4800um^2 device size, to be realized through fabrication.

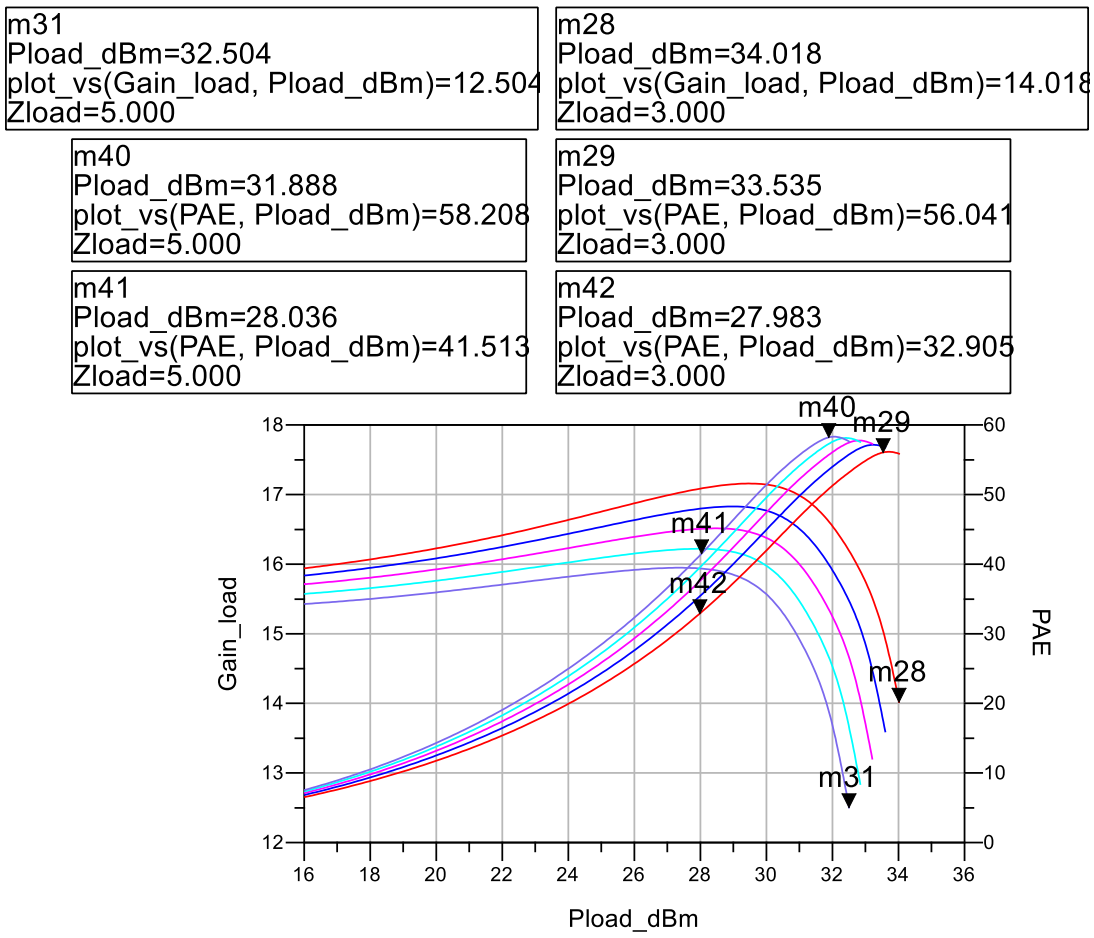


Figure 3.8: The load resistance R_{load} is swept from 3Ω to 5Ω, in 0.5Ω step

3.3 Thermal Runaway Phenomenon

3.3.1 Thermal runaway in HBT

The ability to deliver high output power at high frequency favors Hybrid Bipolar Transistor (HBT) technology as a solution for high frequency PA design (Sweet, Designing Bipolar Transistor Radio Frequency Integrated Circuits, 2008). However, due to its positive temperature coefficient characteristic, HBT is susceptible to an undesired phenomenon, known as thermal runaway. Liu et.al reported that, this is due to the collapse of current gain as the temperature of HBT increases (Liu, Nelson, Hill, & Khatibzadeh, 1993). An analytical model has been accordingly presented in predicting this phenomenon to certain accuracy (Liou, Liou, & Huang, 1994). The collapse of current gain is initiated, in the event the current of the parallel multiple HBT unit cells tumble. The parallel configuration is essential in delivering high transmission output power. Current collapse commences if any of the unit cell operates at higher temperature due to self-heating effect. The aftermath of this effect observes a higher collector current being injected by the designated unit cell. Higher collector current would eventually lead to a dependent chain of increase in the unit cell temperature. Subsequently the base-emitter voltage of the cell will drop due to the self-heating effect, resulting in the collector current hogs the remaining active unit cell. Current hogging increases the temperature and subsequently shuts down the remaining unit cells. Eventually, it leads to the collapse of the total collector current in the transistors. Figure 3.9 illustrates two unit cells which are connected in parallel. When Device 1 is operating at a higher temperature, a drop in the base-emitter voltage increases its collector current, I_{cc1} to compensate the drop. On the other hand, Device 2, which runs at a slightly cooler temperature, compensates to maintain the total collector current, I_{cc} by regulating its base-

emitter voltage resulting in a lower I_{cc2}. As I_{cc1} increases, I_{cc2} moves downhill, which eventually shuts down Device 2, as depicted in Figure 3.10.

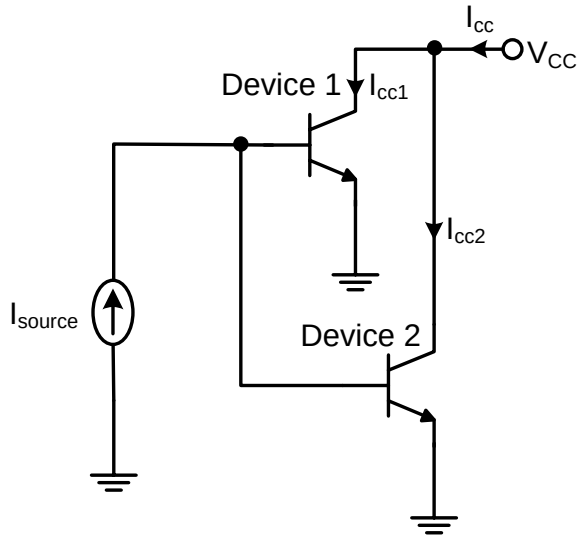


Figure 3.9: HBT unit cells in parallel

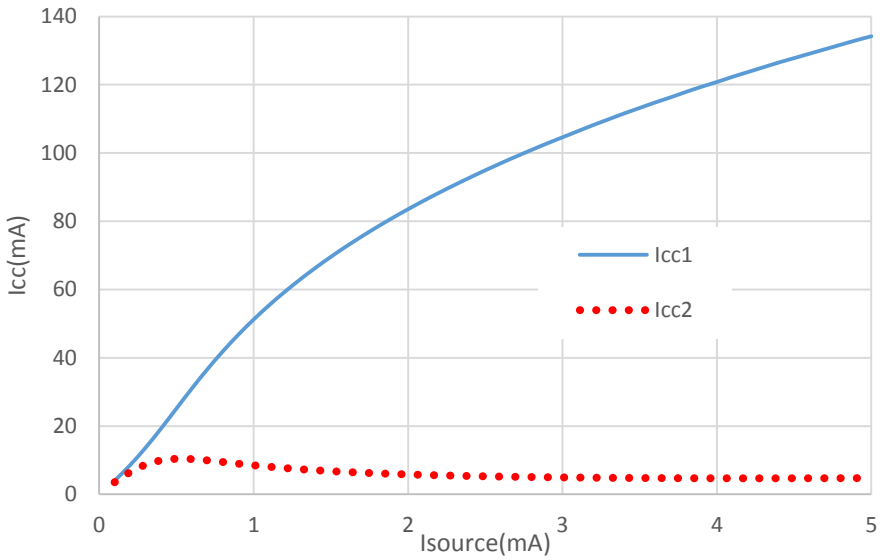


Figure 3.10: Current collapse phenomenon observed in Device 2, represented by I_{cc2}

Figure 3.11 illustrates the progressive decrease in the base-emitter voltage, V_{be} of Device 1 as the base current increases proportionally respective to the device operating temperature. Figure 3.10 and Figure 3.11 verify that the HBT unit cells are subjected to thermal runaway effect.

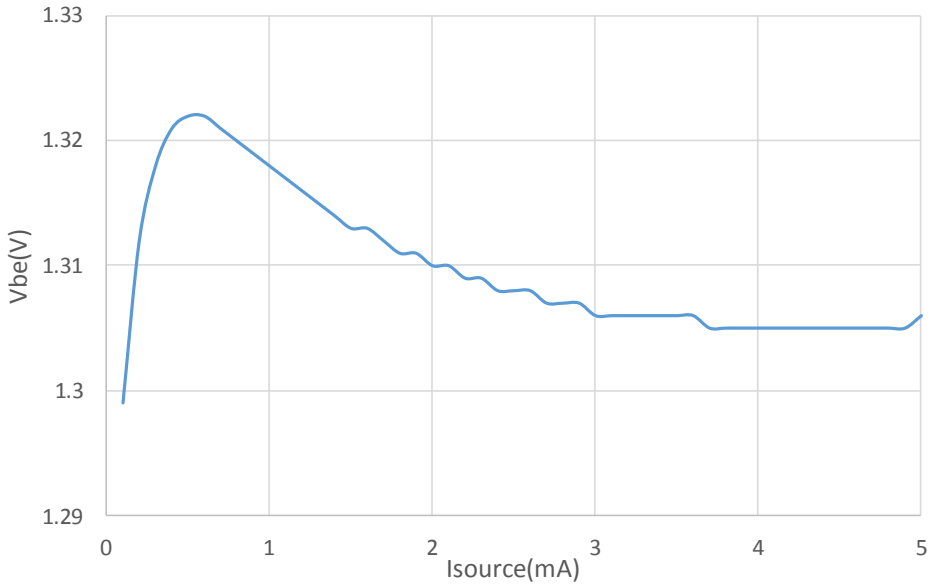


Figure 3.11: Device 1 is experiencing V_{be} degradation, which is indication of thermal runaway phenomenon

In designing a PA compatible to multi-carrier modulation scheme such as LTE and WCDMA, the HBT PA needs to be thermally efficient as the modulation scheme observe a high peak to average ratio, which encourages the increment in the junction temperature of the PA, leading towards non-linear operation (Thein, Law, & Fu, 2011). Liou et al reported on the advantages of emitter ballasting based on the junction temperature rise threshold (Liou, Jenkins, & Huang, 1996). On the other hand, Liu et al proposed base ballast integration as an appropriate solution respective to the emitter ballast for HBT due to its

decreasing current gain to temperature dependency (Liu, Khatibzadeh, Sweder, & Chau, 1996). However, base ballast tends to degrade the power gain of the PA and contributes to the degradation of linear output power (Maas, 2006). Jang et al alternatively integrated a depletion FET to the base of HBT to act as non-linear base ballast outlining thermal stability (Jang, Kan, Arnborg, Johansson, & Dutton, 1998), with a penalty paid in the complexity of the physical layout and fabrication cost. On the other hand, Jin-Dong et al proposed an optimized value of base ballast resistor based on thermal feedback network analysis to reduce the trade-off in power gain. Based on computer aided simulation result, HBT architecture conceptually requires a smaller base ballast resistor as compared to BJT (Dong, Zhang, Jun, Pan, & Ying, 2006). Bayraktaroglu et al alternatively proposed for a thermal isolation circuit to be integrated between the current source and the power stage as a substitute of the base ballasting concept (Bayraktaroglu & Salib, 1997).

3.3.2 Thermal Compensation Circuit

Figure 3.12 describes the circuit diagram of integrating the strap resistors, R_{ss1} and R_{ss2}. Expressing the temperature delta of both devices in Figure 3.12 as:

$$\Delta T = \theta_{jc} P_d \tag{3.11}$$

where θ_{jc} is the thermal resistance and P_d is the power dissipated, defined to be:

$$P_d = I_{cc} V_c \tag{3.12}$$

where $I_{cc} = I_{cc1} + I_{cc2}$.

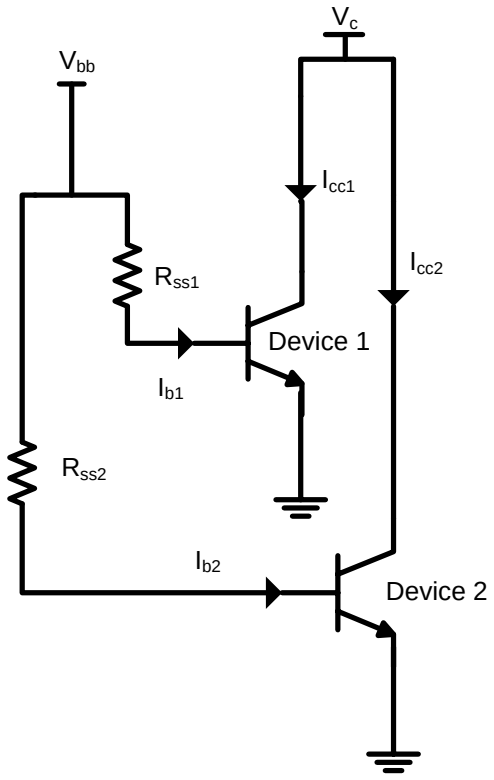


Figure 3.12: Strap resistor, R_{ss1} and R_{ss2} are implemented to mitigate thermal runaway phenomenon

Substituting P_d into (3.11):

$$\Delta T = \theta_{jc} I_{cc} V_c \tag{3.13}$$

Since Device 1 and Device 2 are equivalent in size, therefore

$$I_{cc1} = I_{cc2} \tag{3.14}$$

Consequently,

$$I_{cc1} = \beta I_{b1} \tag{3.15}$$

and

$$I_{cc2} = \beta I_{b2} \tag{3.16}$$

The relationship between the base currents and strap resistors is given as:

$$I_{b1} = \frac{V_{bb}}{R_{ss1}} \tag{3.17}$$

and

$$I_{b2} = \frac{V_{bb}}{R_{ss2}} \tag{3.18}$$

Substituting I_{b1} and I_{b2} in equation (3.15) and (3.16) respectively:

$$I_{cc1} = \beta \frac{V_{bb}}{R_{ss1}} \tag{3.19}$$

and

$$I_{cc2} = \beta \frac{V_{bb}}{R_{ss2}} \tag{3.20}$$

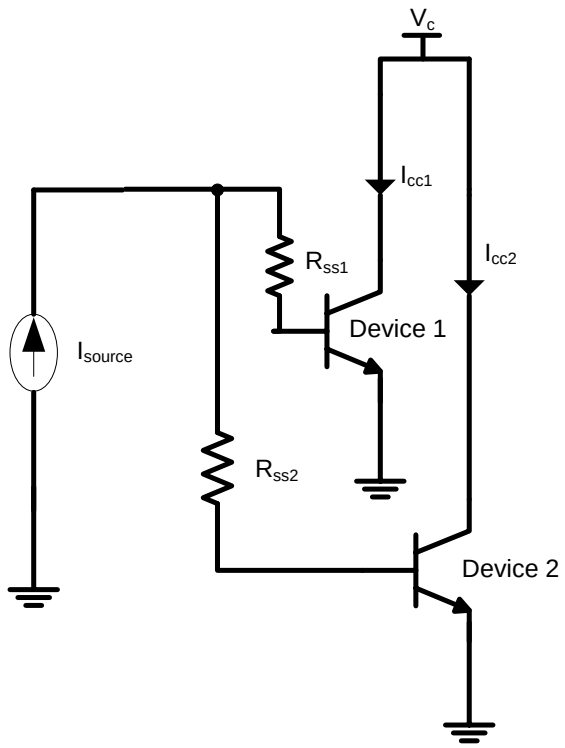
The total collector current I_{cc} can be equated as:

$$\begin{aligned} I_{cc} &= \beta V_{bb} \left[\frac{1}{R_{ss1}} + \frac{1}{R_{ss2}} \right] \\ &= \frac{\beta V_{bb}}{R_{ss1} \,||\, R_{ss2}} \end{aligned} \tag{3.21}$$

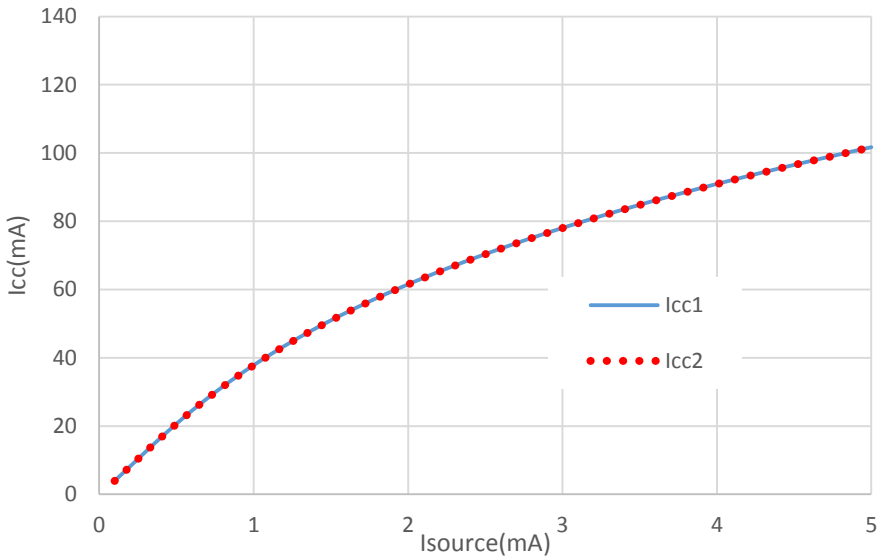
substituting (3.21) into (3.13):

$$\Delta T = \theta_{jc}\beta \frac{V_{bb}}{R_{ss1} \parallel R_{ss2}} V_c \tag{3.22}$$

Equation (3.22) concludes that an increase in the temperature delta relates to an inverse dependency to the total strap resistance, $R_{ss} = R_{ss1}||R_{ss2}$. Hence an equivalent temperature is preserved at the unit cells inheriting the highlighted relation in (3.22), which results in uniform current flow among the unit cells where $I_{cc1}=I_{cc2}$. This evidently illustrated as in Figure 3.13.



(a)



(b)

Figure 3.13: (a) The schematic in Figure 3.9 is redrawn with strap resistors integrated at the base of the transistors. (b) Collector current in Device 1, I_{cc1} and Device 2, I_{cc2} do not collapse after integration of strap resistors

As these strap resistors are not placed in series at the base of the HBT unit cell, the gain is not adversely affected.

3.3.3 Measurement Evaluation

Figure 3.14 illustrates the micrograph of the fabricated PA integrated with strap resistor and implemented in GaAs HBT technology. The corresponding schematic is depicted in Figure 3.15.

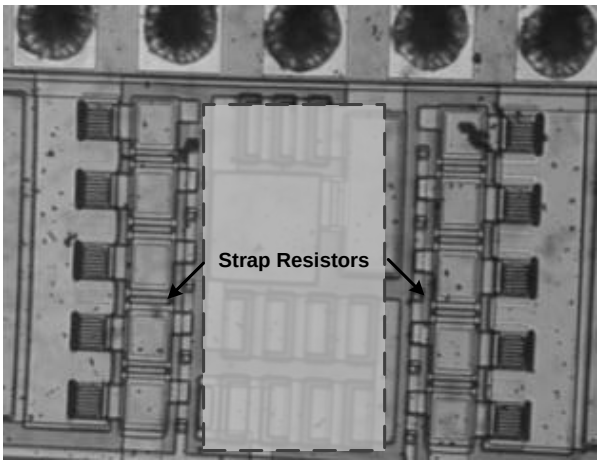


Figure 3.14: Micrograph of PA fabricated with strap resistors

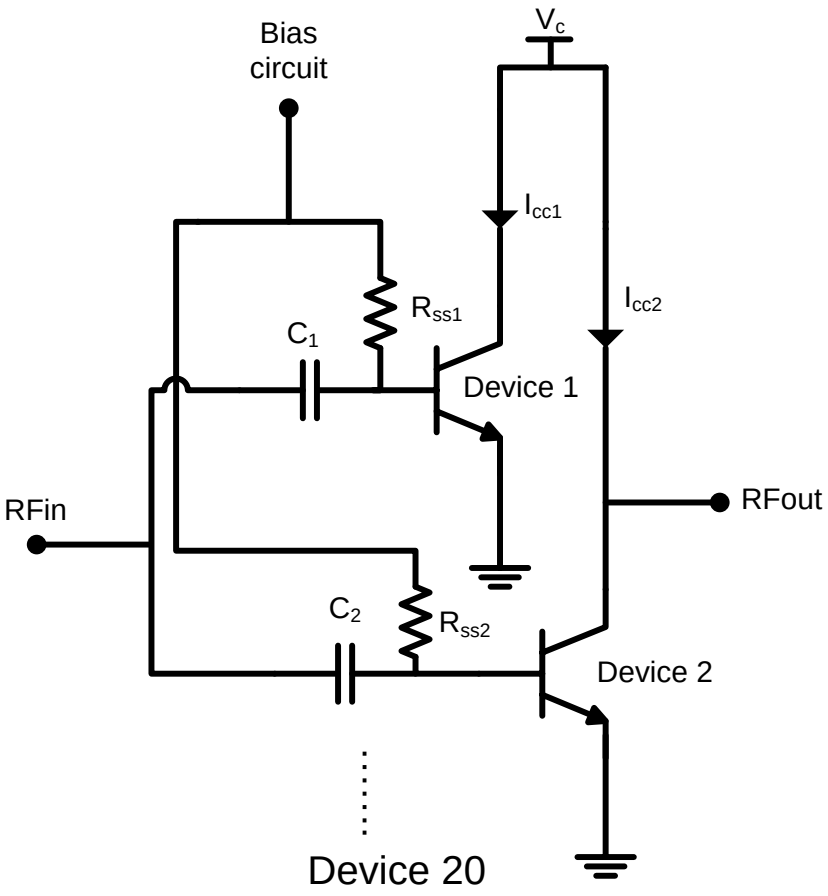


Figure 3.15: Schematic of the fabricated PA with strap resistors integration. For base ballast configuration, R_{ssn} is connected in series to C_n and $Device_n$

Figure 3.16 illustrates the AM-AM plot, which compares the implementation of base ballasting and strap resistor, achieving a maximum output power of 30dBm and 32.3dBm, respectively at supply voltage of 3.3V. The base ballasting approach observes a respective gain compression of 2.5dB. The void presence of gain expansion or compression in the strap resistor based integration evidently indicates a linear transmission.

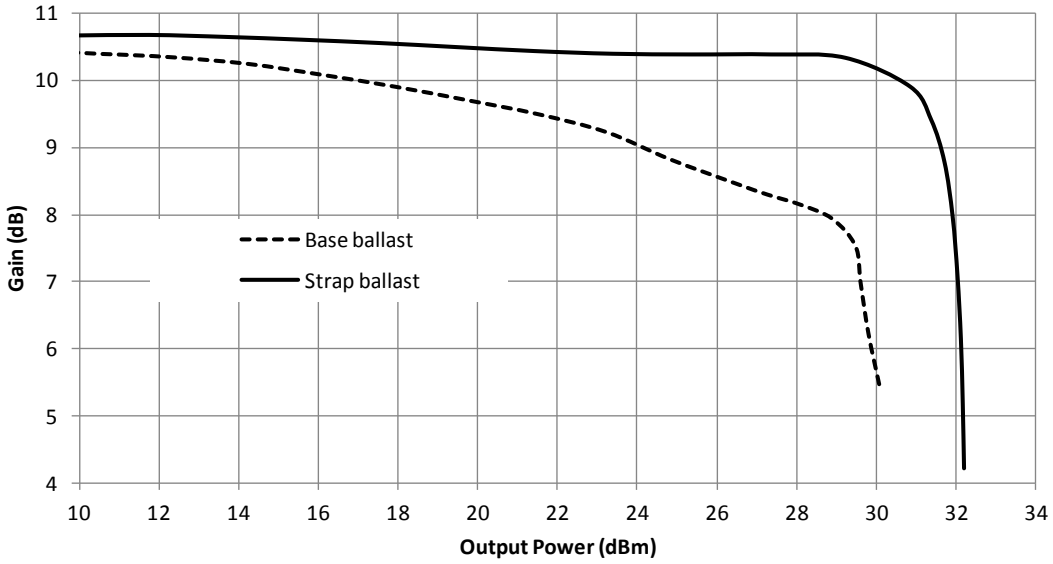


Figure 3.16: AM-AM comparison plot of the PA with base ballast and strap ballast for the same device size of 4800um^2

The improvement observed in the aforementioned maximum output power in Figure 3.16 is due to continuous increment in the collector current with the aid of strap ballast resistor, which is depicted in Figure 3.17. In the conventional practice of base ballast integration, the collector current became constant from output power of 28dBm to 29.5dBm and eventually collapses at an output power of 30dBm as shown in Figure 3.17. In a nutshell this shows base ballast limits the current swing at higher output power.

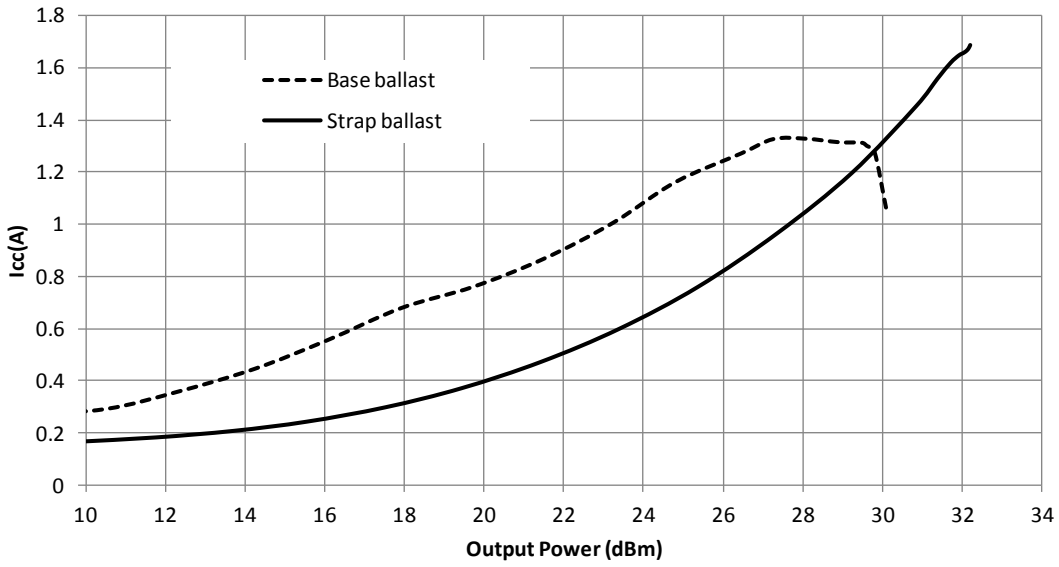


Figure 3.17: Collector current (I_{cc}) against output power comparison in base ballast and strap resistor integration

The definition of a highly linear power amplifier encapsulates thermally stable operation as much as in the implementation of linearization techniques. The conventional practice of integrating base ballasting for HBT transistors has an inherited penalty in the degradation of the linearity, power gain and efficiency. Figure 3.18 shows the ACLR plot portraying the advantage of the strap resistor ballasting as compared to base ballast, where in this measurement, a LTE input signal is adapted. In Figure 3.19, the benefit in obtaining a higher PAE is displayed by the strap resistor concept. Hence, it can be concluded that the proposed strap ballasting concept indeed suits well the PA for LTE operation.

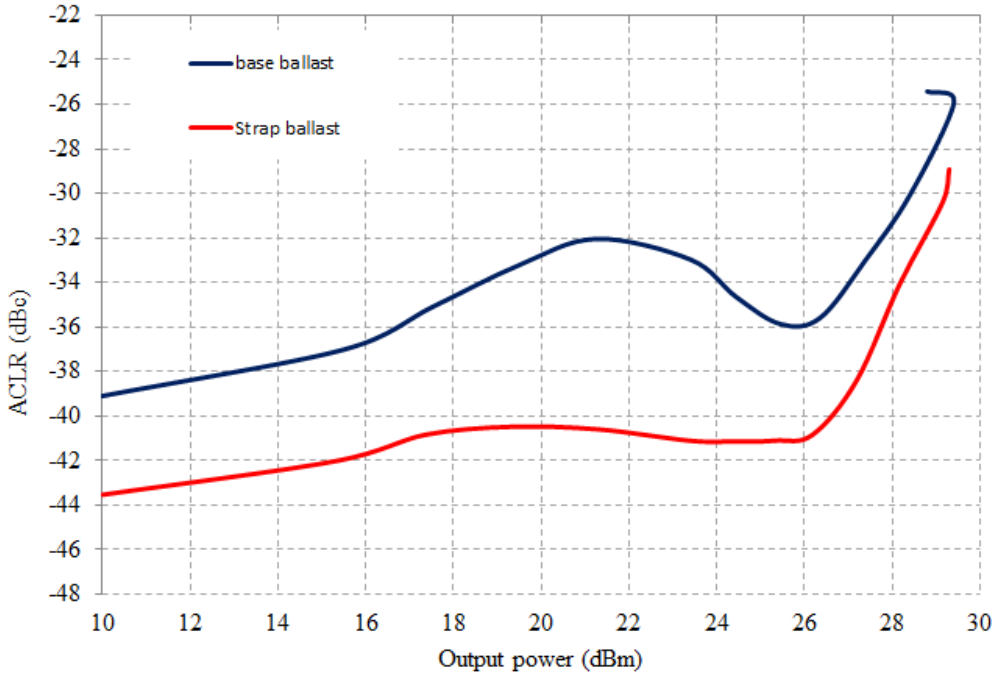


Figure 3.18: LTE ACLR plots comparing the two different combinations

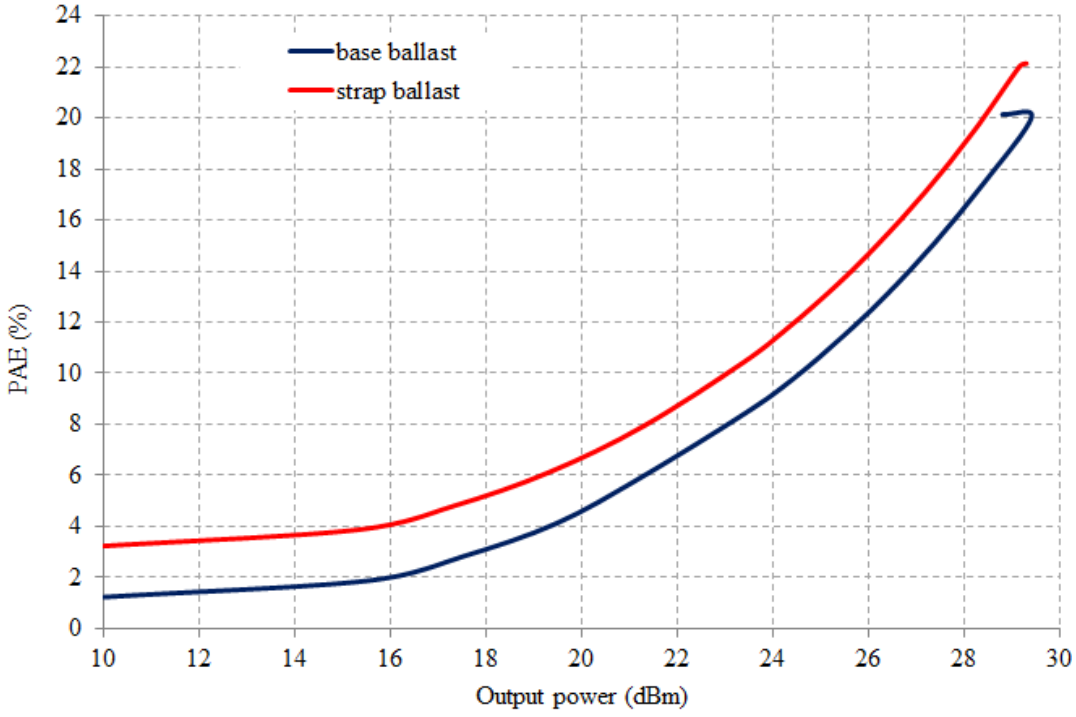


Figure 3.19: The PAE comparison plot across output power for both techniques. At higher output power, it can be observed that the PAE of base ballast configuration PA collapses.

Therefore it can be concluded strap resistors not only prevent the collapse of current at high input power, but also guarantees a higher linear output power and PAE delivery as compared to the conventional practice base ballast integration. Therefore, in this work, this concept is applied in the PA design as an effort to preserve its linear output power and PAE.

3.4 Power Cell Optimum Conduction Angle

3.4.1 Fourier Analysis

The trade-off between linear operation and efficiency is fundamentally determined by the PA's biasing point, alternately known as the conduction angle of the PA. Selecting an optimum conduction angle is essential in designing a linear and efficient PA. As the conduction angle reduces, the rise of even and odd orders components are more significant. Third order component adversely affects the linearity performance of the PA. Cripps has conducted a mathematical analysis to determine the even and odd order responses for a FET transistor (Cripps, RF Power Amplifiers for Wireless Communications, 2006). Adapting the analysis as a reference, a similar mathematical analysis has been done for the HBT transistor in this work and extended up to 5^{th} order components. Figure 3.20 illustrates the RF collector current waveform plot of a class B HBT amplifier.

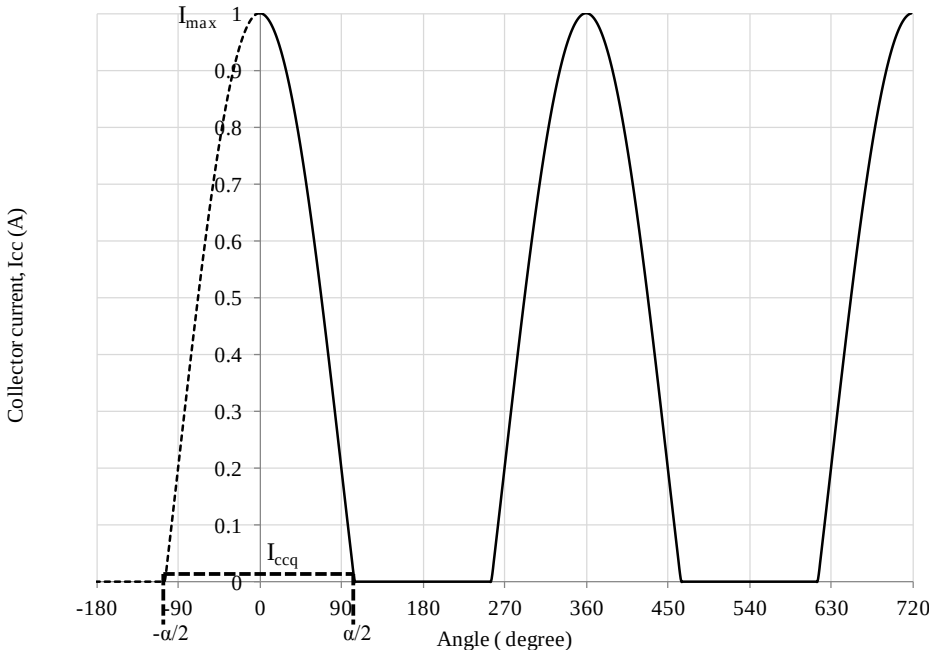


Figure 3.20: The collector current waveform plot. I_{ccq} is the quiescent biasing point whereas α/2 is the corresponding conduction angle

Mathematically, the illustrated waveform can be represented as:

$$I_{cc} = I_{ccq} + (I_{\max} - I_{ccq})\cos\theta \quad -\alpha/2 < \theta < \alpha/2 \tag{3.23}$$

where

$$\cos(\alpha/2) = -\left(\frac{I_{ccq}}{I_{\max} - I_{ccq}}\right) \tag{3.24}$$

Hence resulting,

$$I_{cc} = \frac{I_{\max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2)) \tag{3.25}$$

The Trigonometric Fourier Series (TFS) is applied to analyze equation (3.25). TFS is given as:

$$I_{cctotal} = I_{dc} + \sum_{n=1}^{\infty} I_{ccn} \cos(n\theta) + \sum_{n=1}^{\infty} I_{ccn} \sin(n\theta) \tag{3.26}$$

Since the collector current waveform in Figure 3.19 is an even waveform, therefore:

$$I_{cctotal} = I_{dc} + \sum_{n=1}^{\infty} I_{ccn} \cos(n\theta) \tag{3.27}$$

The DC current, I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) d\theta \tag{3.28}$$

whereas the magnitude of the nth order collector current components is given by:

$$I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)).\cos n\theta d\theta \tag{3.29}$$

Solving Equation (3.28) for DC term and Equation (3.29) for the fundamental component, I_1 (n=1) to fifth order I_5 (n=5) results in:

$$I_{dc} = \frac{I_{\max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{3.30}$$

$$I_1 = \frac{I_{\max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \tag{3.31}$$

$$I_2 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\sin\left(\frac{\alpha}{2}\right) - \frac{1}{3}\sin\left(\frac{3\alpha}{2}\right)\right] \quad (3.32)$$

$$I_3 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\frac{1}{3}\sin\alpha - \frac{1}{6}\sin 2\alpha\right] \quad (3.33)$$

$$I_4 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\frac{1}{6}\sin\frac{3\alpha}{2} - \frac{1}{10}\sin\frac{5\alpha}{2}\right] \quad (3.34)$$

$$I_5 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\frac{1}{10}\sin 2\alpha - \frac{1}{15}\sin 3\alpha\right] \quad (3.35)$$

The current equation (3.30) to (3.35) is plotted across the conduction angle as depicted in Figure 3.21.

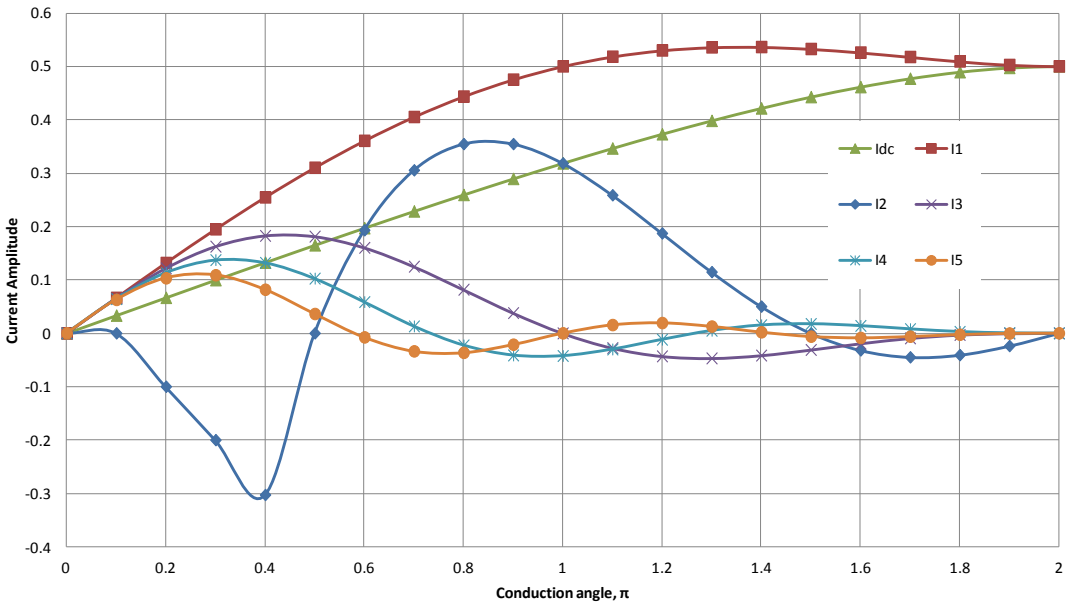


Figure 3.21: Current waveform normalized amplitude across conduction angle

It can be observed from Figure 3.21 that as the conduction angle increases, the fundamental current component increases due to the increment of the DC component. The second order

component which translates to second harmonic has an amplitude more than 0 from 0.5π to 1.5π. The peak is at 0.8π, which is close to class-B biasing. On the other hand, the third order current component also reduces as the conduction angle increases. An interesting observation is at the conduction angle within the range of $\pi<\alpha<1.8\pi$. In this region, the fundamental component is the highest and the third order component is at the lowest. This shows that it is theoretically possible to obtain higher fundamental output power, although the PA is not biased at class-A (conduction angle 2π) mode. The lowest third order component on the other hand promises a linear operation to a certain extent without sacrificing the efficiency at much.

3.4.2 Relationship between Conduction Angle and Efficiency

In order to determine the efficiency corresponding to $\alpha=2\pi$ which represents the conduction angle of a class-A amplifier, Equation (3.30) and (3.31) is appreciated, resulting in $I_{dc}= I_{max}/2\pi$ and $I_1= I_{max}/2\pi$ hence reflecting the efficiency of class A, which is I_1/I_{dc} to be 1. Using this result, the relationship between the conduction angle and efficiency in reference to class-A mode is given by:

$$\eta = \frac{I_1}{I_{dc}}.1 \tag{3.36}$$

$$\eta = \frac{I_1}{I_{dc}}.*\eta_{class-A} \tag{3.37}$$

Subsequently from equation (3.30) and (3.31):

$$\eta = \frac{\alpha - \sin\alpha}{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)} * \eta_{class-A} \tag{3.38}$$

From equation (3.38), it can be concluded that the efficiency of the PA increases as the conduction angle reduces. Table 3.1 tabulates the theoretical efficiency for various conduction angle of the PA.

Table 3.1: Conduction angle and corresponding quiescent current for a typical class-A, AB and B amplifier.

Class	Conduction angle, α	Efficiency, η (%)
A	2π	50
AB	1.3π	67.3
AB	1.2π	71
AB	1.1π	74.8
B	π	78.5

The resultant collector current waveform is depicted in Figure 3.22.

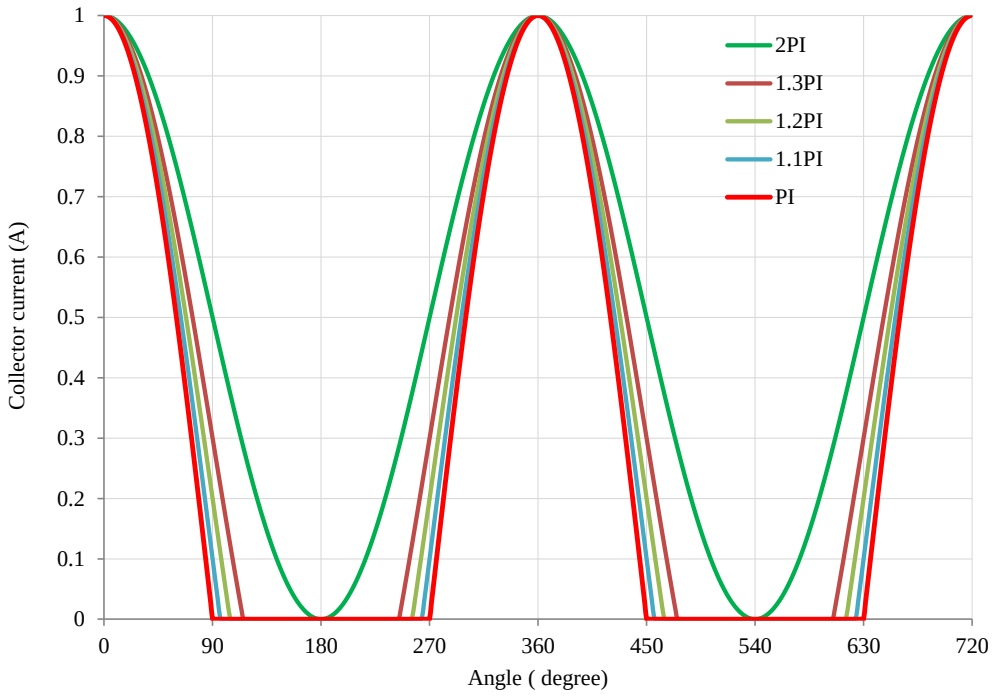


Figure 3.22: Collector current waveform for various conduction angle of the PA

3.4.3 Optimum Bias Point Determination

Section 3.4.1 and 3.4.2 shows the possibility to obtain optimum biasing point for the optimum ACLR and PAE. The impact of third order can be appreciated in the definition of ACLR (Carvalho & Pedro, 1999). In order to verify this, an experiment has been set up. In this experiment, a single stage amplifier has been tested by sweeping its biasing current to determine the optimum value for the best ACLR at the region close to class-B biasing point. Figure 3.23 illustrates the schematic of the designed amplifier whereas Figure 3.24 depicts the measurement setup.

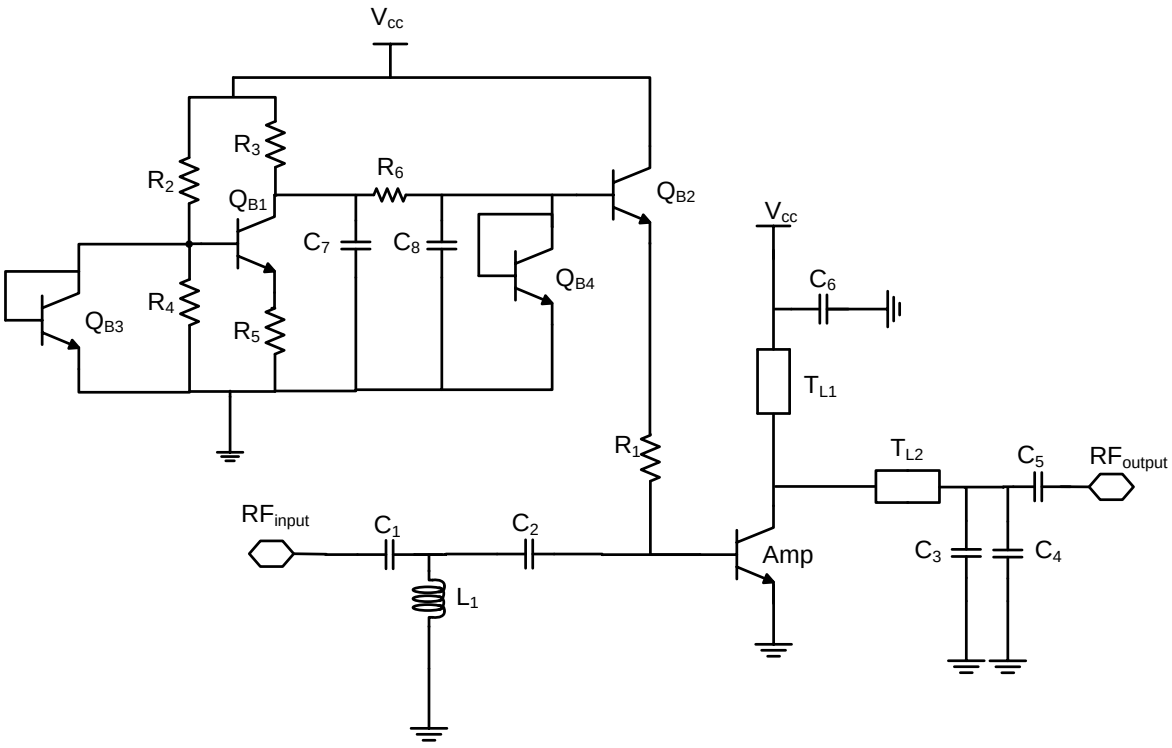


Figure 3.23: Single stage power amplifier for the optimum bias point determination

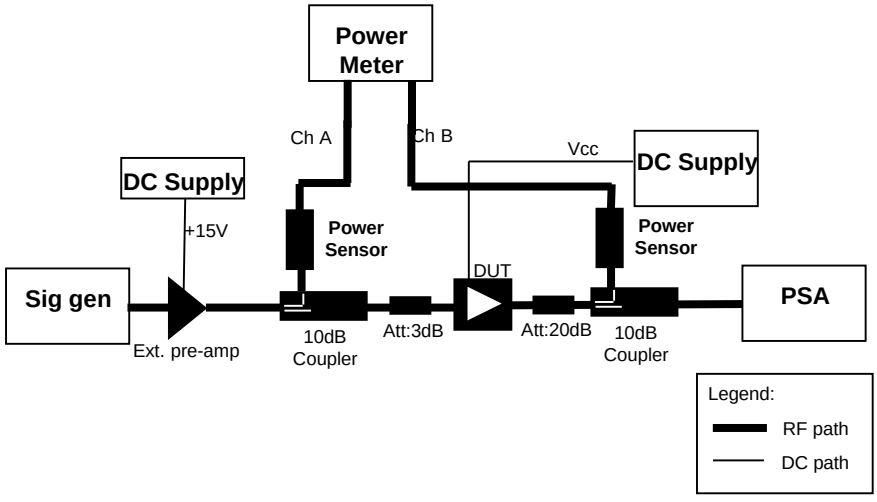


Figure 3.24: Measurement setup

Based on the measurement setup above, various bias point has been tested out to determine the best operating point for ACLR without significant trade-off in the PAE. The resultant plot is shown in Figure 3.25.

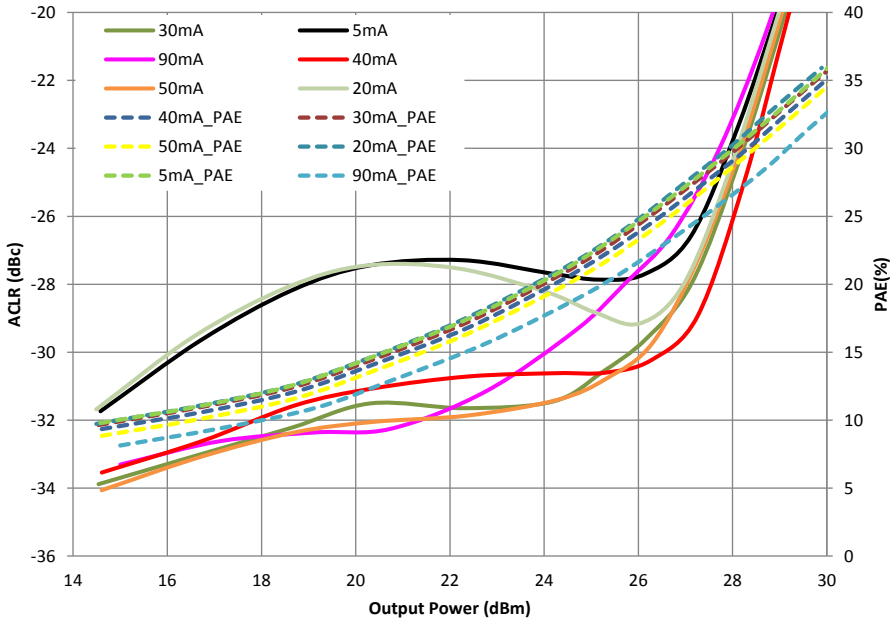


Figure 3.25: ACLR and PAE plot for various biasing current for the single stage amplifier

From Figure 3.25, it is evident that the PA delivers the best ACLR at a quiescent current of 40mA. The resultant PAE at the output power of 28dBm is 28%. Measurement has been done at operating frequency of 1.98GHz. Therefore, this quiescent current is desirably chosen to bias up the final stage amplifier.

3.5 Biasing Circuit Design

In order to provide a stable biasing platform for the main amplifiers, a base voltage stabilizer architecture is proposed to bias the amplifier as shown in Figure 3.26. In this bias configuration, an increase in the V_{be} of transistor Q_{B1}, due to the changes in supply voltage

V_{CC} is compensated by the voltage drop across the resistor, R_3. Also, the sensitivity of V_{be} due to Q_{B1} collector current is reduced by integrating the voltage degeneration resistor, R_5. Hence, the voltage delivered to the base-emitter junction of Q_{B2} becomes less sensitive to the changes in the input current of Q_{B1}.This circuit therefore provides a stable biasing condition for the RF transistors. The cascaded connections of Q_{B1} and Q_{B2} boost up the current gain of the biasing circuit, therefore provides more room for the main amplifier's base current swing which consist of 20 unit of power cells.

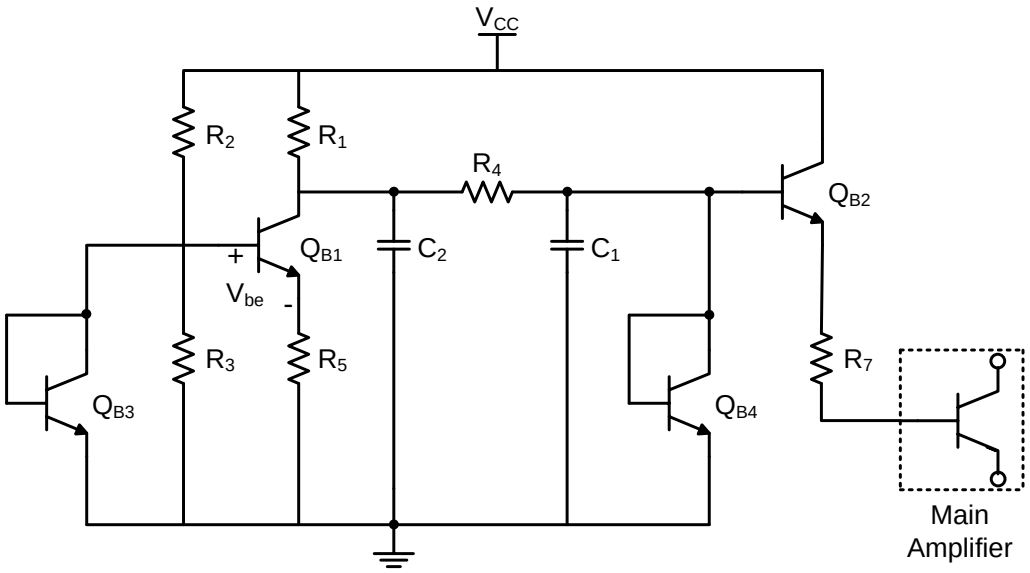


Figure 3.26: Proposed biasing circuit

Q_{B1} is biased through a voltage division network of resistor R_2 and R_3. Q_{B3} and Q_{B4} serve to be diode connected transistors outlining a consistent biasing profile across different temperature condition. R_4, C_1 and C_2 act as a low pass filter to protect the biasing circuit from the influential of higher frequency components.

CHAPTER 4. DESIGN OF WIDEBAND EFFICIENCY POWER AMPLIFIER

4.1. Introduction

Efficiency is a critical parameter in power amplifier design. Primarily, the conduction angle of the power amplifier marks the optimum operating point for a highly efficient with reasonable trade-off in linearity. However, this is just not enough to fulfill the specification requirement for handset operation as it operates at backed-off output power where the efficiency is much lower.

In order to improve the efficiency of the PA, the voltage and current waveform is manipulated. Figure 4.1 shows the voltage and current waveform for various classes of PA.

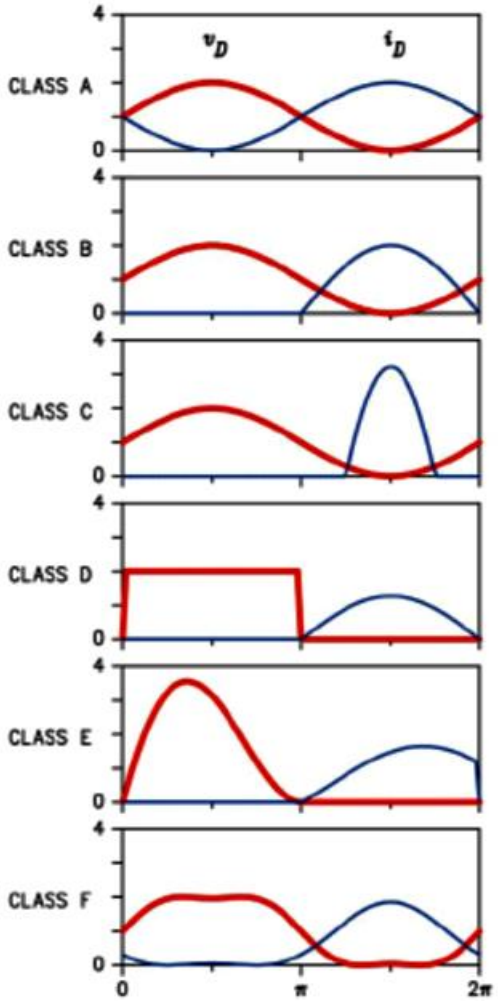


Figure 4.1: The voltage and current waveform of various classes of PA.

From Figure 4.1, it can be observed that as the voltage and current waveforms move away from its ideal sinusoidal shape (Class-A waveform), the efficiency of the PA improves (Class-B to Class-F). Typically, the class A PA's efficiency is 50% whereas class-F's efficiency is 100% (Colantonio, Giannini, & Limiti, 2009). The improvement in efficiency through waveform manipulations usually obtained by reducing the biasing level of the PA and at the same time employing additional matching networks to terminate the second and third harmonics. If all the harmonics are shorted, the voltage waveform represents a sinusoidal shape as shown in Figure 4.1 from Class-A to Class –C operation. As for Class-

F, the efficiency is boosted by imparting the odd harmonics to the voltage waveform which approximates a square wave (Raab, et al., 2002). Designing wideband harmonic resonators to have wideband efficiency usually ends with trade off in the fundamental output power (Tuffy, Zhu, & Brazil, 2011). As a result of this trade-off degradation in linear output power is observed as well.

4.2. Class-J Power Amplifier – Theoretical Analysis

4.2.1. Fundamental of Class-J Design

The class-J PA was invented by S.C. Cripps (Cripps, RF Power Amplifiers for Wireless Communications, 2006). It is capable of delivering the same efficiency and linearity as with the class-AB power amplifier without the need of band limiting transmission line harmonic short (Wright, Lees, Benedikt, Tasker, & Cripps, 2009). Instead, it employs a reactance harmonic termination technique to achieve the efficiency goal.

The conduction angle method to improve the efficiency of the power amplifier focuses in modifying the current waveform. Modifying the current waveform from sinusoidal (Class-A) to rectified sine wave (Class-B) increases the efficiency of the PA by the factor of $\pi/2$ which can be proven with equation (3.38) in Chapter 3. However, in class-J mode, the modification includes the voltage waveform as well which is explained through the following analysis.

If the fundamental RF output power is given as:

$$P_1 = \frac{V_{dc}}{\sqrt{2}} \frac{I_1}{\sqrt{2}} = \frac{V_{dc} I_1}{2} \tag{4.1}$$

And the DC power consumption of the PA is given as:

$$P_{dc} = V_{dc} I_{dc} \tag{4.2}$$

Referring to Equation (3.30) in Chapter 3, I_{dc} for class-A amplifier and class-B amplifier is $I_{max}/2$ and I_{max}/π respectively. For both classes of amplifier, the fundamental current I_1 is found to be the same with the utilization of equation (3.31), which is $I_{max}/2$. Therefore the efficiency of a class-A PA can be determined as:

$$\eta_{class-A} = \frac{P_1}{P_{dc}} \cdot 100\% \tag{4.3}$$

$$= \frac{1}{2} \frac{I_1}{I_{dc}} \cdot 100\%$$

$$= \frac{1}{2} \left[\frac{\frac{I_{\max}}{2}}{\frac{I_{\max}}{2}} \right] \cdot 100\%$$

$$= \frac{1}{2} \cdot 100\%$$

$$= 50\%$$

On the other hand the efficiency of class-B is determined as:

$$\eta_{class-B} = \frac{1}{2}\left[\frac{\frac{I_{\max}}{2}}{\frac{I_{\max}}{\pi}}\right]\cdot 100\% \qquad (4.4)$$

$$= \frac{\pi}{4}\cdot 100\%$$

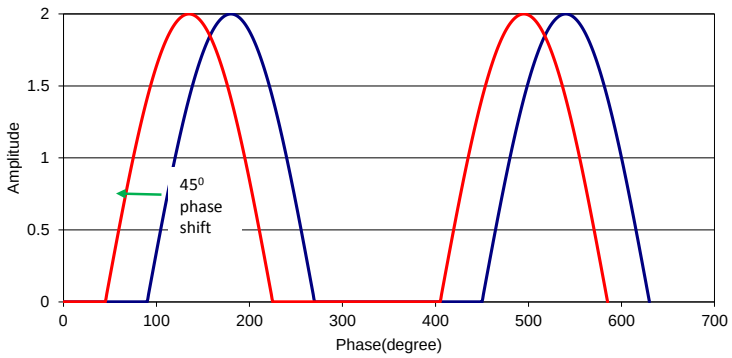
$$=78.5\%$$

It is evident from the calculation shown that modifying the current waveform from a sine wave to a rectified sine wave increases PA's efficiency by a factor of π/2.

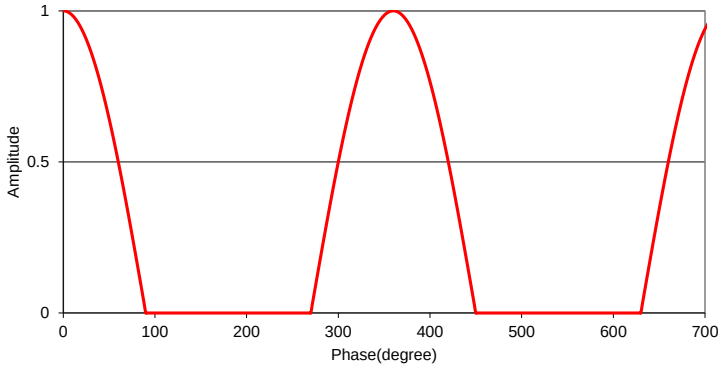
If the voltage waveform is also modified from sine wave to rectified sine wave as represented by the blue curve in Figure 4.2 (a), then the PA's efficiency expected to be increased further by another factor of π/2. However, this is impractical due to the requirement of the second harmonic load to be a negative resistance (Cripps, Advanced RF Power Amplifier Techniques for Modern Wireless and Microwave Systems, 2006). Nevertheless if the voltage waveform is displaced by 45º as represented by the red curve shown in Figure 4.2 (a), the second harmonic is now purely reactive (Cripps, Advanced RF Power Amplifier Techniques for Modern Wireless and Microwave Systems, 2006). This process defines class –J PA. Therefore, the effective efficiency in a class-J PA is given by:

$$\eta_{class-J} = \left(\frac{\pi}{4}\cdot\frac{\pi}{2}\cdot\cos\frac{\pi}{4}\right)\times 100\% \qquad (4.5)$$

$$= 87.2\%$$



(a)



(b)

Figure 4.2: The modification of the voltage waveform which is shown in (a) and the half wave rectified current waveform is shown in (b)

In practice, the efficiency of the class-J PA is lower as compared to the theoretical value due to the higher order even harmonics effect (Cripps, Advanced RF Power Amplifier Techniques for Modern Wireless and Microwave Systems, 2006).

Based on the Fourier analysis conducted on the half sinusoidal current waveform in Chapter 3 (Equation (3.30) to (3.35)), the current waveform in Figure 4.2(b) can be represented as:

$$I(\theta) = I_{\max}\left(\frac{1}{\pi} + \frac{1}{2}\cos\theta + \frac{2}{3\pi}\cos 2\theta + ...\right) \quad (4.6)$$

whereas the shifted voltage waveform in Figure 4.2(a) is represented as:

$$V(\theta) = kV_{dc}\left(\frac{1}{\pi} - \frac{1}{2}\cos\left(\theta + \partial\right) + \frac{2}{3\pi}\cos\left(2\left(\theta + \delta\right)\right) - .....\right)$$

……. (4.7)

where k is a constant with a value ≥ 2 which illustrates the class-J voltage waveform and δ represents the shifted phase of the voltage waveform (Moon, Kim, & Kim, 2010). The load impedance for each harmonic frequency can be calculated by:

$$Z_n = -\frac{V_n}{I_n} \quad (4.8)$$

Referring to Eq (4.6) and (4.7), if I_{max} =1 and k = π and the DC voltage is normalized to 1 by selecting k = π and V_{dc}= 1/π, the fundamental and second harmonic load impedances are given as:

$$Z_1 = 1\angle\partial \quad (4.9)$$

$$Z_2 = 1\angle\left(2\partial - \pi\right) \quad (4.10)$$

For class-J application, $\delta = \pi/4$ rad. Therefore in rectangular form, equations (4.9) and (4.10) can be represented as:

$$Z_1 = \frac{1}{\sqrt{2}}(1 + j) \tag{4.11}$$

$$Z_2 = -j \tag{4.12}$$

which shows presence of positive reactive component for the fundamental load impedance and negative reactive component for the second harmonic, assuming the rest of the harmonics are shorted.

The maximum value of the fundamental voltage of the class-J amplifier is increased by factor of $\sqrt{2}$ above the class B amplifier. Therefore the fundamental load impedance is set to $\sqrt{2}R_{opt}$ where R_{opt} is the load impedance of the amplifier (Moon, Kim, & Kim, 2010). On the other hand, in order to properly shape up the half-sinusoidal voltage waveform, the ratio between second harmonic voltage waveform to fundamental voltage waveform is set to $\frac{-\sqrt{2}}{4}$. Therefore:

$$V_{f0} = \frac{\sqrt{2}}{2} \tag{4.13}$$

where V_{fo} is the fundamental voltage waveform. The ratio between the second harmonic waveform (V_{2f0}) to V_{f0} is given as:

$$\frac{V_{2f0}}{V_{f0}} = \frac{-\sqrt{2}}{4} \tag{4.14}$$

Hence,

$$V_{2f0} = \frac{-\sqrt{2}}{4} \cdot \frac{\sqrt{2}}{2} = \frac{-1}{4} \tag{4.15}$$

With this, the second harmonic impedance Z_{2f0} is calculated as:

$$\begin{aligned} Z_{2f0} &= \frac{V_{2f0}}{I_{2f0}} \cdot R_{opt} \\ &= \frac{-\frac{1}{4}}{\frac{2}{3\pi} \cdot 1} \cdot R_{opt} \\ &= -\frac{3}{8} R_{opt} \\ &= \frac{3\pi}{8} R_{opt} \angle -90° \end{aligned} \tag{4.16}$$

4.2.2. Class-J Output Impedance Analysis with the Integration of Output Matching Network

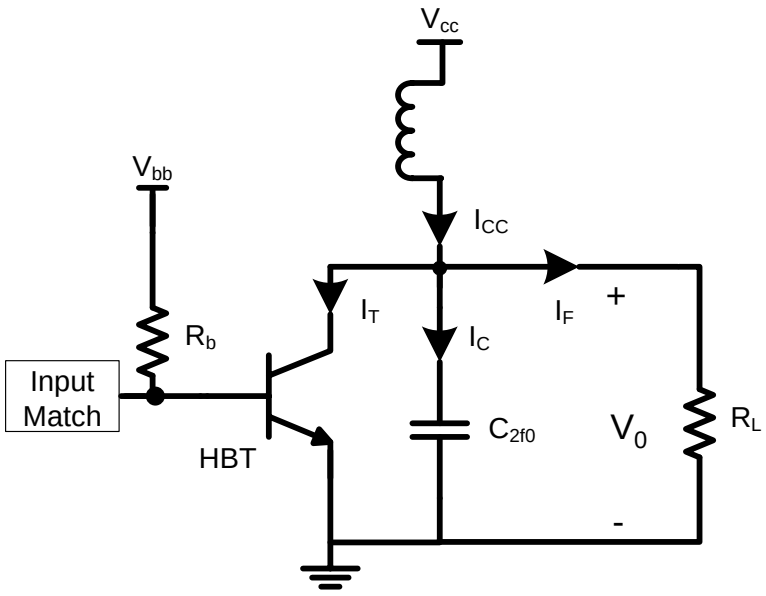


Figure 4.3: The schematic of class-J HBT PA

Figure 4.3 depicts the schematic of the HBT class-J PA. The transistor is biased in class-B mode where the RF output current waveform is half-wave rectified. Therefore:

$$I_T = I_{\max} \sin\theta \qquad \text{for} \quad 0 < \theta < \pi$$

$$= 0 \qquad \text{for} \quad \pi < \theta < 2\pi \tag{4.6}$$

The fundamental current component flowing in the matching network is given as:

$$I_F = I_1 \sin(\theta + \varphi) \tag{4.7}$$

where ϕ is the phase deviation contributed by the matching network and I_1 is fundamental current.

The current flowing into C_{2f0} of Figure 4.3 is:

$$I_C = I_{CC} - I_F - I_T \tag{4.8}$$

where the DC output current, $I_{CC} = \frac{I_{\max}}{\pi}$.

The output voltage V_0 is:

$$V_0 = \frac{1}{\omega C_{2f0}} \int_0^{\theta} I_C d\theta \tag{4.9}$$

$$= \frac{1}{\omega C_{2f0}} \left[\int_0^{\pi} I_C d\theta + \int_{\pi}^{\theta} I_C d\theta \right]$$

Therefore from conduction angle $0< \theta<\pi$,

$$V_0 = \frac{1}{\omega C_{2f0}} \int_0^{\pi} \left(\frac{I_{\max}}{\pi} - I_1 \sin(\theta + \varphi) - I_{\max} \sin\theta \right) d\theta \qquad (4.10)$$

The solution for equation (4.10) is given in (4.11):

$$V_0 = -\frac{1}{\omega C_{2f0}} \left(I_{\max} + 2I_1 \cos\varphi \right) \qquad (4.11)$$

The negative sign means the voltage and current are out of phase to each other.

From conduction angle $0< \theta<2\pi$, I_T of equation (4.8) is zero. Therefore:

$$V_0 = \frac{1}{\omega C_{2f0}} \int_0^{\pi} \left(\frac{I_{\max}}{\pi} - I_1 \sin(\theta + \varphi) \right) d\theta \qquad (4.12)$$

where the resultant is given as:

$$V_0 = -\frac{1}{\omega C_{2f0}} \left(I_1 \left[\cos(\theta + \varphi) - \cos\varphi \right] - \frac{I_{\max}}{\pi} \left[\theta - \pi \right] \right) \qquad (4.13)$$

Fourier analysis is conducted on the output voltage to determine its fundamental and second order components. The fundamental component is given as:

$$V_1 = \frac{1}{\omega C_{2f0}\pi} \left[\begin{array}{l} I_{\max} \left[-2\sin\theta + \frac{1}{\pi}(\cos\theta + \theta\sin\theta - 1) \right] - \\ I_1 \left[\sin\theta\cos\varphi + \frac{1}{2}\theta + \frac{1}{4}(\sin 2\theta\cos\varphi + \sin\varphi(1 + \cos 2\theta)) \right] \end{array} \right] + \qquad (4.14)$$

$$j \frac{1}{\omega C_{2f0}\pi} \left[\begin{array}{l} I_{\max} \left[\frac{1}{\pi}(\sin\theta - \theta\cos\theta) - 2(1 - \cos\theta) \right] - \\ I_1 \left[\cos\theta(1 - \cos\theta) - \frac{1}{2}\left(\frac{1}{2}\cos\varphi(1 - \cos 2\theta) - \sin\theta\left(\theta - \frac{1}{2}\sin 2\theta \right) \right) \right] \end{array} \right]$$

The second order component is:

$$V_2 = \frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} I_{\max}\left[\frac{1}{\pi}\left(\frac{1}{2}\theta\sin 2\theta - \frac{1}{4}\cos 2\theta + \frac{1}{4}\right) - \sin 2\theta\right] + \\ I_1\left[\sin(\theta-\varphi) - \frac{1}{3}\sin\varphi - \frac{1}{6}\sin(3\theta+\varphi) - \frac{1}{2}\sin 2\theta\cos\varphi\right] \end{array}\right] -$$

$$j\frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} \frac{1}{2}I_1\left(\cos\varphi\left[1-\cos 2\theta\right] + \cos\varphi\left[1-\cos\theta\right] - \frac{1}{3}\cos\varphi\left[1-\cos 3\theta\right] - \sin\theta\sin\varphi + \frac{1}{3}\sin 3\theta\sin\varphi\right) \\ -I_{\max}\left(\frac{1}{2\pi}\left(\frac{1}{2}\sin 2\theta - \theta\cos 2\theta\right) + \cos 2\theta - 1\right) \end{array}\right]$$

(4.15)

The full derivation of equation (4.10) to (4.15) is given in **Appendix B**. In equation (4.14) and (4.15) it can be observed that the fundamental (V_1) has a positive imaginary component whereas the second order voltage (V_2) has negative imaginary component. Therefore it can be confirmed mathematically that the polarity of the imaginary components will not be affected by the output matching network.

4.3 Simulation Analysis

As mentioned in Chapter 3, the R_{opt} is set to 5Ω which set to be optimum value for maximum output power and PAE. Therefore, the initial 2nd harmonic reactive termination capacitor value is calculated as below:

$$C_{2f0} = \frac{1}{2\pi f Z_{2f0}} \tag{4.18}$$

Since $Z_{2f0} = \frac{3\pi}{8} R_{opt}$ and R_{opt} = 5Ω, at the highest operating frequency of 2GHz,

C_{2f0} = 13.5pF.

In this work, by setting the C_{2f0} to 13.5pF, the fundamental load impedance is optimized to deliver the highest backed off PAE with saturated output power (P_{sat}) more than 32dBm. Figure 4.4 illustrates the schematic setup.

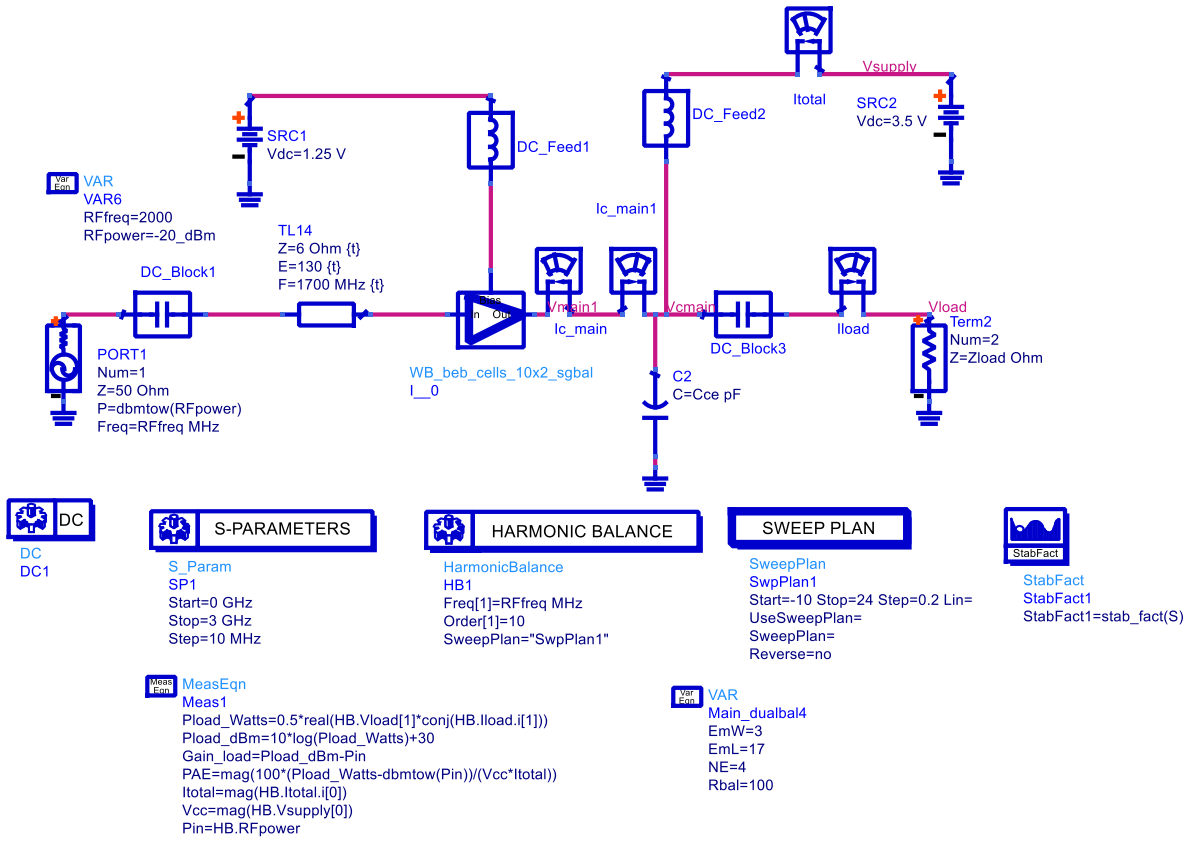


Figure 4.4: Class-J amplifier load pull simulation setup

In the setup above, with the aid of the harmonic balance simulator, the load impedance which is represented by Zload Ohm in Figure 4.4 is varied and the corresponding output power and PAE is obtained as the simulation result. The amplifier's quiescent collector current is set to 40mA which is obtained through the analysis result given in Figure 3.24 in Chapter 3. The amplifier is simulated up to its 10^{th} harmonic. As a result, the optimum fundamental load impedance obtained, Z_{out} is 2+j3. The resultant plot is illustrated in Figure 4.5.

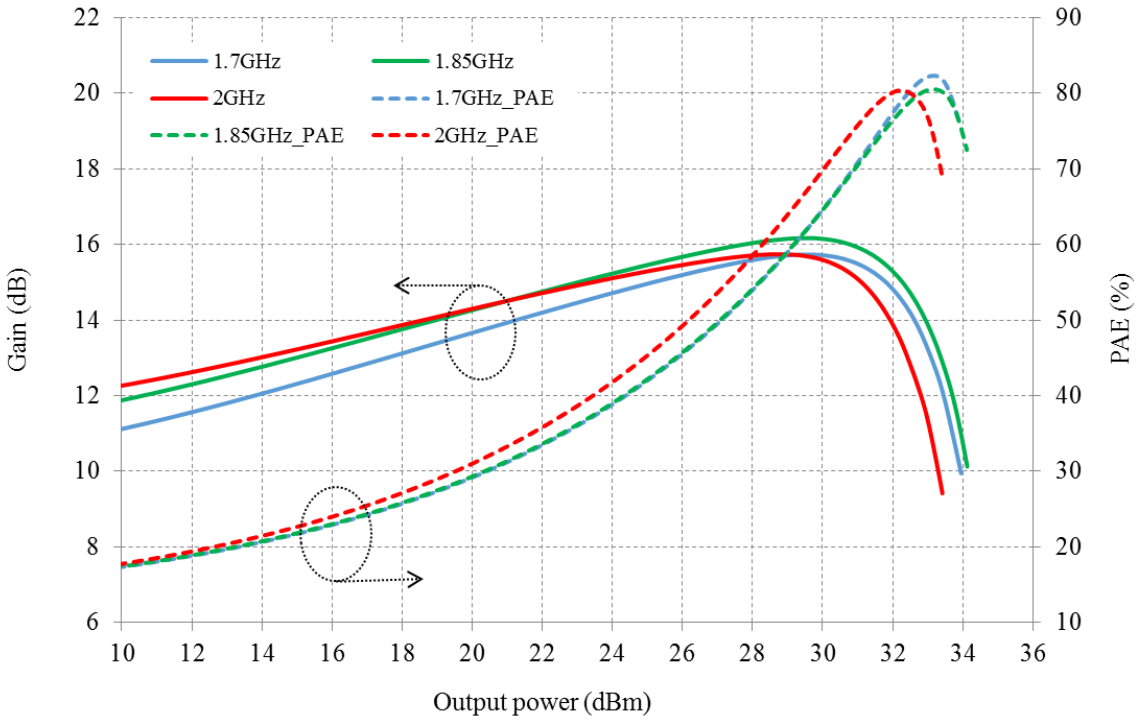


Figure 4.5: Gain and PAE plot across output power for Z_{out} 2+j3

In Figure 4.5, it can be observed that the maximum output power is indeed more than 32dBm from 1.7GHz up to 2GHz with PAE more than 50% at 28dBm of output power.

4.4 Output Matching Network Design

Figure 4.6 illustrate the proposed output matching network to transform the 50 ohm load impedance to the desired Z_{out} = 2 + j3.

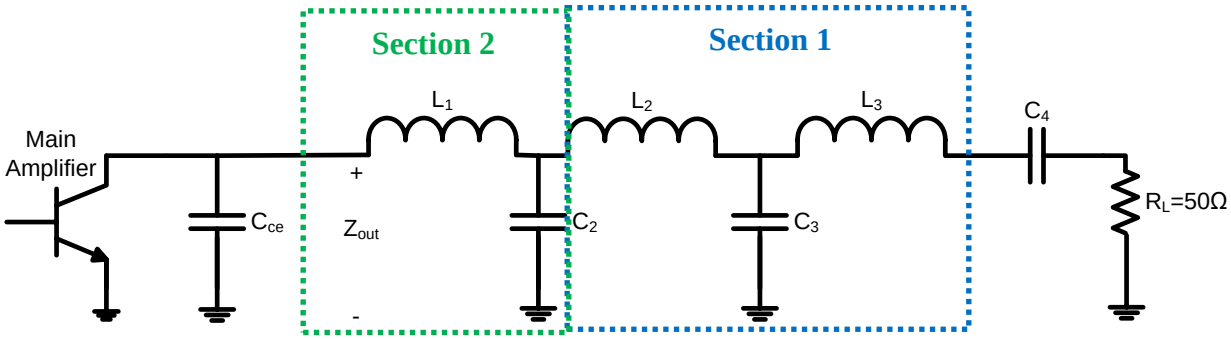


Figure 4.6: Output matching network topology of the class-J amplifier

The matching network can be divided into two sections which are:

a) Section 1 which compromises T-network L_2, C_3 and L_3 which transforms the 50 ohm load to an imaginary impedance of 25 ohm.

b) Section 2 which compromises an L-network C_2 and L_1 which transforms the 25 ohm to 2+j3 ohm.

In Section 1, values of L_2, C_3 and L_3 are determined using the following equations (Bahl, 2003):

$$L_2 = R_1 \frac{\sqrt{N-1}}{\omega_0} \tag{4.19}$$

$$C_3 = \frac{\sqrt{N-1} + \sqrt{\frac{N}{M} - 1}}{\omega_0 N R_1} \tag{4.20}$$

$$L_3 = R_2 \frac{\sqrt{\frac{N}{M} - 1}}{\omega_0} \tag{4.21}$$

where $M = \frac{R_2}{R_1} > 1$ and $N > M$

In this work, R_1= 25Ω and R_2 = 50Ω. Therefore M= 2 and N has been set to 2.2.

For section 2, the value of C_2 and L_1 are obtained through the following equations:

$$L_1 = \frac{3 + \sqrt{46}}{\omega_0} \tag{4.22}$$

$$C_2 = \frac{\frac{\sqrt{46}}{50}}{\omega_0} \tag{4.23}$$

where $\omega_0 = 2\pi f_o$ in which f_0 is the center frequency at 1.85GHz. The derivation of equation (4.22) and (4.23) has been given in **Appendix C**. The Impedance transformation plot is shown in Figure 4.7. The red oval plot in the smith chart in this figure represents the corresponding Q of the network which is 3.

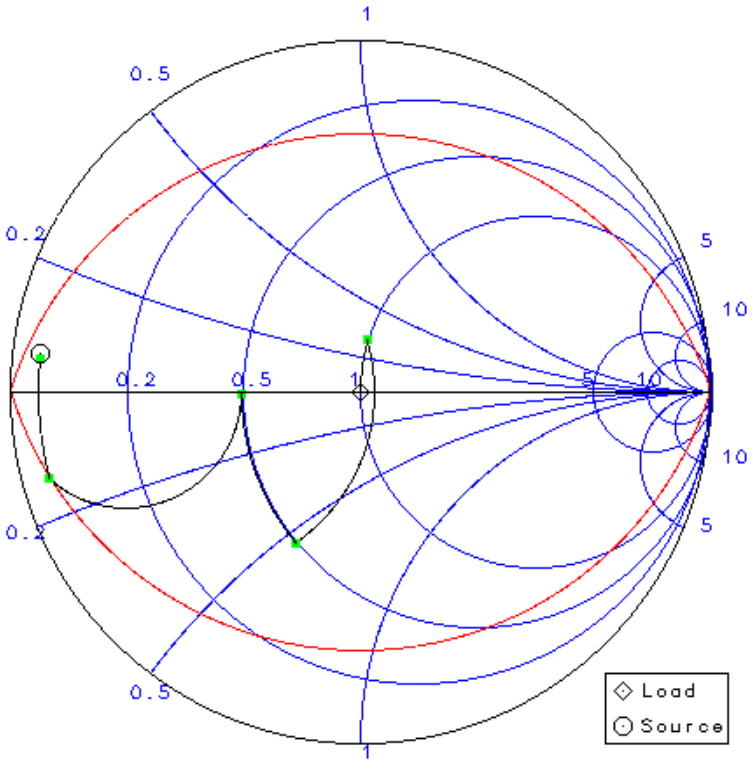


Figure 4.7: Impedance Transformation Plot

Subsequently, L_1, L_2 and L_3 are transformed to microstrip line using the following equations (Bahl, Fundamentals of RF and Microwave Transistor Amplifiers, 2009):

$$L(H/mm) = \frac{Z_0\sqrt{\varepsilon_{re}}}{c} \tag{4.25}$$

where c is the speed of light, $3x10^{11}$ $mms^{-1.}$ ε_{re} can be determined using Eq. (4.26).

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} F(W/h) \tag{4.26}$$

where F (W/h) is given as:

$$F(W/h)=\begin{cases}\left(1+12h/W\right)^{-1/2}+0.041\left(1-W/h\right)^{2} & (W/h\le 1)\\ \left(1+12h/W\right)^{-1/2} & (W/h\ge 1)\end{cases} \quad \ldots\ldots (4.27)$$

where h is the substrate thickness whereas W is the microstrip line width.

Z_0 is given as:

$$Z_0=\frac{\eta}{2\pi\sqrt{\varepsilon_{re}}}\ln\left(\frac{8h}{W}+0.25\frac{W}{h}\right) \qquad (W/h\le 1) \qquad (4.28a)$$

$$Z_0=\frac{\eta}{\sqrt{\varepsilon_{re}}}\left\{\frac{W}{h}+1.393+0.667\ln\left(\frac{W}{h}+1.444\right)\right\}^{-1} \qquad (W/h\ge 1)$$

……..... (4.28b)

where $\eta = 120\ \pi$ ohms.

The microstrip transmission lines have been routed in a 3mm x 3mm module chip on board (MCOB) package. Then a 3D simulation has been conducted to simulate which includes all the parasitic effects. The simulation result is illustrated in Figure 4.8. The corresponding output impedance which consist of the fundamental and second harmonics of operating frequency 1.7GHz to 2GHz is illustrated in Figure 4.9.

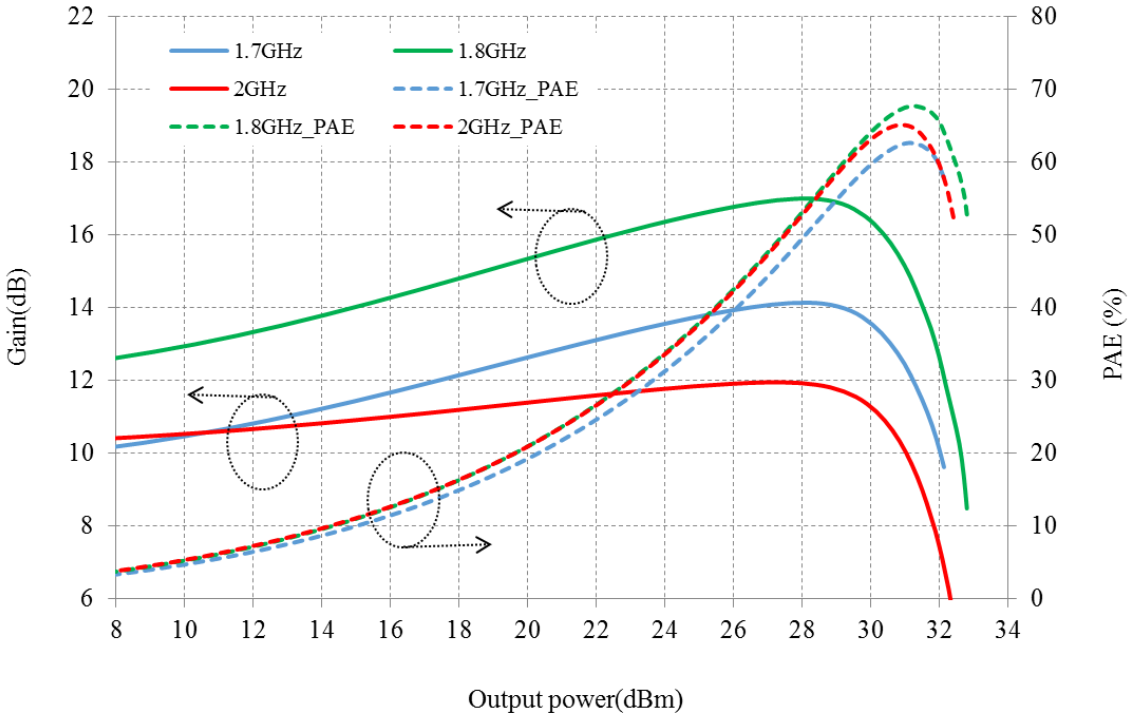


Figure 4.8: The simulated output power and PAE of the fully modelled final stage class-J amplifier

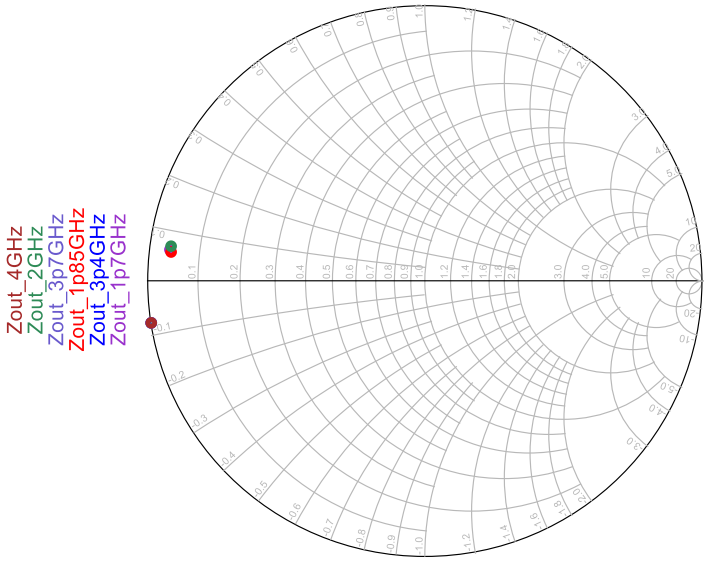
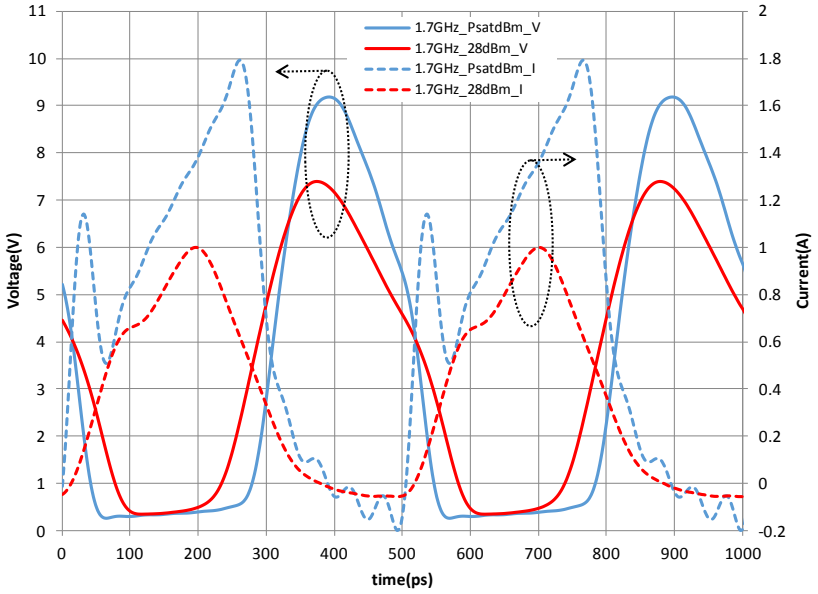
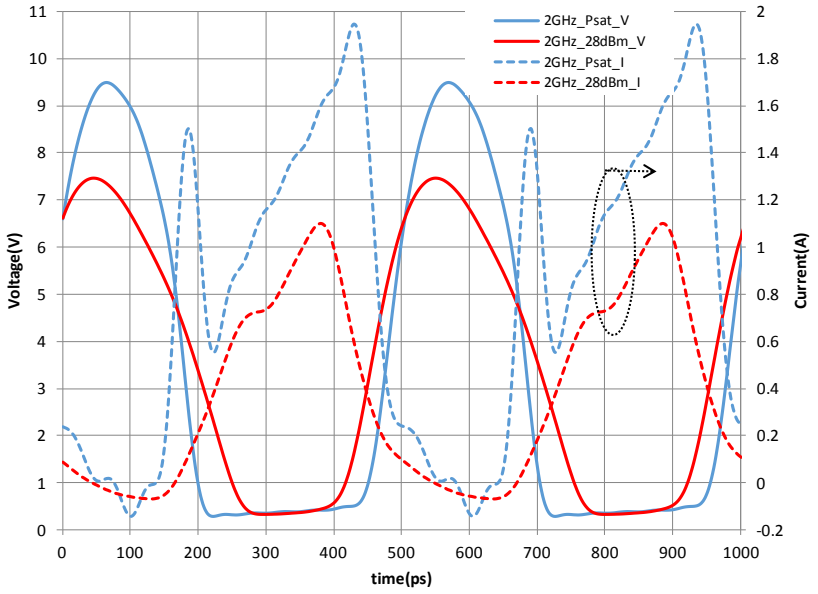


Figure 4.9: Class-J Output impedance and second harmonic plot across output power from 1.7GHz to 2GHz. Second harmonic termination is purely reactive across the frequencies

The voltage and current waveform at saturated output power (P_{sat}) and backed off output power (P_{bo}) 28dBm is illustrated in Figure 4.10.



(a)



(b)Figure 4.10: Class-J voltage and current waveform at P_{sat} and P_{bo} of 28dBm for (a) 1.7GHz and (b) 2GHz

It can be observed in Figure 4.10 that the current waveform of P_{sat} is bifurcated which translates to a drop in PAE at output power more than 31dBm. This is known as bifurcation phenomena (Cripps, RF Power Amplifiers for Wireless Communications, 2006). This issue can be minimized if the supply voltage of the PA is increased.

CHAPTER 5. ANALOG PRE-DISTORTER DESIGN AND THE REALIZATION OF HIGH GAIN POWER AMPLIFIER

5.1. Introduction

The goal of the linearization technique in this work is to reduce the back-off output power level due to PAPR backlash, thus exhibiting higher linear output power with low quiescent current. This is accomplished by integrating an analog pre-distorter (APD) block at the input of the low voltage main amplifier in the proposed architecture.

Operating the main amplifier at low quiescent current headroom results into gain expansion phenomena. This is due to the rise of the third order intermodulation distortion (IMD3) component as the output power increases (Carvalho & Pedro, 1999). The rise of the third order nonlinearity significantly degrades the ACLR (Carvalho & Pedro, Compact Formulas to Relate ACPR and NPR to Two Tone IMR and IP3, 1999). In order to mitigate this adverse effect, the APD architecture is integrated to produce IMD3 components, which are equal in amplitude but 180^{o} out-of-phase respective to the IMD3 spurs generated by the main amplifier. Thus, the IMD3 cancellation attained extends the overall linear output power span of the PA.

Finally, in order to boost up the power gain to be more than 30dB, a pre-driver amplifier is cascaded to the class-J PA with a built in APD. A higher gain cannot be achieved with a single stage amplifier due to the technology constraint whereby as the output power of the amplifier increases the power gain will be lower (Gilmore & Besser, 2003). The inter-stage matching network between the pre-driver amplifier and the APD

plays an important role to ensure a maximum power transfer from the input to output. Hence an appropriate matching elements needs to be designed and integrated in chip to achieve this goal. This chapter deliberately explains the adapted method.

5.2. Theoretical Analysis of APD Technique

Figure 5.1 conceptually illustrates the non-linear components generated by a PA which transmits a dual carrier signal.

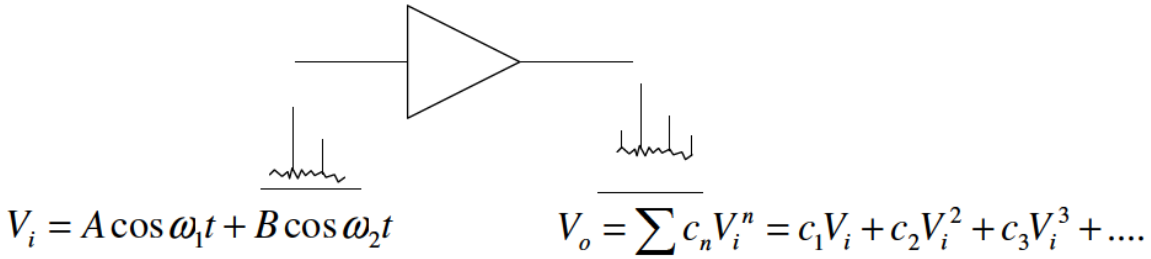


Figure 5.1: Nonlinear amplification of PA

If the input signal to the PA is given as:

$$V_i = A\cos\omega_1 t + B\cos\omega_2 t \tag{5.1}$$

where $A\cos\omega_1 t$ is the intended signal and $B\cos\omega_2 t$ is the interference signal. Then the amplified output signal, V_0 would be:

$$V_0 = \sum c_n V_i^n = c_1 V_i + c_2 V_i^2 + c_3 V_i^3 + ... \tag{5.2}$$

Substituting (5.1) into (5.2) and computing the third order term, results in:

$$c_3 V_i^3 = c_3 \left[A\cos\omega_1 t + B\cos\omega_2 t \right]^3 \tag{5.3}$$

Expanding equation (5.3):

$$c_3 V_i^3 = \left[\begin{array}{l} \left(\frac{3A^3}{4} + \frac{3AB^2}{2} \right) \cos \omega_1 t + \left(\frac{3B^3}{4} + \frac{3BA^2}{2} \right) \cos \omega_2 t + \frac{3AB^2}{2} \cos 2\omega_2 t \cos \omega_1 t \\ + \frac{3A^2 B}{2} \cos 2\omega_1 t \cos \omega_2 t + \frac{A^3}{4} \cos 3\omega_1 t + \frac{B^3}{4} \cos 3\omega_2 t \end{array} \right] \quad (5.4)$$

From the identity:

$$\cos 2\omega_2 t \cos \omega_1 t = \frac{1}{2} \left[\cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t \right] \quad (5.5)$$

$$\cos 2\omega_1 t \cos \omega_2 t = \frac{1}{2} \left[\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t \right] \quad (5.6)$$

Substituting (5.5) and (5.6) into (5.4) results in:

$$c_3 V_i^3 = \left[\begin{array}{l} \left(\frac{3A^3}{4} + \frac{3AB^2}{2} \right) \cos \omega_1 t + \left(\frac{3B^3}{4} + \frac{3BA^2}{2} \right) \cos \omega_2 t + \frac{3AB^2}{4} \left(\cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t \right) \\ + \frac{3A^2 B}{4} \left(\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t \right) + \frac{A^3}{4} \cos 3\omega_1 t + \frac{B^3}{4} \cos 3\omega_2 t \end{array} \right] \quad \ldots\ldots (5.7)$$

Figure 5.2 illustrates the generated IMD3 components derived in equation (5.7).

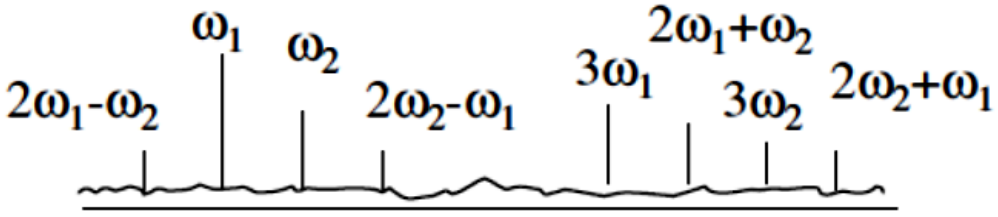


Figure 5.2: The resultant third order frequency components generated due to amplification of dual carrier signals ω_1 and ω_2

Respective to (5.7), if the interfering signal component with an amplitude of B and fundamental frequency of ω_1, is amplitude modulated, the exact applies same with the desired signal component. Additionally, if there is a presence of another interfering signal at frequency ω_3 as shown in Figure 5.3, IMD3 component with frequency of $(2\omega_2-\omega_3)=\omega_1$ will cause interference to the desired frequency at ω_1.

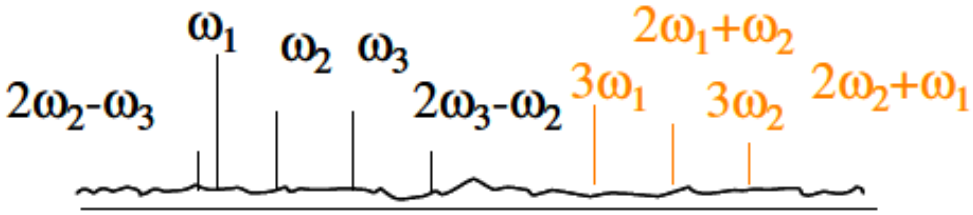


Figure 5.3: Interference component generated by ω_3 to ω_1

The APD operation as described in Figure 5.4 can be explained with the aid of the following simplified third order analysis.

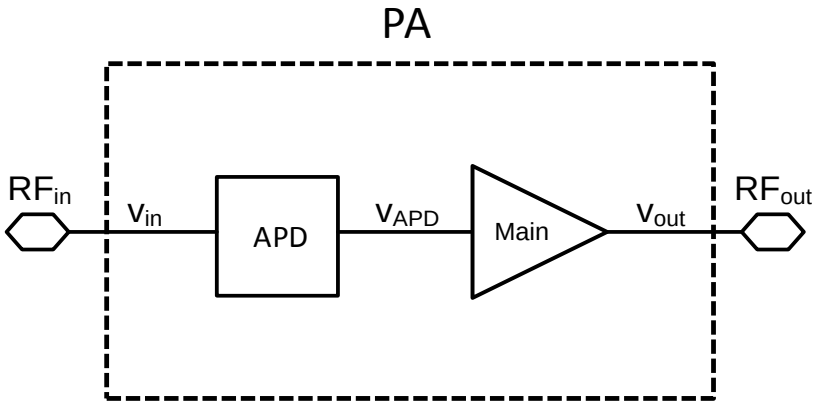


Figure 5.4: IMD3 cancellation analysis

From the expression of the power series, given by:

$$f(x) = \sum_{n=0}^{\infty} a_n x^n \tag{5.8}$$

$$v_{out} = a_0 + a_1 v_{APD} + a_2 v_{APD}^2 + a_3 v_{APD}^3 \tag{5.9}$$

$$v_{APD} = b_0 + b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3 \tag{5.10}$$

Taking into consideration the fundamental and third order components only and incorporating (5.10) into (5.9):

$$v_{out} = a_1[b_1 v_{in} + b_3 v_{in}^3] + a_3[b_1 v_{in} + b_3 v_{in}^3]^3 \tag{5.11}$$

$$= a_1 b_1 v_{in} + [a_1 b_3 + a_3 b_1^3] v_{in}^3 + 3a_3 b_1^2 b_3 v_{in}^5 + 3a_3 b_1 b_3^2 v_{in}^7 + a_3 b_3^3 v_{in}^9 \tag{5.12}$$

to nullify the third order interaction components which impacts the ACLR (Katz, 2001),

$$a_1 b_3 + a_3 b_1^3 = 0 \tag{5.13}$$

$$b_3 = \frac{-a_3 b_1^3}{a_1} \tag{5.14}$$

normalizing (5.14) in the context of the linear fundamental gain, establishes

$$b_3 = -a_3 \tag{5.15}$$

It can be concluded from (5.15) that in order to achieve IMD3 cancellation, the third order components generated at the output of the APD need to have an opposite response respective to the third order components generated by the main amplifier. In practice, this

can be achieved if an opposite AM-AM and AM-PM responses are generated between the APD and main amplifier (Katz, 2001).

5.3. APD Design Methodologies

5.3.1 Initial Design Methodologies

5.3.1.1 Passive Pre-distorter Linearizer

Figure 5.5 illustrates the topology of the proposed PA, which integrates a Class-E PA, passive pre-distorter linearizer and an output matching network ensuring a maximum linear output power at the designated PAE. The Class-E PA encapsulates a HBT transistor and a shunt capacitor, C_1. The passive pre-distorter is connected at the input of the Class-E PA, prior to the parallel RC network.

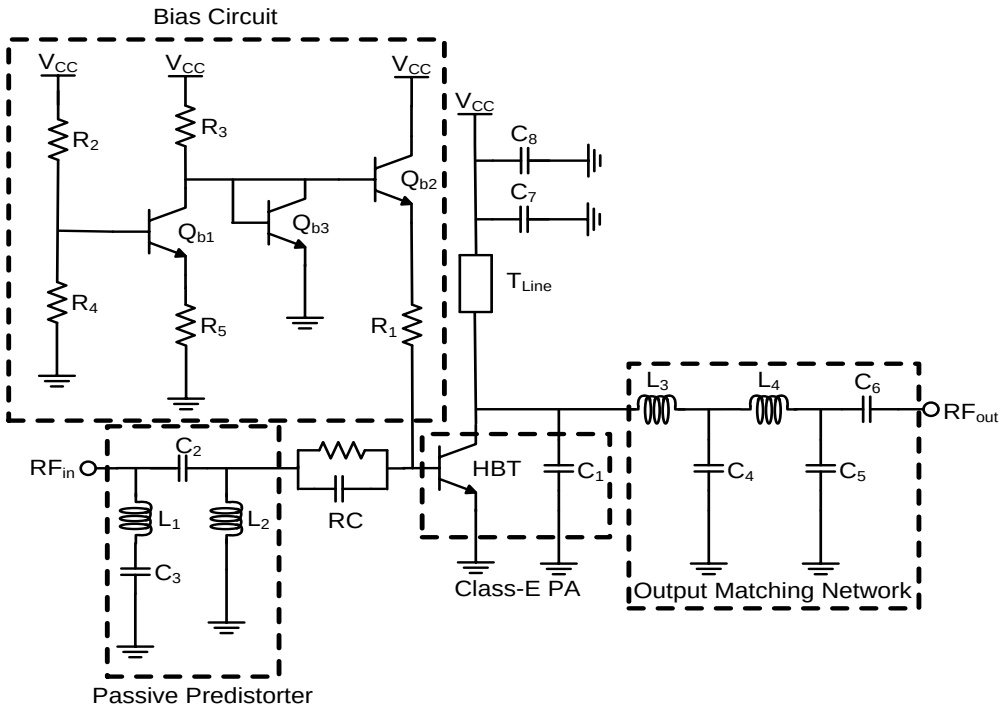


Figure 5.5: Proposed class-E LTE PA with passive pre-distorter

The passive pre-distorter linearizes the PA by generating an opposite AM-AM response to cancel off the gain expansion faced by the class-E PA. The resultant plot is illustrated in Figure 5.6 and 5.7 respectively. The limitation of this type of pre-distorter is that it is not capable to generate an opposite AM-PM response.

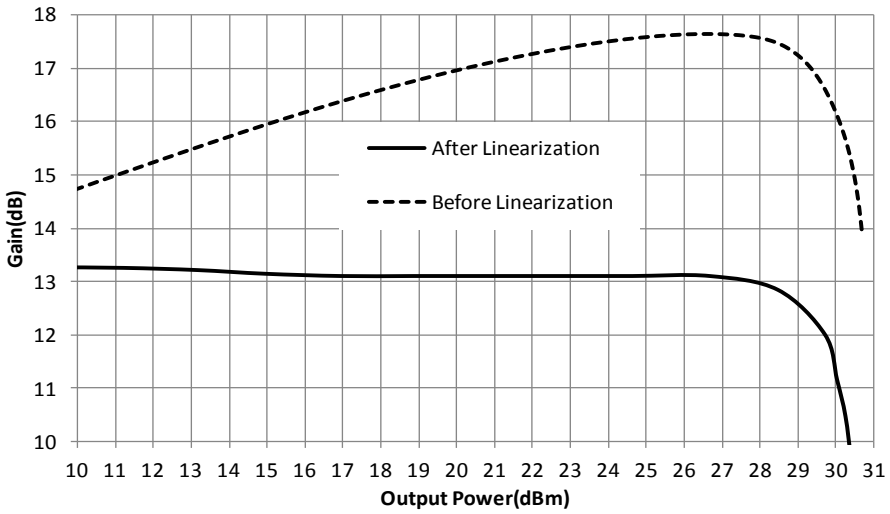


Figure 5.6: Measured AM-AM responses of the Class-E PA before and after linearization

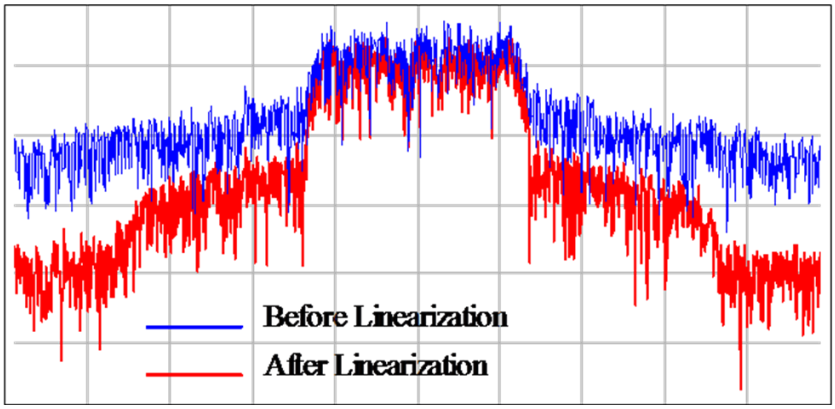


Figure 5.7: Simulated spectrum of the PA at 1.95 GHz

5.3.1.2 Dual stage linearizer

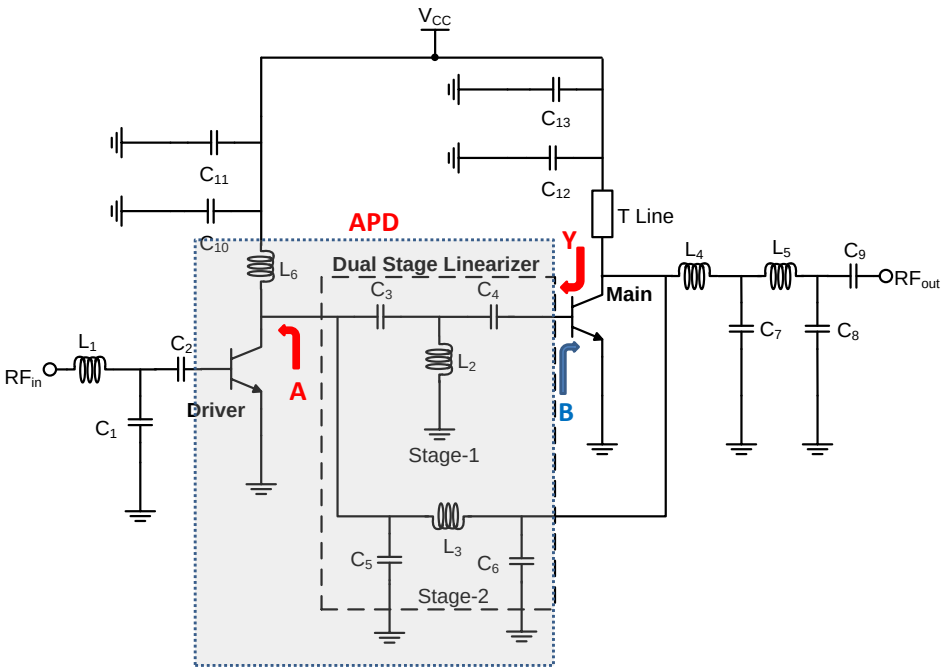


Figure 5.8: The schematic of the proposed PA with integrated dual stage linearizer network

Figure 5.8 illustrates the schematic of the proposed PA, consists of an integrated APD block connected to the input of the main amplifier. The APD block encapsulates of a driver amplifier, and a dual stage linearizer. The first stage of the linearizer, which comprises a T- network (C_3, L_2 and C_4), eliminates the low frequency components of the IMD3 generated by the driver amplifier. This low frequency components are capable of generating low frequency non-linear spurs through the coupling with the biasing circuit of the main amplifier under modulated transmission. This phenomenon is known as the bias modulation effect (Cripps, RF Power Amplifiers for Wireless Communications, 2006).

Here, the generation of an opposite AM-AM response is accomplished through the second stage linearizer consists of C_5, L_3 and C_6. The low pass PI network will feed back

the third order component back to the output of the driver amplifier, which results in a gain compression at location Y in Figure 5.8. Evidently from Figure 5.9, and with the aid of the dual stage linearizer, the PA is able to meet -30dBc ACLR specifications up to the output power of 30dBm, in comparison to the operation of the PA if it is only biased at low quiescent current in the absence of any linearizer circuit.

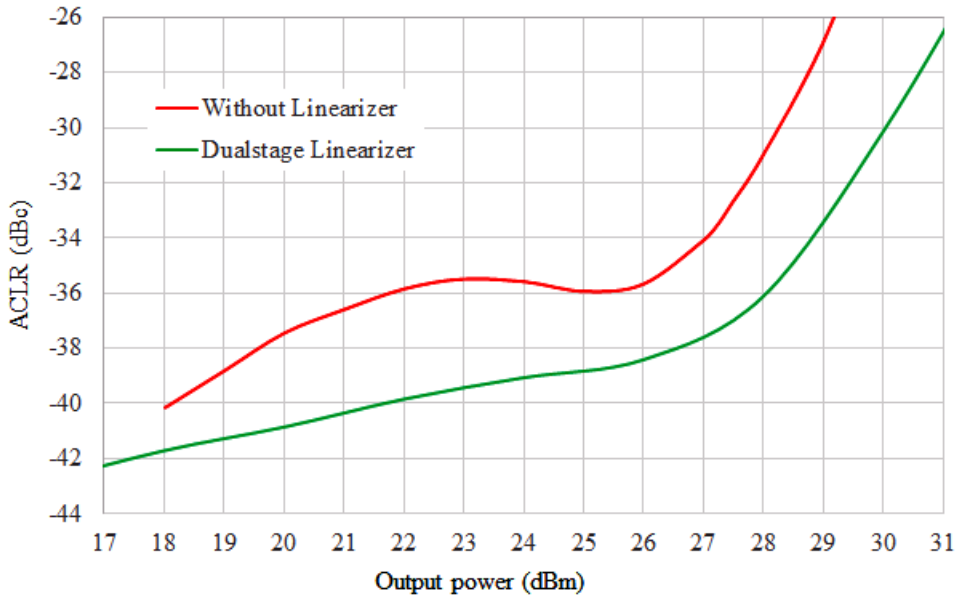


Figure 5.9: Measured ACLR comparison between PA with and without dual stage linearizer at 1980MHz. ACLR improves by 3dB at low output power and more than 3dB after surpassing 28dBm

5.3.2 Novel Wideband APD

The attempted methods in Section 5.3.1 are able to cover for a single LTE band. This is due the inability of both pre-distortion method to generate an opposite AM-PM response. In order to extend the operating LTE bandwidth, the phase pre-distorter and amplitude pre-distorter has been split to two sub circuits. The implementation of this novel circuit at the input of the class-J amplifier is illustrated in Figure 5.10.

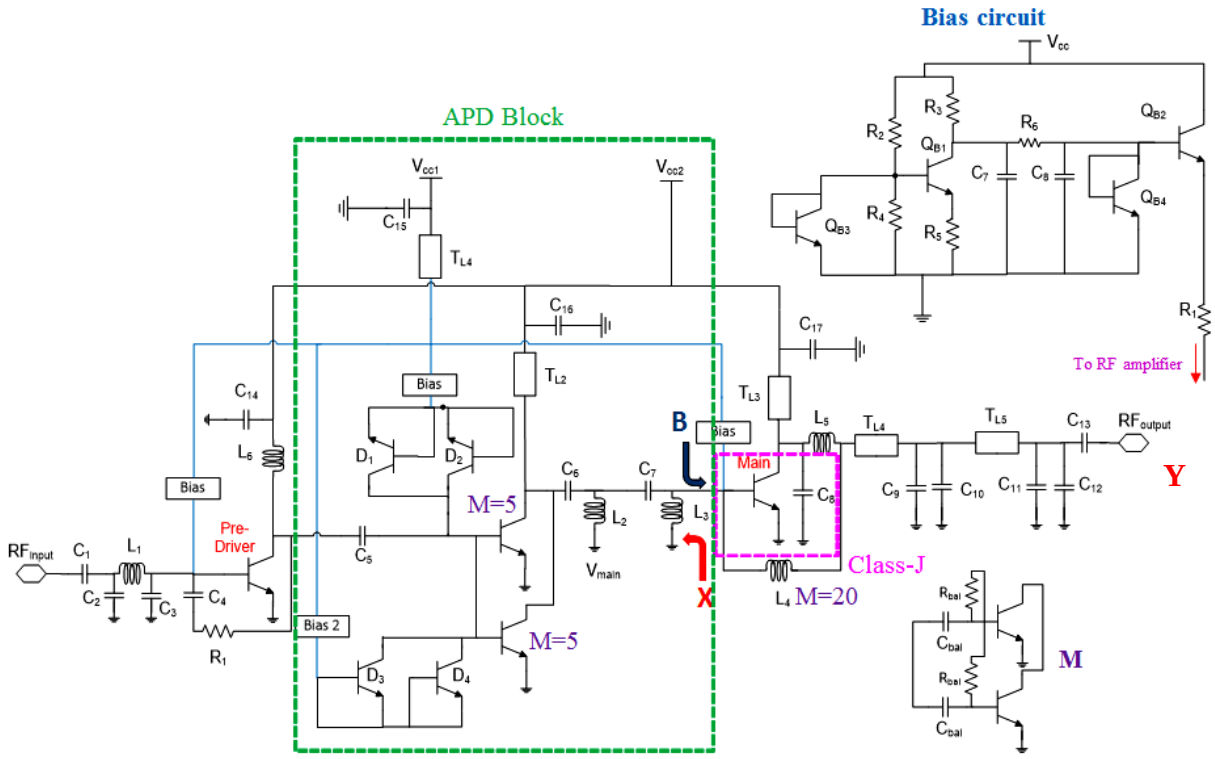
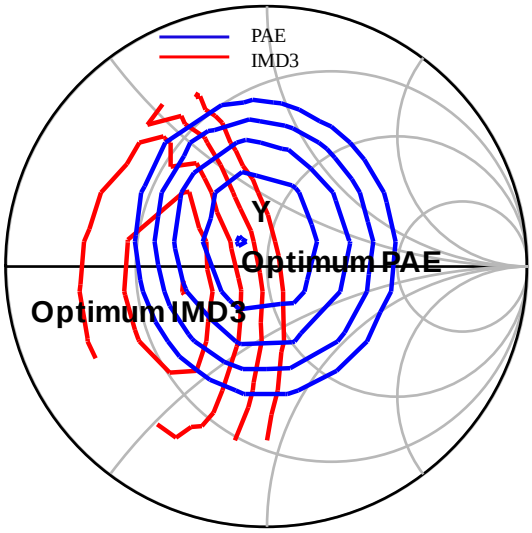
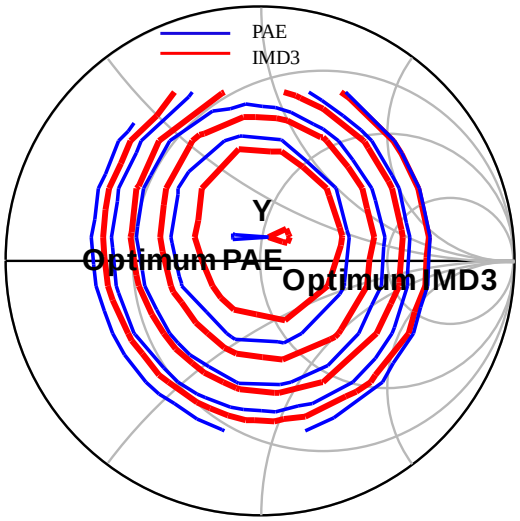


Figure 5.10: Schematic diagram of the LTE PA with built in APD. X denotes the output impedance of the APD, Y is the output impedance of the class-J amplifier. The Pre-Driver and main amplifier has the similar bias circuit topology whereas for the Driver, its bias circuit does not couples resistor R_1 of the bias circuit. M is equivalent to 1 unit cell

Figure 5.11 illustrates the IMD3 and PAE load pull contours prior to the linearization. Y is the output impedance of the main amplifier. These contours are plotted at an output power of 28dBm.



(a)



(b)

Figure 5.11: Load pull simulation result which illustrates the IMD3 and PAE contours of the main amplifier at output power 28dBm, (a) at 1.7GHz and (b) at 2GHz.The PAE contour is plotted in 1% step whereas the IMD3 contour is plotted in 2dB step

With the optimum conduction angle of 1.1π, Y is located closed to the optimum IMD3 point at 2GHz. However, it is still located almost 8dB away from the optimum IMD3 point at 1.7GHz, as described in Figure 5.11.

In HBT, spectral re-growth is mainly contributed by its base-collector parasitic capacitance C_{bc} (Kim, Kang, Lee, Chung, & Kang, 2002). To mitigate this effect, a novel phase cancellation method is proposed by integrating a base collector diode at the input of the driver amplifier. The reverse bias capacitance $C_{bc\text{-}reversebias}$ and forward bias capacitance $C_{bc\text{-}forwardbias}$ are expressed as follows (Gray, Hurst, Lewis, & Meyer, 2005):

$$C_{bc-reversebias} = \frac{C_{bc0}}{\left(1+\frac{V_{CB}}{\phi_0}\right)^{n_c}} \tag{5.16}$$

where C_{bc0} is the collector-base capacitance when $V_{CB}=0$,φ_0 is the collector base junction built in voltage and n_c is the grading coefficient of the collector base junction. In order to generate an opposite output phase response, the collector-base junction is forward biased. The aforementioned collector base capacitance is expressed by:

$$C_{bc-forwardbias} = \frac{C_{bc0}}{\left(1-\frac{V_{CB}}{\phi_0}\right)^{n_c}} \tag{5.17}$$

Based on (5.16) and (5.17) the positive and negative phase insight in effect to V_{CB} cancels off the $C_{bc\text{-}reversebias}$ with single forward biased base collector diode integration, $C_{bc\text{-}forwardbias}$. However, with the aid of two base collector diodes ($C_{bc\text{-}forwardbias} > C_{bc\text{-}reversebias}$), an opposite phase response (AM-PM) is observed at the output of the APD. The biasing profile of the diode to turn ON the driver amplifier in the APD is shown in Figure 5.12.

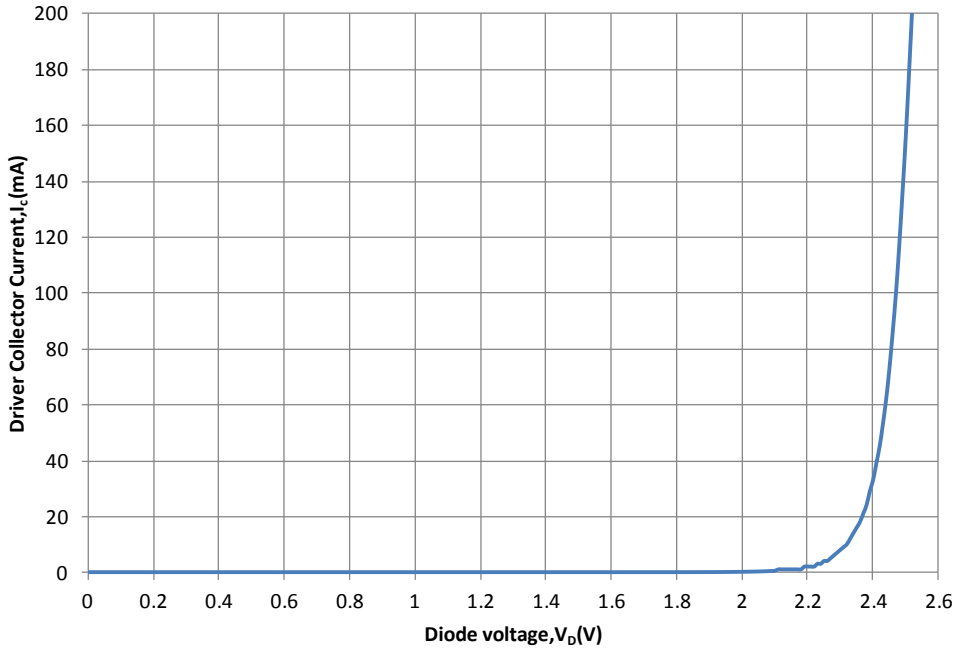


Figure 5.12: Biasing profile of the integrated parallel base collector diodes. The supply voltage to the diodes has to be at least 2.2V to turn ON the driver stage

The simulated AM-PM response at the output of the APD and class-J main amplifier are illustrated in Figure 5.13.

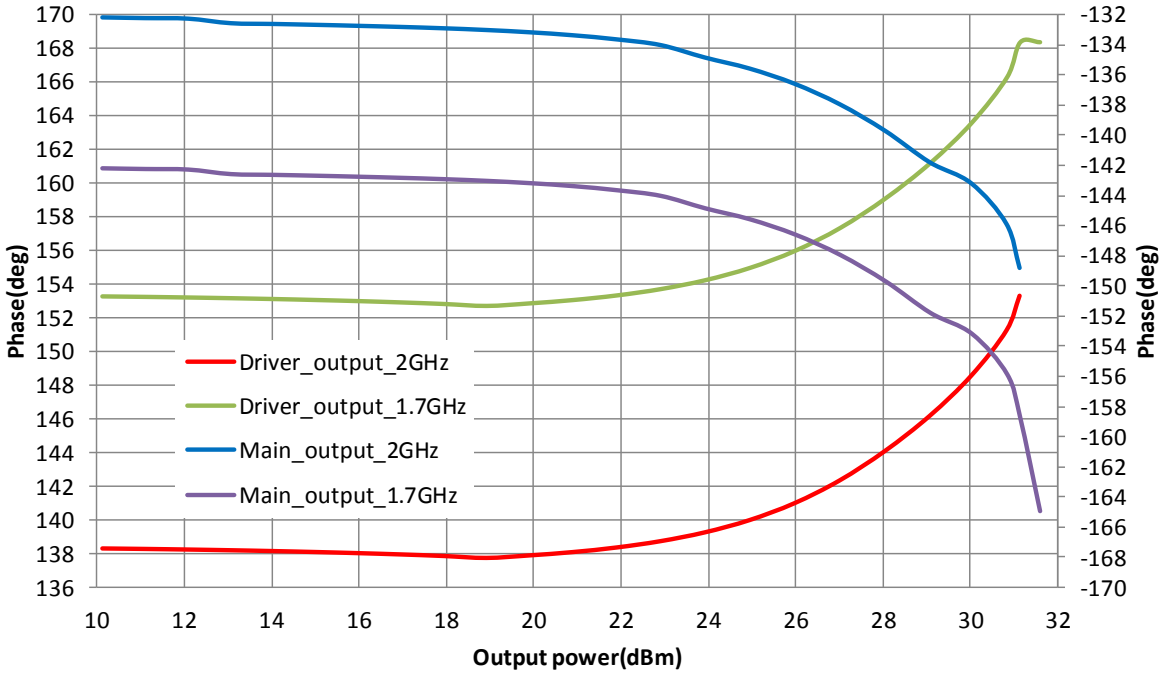


Figure 5.13: Simulated AM-PM responses of the APD and main amplifier across operating band

It can be observed from Figure 5.13 that the driver's phase expansion and main amplifier's phase compression cancels out each other contributing to the improvement of the IMD3 performance.

Generation of an opposite AM-AM response is accomplished through the T section intermediate matching network, consists of C_6, L_2, C_7 and L_3. The Smith plot of Figure 5.14 illustrates the location of the output impedance of the driver denoted at point A. This impedance is potentially matched to X, B or Bcon. Point B describes the input impedance of the main amplifier integrated with the ballasting network. Point X is the output impedance of the APD where else Bcon is the conjugate of B. Based on the profile of Figure 5.15, matching towards point X observes a favorable gain compression which

compensates the gain expansion of the main amplifier. Matching towards point B observes a gain expansion begins from lower output power which would not result into a desirable IMD3 cancellation. Point Bcon observes a flat profile till the 1dB compression point in which results into a similar effect as with point B matching.

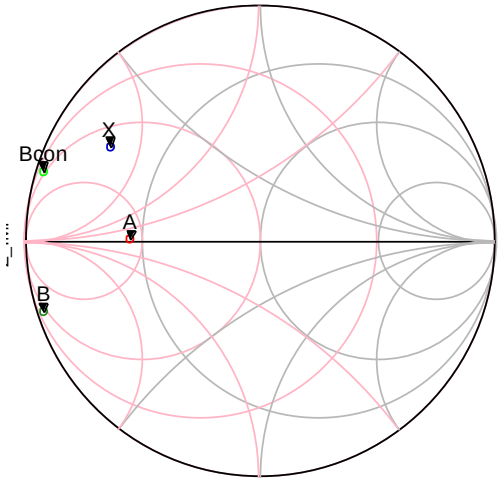


Figure 5.14: Location of the impedance point of the driver (A), main amplifier (B) and APD(X) at 1.7GHz

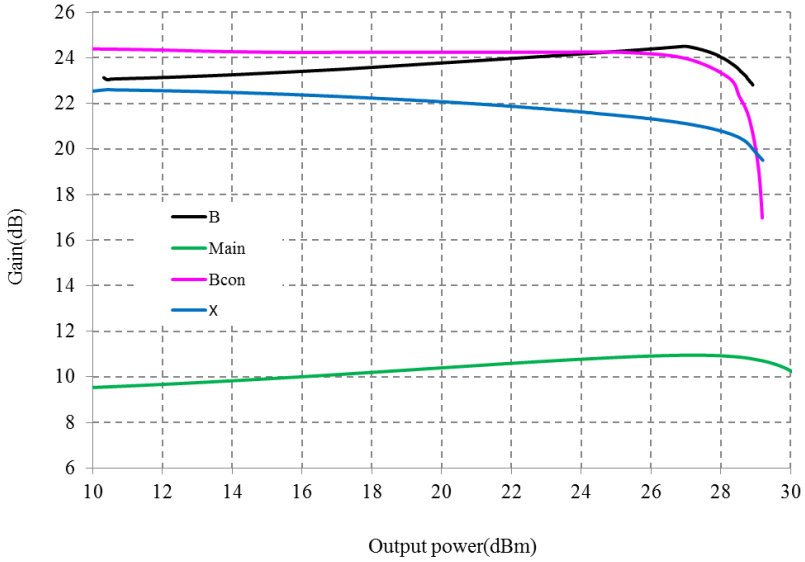
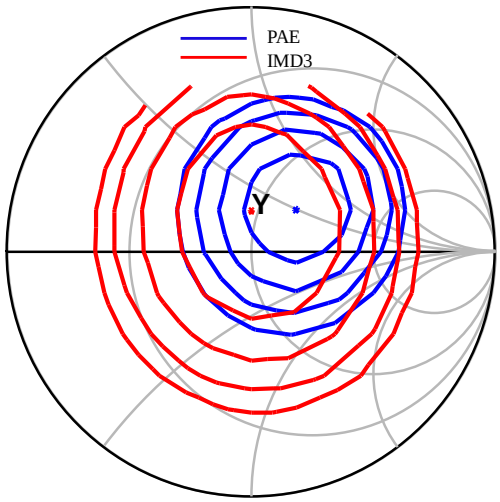
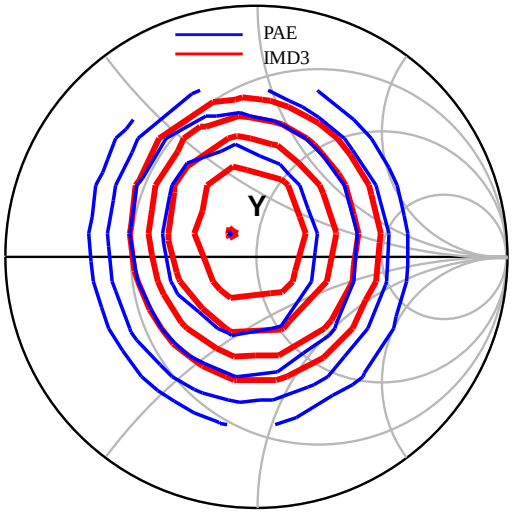


Figure 5.15. AM-AM profile for various intermediate matching network impedances mentioned in Figure 5.14.

The effect of AM-AM and AM-PM cancellation between the APD and main amplifier in the PA is illustrated in Figure 5.16. The IMD3 optimum impedance moves to location Y for 1.7GHz and 2GHz while the PAE degrades slightly due to the current consumption of the APD.



(a)



(b)

Figure 5.16: IMD3 and PAE contours of the PA after linearization at (a) 1.7GHz and (b) 2GHz

5.4 High Gain Power Amplifier Design

For an operation of the amplifier with a cumulative gain of 35dB, an additional pre-driver stage has been cascaded to the amplification chain. The matching network between the pre-driver and input of the APD has been designed to have a high operating gain, which can be expressed as (Gonzalez, 1997):

$$G_p = \frac{\text{Power delivered to the load}}{\text{Power input to the network}} \tag{5.18a}$$

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{5.18b}$$

where Γ_{IN} and Γ_L can be expressed as follows:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{5.19}$$

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{5.20}$$

where S_{11} is the input return loss, S_{22} is the output return loss and S_{21} is the gain of the pre-driver. On the other hand, Z_L represents the load impedance and Z_0 represents the characteristic impedance, respectively. The characteristics impedance is set to 50 ohm as a tradeoff between lowest loss and highest power carrying capability (Pozar, 2005). Besides high operating gain, the designed matching network also ensures a maximum power transfer occurs from output of the driver to the input of the APD.

Another important parameter which has been given priority in this paper is the unconditional stability factor, which known the Rollett factor, K (Rollett, 1962). The power amplifier has been designed to meet this criterion, which is conditioned as (Ludwig & Bretchko, 2000):-

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} > 1 \qquad (5.21)$$

Besides the above mentioned stability factor, the source and load stability circles of the integrated PA has also been plotted to ensure it is located outside the Smith chart to operate in unconditional stability mode. The plots are reviewed in Chapter 6.

CHAPTER 6. MEASUREMENT RESULTS

6.1 Measurement Station Setup

The measurement result has been categorized in to two sections:

i) Small signal analysis

ii) Large signal analysis

The small signal measurement involves the S-Parameter measurement whereas the large signal measurement includes the 1dB compression point (P1dB), ACLR and error vector magnitude (EVM) measurements. Figure 6.1 shows the setup for small signal measurement whereas Figure 6.2 shows the large signal measurement setup. The network analyzer in Figure 6.1 is used to measure the input return loss (S_{11}), output return loss (S_{22}) and power gain (S_{21}). The DUT needs one 4-channels power supply for V_{cc}, $V_{c1,}$ $V_{c2,}$ and V_{c3} .V_{c1}, V_{c2} and V_{c3} will turn on the pre- driver, driver and main amplifier stages respectively. In Figure 6.2, two power meters are used to measure the input and output power respectively. A spectrum analyzer is used to measure ACLR and EVM performance of the PA. A signal generator is use to supply the LTE modulated signal at the input of the PA.

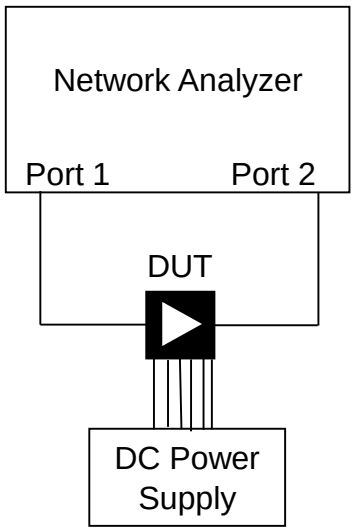


Figure 6.1: Small signal measurement setup

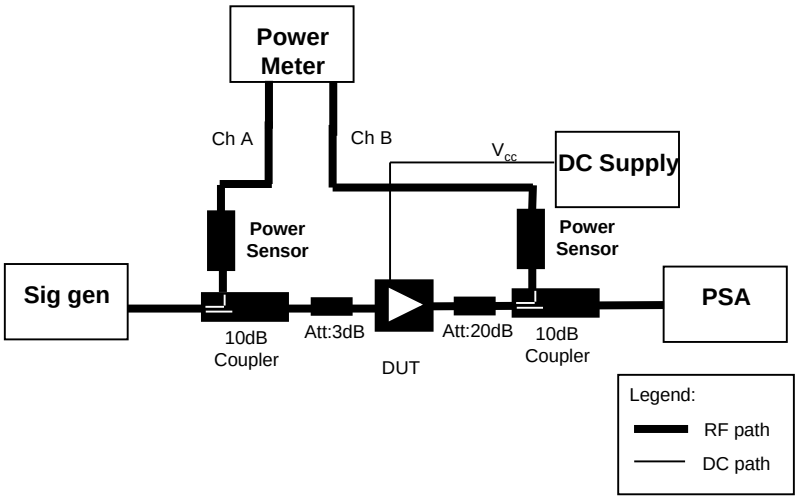


Figure 6.2: Large signal measurement setup

A 20dB attenuator is placed at the output to protect the power meter and spectrum analyzer from any possibility of damages caused by high output power transmission. The clock signals of all the signal generator and spectrum analyzer needs to be synchronized to the default 10MHz in order for them to run simultaneously. The measurement is automated with the aid of Agilent-Vee software to ease data collection. Before the measurement is

executed, the RF signal path is calibrated to take into account the input and output path losses.

Figure 6.3 illustrates the microphotograph of the die, fabricated in 2µm InGaP/GaAs HBT process. The size of the die is 950µm x 900µm. The class-J amplifier and APD are integrated in a single chip, along with the driver and pre-driver amplifiers.

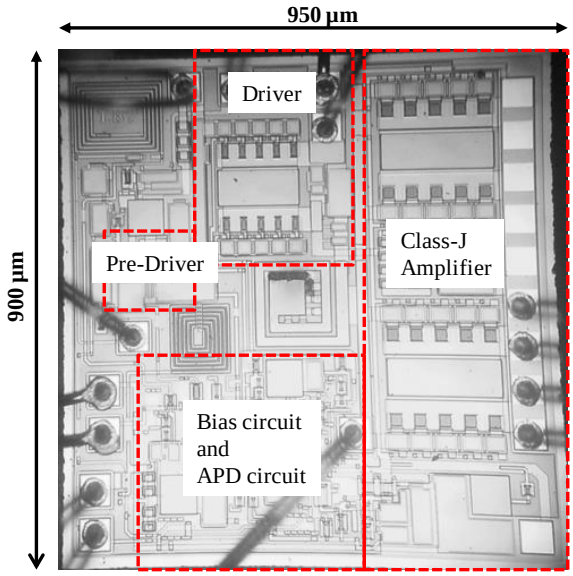


Figure 6.3: Die microphotograph of the fabricated PA with integrated APD .The size of the die is less than 1mm x 1mm

6.2 Measurement Results

6.2.1 Small Signal Measurement Results

The supply voltage headroom of the LTE PA is 3.3V. The simulated and measured S-parameter of the proposed PA is shown in Figure 6.4. The S_{11} and S_{22} are well matched from 1.7GHz to 2.1GHz, with a corresponding gain S_{21} more than 35dB across 300MHz bandwidth. A low S_{11} indicates that the APD does not generate a severe input mismatch loss at the fundamental frequency.

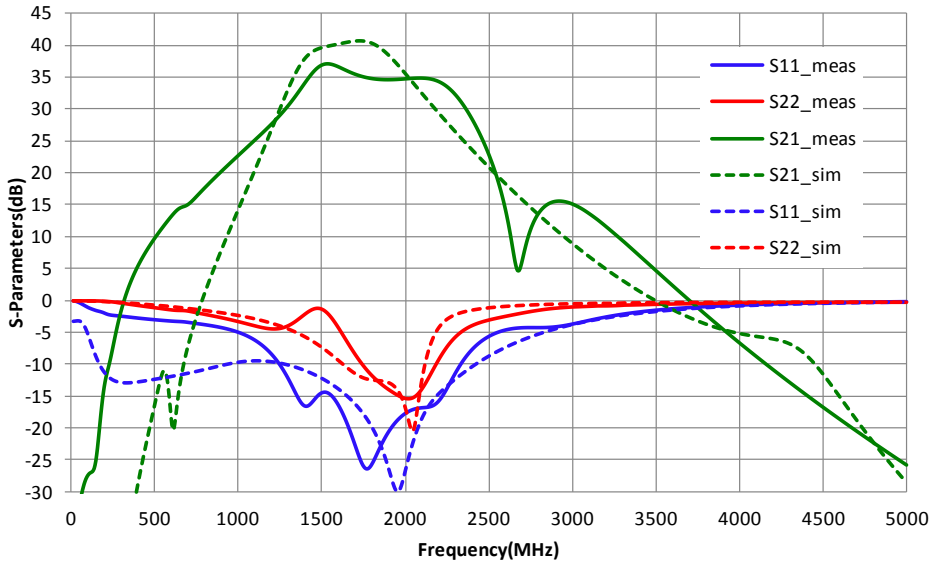


Figure 6.4: Measured and simulated S-parameters of the PA with supply headroom of 3.3V

With more than 35dB of power gain, the PA maintains to be unconditionally stable. The K-factor plot is illustrated in Figure 6.5. From DC to 5GHz, K-Factor is more than 1.

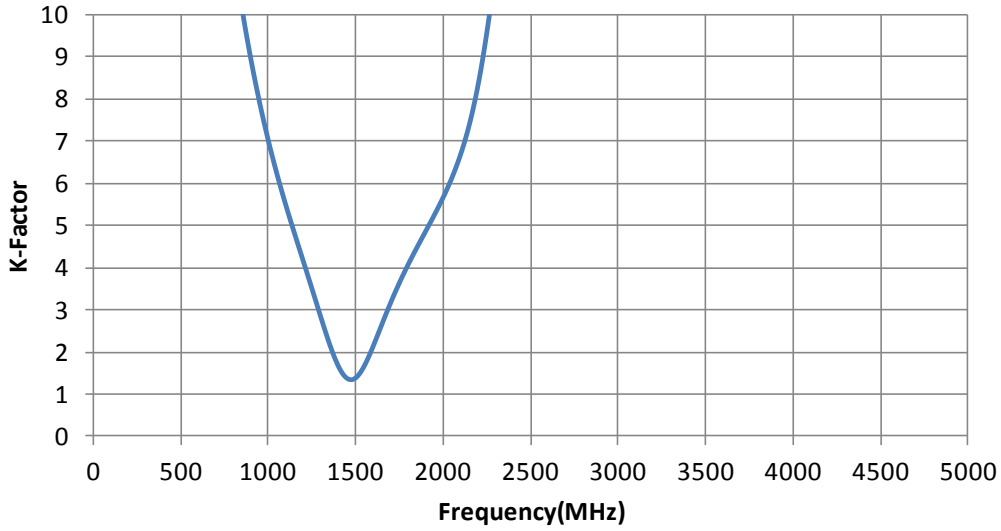


Figure 6.5: PA has K-Factor >1 from DC up to 5GHz

In Figure 6.6, the source and load stability circles are plotted together with the Smith chart. The source and load stability circles are located outside the Smith chart which translates to unconditional stability.

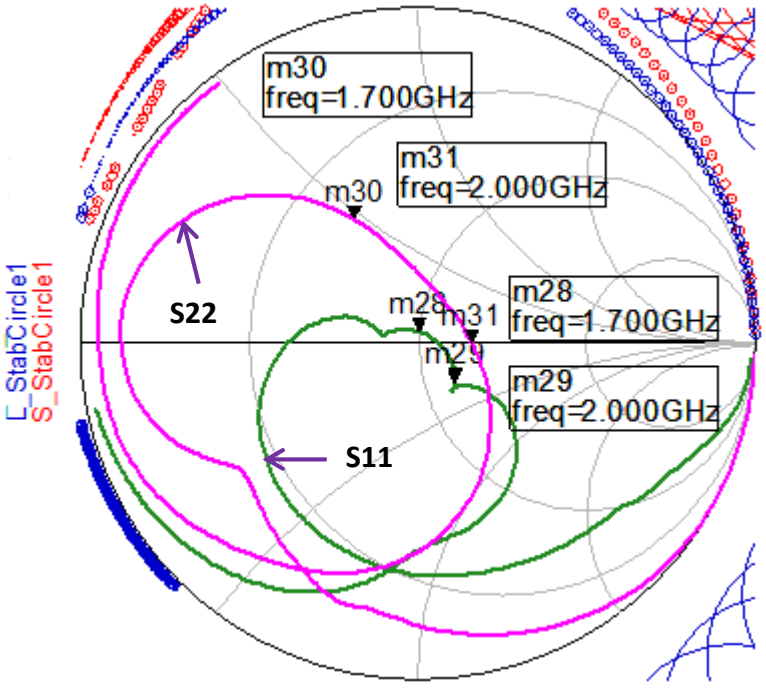


Figure 6.6: Source and load stability circles

6.2.2 Large Signal Measurement Results

Figure 6.7 illustrates the power gain plot across output power for the three frequencies which covers LTE band 1, 2, 3, 4, 10, 33, 34, 35, 36, 37 and 39. It can be seen that the maximum output power of the PA is 32dBm across frequency.

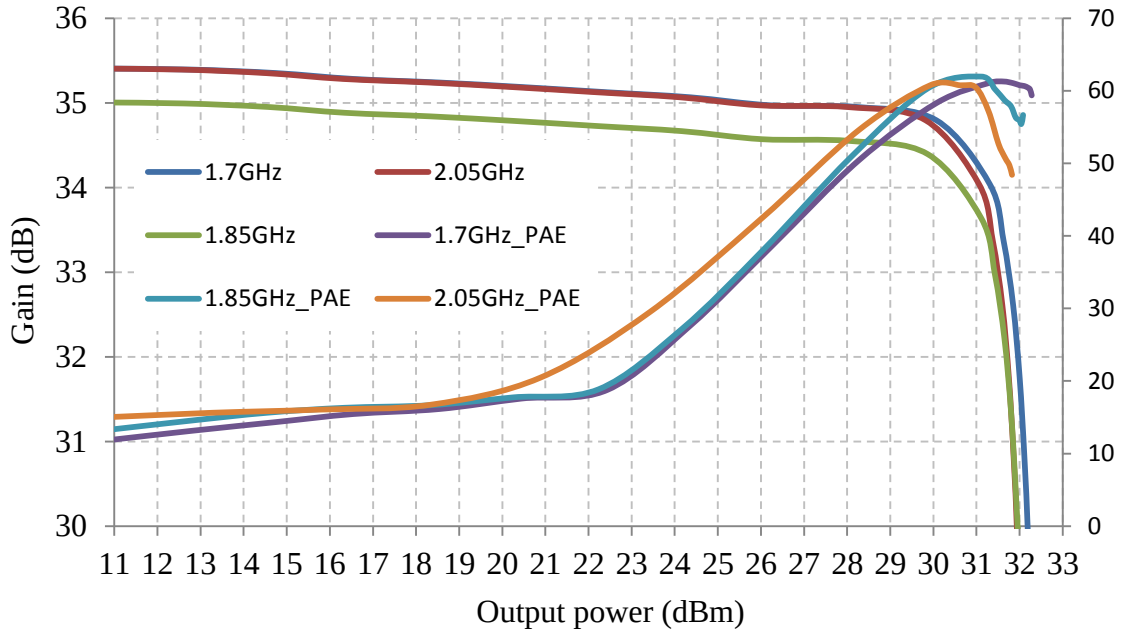


Figure 6.7: Power gain plot across output power

For LTE operation, the designed PA is tested with a 16-QAM modulation signal which has 20MHz channel bandwidth. The PAPR of the signal is 7.88dB (at 0.001%), as illustrated in Figure 6.8. The resulting ACLR and PAE plot is shown in Figure 6.9. With a supply voltage of 3.3V, PA is capable to deliver PAE of more than 40% from 1.7GHz to 2.05GHz at output power of 28dBm, with a maximum corresponding ACLR reading out to -30dBc which meets the specification for ACLR as per stated in the 3GPP specifications (3GPP TS 36.101), release 10.5 (2012). The higher ACLR at lower output power can be treated as a

mild setback due to injection of a distorted RF input signal to the input of the PA. Nevertheless, the ACLR at this power level is still below the specification.

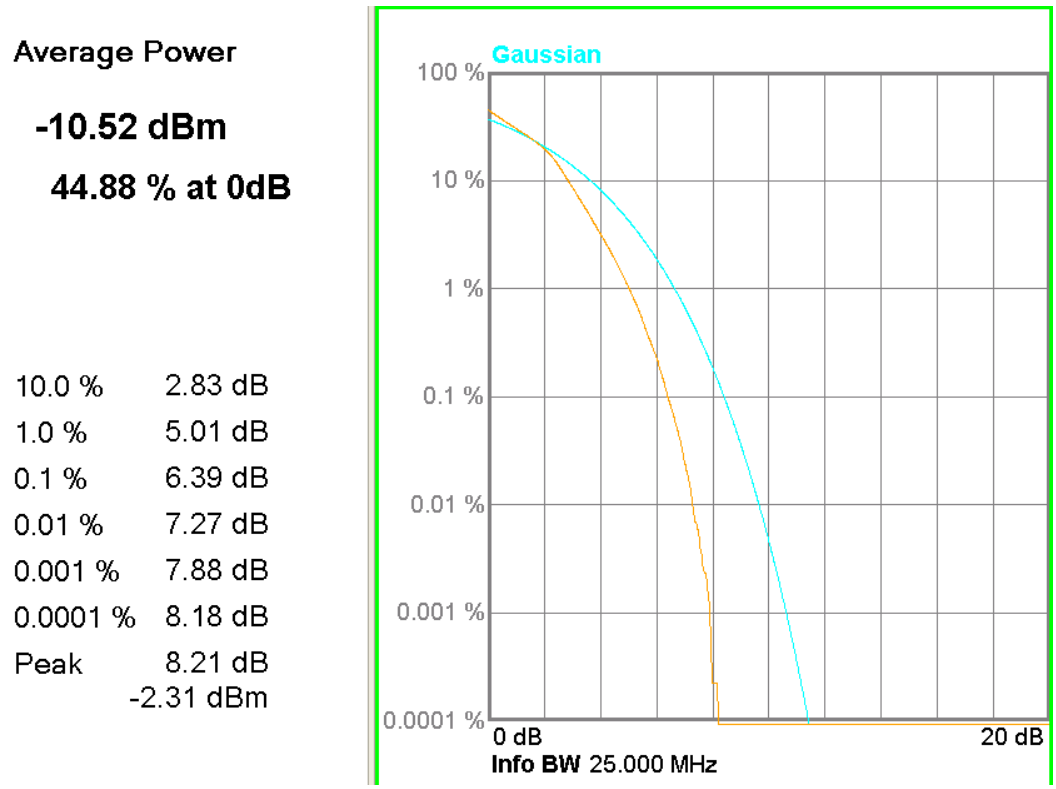


Figure 6.8: CCDF curve of the 20MHz 16QAM LTE signal, which uses SC-FDMA multicarrier modulation scheme. At 0.001% the PAPR is 7.88dB

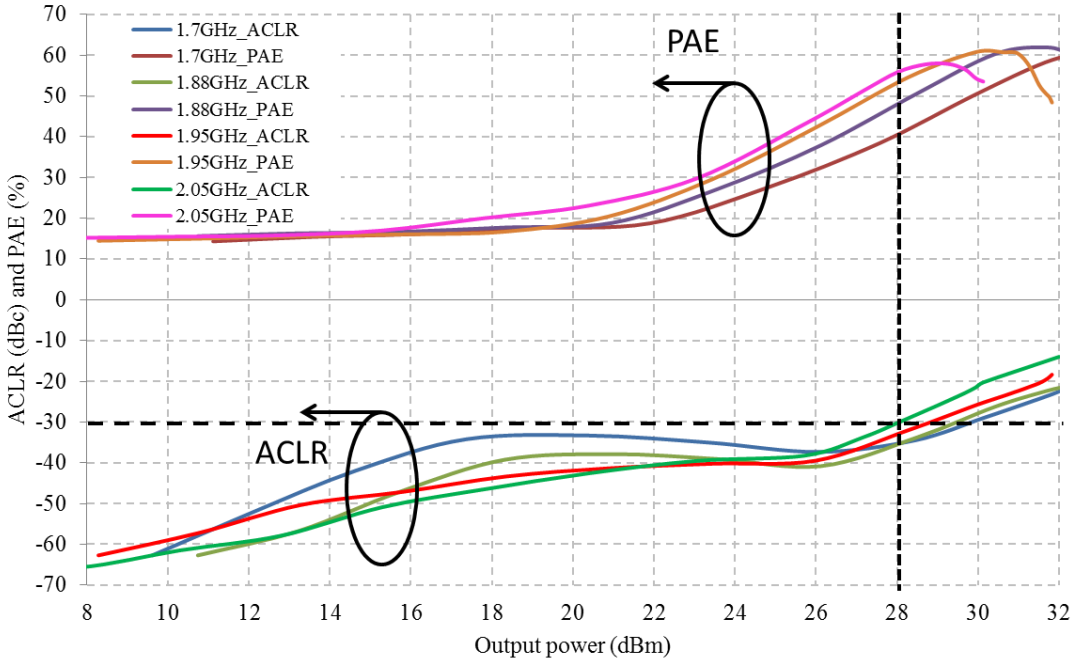
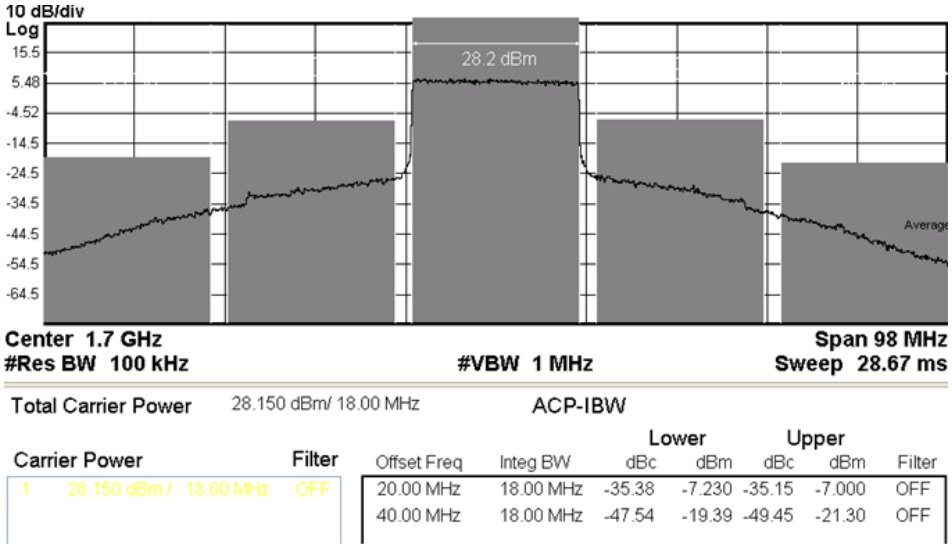
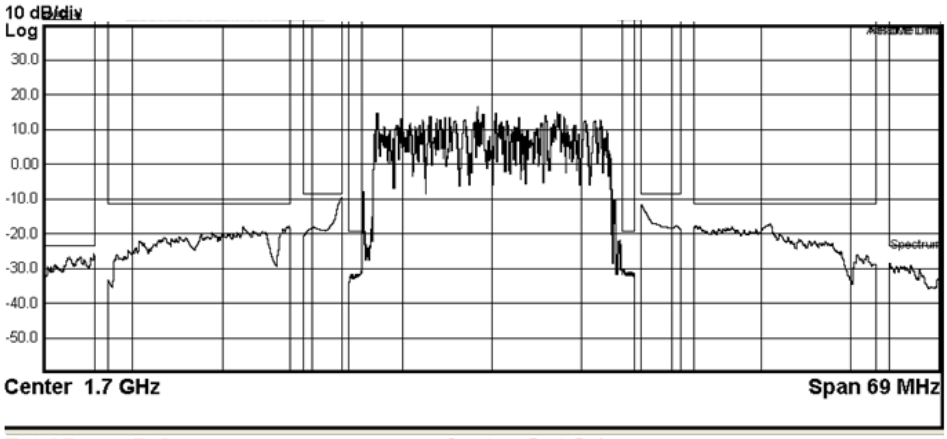


Figure 6.9: ACLR and PAE performances of the linearized PA from 1.7GHz to 2.05GHz

In Figure 6.10, the ACLR spectrum and spectral mask at the maximum linear output power of 28dBm is illustrated. The measurement result shows that the linearized PA meets the ACLR specifications of -30dBc and within the regulated spectral mask.



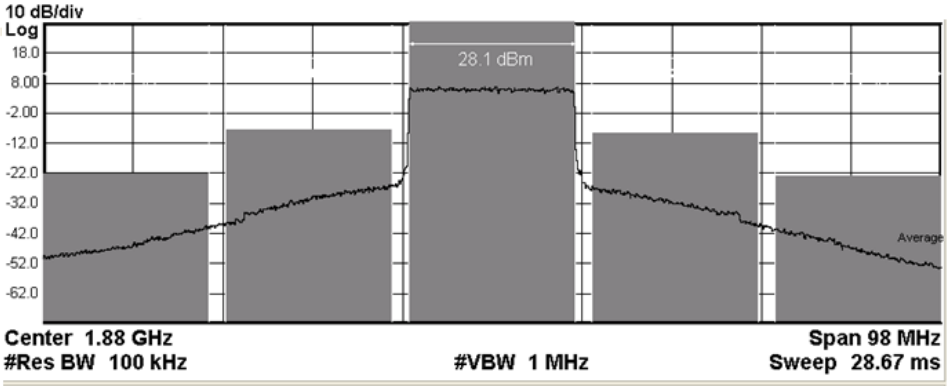
(a)



Total Power Ref 28.20 dBm / 18 MHz Spectrum Peak Ref

Start Freq	Stop Freq	Integ BW	dBm	Lower ΔLim(dB)	Lower Freq (Hz)	<- Peak -> dBm	Upper ΔLim(dB)	Upper Freq (Hz)
15.00 kHz	985.0 kHz	30.00 kHz	-30.78	(-11.28)	-94.18 k	-30.20	(-10.70)	39.74 k
1.500 MHz	4.500 MHz	1.020 MHz	-9.47	(-0.97)	-1.500 M	-11.69	(-3.19)	1.500 M
5.500 MHz	19.50 MHz	1.000 MHz	-17.89	(-6.39)	-5.567 M	-17.28	(-5.78)	11.40 M
20.50 MHz	24.50 MHz	1.000 MHz	-25.83	(-2.33)	-20.53 M	-28.47	(-4.97)	20.53 M
25.00 MHz	30.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---
30.00 MHz	40.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---

(b)

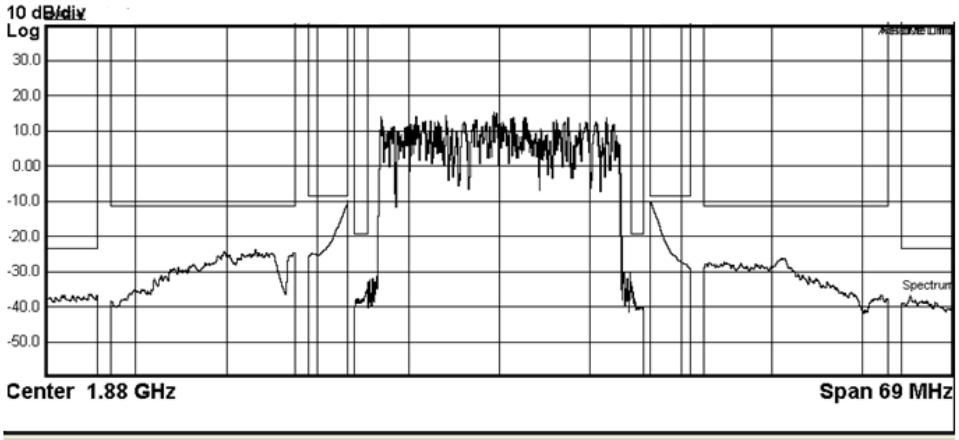


Total Carrier Power 28.118 dBm/ 18.00 MHz ACP-IBW

Carrier Power			Filter
1	28.118 dBm /	18.00 MHz	OFF

Offset Freq	Integ BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm	Filter
20.00 MHz	18.00 MHz	-35.91	-7.787	-36.80	-8.681	OFF
40.00 MHz	18.00 MHz	-50.46	-22.34	-51.39	-23.28	OFF

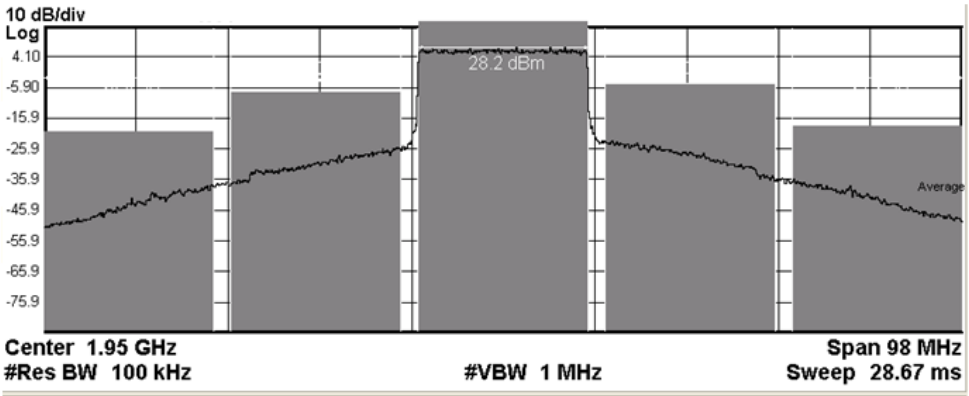
(c)



Total Power Ref 28.21 dBm / 18 MHz Spectrum Peak Ref

Start Freq	Stop Freq	Integ BW	dBm	Lower ΔLim(dB)	Lower Freq (Hz)	<- Peak -> dBm	Upper ΔLim(dB)	Upper Freq (Hz)
15.00 kHz	985.0 kHz	30.00 kHz	-33.79	(-14.29)	-19.95 k	-34.42	(-14.92)	24.90 k
1.500 MHz	4.500 MHz	1.020 MHz	-9.95	(-1.45)	-1.500 M	-10.32	(-1.82)	1.500 M
5.500 MHz	19.50 MHz	1.000 MHz	-23.87	(-12.37)	-8.470 M	-26.32	(-14.82)	11.68 M
20.50 MHz	24.50 MHz	1.000 MHz	-36.51	(-13.01)	-21.09 M	-36.92	(-13.42)	21.19 M
25.00 MHz	30.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---
30.00 MHz	40.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---

(d)

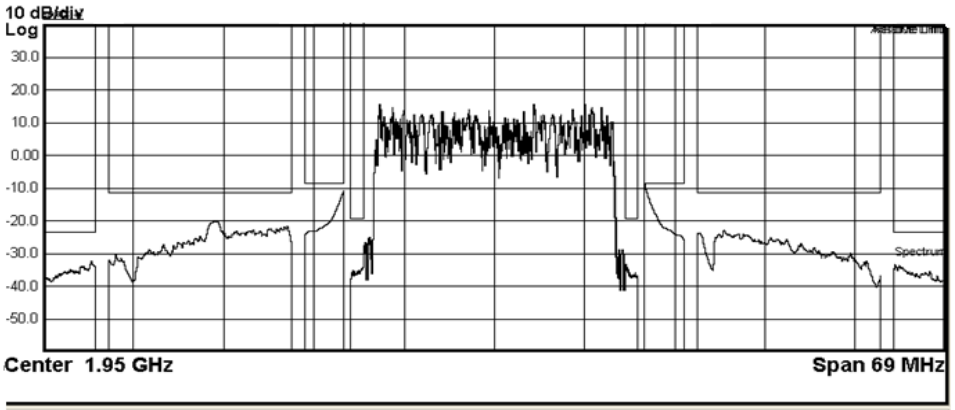


Total Carrier Power 28.199 dBm/ 18.00 MHz ACP-IBW

Carrier Power			Filter
1	28.199 dBm /	18.00 MHz	OFF

Offset Freq	Integ BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm	Filter
20.00 MHz	18.00 MHz	-35.81	-7.607	-33.23	-5.034	OFF
40.00 MHz	18.00 MHz	-48.82	-20.62	-47.06	-18.86	OFF

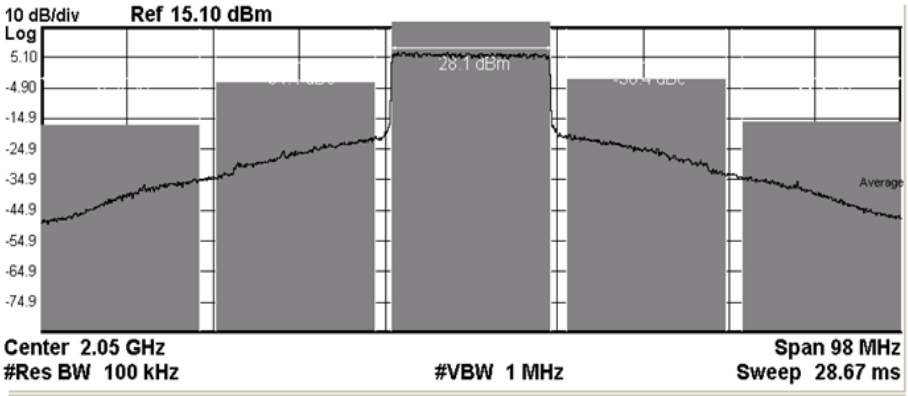
(e)



Total Power Ref 28.02 dBm / 18 MHz Spectrum Peak Ref

Start Freq	Stop Freq	Integ BW	dBm	Lower ΔLim(dB)	Freq (Hz)	<- Peak -> dBm	Upper ΔLim(dB)	Freq (Hz)
15.00 kHz	985.0 kHz	30.00 kHz	-33.08	(-13.58)	-19.95 k	-33.36	(-13.86)	24.90 k
1.500 MHz	4.500 MHz	1.020 MHz	-10.91	(-2.41)	-1.500 M	-8.79	(-0.29)	1.500 M
5.500 MHz	19.50 MHz	1.000 MHz	-20.31	(-8.81)	-11.24 M	-22.91	(-11.41)	7.565 M
20.50 MHz	24.50 MHz	1.000 MHz	-32.24	(-8.74)	-20.78 M	-33.46	(-9.96)	20.64 M
25.00 MHz	30.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---
30.00 MHz	40.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---

(f)

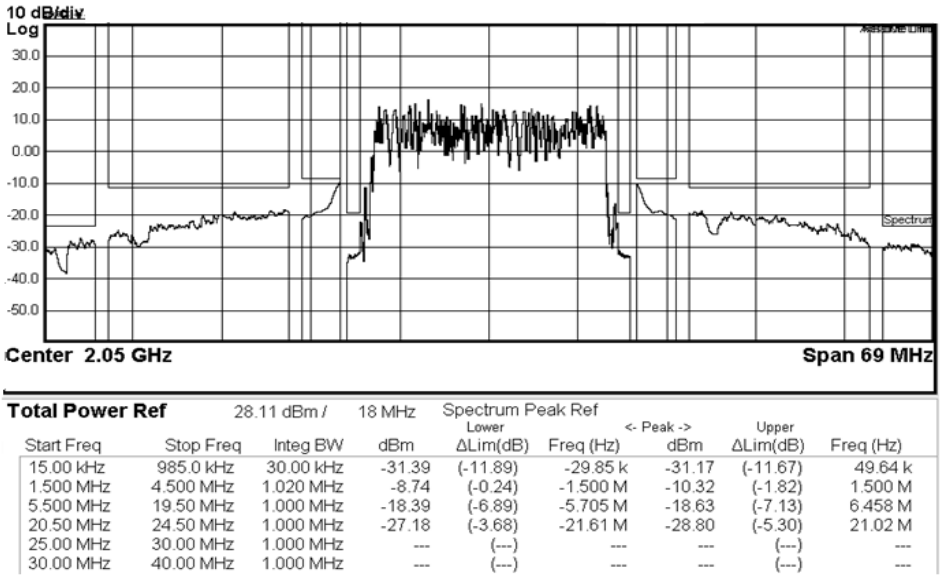


Total Carrier Power 28.064 dBm/ 18.00 MHz ACP-IBW

Carrier Power			Filter
1	28.064 dBm /	18.00 MHz	OFF

Offset Freq	Integ BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm	Filter
20.00 MHz	18.00 MHz	-31.37	-3.302	-30.39	-2.324	OFF
40.00 MHz	18.00 MHz	-45.23	-17.16	-44.39	-16.32	OFF

(g)



Total Power Ref 28.11 dBm / 18 MHz Spectrum Peak Ref

				Lower		<- Peak ->	Upper	
Start Freq	Stop Freq	Integ BW	dBm	ΔLim(dB)	Freq (Hz)	dBm	ΔLim(dB)	Freq (Hz)
15.00 kHz	985.0 kHz	30.00 kHz	-31.39	(-11.89)	-29.85 k	-31.17	(-11.67)	49.64 k
1.500 MHz	4.500 MHz	1.020 MHz	-8.74	(-0.24)	-1.500 M	-10.32	(-1.82)	1.500 M
5.500 MHz	19.50 MHz	1.000 MHz	-18.39	(-6.89)	-5.705 M	-18.63	(-7.13)	6.458 M
20.50 MHz	24.50 MHz	1.000 MHz	-27.18	(-3.68)	-21.61 M	-28.80	(-5.30)	21.02 M
25.00 MHz	30.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---
30.00 MHz	40.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---

(h)

Figure 6.10: (a) – (h) ACLR and spectral mask at output power of 28dBm from 1.71GHz to 2.05GHz which are within the specifications

Figure 6.11 depicts the EVM plot. At the maximum linear output power of 28dBm, the EVM achieved is below the specification of 4% across the operating band.

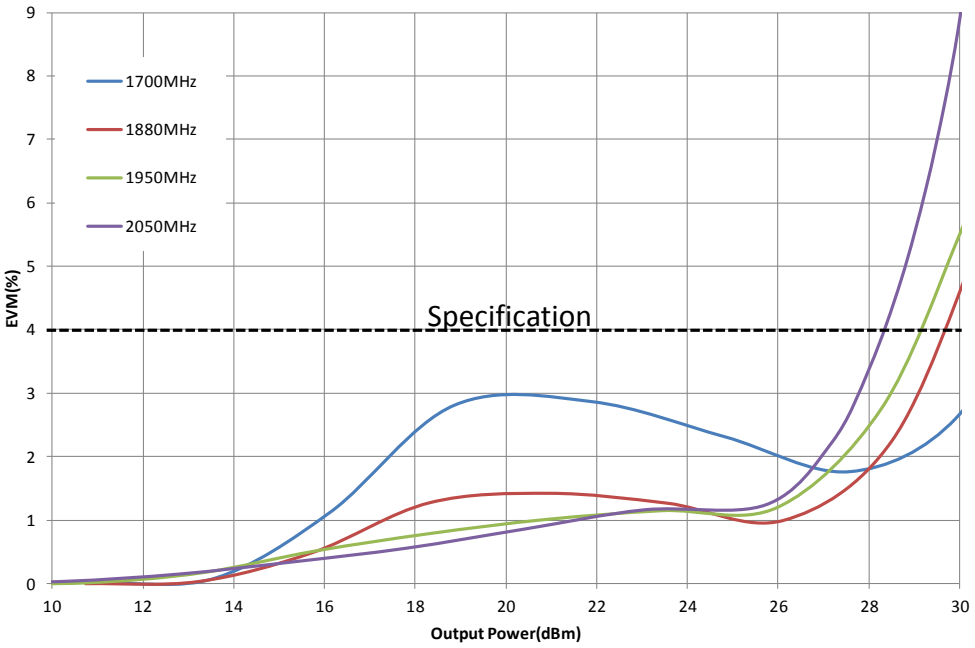
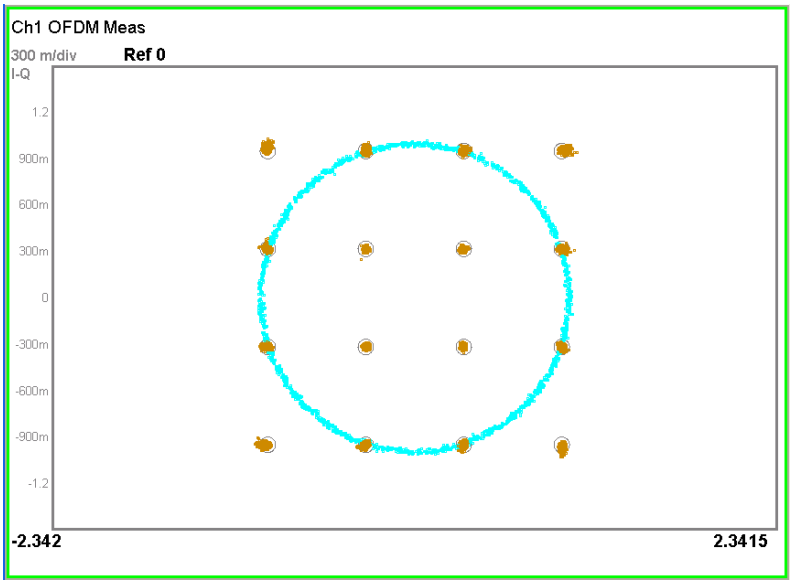
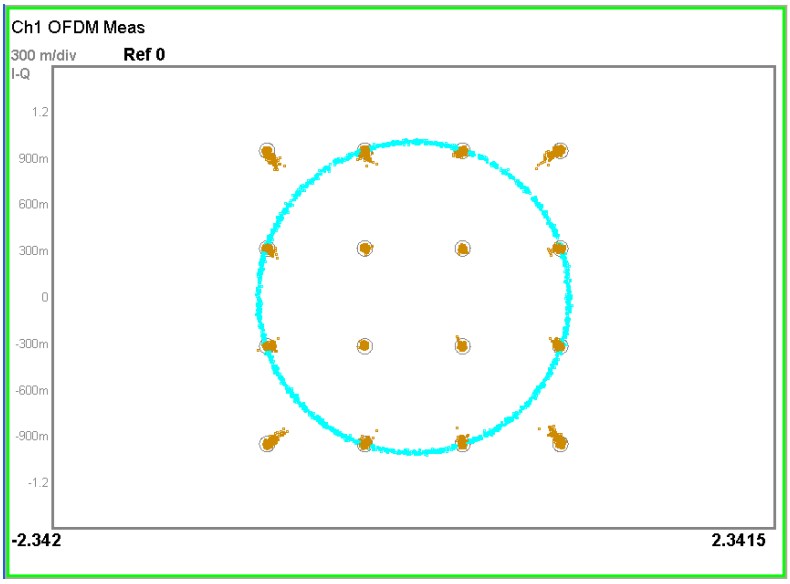


Figure 6.11: EVM plot of the linearized PA. The input signal is LTE 20MHz 16QAM

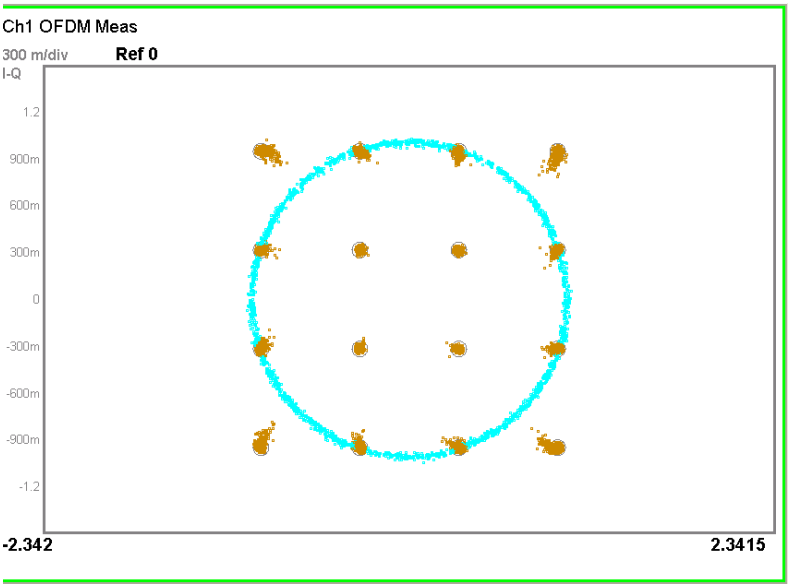
In relation to Figure 6.11, the plot of Figure 6.12 gives the corresponding constellation points at 28dBm of output power confirming the EVM performances.



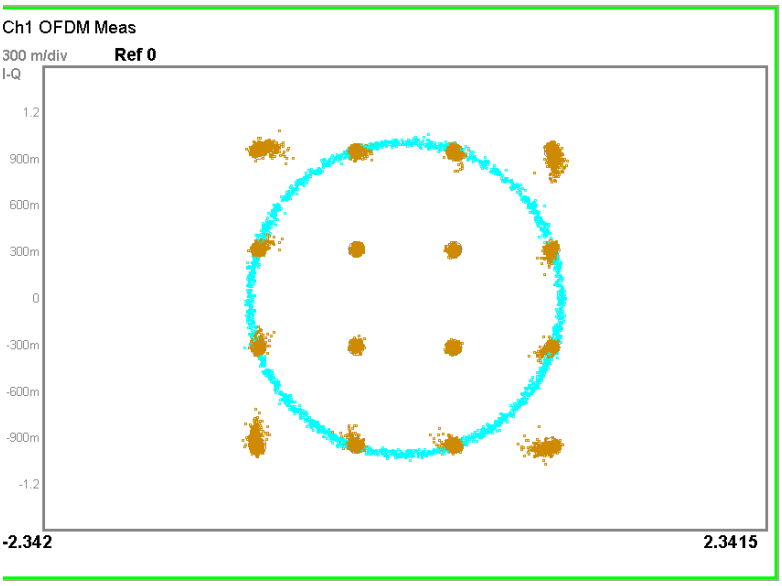
(a) 1.7GHz



(b) 1.88GHz



(c) 1.95GHz



(d) 2.05GHz

Figure 6.12: (a) – (d) EVM constellation diagram at output power of 28dBm from 1.71GHz to 2.05GHz which are within the specifications

Table 6.1 tabulates the proposed PA's measured performance summary.

Table 6.1: Performance summary of the PA

Properties	Results
Technology	2um InGaP/GaAs HBT
Die size	950um x 900um
Package size	3mm x 3mm
Supply voltage	3.3V
Frequency	1.71GHz-2.05GHz
Mode	LTE
LTE Band	1,2,3,4,9,10,33,34,35,36,37,39
Channel BW	20MHz
Max Linear output	28dBm
EVM (16-QAM)	1.74% -3.38% at 28dBm
PAE	40.5%-55.8%
Gain	34.6dB-35.8dB
S11	< -15dB
S22	< -10dB
Stability	Unconditionally Stable

Table 6.2: Performance comparison of published LTE power amplifiers

Work	Operating Freq [GHz]	LTE Channel Bandwidth [MHz]	Supply Voltage [V]	Gain [dB]	Maximum Linear Output Power [dBm]	PAE [%]	Chip Size [mm^2]
(Choi, Kim, Kang, & Kim, 2011)	2.5	10	3.3	24.8	25.8	31.6	2.6x1.7
(Hassan, Larson, Leung, Kimball, & Asbeck, 2012)	2.5	20	6.0	29.0	30.0	45.0	1x1.6
(Li, Lopez, Wu, Wu, & Lie, 2011)	2.4	5	4.2	16.0	24.3	42.0	1.1x1.5
(Kim, Kwak, & Lee, 2011)	0.84	10	3.4	27.2	27.0	34.5	1.7x1.7
(Francois & Reyneart, 2012)	0.93	10	2.0	28	25.1	15.0	1.8x1.85
(Kang, et al., 2010)	1.7 - 2	10	3.4	26.8	28.0	33.3 - 39	-
This work	1.7-2.05	20	3.3	35.8	28.0	40.5-55.8	0.95x0.9

In Table 6.2, recent work on envelope tracking methodology by (Hassan, Larson, Leung, Kimball, & Asbeck, 2012) and (Kang, et al., 2010) indeed has improve the PAE of the LTE PA. Furthermore, (Kang, et al., 2010) has achieved more than 30% PAE for 300MHz bandwidth. Both technique needs the additional CMOS chip besides the GaAs HBT PA to achieve the reported performance. An attempt by (Francois & Reyneart, 2012) is a great start to design LTE PA with CMOS process. However, work still need to be done to improve the PAE.

On the other hand, the proposed architecture in this research able to deliver more than 40% PAE for bandwidth of 350MHz. This is achieved with integrating a wideband efficiency PA (Class-J) and the linearization scheme (APD) in a single chip. Furthermore, the performance is achieved with high gain of more than 34dB for 350MHz bandwidth. The comparison data shows that the designed architecture can be well implemented in the handset's transmitter without much constraint in terms of performance and space on the phone board.

CHAPTER 7. CONCLUSION AND FUTURE WORKS

7.1 Conclusion

In this work, the design of a multi-band LTE power amplifier has been presented. The design integrates two distinct techniques which are the class-J power amplifier to improve backed-off output power efficiency and analog pre-distorter linearization scheme which ensure PA meets the linear transmission specifications respectively.

In order to meet the wideband performance, the design of a power cell is highlighted in Chapter 3. The optimum power cell size followed by the integrating ballasting concept is proven essential through this chapter. As a result, a novel ballasting concept which does not serve a trade-off for linearity and efficiency is successfully designed and implemented. In a nutshell, the foundation of the power amplifier building is strengthen before moving to the next level. Also, importance is given in choosing an optimum conduction angle for the power amplifier. Through Fourier analysis, an optimum operating point in the appreciation of the linearity and efficiency is defined. This operating point was verified through bias sweep experiment analysis. On the other hand, an appropriate biasing circuit to bias up the respective power cells has been reviewed in. The biasing circuits is constructed in an effort to make sure it does not impact the linearity of the PA.

Chapter 4 demonstrates the design methodology of class-J power amplifier. The mathematical analysis concludes the need of a reactive second harmonic termination to amend the voltage component of the PA to boost up its efficiency. Load pull simulation is

executed in order to determine the optimum fundamental and second harmonic output impedances. This is followed by the design of the desired output matching network which delivers more than 40% power added efficiency from 1.7GHz to 2.0GHz at backed off output power of 28dBm. The highest efficiency is at 2.05GHz which reads to 55.8%.

In Chapter 5, a novel analog pre-distorter linearization scheme is designed to meet the linearity specification from 1.7GHz to 2.05GHz. The insight of this design is to execute the amplitude and phase linearization through two sub-circuits which ensures wideband operation. Furthermore, these circuits are implemented as an integrating part of the PA itself.

The designed PA consists of a 950µm x 900µm die mounted on a 3mm x 3mm package is capable to operate linearly from 1.7GHz to 2.05GHz which covers LTE band 1,2,3,4,9,10,33,34,35,36,37 and 39. The PAE ranges from 40.5% to 55.8%. The size and performance of the PA places it as the right choice for handset applications.

7.2 Future Works

The successful implementation of the class-J power amplifier with integrated analog pre-distorter linearizer in this work increases the desire to further improve the linearity and efficiency to cater for the increasing data rate requirement. This opens the door for future works. The suggestions are as follows:

a) Improve the efficiency of the APD linearized class-J PA with integrated envelope tracking method.
b) Improving the linearity of the wideband efficiency class-J PA with digital pre-distortion linearization (DPD). Through this method, the class-J PA can be used for base station application which has more stringent linearity specifications.
c) Integrating the APD linearization technique with other high efficiency topology such as Doherty power amplifier.
d) To explore all the above mentioned techniques with CMOS process which will benefit in the context of cost.

REFERENCES

3GPP TS 36.101 version 9.4.0 Release 9. (2010). Retrieved from ETSI: http://www.etsi.org

Akter, R., Islam, M.-R., & Song, J.-B. (2010). PAPR in 3rd Generation Partnership Project Long Term Evolution: An Overview to Find the Impact. *IETE Technical Review*, 493-502.

Amon, C. (4 March, 2011). LTE: The Road Ahead. *EE Times*.

Aref, A.-F., Askar, A., Nafe, A., Tarar, M., & Negra, R. (2012). Efficient Amplification of Signals with High PAPR using a Novel Multilevel LINC Transmitter Architecture. *7th European Microwave Integrated Circuit Conference* (pp. 655-658). Amsterdam: IEEE.

Bahl, I. (2003). *Lumped Elements for RF and Microwave Circuits.* Norwood: Artech House.

Bahl, I. (2009). *Fundamentals of RF and Microwave Transistor Amplifiers.* New Jersey: Wiley.

Bayraktaroglu, B., & Salib, M. (1997). Unconditional Thermally Stable Cascode GaAs HBTs for Microwave Applications. *IEEE Microwave Guided Wave Letters*, 187-189.

Bulja, S., & Syahkal, D.-M. (2009). Combined Low Frequency and Third Harmonic Injection in Power Amplifier Linearization. *IEEE Microwave and Wireless Components Letters*, 584-586.

Carvalho, N., & Pedro, C. (1999). Gain Compression or Expansion, Distortion and Other Large Signal Power Amplifier Related Phenomena. *Telecommunication Conference* (pp. 1-4). Sesembra: University De Aveiro.

Carvalho, N., & Pedro, J.-C. (1999). Compact Formulas to Relate ACPR and NPR to Two Tone IMR and IP3. *Microwave Journal*, 70-75.

Cha, J., Yi, J., Kim, J., & Kim, B. (2004). Optimum Design of a Predistortion RF Power Amplifier for Multicarrier WCDMA Applications. *IEEE Transactions on Microwave Theory and Techniques*, 655-663.

Chen, C.-T., Li, C.-J., Horng, T.-S., Jau, J.-K., & Li, J.-Y. (2009). Design and Linearization of Class-E Power Amplifier for Nonconstant Envelope Modulation. *IEEE Transaction on Microwave Theory and Techniques*, 957-964.

Cho, Y., Kang, D., Kim, J., Kim, D., Park, B., & Kim, B. (2013). A Dual Power Mode Multi-band Power Amplifier with Envelope Tracking for Handset Applications. *IEEE Transactions on Microwave Theory and Techniques*, 1608-1619.

Choi, J., Kim, D., Kang, D., & Kim, B. (2009). A Polar Transmitter with CMOS Programmable Hysteretic Controlled Hybrid Switching Supply Modulator for Multi-Standard Applications. *IEEE Transactions on Microwave Theory and Techniques*, 1675-1686.

Choi, J., Kim, D., Kang, D., & Kim, B. (2011). A New Power Management IC Architecture for Envelope Tracking Power Amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 1796-1802.

Chu, W., Bakkaloglu, B., & Kiaei, S. (2008). A 10MHz Bandwidth 2mV-Ripple PA-Supply Regulator for CDMA Transmitters. *IEEE International Solid Circuit Conference Digest Technical Papers*, 448-449.

Colantonio, P., Giannini, F., & Limiti, E. (2009). *High Efficiency RF and Microwave Solid State Power Amplifiers.* West Sussex: John Wiley.

Cripps, S. (2006). *Advanced RF Power Amplifier Techniques for Modern Wireless and Microwave Systems.* Chard: Hywave Associates.

Cripps, S. (2006). *RF Power Amplifiers for Wireless Communications.* Norwood: Artech House.

Cripps, S. (2012). Amplifier Classes, A to S. In J. Walker, *Handbook of RF and Microwave Power Amplifiers* (pp. 159-161). Cambridge: Cambridge University Press.

Deng, J., Gudem, P.-S., Larson, L.-E., & Asbeck, P.-M. (2005). A High Average Efficiency SiGe HBT Power Amplifier for WCDMA Handset Applications. *IEEE Transactions on Microwave Theory and Techniques*, 529-537.

Deng, J., Gudem, P.-S., Larson, L.-E., Kimball, D.-F., & Asbeck, P.-M. (2006). A SiGe PA with Dual Dynamic Bias Control and Memoryless Digital Predistortion for WCDMA Handset Applications. *IEEE Journal of Solid State Circuits*, 1210-1221.

Doherty, W.-H. (1936). A New High Efficiency Power Amplifier for Modulated Waves. *Bell System Technical Journal,The*, 469-475.

Dong, Y., Zhang, W.-R., Jun, Q.-J., Pan, G., & Ying, X. (2006). A Simple Method to Optimize the Ballasting Resistor of RF Power HBT. *IEEE International Symposium on Antenna Propagation and EM Theory* (pp. 1-4). Guilin: IEEE.

Francois, B., & Reyneart, P. (2012). A Fully Integrated Watt Level Linear 900MHZ CMOS RF Power Amplifier for LTE Applications. *IEEE Transactions on Microwave Theory and Techniques*, 1878-1885.

Ganesan, S. (1993). *GaAs/AlGaAs HBT Device Modeling and Implementation as a High Power Device in Broadband Microwave Circuits.* Ohio: Ohio University.

Gilmore, R., & Besser, L. (2003). *Practical RF Circuit Design for Modern Wireless Systems.* Norwood: Artech House.

Gonzalez, G. (1997). *Microwave Transistor Amplifiers.* New Jersey: Prentice Hall.

Gray, P., Hurst, P., Lewis, S., & Meyer, R. (2005). *Analysis and Design of Analog Integrated Circuits.* New York: Wiley.

Han, K., & Kim, B. (2008). A Parallel Power Amplifier with a Novel Mode Switching Control. *IEEE Microwave and Wireless Components Letters*, 200-202.

Hassan, M., Larson, L.-E., Leung, V.-W., Kimball, D.-F., & Asbeck, P.-M. (2012). A Wideband CMOS/GaAs HBT Envelope Tracking Power Amplifier for 4G LTE Mobile Terminal Applications. *IEEE Transactions on Microwave Theory and Techniques*, 1321-1330.

Hau, G., Nishimura, T.-B., & Iwata, N. (2001). A Highly Efficient Linearized Wide-Band CDMA Handset Power Amplifier based on Predistortion Under Various Bias Conditions. *IEEE Transactions on Microwave Theory and Techniques*, 1194-1201.

Heinrich, W., Wentzel, A., & Melaini, C. (2010). Advanced Switch-Mode Concepts using GAN: The Class-S Amplifier. *Microwave Radar and Wireless Communications (MIKON)* (pp. 1-6). Lithuania: IEEE.

Huang, J., Liao, Y., & Chen, Z. (2010). A dual mode GaAs HBT Power Amplifier for LTE Applications. *IEEE International Conference on Solid State and Integrated Circuit Technology Proceedings* (pp. 722-724). Shanghai: IEEE.

Iwamoto, M., Williams, A., Chen, P.-F., Metzger, A.-G., Larson, L.-E., & Asbeck, P. (2001). An Extended Doherty Amplifier with High Efficiency Over A Wide Power Range. *IEEE Transactions on Microwave Theory and Techniques*, 2472-2479.

Jang, J., Kan, E., Arnborg, T., Johansson, T., & Dutton, R. (1998). Characterization of RF Power BJT and Improvement of Thermal Stability with Nonlinear Base Ballasting. *IEEE Solid State Circuit Journal*, 1428-1432.

Jeong, J., Kimball, D.-F., Kwak, M., Hsia, C., Draxler, P., & Asbeck, P.-M. (2009). Wideband Envelope Tracking Power Amplifiers with Reduced Bandwidth Power Supply Waveforms and Adaptive Digital Predistortion Techniques. *IEEE Transactions on Microwave Theory and Techniques*, 3307-3314.

Kahn, L.-R. (1952). Single Sideband Transmission by Envelope Elimination and Restoration. *IRE Proceedings*, 803-806.

Kang, D., Choi, J., Yu, K., Min, K., Min, M., Jun, M., . . . Kim, B. (2009). Input Power Dividing of Doherty Power Amplifiers for Handset Applications. *IEEE MTT-S International Microwave Symposium* (pp. 421-424). Boston: IEEE.

Kang, D., Kim, D., Cho, Y., Park, B., Kim, J., & Kim, B. (2011). Design of Bandwidth Enhanced Doherty Power Amplifiers for Handset Applications. *IEEE Transactions on Microwave Theory and Techniques*, 3474-3483.

Kang, D., Kim, D., Choi, J., Kim, J., Cho, Y., & Kim, B. (2010). A Multimode/Multiband Power Amplifier with a Boosted Supply Modulator for Multi-Standard Applications. *IEEE Transactions on Microwave Theory and Techniques*, 2598-2608.

Kang, D., Yu, D., Min, K., Choi, J., Jun, M., Kim, D., & Kim, B. (2008). Class-AB/F Doherty Power Amplifiers. *Proceedings of 38th European Microwave Conference* (pp. 230-233). Amsterdam: IEEE.

Kang, D., Yu, D., Min, K., Han, K., Choi, J., Kim, D., . . . Kim, B. (2008). A Highly Efficient and Linear Class-AB/F Power Amplifier for Multimode Operation. *IEEE Transactions on Microwave Theory and Techniques*, 77-87.

Kang, S., Park, U., Lee, K., & Hong, S. (2003). Adaptive Feedforward Amplifier using Digital Contoller. *57th IEEE Semianual Vehicular Technology Conference* (pp. 2076-2079). South Korea: IEEE.

Kato, T., Yamaguchi, K., & Kuriyama, Y. (2006). A Doherty Power Amplifier Module for Mobile Terminals with Variable Linearity Function. *Proceedings of Asia-Pacific Microwave Conference* (pp. 1881-1884). Yokohama: IEEE.

Katz, A. (2001). Linearization: Reducing Distortion in Power Amplifiers. *IEEE Microwave Magazine*, 37-49.

Kim, B., Kwak, C., & Lee, J. (2011). A Dual Mode Power Amplifier with on Chip Switch Bias Control Circuits for LTE Handsets. *IEEE Transactions on Circuits and Systems*, 857-861.

Kim, B., Kwak, C., & Lee, J. (2011). A Dual Mode Power Amplifier with on Chip Switch Bias Control Circuits for LTE Handsets. *IEEE Transactions on Circuits and Systems*, 857-861.

Kim, I., Cha, J., Hong, S., Woo, Y., Kim, J., & Kim, B. (2006). Predistortion Power Amplifier for Base Station using a Feedforward Loop Linearizer. *36th European Microwave Conference* (pp. 141-144). Manchester: IEEE.

Kim, J., Son, S., Jee, S., Kim, S., & Kim, B. (2013). Optimization of Envelope Tracking Power Amplifier for Base Station Applications. *IEEE Transactions on Microwave Theory and Techniques*, 1620-1627.

Kim, W., Kang, S., Lee, K., Chung, M., & Kang, J. (2002). Analysis of Nonlinear Behavior of Powr HBTs. *IEEE Transactions on Microwave Theory and Techniques*, 1714-1722.

Kousai, S., Onikuza, K., Yamaguchi, T., Kuriyama, Y., & Nagaoka, M. (2012). A 28.3mW PA Closed Loop for Linearity and Efficiency Improvement Integrated in a 27.12dBm WCDMA CMOS Power Amplifier. *IEEE International Solid State Circuits Conference Digest Technical Papers*, 84-86.

Landin, P.-N., Fritzin, J., Moer, W.-V., Isaksson, M., & Alvanpour, A. (2012). Modeling and Digital Predistortion of Class D Outphasing RF Power Amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 1907-1915.

Legarda, J., Presa, J., E, H., Solar, H., J, M., & J, P. (2005). An Adaptive Feedforward Amplifier under Maximum Output Control Method for UMTS Downlink Transmitters. *IEEE Transactions on Microwave Theory and Techniques*, 2481-2486.

Li, Y., Lopez, J., Wu, P.-H. H., Wu, R., & Lie, D.-Y. (2011). A SiGe Envelope Tracking Power Amplifier with an Integrated CMOS Envelope Modulator for Mobile WiMAX/3GPP LTE Transmitters. *IEEE Transactions on Microwave Theory and Techniques*, 2525-2536.

Liou, J.-J., Liou, L.-L., & Huang, C.-I. (1994). Analytical Model for the AlGaAs/GaAs Multiemitter Finger HBT Including Self Heating and Thermal Coupling Effects. *IET Journal*, 469-475.

Liou, L.-L., Jenkins, T., & Huang, C.-I. (1996). Effect of Base Potential Distribution on Thermal Runaway and the Power Limitation of the Heterojunction Bipolar Transistor with CIrcular Dot Geometry. *Electron Devices Meeting* (pp. 49-52). Ohio: IEEE.

Liu, W., Khatibzadeh, A., Sweder, J., & Chau, H.-F. (1996). The Use of Base Ballasting to Prevent the Collapse of Current Gain in AlGaAs/GaAs Heterojunction Bipolar Transistors. *IEEE Electron Devices*, 245-251.

Liu, W., Nelson, S., Hill, D.-G., & Khatibzadeh, A. (1993). Current Gain Collapse in Microwave Multifinger Heterojunction Bipolar Transistors Operated at very High Power Densities. *IEEE Electron Device*, 1917-1927.

Ludwig, R., & Bretchko, P. (2000). *RF Circuit Design Theory and Applications.* New Jersey: Prentice Hall.

Maas, S. (2006). Ballasting HBTs for Wireless Power Amplifier Operation. *ARMMS Conference* (pp. 1-9). Steventon: ARMMS UK.

Maier, S., Wiegner, D., Zierdt, M., Kuebart, W., Seyfried, U., Haslach, C., . . . Quay, R. (2011). 900 MHz Pulse Width Modulated Class-S Power Amplifier with Improved Linearity. *Microwave Symposium Digest (MTT)* (pp. 1-4). Baltimore: IEEE.

Moon, J., Kim, J., & Kim, B. (2010). Investigation of a Class-J Power Amplifier with a Non-linear Cout for Optimized Operation. *IEEE Transactions on Microwave Theory and Techniques*, 2800-2811.

Moon, J., Son, J., Lee, J., & Kim, B. (2011). A Multimode/Multiband Envelope Tracking Transmitter with Broadband Saturated Amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 3463-3473.

Nam, J., & Kim, B. (2007). The Doherty Power Amplifier with On-Chip Dynamic Bias Control Circuit for Handset Application. *IEEE Transactions on Microwave Theory and Techniques*, 633-642.

Park, H.-M., Baek, D.-H. J.-I., & Hong, S. (2000). A Predistortion Linearizer Using Envelope Feedback Technique with Simplified Carrier Cancellation Scheme for Class-A and Class-AB Power Amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 898-904.

Pinon, V., Hasbani, F., Giry, A., Pache, D., & Garnier, C. (2008). A Single Chip WCDMA Envelope Reconstruction LDMOS PA with 130MHz Switched Mode Power Supply. *IEEE International Solid State Circuits Conference Digest Technical Papers*, 564-565.

Pozar, D. (2005). *Microwave Engineering.* New York: Wiley.

Raab, F.-H., Asbeck, P., Cripps, S., Kenington, P.-B., Popovic, Z.-B., Pothecary, N., . . . Sokal, N.-O. (2002). Power Amplifiers and Transmitters for RF and Microwave. *IEEE Transactions on Microwave Theory and Techniques*, 814-826.

Rana, M.-M., Islam, M.-S., & Kouzani, A.-Z. (2010). Peak to Average Power Ratio Analysis for LTE Systems. *IEEE International Conference on Communication Software and Networks* (pp. 516-520). Singapore: IEEE.

Reynaert, P., & Steyaert, M. (2005). A 1.7GHz Polar Modulated CMOS RF Power Amplifier for GSM-EDGE. *IEEE Journal of Solid State Circuits*, 2598-2608.

Rollett, J.-M. (1962). Stability and Power Gain Invariants of Linear Two Ports. *IRE Transactions on Circuit Theory*, 29-32.

Rui, M., Zhancang, W., Yang, X., & Lanfranco, S. (2012). Implementation of a Current Mode Class-S RF Power Amplifier with GaN HEMTS for LTE Advanced. *Wireless and Microwave Technology Conference (WAMICON)* (pp. 1-6). Florida: IEEE.

Rumney, M. (2009). Air Interface Concepts. In M. Rumney, *LTE and the Evolution to 4G Wireless* (pp. 11-57). China: Agilent Technologies.

Rumney, M. (2009). *LTE and the Evolution to 4G Wireless.* China: Agilent Technologies.

Rumney, M. (2009). LTE Introduction. In M. Rumney, *LTE and the Evolution to 4G Wireless* (pp. 1-7). China: Agilent Technologies.

Sahu, B., & Rincon-Mora, G.-A. (2007). A High Efficiency WCDMA RF Power Amplifier with Adaptive Dual Mode Buck-Boost Supply and Bias Current Control. *IEEE Microwave and Wireless Components Letters*, 238-240.

Shameli, A., Safarian, A., Rofougaran, A., Rofougaran, M., & DeFlaviis, F. (2008). A Two Point Modulation Technique for CMOS Power Amplifier in Polar Transmitter Architecture. *IEEE Transactions on Microwave Theory and Techniques*, 31-38.

Suzuki, Y., Ohkawara, J., & Narahashi, S. (2011). A 3.5GHz Band 140-W Class Wideband Feedforward Power Amplifier for Mobile Base Stations. *General Assembly and Scientific Symposium* (pp. 1-4). Istanbul: IEEE.

Suzuki, Y., Ohkawara, J., & Narahashi, S. (2011). A 3.5GHz Band 140-W Class Wideband Feedforward Power Amplifier for Mobile Base Stations. *General Assembly and Scientific Symposium* (pp. 1-4). Istanbul: IEEE.

Sweet, A. (1990). *MIC and MMIC Amplifier and Oscillator Circuit Design.* Norwood: Artech House.

Sweet, A. (2008). *Designing Bipolar Transistor Radio Frequency Integrated Circuits.* Norwood: Artech House.

Takahashi, K., Yamanouchi, Y., Hirayama, & Kunihiro, k. (2008). An Envelope Tracking power Amplifier Using an Adaptive Biased Envelope Amplifier for WCDMA Handsets. *Radio Frequency Integrated Circuits (RFIC) Symposium* (pp. 405-408). Atlanta: IEEE.

Thein, T.-T., Law, C.-L., & Fu, K. (2011). Frequency Domain Dynamic Thermal Analysis in GaAs HBT for Power Amplifier Applications. *Progress in Electromagnetic Research*, 71-87.

Tombak, A., Baeten, R.-J., Jorgenson, J.-D., & Dening, D.-C. (2006). Integration of a Cellular Handset Power Amplifier and a DC/DC Converter in a Silicon-On-Insulator(SOI) Technology. *Radio Frequency Integrated Circuits (RFIC) Symposium* (pp. 413-416). Atlanta: IEEE.

Tuffery, A., Deltimple, N., Leite, B., Cathelin, P., Knopik, V., & Kerherye, E. (2011). A 27.5dBm Linear Reconfigurable CMOS Power Amplifier for 3GPP LTE Applications. *NEWCAS* (pp. 221-224). France: IEEE.

Tuffy, T., Zhu, A., & Brazil, T.-J. (2011). Class-J RF Power Amplifier with Wideband Harmonic Supression. *IEEE MTT-S International* (pp. 1-4). Baltimore: IEEE.

Walsh, K., & Johnson, J. (2009). *3G/4G Multimode Cellular Front End Challenges; Impact on Power Amplifier Design.* San Jose: RFMD.

Wang, F., Kimball, D.-F., Lie, D.-Y., & Asbeck, P.-M. L.-E. (2007). A Monolithic High Efficiency 2.4GHz 20-dBm SiGe BiCMOS Envelope Tracking OFDM Power Amplifier. *IEEE Journal of Solid State Circuits*, 1271-1281.

Wen, J.-C., & Sun, L.-L. (2006). A GaAs HBT Power Amplifier with a Newly Active Bias Linearizer for WCDMA Terminal. *8th International Conference on Solid State and Integrated Circuit Technology Proceedings* (pp. 1727-1729). Shanghai: IEEE.

Wentzel, A., Meliani, C., & Heinrich, W. (2010). RF Class-S Power Amplifiers: State of the Art Results and Potential. *Microwave Symposium Digest (MTT)* (pp. 812-815). Anaheim: IEEE.

Wright, P., Lees, J., Benedikt, J., Tasker, P.-J., & Cripps, S.-C. (2009). A Methodology for Realizing High Efficiency Class-J in Linear and Broadband Power Amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 3196-3204.

Yamanouchi, S., Aoki, Y., Kunihiro, K., Hirayama, T., Miyazaki, T., & Hida, H. (2007). Analysis and Design of a Dynamic Predistorter for WCDMA Handset Power Amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 493-503.

Yu, D., Kim, Y., Han, K., Shin, J., & Kim, B. (2006). Fully Integrated Doherty Power Amplifiers for 5GHz Wireless-LANs. *Radio Frequency Integrated Circuits (RFIC) Symposium* (pp. 177-180). San Francisco: IEEE.

Cho, Y., Kang, D., Kim, J., Moon, K., Park, B., & Kim, B. (2014). Linear Doherty Power Amplifier with an Enhanced Back-Off Efficiency Mode for Handset Applications. *IEEE Transactions on Microwave Theory and Techniques*, 567-578.

Hammi, O., Kwan, A., Bensmida, S., & Morris, K. (2014). A Digital Predistortion System with Extended Correction Bandwidth with Application to LTE-A Nonlinear Power Amplifiers . *IEEE Transactions on Circuits and Syatems*, 3487-3495.

Yang, S.-H., Chen, J.-H., & Chen, Y.-J. (2014). A 1.2V 90-nm Fully Integrated Compact CMOS Linear Power Amplifier Using the Coupled L-Shape Concentric Vortical Transformer. *IEEE Transactions on Microwave Theory and Techniques*, 2689-2699.

LIST OF PUBLICATIONS AND PAPERS PRESENTED

ISI Journals

Eswaran, U., Ramiah, H., Kanesan, J., & Reza, A.-W. (2014). Class-E GaAs HBT Power Amplifier with Passive Linearization Scheme for Mobile Wireless Communications. *Turkish Journal of Electrical Engineering and Computer Sciences,* 1210-1218.

Ramiah, H., Eswaran, U., & Kanesan, J. (2014). A High Gain and High Linearity Class-AB Power Amplifier for WCDMA Applications. *Microelectronics International*, 1-7.

Eswaran, U., Ramiah, H., & Kanesan, J. (2014). Power Amplifier Design Methodologies for Next Generation Wireless Communications. *IETE Technical Review*, 241-248.

Eswaran, U., Ramiah, H., Kanesan, J., & Reza, A.-W. (2014). Design of Wideband LTE Power Amplifier with Novel Dual Stage Linearizer for Mobile Wireless Communication. *Journal of Circuits, Systems and Computers*, 1-9.

Eswaran, U., Ramiah, H., & Kanesan, J. (2014). Class-E Power Amplifier with Novel Pre-Distortion Linearization Technique for 4G Mobile Wireless Communications. *Elektronika Ir Elektrotechnika*, 53-56.

Eswaran, U., Ramiah, H., Kanesan, J., & Reza, A.-W. (2014). Wideband LTE Power Amplifier with Integrated Novel Analog Pre-Distorter Linearizer for Mobile Wireless Communications. *Plos One*, 1-16.

Eswaran, U., Ramiah, H., & Kanesan, J. (2014). A High Efficiency 1.8W Power Amplifier for Wireless Communications. *Elektronika Ir Elektrotechnika*, (Accepted for Publications).

Conference Paper

U. Eswaran, H. Ramiah & J. Kanesan. (2013). A Novel Power Amplifier Linearization Method for Handset Applications. *International Conference on Innovative Trends in Electronic Communication and Applications (ICIECA)* (pp. 17-22). India: ASDF.

TÜBİTAK

Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2014) 22: 1210 – 1218

doi:10.3906/elk-1212-43

Class-E GaAs HBT power amplifier with passive linearization scheme for mobile wireless communications

Uthirajoo ESWARAN, Harikrishnan RAMIAH*, Jeevan KANESAN, Ahmed Wasif REZA

Department of Electrical Engineering, University of Malaya, Kuala Lumpur

Received: 07.12.2012 • **Accepted:** 01.02.2013 • **Published Online:** 15.08.2014 • **Printed:** 12.09.2014

Abstract: A linearization technique for improving the class-E power amplifier (PA)'s adjacent channel power ratio (ACPR) is proposed. The design is simulated in a 2-μm InGaP/GaAs heterojunction bipolar transistor process. The integration of a passive predistorter at the input of the PA linearizes the proposed architecture. At a 29-dBm output power, the PA's ACPR is indicated to be –51 dBc, meeting the stringent code division multiple access regulation. At this exact output power, the simulated power added efficiency is 55% with the collector voltage headroom consumption of 3.4 V. The input return loss, S11, of the PA is simulated as –12.5 dB. With an active finger print dimension of 1000 μm × 750 μm, the proposed PA is well suited for the application of mobile wireless communication.

Key words: Class-E, HBT, linearization, power amplifier

1. Introduction

In recent years, increasing demand for a higher data rate for mobile wireless communication has set an innovative milestone in the art of transmitter design. As the data rate increases, the transmitter, in particular the power amplifier (PA), needs to maintain a linear operating region, thus establishing the requirement to operate at a back-off region from maximum saturated output power [1]. This restriction imparts design challenges in maintaining high power-added efficiency (PAE) at the back-off output power level.

In an effort to improve the efficiency at the back-off output power, the preferred enhancement methods can be capsulated into 2 distinct categories, the efficiency enhancement method and linearization method [2]. These methods have gained popularity and are reported in several distinguished implementations [3–12].

Among the architecture of design concern in targeting efficiency enhancement are Doherty PA and envelope tracking PA. The Doherty PA, consisting of 2 amplifiers connected in parallel, employs the load modulation technique to enhance the efficiency at the back-off output power [3–6]. A quarter-wave transformer is used to modulate the load in improving the efficiency and third-order intermodulation distortion (IMD3) cancellation between the main and auxiliary amplifiers, paving into the linearity enhancement [7]. The implementation and integration of an on-chip quarter-wave transformer will substantially increase the die size. Alternately, a popular method in improving the efficiency of the PA is envelope tracking, where the supply voltage of the PA is modulated respective to the output power level. This enables the PA to operate at a low supply voltage at an equivalently low power level, which in turn boosts its efficiency. However, the complexity in implementation serves to be the penalty paid. Often, a hybrid technology merger of the complementary metal-oxide

*Correspondence: hrkhari@um.edu.my

A high gain and high linearity class-AB power amplifier for WCDMA applications

Harikrishnan Ramiah
Faculty of Engineering, University of Malaya, Kuala Lumpur, Malaysia

U. Eswaran
University of Malaya, Kuala Lumpur, Malaysia, and

J. Kanesan
Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia

Abstract

Purpose – The purpose of this paper is to design and realize a high gain power amplifier (PA) with low output back-off power using the InGaP/GaAs HBT process for WCDMA applications from 1.85 to 1.91 GHz.

Design/methodology/approach – A three stages cascaded PA is designed which observes a high power gain. A 100 mA of quiescent current helps the PA to operate efficiently. The final stage device dimension has been selected diligently in order to deliver a high output power. The inter-stage match between the driver and main stage has been designed to provide maximum power transfer. The output matching network is constructed to deliver a high linear output power which meets the WCDMA adjacent channel leakage ratio (ACLR) requirement of −33 dBc close to the 1 dB gain compression point.

Findings – With the cascaded topology, a maximum 31.3 dB of gain is achieved at 1.9 GHz. S11 of less than −18 dB is achieved across the operating frequency band. The maximum output power is indicated to be 32.7 dBm. An ACLR of −33 dBc is achieved at maximum linear output power of 31 dBm.

Practical implications – The designed PA is an excellent candidate to be employed in the WCDMA transmitter chain without the aid of additional driver amplifier and linearization circuits.

Originality/value – In this work, a fully integrated GaAs HBT PA has been implemented which is capable to operate linearly close to its 1 dB gain compression point.

Keywords Micro-circuit technology, Semiconductor technology

Paper type Technical paper

I. Introduction

WCDMA has proven to be a promising technique for terrestrial cellular communications (Oetting, 2007). With a 4,096 kbps spreading rate and a pulse shaping roll-off factor of 0.22, which translates to a wide bandwidth operation, adjacent channel interference has become one of the most critical issues for WCDMA integration (Lilja and Mattila, 1999a). It is expected that adjacent channel leakage ratio (ACLR) of −30 dBc would guarantee that two adjacent channel signals can coexist at the same time without interfering with each other (Lilja and Mattila, 1999b). The power amplifier (PA) needs to operate in linear region to ensure this criterion of ACLR is met. Concurrently, for mobile wireless communications, the standby and talk time is a crucial specification that needs to be given attention in the design and development of the PA. In order to maximize these parameters an enhanced power added efficiency is essential (Shinjo *et al.*, 2002; Hau *et al.*, 2005). Hence a trade-off is usually in existence between these two parameters catering towards best case solution. In recent practice, PA operates at a prescribed back-off region to maintain a strict linearity requirement (Raab *et al.*, 2002).

In this work, a PA which has a high linear output power of 31 dBm, and a corresponding PAE of 50 per cent is proposed. With this high linear output power, the PA is capable to tolerate a maximum output path loss of 7 dB from the antenna input of a WCDMA transmitter. Concurrently, it is able to operate close to its 1 dB compression point, ruling out the need to have high output back-off power from 1 dB compression point due to linearity concern. With the aid of proper impedance matching network, the severity of the trade-off between the ACLR and PAE is minimized. This paper is organized as follows: Section II explains the design methodology in the integration of the PA; Section III presents the measurement results; and the conclusion is given in Section IV.

II. Design methodology

Device size

In this work, in order to meet a 31 dBm maximum linear output power, the PA has been designed to deliver a maximum (saturation) output power of 33 dBm. The load resistance, $R_{loadopt}$ to achieve this maximum output power is defined as (Sweet, 2008):

The current issue and full text archive of this journal is available at www.emeraldinsight.com/1356-5362.htm

Microelectronics International
31/1 (2014) 1–7

[DOI 10.1108/MI-09-2012-0069]

This work was in part supported by the UMRG Grant RG082-10AET.

Power Amplifier Design Methodologies for Next Generation Wireless Communications

U. Eswaran, H. Ramiah and J. Kanesan

Department of Electrical Engineering, University of Malaya

ABSTRACT

As wireless communication standard continues to evolve accommodating the demand of high data rate operation, the design of radio frequency (RF) power amplifier (PA) becomes ever challenging. PAs are required to operate more efficiently while maintaining stringent linearity requirement. In this paper, the design concepts of the PA in addressing these challenges are reviewed. The concepts are divided into two main categories, namely the linearization technique and efficiency enhancement technique. The mandatory attempt in realizing a low-cost design is also discussed.

Keywords:
Power amplifiers, Linearization, Wireless, LTE.

1. INTRODUCTION

As the demand for higher data rate continuously increases, the transition from wideband code division multiple access (WCDMA) communication standard to 3rd generation partnership project (3GPP) long-term evolution (LTE) begins to pave through the entrance of realization. LTE employs single carrier frequency division multiple access (SC-FDMA) for uplink and orthogonal frequency division multiple access (OFDMA) for downlink, a multicarrier modulation scheme ensuring spectral efficiency [1]. This modulation scheme is subjected to high peak to average ratio (PAPR). SC-FDMA has a similar performance and complexity respective to OFDMA, in favour of lower PAPR [2]. Typically, the PAPR of SC-FDMA signal is 7 dB whereas OFDMA is 10 dB, heavily depending on the modulation scheme adapted (quadrature phase shift keying [QPSK], 16 quadrature amplitude modulation [QAM], or 64 QAM) [3]. To amplify signals with high PAPR, the power amplifier (PA) needs to operate at a backed-off output power satisfying the stringent linearity requirement, specified in terms of adjacent channel leakage ratio (ACLR) and error vector magnitude. The drawback of this conventional technique is in the degradation in PA's power added efficiency (PAE). The relationship between backed-off output power and efficiency for a multicarrier signal can be appreciated in the following equations [4]:

$$\eta_{\text{pbo-class A}} = \frac{1}{2} \cdot \frac{P_{\text{bo}}}{P_{\text{max}}} \quad (1)$$

$$\eta_{\text{pbo-class B}} = \frac{\pi}{4} \cdot \sqrt{\frac{P_{\text{bo}}}{P_{\text{max}}}} \quad (2)$$

where P_{bo} and P_{max} represent backed-off output power and maximum output power, respectively. For example, if a PA which has P_{max} of 35 dBm is transmitting LTE signal with PAPR of 7 dB, the resultant efficiency at P_{bo} of 28 dBm is 9.9% and 30% in a respective operation of class A and class B mode. These values may not be suitable for battery-operated mobile devices.

The solution to improve the PAE of LTE PA lies in two techniques, which are the efficiency enhancement technique and linearization technique. The efficiency enhancement technique mandates in improving the efficiency of a linear PA, while linearization techniques improves the linearity of an efficient non-linear PA.

This paper reviews recent research reports on WCDMA and LTE radio frequency (RF) power amplifiers. Section 2 presents the work reported in efficiency enhancement techniques. In Section 3, the research output on the linearization techniques are discussed. The process evolution in radio frequency power amplifier (RFPA) design is presented in Section 4. Finally, the conclusion is provided in Section 5.

2. EFFICIENCY ENHANCEMENT TECHNIQUES

2.1 Device Switching

Efficiency enhancement technique mandates in improving the efficiency of a linear PA, which is typically biased at class AB mode of operation. The device switching approach is a simple methodology to improve the efficiency of WCDMA PA at P_{bo}. In this technique, the size of the power cells is varied

Journal of Circuits, Systems, and Computers
Vol. 23, No. 8 (2014) 1450111 (9 pages)

DOI: 10.1142/S0218126614501114

World Scientific
www.worldscientific.com

DESIGN OF WIDEBAND LTE POWER AMPLIFIER WITH NOVEL DUAL STAGE LINEARIZER FOR MOBILE WIRELESS COMMUNICATION*

U. ESWARAN†, H. RAMIAH‡, J. KANESAN§ and A. W. REZA¶

Department of Electrical Engineering, University of Malaya, 50603, Kuala Lumpur, Malaysia
†*urjeswaran@siswa.um.edu.my*
‡*hrkhari@um.edu.my*
§*jievan@um.edu.my*
¶*wasif@um.edu.my*

Received 16 January 2013
Accepted 17 April 2014
Published 21 May 2014

In this paper, a 1 mm × 1 mm fully integrated wideband dual-stage power amplifier (PA) for long-term evolution (LTE) band 1 (1920–1980 MHz) is presented. Fabricated in a 2 μm InGaP/GaAs hetero-junction bipolar transistor (HBT) process, the operating gain is observed to be 31.3 dB. The PA meets the minimum adjacent channel leakage ratio (ACLR) requirement of −30 dBc for LTE with 20 MHz wide channel bandwidth up to an output power of 30 dBm with the aid of a novel dual stage linearizer. Biased at low quiescent current of less than 100 mA with a headroom consumption of 3.5 V, the power added efficiency (PAE) is observed to be 38.29% at 30 dBm. With this high linear output power, the stringent requirement of antenna path loss is nullified. PA serves to be the first reported work to achieve 30 dBm linear output power at supply voltage of 3.5 V.

Keywords: Power amplifier; linearizer; LTE.

1. Introduction

The demand for high data rate information in modern wireless communication systems has led to the birth of long-term evolution (LTE). LTE presents great opportunities for high speed wireless communication. However, the requirement of high output data rate results in an increased signal complexity such as the employment of multicarrier modulation standards and non-constant envelope modulation techniques. LTE employs quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM) modulation techniques. The access

*This paper was recommended by Regional Editor Piero Malcovati.
‡Corresponding author.

http://dx.doi.org/10.5755/j01.eee.20.4.3185 ELEKTRONIKA IR ELEKTROTECHNIKA, ISSN 1392–1215, VOL. 20, NO. 4, 2014

Class-E Power Amplifier with Novel Pre-Distortion Linearization Technique for 4G Mobile Wireless Communications

U. Eswaran[1], H. Ramiah[1], J. Kanesan[1]
[1]*Department of Electrical Engineering, Faculty of Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia*
hrkhari@um.edu.my

***Abstract*—A new method to improve the battery life span of a 4G handset power amplifier (PA) is proposed. This technique is realized by employing a novel passive linearization topology on a class-E PA. Implemented in a 2 µm InGaP/GaAs Hetero-Junction Bipolar Transistor (HBT) technology, the PA delivers 49 % of power added efficiency (PAE) at output power of 28 dBm while complying with the Long Term Evolution (LTE) regulation at Band 1(1920 MHz–1980 MHz) with corresponding supply voltage headroom of 4 V. The performance enhancement is achieved at LTE channel bandwidth of 20 MHz. To the best of the author's knowledge, this is the first class-E PA which meets adjacent channel leakage ratio (ACLR) specifications at 20 MHz LTE bandwidth.**

***Index Terms*—Linearization, LTE, PAE, power amplifier.**

I. Introduction

Long Term Evolution (LTE) protocol is a prominent solution to fulfill the continuous demand for high data rate transmission. LTE is capable in establishing a downlink peak data rate up to 326.4 Mbps and maximum data rate of 86.4 Mbps for the uplink [1]. Therefore, the demand of high output data rate results in an increased signal complexity nurturing towards the employment of multicarrier modulation standards. Owing to this signal complexity, the transmitter system, especially the power amplifier is regulated to maintain a linear operating region [2]. In fulfilling this criterion, the PA is operated at a back-off output power level from its 1 dB compression point. The operation is subjected to the degradation in the efficiency of the PA.

Several optimization methods have been reported in the effort to achieve a desired PAE for the designated PA. The most prominent is the envelope tracking method, which is reported to deliver a PAE of up to 39 %, thus complying the linearity specification for LTE signal with 10 MHz of channel bandwidth. However, in order to meet the stipulated performance criterion, a hybrid, cost ineffective dual technology has to be employed, which is a merger of CMOS and GaAs HBT [3]. An alternative approach is in realizing a RF CMOS only PA, which proves to deliver 25.8 % of PAE at a corresponding output power of 29.4 dBm [4].

In this work, a class E PA has been designed and realized in an objective to achieve a high PAE, which is measured to be 49 %. A class-E PA is categorized as a non-linear PA due to its operation at the cut-off region of the I-V curve. Hence, in order for the PA to meet the LTE linearity requirement as regulated in the 3GPP specifications [5], a novel passive linearization technique has been proposed and integrated. The linearization technique cancels out the third order intermodulation (IMD3) at high output power, thus confirming to the ACLR specifications.

This paper is organized as follows. Section II reviews the operation principle of the proposed circuit. Section III explains the theory of operation of the linearized class-E PA. In Section IV, the measured results are presented, followed by the conclusion in Section V.

II. Principle of Operation

Figure 1 illustrates the topology of the proposed PA, which integrates a Class-E PA, passive pre-distorter linearizer and an output matching network ensuring a maximum linear output power at the designated PAE. The Class-E PA encapsulates a HBT transistor and a shunt capacitor, C_1. The passive pre-distorter is connected at the input of the Class-E PA, prior to the parallel RC network. The parallel RC network protects the PA from thermal runaway phenomenon [6]. The output matching network is tasked upon to transform the 50 ohm output impedance to a desired impedance point, which delivers the maximum output power. The methodology in obtaining this impedance point is explained in section III. The G_m compensation technique [7] is adapted in the development of the biasing circuit. This technique helps to stabilize the base-emitter voltage of the biasing circuit, ensuring insensitivity towards an abrupt change of the supply voltage. The collector and base of transistor Q_{b3} is shorted realizing a diode and further connected to the base of Q_{b2}. Transistor, Q_{b3} acts as temperature compensator alleviating significant changes in the biasing current across temperature variation.

The proposed PA is fabricated using GaAs HBT technology due to its superior electrical characteristics at high frequency operation [8]. Its inherent characteristics of low collector-emitter offset voltage and low resistance

Manuscript received May 2, 2013; accepted December 17, 2013.
This research is supported by the Science Fund Grant SF003-2013 from the Ministry of Higher Education Malaysia.

OPEN ACCESS Freely available online

PLOS ONE

Wideband LTE Power Amplifier with Integrated Novel Analog Pre-Distorter Linearizer for Mobile Wireless Communications

Eswaran Uthirajoo, Harikrishnan Ramiah*, Jeevan Kanesan, Ahmed Wasif Reza

Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur, Malaysia

Abstract

For the first time, a new circuit to extend the linear operation bandwidth of a LTE (Long Term Evolution) power amplifier, while delivering a high efficiency is implemented in less than 1 mm^2 chip area. The 950 μm × 900 μm monolithic microwave integrated circuit (MMIC) power amplifier (PA) is fabricated in a 2 μm InGaP/GaAs process. An on-chip analog pre-distorter (APD) is designed to improve the linearity of the PA, up to 20 MHz channel bandwidth. Intended for 1.95 GHz Band 1 LTE application, the PA satisfies adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) specifications for a wide LTE channel bandwidth of 20 MHz at a linear output power of 28 dBm with corresponding power added efficiency (PAE) of 52.3%. With a respective input and output return loss of 30 dB and 14 dB, the PA's power gain is measured to be 32.5 dB while exhibiting an unconditional stability characteristic from DC up to 5 GHz. The proposed APD technique serves to be a good solution to improve linearity of a PA without sacrificing other critical performance metrics.

Citation: Uthirajoo E, Ramiah H, Kanesan J, Reza AW (2014) Wideband LTE Power Amplifier with Integrated Novel Analog Pre-Distorter Linearizer for Mobile Wireless Communications. PLoS ONE 9(7): e101862. doi:10.1371/journal.pone.0101862

Editor: Sefer B. Lisesivdin, Gazi University, Turkey

Received March 2, 2014; **Accepted** June 12, 2014; **Published** July 17, 2014

Funding: This research is supported by the UM High Impact Research Grant UM.C/HIR/MOHE/ENG/51 from the Ministry of Higher Education Malaysia. The funder had no role in study design, data collection and analysis, decision to publish, or preparation of the manuscript.

Competing Interests: The authors have declared that no competing interests exist.

* Email: hrkhari@um.edu.my

Introduction

Information and communication technology (ICT) plays a significant role in globalization process which has reorganized the world economy [1]. Therefore, communication standards need to be continuously upgraded to the next level. This has led into the birth of Long Term Evolution (LTE) protocol. LTE is a prominent solution to fulfill the continuous demand for high data rate transmission. LTE is capable in establishing downlink peak data rates up to 326.4 Mbps and 86.4 Mbps for the uplink [2]. It also has an advantage of variable channel bandwidth, which ranges from 1.4 MHz to 20 MHz. Service providers are expected to benefit from this luxury, in the context of cost and channel allocations. LTE utilizes single carrier frequency division multiple access (SC-FDMA) for uplink and orthogonal frequency division multiple access (OFDMA) for downlink as its multicarrier modulation standard catering towards high data rates transmission [3]. SC-FDMA has a comparable performance and complexity to OFDMA, with an advantage of lower peak-to- average-power-ratio (PAPR) [4]. Typically, the PAPR of OFDMA signal is 10 dB whereas for SC-FDMA is 7 dB [2].

In order to transmit signals with high PAPR linearly (without any clipping), power amplifiers are usually operated at backed off output power. For example, if the signal's PAPR is 7 dB, the PA's maximum output power has to be 35 dBm in order to meet LTE linearity specifications (ACLR and EVM) at an output power of 28 dBm. This degrades its efficiency, η. η is defined as:

$$\eta = \frac{P_{out}}{P_{DC}} \times 100\% \quad (1)$$

where P_{out} represents the output power delivered by the PA whereas P_{DC} denotes the DC power supplied to the PA. The relationship between backed off output power and efficiency is expressed as [5]:

$$\eta_{pbo-classA} = \frac{1}{2} \cdot \frac{P_{bo}}{P_{\max}} \text{ for class A PA} \quad (2)$$

$$\eta_{pbo-classB} = \frac{\pi}{4} \cdot \sqrt{\frac{P_{bo}}{P_{\max}}} \text{ for class B PA} \quad (3)$$

where P_{bo} and P_{max} represent backed off output power and maximum output power respectively. With reference to (2) and (3), PA which transmits LTE signal with PAPR of 7 dB, delivers an efficiency of 9.9% and 35% at backed off output power, P_{bo} of 28 dBm (P_{max} is 35 dBm) if it's operating in class-A or class-B mode. As a consequence, the battery energy is drained out rapidly.

The solution to improve η at backed off output power is to either reduce the back-off level by reducing the P_{max} (smaller device size) or through the introduction of efficiency enhancement techniques. However, reduction of backed off output power level drives the PA to fail linearity specifications, thus mandating

A High Efficiency 1.8W Power Amplifier for Wireless Communications

U.Eswaran[1], H.Ramiah[1, 2], J.Kanesan[1]
[1]*Department of Electrical Engineering, Faculty of Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia*
[2]*hrkhari@um.edu.my*

***Abstract*—A power amplifier, implemented in 2µm InGaP/GaAs Heterojunction Bipolar Transistor (HBT) is presented. The size of the fabricated chip is 700 µm x 700 µm. With an integrated input matching network, the PA observes an input return loss (S_{11}) of -22dB. Biased at low quiescent current of 65mA, it delivers a maximum output power of 1.8W with 71% efficiency at 1.85GHz. The output return loss (S_{22}) of the PA is -15.2dB.The output matching network is designed to reduce the mismatch loss between the power amplifier and the antenna without compromising the output power and efficiency. The PA also exhibits a K-factor greater than 1 from DC up to 5GHz, ensuring unconditional stability. The power gain of the PA is 14.9dB. The measured results verify that the PA is capable to operate at high efficiency and to deliver high output power with a good output return loss.**

***Index Terms*— Heterojunction Bipolar Transistor (HBT), Power amplifier, power added efficiency (PAE), return loss**

I. INTRODUCTION

Power amplifier (PA) is tasked upon in the amplification of low level signal to a desired output power in a transmitter system. This is accomplished by converting a dc input power to a significant amount of microwave/RF output power [1]-[5].Therefore an efficient transmission is always desired [6]-[10].

Several technologies are utilized in designing PA for various applications in wireless communications. For low voltage application, the HBT technology appears to be prominent. This is due to its inherent characteristic of low collector-emitter offset voltage and low resistance [11]-[13]. Moreover, it has superior electrical characteristics at high frequencies [14], which helps to transmit high output power with minimum parasitic loss. The HBT technology inherits low leakage current, thus eliminating the need to have an extra dc switch to turn off the power supply, which is a common practice in GaAs MESFET amplifiers [15].

An efficient power conversion is always desired in realizing a good PA. Often, power losses in HBT PA are due to thermal effect and mismatch loss in the transmitter system. In HBT technology, the former effect is minimized with ballasting technique. In this technique, a resistor is implemented at the base or emitter of a HBT to prevent the collapse of the collector current in the event one of the HBT unit cell operates at a higher temperature [16]-[19]. The solution to the latter effect is usually found by designing an antenna respective to the output impedance of the PA. Hence a custom antenna design is always needed. This imposes a great inconvenience to the transmitter system designers.

This paper presents the design of a PA which observes less than -12dB input and output return loss with maximum output power of 1.8W. The PA has highest PAE of 71% and power gain of 14.9dB, while maintaining a broadband stability factor from DC to 5GHz.

II. POWER AMPLIFIER DESIGN METHODOLOGY

Fig. 1 depicts the schematic of the designed PA, encapsulating the HBT transistor, input matching network, output matching network and bias circuit.

The PA employs common emitter structure in order to achieve reasonable trade-off between gain, output power and efficiency [20]. An accurate input impedance matching network is an important criterion since it allows maximum power transfer under a prescribed load condition [21]. Hence, the input matching network integrating C_2, L_1, C_4, L_3 and C_6 has been designed based on the following equation [22]:

$$P_{IN} = P_{AVS} M_S \tag{1}$$

where

$$M_S = \frac{(1-|\Gamma_S|^2)(1-|\Gamma_{IN}|^2)}{|1-\Gamma_S\Gamma_{IN}|^2} \tag{2}$$

P_{IN}, P_{AVS} and M_S denotes input power to the amplifier, available power from the signal source and mismatch loss between signal source and input of the PA, respectively. If M_S=1, then all the available power from source will be transferred to the input of the PA. This is quantified by a very low input return loss (S_{11}) in the measurement. The objective of M_S=1 is achieved when the condition is satisfied to be:

$$\Gamma_{IN} = \Gamma_S^* \tag{3}$$

The relationship between Γ_{IN} and S_{11} is given by:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}\cdot S_{21}\cdot \Gamma_L}{1-S_{22}\cdot \Gamma_L} \tag{4}$$

where S_{12}, S_{21}, S_{22} and Γ_L represents the isolation between input and output port of the PA, gain of the PA, output return loss of the PA and load reflection coefficient, respectively. If S_{12}=0, which translates to a perfect isolation, then Γ_{IN}=S_{11}.

A Novel Power Amplifier Linearization Method for Handset Applications

U. Eswaran*, H. Ramiah, J. Kanesan

Department of Electrical Engineering
Faculty of Engineering
University of Malaya
50603 Kuala Lumpur, Malaysia
Email: urjeswaran@siswa.um.edu.my

Abstract –A new circuit concept to improve the maximum linear output power of a Universal Mobile Telecommunication System (UMTS) power amplifier (PA) is introduced in this paper. The proposed circuit consists of an analog pre-distorter (APD) integrated at the input of a class B amplifier. The proposed APD extends the maximum linear output power of the PA to 28dBm with corresponding power added efficiency (PAE) of 52.3%. Simulation result shows that at 1.95GHz, PA has a worst case adjacent channel leakage ratio (ACLR) of -36dBc at output power of 28dBm. With a respective input and output return losses of -27.6dB and -13.2dB, the PA's power gain is simulated to be 33.3dB while exhibiting an unconditional stability characteristic from DC to 3GHz. The monolithic microwave integrated circuit (MMIC) power amplifier (PA) is designed in 2μm InGaP/GaAs process. The proposed APD technique serves to be a good solution to improve the maximum linear output power of the UMTS PA without sacrificing other critical performance metrics.

Keywords: Power amplifier, Analog Pre-distorter, Power added efficiency, Heterojunction bipolar transistor, Universal mobile telecommunication system, Adjacent channel leakage ratio

Introduction

Recently, there is an explosive growth in the number of UMTS standard users. This is due to the excitement in the high data rate usage around the globe. Therefore, handset designers, particularly power amplifier (PA) designers confront stiff challenges in improving the maximum linear output power so that linear transmission still occurs in remote areas. This transmission also needs to be efficient in order to prevent rapid energy drainage of the battery.

Several methods have been reported recently to improve the maximum linear output power of the PA. The most prominent technique among them is the pre-distortion technique. In this method, the input RF signal to the PA is distorted prior amplification by changing its non-linear transfer function's magnitude and phase to have an opposite responses to the phase and magnitude of the non-linear components generated by the PA. The Digital Pre-distortion Technique (DPD) is the upcoming pre-distortion method used to linearize the PA [1]-[3]. In this method, these non-linear responses are generated with the aid of a DSP processor. The complexity in integration, resulting in larger chip size and dual fabrication process are among the visible disadvantages of DPD. On the other hand, APD offers a simple solution of integrating additional active devices, usually

APPENDIX A – REDUCED CONDUCTION ANGLE ANALYSIS

If

$$I_{cc}(\theta) = \frac{I_{\max}}{1-\cos(\alpha/2)}\left(\cos\theta - \cos(\alpha/2)\right), \tag{1}$$

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}\left(\cos\theta - \cos(\alpha/2)\right)d\theta \tag{2}$$

and

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2)).\cos(n\theta)d\theta \tag{3}$$

Resultant of Equation (2):

$$I_{dc} = \frac{I_{\max}}{2\pi}\left(\frac{2\sin(\alpha/2) - (\alpha\cos(\alpha/2))}{1-\cos(\alpha/2)}\right) \tag{4}$$

Fundamental component I_1 (n=1)

$$I_1 = \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\cos^2\theta d\theta - \int_{-\alpha/2}^{\alpha/2}\cos(\alpha/2).\cos\theta d\theta \tag{5}$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\frac{1+\cos 2\theta}{2}d\theta - \cos(\alpha/2)\int_{-\alpha/2}^{\alpha/2}\cos\theta d\theta \tag{6}$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\frac{1}{2}d\theta + \frac{1}{2}\int_{-\alpha/2}^{\alpha/2}\cos 2\theta - \cos(\alpha/2)\int_{-\alpha/2}^{\alpha/2}\cos\theta d\theta \tag{7}$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\left[\frac{1}{2}\right]_{-\alpha/2}^{\alpha/2} + \frac{1}{2}\left[\frac{1}{2}\sin 2\theta\right]_{-\alpha/2}^{\alpha/2} - \cos(\alpha/2)\left[\sin\theta\right]_{-\alpha/2}^{\alpha/2}\right) \tag{8}$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\frac{\alpha}{2}+\frac{1}{2}\left[\frac{1}{2}\sin(\alpha)-\frac{1}{2}\sin(-\alpha)\right]-\cos\left(\frac{\alpha}{2}\right)\left[\sin\left(\frac{\alpha}{2}\right)+\sin\left(\frac{\alpha}{2}\right)\right]\right) \quad (9)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\frac{\alpha}{2}+\frac{1}{2}\sin(\alpha)-2\cos\left(\frac{\alpha}{2}\right)\sin\left(\frac{\alpha}{2}\right)\right) \quad (10)$$

$$= \frac{I_{max}}{2\pi(1-\cos(\alpha/2))}\left(\frac{\alpha}{2}+\frac{\sin\alpha}{2}-\sin\alpha\right) \quad (11)$$

$$I_1 = \frac{I_{max}}{2\pi}\left[\frac{\alpha-\sin\alpha}{1-\cos\left(\frac{\alpha}{2}\right)}\right] \quad (12)$$

Second order component I_2 (n=2)

$$I_2 = \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\cos\theta\cos 2\theta d\theta - \int_{-\alpha/2}^{\alpha/2}\cos(\alpha/2)\cos 2\theta d\theta \quad (13)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\frac{1}{2}\left[\cos(\theta-2\theta)+\cos(\theta+2\theta)\right]d\theta - \cos(\alpha/2)\int_{-\alpha/2}^{\alpha/2}\cos 2\theta d\theta \quad (14)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\left[\int_{-\alpha/2}^{\alpha/2}\cos\theta d\theta+\int_{-\alpha/2}^{\alpha/2}\cos 3\theta d\theta\right]-\cos\left(\frac{\alpha}{2}\right)\int_{-\alpha/2}^{\alpha/2}\cos 2\theta d\theta\right) \quad (15)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\left[\left[\sin\theta\right]_{-\alpha/2}^{\alpha/2}+\left[\frac{1}{3}\sin 3\theta\right]_{-\alpha/2}^{\alpha/2}\right]-\cos\left(\frac{\alpha}{2}\right)\left[\frac{1}{2}\sin(2\theta)\right]_{-\alpha/2}^{\alpha/2}\right) \quad (16)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\left[2\sin\frac{\alpha}{2}+\frac{2}{3}\sin\frac{3\alpha}{2}\right]-\cos\frac{\alpha}{2}\sin\alpha\right) \quad (17)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\sin\frac{\alpha}{2}+\frac{1}{3}\sin\frac{3\alpha}{2}-\left[\frac{1}{2}\left(\sin\left(\alpha-\frac{\alpha}{2}\right)+\sin\left(\alpha+\frac{\alpha}{2}\right)\right)\right]\right) \quad (18)$$

$$= \frac{I_{max}}{\pi(1-\cos(\alpha/2))}\left(\sin\frac{\alpha}{2}+\frac{1}{3}\sin\frac{3\alpha}{2}-\left[\frac{1}{2}\sin\frac{\alpha}{2}+\frac{1}{2}\sin\frac{3\alpha}{2}\right]\right) \quad (19)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\sin\frac{\alpha}{2}+\frac{1}{3}\sin\frac{3\alpha}{2}-\frac{1}{2}\sin\frac{\alpha}{2}-\frac{1}{2}\sin\frac{3\alpha}{2}\right) \quad (20)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\sin\frac{\alpha}{2}-\frac{1}{6}\sin\frac{3\alpha}{2}\right) \quad (21)$$

$$\mathrm{I}_2 = \frac{I_{\max}}{2\pi(1-\cos(\alpha/2))}\left(\sin\frac{\alpha}{2}-\frac{1}{3}\sin\frac{3\alpha}{2}\right) \quad (22)$$

Third order component I_3 (n=3)

$$I_3 = \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\cos\theta\cos3\theta d\theta - \int_{-\alpha/2}^{\alpha/2}\cos(\alpha/2)\cos3\theta d\theta \quad (23)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\frac{1}{2}[\cos(\theta-3\theta)+\cos(\theta+3\theta)]d\theta - \cos(\alpha/2)\int_{-\alpha/2}^{\alpha/2}\cos3\theta d\theta \quad (24)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\left[\int_{-\alpha/2}^{\alpha/2}\cos2\theta d\theta + \int_{-\alpha/2}^{\alpha/2}\cos4\theta d\theta\right] - \cos\left(\frac{\alpha}{2}\right)\int_{-\alpha/2}^{\alpha/2}\cos3\theta d\theta\right) \quad (25)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\left[\left[\frac{1}{4}\sin2\theta\right]_{-\alpha/2}^{\alpha/2} + \left[\frac{1}{8}\sin4\theta\right]_{-\alpha/2}^{\alpha/2}\right] - \cos\left(\frac{\alpha}{2}\right)\left[\frac{1}{3}\sin3\theta\right]_{-\alpha/2}^{\alpha/2}\right) \quad (26)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\sin\alpha+\frac{1}{4}\sin2\alpha-\frac{1}{3}(\sin\alpha+\sin2\alpha)\right) \quad (27)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{6}\sin\alpha-\frac{1}{12}\sin2\alpha\right) \quad (28)$$

$$\mathrm{I}_3 = \frac{I_{\max}}{2\pi(1-\cos(\alpha/2))}\left(\frac{1}{3}\sin\alpha-\frac{1}{6}\sin2\alpha\right) \quad (29)$$

Fourth order component I_4 (n=4)

$$I_4 = \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\cos\theta\cos4\theta d\theta - \int_{-\alpha/2}^{\alpha/2}\cos(\alpha/2)\cos4\theta d\theta \quad (30)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))} \int_{-\alpha/2}^{\alpha/2} \frac{1}{2}[\cos(\theta-4\theta)+\cos(\theta+4\theta)]d\theta - \cos(\alpha/2)\int_{-\alpha/2}^{\alpha/2}\cos 4\theta d\theta \quad (31)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{2}\left[\int_{-\alpha/2}^{\alpha/2}\cos 3\theta d\theta + \int_{-\alpha/2}^{\alpha/2}\cos 5\theta d\theta\right] - \cos\left(\frac{\alpha}{2}\right)\int_{-\alpha/2}^{\alpha/2}\cos 4\theta d\theta\right) \quad (32)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\left[\left[\frac{1}{6}\sin 3\theta\right]_{-\alpha/2}^{\alpha/2} + \left[\frac{1}{10}\sin 5\theta\right]_{-\alpha/2}^{\alpha/2}\right] - \cos\left(\frac{\alpha}{2}\right)\left[\frac{1}{4}\sin 4\theta\right]_{-\alpha/2}^{\alpha/2}\right) \quad (33)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{3}\sin\frac{3\alpha}{2} + \frac{1}{5}\sin\frac{5\alpha}{2} - \frac{1}{4}\sin\frac{3\alpha}{2} - \frac{1}{4}\sin\frac{5\alpha}{2}\right) \quad (34)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{12}\sin\frac{3\alpha}{2} - \frac{1}{20}\sin\frac{5\alpha}{2}\right) \quad (35)$$

$$\mathrm{I}_4 = \frac{I_{\max}}{2\pi(1-\cos(\alpha/2))}\left(\frac{1}{6}\sin\frac{3\alpha}{2} - \frac{1}{10}\sin\frac{5\alpha}{2}\right) \quad (36)$$

Fifth order component I_5 (n=5)

$$I_5 = \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\int_{-\alpha/2}^{\alpha/2}\cos\theta\cos 5\theta d\theta - \int_{-\alpha/2}^{\alpha/2}\cos\frac{\alpha}{2}\cos 5\theta d\theta \quad (37)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\int_{-\alpha/2}^{\alpha/2}\frac{1}{2}\cos 4\theta d\theta + \int_{-\alpha/2}^{\alpha/2}\frac{1}{2}\cos 6\theta - \cos\frac{\alpha}{2}\int_{-\alpha/2}^{\alpha/2}\cos 5\theta d\theta\right) \quad (38)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\left[\left[\frac{1}{8}\sin 4\theta\right]_{-\alpha/2}^{\alpha/2} + \left[\frac{1}{12}\sin 6\theta\right]_{-\alpha/2}^{\alpha/2}\right] - \cos\left(\frac{\alpha}{2}\right)\left[\frac{1}{5}\sin 5\theta\right]_{-\alpha/2}^{\alpha/2}\right) \quad (39)$$

$$= \frac{I_{\max}}{\pi(1-\cos(\alpha/2))}\left(\frac{1}{4}\sin 2\alpha - \frac{1}{5}\sin 2\alpha + \frac{1}{6}\sin 3\alpha - \frac{1}{5}\sin 3\alpha\right) \quad (40)$$

APPENDIX B – CLASS-J POWER AMPLIFIER FUNDAMENTAL AND SECOND ORDER VOLTAGE ANALYSIS

Fourier analysis on Fundamental Voltage component of Class-J Amplifier

$$V_1(\theta) = V_A \cos(\theta) + V_B \sin(\theta) \tag{1}$$

where

$$V_A = \frac{1}{\pi} \int V_0(\theta) \cos(\theta) d\theta \tag{2}$$

and

$$V_B = \frac{1}{\pi} \int V_0(\theta) \sin(\theta) d\theta \tag{3}$$

$$V_0 = \frac{1}{\omega C_{2f0}} \left[-\left(I_{\max} + 2I_1 \cos\phi\right) + \frac{I_{\max}}{\pi}(\theta - \pi) - I_1 \left[\cos(\theta + \phi) - \cos\phi\right] \right] \tag{4}$$

$$= \frac{1}{\omega C_{2f0}} \left[-2I_{\max} + \frac{I_{\max}}{\pi}\theta - I_1 \cos\phi - I_1 \cos(\theta + \phi) \right] \tag{5}$$

Insert (5) into (2):

$$V_A = \frac{1}{\omega C_{2f0}\pi} \left[\int_0^\theta -2I_{\max} \cos\theta d\theta + \int_0^\theta \frac{I_{\max}\theta}{\pi} \cos\theta d\theta - \int_0^\theta I_1 \cos\varphi \cos\theta d\theta - \int_0^\theta I_1 \cos(\theta + \varphi) \cos\theta d\theta \right]$$

…….. (6)

$$= \frac{1}{\omega C_{2f0}\pi} \begin{bmatrix} 2I_{\max}\left[-\sin\theta\right]_0^\theta + \frac{I_{\max}}{\pi}\left[\cos\theta + \theta\sin\theta\right]_0^\theta - I_1 \cos\varphi \left[\sin\theta\right]_0^\theta \\ -I_1 \left[\frac{1}{2} \left[\left[\theta\right]_0^\theta + \cos\varphi \left[\frac{1}{2}\sin 2\theta \right]_0^\theta - \sin\varphi \left[-\frac{1}{2}\cos 2\theta \right]_0^\theta \right] \right] \end{bmatrix} \tag{7}$$

$$V_A = \frac{1}{\omega C_{2f0}\pi}\begin{bmatrix} I_{\max}\left[-2\sin\theta + \frac{1}{\pi}\left(\cos\theta + \theta\sin\theta - 1\right)\right] \\ -I_1\left[\sin\theta\cos\varphi + \frac{1}{2}\theta + \frac{1}{4}\left(\sin 2\theta\cos\varphi + \sin\varphi\left(1+\cos 2\theta\right)\right)\right] \end{bmatrix} \quad (8)$$

Insert (5) into (3):

$$V_B = \frac{1}{\omega C_{2f0}\pi}\left[\int_0^\theta -2I_{\max}\sin\theta d\theta + \int_0^\theta \frac{I_{\max}\theta}{\pi}\sin\theta d\theta - \int_0^\theta I_1\sin\theta\cos\varphi d\theta - \int_0^\theta I_1\cos\left(\theta+\varphi\right)\sin\theta d\theta\right]$$

..... (9)

$$= \frac{1}{\omega C_{2f0}\pi}\begin{bmatrix} -2I_{\max}\left[-\cos\theta\right]_0^\theta + \frac{I_{\max}}{\pi}\left[\sin\theta - \theta\cos\theta\right]_0^\theta - I_1\cos\varphi\left[-\cos\theta\right]_0^\theta \\ -I_1\left[\frac{1}{2}\cos\varphi\left[-\frac{1}{2}\cos 2\theta\right]_0^\theta - \frac{1}{2}\sin\varphi\left[\left[\theta\right]_0^\theta - \left[\frac{1}{2}\sin 2\theta\right]_0^\theta\right]\right] \end{bmatrix} \quad (10)$$

$$V_B = \frac{1}{\omega C_{2f0}\pi}\begin{bmatrix} I_{\max}\left[\frac{1}{\pi}\left(\sin\theta - \theta\cos\theta\right) - 2\left(1-\cos\theta\right)\right] \\ -I_1\left[\cos\theta\left(1-\cos\theta\right) - \frac{1}{2}\left(\frac{1}{2}\cos\varphi\left(1-\cos 2\theta\right) - \sin\theta\left(\theta - \frac{1}{2}\sin 2\theta\right)\right)\right] \end{bmatrix} \quad (11)$$

Therefore, the fundamental voltage component of the class-J PA if the output matching network is taken account is:

$$V_1(\theta) = \frac{1}{\omega C_{2f0}\pi}\begin{bmatrix} \begin{bmatrix} I_{\max}\left[-2\sin\theta + \frac{1}{\pi}\left(\cos\theta + \theta\sin\theta - 1\right)\right] \\ -I_1\left[\sin\theta\cos\varphi + \frac{1}{2}\theta + \frac{1}{4}\left(\sin 2\theta\cos\varphi + \sin\varphi\left(1+\cos 2\theta\right)\right)\right] \end{bmatrix} + \\ j\begin{bmatrix} I_{\max}\left[\frac{1}{\pi}\left(\sin\theta - \theta\cos\theta\right) - 2\left(1-\cos\theta\right)\right] \\ -I_1\left[\cos\theta\left(1-\cos\theta\right) - \frac{1}{2}\left(\frac{1}{2}\cos\varphi\left(1-\cos 2\theta\right) - \sin\theta\left(\theta - \frac{1}{2}\sin 2\theta\right)\right)\right] \end{bmatrix} \end{bmatrix}$$

.....(12)

Fourier analysis on 2nd order voltage component of Class-J Amplifier

$$V_2(\theta) = V_{2A}\cos(2\theta) + V_{2B}\sin(2\theta) \tag{13}$$

where

$$V_{2A} = \frac{1}{\pi}\int V_0(\theta)\cos(2\theta)d\theta \tag{14}$$

and

$$V_{2B} = \frac{1}{\pi}\int V_0(\theta)\sin(2\theta)d\theta \tag{15}$$

$$V_{2A} = \frac{1}{\omega C_{2f0}\pi}\left[\int_0^\theta -2I_{\max}\cos 2\theta d\theta + \int_0^\theta \frac{I_{\max}\theta}{\pi}\cos 2\theta d\theta - \int_0^\theta I_1\cos\varphi\cos 2\theta d\theta - \int_0^\theta I_1\cos(\theta+\varphi)\cos 2\theta d\theta\right]$$

$$= \frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} 2I_{\max}\left[-\frac{1}{2}\sin 2\theta\right]_0^\theta + \frac{I_{\max}}{\pi}\left[\frac{1}{2}\theta\sin 2\theta - \frac{1}{4}\cos 2\theta\right]_0^\theta - I_1\cos\varphi\left[\frac{1}{2}\sin 2\theta\right]_0^\theta \\ -\frac{1}{2}I_1\left[\cos\varphi\left[\sin\theta\right]_0^\theta + \sin\varphi\left[-\cos\theta\right]_0^\theta + \cos\varphi\left[\frac{1}{3}\sin 3\theta\right]_0^\theta - \sin\varphi\left[-\frac{1}{3}\cos 3\theta\right]_0^\theta\right] \end{array}\right]$$

…… (16)

$$V_{2A} = \frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} I_{\max}\left[\frac{1}{\pi}\left(\frac{1}{2}\theta\sin 2\theta - \frac{1}{4}\cos 2\theta + \frac{1}{4}\right) - \sin 2\theta\right] \\ +I_1\left[\sin(\theta-\varphi) - \frac{1}{3}\sin\varphi - \frac{1}{6}\sin(3\theta+\varphi) - \frac{1}{2}\sin 2\theta\cos\varphi\right] \end{array}\right] \tag{17}$$

$$V_{2B} = \frac{1}{\omega C_{2f0}\pi}\left[\int_0^\theta -2I_{\max}\sin 2\theta d\theta + \int_0^\theta \frac{I_{\max}\theta}{\pi}\sin 2\theta d\theta - \int_0^\theta I_1\sin 2\theta\cos\varphi d\theta - \int_0^\theta I_1\cos(\theta+\varphi)\sin 2\theta d\theta\right]$$

…… (18)

$$= \frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} -2I_{\max}\left[-\frac{1}{2}\cos 2\theta\right]_0^{\theta} + \frac{I_{\max}}{\pi}\left[\frac{1}{4}\sin 2\theta - \frac{1}{2}\theta\cos 2\theta\right]_0^{\theta} - I_1\cos\varphi\left[-\frac{1}{2}\cos 2\theta\right]_0^{\theta} \\ -\frac{1}{2}I_1\left[\cos\varphi\left[-\cos\theta\right]_0^{\theta} - \sin\varphi\left[\sin\theta\right]_0^{\theta} + \cos\varphi\left[-\frac{1}{3}\cos 3\theta\right]_0^{\theta} + \sin\varphi\left[\frac{1}{3}\sin 3\theta\right]_0^{\theta}\right] \end{array}\right]$$

… (19)

$$V_{2B} = \frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} I_{\max}\left[\frac{1}{2\pi}\left(\frac{1}{2}\sin 2\theta - \theta\cos 2\theta\right) + \cos 2\theta - 1\right] \\ -\frac{1}{2}I_1\left[\begin{array}{l} \cos\varphi\left[1-\cos 2\theta\right] + \cos\varphi\left[1-\cos\theta\right] - \frac{1}{3}\cos\varphi\left[1-\cos 3\theta\right] \\ -\sin\theta\sin\varphi + \frac{1}{3}\sin 3\theta\sin\varphi \end{array}\right] \end{array}\right]$$

…. (20)

Therefore, the second order voltage component of the class-J PA if the output matching network is taken account is represented as:

$$V_2(\theta) = \frac{1}{\omega C_{2f0}\pi}\left[\begin{array}{l} \left[\begin{array}{l} I_{\max}\left[\frac{1}{\pi}\left(\frac{1}{2}\theta\sin 2\theta - \frac{1}{4}\cos 2\theta + \frac{1}{4}\right) - \sin 2\theta\right] \\ +I_1\left[\sin(\theta-\varphi) - \frac{1}{3}\sin\varphi - \frac{1}{6}\sin(3\theta+\varphi) - \frac{1}{2}\sin 2\theta\cos\varphi\right] \end{array}\right] - \\ j\left[\begin{array}{l} \frac{1}{2}I_1\left[\begin{array}{l} \cos\varphi\left[1-\cos 2\theta\right] + \cos\varphi\left[1-\cos\theta\right] - \\ \frac{1}{3}\cos\varphi\left[1-\cos 3\theta\right] - \sin\theta\sin\varphi + \frac{1}{3}\sin 3\theta\sin\varphi \end{array}\right] \\ -I_{\max}\left[\frac{1}{2\pi}\left(\frac{1}{2}\sin 2\theta - \theta\cos 2\theta\right) + \cos 2\theta - 1\right] \end{array}\right] \end{array}\right]$$

…….. (21)

APPENDIX C – CLASS-J OUTPUT MATCHING NETWORK ANALYSIS

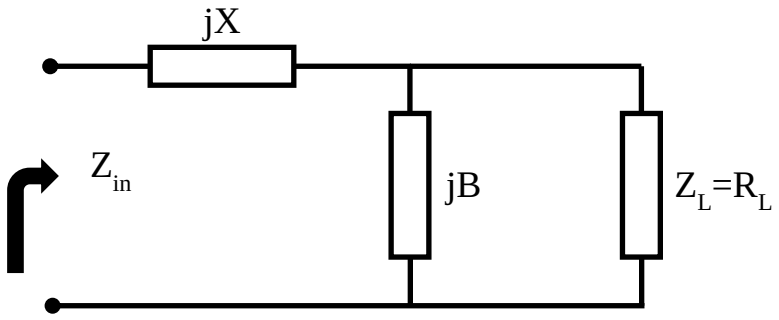


Figure C1: Impedance transformation from 25Ω to 2+j3Ω

Z_L =25Ω, Z_{in}= 2+j3Ω

$$Z_{in} = jX + \frac{1}{jB + \frac{1}{R_L}} \tag{1}$$

$$= jX + \frac{1}{\frac{jB(R_L)+1}{R_L}} \tag{2}$$

$$= jX + \frac{R_L}{jBR_L + 1} \tag{3}$$

$$= \frac{j^2 XBR_L + jX + R_L}{jBR_L + 1} \tag{4}$$

$$Z_{in} = \frac{-XBR_L + jX + R_L}{jBR_L + 1} \tag{5}$$

$$Z_{in} + jBR_L Z_{in} = R_L(1 - XB) + jX \tag{6}$$

$$2 + j3 + jB(25)(2 + j3) = 25(1 - XB) + jX \tag{7}$$

$$(2 - 75B) + j(3 + 50B) = 25 - 25XB + jX \tag{8}$$

Equating the real part:

$$2 - 75B = 25(1 - XB) \tag{9}$$

Equating the imaginary part:

$$3+50B=X \tag{10}$$

Insert (9) into (10):

$$2-75B=25\left[1-B\left(3+50B\right)\right] \tag{11}$$

$$B=\frac{\sqrt{46}}{50} \tag{12}$$

Insert (12) into (10):

$$X=3+\sqrt{46} \tag{13}$$

Therefore the respective components value is calculated as:

$$L=\frac{3+\sqrt{46}}{\omega_0} \tag{14}$$

and

$$C=\frac{\frac{\sqrt{46}}{50}}{\omega_0} \tag{15}$$