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Analysis and Design of a Hybrid Dickson Switched Capacitor Converter for Intermediate Bus Converter Applications

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I am submitting herewith a thesis written by Maeve Elise Lawniczak entitled "Analysis and Design of a Hybrid Dickson Switched Capacitor Converter for Intermediate Bus Converter Applications." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Abstract

By 2020 it is predicted that 1/3 of all data will pass through the cloud. With society's growing dependency on data, it is vital that data centers, the cloud's physical house of content, operate with optimal energy performance to reduce operating costs.

Unfortunately, today's data centers are inefficient, both economically and environmentally. This has led to an increase in demand for energy-efficient servers. One opportunity for improved efficiency is in the power delivery architecture which delivers power from the grid to the motherboard. In this dissertation, the main focus is the intermediate bus converter (IBC), used for the intermediate conversion, typically 48-12V/5V, in server power supplies. The IBC requires compact design so that it can be placed as close to the load as possible to enable more space for computing power and high efficiency to reduce the need for external cooling. Most commonly used converter topologies today include expensive bulky magnetics hindering the converter's power density. Furthermore, high output current of an IBC makes the efficiency very sensitive to any resistance, such as magnetic parasitic resistance or PCB trace resistance. In this work, analytical loss models are used to review the advantages and disadvantages of frequently used IBC topologies such as the phase-shifted full bridge and LLC. The Hybrid Dickson Switched Capacitor (HDSC) topology is also analyzed. The HDSC's high step-down conversion ratio and low dependence on magnetics due to the reduced applied volt-seconds, provides a new opportunity for applications such as the intermediate bus converter. The HDSC designs the on-time of devices in order to achieve soft-charging between flying capacitors. Other advantages of the HDSC include low switch stress, small magnetics and adjustable duty cycle for voltage regulation. Challenges, such as minimizing parasitic inductance and resistance between flying capacitors, are addressed and recommendations for PCB layout are provided. In this paper, a 4:1 24-5V and 8:1 48-5V,

100W GaN-based HDSC is designed and tested. The influences of capacitor mismatch and limitations placed on soft-charging operation for the HDSC is also modeled. This analysis can be used as a tool for designers when selecting flying capacitors.

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Chapter 1

Introduction

1.1 Data Centers and the Global Economy

Global Economy's Dependence on Data Centers

In recent decades, data centers have become the backbone of the global economy. Without data centers, businesses could not operate, communications could not occur and online consumer services would not be possible. Furthermore, with new technologies such as driver-less vehicles and crypto-currency leveraging data centers as well, the global economy's dependency on data centers is undeniable and continuing to grow [10].

Massive Data Center Infrastructure

The data center infrastructure required to support the world's Internet users is massive. On an individual level, most Americans today have a significant digital presence. Emails, social media, banking transactions, streaming entertainment, etc., all require the Internet and are made possible by data centers. On a global scale, there are approximately 2.5 billion people who use the Internet, 70 percent of which use the Internet every day [11] [12]. Not surprisingly, the infrastructure to support this global system is extremely large. In fact, according to the International Data Corporation (IDC), in 2015 there were 8.55 million data centers in the world, with the largest called The Citadel, covering 7.2 million square feet in Tahoe Reno, Nevada [13].

Data Center Energy Consumption

As stated in [14], "Data centers are one of the most energy-intensive building types, consuming 10-50 times the energy per floor space of a typical commercial office building." Put into more personal terms, charging a single tablet or smart phone requires a negligible amount of energy. However, streaming an hour of video once a week on either of these devices requires more energy from the data centers than two new refrigerators use in one year [15]. According to a study on data center energy usage conducted by the United States Department of Energy in 2014, US data centers consumed about 70 billion kilowatt-hours of electricity, representing about 2 percent of the country's total energy. This is a 4 percent increase in the data center energy consumption from 2010 to 2014 [16]. On a global scale, data centers consume approximately 3 percent of the world's global power [**?**]. And while the rate of increase has slowed down in recent years, the integral nature of data centers and cloud computing in today's global economy is undeniable and will continue to be one of the single largest global energy consumers.

Energy Consumption and Efficiency

A data center's massive energy consumption is largely due to the inefficiency of the system. Not only is energy needed for direct computing power, but to avoid temperature and humidity rise, which may lead to condensation forming on machines, energy is also needed for massive cooling systems. Most of the energy loss for a server occurs at the power supply, which converts the AC voltage coming from a standard outlet to a set of low DC voltages used to power microprocessors, memory subsystems, mass storage, network devices and the analog and digital interfaces that complete the system [17] [18]. Considering the power delivered from the grid to the motherboard, typical overall delivery efficiencies are around 50% [19]. As for the power supply, because of multiple power conversions within a single architecture, efficiencies are typically range from 70% [20]-80% [3] [21].

Summary

In summary, the global economy's reliance on data centers is undeniable. The sheer size and energy consumption is massive and there is a lot of room for improvement for making data centers more efficient. In particular, substantial efficiency improvements are needed in the power delivery architecture. Increasing efficiency and power density of the power delivery architecture will enable the overall system to operate more efficiently and in turn decrease the energy consumption and operating costs of data centers.

1.2 Market Trends for the Intermediate Bus Converter (IBC)

As stated in the previous section, increasing the efficiency of the data center power supply can greatly impact a data center's operating costs. Over recent decades, the power distribution technology for data centers has transitioned through several architectures starting with the centralized-power architecture (CPA) and evolving to the intermediate bus architecture. Each advancement has been driven by factors such as new technologies, demand for wider input voltage ranges, higher power levels and better supply performance [22].

This thesis focuses on the design for the intermediate bus converter (IBC), which is part of the intermediate bus architecture (IBA) depicted in Fig. 1.1. The IBC is one of three conversions in the power supply architecture and high efficiency is paramount for the design. The IBC is what differentiates the distributed power architecture (DPA) from the IBA. In order for the IBA to be competitive to the DPA, the IBC must have the highest efficiency among the power conversion stages. The power density is also critical. In order to keep conduction loss from connectors between conversion stages low, the IBC needs to be placed close to the motherboard. The evolution of the power supply system architecture ending with the inclusion of the IBC is summarized in the following section.

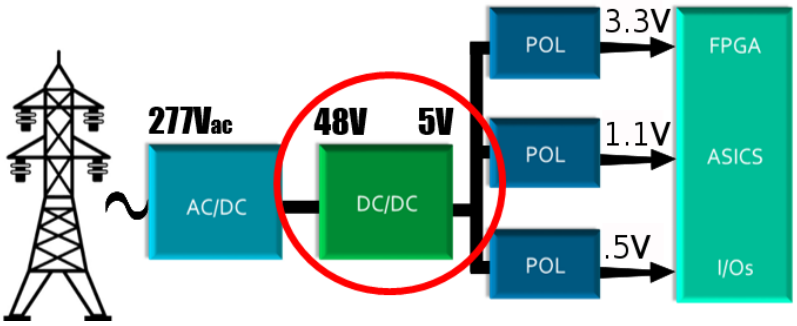


Figure 1.1: Intermediate bus location in the data center power supply system.

1.2.1 Centralized Power System

During the 1960's when semiconductor switches were becoming more accessible, a typical configuration for the centralized power system included an AC-DC rectifier/ charger that converted the AC input voltage to a 48V bus voltage. Then a DC/DC converter was used to step the voltage down from 48V to 5V or 12V. The centralized power supplies were typically located at the bottom of a server cabinet and connectors between conversion stages were long and made it difficult to deliver high power. The typical configuration is provided in Fig. 1.2. All of the voltages were generated at a central location and distributed to loads via buses. This particular design was used until the mid 1980's and was discontinued due to issues relating to long time to market, system failures occurring from a single component power failure, high cost for bulky bus bars and inability to accurately regulate the supply voltage [2].

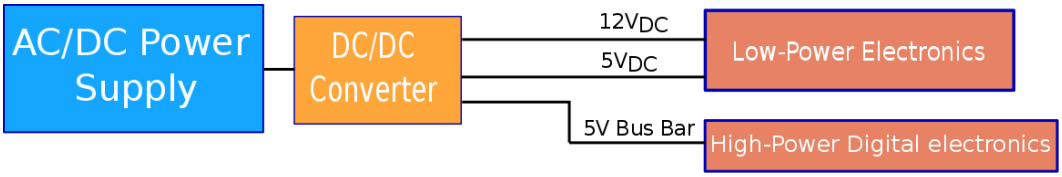


Figure 1.2: Centralized power architecture [2].

1.2.2 Distributed Power Architecture

In the early 1990s, following the centralized power system, came the distributed power architecture (DPA). The distributed power architecture broke the power conversion into building blocks as pictured in Fig. 1.3. The centralized system was replaced with an AC/DC front-end power supply that provided a 48V output to each shelf and line card. This more modular architecture enabled the line cards to be replaced when component failures occurred and decreased failure downtime. Each line card included multiple 48V, isolated DC/DC modules that provided the required voltages for the line-card loads. A combination of the trends towards digital functional blocks with lower voltages, market introduction of modular-isolated DC/DC converters and a need for higher reliability contributed to the evolution from the centralized power system to the distributed power architecture [2].

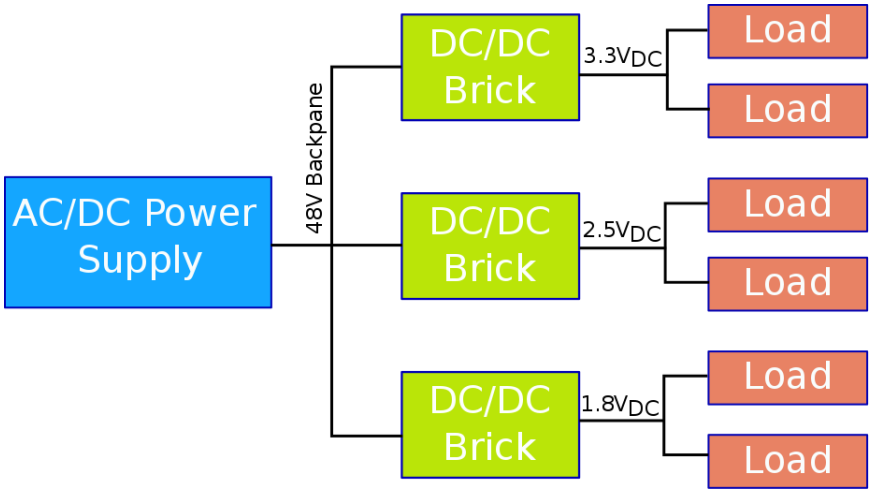


Figure 1.3: Distributed power supply [2].

1.2.3 Intermediate-Bus Architecture

By the early 2000s, demand increased for on-board low-cost point of load regulators, ranging from .5-3.3V, for digital and analog chips. This meant more DC/DC bricks were needed which took up more space and increased the system cost. This led to the market adoption of the Intermediate Bus Architecture (IBA). The IBA includes a front end AC/DC power supply, with a typical output of 48V, an intermediate bus converter that provides isolation and steps the voltage down to a bus voltage, typically between 14V-5V and non-isolated

point of loads (POLs) which provides high-quality voltages for a variety of digital and analog blocks. A diagram of this architecture is provided in Fig. 1.4. The IBA has been widely adopted and due to requiring only one isolated converter has enabled financial savings. The high quality voltage from the POLS has enabled higher efficiency and processing power for data center operations [23, 24, 25]. Other industries, such as space, are also taking a page from the data center world and are incorporating the intermediate bus architecture into their own technical designs [26].

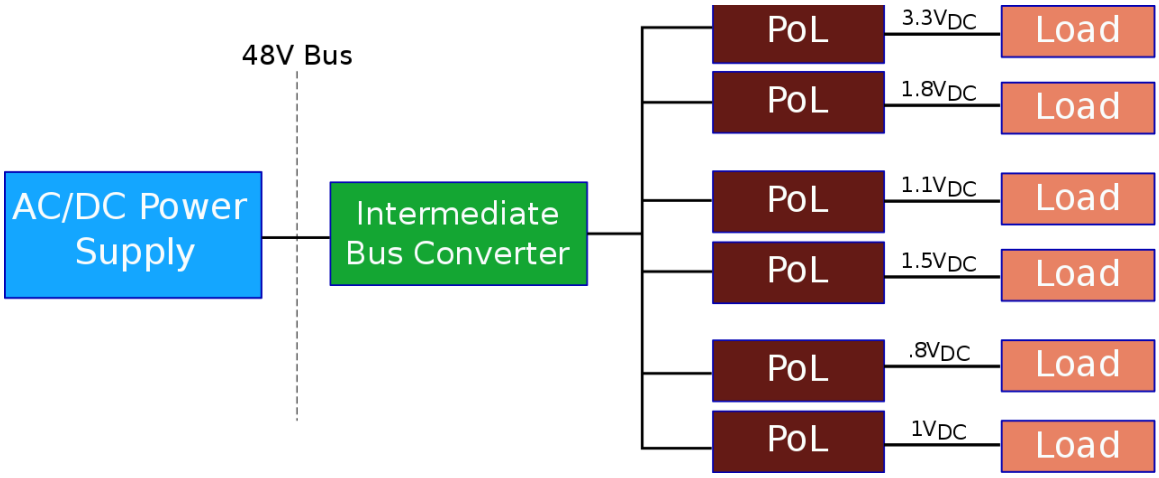


Figure 1.4: Intermediate-bus architecture [2].

1.2.4 Other Architecture Designs

With data centers upgrading IT equipment every 3-5 years [27], new architecture designs are looking for ways to lengthen system longevity while continuing to increase power density and efficiencies. Other approaches include the Factorized Power Architecture (FPA) developed by Vicor, claiming to provide better system performance, longevity and cost compared to the IBA [17]. This architecture eliminates the IBC and converts 48V to 1V as detailed in Fig.1.5. Google and Facebook have also recently collaborated to propose a similar architecture, boasting to reduce losses by 30% by delivering 48V directly to the server [3]. For this system, regulation occurs at the 277Vac-48V conversion, enabling the converter to be compact and placed closer to the load. While new architectures such as this may have proven to be

efficient, they require large scale redesigns of data center server structuring and large initial infrastructure investments.

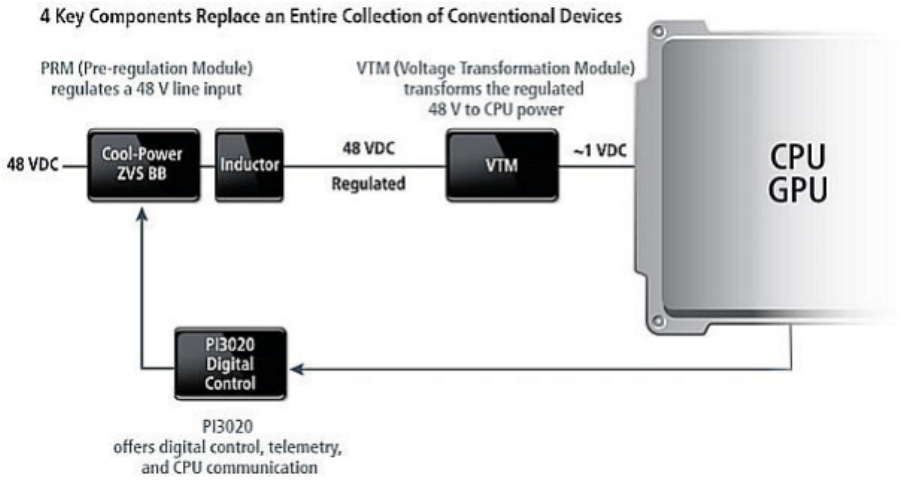


Figure 1.5: Vicor's 48V direct to the CPU architecture [3].

Summary

Over the past few decades the power supply architecture has evolved to the IBA. The IBA is cost effective and its modular structure enables high flexibility for modifications and updates. Adoption of the IBA is in part due to the IBC. IBCs need to have high efficiency for improved overall system efficiency as well as high power density. The IBC needs to be placed as close to the load as possible to reduce any I^2R loss that can be introduced by parasitics in the connectors between stages.

Chapter 2

Topology Exploration for the IBC

In the following section different topologies used in data center power supplies and for similar power levels are reviewed. Not all of the topologies include isolation though. Generally, the IBC is implemented using an isolated structure to protect the server components from power faults that could propagate from the front-end AC/DC converter. If a power surge occurs, the isolated IBC can shield the POL converters, which do not have isolation. Recently however, isolation for the IBC stage has not been required in some systems. Interestingly, the isolation characteristic was adopted from telecommunication systems which do require isolation. However, the power spike that warrants the isolation in telecommunication systems does not actually occur in data centers due to the isolation from the ac/dc conversion stage before the IBC. Therefore, isolation in the IBC stage, for particular systems, has been increasingly viewed as an over provisioned safety requirement [28].

2.1 Buck Converter

The buck converter is appealing for stepping down voltage due to its design simplicity and low cost. The buck, depicted in Fig. 2.1, is commonly used today for the Point-of-Load (POL) stage [**?** 29, 30]. With some data centers shifting to DC distribution systems due to the penetration of renewable energy sources in the distribution networks, the buck has been researched for other stages within the IBA, such as the 380V-48V conversion [31].

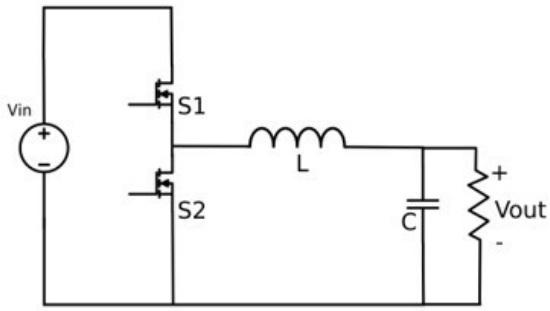


Figure 2.1: Buck topology.

One of the design limitations of the buck is the stress and loss created when operating with an extreme duty cycle. To extend a short duty cycle, designs such as [32] can divide the input voltage across stacked capacitors, increasing the duty cycle and decreasing the voltage stress across the high-side device. Other designs reduce the conduction loss at the output using a multi-phase design [33, 34, 35]. In [32] a multi-phase cascaded buck design is used for a 54V-1V conversion, the input voltage is stacked in series and the outputs are connected in parallel, however the overall power density becomes limited by the output inductors.

2.2 Phase-Shifted Full Bridge Converter

For IBC designs that still require isolation between the input and output, a transformer is needed in the converter design. The Phase-Shifted Full Bridge (PSFB) provides isolation as well as lower stress on devices and higher efficiencies compared to the buck converter. The phase-shifted full bridge, depicted in Fig. 2.2, is typically used for medium power levels ranging from 200W-3kW and for applications such as data center power supplies, telecommunication, micro/mild hybrid vehicles, renewable energy systems and battery based storage systems. Efficiencies for PSFB used across these applications range from 85% to 93% [36, 37, 38, 39, 40]. Similar to the buck design, the phase shifted full bridge includes an inductor at the output which commonly causes high conduction loss. In [41], series-connected transformers were used, each acting as a transformer or inductor depending on the switching interval and could be used to replace the output inductor. Other factors that impact the performance of the PSFB are the turns ratio of the transformer, core loss, AC winding loss

and non-zero current switching (ZCS) of the synchronous rectifier devices. This topology uses zero voltage switching (ZVS) for increased efficiency but it is not achievable across the full load range [42]. Efforts to extend the ZVS range include utilizing the adaptive energy stored in components of an auxiliary circuit [43].

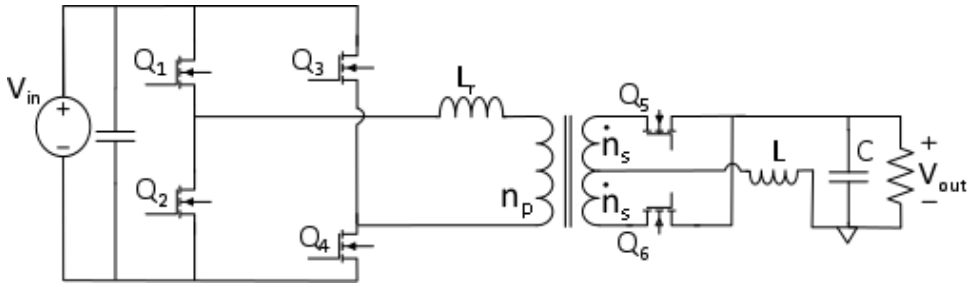


Figure 2.2: Phase-shifted full bridge topology.

2.3 LLC Converter

An additional option for an isolated IBC design is the LLC converter. The LLC converter, depicted in Fig. 2.3, is a popular topology used in DC-DC converters for data center server power supplies [40], telecommunication power supplies [44] and electric hybrid vehicle converters [45]. Compared to the PSFB, the LLC is capable of achieving ZVS over the full load range [46]. By greatly reducing switching loss, the LLC is able to operate at high frequencies to increase power density and reduce the size of the resonant components [47]. Transformer loss is typically the dominant loss mechanism in high-frequency LLC designs [48]. Planar transformers can be used for greater power density but they can introduce other issues such as termination loss that can hinder efficiency [49]. Typical LLC designs range in power levels from 400W to 5kW with efficiencies ranging from 92% to 98% [50] [51] [52] [53] [54].

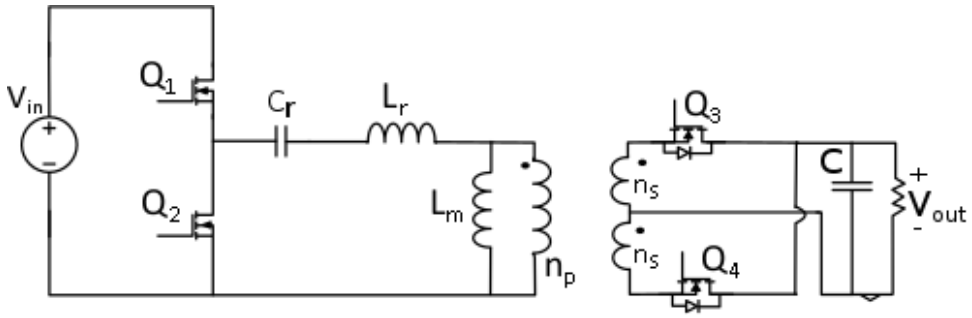


Figure 2.3: LLC topology.

2.4 Switched-Tank Converter

The switched-tank converter (STC), shown in Fig. 2.4 is also a resonant converter. Each of the inductors creates a resonant tank with the capacitors. Compared to the PSFB and LLC, the STC does not use a bulky transformer to step down the voltage. Instead, capacitors are used to step down the voltage. The STC design has been used for data center power supply applications due to its high efficiency, high power density and light-weight. One drawback to the design is it's inability to regulate the output voltage. Furthermore, while the topology component count can be high increasing overall converter costs, the efficiencies achieved are comparable to the LLC. The topology has achieved 98% efficiency for power levels up to 600W [55] [56] [57].

Summary

Fig. 2.5 shows a graphical summary of the articles reviewed in this chapter. The converter efficiencies are compared with their output current. The buck converter design had the lowest efficiency and current capability, followed by the PSFB. The LLC and STC are capable of achieving efficiencies close to 98% at output currents upwards of 50A. The resonant converters are limited by conduction loss of the resonant tank and in the case of the LLC, transformer loss. The design specifications for this IBC are provided in Table 2.1 and the target is included in the graphical summary.

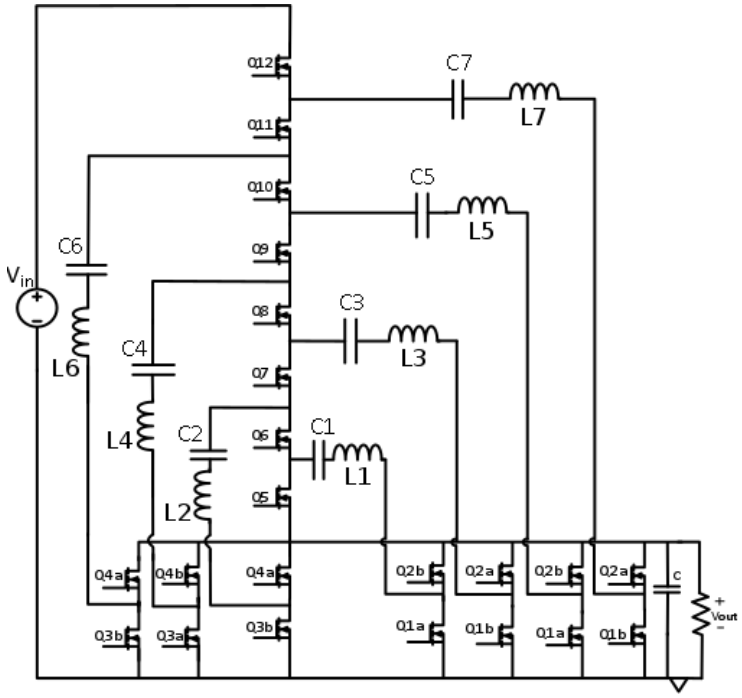


Figure 2.4: Switched-tank capacitor topology.

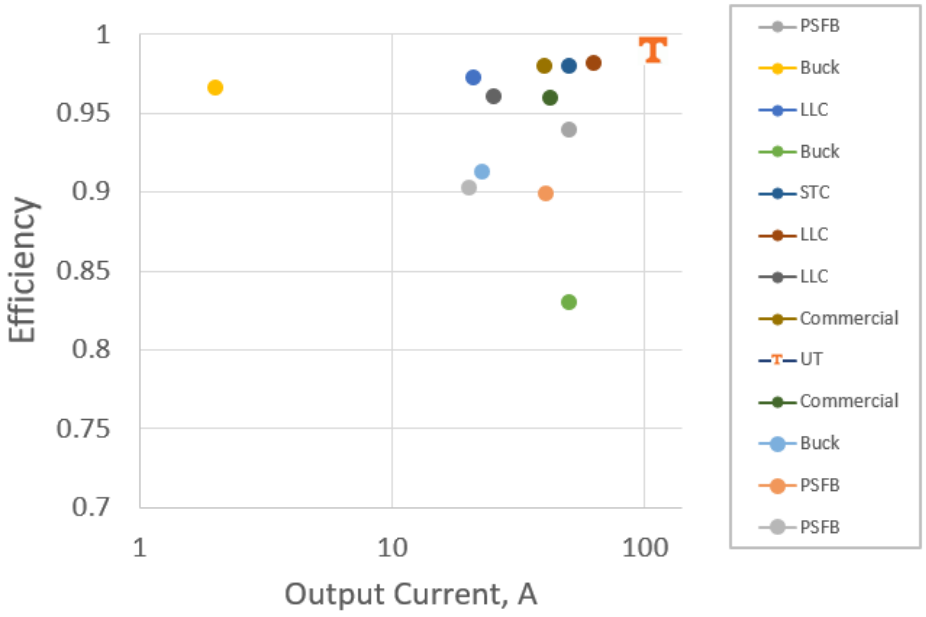


Figure 2.5: Efficiency summary at maximum currents.

Table 2.1: IBC target design specifications.

Design Parameter	Value
DC Input Voltage	$48V$
Output Power	$500W$
DC Output Voltage	$5V$
Output Current	$100A$
Conversion Efficiency	99%
Size	1/8 Brick

2.5 Switched Capacitor Converters

High current applications have long been dominated by resonant converters such as the LLC and phase-shifted full bridge. While such converters are capable of achieving high efficiencies, further improvement of efficiency is strongly linked to specialized magnetic design and manufacturing. Searching for a topology that does not rely on magnetics for energy transfer naturally pushes the designer towards switched capacitor (SC) topologies. With high-power density becoming of greater importance for the power electronics designer, switched capacitor designs offer unique opportunities for increased power density. Conventional switched capacitor topologies include the Ladder, Fibonacci, Dickson, and Series-Parallel. From these traditional designs, other topologies have been introduced such as the multilevel modular capacitor-clamped converter (MMCCC) [58] and flying capacitor multilevel converter (FCMDC) [59].

Switched capacitor converters have been used in a wide range of applications such as low and high power integrated circuits [60, 61, 62], energy harvesting [63], interconnections of offshore wind farms to DC grids [64] and for self-powered signal processing [65, 66]. Limitations of the SC topologies include inherent loss due to voltage mismatch during energy transfer between capacitors that are shorted together and inability to regulate the output voltage.

2.6 Hybrid Dickson Switched Capacitor (HDSC)

The Hybrid Dickson Switched Capacitor (HDSC) Converter is based on the original Dickson switched capacitor topology [61] which will be discussed in depth in Ch. 3. The HDSC is suitable for extreme conversion ratios, has low switch stress [67], reduced magnetic size, provides voltage regulation [68] and increased efficiency using soft-charging [69]. This topology is analyzed, designed and tested for the IBC application and discussed in Chapters 3 and 4.

2.7 Topology Design and Loss Analysis

In this section, the four topologies introduced in Sections 2.1-2.4, the Buck, PSFB, LLC and STC are analyzed and simulated for a loss comparison to the HDSC. The characteristics of the selected passive elements and devices, such as $R_{ds,on}$, C_{oss}, capacitor ESR and inductor DCR, are integrated into the simulation for accurate efficiency calculations. Magnetic loss due to core loss and ac winding loss are calculated separately and included in the loss distribution summary. The loss breakdown for each topology enables insight into the limitations of these converters and used for comparison to the HDSC. The topologies are compared for a 135W design and most of the designs are analyzed at a switching frequency, f_s=1 MHz. In each analysis the power loss distribution and required component list are provided.

2.7.1 Buck Converter Design and Loss Analysis

One of the advantages to the Buck topology is the simple design. It requires two switches, an output inductor, input capacitor and output capacitor. The basic operation and operating waveforms are depicted in Fig. 2.8 along with the operating characteristics in Table 2.2.

Each of the devices, Q_1 and Q_2, are driven with complementary gate-to-source voltage signals. The length of time that Q_1 is ON is related to the duty cycle, D, and conducts current for DT_s, where T_s represents the switching period. Q_2 conducts for the remaining

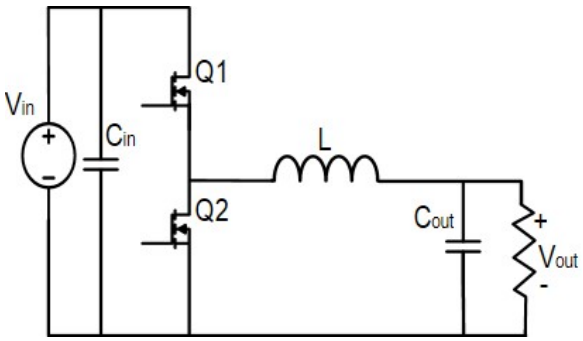
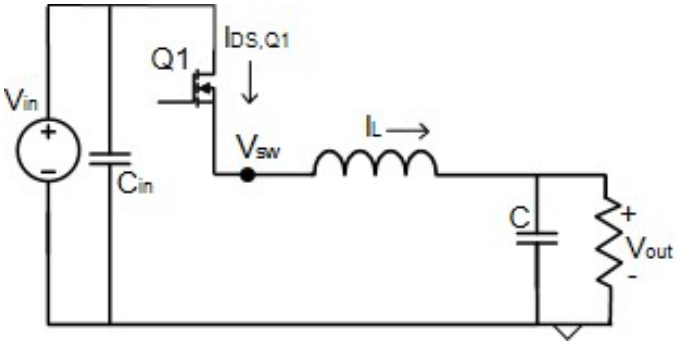


Figure 2.6: Buck schematic.

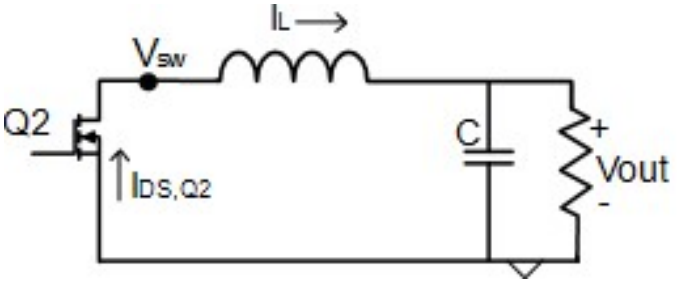
period, $(1-D)T_s$. The duty cycle is determined using the following equation,

$$D = \frac{V_{out}}{V_{in}} \tag{2.1}$$

One of the disadvantages to the buck converter is the high stress that occurs on the hi-side device, Q_1, when operating under a high voltage conversion ratio. This high stress is due to high voltage and peak current, resulting in increased switching loss, such as turn-off loss and overlap loss. Additionally, the high peak currents through the inductor will lead to increased RMS currents, $I_{L,RMS}$, and higher inductor conduction loss. From Eq. 2.1 and the design parameters listed in Table 2.3, the duty cycle is D=.104. This short duty cycle means that Q_1, must transfer the entire power flow of the converter during this short amount of time. The device not only has to block the input voltage but also withstand much higher current levels than the average current that goes through the device. From the simulated buck model, where $L = 4.7\mu H$, I_L=27 A, the average current through Q_1 is 2.8 A. The RMS current through the device is over three times the average current, $Q_{1,rms}$=8.7 A. This high rms current will result in high conduction loss. The simulated drain-to-source voltage, V_{ds}, waveforms for Q_1 and Q_2 are provided in Fig. 2.9. The list of components selected for the buck design are provided in Table 2.4. With regards to cost, when selecting devices, the cost of the device will increase depending on the voltage and current stresses that each device needs to withstand. The discrete device and passive characteristics were integrated into the simulation for an accurate efficiency approximation. The losses of this converter include, conduction loss due to the on-resistance of the devices, $R_{ds,on}$, switching loss due to device



(a) Buck schematic for subinterval 1, DT_s. (b) Buck schematic for Subinterval 2



(b) Buck schematic for Subinterval 2, $(1-D)T_s$.

Figure 2.7: Buck circuit configurations.

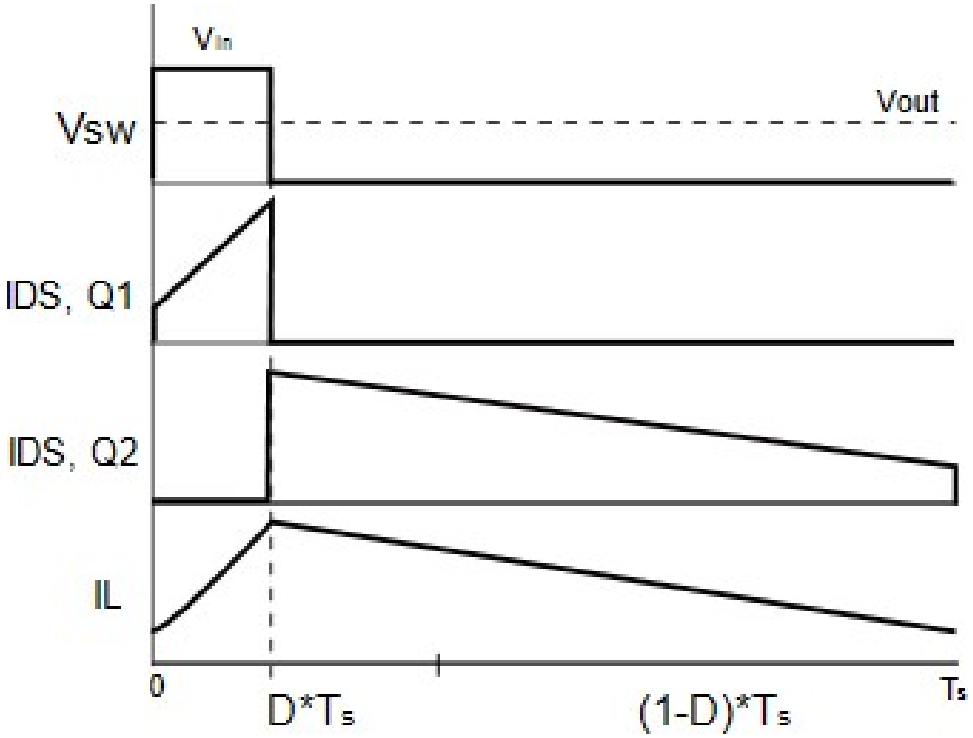


Figure 2.8: Buck operating waveforms.

Table 2.2: Buck Characteristics

Operation Characteristics	Symbol
Conversion Ratio, $\frac{V_{out}}{V_{in}}$	D
Max. Switch Voltage	V_{in}
Max. rectifier voltage	V_{in}
Average Rectifier Current	$I_{out}D$
Switch Utilization	$\frac{V_{out}}{V_{in}}$

output capacitance, conduction loss from the DCR of the output inductor, inductor core loss, inductor ac winding loss and gate charge loss, accounting for the charge required to turn the FET on and off. The conduction loss and output capacitance loss were calculated from the simulation, the core and winding loss were determined using Coilcraft's Power Inductor Analysis and Comparison Tool. The loss distribution is provided in Fig. 2.10. The overall efficiency of the converter was 87.2%. The leading loss is due to the inductor conduction loss from the inductor's parasitic resistance and core loss.

Table 2.3: Buck Simulation Parameters

V_{in}	48V
V_{out}	5V
I_{load}	27A
f_s	1MHz
D	.104

Table 2.4: Values and components for buck design.

Component	Name	Rating	Value
Q_1	EPC2001C	100V, 25A,	$R_{ds,on}$=7mΩ C_{oss}=450pF
Q_2	EPC2023	30V, 60A	R_{dson}=1.3mΩ C_{oss}=2400pF
inductor	XAL1510-472	DCR=3.8mΩ	4.7μH

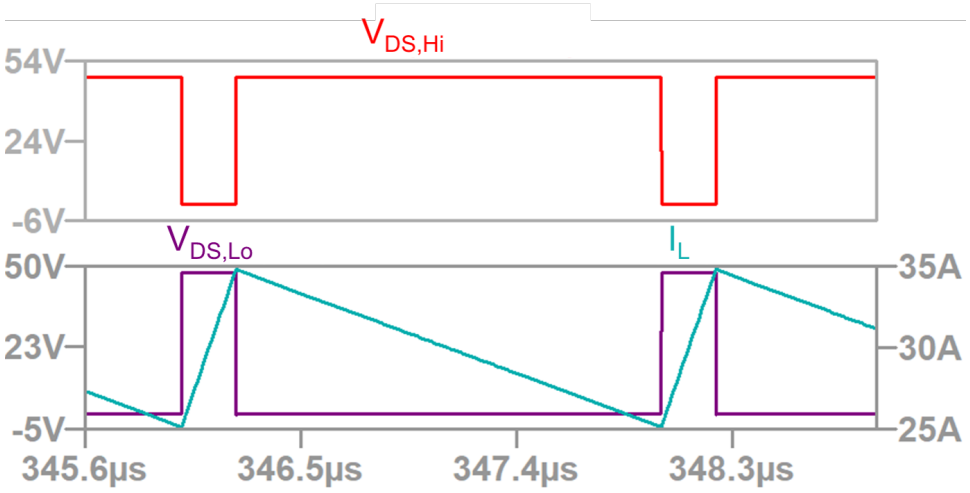


Figure 2.9: SPICE simulated buck waveforms.

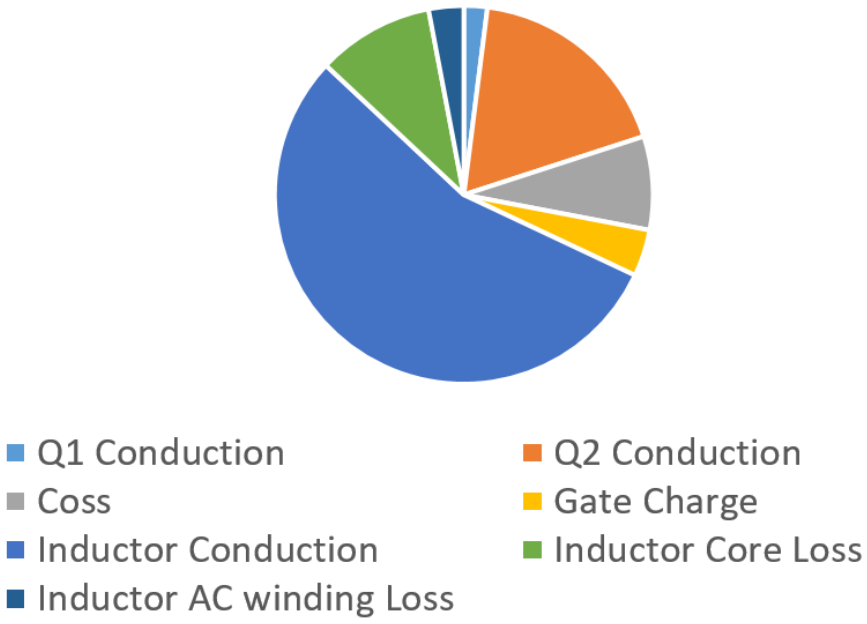


Figure 2.10: Loss distribution of designed buck converter.

Buck Summary

To improve the efficiency of this buck design, multiple devices could be used in parallel to reduce the conduction loss attributed to the device's on resistance and multiple inductors could be used in parallel to reduce the equivalent parasitic resistance of the output inductor. While adding devices in parallel will reduce the conduction loss it will increase the overall volume as well as increase switching losses such as turn-off loss, with every additional device added.

2.7.2 Phase Shifted Full Bridge Design and Loss Analysis

The PSFB design is more complex than the buck converter and requires more components leading to increased overall cost. The components required include four switches on the primary side, a transformer, and two diodes or synchronous switches on the secondary side. The phase shifted-full bridge circuit is provided in Fig. 2.11

The phase shifted gate signals and operational waveforms are provided in Fig. 2.12. The basic operation entails, Q_1 and Q_2 switched at 50% duty cycles and 180° out of phase from

each other. Q_3 and Q_4 follow this same switching scheme and are phase shifted with respect to Q_1 and Q_2. The amount of energy transfered depends on the phase-shift, ϕ, or overlap between the diagonal switches of the Q_1/Q_2 and the Q_3/Q_4 leg. The leakage inductance, L_r resonates with the output capacitance of the devices and enables soft-switching. The synchronous devices on the secondary side act as a current rectifier followed by an output filter. The operating characteristics are provided in Table 2.5.

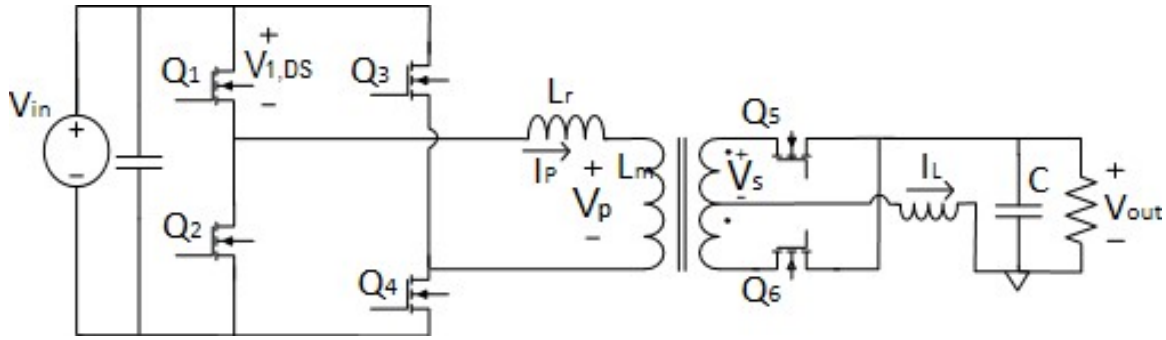


Figure 2.11: Phase shifted full bridge circuit.

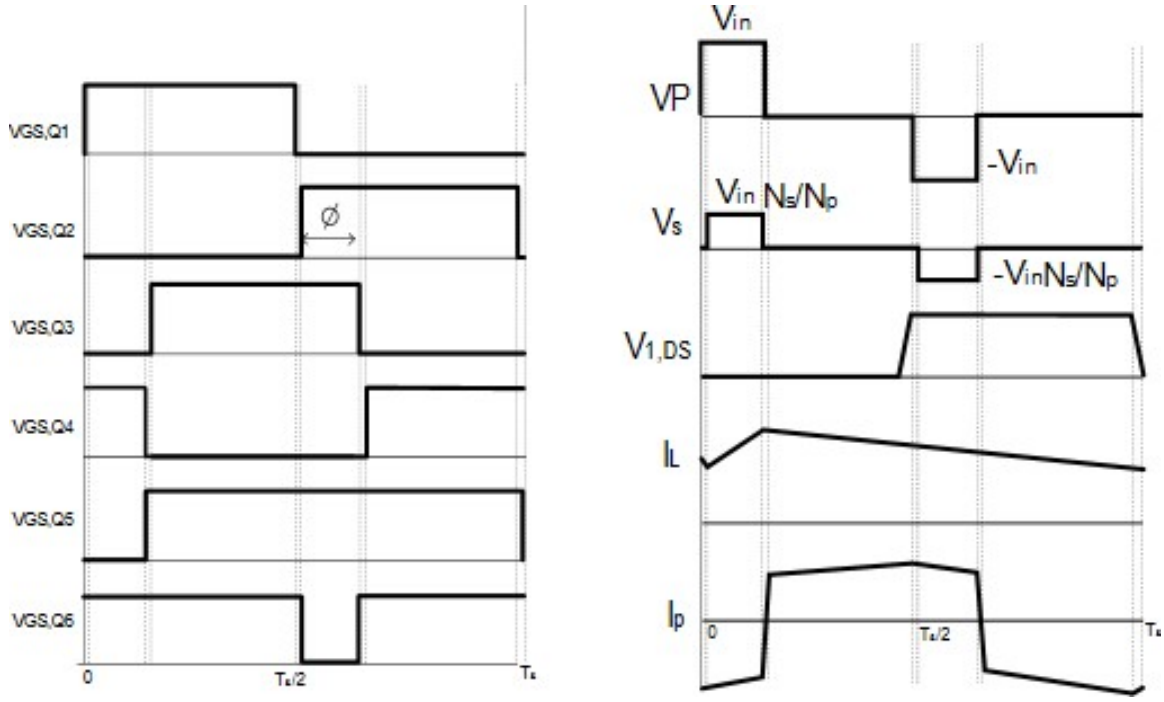


Figure 2.12: Phase shifted full bridge waveforms.

Table 2.5: Phase shifted full bridge characteristics.

PSFB Converter Operation Characteristics	
Conversion Ratio	$\frac{N_s}{N_p}\frac{V_{out}}{V_{in}}$
Pri. Side Max. Switch Voltage	V_{in}
Pri. Side Peak Switch Current	$I_{out}\frac{N_s}{N_p}$
Max rectifier Voltage	$V_{in}\frac{N_s}{N_p}$
Average Rectifier Current	$\frac{(I_{out})}{2}$

When considering the PSFB design for a high output current application it is mandatory to replace the secondary side diode rectification with synchronous devices. This is due to the forward voltage drop, V_F of each diode. The losses caused by the forward voltage drop of the diode current rectification can greatly impact the overall efficiency. Loss due to the forward voltage drop of a diode rectifier can be calculated using Eq. 2.2.

$$P_{V_F} = V_F I_F \tag{2.2}$$

At high output currents, losses become detrimental to proper operation.

$$P_{synch.} = I^2 R_{ds,on} \tag{2.3}$$

In [**?**] the $R_{ds,on}$ losses due to the synchronous rectifiers, calculated using Eq. 2.3 and switching losses of the synchronous FETs are shown to be less compared to loss from the forward voltage drop of the secondary rectifiers.

The leakage inductance of the transformer is leveraged to achieve zero voltage switching (ZVS) on all of the primary side devices by resonating with the output capacitance of the primary side devices. The resonant tank, consisting of the device output capacitance and transformer leakage inductance, is used to position zero volts across the switching device eliminating any loss due to simultaneous overlap of the switch current and voltage at each transition. It should be noted that ZVS is not achievable across the full load range, but is limited to the bounds of minimum output load and maximum input line voltage [42]. The duty cycle of the PSFB is determined by

$$D_{PSFB} = \frac{nV_{out}}{V_{in}} \tag{2.4}$$

Comparing Equation 2.4 to Equation 2.1 for the buck, the duty cycle is extended by the turns ratio, n. Assuming a phase shift of $\phi = .4$, the turns ratio of the transformer $\frac{N_s}{N_p}$, can be solved by

$$\frac{N_s}{N_p}\phi = \frac{V}{Vg} \tag{2.5}$$

From Equation 2.5 and the simulation parameters of Table 2.6 the turns ratio is approximately n=.25. Proper dead-time, dt, must be included in order for the converter to achieve ZVS this can be determine using the resonant frequency of the magnetizing inductance, L_m and output capacitance, C_{oss} of the primary side devices using the following equation,

$$f_r = \frac{1}{2\pi\sqrt{L_m 2C_{oss}}} \tag{2.6}$$

$$dt \geq \frac{\pi}{2}\sqrt{L_m(2C_{oss})} \tag{2.7}$$

Using the parameters provided in Table 2.6 and the selected discrete components listed in Table 2.7, the design is verified in simulation. The results are provided in Fig. 2.13. The overall efficiency for the 135W design is 89.3%. The PSFB loss distribution is provided in Fig. 2.14.

Table 2.6: PSFB Simulation Parameters

V_{in}	48V
V_{out}	4.89V
I_{load}	28.9A
f_s	1MHz
D	.365
C_r	100nF
$N_s : N_p$	4:1

Table 2.7: Components for Phase Shifted Full Bridge Design

Component	Value	Rating	Characteristics
Q1, Q2, Q3, Q4	EPC2031	60V, 48A	$R_{ds,on}$=2.6mΩ C_{oss}=940pF Q_g=16nC
Q5, Q6	EPC2023	30V, 60A	$R_{ds,on}$=1.3mΩ C_{oss}=2400pF Q_g=19nC
Transformer	coilcraft-RA7040	4:1	DCR_{pri}=10.75mΩ DCR_{sec}=4.25mΩ L_m=.55μH
Output inductor	coilcraft-SER2915L-222	2.2uH	DCR=2.5mΩ

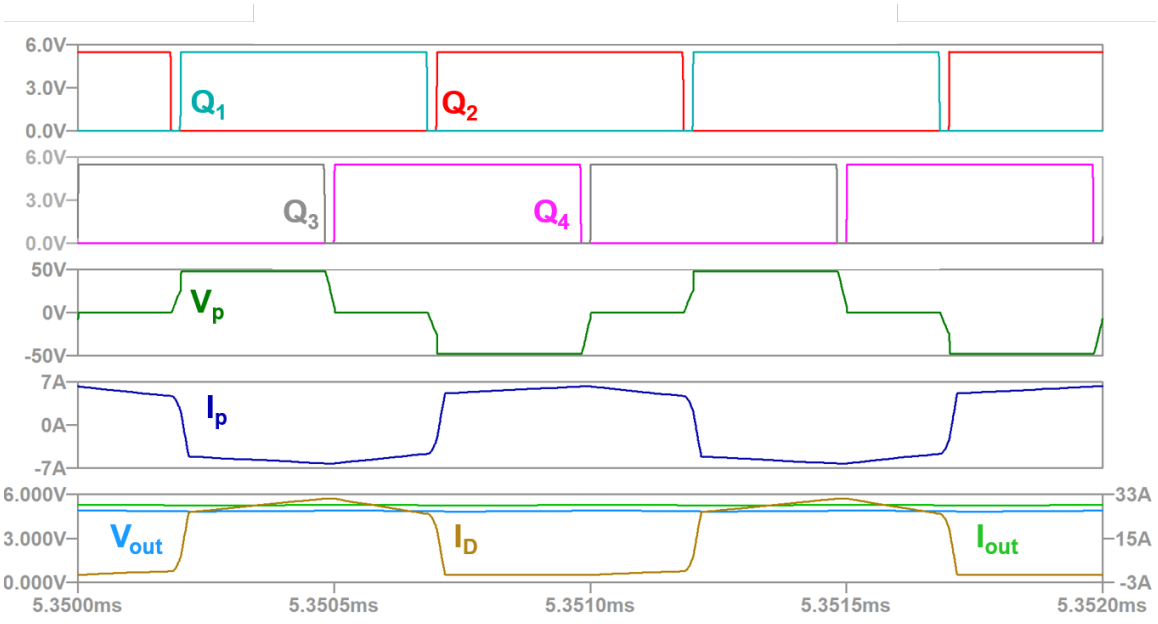


Figure 2.13: PSFB simulated waveforms.

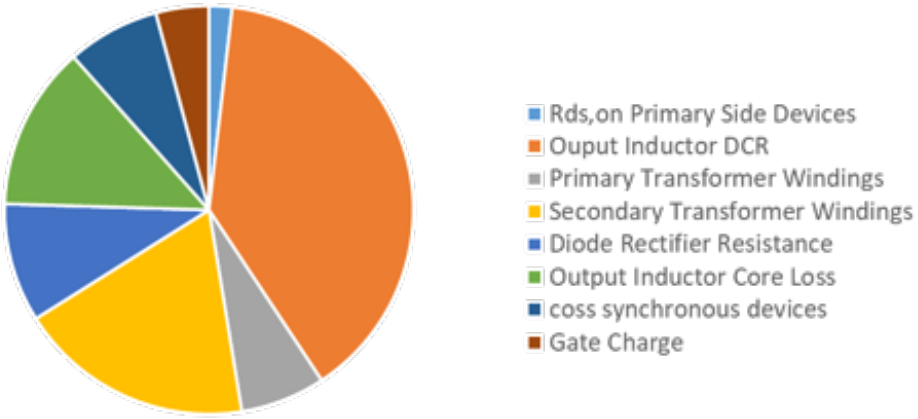


Figure 2.14: Simulated PSFB loss breakdown.

PSFB Summary

The loss distribution shows that over half of the losses are related to the output inductor and the transformer. Similar to the buck converter multiple inductors could be used in parallel to decrease conduction loss at the output, however power density will be reduced.

2.7.3 LLC Design and Loss Analysis

The LLC converter, illustrated in Fig. 2.15, is a widely used design that is capable of achieving high efficiencies for a wide load range. One advantage the LLC has in comparison to the PSFB is its ability to achieve soft-switching for all of the switching devices over the full load range where as the PSFB is limited in operation for maintaining ZVS. Due to the low switching losses of the LLC, the converter is able to operate at higher switching frequencies and can therefore use smaller passive components for increased power density. Additionally, in comparison to the PSFB which suffers from high-order harmonics on the secondary side currents requiring a large output inductor to reduce the current ripple, the LLC has the advantage of not needing an output inductor and can further increase its power density in comparison to the PSFB [70] [71].

The LLC is a resonant converter, obtaining regulation through frequency modulation not pulse-width modulation. Compared to the PSFB the LLC requires the same amount of switches with the option to implement a half or full bridge on the primary or secondary. In this design a half bridge, Q_1 and Q_2, is designed on the primary and synchronous switches, Q_3 and Q_4 are used on the secondary. As stated previously, each of the switches can achieve soft-switching enabling the LLC to operate at higher switching frequencies for increased power density. While the design of the converter is more complicated in comparison to the buck or PSFB, the basic operation shown in Fig. 2.15, is simple. Q_1 and Q_2 operate complimentary and generate a square wave voltage across the resonant tank. The reactive components, L_r and C_r, generate a sinusoidal current. The sinusoidal current is then rectified by the synchronous devices on the secondary side and sent through a low pass filter to the output. Zero-voltage switching is achievable on all devices and zero current switching (ZCS) is achievable on the secondary side devices. The resonant circuit is comprised of the primary side inductance, L_m, leakage inductance of the transformer, L_r and the device output capacitance, C_r. In order to reduce the size of the magnetics high frequency operation is needed. The disadvantage of operating at high frequencies however is this leads to increased AC loss in the magnetics. Other drawbacks of the transformer include core loss heating, large footprint and expensive implementation costs. For designs that include planar transformers, cost can by high due to multilayer PCBs and cutouts for transformer pieces. The loss breakdown of the LLC include the synchronous rectifier conduction loss, transformer loss, primary side conduction loss and resonant tank conduction loss.

The LLC was simulated using the characteristics for the selected devices listed in Table 2.8. The operating point and simulation parameters for the LLC design is provided in Table 2.9. The simulated waveforms are provided in Fig. 2.16. The overall efficiency for the 141W design was 95.6%.

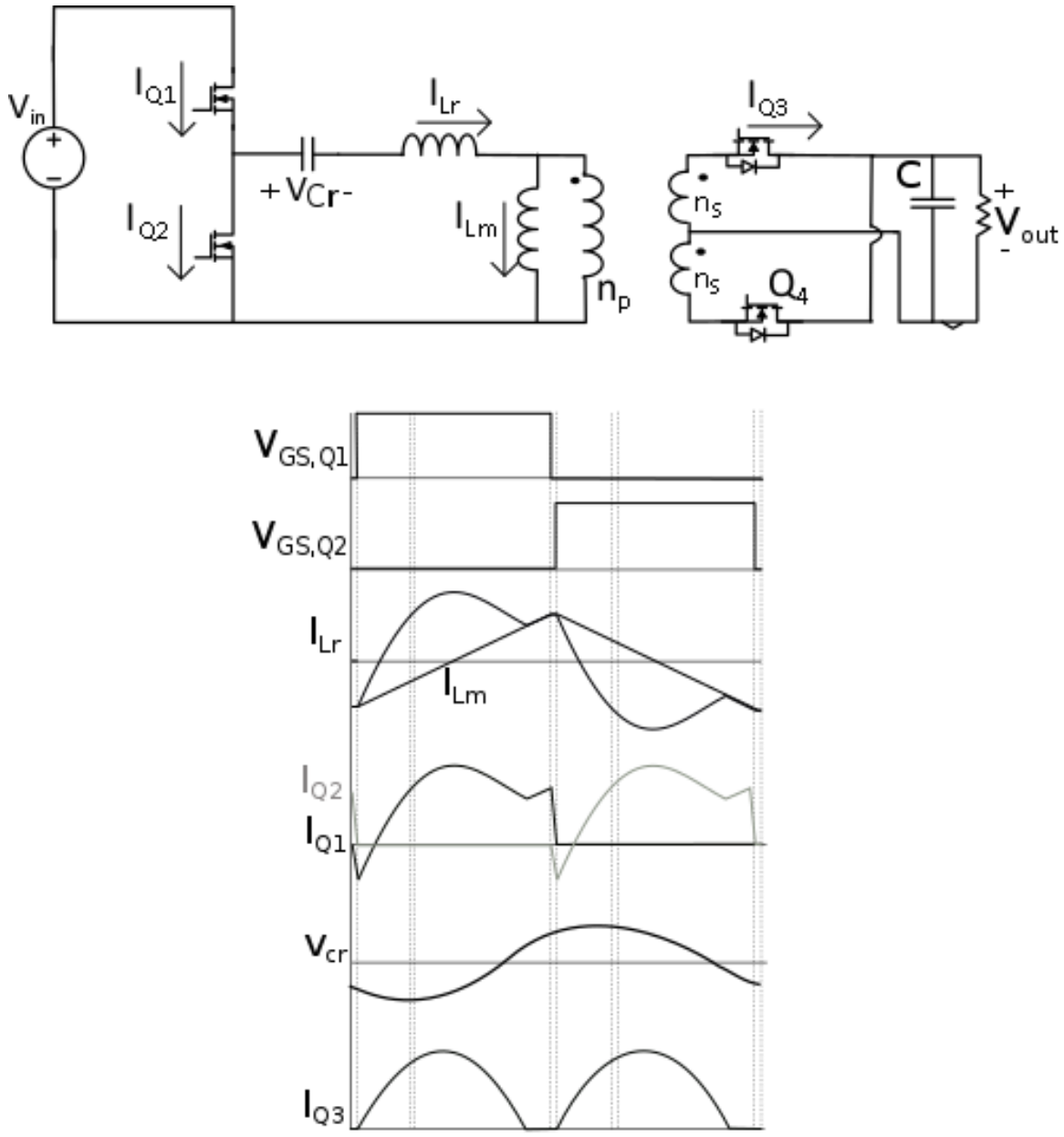


Figure 2.15: LLC operating waveforms.

Table 2.8: Components for LLC Design

Component	Name	Rating	Characteristics
Q_1, Q_2	EPC2031	60V, 48A	$R_{ds,on}$=2.6mΩ C_{oss}=940pF Q_g=16nC
Q_3, Q_4	EPC2023	30V, 60A	$R_{ds,on}$=1.3mΩ C_{oss}=2400pF Q_g=19nC
C_r	Murata-$GCM21BR72A104KA37K$	100nF	100V, X7R, ESR=30mΩ
L_r	coilcraft-$XEL6030-28ME$	280nH	DCR=2.1mΩ
transformer	coilcraft-$POE120PL-33$	24:5	DCR=5mΩ

Table 2.9: LLC simulation parameters.

V_{in}	48V
V_{out}	4.89V
I_{load}	28.9A
f_s	1MHz
Lr	280nH
Cr	100nF
$N_s : N_p$	24:5

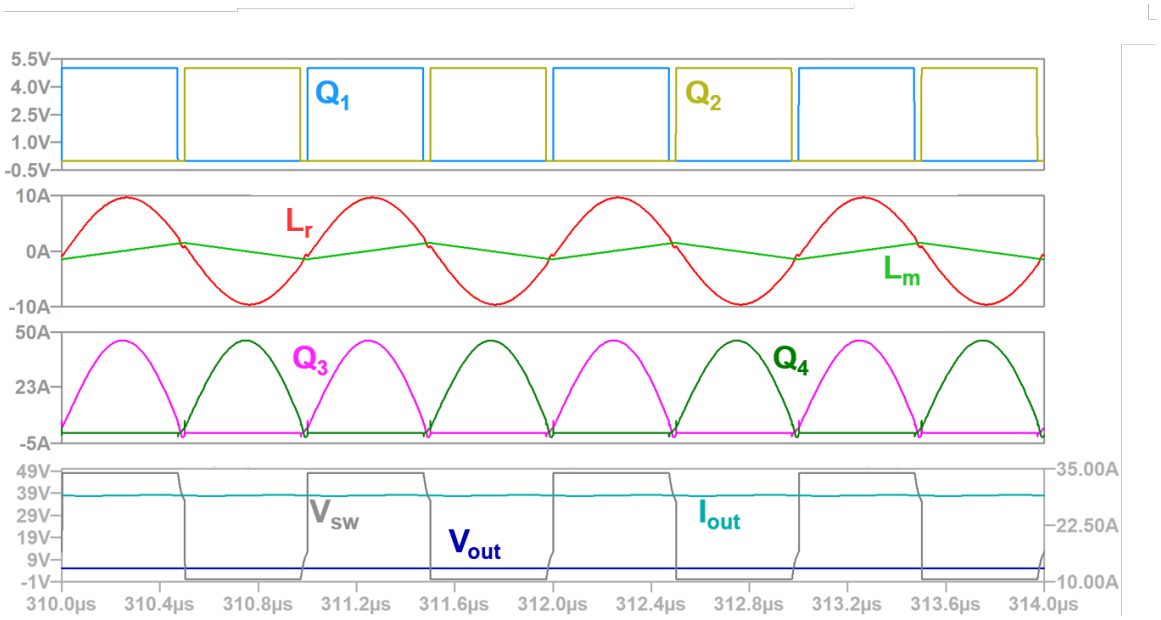


Figure 2.16: LLC simulated waveforms.

Summary of LLC

The simulated LLC loss breakdown in Fig. 2.17 shows that the transformer and the synchronous secondary devices are the largest contributors of loss. In [72] a matrix transformer is used with enhanced termination loop for the synchronous rectifier using a non uniform winding structure. AC losses such as proximity effect, skin effect and termination loss can be improved through magnetic manufacturing [73] [74] [75].

2.7.4 Switched Tank Design and Loss Analysis

The advantage that the STC has over the previous topologies, is it does not require a large output inductor or bulky transformer. The disadvantage is that the STC requires many more switches than the previous designs. However, each device has low voltage stress helping to reduce switching loss. While no transformer is needed, small inductors are used to create resonant currents. The sinusoidal resonant currents enable zero-current switching. While many switches are needed the switching scheme is simple, each half-bridge operates with complimentary gate signals that are 180 deg out of phase. The circuit subintervals and corresponding waveforms are provided in Fig. 2.18.

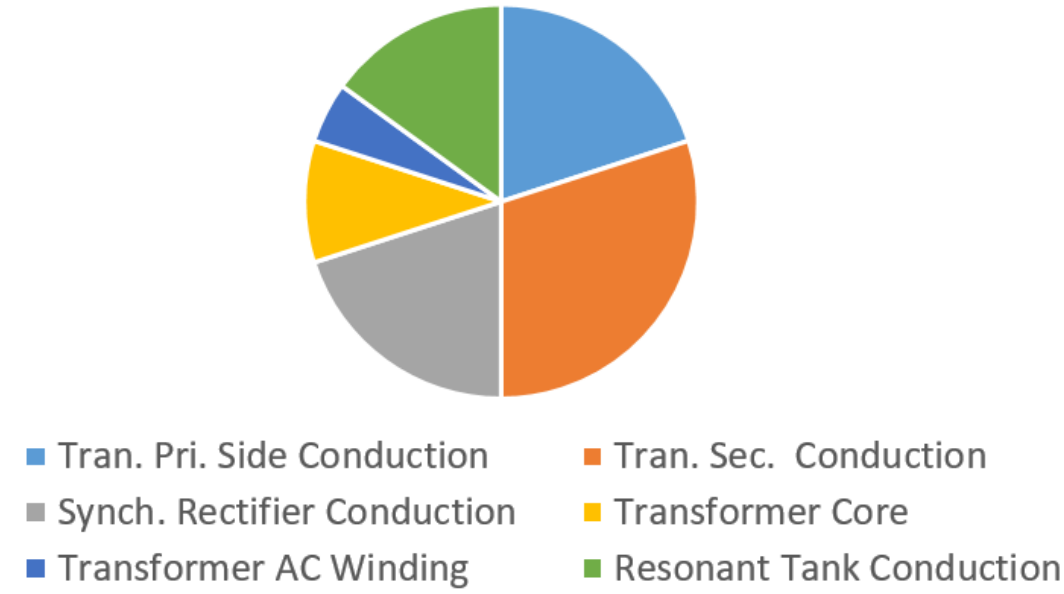


Figure 2.17: LLC loss distribution.

The resonant frequency is determined using Equation 2.8. The resonance occurs between the capacitor and inductor in series in each branch.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{2.8}$$

Using the discrete devices used in Table 2.11, the STC topology was simulated and the corresponding waveforms are provided in Fig. 2.19 with a summary of the simulated waveforms given in Table 2.10. The overall efficiency for the 179W design is 93.6%.

STC Summary

The loss breakdown in Fig. 2.20 shows that the combined conduction loss of the resonant tank capacitors and devices are the dominant loss mechanism. This can be improved by paralleling more capacitors for a decreased equivalent ESR, but will require re-design of the resonant tank and switching frequency. Furthermore, added capacitors will decrease power density and increase the design cost.

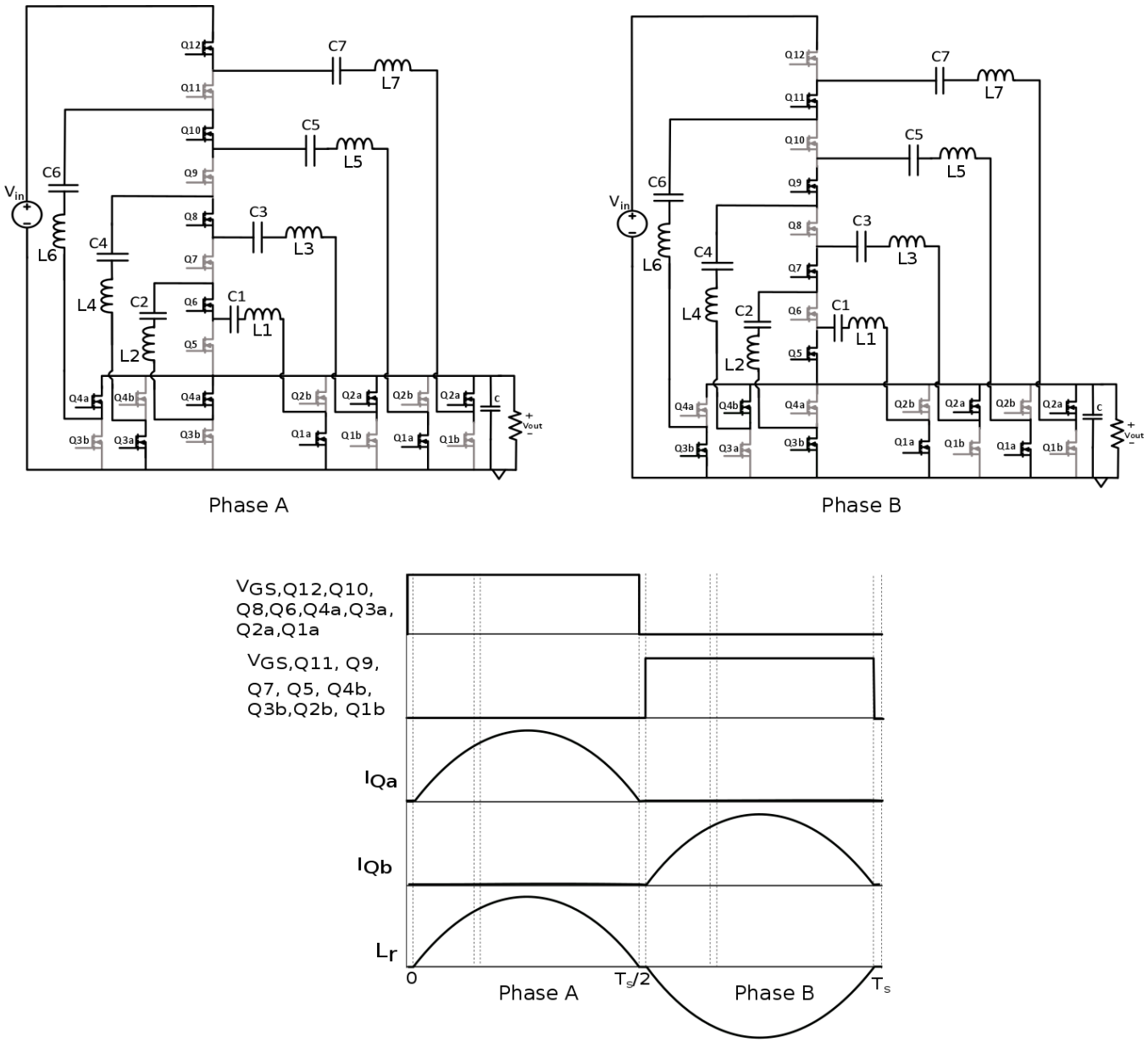


Figure 2.18: Switched-tank converter subintervals and waveforms.

Table 2.10: STC Simulation Parameters

Simulated Parameters	
V_{in}	48V
V_{out}	5.87V
I_{load}	28.7A
f_s	328kHz
$I_{Q11,pk}$	11.9A
$I_{Q11,rms}$	5.9A

Table 2.11: Components for STC Design

Component	Value	Rating	Characteristics
GaN device	EPC2023	30V, 60A	$R_{ds,on}$=1.3mΩ C_{oss}=2400pF Q_g=19nC
C_r	C3225X7S2A475K200AB	4.7μF, 100V	X7S, ESR=5mΩ
L_r	LP02-500-1S	50nH, 50A	DCR=.22mΩ

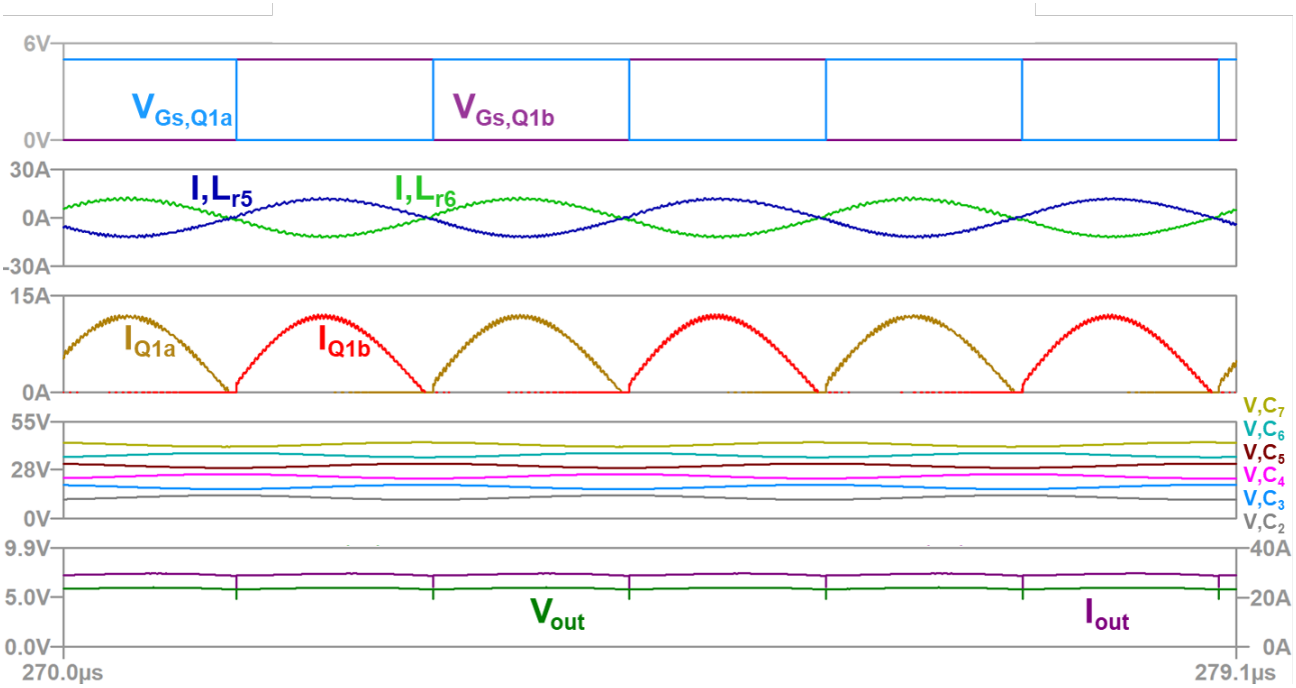


Figure 2.19: STC simulated waveforms.

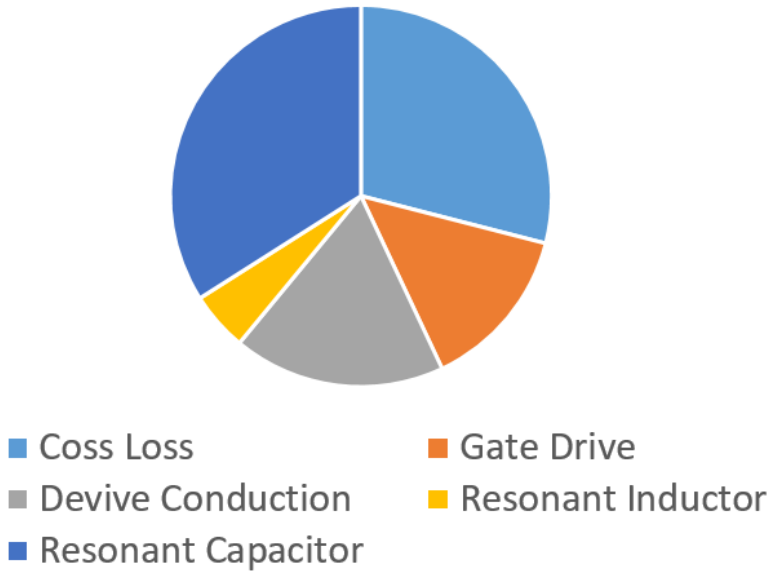


Figure 2.20: STC simulated waveforms.

2.7.5 Topology Comparison and Summary

While the designed buck converter required the fewest number of devices, the efficiency was the lowest. For the buck design a large inductor was needed to reduce the inductor current ripple. Due to the large inductance the series resistance was high as well causing high conduction loss of the output inductor. While the PSFB has better efficiency the greatest loss is similarly attributed to the output inductor series resistance. The resonant converters eliminate the need for an output inductor and instead conduction losses for the resonant tank largely contribute to the overall power loss. For this high output current application, series resistance from magnetics, whether at the output or in the resonant tank are a common loss mechanism across each of the converters simulated.

Chapter 3

Switched Capacitor Converters

SC converters use capacitors to store and transfer energy instead of inductors. The energy storing capacitors, commonly called flying capacitors, C_{fly}, transfer power by alternately connecting the source to the load or another capacitor. The following sections cover the fundamentals of switched capacitor circuits and their inherent loss.

3.1 Energy Density of Capacitors

Today's capacitor dielectric materials allow capacitors to exceed the power density of inductors [76]. In [77], a detailed analysis of available surface mount discrete components was performed and the results show that capacitors have substantially higher energy and power density than inductors. For example, a 1μF T-Y Ceramic capacitor was 149x more energy dense than the 10μH Coilcraft SMT inductor it was compared to. Fig. 3.1 compares the energy density of shielded inductors and ceramic capacitors, confirming that capacitors can provide increased energy density [78].

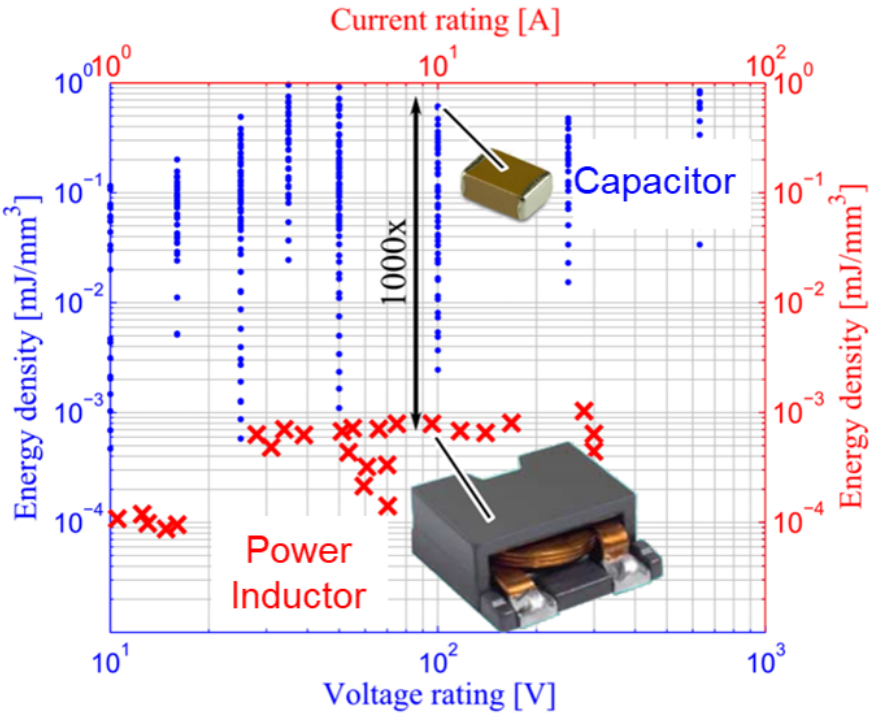


Figure 3.1: Energy density comparison of ceramic capacitors and inductors [4].

3.2 Ideal Simplified Switched Capacitor Model

A simplified model for the switched capacitor converter is presented in Fig.3.2 [**?**]. The ideal SCC model uses a transformer to represent the voltage conversion and an output impedance representing the losses and output variation. For switched capacitor converters, the output impedance is a measure of performance and power loss.

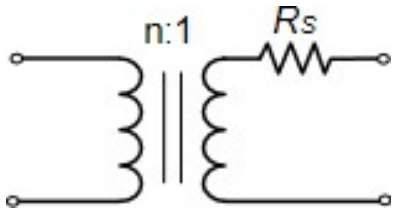


Figure 3.2: Basic Model for a switched capacitor converter.

The transformer turns ratio represents the unloaded conversion ratio of the converter. When the ideal converter is connected to a load, there is a voltage drop across R_s, due to charge transfer and conduction loss.

There are two asymptotic limits to R_s, the slow switching limit, SSL and the fast switching limit, FSL. The ideal SSL and FSL output impedance asymptotes along with the corresponding capacitor current wave-shapes, are plotted in Fig. 3.3. For SSL, the capacitors are able to fully equilibrate during each switching cycle and the charge transfer is impulsive, resulting in high current spikes. When a SC converter is operating in the SSL region, R_s is determined by switching frequency and capacitance. For the FSL region of operation, when the switching frequency exceeds the critical frequency, f_{crit}, the output resistance becomes independent of frequency. The capacitor voltages remain constant due to the nature of high switching frequency and current flow is constant. When operating in FSL, R_s is determined by the device on-resistance, $R_{ds,on}$, capacitor ESR and other parasitic resistances in the charge transfer path [79]. The optimal design is at the intersection of the SSL and FSL. The analytical expressions for the output impedance for the two operating regions of a SCC are provided in Equations 3.1 and 3.2. The charge flow coefficient for each capacitor and switch, $a_{r,i}$, correspond to charge flows that occur immediately after the switches are closed to initiate each respective phase of the SC and are derived in [5].

$$R_{SSL} = \sum \frac{(a_{r,i})^2}{C_i f_{sw}} \tag{3.1}$$

$$R_{FSL} = 2 \sum R_i((a_{r,i})^2 \tag{3.2}$$

Charge sharing determines R_{SSL} so the next section will analyze the effects of charge-sharing and the losses that are inherent for operation in the SSL region.

3.3 Hard-Charging Loss

As stated in the previous section when operating in SSL, hard-charging losses are the dominant loss mechanism. In this section a basic capacitor charge sharing scenario and the inherent loss is described.

Hard charging loss, also known as charge sharing loss, occurs when two capacitors, or a voltage source and a capacitor, with a difference in voltage, ΔV_{diff}, are shorted together. The basic capacitor charging scenarios are provided in Fig. 3.4.

As stated in [6], after the switch is closed between the two capacitors in Fig. 3.14b, "The capacitor voltage can not change instantaneously and the mismatch of the initial capacitor voltage will be present across the series resistance, R_s, resulting in a large instantaneous current," as shown in Fig. 3.5. This can be described analytically in Equation 3.3. Where C_{eq} is the equivalent series and parallel capacitance seen at the output.

$$I_C = \frac{\Delta V_{diff}}{R_s} e^{\frac{-t}{R_s C_{eq}}} \tag{3.3}$$

Due to the voltage difference, ΔV_{diff}, the rate of change in voltage across the capacitor is extremely high causing the current in the capacitor, I_c to be very high with a decay rate related to the time constant of the series resistance, R_s and capacitance, C_{eq}.

Assuming that the time constant, $\tau = R_s C_{eq} \ll T_s$, such that the converter is operating in the SSL region, the power loss for hard-charging for the scenarios of Fig. 3.4 can be related

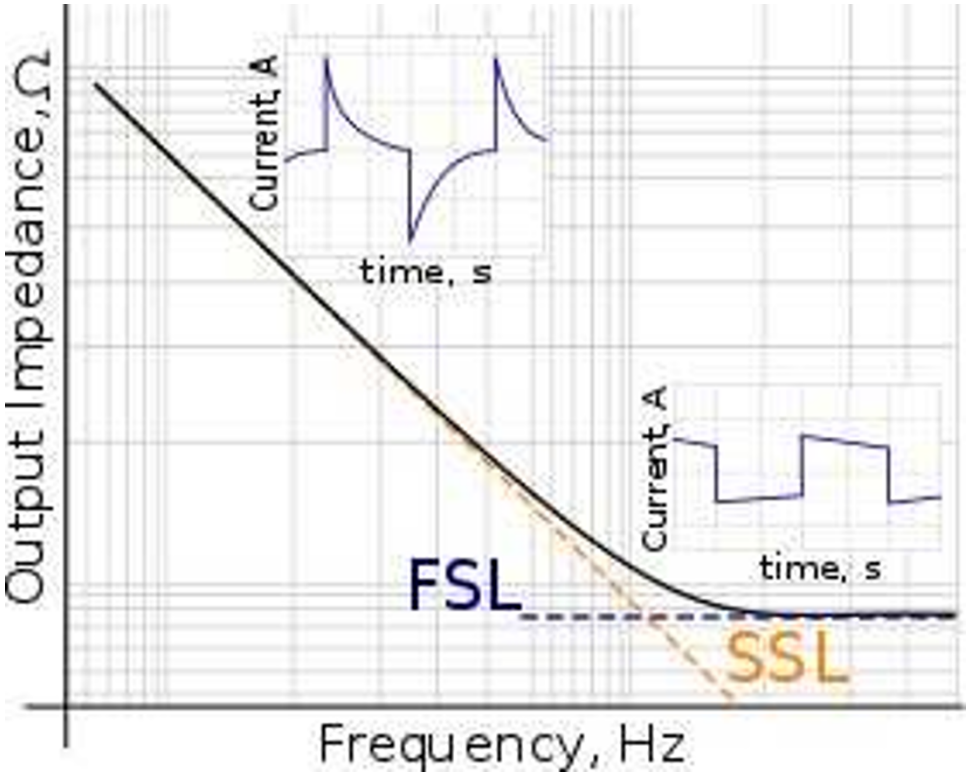
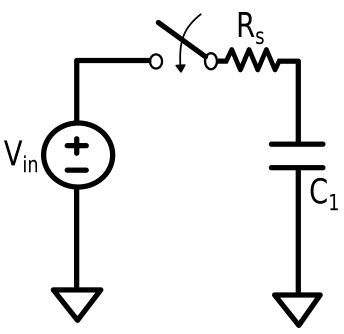
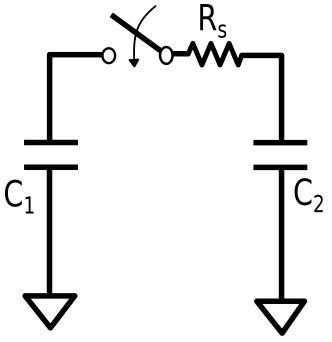


Figure 3.3: Output impedance vs. switching frequency [5].



(a) Voltage source charging capacitor.



(b) Capacitor charging capacitor.

Figure 3.4: Basic capacitor charging scenarios.

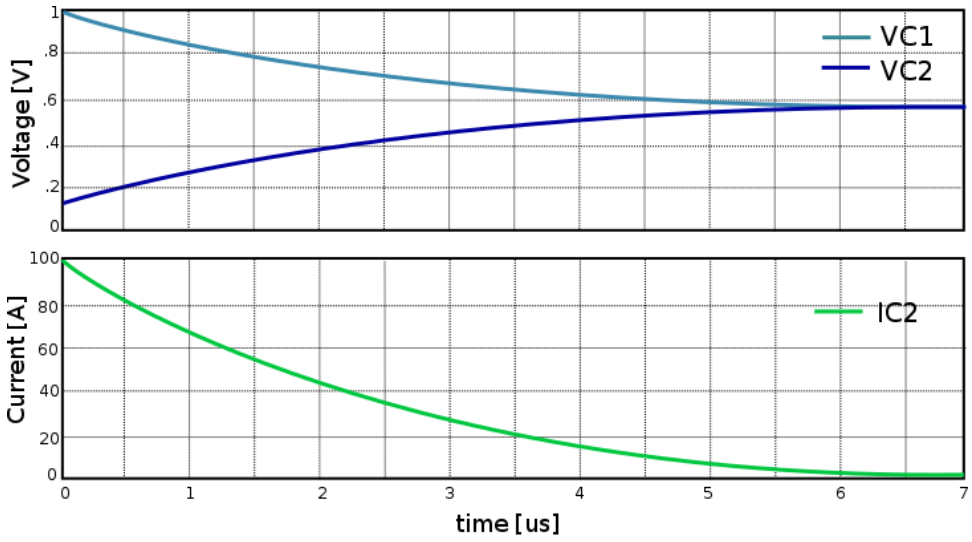


Figure 3.5: Capacitor voltages and current waveforms in the charge redistribution process [6].

to the average current, I_{avg}. The average current can be calculated using Equations 3.4 to Equation 3.7.

$$\frac{d(Q)}{dt} = I_{avg} \tag{3.4}$$

$$I_{avg} = C_1 \frac{(V_{in} - V_1)}{T_s} = \frac{C_1 \Delta V}{T_s} \tag{3.5}$$

$$R_{eq} = \frac{\Delta V}{I_{avg}} = \frac{T_s}{C_1} = \frac{1}{f_s C_1} \tag{3.6}$$

$$P_{HC} = \frac{(\Delta V)^2}{R_{eq}} = f_s C_1 (\Delta V)^2 \tag{3.7}$$

Notice that this inherent charge transfer loss does not depend on the series resistance, R_s. Therefore, a lower $R_{ds,on}$ or decreased parasitic resistance will only result in an increased current spike over a shorter time, but the total power loss in each charge cycle will remain the same [80]. Instead the change in energy stored in the capacitors and the losses of the charging process are a function of the voltage mismatch, ΔV_{diff}, and capacitance.

For a constant current load where I_{rms}=I_{avg}, the mismatch is related to how much charge each capacitor transfers in the previous subinterval of the switching period. The voltage mismatch is proportional to the load current or the charge drawn from the load and inversely proportional to the capacitor values. Using the relationship between voltage and current in

a capacitor,

$$I_C = C\frac{dV}{dt} \tag{3.8}$$

equations 3.9 and 3.10, presented in [6] summarize the relationship between the capacitor voltage difference, switching frequency and capacitance. From Equation 3.10 we see that for a constant capacitor current, losses due to hard-charging can be decreased by increasing the switching frequency, f_s or the capacitance, C_{fly}. While a higher f_s would allow smaller passives to be used, drawbacks of increasing the switching frequency or capacitance include, increased switching loss, difficulty with control, achieving precise timing intervals, increased capacitor size and increased cost.

$$\Delta V \propto \frac{1}{f_s}, \frac{1}{C_{fly}} \tag{3.9}$$

$$P_{loss} \propto \frac{1}{f_s}, \frac{1}{C_{fly}} \tag{3.10}$$

Therefore, it is desirable to minimize the capacitor voltage mismatch, ΔV, without increasing f_s or C_{fly} [6]. This is achieved with the ideal hybrid Dickson switched capacitor topology and will be addressed in a later section.

3.4 Dickson Topology

The hybrid Dickson switched capacitor circuit is derived from the original Dickson topology [61]. The 4:1 Dickson topology, provided in Fig. 3.6 has two switching intervals which will be referred to as phases. Each phase lasts half of the switching period. The corresponding gate signals for the circuit are provided in Fig. 3.7. The simplified circuits for subintervals 1 and 2, are provided in Fig. 3.8. The characteristics of the Dickson topology design are described in Table 3.1. The basic operation of the Dickson Converter is summarized below.

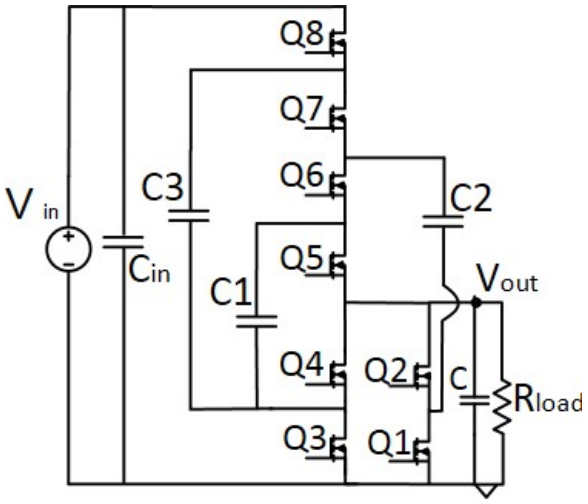


Figure 3.6: 4:1 Dickson Topology

Table 3.1: Dickson Converter Characteristics

Conversion Ratio	$n+1$
Capacitors	n
Switches	$n+5$

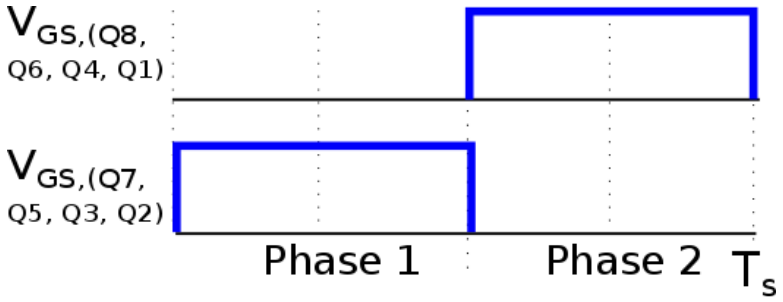
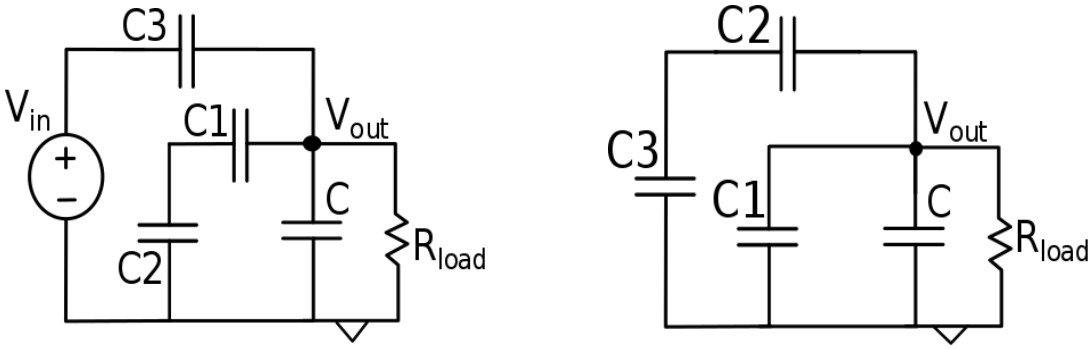


Figure 3.7: Gate signals for 4:1 Dickson Converter



(a) Phase 1 **(b)** Phase 2

Figure 3.8: 4:1 Dickson topology for each phase of the switching period.

Subinterval 1

Q_1, Q_4, Q_6 and Q_8 turn-on and the input voltage, V_{in} charges C_3. C_2 discharges into C_1. Each branch discharges to the load.

Subinterval 2

Q_2, Q_3, Q_5 and Q_7 turn-on and the previously on switches turn-off. C_3 is now connected in series to C_2. C_1 is connected to the load, in parallel with the branch containing C_2 and C_3. C_3 which was just charged in the previous subinterval, discharges into C_2 which discharges to the load. In a parallel branch C_1 also discharges to the load.

Advantages and Limitations of the Dickson

One advantage of the Dickson switched capacitor converter is its low switch stress [81] [82]. The bottom switches, $Q_1 - Q_4$, are rated for V_{out} while the upper switches, $Q_5 - Q_8$ are rated for $2V_{out}$. Admittedly, other switched capacitor circuits such as the ladder topology, also have similar switch utilization, but the ladder topology requires more flying capacitors and is therefore less appealing for the design [83]. Limitations to the Dickson include it's inability to regulate the output voltage [6] and low capacitor utilization [84]

. Regarding voltage regulation, instead of being able to regulate the output voltage, the conversion ratio is fixed, and is determined by the circuit topology. This results in loss as the load changes. Capacitor utilization [82] provides a way to quantify the capacitor's ability to effectively utilize energy. The constraint can be calculated as

$$E_{tot} = \sum_i \frac{1}{2}(V_{C,i(rated)})^2(C_i) \tag{3.11}$$

where C_i is the value of the capacitor and $(V_{C,i(rated)})$ is the voltage rating of the capacitor. A capacitor's utilization, or energy storage capability, is related to the voltage rating which corresponds to the volume and price of the capacitor [82]. To decide whether switch utilization should take priority over capacitor utilization the cost of devices and capacitors can be considered. Since capacitors are less expensive than devices it was decided that switch utilization should be higher in order to reduce converter cost.

Each of the flying capacitors in the Dickson converter requires a different voltage rating related to a fraction of the input voltage. The capacitor voltage ratings for the 4:1 are provided in Table 4.1. The capacitor DC bias is derived using the charge-flow voltage vector in a later section. In Section 3.3, the impact on efficiency due to hard-charging loss was

Table 3.2: 4:1 Dickson Capacitor Voltage Rating

Component	Rating
C_3	$\frac{3V_{in}}{4}$
C_2	$\frac{V_{in}}{2}$
C_1	$\frac{V_{in}}{4}$

introduced. To determine whether a circuit can achieve soft-charging, where hard-charging losses are eliminated, KVL equations in each interval must be satisfied at all times [85] including during phase transitions. In the original Dickson, since the output capacitance does not allow instantaneous change in the output voltage, the KVL equations can not be satisfied for each phase. As a result, there is a mismatch in capacitor voltage during each phase transition. This mismatch causes high transient currents as demonstrated in Fig. 3.5. This is characteristic of a converter operating in the slow switching limit, where efficiency is dominated by voltage mismatch losses and result in low efficiency [86].

Original Dickson Topology Summary

The Dickson converter has the advantage of low switch stress and the disadvantage of low capacitor utilization and hard-charging loss. The next section will discuss steps that can be taken in order to eliminate the hard-charging loss.

3.5 Reducing Hard-Charging Loss by Adding an Output Inductor

The premise behind soft-charging is to add an element that can absorb the voltage mismatch between capacitors and control the capacitor current without transferring ohmic loss from

the original element to the new element [81]. Therefore, by incorporating one or multiple magnetics into switched capacitor topologies, high-current transients caused by voltage mismatch between capacitors can be reduced and higher efficiencies can be achieved. There are two ways to incorporate magnetics into SC topologies and they are listed below.

Cascaded Second Stage

One method to integrate magnetics into a switched capacitor topology is to cascade a magnetic based second-stage converter. A simple model of this topology is illustrated in Fig. 3.9. In this example, a switched capacitor converter is followed by a magnetic converter for ripple reduction and better regulation. The magnetic stage acts as a controlled current load and reduces loss caused by voltage mismatch [87]. This method has the advantage of simple design and low cost.

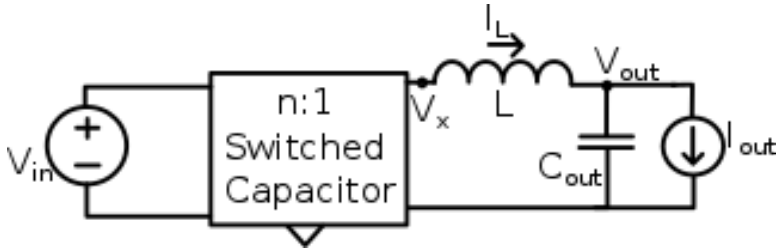


Figure 3.9: Direct Energy Transfer

Integrated Magnetics for Resonance with Flying Capacitors

The second method uses multiple inductors in series with the flying capacitors to create a resonant switched capacitor circuit (ReSC). The simplified model is provided in Fig. 3.10. This type of topology is able to achieve zero current switching (ZCS) and increase overall

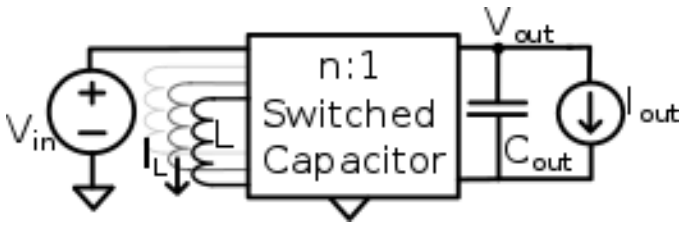


Figure 3.10: Indirect Energy Transfer

efficiency [6]. This method is used in the STC topology introduced in section 2.7.4. There is a subtle difference between these two methods and as shown in [85] [87], even with a single inductor added to the output the SC converter can operate as a ReSC as well as using the direct energy transfer method.

The Dickson topology is suitable for the cascaded second stage since each branch of capacitors is connected to the load. The inductor is placed before the output capacitor and reduces hard-charging loss by allowing the output voltage to vary. The output capacitor is still needed because there is nothing to maintain the output voltage with only a current source. Otherwise, if an output capacitor was not used in parallel with the load the voltage ripple would become quite large. The updated 4:1 Dickson topology is provided in Fig. 3.11. The operating modes are provided in Fig. 3.12. A simplified circuit model is depicted in Fig. 3.13 where a constant current source replaces the constant voltage source, discharging the capacitor [7]. When the switch closes, a majority of the voltage mismatch will occur across the current source and not the series resistance.

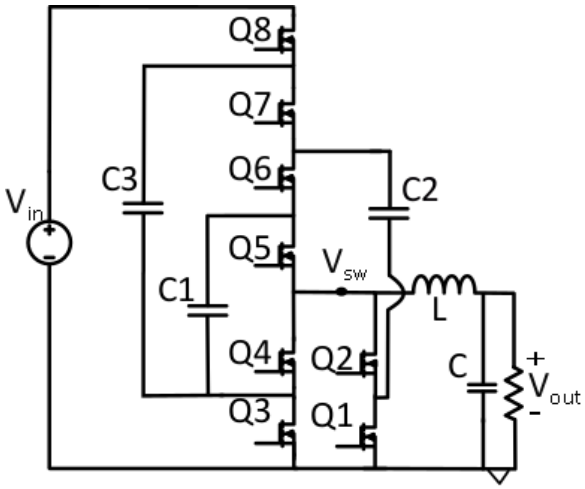
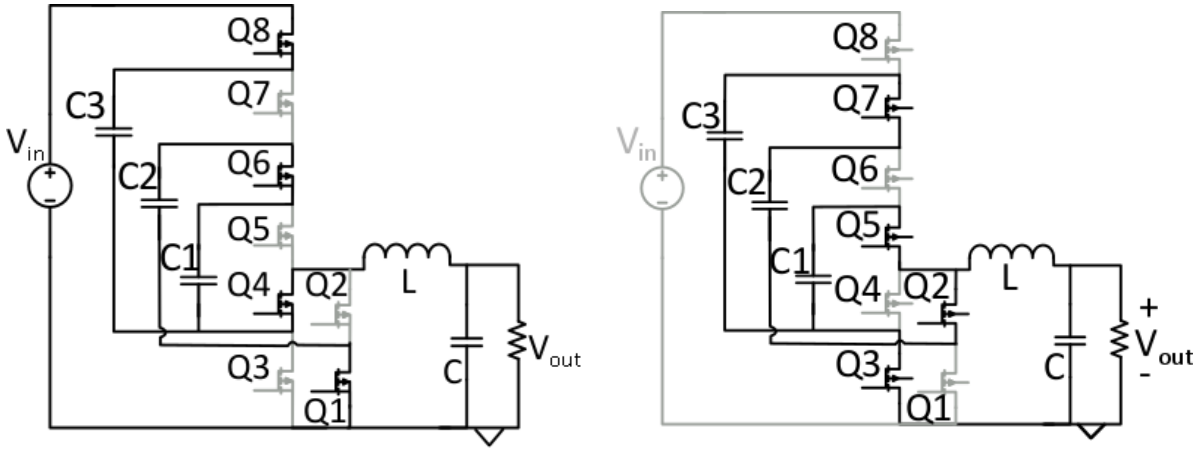


Figure 3.11: 4:1 Dickson with soft-charging capability.

In order to determine whether the Dickson with an added output inductor can achieve complete soft-charging the analysis presented in [5] shows that complete soft-charging can not be achieved. In this analysis, Kirchoff's Voltage Law (KVL) and Kirchoff's Current Law (KCL) are used to solve for the voltage and charge flow vectors. The results from this analysis for the 4:1 Dickson topology with an added inductor suggest that C_2 must have



(a) Phase 1

(b) Phase 2

Figure 3.12: Circuit configurations for the 4:1 Dickson.

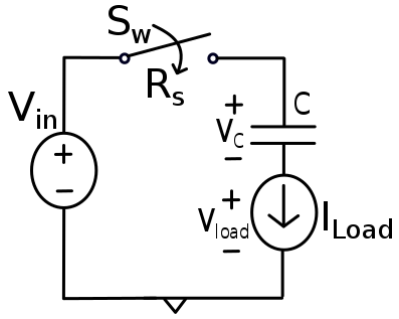
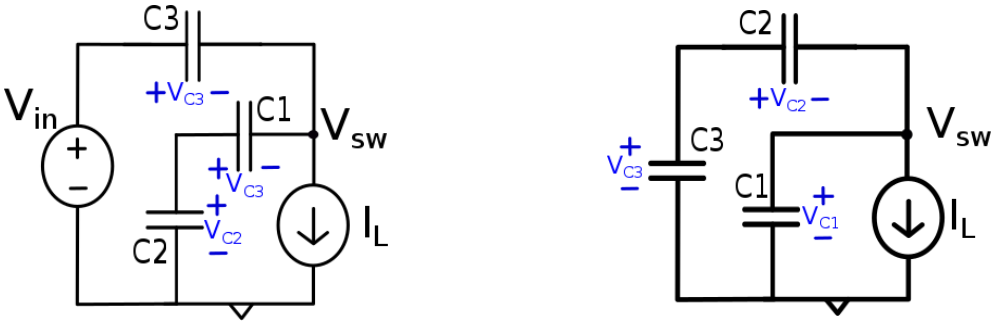


Figure 3.13: Capacitor discharged by a constant current load.

and infinite capacitance. Since it is impossible for C_2 to have an infinite capacitance, these results show the Dickson topology can only *approach* complete soft-charging as long as C_2 is much larger than C_1 and C_3. While the constant current source mitigates the mismatch at the output, there is still a mismatch between the parallel capacitor connections. The next section discusses how the timing of each interval can be leveraged in order to eliminate the remaining hard-charging occurring between the parallel branches.



(a) Phase 1 **(b)** Phase 2

Figure 3.14: KVL 4:1 Dickson Modes of Operation

The reduced loop matrices for each subinterval, used in the analysis in [5], can also be used to determine the DC bias of each flying capacitor as given in Table 4.1. The voltage matrices can be determined by using the polarities of the voltages used for KVL in each subinterval. The corresponding simple circuits for each subinterval, or phase, is provided in Fig. 3.14. The corresponding KVL equations for each of the phases are:

Phase 1

$$V_{in} - V_{C3} - V_{sw} = 0 \tag{3.12}$$

$$V_{C2} - V_{C1} - V_{sw} = 0 \tag{3.13}$$

Phase 2

$$V_{C3} - V_{C2} - V_{sw} = 0 \tag{3.14}$$

$$V_{C1} - V_{sw} = 0 \tag{3.15}$$

The corresponding reduced loop matrices for phases 1 and 2 are then combined to form the matrix used in Equation 3.16. The flying capacitor voltages are found by multiplying the inverse of the 4x4 voltage matrix by a constant V_{in}. The matrix solution is the flying capacitor voltage in terms of V_{in}.

$$\begin{pmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{out} \end{pmatrix} = \begin{pmatrix} 0 & 0 & -1 & -1 \\ -1 & 1 & 0 & -1 \\ 0 & -1 & 1 & -1 \\ 1 & 0 & 0 & -1 \end{pmatrix}^{-1} V_{in} \tag{3.16}$$

$$\begin{pmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{out} \end{pmatrix} = \begin{pmatrix} 1/4 \\ 1/2 \\ 3/4 \\ 1/4 \end{pmatrix} V_{in} \tag{3.17}$$

3.6 Complete Soft-Charging for the HDSC

In the previous section it was determined that while adding an inductor to the output of the Dickson topology reduces the hard-charging loss, it does not eliminate it. Therefore, more analysis is needed in order to achieve complete soft-charging.

Due to the asymmetry of the 4:1 Dickson topology, the voltage ripple across the outer most capacitor, C_3, and innermost capacitor, C_1, are not equal in Phase 1 and Phase 2. Assuming a constant load current, I_{out}, means that a constant current through each capacitor can be assumed as well. With an equivalent capacitance between each of the flying capacitors, the voltage ripple will be proportional to the impedance in each branch. The outer branch consisting of V_{in} and C_3 has a lower impedance than the inner branch of C_2 and C_1. Therefore, the constant load current will not be distributed equally between each branch.The voltage across C_3 during Phase 1 is linear and can be calculated using Equation 3.18.

$$V_{C3,Phase1}(t) = \frac{I_{C3}(t)}{C_3} = \frac{2I_{out}}{3C} \tag{3.18}$$

The voltage ripple across C_3 will increase faster than the voltage ripple of the inner branch consisting of C_2 and C_1 in series. In the next phase when C_3 is in series with C_2 the current through the branch will be less than it was in the previous phase, such that,

$$\frac{dv}{dt}_{C3,Phase1} > \frac{dv}{dt}_{C3,Phase2} \tag{3.19}$$

Therefore, it is not possible for the system of KVL-based equations, which imply the flying capacitors are balanced (i.e. $V_{in} - V_{C3} = V_{C2} - V_{C1}$), to be satisfied during each of the phase transitions and capacitor charge sharing loss is inevitable between the parallel capacitor branches. This is demonstrated in the simulation of the combined capacitor voltages in each branch. The simulation is provided in Fig. 3.15 where it is clear that there is still a mismatch between the capacitor voltages during phase transitions.

To eliminate the voltage mismatch between parallel capacitor branches, two additional phases are added to allow each branch with larger impedance additional time to reach the same ΔV as the lower impedance branch. These additional phases are named "*split*

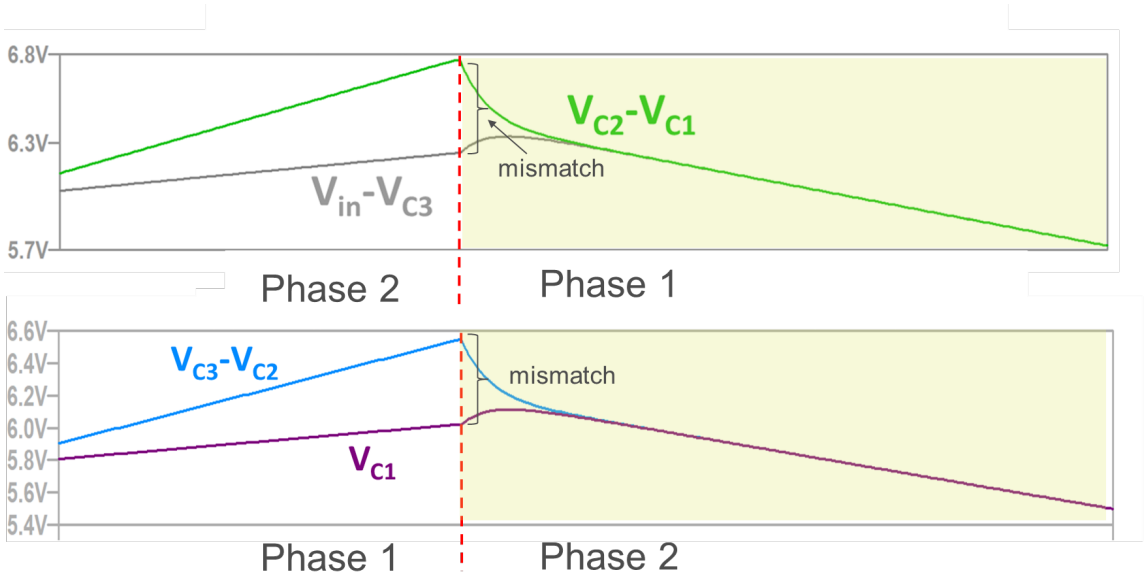


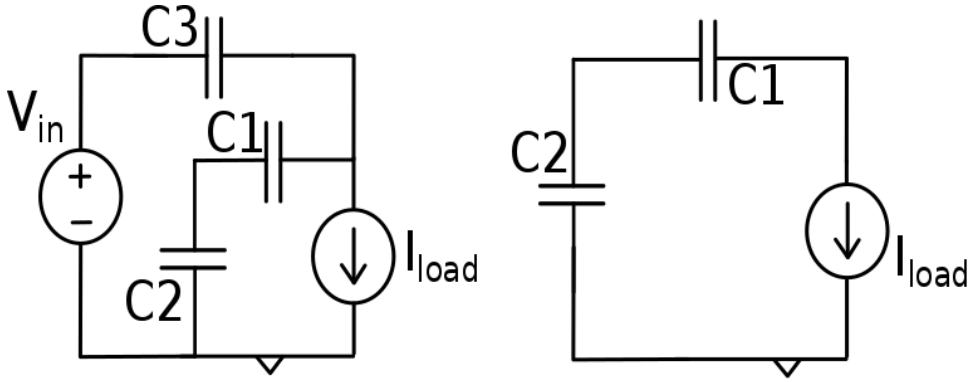
Figure 3.15: Voltage mismatch between branches during phase transitions.

phases" in [69]. The method for determining the split-phase intervals is derived in [69] and will be reviewed in this section. The simplified circuits for the split-phase intervals are provided in Fig. 3.16. The circuit topology remains the same as the Dickson with a constant current source, however the switching sequence changes. The updated switching sequence is provided in Fig. 3.17. By incorporating Phases 1b and 2b, the parallel branches with a lower impedance have additional time to ramp voltage down until the voltage mismatch reaches zero. Once the voltage mismatch reaches zero, the next phase of the period can begin. The length of time required for the split phase interval can be calculated using charge vector analysis and is related to the native conversion ratio, N. Switching loss will not increase because these switches were used in the original design and are turned-off earlier in comparison to the circuit that does not implement the split phase intervals.

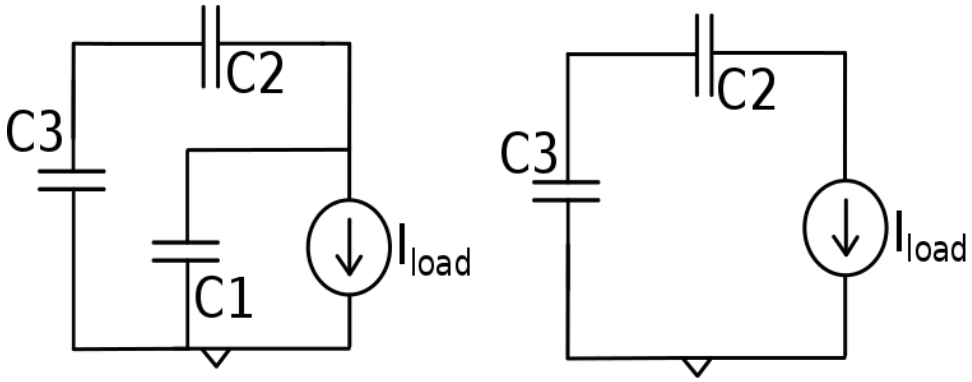
Determining Timing for Split-Phase Interval

To determine the timing of the split phase intervals current division can be applied to the simple circuits. For Phase 1a the equivalent capacitance in the inner loop is

$$C_{inner} = C_2||C_1 = \frac{C_2 C_1}{C_1 + C_2} \tag{3.20}$$



(a) Phases 1a and 1b



(b) Phases 2a and 2b

Figure 3.16: 4:1 Dickson simplified circuit configurations for each interval within the switching period with additional split phases.

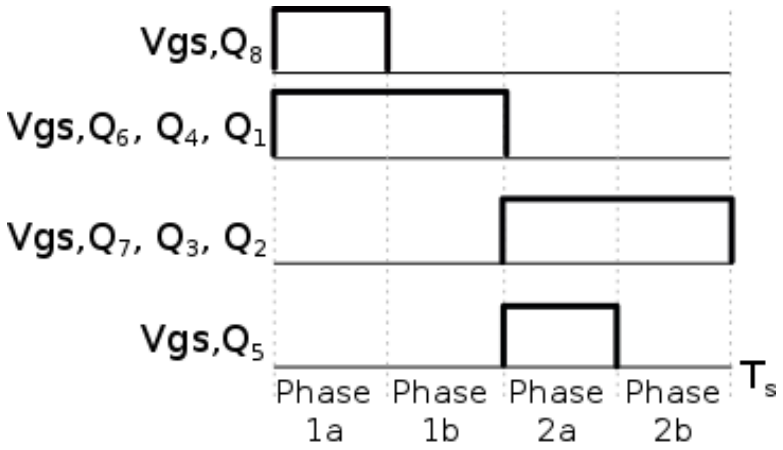


Figure 3.17: 4:1 Dickson gate signals operating with added split phase intervals.

The current will distribute through each branch based on the ratio of the capacitance.

$$I_{inner} = \frac{C_{inner}}{C_3} I_L \tag{3.21}$$

$$I_{inner} + I_{outer} = I_L \tag{3.22}$$

$$I_3 = (1 - \frac{C_{inner}}{C_3}) I_L \tag{3.23}$$

Using the relationship between current and voltage in a capacitor,

$$I_C = C\frac{dv}{dt} \tag{3.24}$$

and assuming steady state operation, equations for the ideal voltage waveforms can be determined. The steady state flying capacitor voltage over one switching period are provided in Equations 3.25-3.28. The voltage mismatch for each flying capacitor can then be solved in terms of T_s and is pictured in Fig. 3.18.

$$\Delta V_{C3_{Ts}} = \frac{2I_L}{3C}(t_{1a}) - \frac{I_L}{3C}(t_{2a}) - \frac{I_L}{C}(t_{2b}) = 0 \tag{3.25}$$

$$\Delta V_{C2} = \frac{-I_L}{3C}(t_{1a}) - \frac{I_L}{C}(t_{2a}) + \frac{I_L}{3C}(t_{2a}) + \frac{I_L}{C}(t_{2b}) = 0 \tag{3.26}$$

$$\Delta V_{C1} = \frac{I_L}{3C}(t_{1a}) + \frac{I_L}{C}(t_{1b}) - \frac{2I_L}{3C}(t_{2a}) = 0 \tag{3.27}$$

$$t_{1a} + t_{1b} + t_{2a} + t_{2b} = T_s \tag{3.28}$$

The capacitor voltage ripple equations can be solved and the timing intervals for the 4:1 Dickson in terms of T_s are given below:

$$t_{1a} = \frac{3}{8}T_s \tag{3.29}$$

$$t_{1b} = \frac{1}{8}T_s \tag{3.30}$$

$$t_{2a} = \frac{3}{8}T_s \tag{3.31}$$

$$t_{2b} = \frac{1}{8}T_s \tag{3.32}$$

$$\tag{3.33}$$

The timing for the split phase interval will change depending on how many flying capacitors there are. As the conversion ratio increases the split phase interval approaches 1/4 of the timing of the original interval.

For this design the split phase intervals will occur after each of the original phases. The additional phases can theoretically occur before or after the original phase, however if in the order 1b-1a-2b-2a, there will be a negative V_{ds} across some of the switches due to the large voltage ripple during the operation and additional blocking devices would need to be added [69]. This would not only increase the complexity but also reduce the efficiency. Therefore, for physical implementation the split phases should be performed in the ordering of 1a-1b-2a-2b.

Split Phase Dickson Summary

In summary, hard-charging losses are inherent to switched capacitor circuits operating in SSL. Hard-charging between capacitors results in a large current spike. To eliminate hard-charging loss there are two requirements. The first is that a constant load current must be added to the output to enable the output to change instantaneously. The second requirement is that there is no mismatch between the parallel capacitor branches between phase transitions. This can be achieved by implementing the split-phase intervals, 1b and 2b. The simulated waveforms for the capacitor current I_{C2} and V_{sw} voltage for each of the topologies previously discussed (original Dickson, Dickson with output inductor and

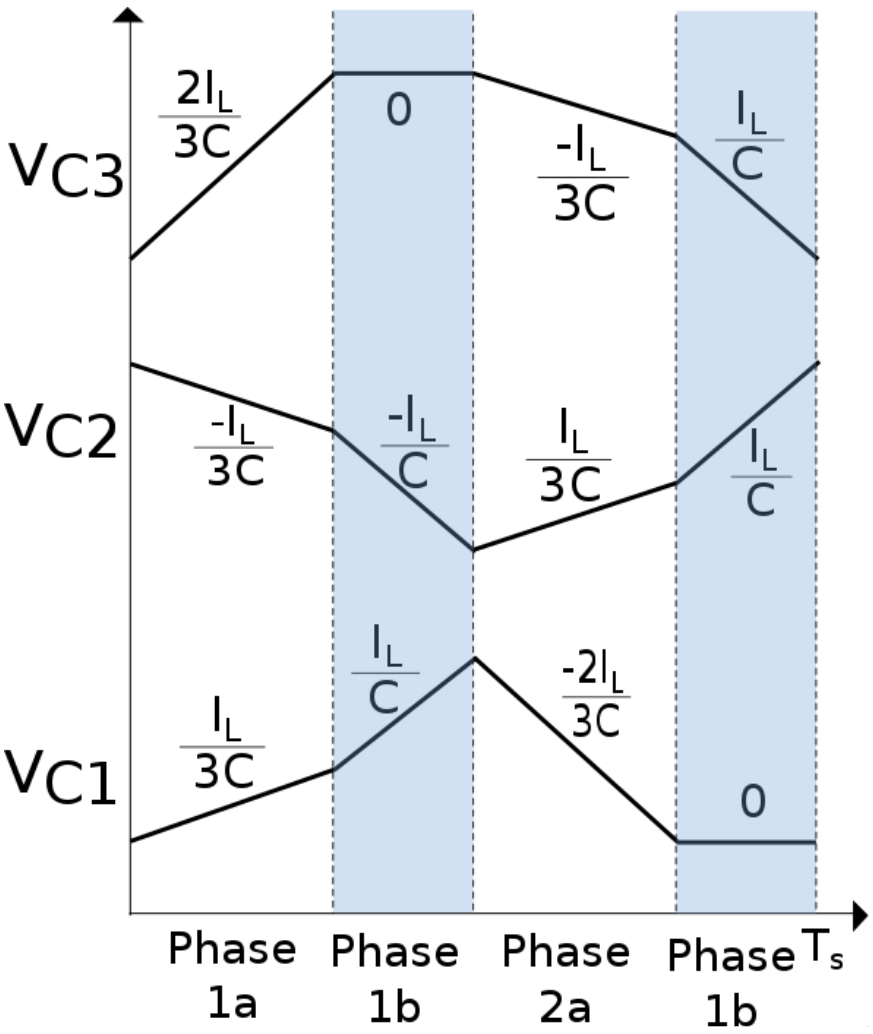


Figure 3.18: Ideal capacitor voltage waveforms.

Dickson with split phase) are compared in Figs. 3.19-3.21. For the same load, the current spikes through each of the flying capacitors are reduced with the added output inductor and removed when operating with the split phase.

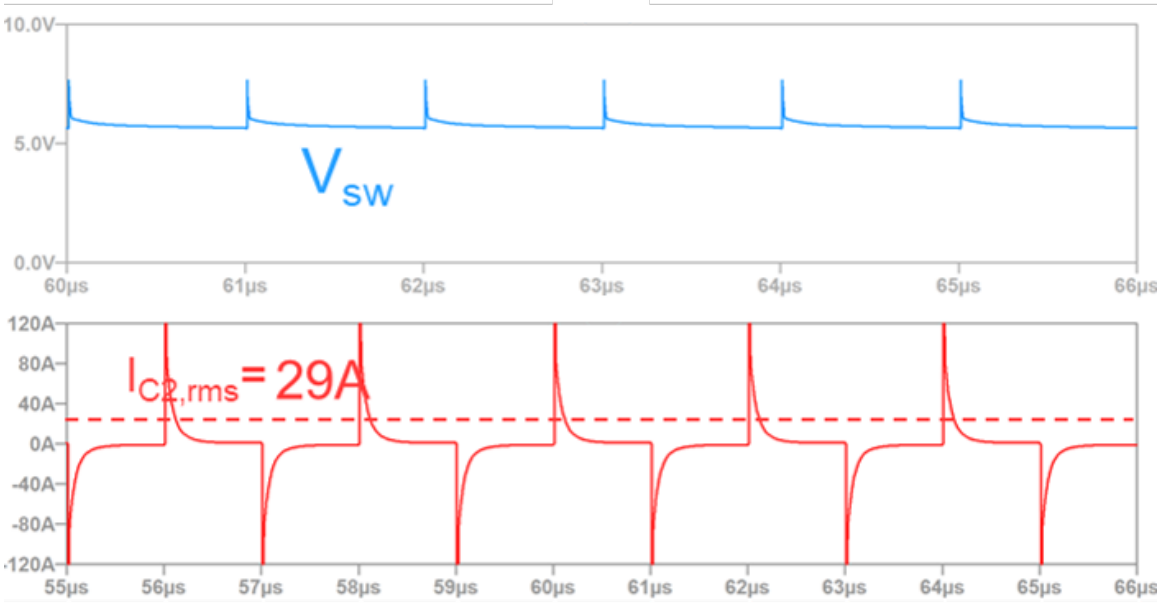


Figure 3.19: Original Dickson,V_{out} (blue), I_{C2} (red).

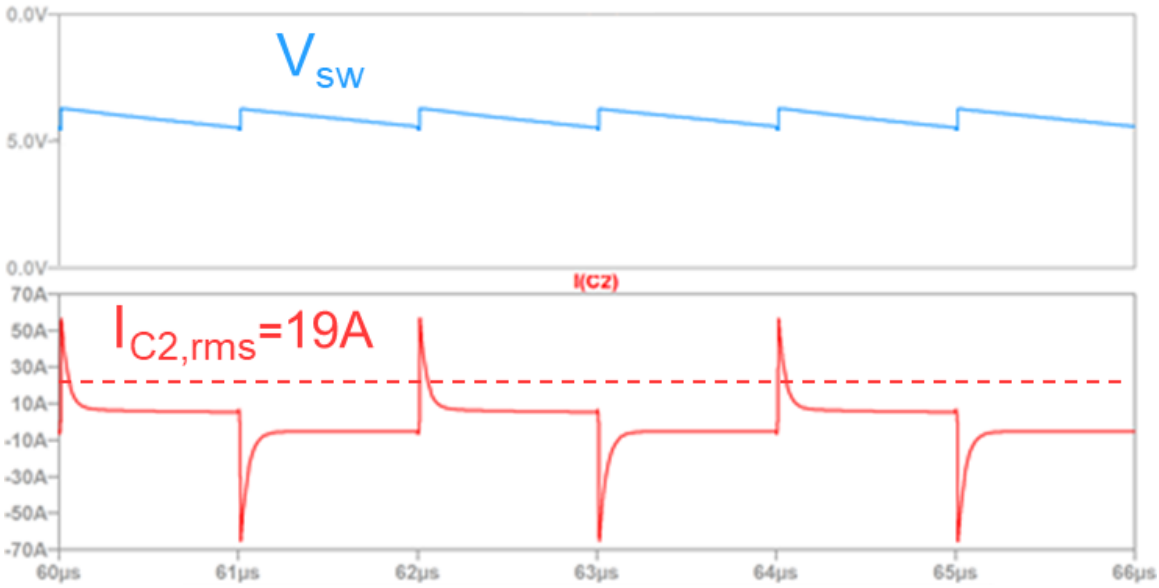


Figure 3.20: Dickson with output inductor,V_{sw} (blue), I_{C2} (red).

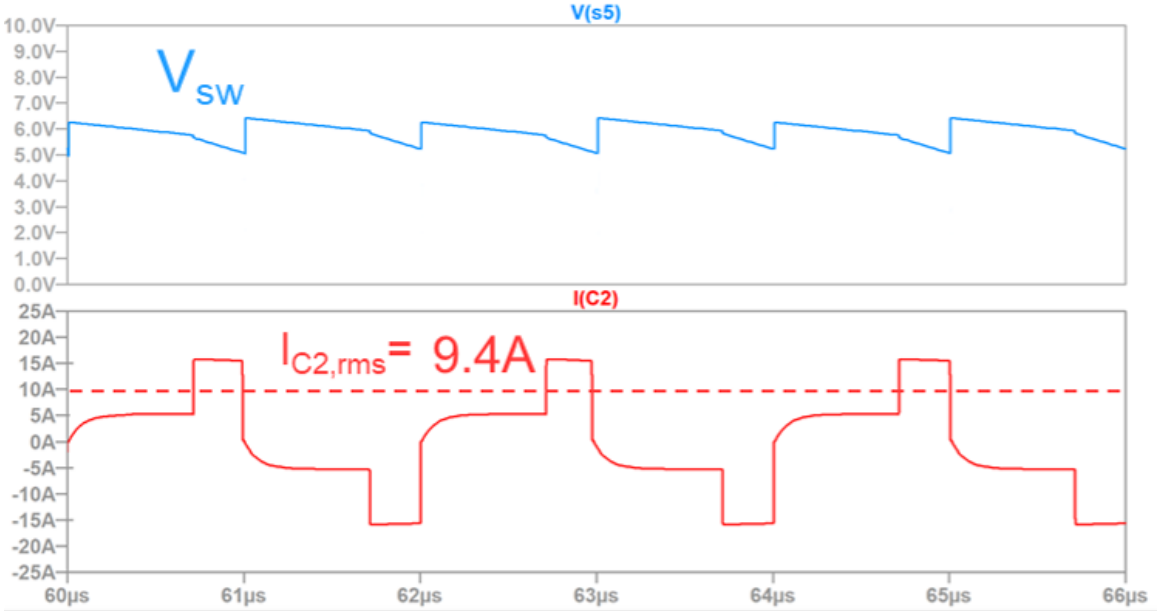


Figure 3.21: Split-phase Dickson with output inductor,V_{sw} (blue), I_{C2} (red).

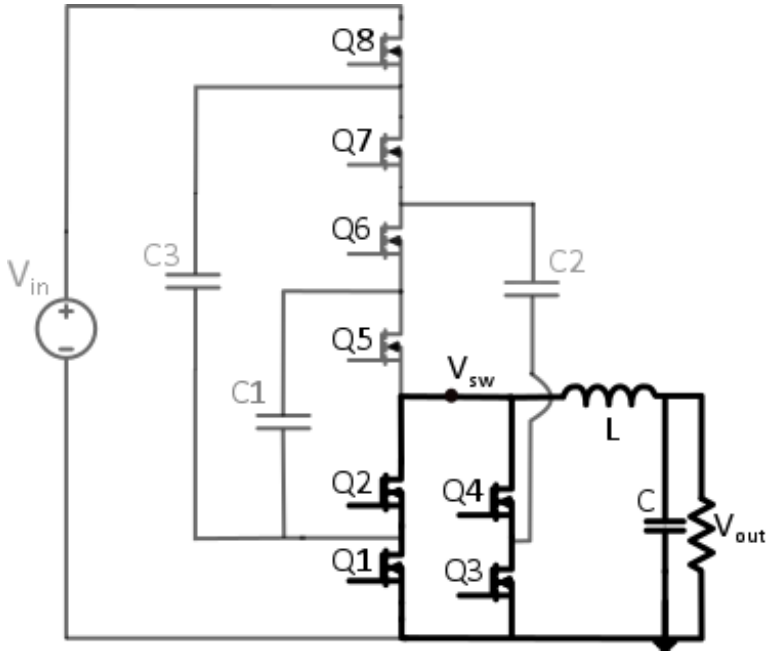
3.7 Incorporating Output Voltage Regulation in the HDSC

Depending on the specific design, the IBC can be fully regulated, semi-regulated, or unregulated. Fully regulated designs are used in architectures were the IBC's output is the supply voltage for the most power-consuming load and tend to be more expensive and less efficient due to its wide duty-cycle range [22]. Semi-regulated designs are lower cost than the regulated version but still have lower power density and efficiency than the unregulated due to the wider duty-cycle range. The unregulated design offers the highest power density but faces challenges such as a high ripple current, start-up problems, reverse energy flow and parallel-operation issues [22].

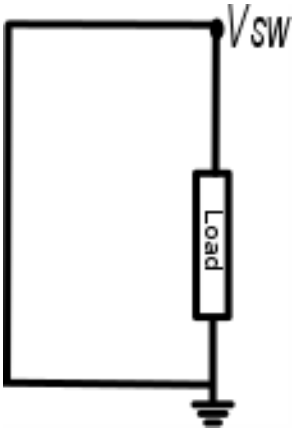
For many switched capacitor topologies, regulation can only be achieved by adjusting the output impedance which results in decreased efficiency. By leveraging the on-time of the bottom four switches the HDSC is able to regulate the output voltage. This ability to regulate the output is also beneficial because it enables the duty cycle to be extended to reduce the peak inductor current through the output inductor, decreasing RMS currents. Using a PWM regulation technique, switches Q_1-Q_4 are turned ON for the duration of $(1-D)T_s$, shorting the switch node to ground. In [88], the equation for the regulated output voltage is

$$V_{out} \approx \frac{DV_{in}}{N} \tag{3.34}$$

The circuit for implementation of the regulation interval is provided in Fig. 3.22a along with the simplified circuit in Fig. 3.22b. The corresponding gate signals are shown in Fig. 3.23.



(a) Split phase



(b) Simplified circuit

Figure 3.22: Voltage regulation circuit.

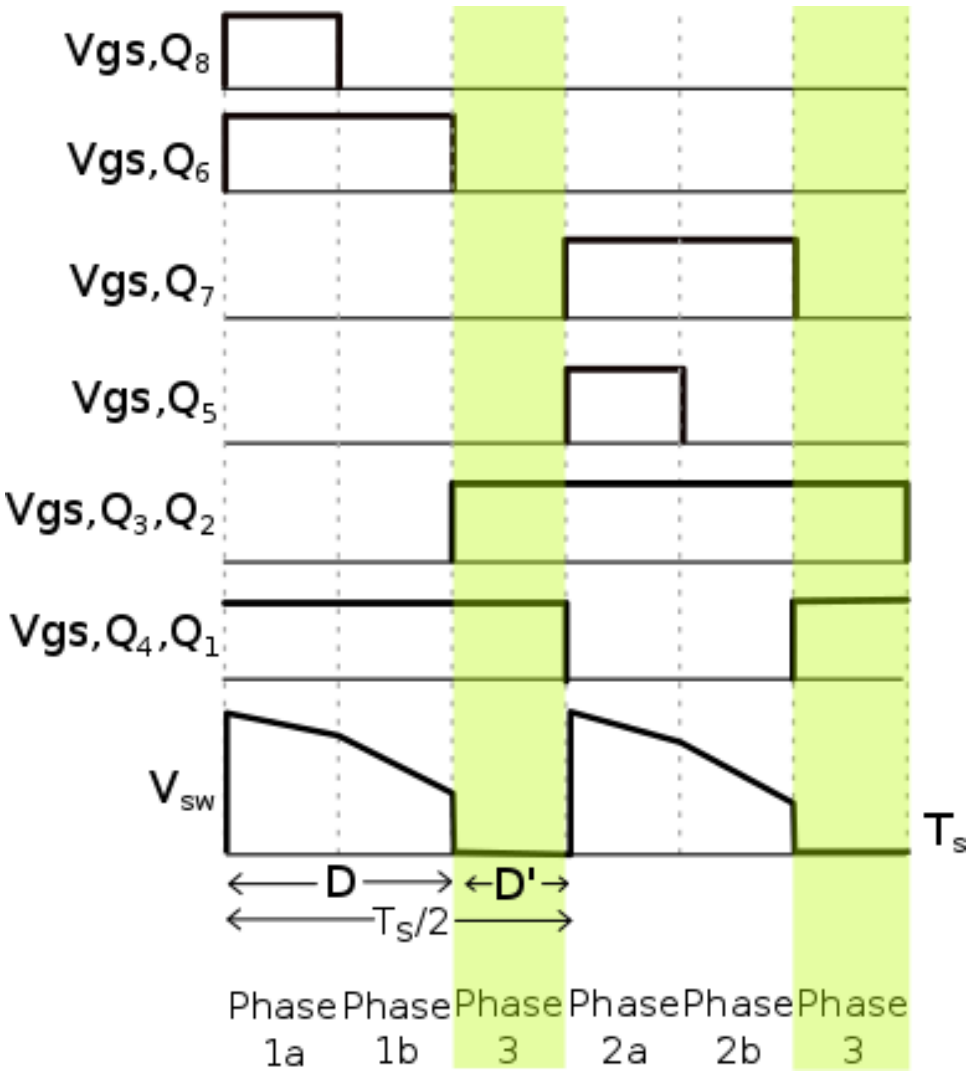


Figure 3.23: Gate signals and the switch node voltage, V_{sw}, for the regulated 4:1 HDSC.

3.8 HDSC Design

3.8.1 Selecting the Conversion Ratio (N), Flying Capacitance (C_{fly}), Inductance (L), and Switching Frequency (f_s)

Conversion Ratio

The 4:1 and 8:1 conversion ratios were considered for this 48-5V application. The circuit parameters for each conversion ratio are provided in Table 3.3. The average current, I_{avg}, is representative of the current through the parallel branches during Phase 1a.

Table 3.3: Comparison of circuit characteristics for the 4:1 and 8:1 HDSC

	4:1	8:1
# of C_{fly}	3	7
# of devices	8	12
V_{ds}	12V	6V
I_{avg}	$\frac{1}{3}I_L$, $\frac{2}{3}I_L$	$\frac{1}{7}I_L$, $\frac{2}{7}I_L$
V_{sw}	12V	6V
D	.417	.833

The 4:1 conversion ratio has the advantage of using fewer switches, reducing implementation costs. The switching losses are not reduced however compared to the 8:1 conversion. With fewer flying capacitors, the voltage domain for each switch in the 4:1 is increased (12V), leading to a higher V_{ds} compared to the 8:1 (6V), which corresponds to higher loss due to the discharge of the device output capacitance. A comparison of the loss breakdown between the 4:1 and 8:1 designs are provided in Fig. 3.24. The losses are analyzed using the same devices (EPC2023C), capacitors (CGA6M3X7S2A475K200AB), output inductor (LP202) and duty cycle. Additionally, as the conversion ratio increases so does the number of parallel capacitor branches. As the number of branches increases, the current through each branch decreases for the same output current. Therefore, conduction losses are reduced as the conversion ratio increases. The loss breakdown in Fig.3.24 includes the inductor conduction loss caused by the

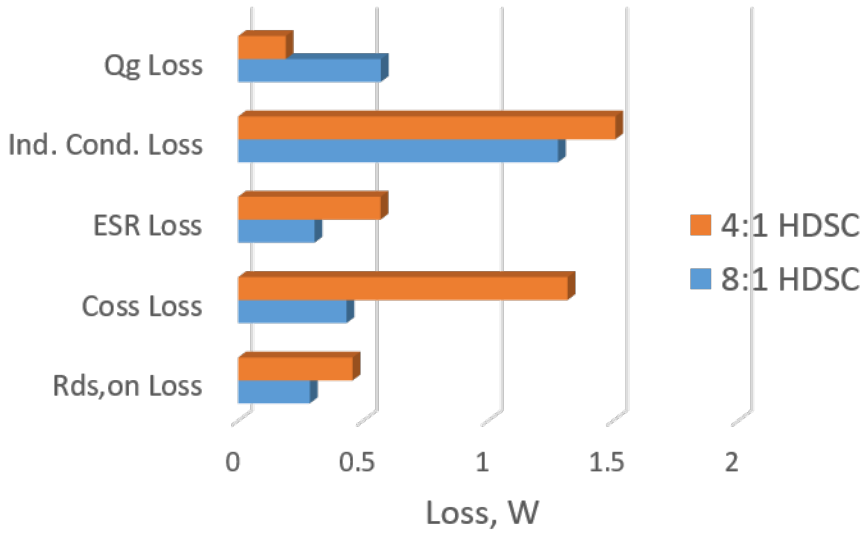


Figure 3.24: Loss comparison for the 4:1 and 8:1 conversion ratio, V_{in}=48V, V_{out}=5V, f_s=500kHz

series parasitic DC resistance of the inductor (DCR). The conduction loss for this parasitic resistance can be calculated using, $I_{rms}^2 R_{DCR}$. However, since the inductor current ripple of the 4:1 is greater than the 8:1, ac losses related to the output inductor such as conduction loss from the inductor's ac resistance, R_{ac}, and core loss should also be considered. Since the applied volts-seconds of the 4:1 is greater than the 8:1, for the same duty cycle, D, there will be a much larger current ripple. A large current ripple is not ideal because it can cause increased inductor core loss and conduction loss due to the inductor's AC resistance. The core loss is related to the applied volts-seconds and is demonstrated in Equation 3.35.

$$(V_{sw} - V_{out})DT_s = \frac{\Delta i_L}{L} = n\Delta B A_c \tag{3.35}$$

where V_{sw} is the positive terminal of the inductor, T_s is the length of the period, ΔB is the maximum flux density, n is the number of turns on the inductor and A_c is the area of the core. To improve the current ripple, the area or the number of turns must increase in order to increase the inductance,

$$L = n^2 \frac{A_c \mu_0}{l_g}. \tag{3.36}$$

where l_g is the length of the air gap and μ_0 is the permeability of air. Therefore, the 4:1 design would require a larger inductor for a comparable current ripple. This would effect the power density as well as increase cost. In comparison to the buck converter, however, the inductance that the HDSC requires is smaller than that of the buck. Equations 3.37 and 3.38 compare the inductance required for both the buck converter and the HDSC.

$$L_{SC} = \frac{V_{out}}{\Delta i_L}(1 - \frac{NV_{out}}{V_{in}})\frac{1}{2f_s} \tag{3.37}$$

$$L_{buck} = \frac{V_{out}}{\Delta i_L}(1 - \frac{V_{out}}{V_{in}})\frac{1}{f_s} \tag{3.38}$$

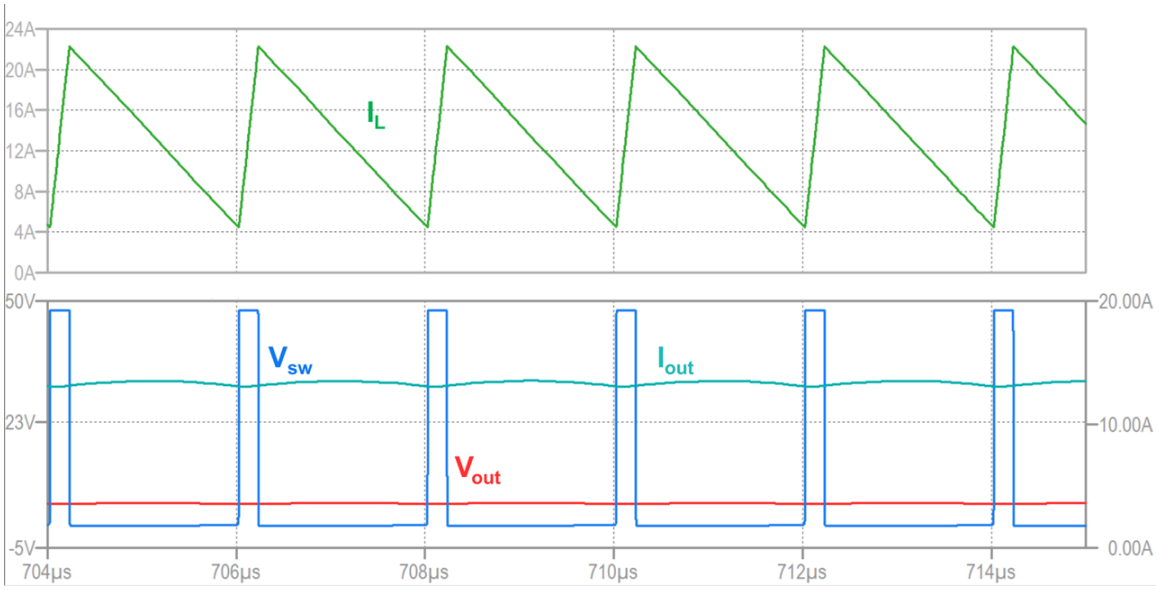
The HDSC inductor, L_{sc}, is reduced by 2 because the switching frequency of the inductor current occurs twice over one period due to the nature of the topology. L_{sc} is further reduced due to the conversion ratio of the switched capacitor network. The inductor current ripples for a buck and 4:1 HDSC at equivalent operating points and are compared in Fig. 3.25a and Fig. 3.26a. For the buck, $\Delta i_L = 17.2A$. For the 4:1 HDSC, $\Delta i_L = 1.68A$.

Selecting C_{fly}, L, and f_s

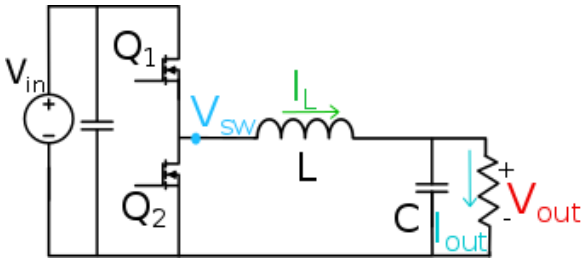
The relationship between capacitance and ΔV are inversely proportional for the same output current, I_{load} as described in Equation 3.39.

$$I_{load} = \frac{C\Delta V}{f_s} \tag{3.39}$$

There is a trade-off when selecting the value for the flying capacitors. A large capacitance will decrease the voltage ripple and minimize hard-charging loss but the large capacitance will decrease the power density and increase the overall costs. A smaller capacitance will mean a smaller footprint and lower cost but the voltage ripple will be large and may cause decreased efficiency. To determine C_{fly}, a constraint can be applied to $\Delta V_{c,fly}$. The constraint on ΔV can be found be determining an acceptable ripple at the output. The capacitor voltage

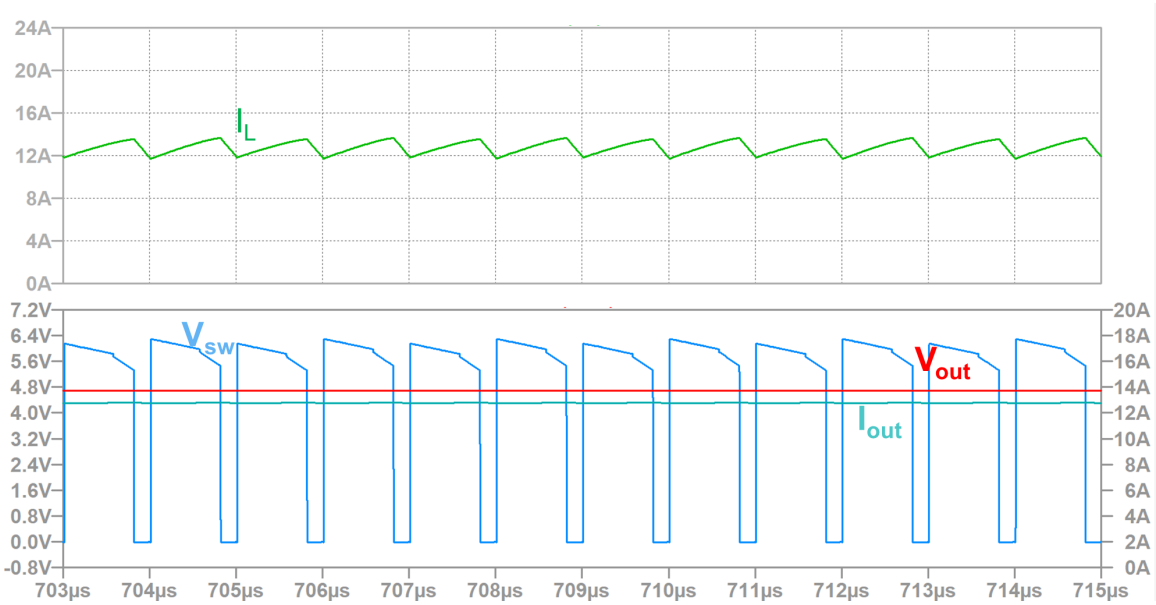


(a) Simulated inductor current ripple of buck converter.

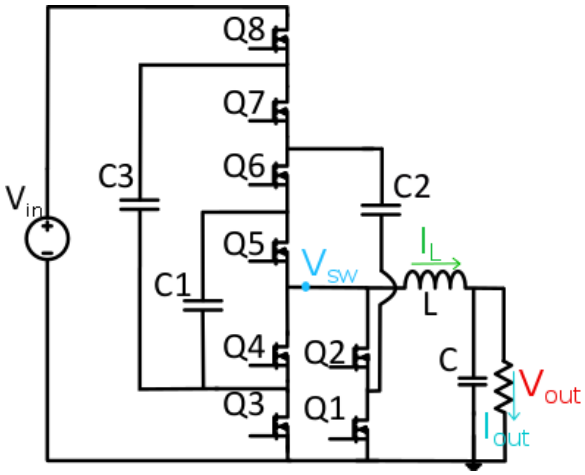


(b) Circuit schematic of buck converter.

Figure 3.25: Simulated inductor current ripple of buck converter and schematic.



(a) Simulated inductor current ripple of 4:1 HDSC converter.



(b) Circuit schematic for 4:1 HDSC.

Figure 3.26: Simulated inductor current ripple of 4:1 HDSC converter and circuit schematic.

ripple, ΔV, can be chosen as a fraction, α, of V_{out}.

$$\Delta V_{C,fly} = \alpha V_{out} \tag{3.40}$$

The capacitance can then be calculated using the amount of charge, Q_c, and the permissible voltage ripple, ΔV.

$$C_{fly} = \frac{Q_c}{\Delta V} = \frac{I_{load}}{f_s C_{eq}} \tag{3.41}$$

C_{eq} is the equivalent series and parallel capacitance seen at the output. For the 4:1 C_{eq} is equal to $1.5C_{fly}$ and for the 8:1, C_{eq} is equal to $2.5C_{fly}$.

When selecting the switching frequency, capacitance of C_{fly}, and output inductance, there is one requirement that must be met in order to stay in the operating region for achieving soft-charging. As previously described the original Dickson operates in the SSL region where the capacitor voltage ripple is tied to the efficiency of the converter. By adding an output inductor, the output impedance is reduced and the converter is able to operate in FSL at a lower switching frequency [7]. This can be seen in Fig. 3.27 where the comparison of impedance curves are shown for a 2:1 switched capacitor with and without an output inductor. Therefore, the requirement is that the switching frequency must be much greater

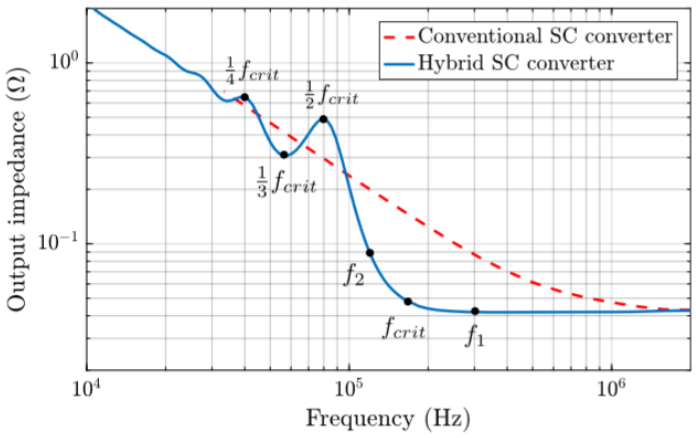


Figure 3.27: Simulated output impedance vs. frequency [7].

than the critical frequency, f_{crit}, which can be calculated using Equation 3.42. This is the

minimum switching frequency that the converter can operate in FSL.

$$f_{crit} = \frac{1}{2\pi\sqrt{LC_{eq}}} \tag{3.42}$$

As previously stated the 8:1 design requires the most devices, but with a higher conversion ratio, and more flying capacitors in parallel branches, the load current is distributed through each branch resulting in lower conduction loss, lower output capacitance loss and decreased stress on the inductor. For these reasons the 8:1 conversion ratio was selected, the topology is provided in Fig. 3.28.

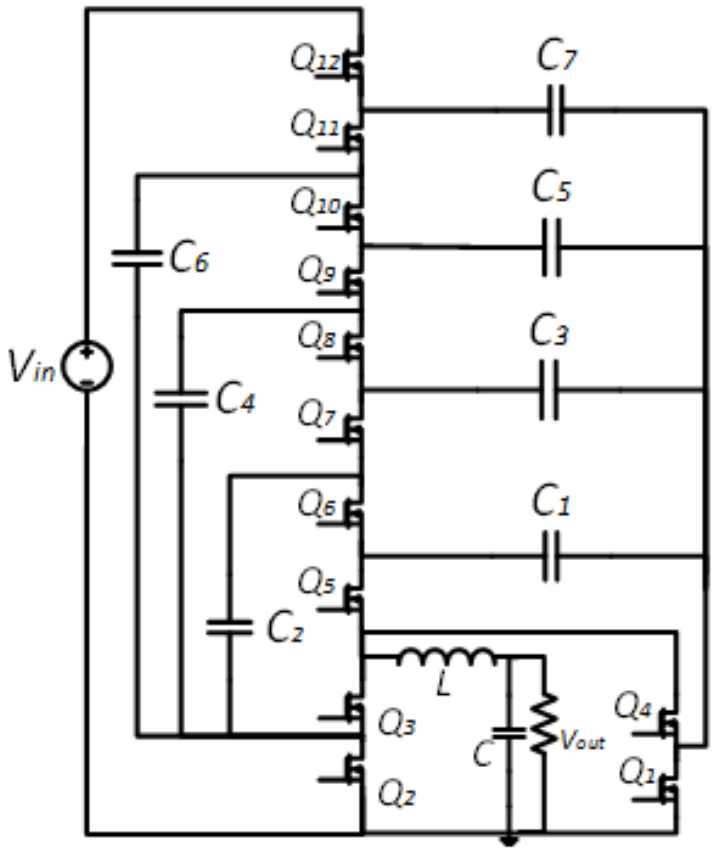


Figure 3.28: 8:1 Hybrid Dickson Switched Capacitor Converter.

Chapter 4

Implementation and Testing

4.1 Flying Capacitor Selection

As devices and control circuity continue to decrease in size, passive elements such as inductors and capacitors become the dominant elements for determining converter volume. Therefore, selecting energy storage elements with high power density is of great importance. Ceramic capacitors were selected for the flying capacitors because they offer high energy density and low equivalent resistance. The drawback of ceramic capacitors, however, is that their capacitance decreases with applied voltage.

Other types of capacitors that were considered were metal film and electrolytic capacitors. Metal film capacitors have very low loss and are able to maintain their capacitance. However, they have low energy density. Electrolytic capacitors can maintain their capacitance with applied voltage but have high ESR limiting RMS current capability and they have low reliability. In [78] the energy storage capability of ceramic, electrolytic and film capacitors operating with a wide voltage swing at high frequencies was analyzed. Ceramic capacitors were shown to have the highest energy density for the application. Electrolytic capacitors were current limited but have a higher density in DC applications.

Class I Ceramic Capacitors

Class I ceramic capacitors have a linear temperature coefficient, their capacitance does not depreciate due to applied voltage, they do not suffer significant aging due to paraelectric

materials, have low electrical loss and have high stability and accuracy. However, Class I capacitors have low energy density and require a large package for high capacitance [78].

Class II Ceramic Capacitors

In comparison, Class II capacitor's nominal capacitance varies nonlinearly with temperature. The capacitance is highly dependent on the applied voltage, suffers significant aging due to the ferro electric materials used in manufacturing, has low stability and accuracy, significantly higher electrical loss compared to Class I but they have high permitivity which enables large capacitance values to be achieved in small device packages. Therefore, Class II capacitors are practical devices for this design [89] [86]. For ceramic capacitors with a voltage rating of 100V, the X7S material offers high energy density [78] and is used in the implementation. Fig. 4.1 shows the Class II ceramic capacitor code definitions. The X7S material can operate between $-55°$ C and 125°C with a capacitance variance of $\pm$ 22%.

Class 2 ceramic capacitors
Code system regarding to EIA RS-198 for some temperature ranges and inherent change of capacitance

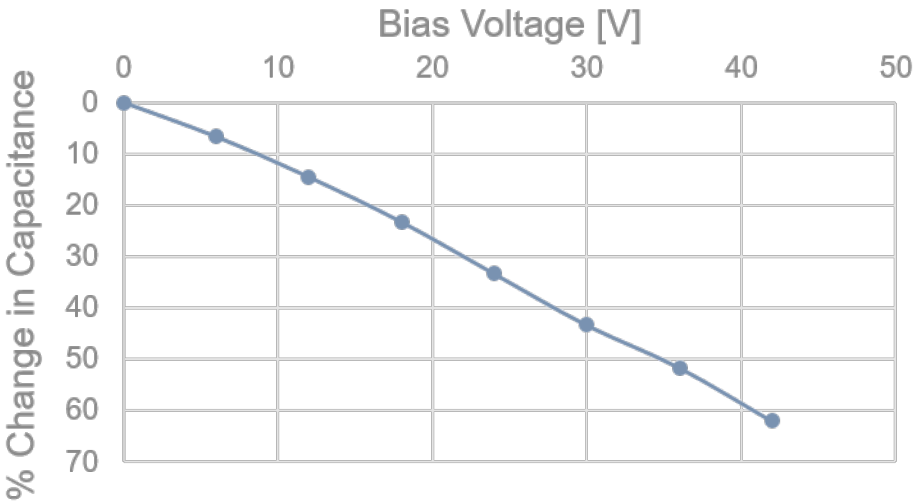
Letter code low temperature	Number code upper temperature	Letter code change of capacitance over the temperature range
X = −55 °C (−67 °F)	4 = +65 °C (+149 °F)	P = ±10%
Y = −30 °C (−22 °F)	5 = +85 °C (+185 °F)	R = ±15%
Z = +10 °C (+50 °F)	6 = +105 °C (+221 °F)	S = ±22%
	7 = +125 °C (+257 °F)	T = +22/−33%
	8 = +150 °C (+302 °F)	U = +22/−56%
	9 = +200 °C (+392 °F)	V = +22/−82%

Figure 4.1: Class 2 ceramic capacitors Code system.

As previously stated, one of the disadvantages of the Class II capacitor is that the nominal capacitance decreases non linearly with applied voltage. Table 4.1 shows the drop in capacitance for three $4.7\mu F$ TDK capacitors (CGA6M3X7S2A475K200AB) in parallel with a DC bias, measured on the 4294A 40Hz-110MHz Precision Impedance Analyzer.

Table 4.1: Measured capacitance with DC bias voltage using the 4294A 40Hz-110MHz Precision Impedance Analyzer.

Applied DC Bias	Capacitance
No DC Bias	13.38μF
6V	12.49μF
12V	11.44μF
18V	10.27μF
24V	8.92μF
30V	7.58μF
36V	6.47μF
42V	5.08μF



(a) Percent change in capacitance with applied DC bias voltage.

Figure 4.2: Capacitance change vs. Voltage for (3) TDK CGA6M3X7S2A475K200AB in parallel.

4.2 Device Selection

Gallium Nitride (GaN) power devices are reshaping the power electronics industry. The material properties of GaN and GaN device structures have many advantages over silicon (Si). Silicon is limited in its voltage blocking capability, operation temperature and switching frequency. Silicon Carbide (SiC) and GaN are the most commercially available WBG devices today. GaN offers a lower thermal conductivity, better high frequency and high voltage performance and commercially available low voltage rated devices than SiC. GaN is therefore the best material for this application. The material properties of GaN compared to other materials are provided in Table 4.2. The large electrical field, high electron mobility and thermal conductivity properties are considerable when compared to silicon [90].

Table 4.2: Material Characteristic of GaN compared to Si and SiC

Parameter	Si	SiC	GaN
Band Gap, E_g(eV)	1.12	3.2	3.4
Breakdown Field, E_{BD} ($\frac{MV}{cm}$)	.3	3.5	3.3
Electron Mobility, μ_n ($\frac{cm^2}{Vs}$)	1500	650	900-2000
Saturated Drift Velocity, V_s ($\frac{cm}{s}$)	1.0	2.0	2.5

The higher breakdown field, E_{BD}, of GaN enables a much higher blocking voltage compared to Si. This higher blocking voltage allows the terminals of the device to be placed closer together while still being able to block larger amounts of voltage, enabling a smaller device, with less capacitance and faster switching capabilities. The specific on-resistance, R_{on} [91], is inversely proportional to the cube of the breakdown field, E_{BD}^3 and the electron mobility, μ_n ($\frac{cm^2}{Vs}$) and inversely proportional to the square of the breakdown voltage, V_{Br} (V).

$$R_{on} = \frac{4V_{BR}^2}{\epsilon_r E_{BD}^3 \mu_n} \tag{4.1}$$

For GaN devices, the electron mobility increases due to a 2-dimensional electron gas. This high mobility and increased E_{BD} can significantly reduce the on- resistance of a GaN device

compared to Si. Fig. 4.3 compares the theoretical on-resistance and blocking voltage capability for silicon, silicon-carbide and gallium nitride .

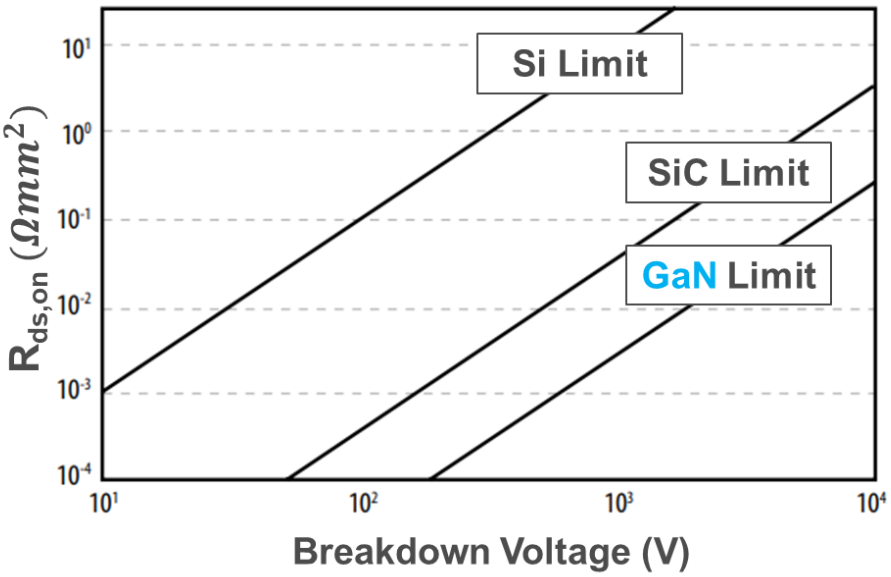


Figure 4.3: Theoretical on-resistance vs. blocking voltage capability for silicon, silicon carbide and gallium nitride [8].

The low $R_{ds,on}$ of GaN devices is beneficial for high current application where every milli-ohm of resistance can significantly impact efficiency. Additionally, the small packaging is desirable as long as thermal requirements can be met. Fig. 4.4 shows the dimensions and footprint for the GaN device used in this converter design.

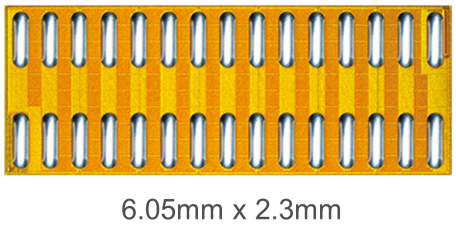


Figure 4.4: Top view of an eGaN FET EPC2023C [9].

In power FETs there is a trade-off between the amount of charge required to turn the device ON and OFF and the on-resistance called the $R_{on}Q_g$ product. The $R_{on}Q_g$ product is a figure of merit (FOM) that has been shown to translate into improved conversion efficiency

in high frequency circuits [92]. Multiple 30V Si and GaN devices are compared in Fig. 4.5. While the GaN device does not suffer from Q_{rr} loss it does have a voltage drop similar to that

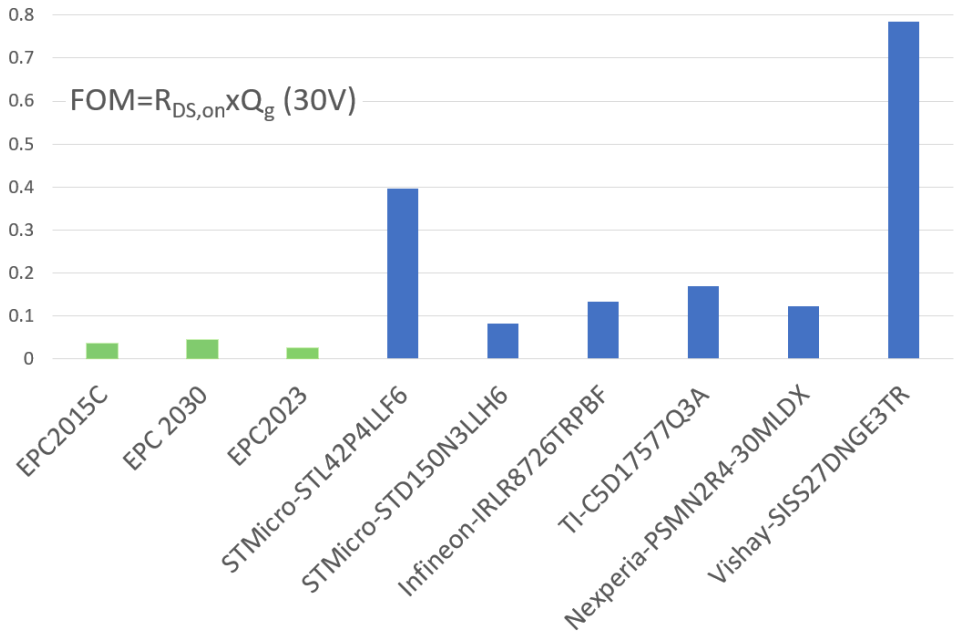


Figure 4.5: $R_{on}Q_g$ product for 30V benchmark silicon compared to GaN.

of a body diode. The forward voltage drop, V_F, is approximately 1.4V for the EPC2023C device selected. To minimize losses associated with the forward voltage of the body diode, dead-times should be designed appropriately. A summary of the device characteristics for the EPC2023C device are provided in Table 4.3.

4.3 Isolation Stage

Each pair of devices, starting with the top two switches, sit in their own voltage domain and each device requires an isolated gate drive signal. For the 8:1 design, 6 isolation blocks were needed for each TI-LM5113 gate driver. The designed isolation board is provided in Fig. 4.6. Each isolation block includes an isolated power supply, a linear regulator to provide V_{CC} to the gate driver and two digital isolators used to provide gate drive signals to the Hi and Lo-side devices.

Table 4.3: EPC2023C device characteristics [1].

Parameter	Value
V_{ds}	30V
I_{ds}	90A
$R_{ds,on}$	1.45mΩ
C_{oss}	2300pF
V_{gs}	6 to -4V
Q_g	19nC

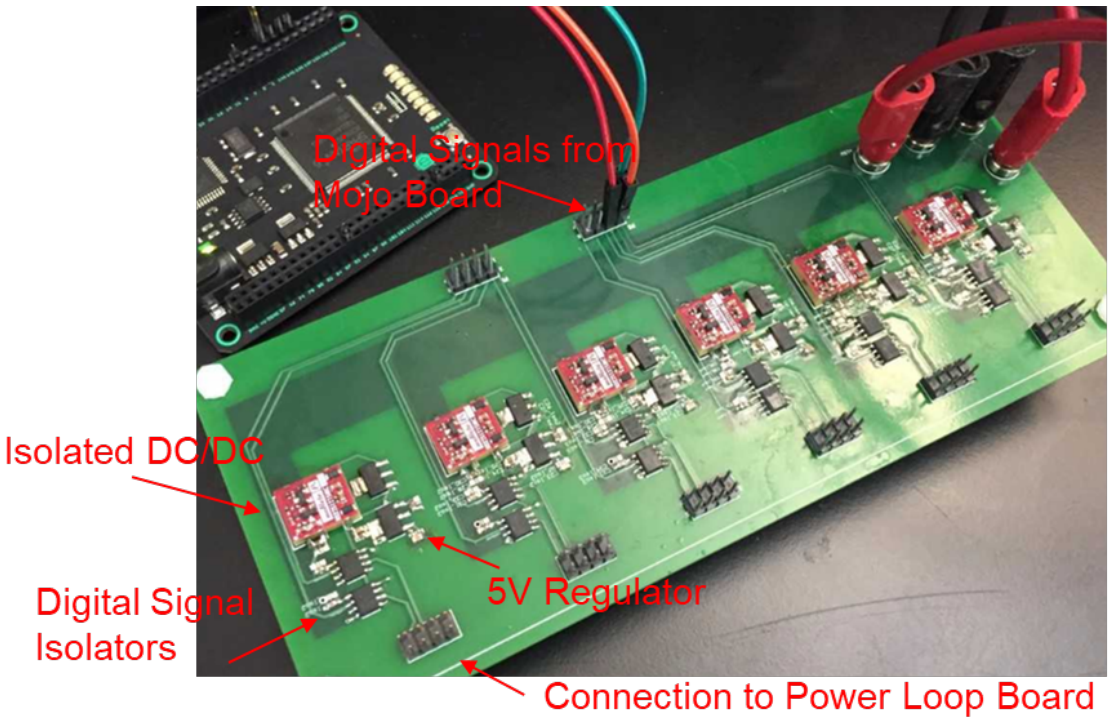


Figure 4.6: Isolation board.

4.4 Power Stage Printed Circuit Board

4.4.1 HDSC 4:1 PCB 1

Three prototypes were designed. Printed circuit board (PCB) 1, Fig. 4.7, was fabricated first, followed by PCB 2, Fig. 4.12, and PCB 3, Fig. 4.27. Each design includes improvements and revisions compared to the previous and will be discussed in this section.

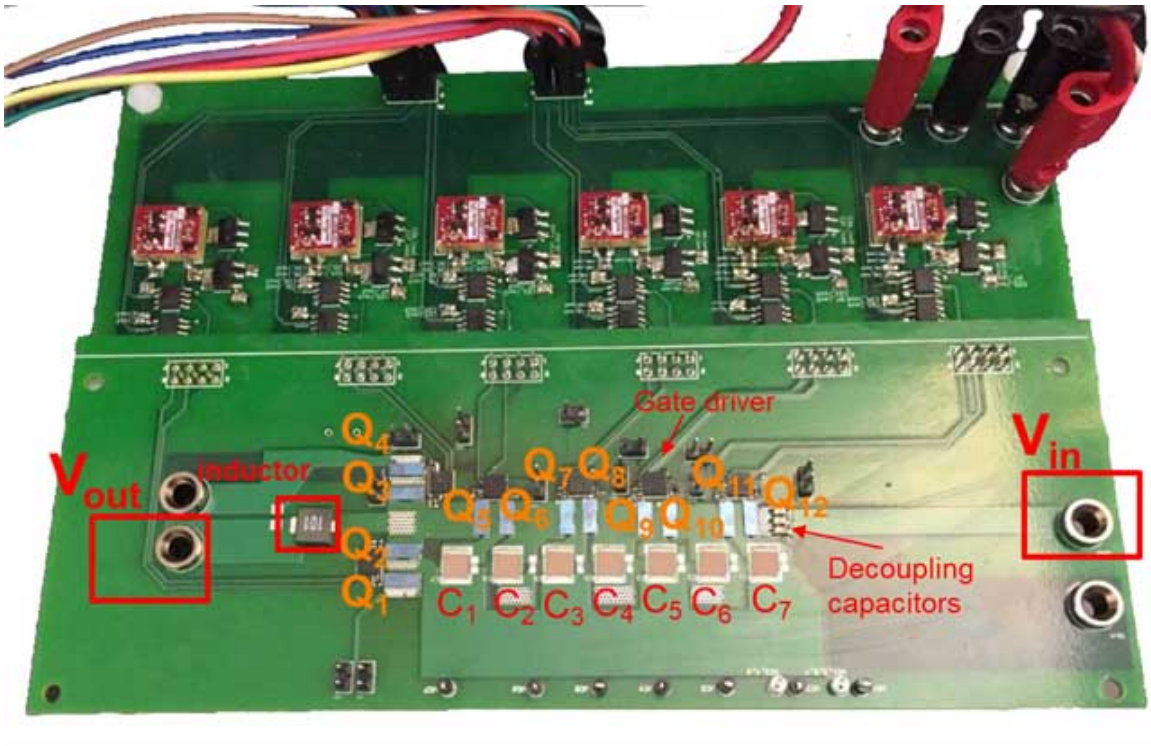
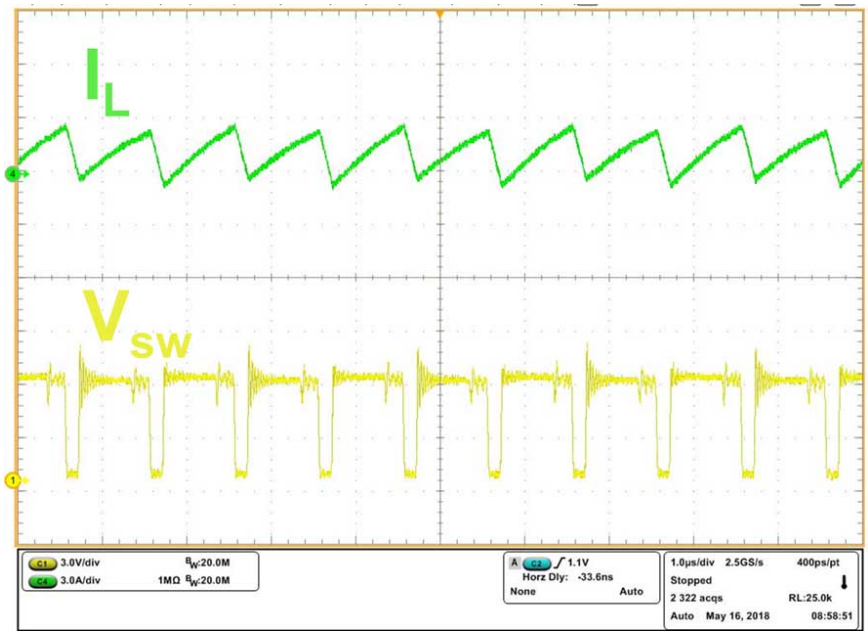
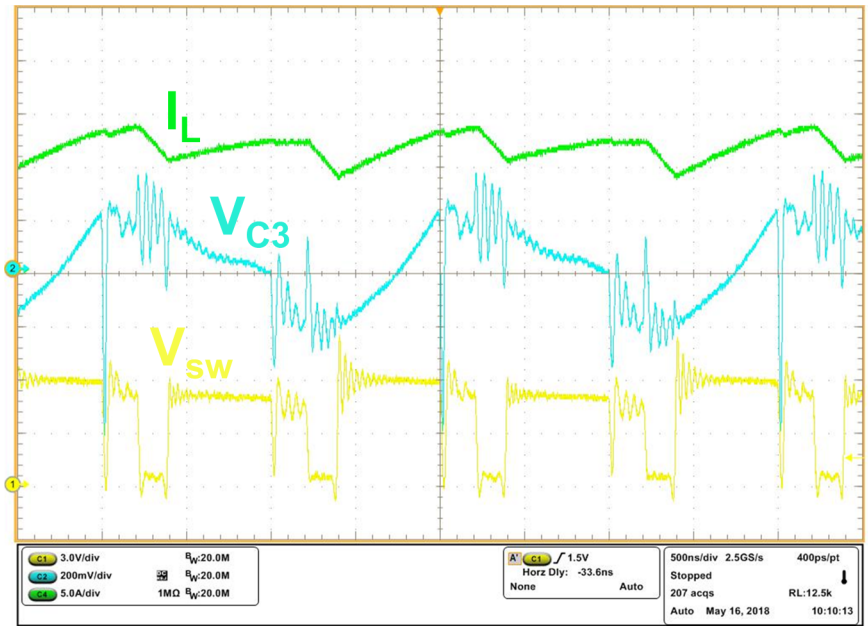


Figure 4.7: PCB 1.

Experimental waveforms from PCB 1 for the inductor current, I_L and the switch-node voltage, V_{sw}, are provided in Fig. 4.8a and Fig. 4.8b. The V_{sw} waveform in heavy load operation shows considerable ringing when transitioning from Phase 1a to 1b and Phase 2a to 2b. During each of these transitions a single device, Q_5 or Q_8 turns off. The output capacitance of the device rings with any parasitic inductance in the PCB. This ringing can over stress the devices, possibly leading to device failure and can cause a decrease in the efficiency. The efficiency results are plotted in Fig. 4.9. The converter reached a peak efficiency of $\eta = 93\%$ at 23W. At the highest power, 55W, the efficiency was 87.5%. The



(a) Light Load: $P_{out} = 5W$



(b) Heavy Load: $P_{out} = 49.3W$, $\eta = 88.6\%$

Figure 4.8: PCB 1 4:1 waveforms: $V_{in} = 24V$, $f_s = 500kHz$.

efficiency decreased quickly as the output current increased. This suggests that conduction loss is a limiting factor.

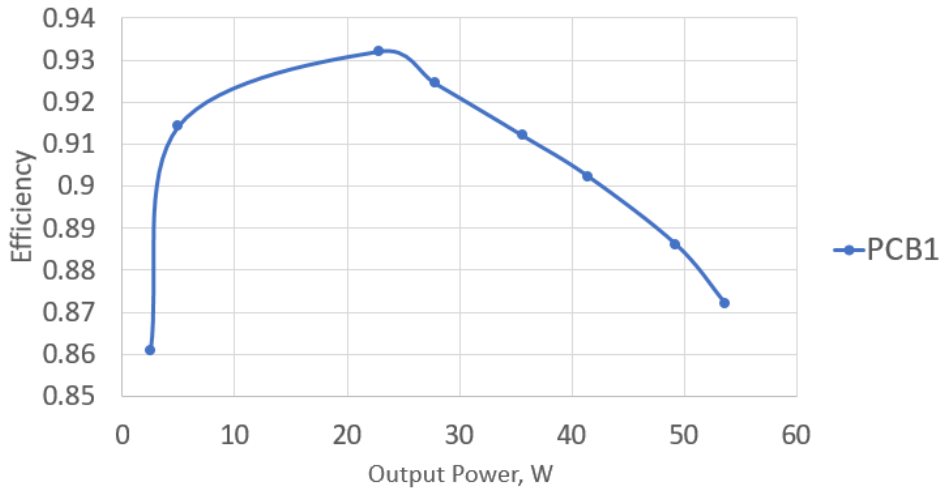


Figure 4.9: PCB 1 experimental efficiency.

ANSYS Q3D Designer software was used to analyze the current density in the 4-layers of PCB1. Current density is the current flow per unit area through a copper trace or metal plated via. The formula for calculating the current density is

$$J = I/A \tag{4.2}$$

where J (A/m^2) is the current density, I (A) is the current and A (m^2) is the cross sectional area. It is well known that that the movement of current through a conductor generates heat. This heat is dissipated into the surrounding area and the power loss is proportional to the resistance of the conductor. Therefore, the current density can provide insight into high resistive traces that will result in increased conduction loss. The current distribution on the top layer is provided in Fig. 4.10a. The simulation was performed placing the source at the input and the sink was placed at V_{sw} and devices Q_{12}, Q_{10}, Q_8, Q_6, Q_4 and Q_1 pads were shorted to resemble the ON state. On the top layer, the two places where current density is the highest is within the input trace and around the vias that connect to a flying capacitor node on the second layer. The high current density at the input is not worrisome due to the low current levels seen at the input. The high current density around the vias on the top

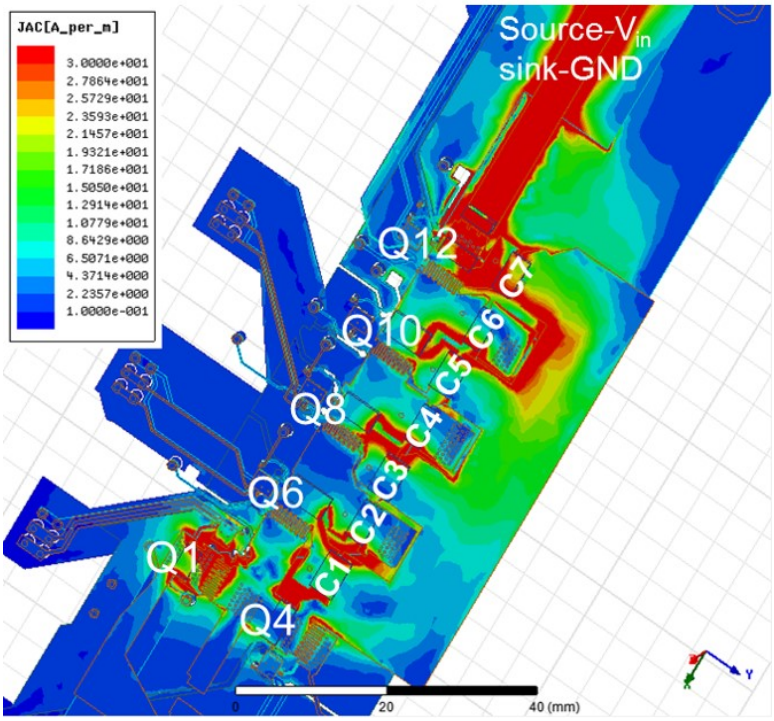
layer, circled in Fig. 4.10a, is troublesome because this is where V_{sw} connects to the trace on the second layer which connects to flying capacitors, C_2, C_4 and C_6.This node sees the full load current for half of the switching period. The via-stitching connection between layers is very small and will result in a large parasitic resistance. Furthermore, the trace used on the second layer to connect to the vias on the first layer as seen in Fig. 4.10b, is too narrow . The much higher current density causes higher trace resistance, leading to increased conduction loss.

A thermal image of PCB 1 operating at 55W, Fig. 4.11, shows significant heat at the V_{sw} node. This result is consistent with the results calculated by the Q3D simulation.

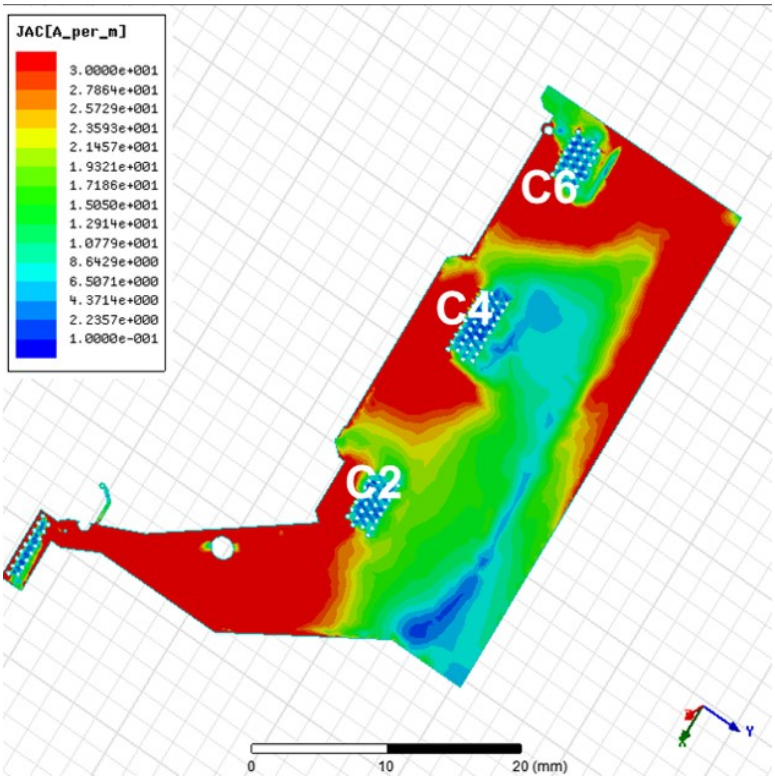
4.4.2 HDSC 4:1 Printed Circuit Board 2

The second revision, PCB 2, is shown in Fig. 4.12. The most significant change made to the layout was moving the bottom half-bridges of $Q_1 - Q_4$ to the other side of the flying capacitors to create a more comparable trace length between each of the flying capacitor branches and the output. These switches enable regulation of the output and are used to connect each flying capacitor to ground or the output inductor. In PCB 1, $Q1 - Q4$ were placed to the far left-hand side. This created a longer loop for the farthest away capacitors to connect to the output inductor. For example, during Phase 1a when C_7 is connected to the output inductor the path is much longer than that of C_1. In PCB 2, $Q1 - Q4$ and the output inductor, were moved onto the other side of the capacitors so that the trace length for each capacitor to connect to the output inductor was comparable.

The experimental waveforms for PCB 2, operating at light and heavy load are provided in Fig. 4.13. There is still significant ringing V_{sw}. Additionally, when Q_5 turns off to shift the circuit from Phase 2a to Phase 2b, disconnecting C_1 from the output, there is large ringing on V_{sw}.

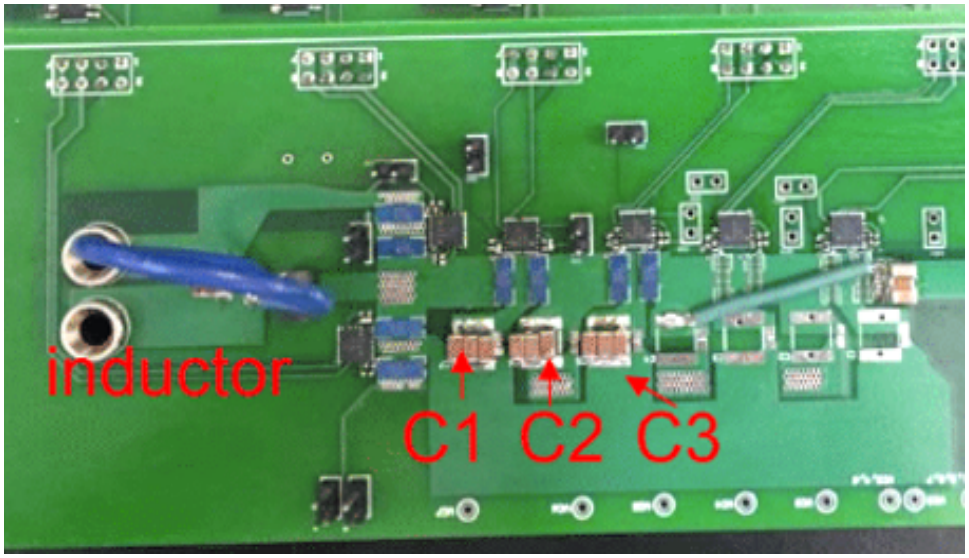


(a) Q3D simulation of current distribution on top layer of PCB 1.

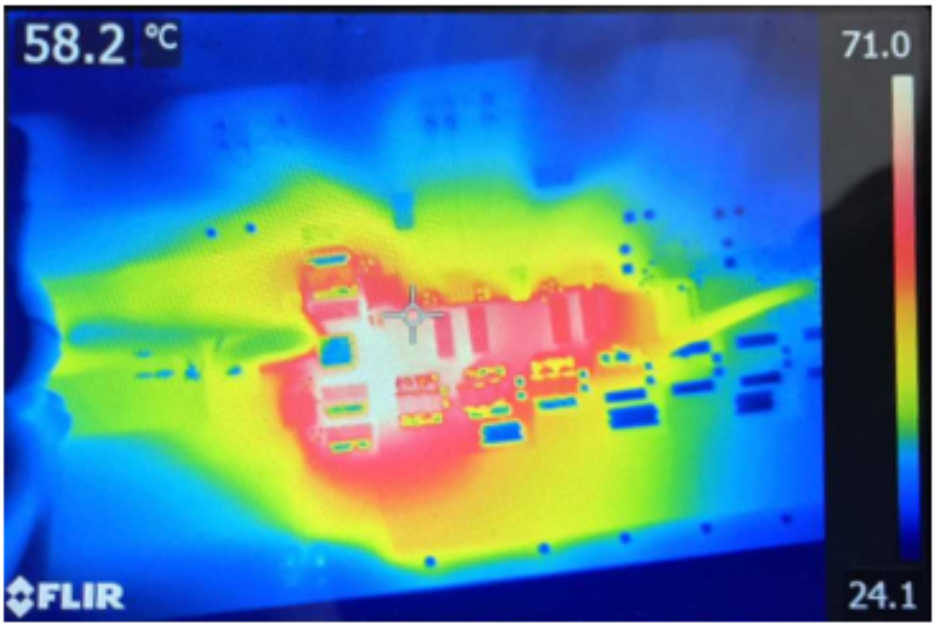


(b) Q3D simulation of current distribution on layer 2 of PCB 1.

Figure 4.10: Q3D simulations of current distribution for PCB 1.



(a) PCB 1 populated as 4:1.



(b) Output Power=55W.

Figure 4.11: Thermal image of PCB 1 taken with FLIR-T630sc camera.

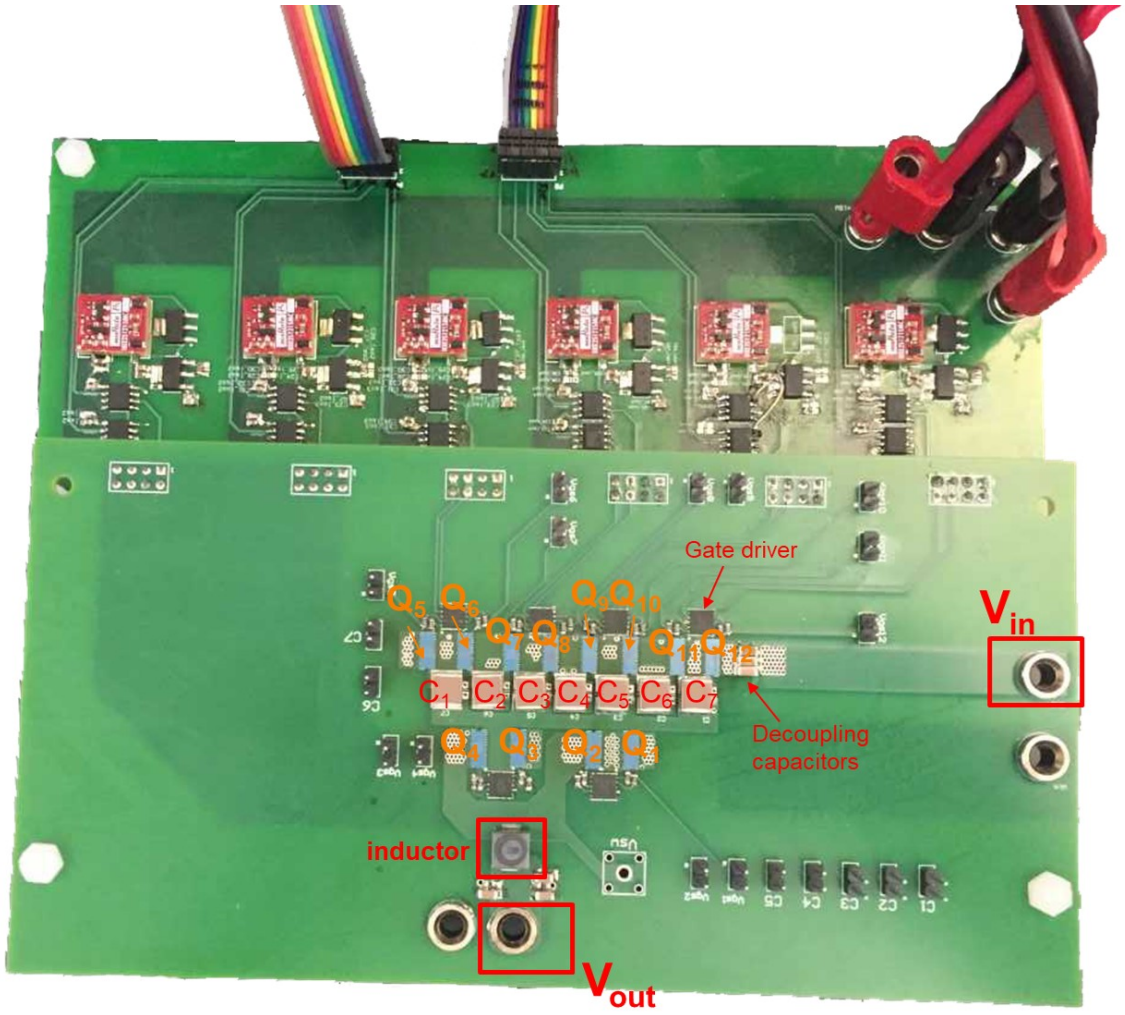
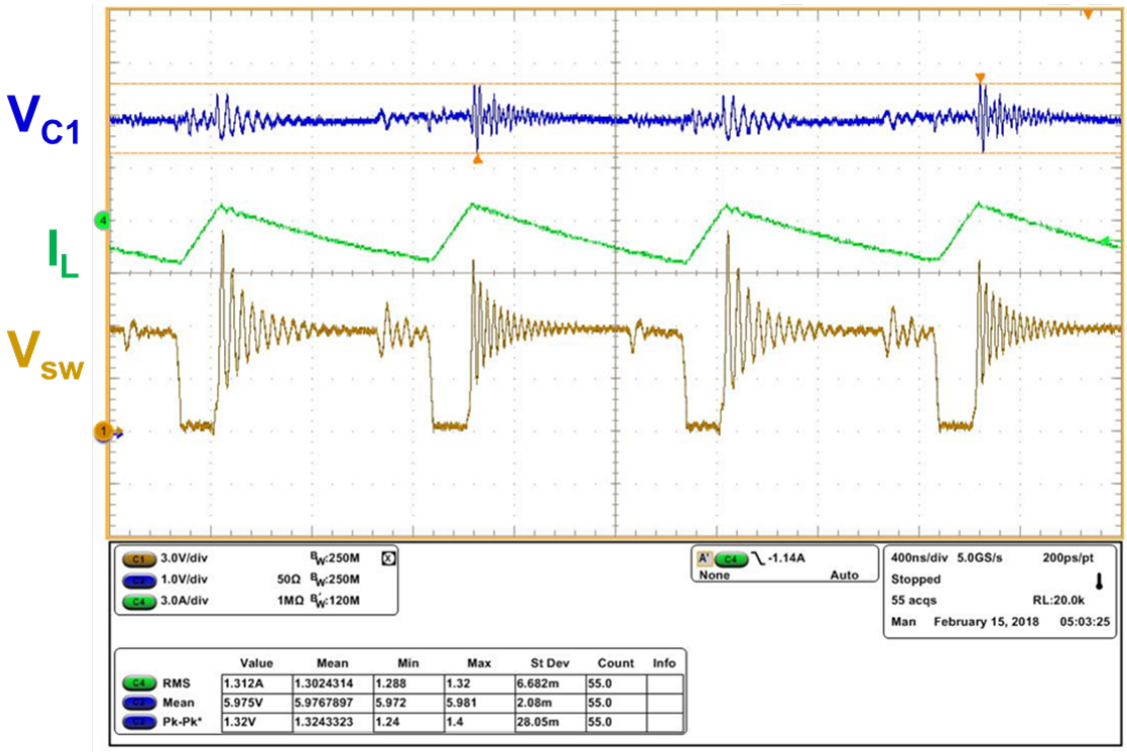
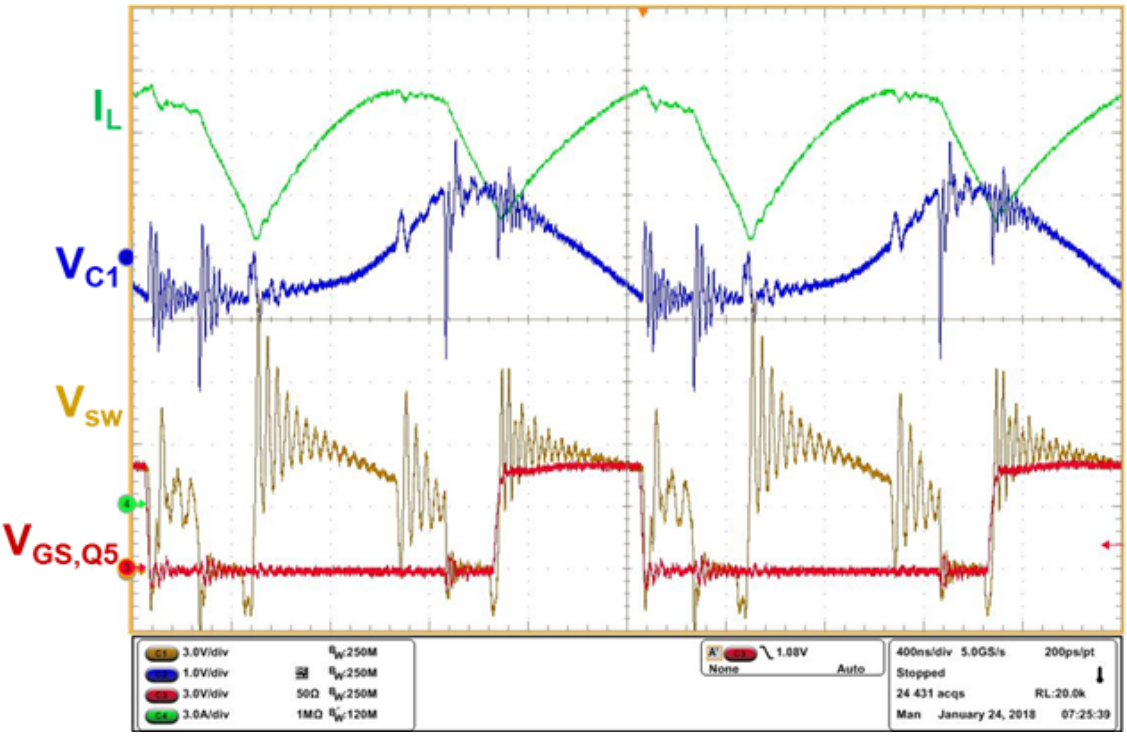


Figure 4.12: Populated PCB 2 power stage connected to isolation board.



(a) Light load: $P_{out} = 4.97W$, $\eta = 90.58\%$.



(b) Heavy load: $P_{out} = 65.3W$, $\eta = 85.44\%$.

Figure 4.13: PCB 2 4:1 waveforms: $V_{in} = 24V$, $f_s = 500kHz$.

4.4.3 HDSC 4:1 Printed Circuit Board 3

The third revision, PCB 3, is shown in Fig. 4.27. The layout included an extra V_{in} terminal and footprints for decoupling capacitors so that the 4:1 topology could be tested without forming a large loop between the input supplies and Q_8. The populated 4:1 circuit is provided in Fig. 4.14. One of the main layout improvements for this board was aim towards reducing parasitic inductance in each of the commutation loops. During each transition between phases, the capacitor current has a high di/dt. This is due to a step change between each phase interval where the average current changes. Fig. 4.17 shows the phase transition from Phase 1a to 1b. During Phase 1a, assuming a constant output current, the current through C_3 changes from $\frac{2}{3}I_L$ to 0. Using the relationship between voltage and inductance,

$$V_L = L_{par}\frac{di}{dt} \tag{4.3}$$

it can be seen that for any parasitic inductance, L_{par}, found in the path, will result in a voltage drop, V_L. Furthermore, a trace carrying current acts like an electromagnet whose field strength is proportional to the current. If the loop is large, magnetic fields can sum together inducing a voltage. This can further impede the flying capacitor's ability to achieve soft-charging. As previously discussed in earlier designs, the parasitic inductance of each loop combined with the output capacitance of the device that turns off for that particular phase transition will results in ringing. In order to reduce the parasitic inductance of each loop, the flying capacitors are pushed to either side of the device. Devices, Q_1-Q_{12}, are placed down the middle. The traces on each layer carry current in opposite directions and directly on top of each other. Therefore, the magnetic fields generated by the changing current are canceled. This is depicted in Fig. 4.15. Each layer of PCB 3 is highlighted and provided in Fig. 4.16.

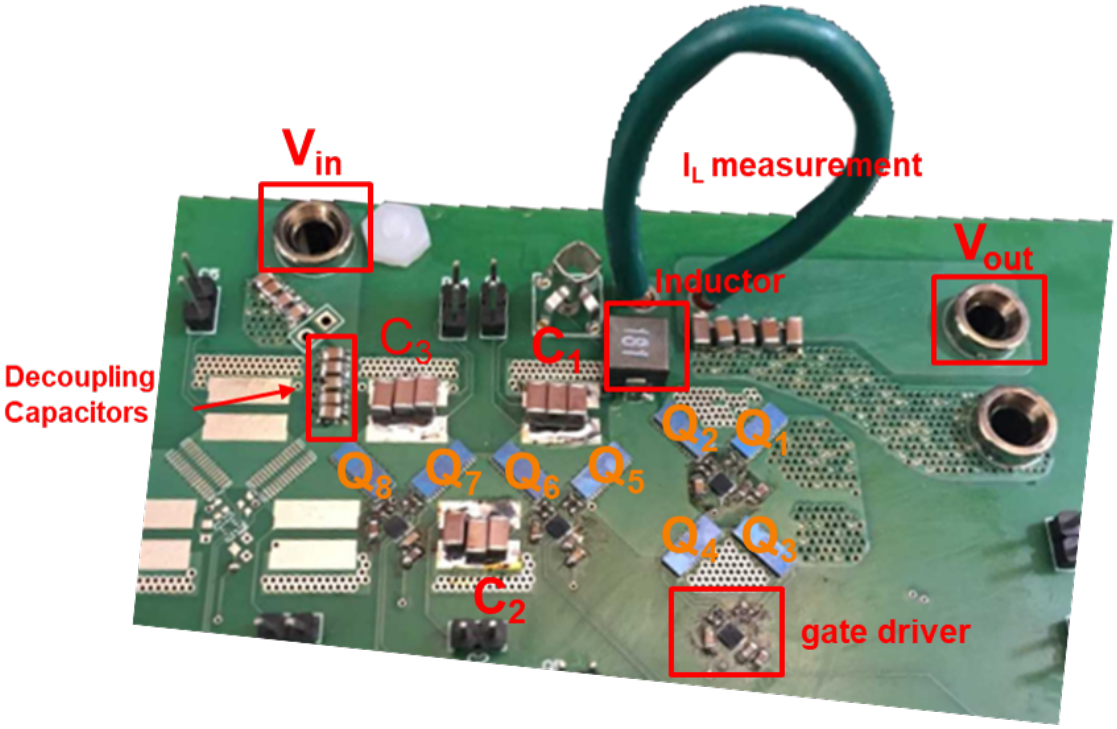


Figure 4.14: PCB 3 populated for 4:1 testing.

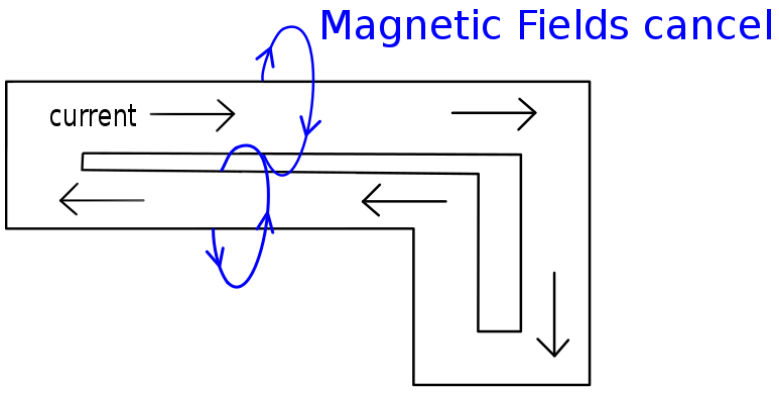


Figure 4.15: Field cancellation of parallel conductors with currents flowing in opposite directions.

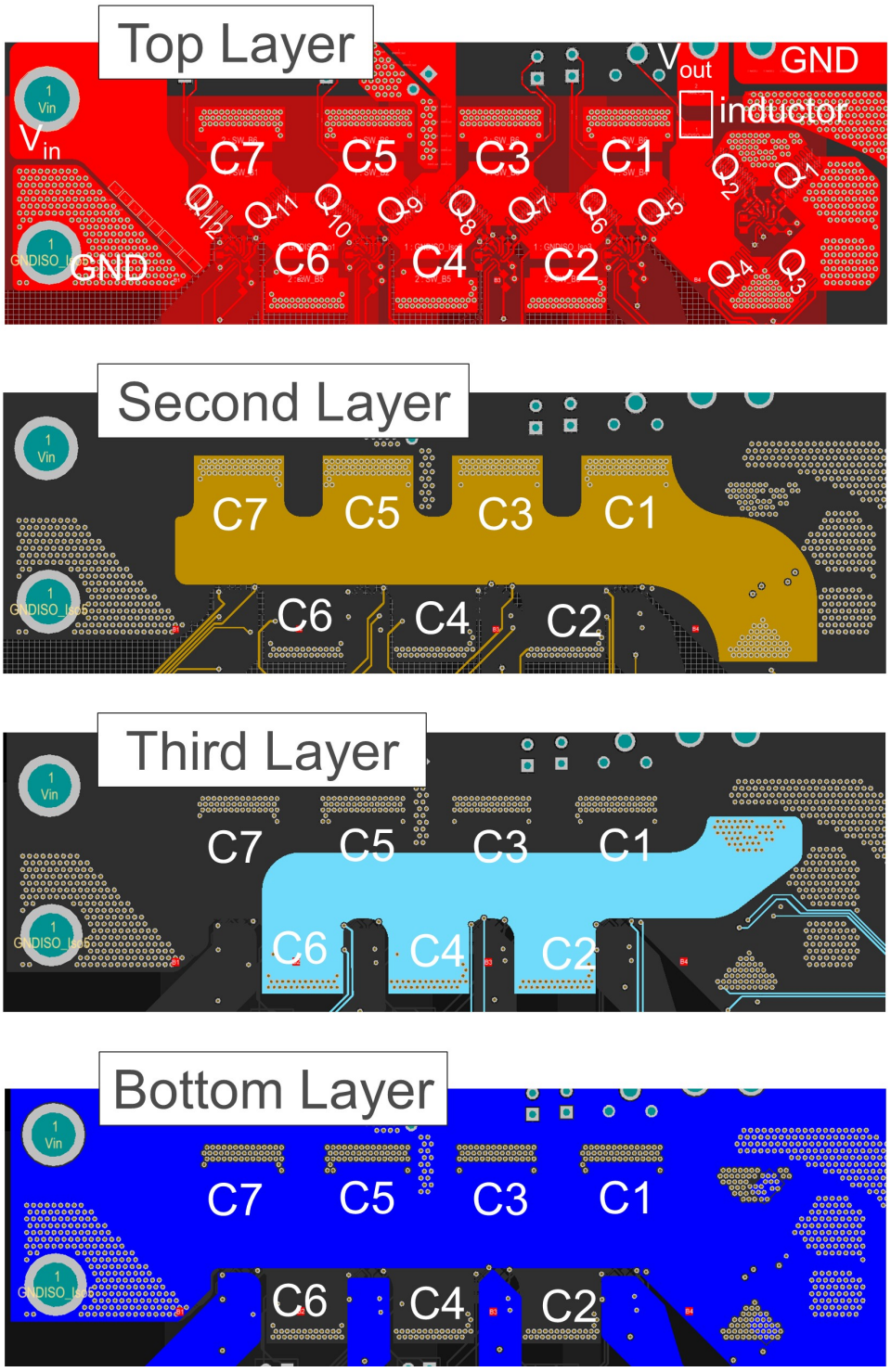


Figure 4.16: PCB 3 Altium layers designed for field cancellation.

To confirm whether the parasitic inductance of the commutation loops were reduced, ANSYS Q3D Extractor software was used to extract the parasitic inductance of selected loops. The software uses method of moments (integral equations) and finite element methods (FEM) to compute the parasitics of a PCB. Simulations were conducted for the Phase 1a loop (Fig.4.18) and the Phase 2a loop. The simulations were ran at 1MHz. Ideal copper connections were placed across device and capacitor footprints to connect the traces forming the commutation loop. The results show that PCB 2 has the highest loop inductance in each phase. Furthermore, layering the traces of the commutation loops directly on top of one another significantly reduced the loop inductance in PCB 3. The Q3D results are provided in Table 4.4 and Table 4.5.

Table 4.4: Q3D results for commutation loop during Phase 2a for PCB 1-3.

PCB Revision	$R_{ac}(\text{m}\Omega)$	$L(\text{nH})$
PCB 1	3.5	7.250
PCB 2	5.9	8.54
PCB 3	2.705	4.907

Table 4.5: Q3D results for commutation loop during Phase 1a for PCB 1-3.

PCB Revision	$R_{ac}(\text{m}\Omega)$	$L(\text{nH})$
PCB 1	11.9	21.21
PCB 2	6.876	14.744
PCB 3	5.748	8.622

The Q3D results show that PCB 3 has the lowest loop inductance when compared to the other PCB revisions. The experimental waveforms for the 4:1 topology of PCB 3 are provided in Fig. 4.19b. In comparison, the experimental waveforms show less ringing than the previous two boards.

To further improve the layout, the traces in PCB 3 connecting the flying capacitor to the regulating half-bridges were made larger to decrease trace resistance. The GaN devices were

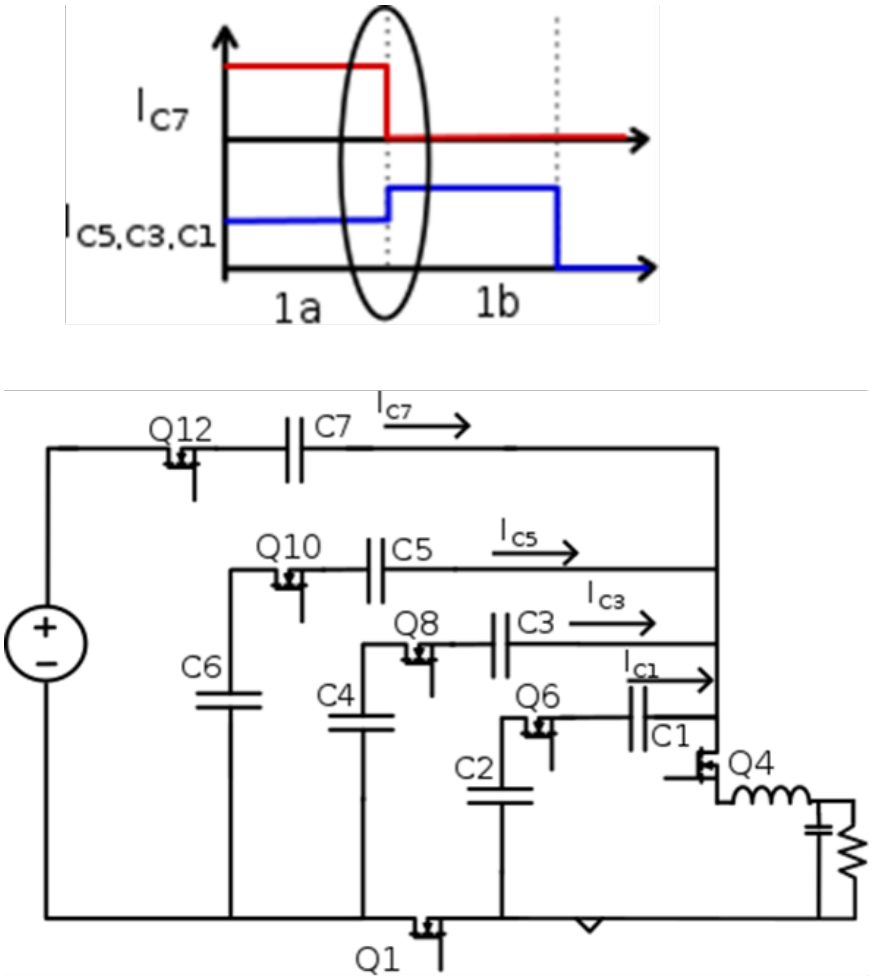
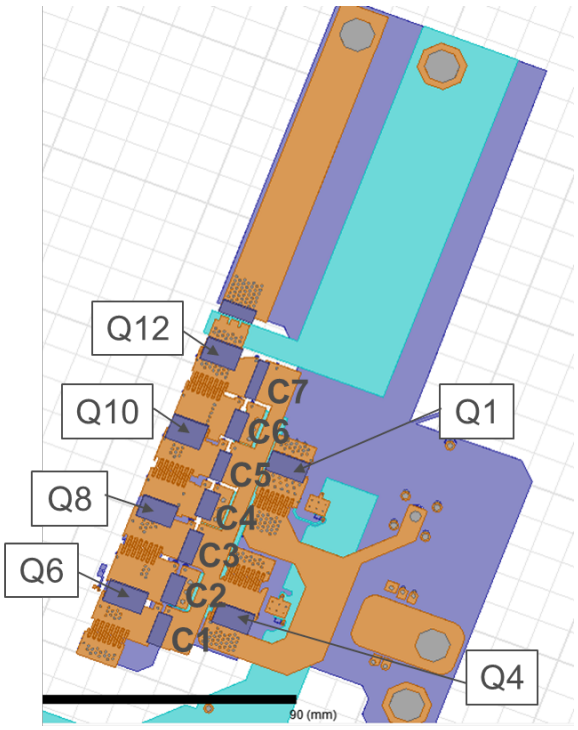
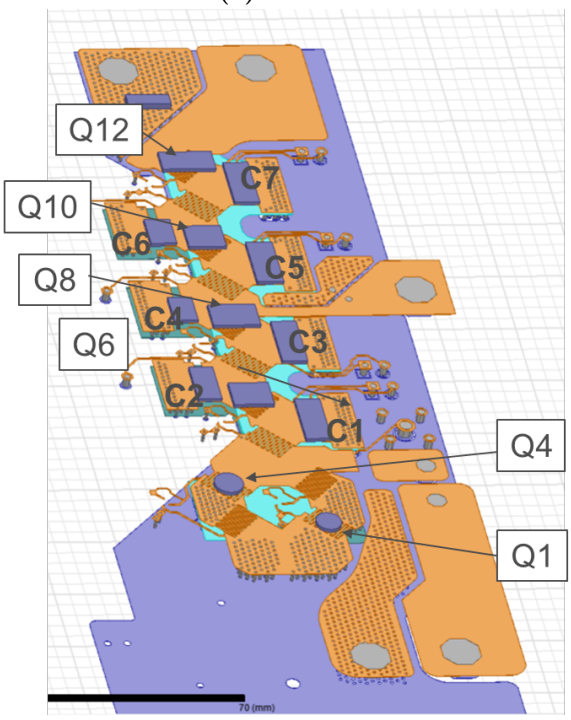


Figure 4.17: Circuit for measured loop inductance of Phase 1a with a constant load current.



(a) PCB 2.

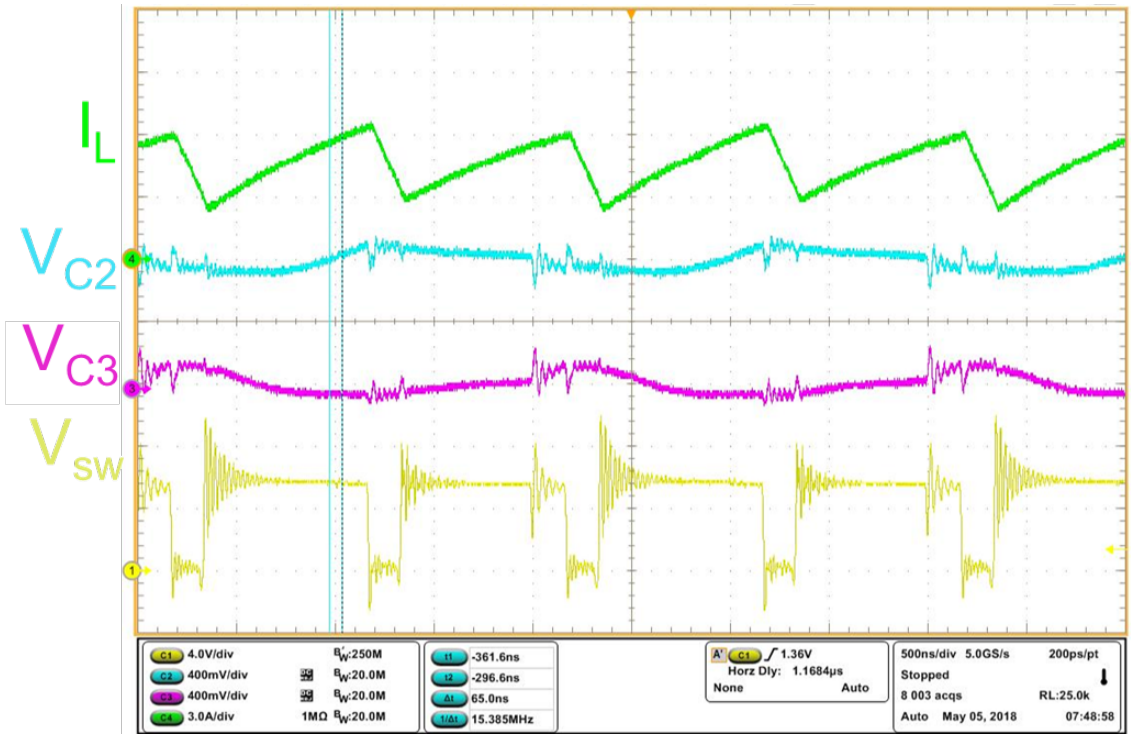


(b) PCB 3.

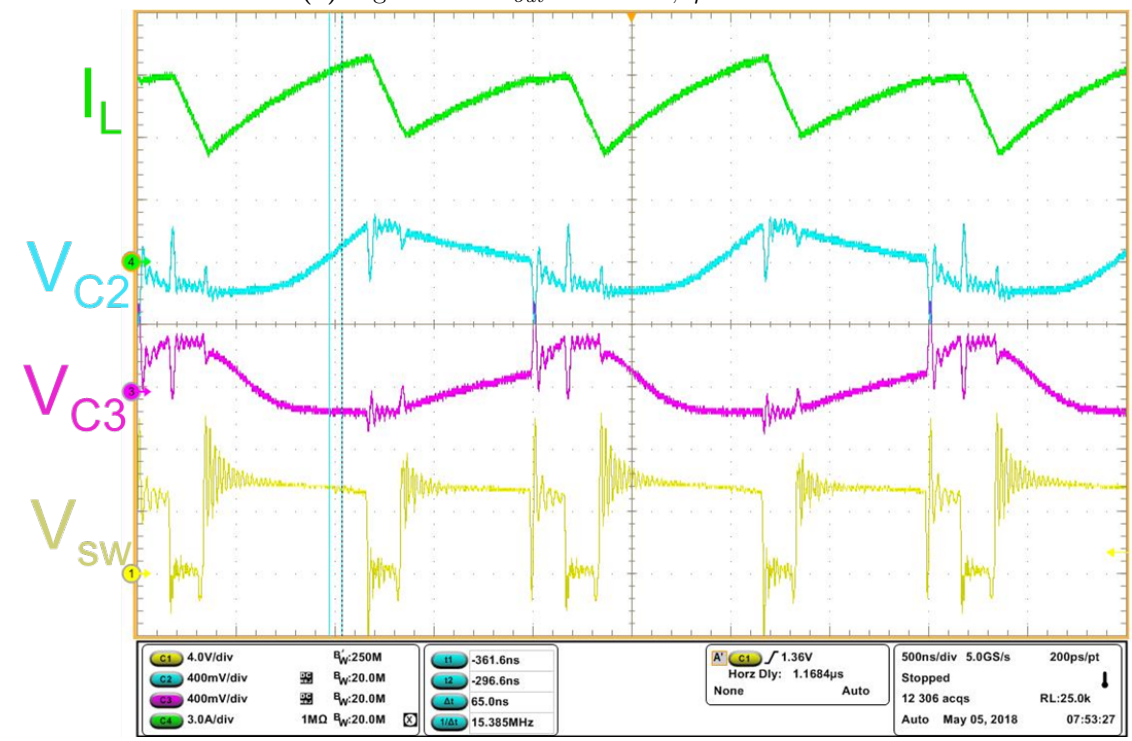
Figure 4.18: Q3D simulation for Phase 1a parasitic loop inductance.

placed at a 45-degree angle to improve the current sharing between the GaN devices. By angling the devices current can be more evenly distributed across each of the drain-source pins and the on-resistance of the pad will be low compared to a device with sharp corners in the conducting path where current crowds at one end and only a few of the drain-source traces are used to conduct current.

The experimental efficiency curve of PCB 3 is compared to PCB 2 in Fig. 4.20. The efficiency curve of PCB 3 does not drop off as quickly as does PCB 2. This is in part due to the reduced trace resistance in each flying capacitor loop. The DC resistance was measured in each of the flying capacitor loops by soldering wires on either side of the trace and sending 2A of current through. Using a multimeter the voltage was measured on either side of the trace. Using Ohm's law the DC resistance could be calculated. The conducting paths for C_3, C_2 and C_1 of PCB 2 and PCB 3 are compared in Table 4.6.



(a) Light Load: $P_{out} = 21.73W$, $\eta = 95.2\%$.



(b) Heavy Load: $P_{out} = 67.8W$, $\eta = 90.6\%$.

Figure 4.19: PCB 3 4:1 waveforms: $V_{in} = 24V$, $f_s = 500kHz$.

Table 4.6: Trace Resistance Comparison between PCB 2 and PCB 3

	R_{trace} PCB 2	R_{trace} PCB 3
C_3 trace	4mΩ	2.3mΩ
C_2 trace	15mΩ	2.3mΩ
C_1 trace	4mΩ	1.1mΩ

The Q3D simulation in Fig. 4.20 shows a significant improvement between the current density in PCB 2 and PCB 3. Aside, from increasing the area of the traces connecting the flying capacitors to the output, the sharp corners of traces and planes were redesigned as well. In PCB 2 current crowding was high at the corners of traces and power planes. In PCB 3 the edges of traces and planes were rounded which further improved the current density. Thermal images were taken with the FLIR-T630sc thermal camera and are provided in Figs. 4.22b and 4.22d. The images confirm the Q3D simulation. PCB 3 has a better thermal performance, operating at a lower temperature at a higher power when compared to PCB 2.

4.4.4 Loss Model

In this section the loss mechanisms of the converter are introduced and used in an analytical loss model. The loss model was evaluated using a constant load current and applied to the experimental results for PCB 3 in the 4:1 configuration. The operating point parameters are provided in Table 4.7.

The efficiency curve generated from the analytical loss model is then compared to the experimental results in Fig. 4.24.

Coss Loss

The output capacitance is the sum of the gate-to-drain capacitance, C_{gd} and drain-to-source capacitance, C_{ds}.

$$C_{oss} = C_{gd} + C_{ds} \tag{4.4}$$

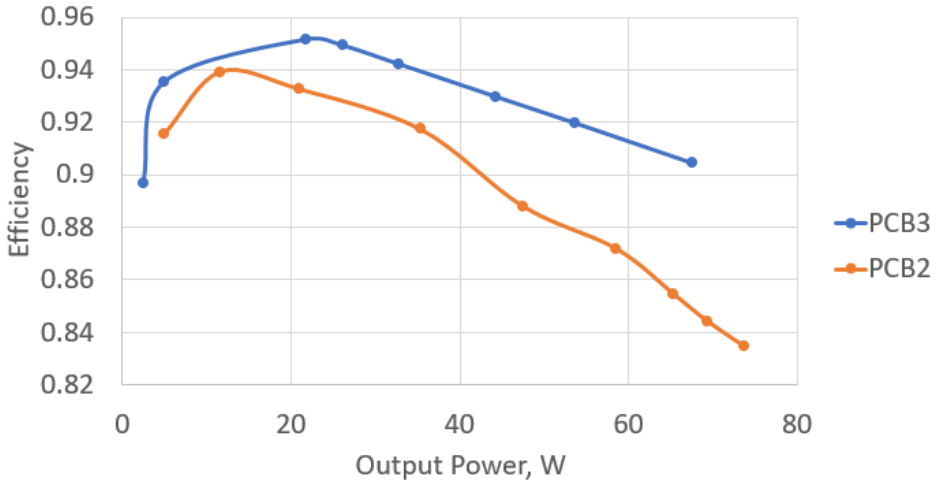
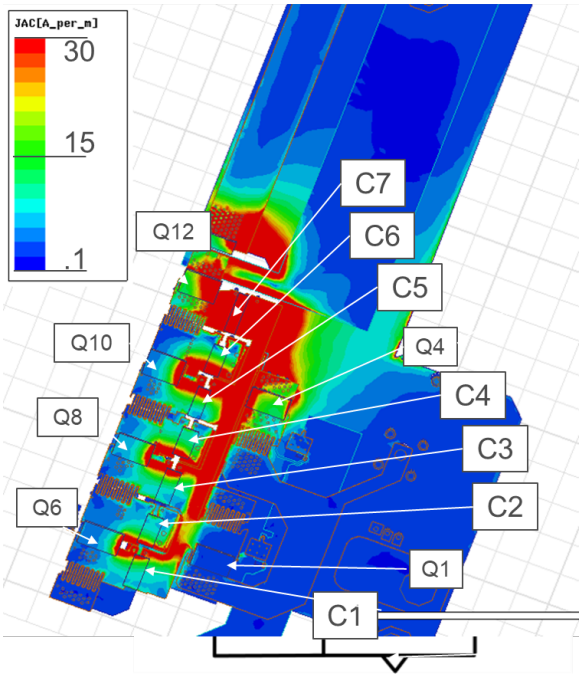


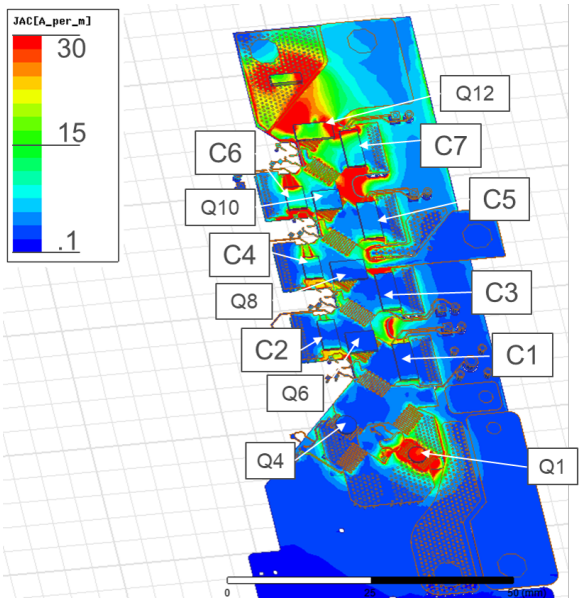
Figure 4.20: Experimental efficiency comparison between PCB 2 and PCB 3.

Table 4.7: Operating Conditions for 4:1 Loss Model and Testing.

Parameter	Value
V_{in}	24V
V_{out}	5V
D	.833
f_s	500kHz
C_{fly}	(3) 4.7μ F, 5mΩ
L	10nH, 20.5mΩ
wire	80nH, 4.7mΩ

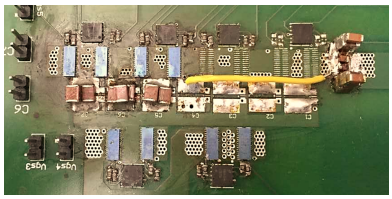


(a) PCB 2: Phase 1a.

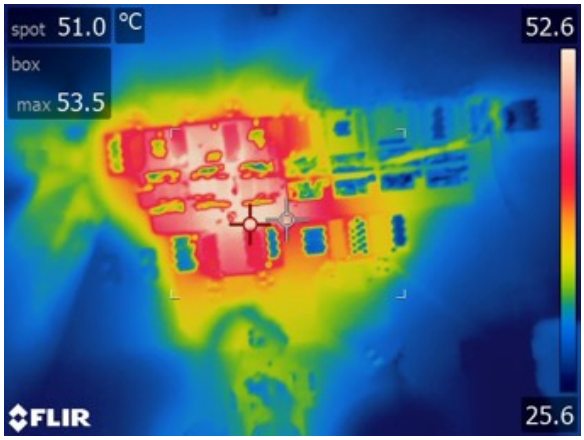


(b) PCB 3: Phase 1a.

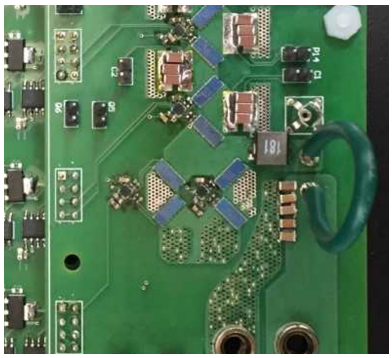
Figure 4.21: Q3D simulation of current density for Phase 1a.



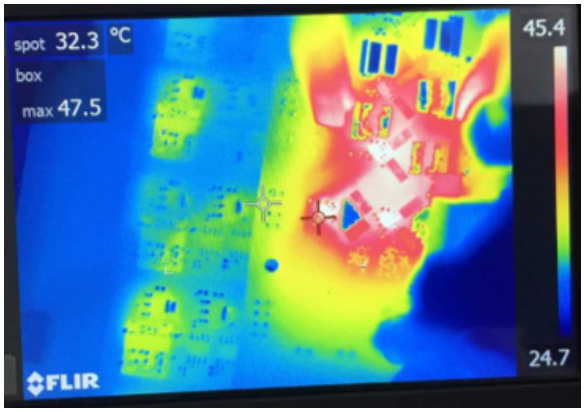
(a) PCB 2



(b) PCB 2, $P_{out} = 53W$



(c) PCB 3



(d) PCB 3, $P_{out} = 67W$

Figure 4.22: Comparison of thermal images for PCB 2 and PCB 3 in the 4:1 configuration.

C_{oss} is a non-linear voltage dependent parasitic. In [93] an equivalent linear capacitance that stores the same energy, $C_{eq,E}$ or charge, $C_{eq,Q}$ as the non-linear model can be calculated using the non-linear capacitance data.

$$C_{eq,E} = \frac{2}{V_c^2}\int_0^{V_c} vC_x(v)dv \tag{4.5}$$

$$C_{eq,Q} = \frac{1}{V_c}\int_0^{V_c} C_x(v)dv \tag{4.6}$$

This capacitance is not dependent on voltage and can more accurately model the turn-off switching loss in Equation 4.7.

$$P_{coss} = \frac{1}{2}C_{oss}V_{ds}^2 f_s \tag{4.7}$$

V_{ds} for each device can be related to the output. For Q_1-Q_4, V_{ds}=V_{out}, for Q_5-Q_8 V_{ds}=$2V_{out}$. Accounting for the voltage ripple ΔV which can be represented as a fraction of V_{out}, enables a more accurate representation of the turn-off loss. For a voltage ripple of 10% V_{out} the equivalent loss becomes,

$$P_{coss,Q5-Q8} = \frac{1}{2}C_{oss}(2.1)V_{out}^2 f_s \tag{4.8}$$

Gate Charge Loss

Gate charge, Q_g is calculated from the current required to switch the FET from V_{gs}=0 to when V_{gs}=V_{dr} reaches the maximum driving voltage which occurs at time, t_r as seen in Fig. 4.23.

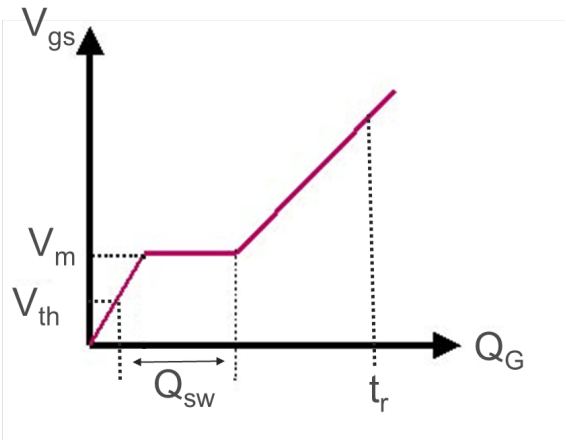


Figure 4.23: Gate charge plot.

$$Q_g = \int_0^{t_r} i_g dt \tag{4.9}$$

The power loss can then be calculated as

$$P_{Q_g} = V_{dr} Q_g f_s \tag{4.10}$$

Conduction Loss

The conduction loss is calculated by summing the device on-resistance, $R_{ds,on}$, the capacitor series resistance, ESR, and the trace resistance, R_{trace}. Assuming a constant load current and a constant current through each capacitor during each phase the conduction losses can be calculated as

$$P_{cond.} = I_{avg}^2 (R_{ds,on} + ESR + R_{trace}) \tag{4.11}$$

The conduction loss due to the output inductor can be calculated using the inductor's equivalent series DC resistance, R_{DCR}, and with a constant output current I_{rms}=I_{avg}.

$$P_{ind.} = I_{rms}^2 R_{DCR} \tag{4.12}$$

A wire was added in series with the output inductor so that the inductor current could be measured with a current probe. The resistance of the wire was lumped into the inductor's DCR. In this testing configuration a large inductance of 10μH was used to maintain a constant output current. If the output rms current I_{rms} was larger than I_{avg} then the ac resistance, R_{ac}, of the inductor would need to be accounted for. The loss due to the ac and dc resistance of the inductor can be calculated using the following equation

$$P_{ind.ac,dc} = I_{rms}^2 R_{DCR} + \Delta i^2 R_{ac} \tag{4.13}$$

where Δi, is the output current ripple.

Using the above loss model, Fig. 4.24 shows the comparison between the analytical loss model and the experimental results. Gate charge loss was not included in the final model due to the gate drive circuitry being powered by a different power supply than the power stage. The loss breakdown of the 4:1 converter operating at 59W is provided in Fig. 4.25. The largest loss is caused by DCR conduction loss of the inductor. The 10uh inductor was replaced with a smaller 180nH and 1.3 mΩ DCR inductor. The overall efficiency improved by approximately 1%. The efficiency curves are compared in Fig. 4.26. The 180nH inductor introduced ac resistive losses that the 10μH inductor did not have. The ac resistive losses limited the overall efficiency improvement. Therefore, to reduce the output inductor conduction loss multiple inductor could be used in parallel. The trade-off would be diminished power density and added costs for the added inductors.

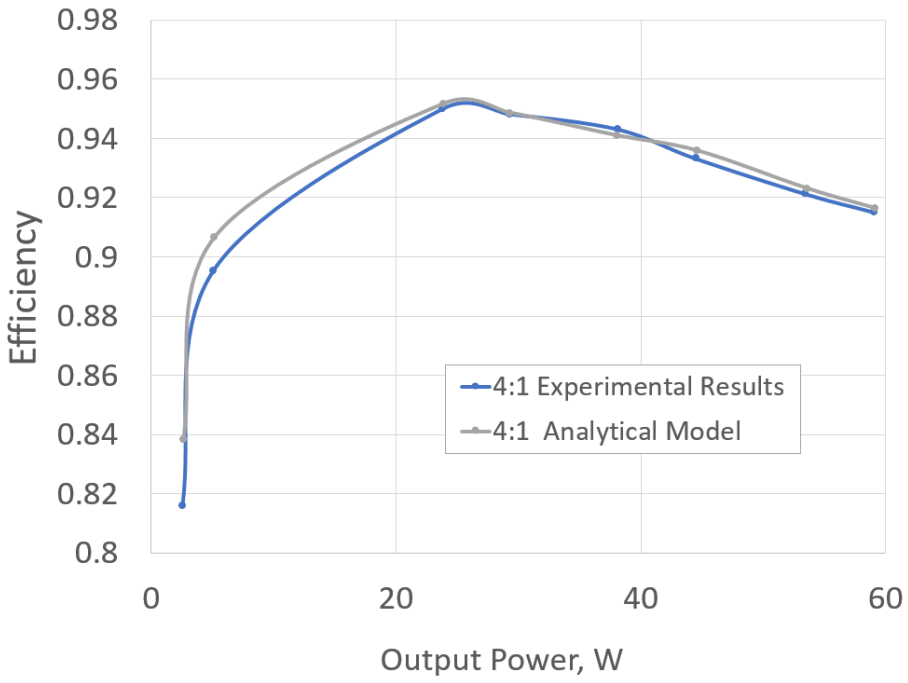


Figure 4.24: Efficiency curve validation for the 4:1 HDSC.

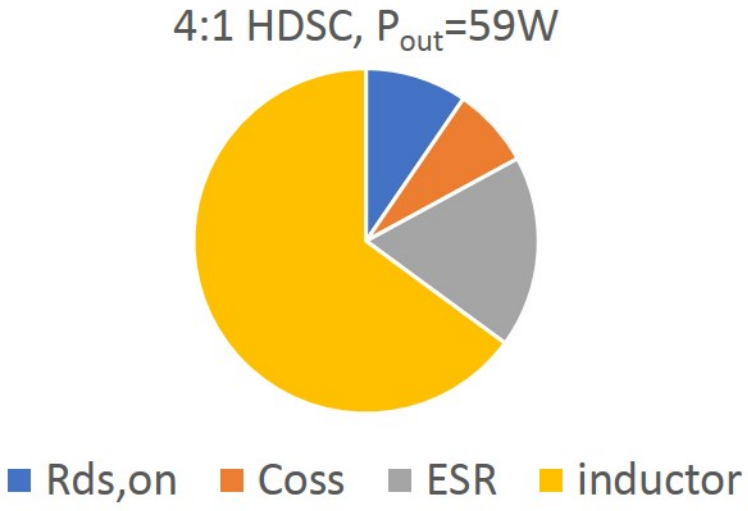


Figure 4.25: 4:1 loss distribution at an output power of 59W, $\eta = 90.3\%$.

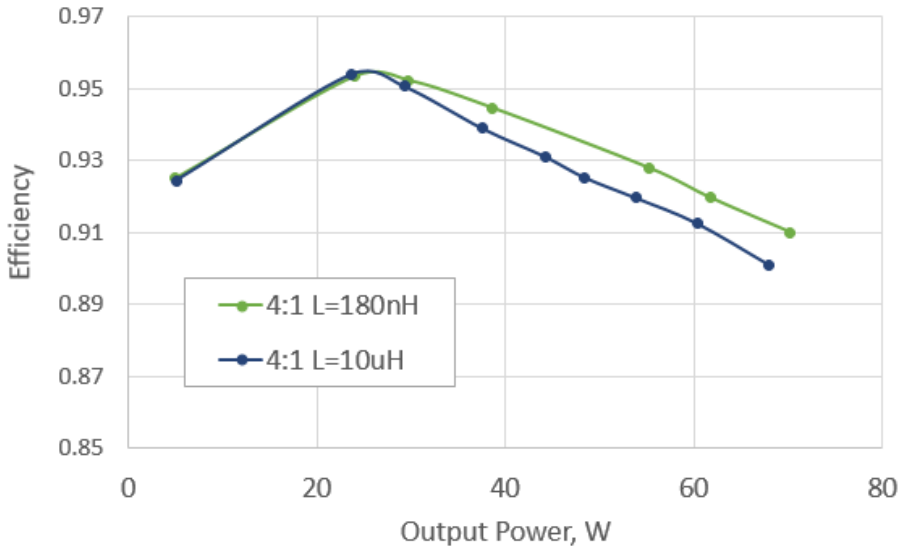


Figure 4.26: Efficiency comparison for L=10uH and L=180nH.

4.4.5 HDSC 8:1 Printed Circuit Board 3

PCB 3 was also tested in the 8:1 configuration with 12 devices (EPC2023C) and 7 flying capacitors (TDK-CGA6M3X7S2A475K200AB). The populated board is provided in Fig. 4.27. The experimental results are provided in Fig.4.28a and Fig. 4.28b. Ringing on V_{sw} was minimal. The testing parameters are listed in Table 4.8.

The 8:1, 48V-5V converter was tested up to an output power of 100.8W (89.9%) with a maximum efficiency of 95%. The experimental efficiency results are provided in Fig. 4.29.

4.5 Modeling Hard-Charging Loss for Varying C_{fly}

As stated previously, the flying capacitors of the HDSC are DC biased with a voltage that depends on the conversion ratio and input voltage. For the 4:1 HDSC with an input of 24V, the flying capacitors, C_1, C_2 and C_3 are biased at 6V, 12V and 18V respectively. For Class II ceramic capacitors as the DC bias increases the nominal capacitance decreases. In Section 3.6 the timing intervals for the split phase intervals were determined based on an ideal equivalent capacitance. If the capacitance changes the load current will distribute differently than in the ideal case, effecting the rate of change of the voltage across the capacitor in a given interval. If

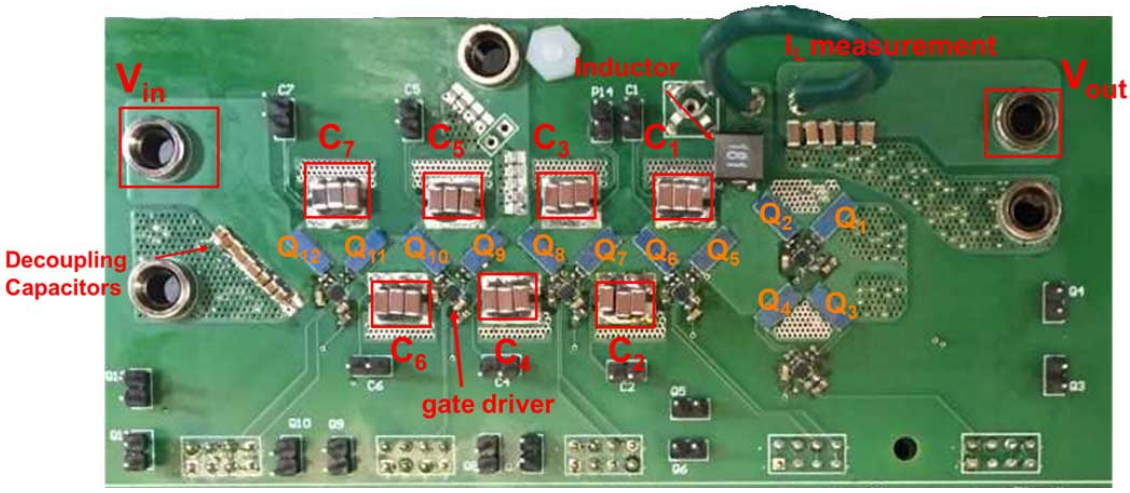
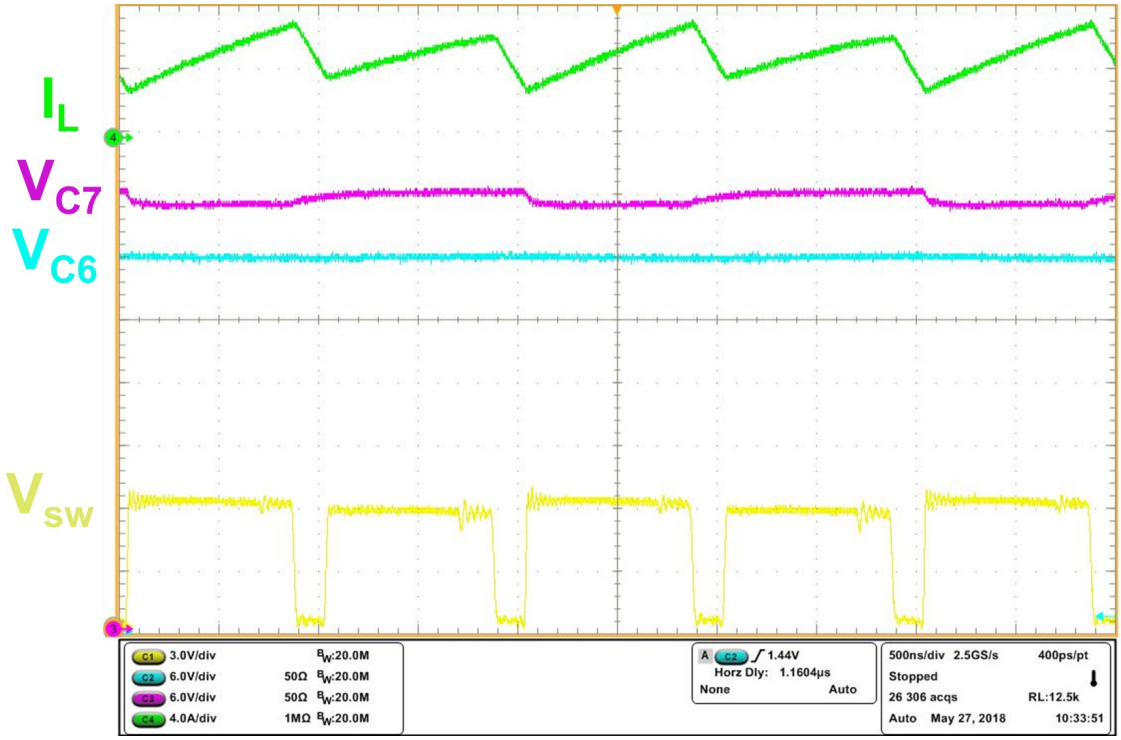


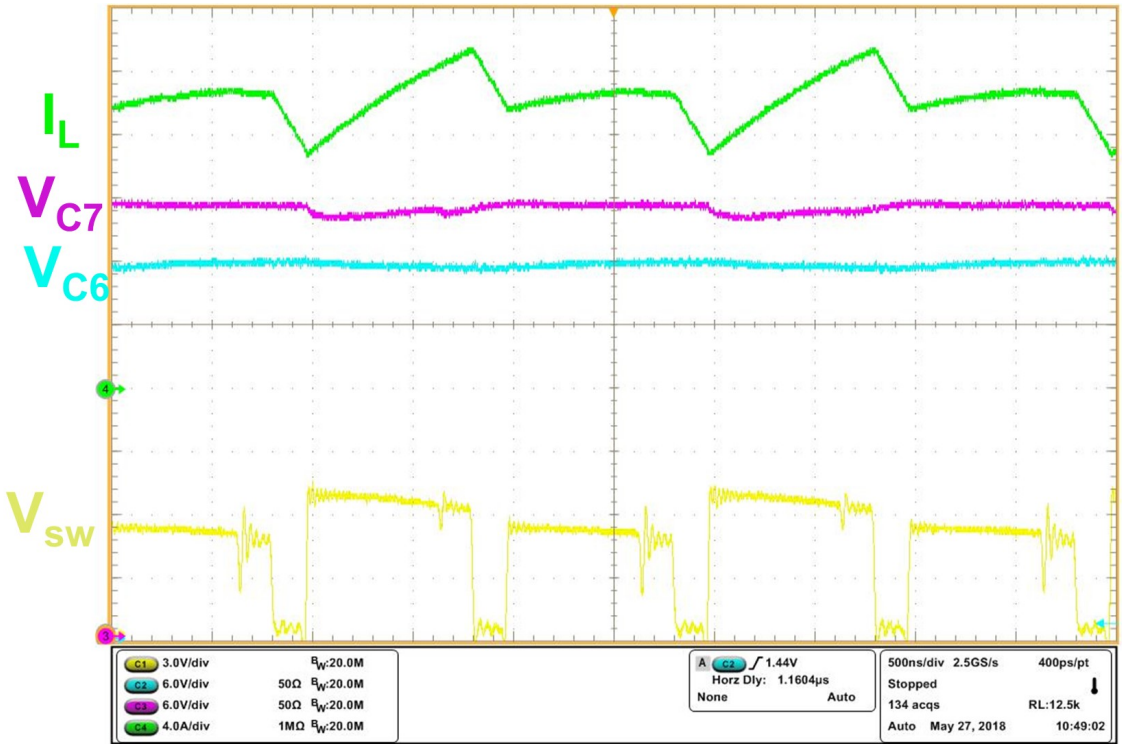
Figure 4.27: PCB 3 populate for 8:1 conversion ratio.

Table 4.8: 8:1 Testing Parameters

Parameter	Value
V_{in}	48V
V_{out}	5V
D	.833
f_s	500kHz
C_{fly}	(3) 4.7uF, $5m\Omega$
L	180nH, $R_{dc} = 1.5\text{m}\Omega$,$R_{ac} = 8.8\text{m}\Omega$
wire	80nH, $R_{dc} = 4.7\text{m}\Omega$,$R_{ac} = 13.5\text{m}\Omega$



(a) Light Load: $P_{out} = 24.2W$, $\eta = 94.2\%$.



(b) Heavy Load: $P_{out} = 100.8W$, $\eta = 89.6\%$.

Figure 4.28: PCB 3 8:1 waveforms $V_{in} = 48V$, $f_s = 500kHz$.

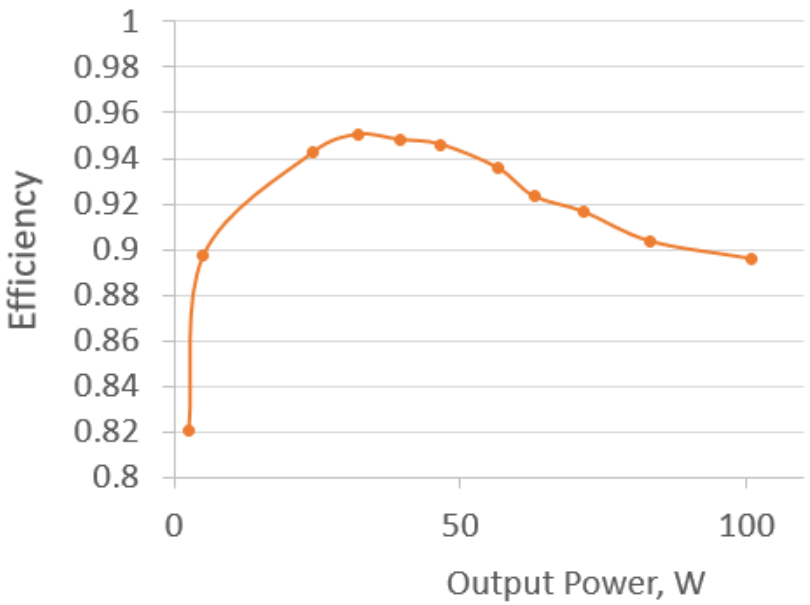


Figure 4.29: 8:1 experimental efficiency.

the rate of change for the voltage across a capacitor changes, the time required to achieve soft-charging will also change. If the timing remains constant, hard-charging will occur. In this section hard-charging losses are analyzed for a range of capacitances, 1-14μF, for each flying capacitor. The analytical capacitor voltage waveforms are calculated based on Equations 3.20-3.28. For each capacitance level the equations are iterated until they reach a steady-state. To determine whether hard-charging loss is occurring, the experimental waveforms of the voltage across each of the flying capacitors in the 4:1 configuration was measured experimentally and compared to the analytical model. Fig. 4.30 compares the experimental capacitor voltage ripple to the analytical model. The analytical model accurately captures the peak to peak voltage ripple.

With the capacitor voltage ripple accurately captured, the waveforms can be added to each other to obtain the KVL equations that occur for each phase transition. This analysis was done for $V_{C,fly1-3}$ of PCB 2 and PCB 3 with a constant output current. The waveforms are compared in Fig. 4.31 and 4.32. In Fig. 4.31a, the experimental waveforms of PCB 2 resonate around the analytical model, such that by the end of Phase 1a there is hard-charging. Fig. 4.31b, shows how reduced resonance around the analytical model and the experimental waveforms of PCB 3 show increased accuracy. A similar comparison was done

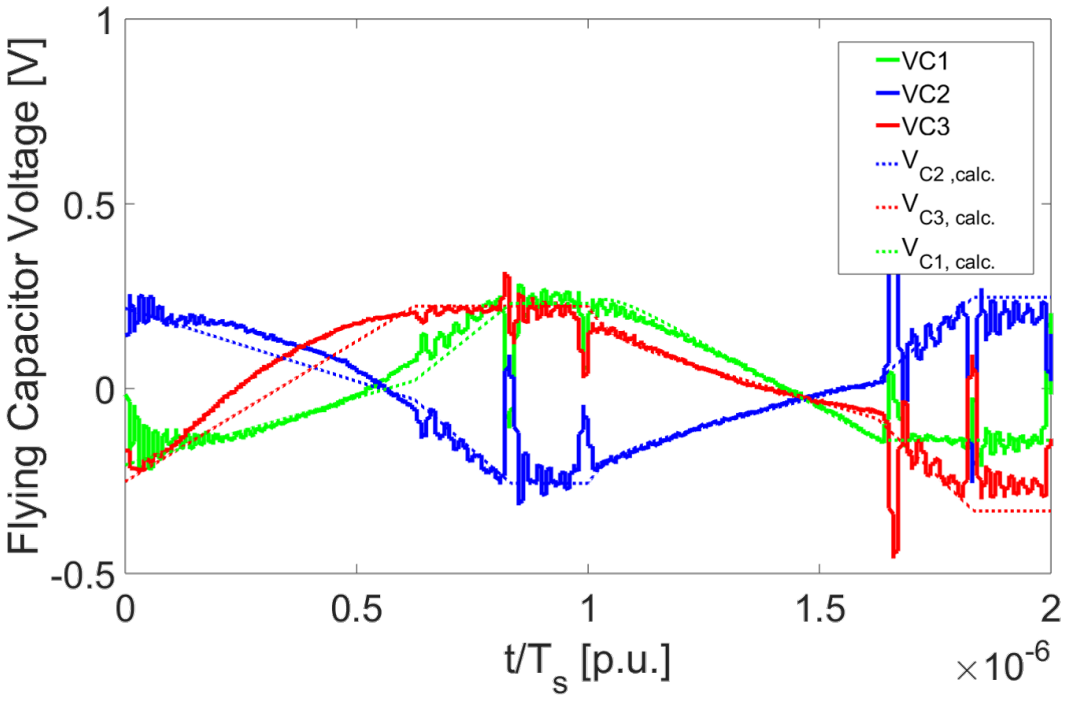
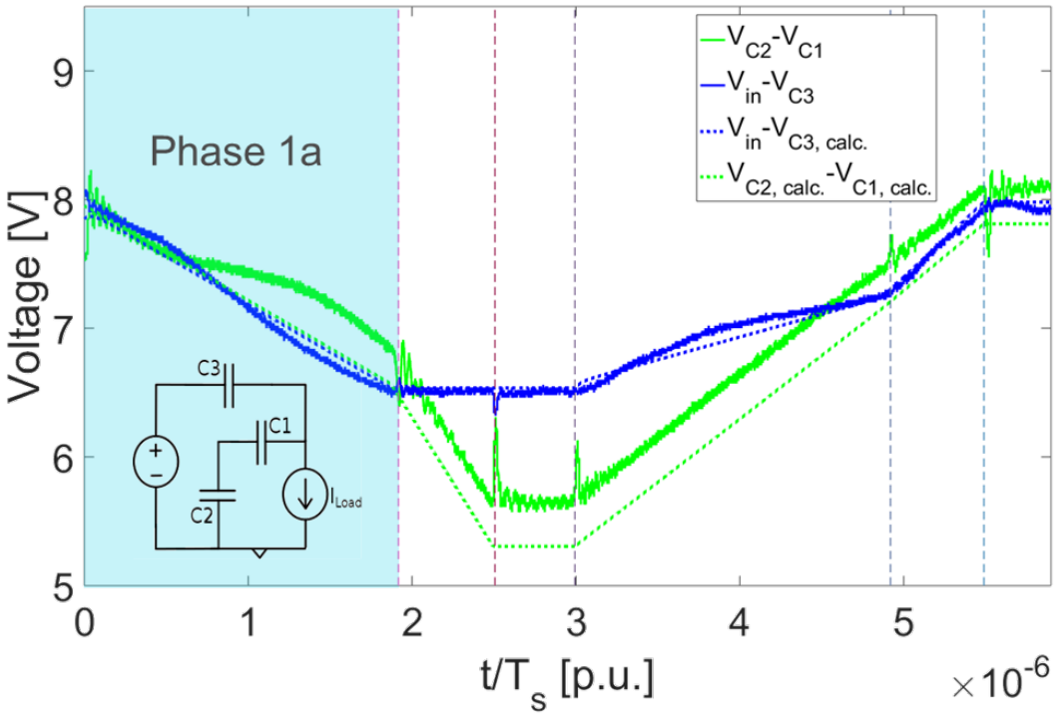
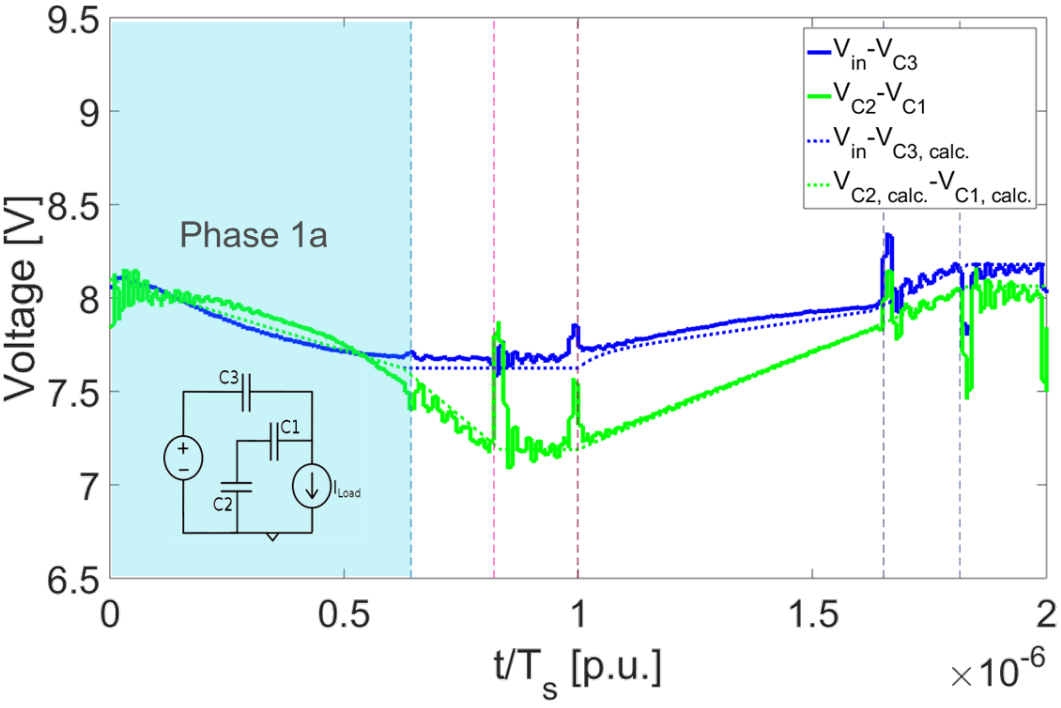


Figure 4.30: Comparing experimental capacitor voltages to analytical models.

for the transition to Phase 2a and is provided in Fig. 4.32a and Fig. 4.32b. Using the well matched analytical model of PCB 3, the waveforms can be adjusted to ensure steady state operation . As stated earlier the charge flow vectors used to calculate the timing for the split phase interval are calculated based on each of the flying capacitors being equal. However, given the characteristics of Class II ceramic capacitors the capacitance depreciates non-linearly with a DC bias voltage. Using the analytical model that accurately captures the capacitor voltage ripple, the voltage ripple can be modeled over a range of capacitances. Models were calculated for varying C_1, C_2 and C_3. Fig. 4.33 shows a varying C_3 voltage ripple, where 14μF provides almost a constant voltage and C_3=1μ F results in a very large voltage ripple. Each of the capacitor voltages iterates through voltage waveforms until the steady state waveform is found for a given C_3. For each value of C_3 that the model iterates through, the varying capacitor voltage ripple can be reconfigured into the original KVL equations and it can be determined whether hard-charging is occurring. From these KVL equations and Equation 3.7, the ΔV_{diff} is calculated and loss due to hard-charging can be modeled based on a varying capacitance. The power loss curves for hard charging that



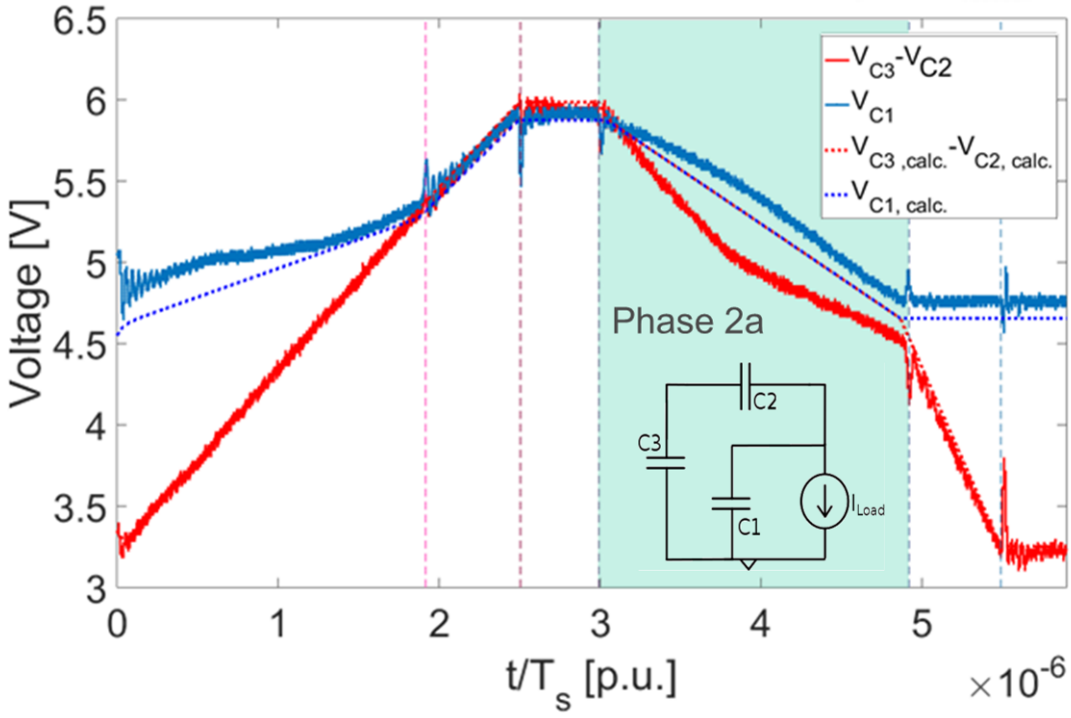
(a) PCB 2



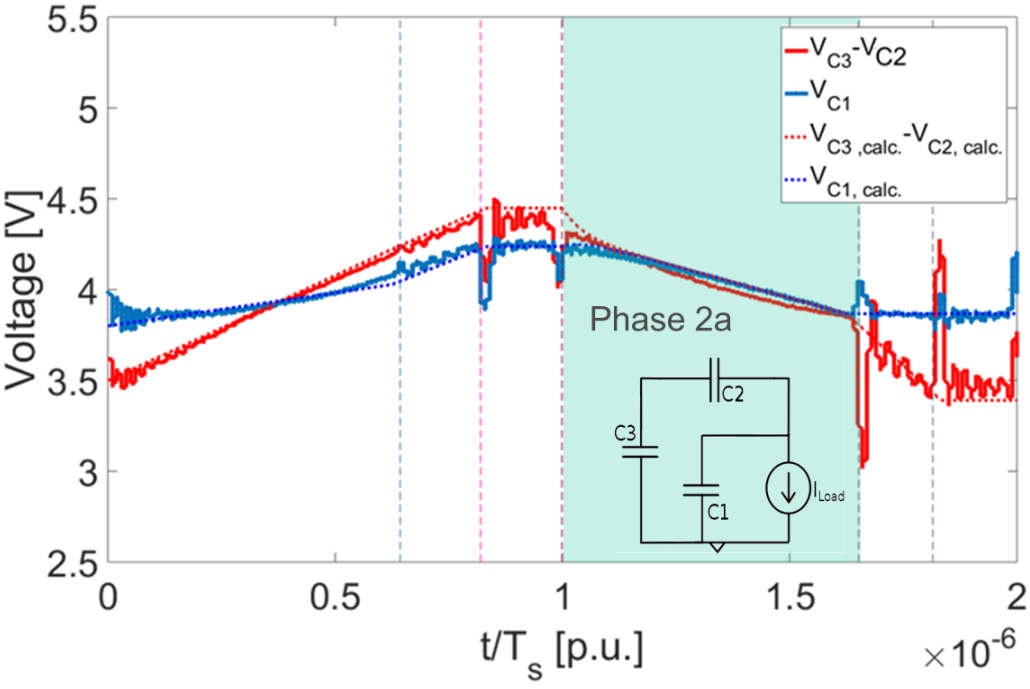
(b) PCB 3

Figure 4.31: Experimental and analytical waveforms of $(V_{in} - V_{C3})$ and $(V_{C2} - V_{C1})$.

occurs in Phase 1a and 2a due to voltage mismatch for a varying C_3 is provided in Fig. 4.36. The same analysis is done for C_2 and C_1. The results are provided in Fig. 4.39 and Fig. 4.42. The results from the hard-charging analysis show that when the nominal flying capacitance varies by over 50% hard-charging loss begins to occur. For the hard-charging losses analyzed at an output power of 59W, when the capacitance dropped below 30% of the nominal capacitance the losses due to hard-charging increased exponentially.



(a) PCB 2



(b) PCB 3

Figure 4.32: Experimental and analytical waveforms of $(V_{C3} - V_{C2})$ and (V_{C1}).

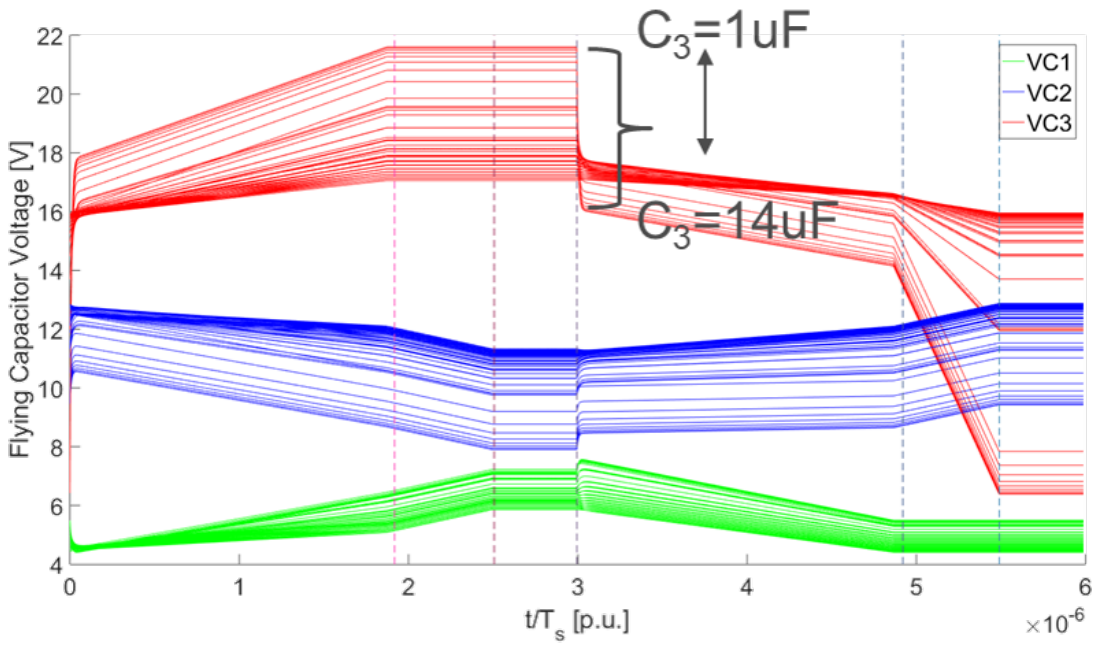


Figure 4.33: Varying C_3 voltage waveform in steady state.

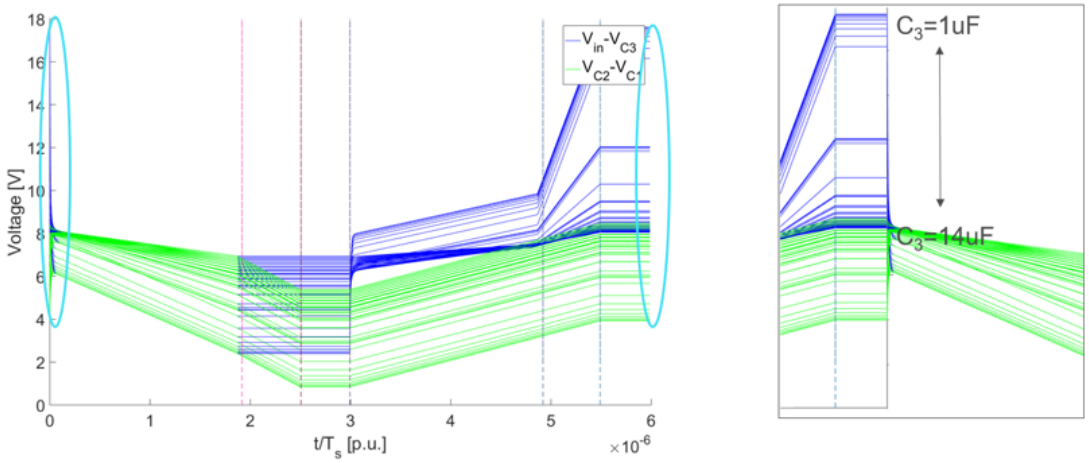


Figure 4.34: Hard-charging during transition to Phase 1a between inner leg and outer leg of capacitors as C_3 iterates through a range of values.

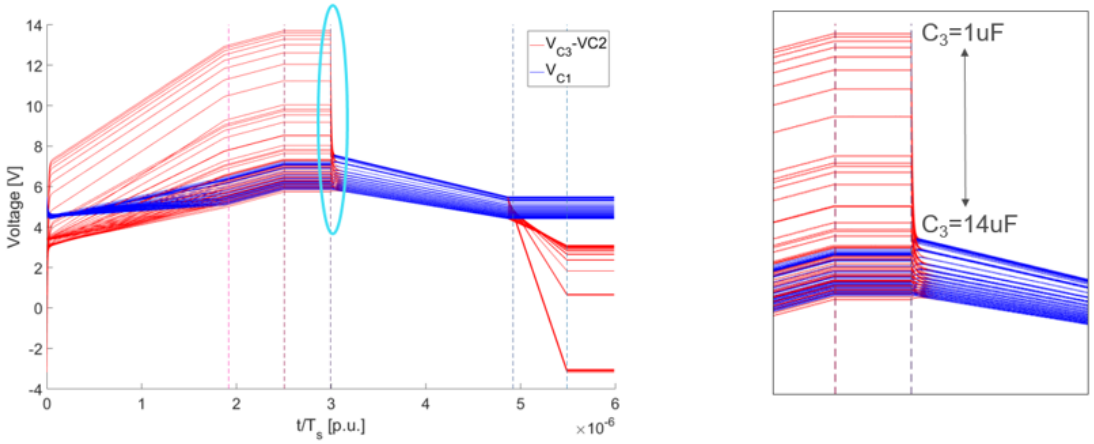
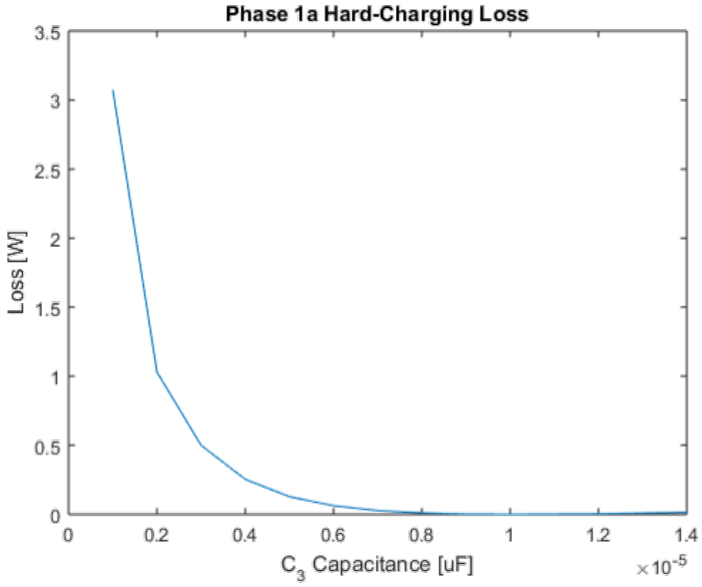
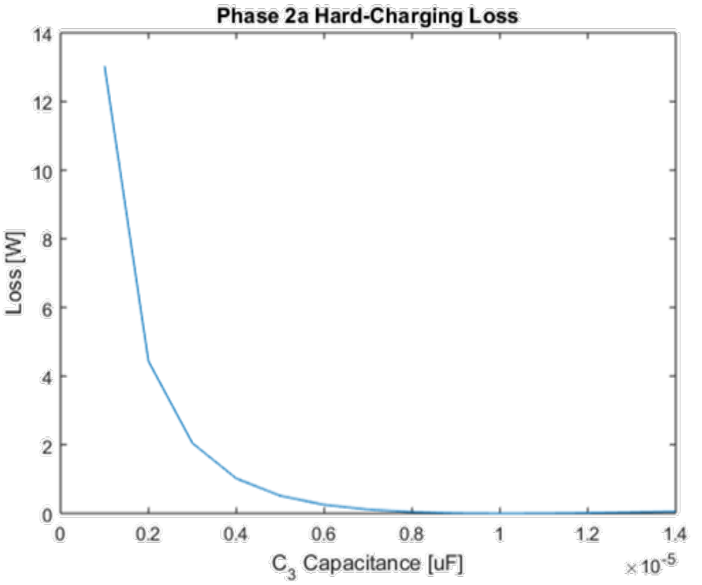


Figure 4.35: Hard-charging during transition to Phase 2a between inner leg and outer leg of capacitors as C_2 iterates through a range of values.



(a) Phase 1a



(b) Phase 2a

Figure 4.36: Hard-charging loss based on a varying C_3 capacitance.

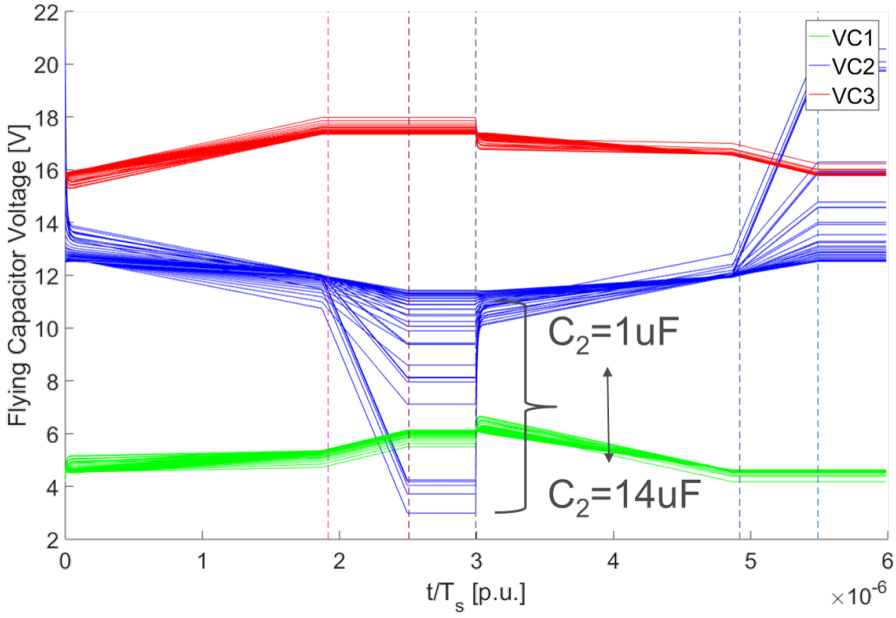
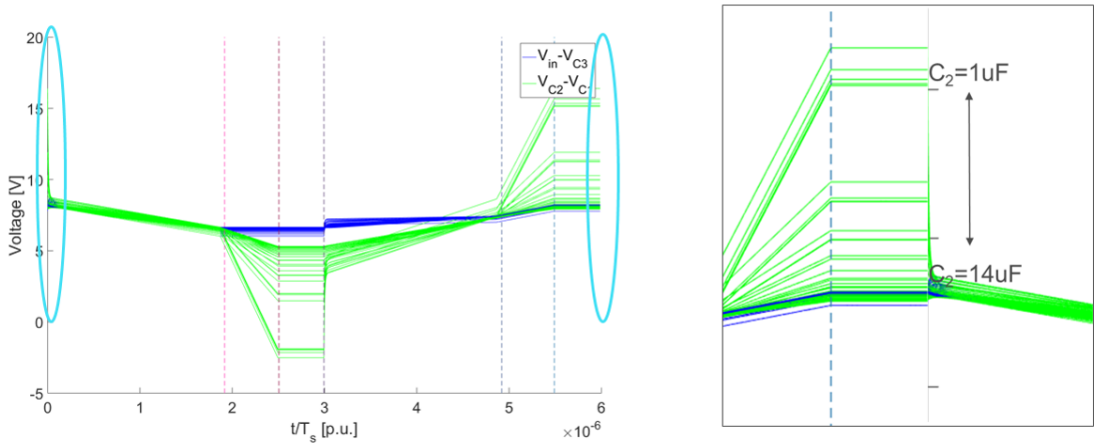
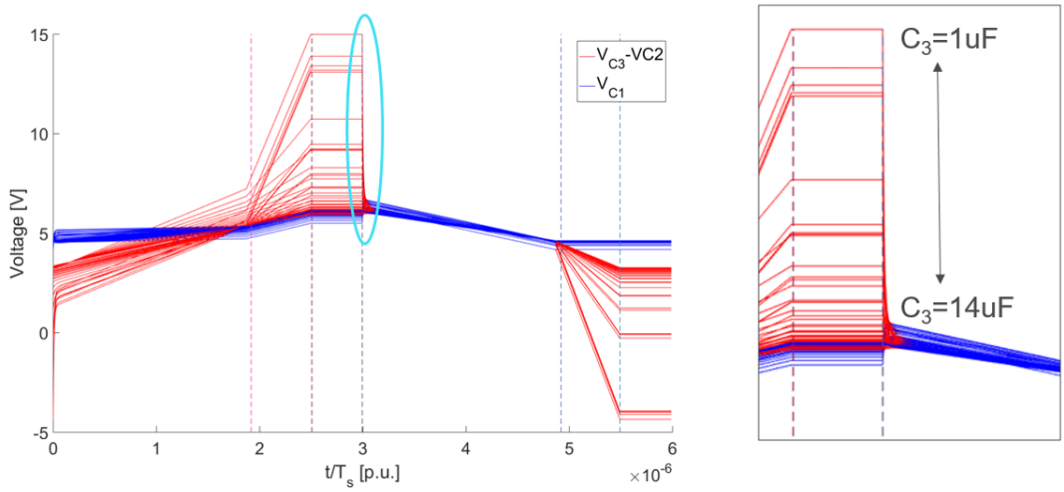


Figure 4.37: Determining steady-state voltage waveforms for a varying C_2.

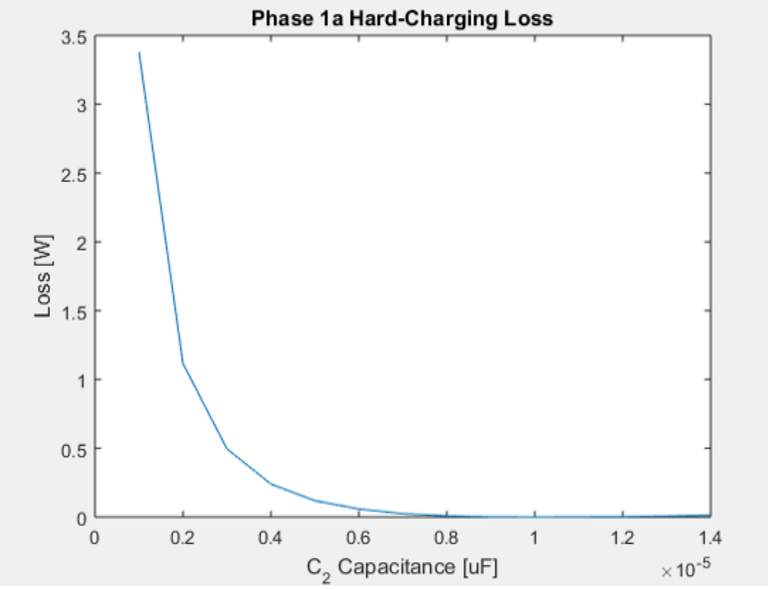


(a) Hard-charging during transition to Phase 1a between inner leg and outer leg of capacitors as C_2 varies.

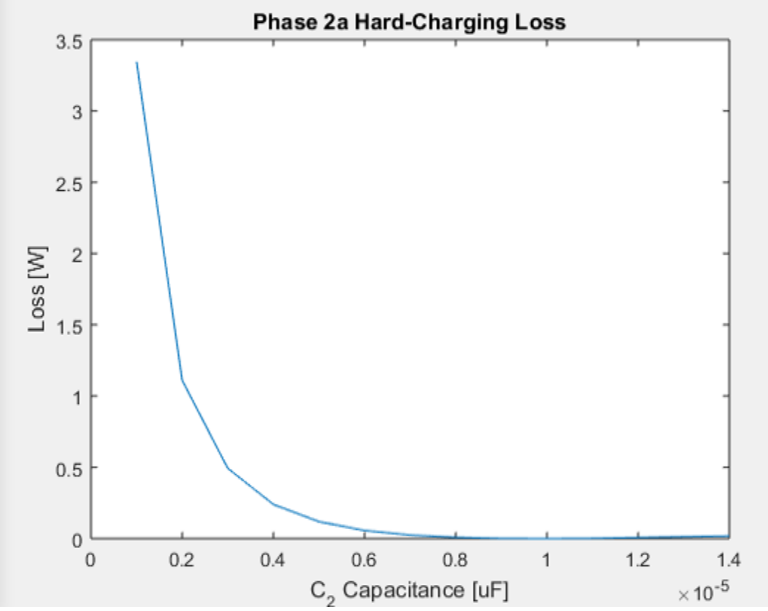


(b) Hard-charging during transition to Phase 2a between inner leg and outer leg of capacitors as C_2 varies.

Figure 4.38: Combined capacitor voltage branch equations to determine voltage mismatch between capacitors as C_2 varies.



(a) Phase 1a



(b) Phase 2a

Figure 4.39: Hard-charging loss for varying C_2.

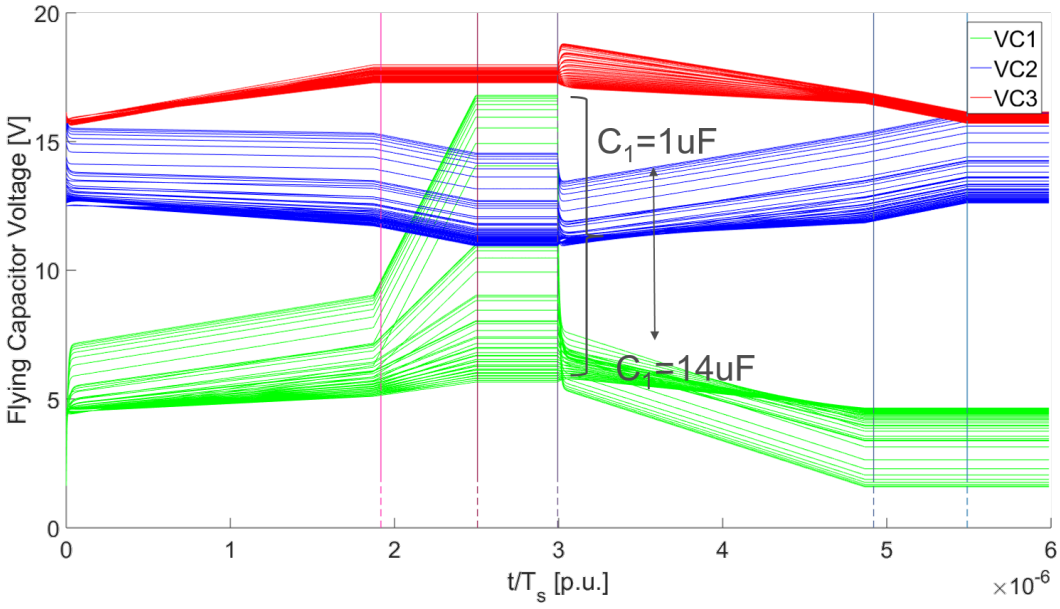
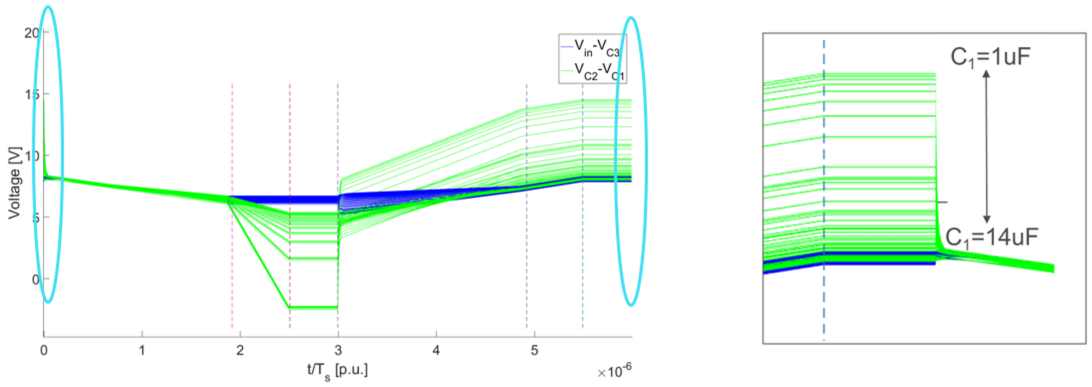
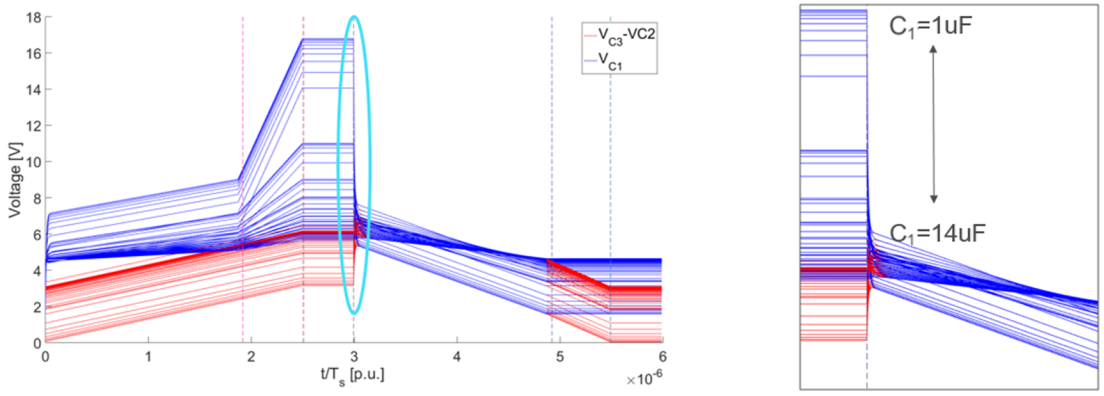


Figure 4.40: Determining steady-state voltage waveforms for a varying C_1.

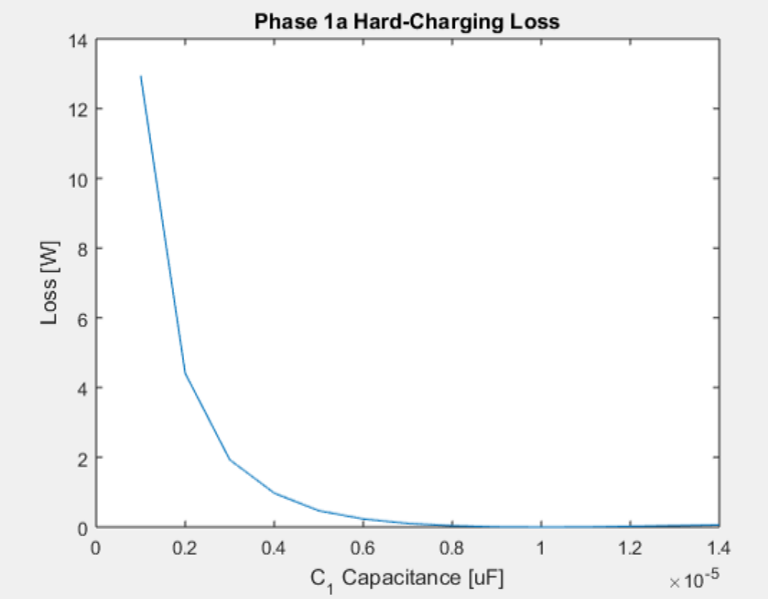


(a) Hard-charging during transition to Phase 1a between inner leg and outer leg of capacitors as C_1 varies.

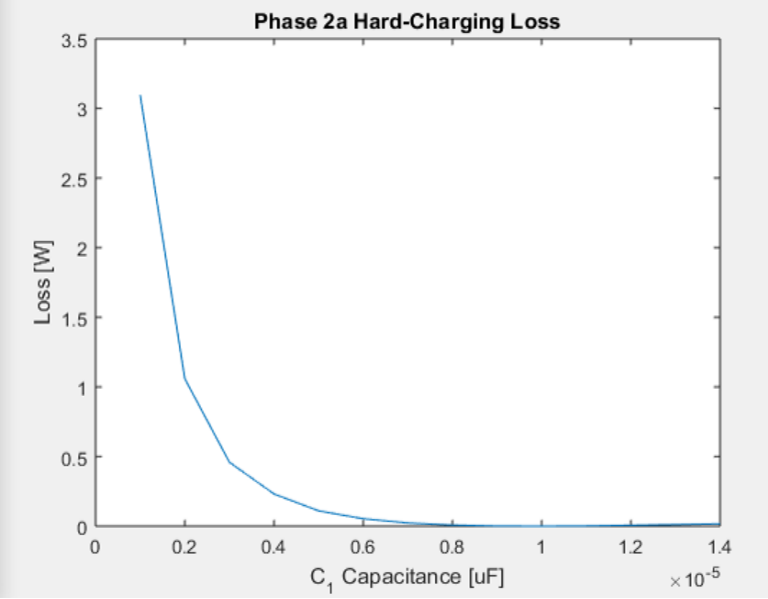


(b) Hard-charging during transition to Phase 2a between inner leg and outer leg of capacitors as C_1 varies.

Figure 4.41: Combined capacitor voltage branch equations to determine voltage mismatch between capacitors as C_1 varies.



(a) Phase 1a



(b) Phase 2a

Figure 4.42: Hard-charging loss for varying C_1.

Chapter 5

Conclusion and Future Work

Increasing the efficiency of the intermediate bus converter will enable a higher percentage of the power provided from the grid to reach the motherboard of the data center server. Increasing the power density of the IBC will enable the converter to be placed closer to the motherboard, reducing conduction loss due to connecting wires and also enable space for more modules, increasing computing density. Of the topologies reviewed in literature the dominant loss mechanisms were related to magnetics and conduction loss at the output. Further improvements were primarily limited to specialized magnetic design and paralleling components for decreased conduction loss, hindering power density. Switched capacitor converters offer high-power density solutions and do not depend on bulky magnetics to step down voltage. However, the efficiency of switched capacitor topologies are typically limited by hard-charging, a loss that results from shorting capacitors together with a voltage mismatch between them. The Hybrid Dickson Switched Capacitor topology eliminates hard-charging loss by incorporating a single inductor at the output and by incorporating additional subintervals, or phases, to reduce the voltage mismatch that occurs between the branches of the flying capacitors. The output inductor increases efficiency by allowing the output voltage to change instantaneously, compared to a SC that uses a capacitor at the output. The additional split phase intervals require no additional switches and therefore there is no trade-off in physical design complexity. The thesis research goals were to investigate whether the HDSC topology is a viable solution for the IBC.

Three 4:1 GaN based HDSC PCBs were designed and tested. The parasitics of each PCB layout was analyzed and the efficiencies were compared. The final design was able to achieve the lowest parasitic inductance and DC resistance among the three designs and also achieved the highest efficiency.

From the loss model derived in Chapter 4 the largest loss contribution of the 4:1 HDSC was due to the DCR of the output inductor. At high output currents, a 25mΩ output resistance contributed to 65% of the total loss. Increasing the efficiency would require using an inductor with a lower DCR or paralleling multiple inductors. Caution must be taken if a lower inductance is used. A lower inductance will increase the output current ripple causing conduction loss due to R_{ac} to be an additional loss and may limit the efficiency improvement as shows in Ch. 4. A model was also developed that provides insight as to how much the flying capacitance can vary from the nominal value before hard-charging loss significantly impacts the efficiency.

For the specific application of a 48-5V DC-DC IBC converter the 8:1 HDSC was designed and tested. The GaN-based HDSC was tested up to 100W with $\eta = 90\%$. While the 8:1 design achieved higher efficiency at a higher power level than the 4:1 HDSC, the output parasitic resistance of the inductor and trace resistance of the PCB in each of the flying capacitor loops were dominant loss mechanisms. Further increase in efficiency would require traces with lower resistance which could be achieved by increasing the copper thickness of the PCB or increasing the trace width in the PCB layout. The output inductor DCR could be reduced by paralleling multiple inductors at the output. In comparison to the designs referenced in the literature review, the HDSC is not able to achieve as high an efficiency as the LLC or STC, with the limiting factor being conduction loss at the output. Moving forward, an analysis of how the timing intervals could be changed to accommodate for a large variance in the nominal flying capacitance would be beneficial. Implementation of a closed-loop design that is able to adjust the split phase timing intervals based on the voltage mismatch between parallel branches would also be valuable.

In conclusion the HDSC topology provides a high-power density solution for the IBC, however the efficiency is limited by parasitics introduced by the PCB layout and conduction loss at the output. A higher efficiency could be achieved with a trade-off in power density.

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