5-2007

Traceable Standard for Sub - 100nm Metrology

Sachin Jayant Deo
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Sachin Jayant Deo entitled "Traceable Standard for Sub - 100nm Metrology." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Materials Science and Engineering.

David C. Joy, Major Professor

We have read this thesis and recommend its acceptance:

Philip D. Rack, Michael L. Simpson

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Michael L Simpson
_____

Accepted for the Council:

Linda Painter
_____

Interim Dean of Graduate Studies

(Original signatures are on file with official student records)

TRACEABLE STANDARDS FOR Sub – 100 nm METROLOGY

A THESIS PRESENTED FOR THE MASTER OF SCIENCE DEGREE
THE UNIVERSITY OF TENNESSEE, KNOXVILLE

SACHIN JAYANT DEO

MAY 2007

This work is dedicated to my family, colleagues and friends

Acknowledgement

The author would like to thank his thesis advisor Dr. David C. Joy for his guidance and support throughout the course of the research work.

The author would like to extend acknowledgement to Semiconductor Research Corporation (SRC), which supports this research work. SRC Task ID: 1281.001, Project Monitor: Dr. Daniel Herr.

Thanks to Dr. Mark Davidson for providing the "Measure" software, and Maggie Connaster for her help during the course of the research work.

The author would like to extend acknowledgement to the colleagues and members of the Electron Beam Facility at the University of Tennessee, Knoxville. Finally, the author would like to extend his gratitude to the University of Tennessee, Knoxville.

Abstract

As we approach the 65nm technological node, transistor gates with dimensions of the order of 40nm are being manufactured. As the device performance is directly related to the dimensions of the gate, critical dimension (CD) control becomes an important part of the fabrication process. Characterization of these small feature size, generally referred to as *Metrology*, is an indispensable ingredient of the semiconductor manufacturing processes. *Metrology* relies not only on the precision, but also the accuracy of commercially used metrology tools like the CD-SEM. To facilitate the magnification calibration of the CD-SEM, an easy access to standard reference artifact traceable to international specifications is an added advantage. Considerable literature is available for CD-SEM, which relies on in-house artifacts or general test objects. The absence of commercially available artifacts hinders evaluation of different CD-SEM. The objective of this abstract is to introduce the fabrication and characterization of artifacts for the sub-100nm metrology, which can be made available in wafer form at low cost.

In this work, artifacts have been designed and fabricated for precise magnification calibration of the CD-SEM. The designing of the artifacts takes into account the *proximity effect*, a problem associated with the e-beam exposure, to produce dense grid type structure in the sub-100nm region. The structures are fabricated using the e-beam lithography tool, operated at 50KeV. The artifacts have been fabricated on a thin layer of negative resist HSQ spun on silicon substrate. Subsequent development in 0.26N TMAH gives a structure on silicon wafer, thereby eliminating contamination issues.

Furthermore, characterization of the artifacts for line pitch determination is carried out using “Measure” (Spectel Corp.), which provides an absolute calibration of the image

pixel size that can then be used to measure other features. The low values for the line edge roughness (LER) further facilitate precise linewidth metrology.

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CHAPTER I

INTRODUCTION

1.1 Introduction

From the birth of the electronic age to the present 21st century, computing power of the microprocessors has evolved rapidly. From the world's first commercial single chip microprocessor - Intel 4004, a 4 bit CPU released by Intel Corp. in 1971, with a computing power of 60000 cycles per second to Intel® Pentium® 4 processor at 2 gigahertz (GHz) – or two billion cycles per second [1], microprocessors computing power has come a long way and is still increasing as we speak. To cater to this need of the consumers to have a better and faster microprocessor, new technologies to sustain this growth have evolved.

Over these three decades, semiconductor industries have moved from micron level to sub-micron level. Circa 2005, we are entering a new frontier of technology, the sub 0.1 micron technology. This has lead to a complicated device fabrication involving small fine features, increased number of masks, variety of light sources and photoresists. Conventional photolithography is still widely used for mass production of microprocessors, but with emphases on the sub 0.1 micron era, new technologies like Extreme Ultra Violet (EUV) lithography, Immersion Lithography, Nanoimprint Lithography to name few, are seriously being considered as an alternative to the conventional photolithography. These new technologies still need to be perfected to use them in mass production, but with time these technologies might be a serious contender for the photolithography technique. To perfect these technologies, companies like Intel,

AMD, IBM are pouring billions of dollars to develop infrastructure supporting these technologies.

1.2 Overview of the lithography process

A brief introduction regarding the lithography process used for semiconductor manufacturing is being discussed (Figure 1.1).

(1) Cleaning of the wafers

Normally done to remove the contaminants from the wafer surface.

(2) Spinning resist on the wafers

Used for applying resist on the wafer surface. The final rpm and the time for spinning play a role in determining the resist thickness.

(3) Baking of the resist on the wafers

The role of baking involves removing the extra solvent present on the wafer surface. It also helps in bond strengthening in the resist.

(4) Exposure of the wafers

Irradiation of the resist surface by either photolithography or electron beam lithography.

(5) Development of the wafers:

After exposure, the wafers are immersed in a development solution to achieve the final pattern shape.

In case of positive resists, the exposed part is removed after development, while the unexposed part remains of the wafers. In case of negative resist, the exposed part remains on the wafer after development, while the unexposed part is removed from the wafer surface.

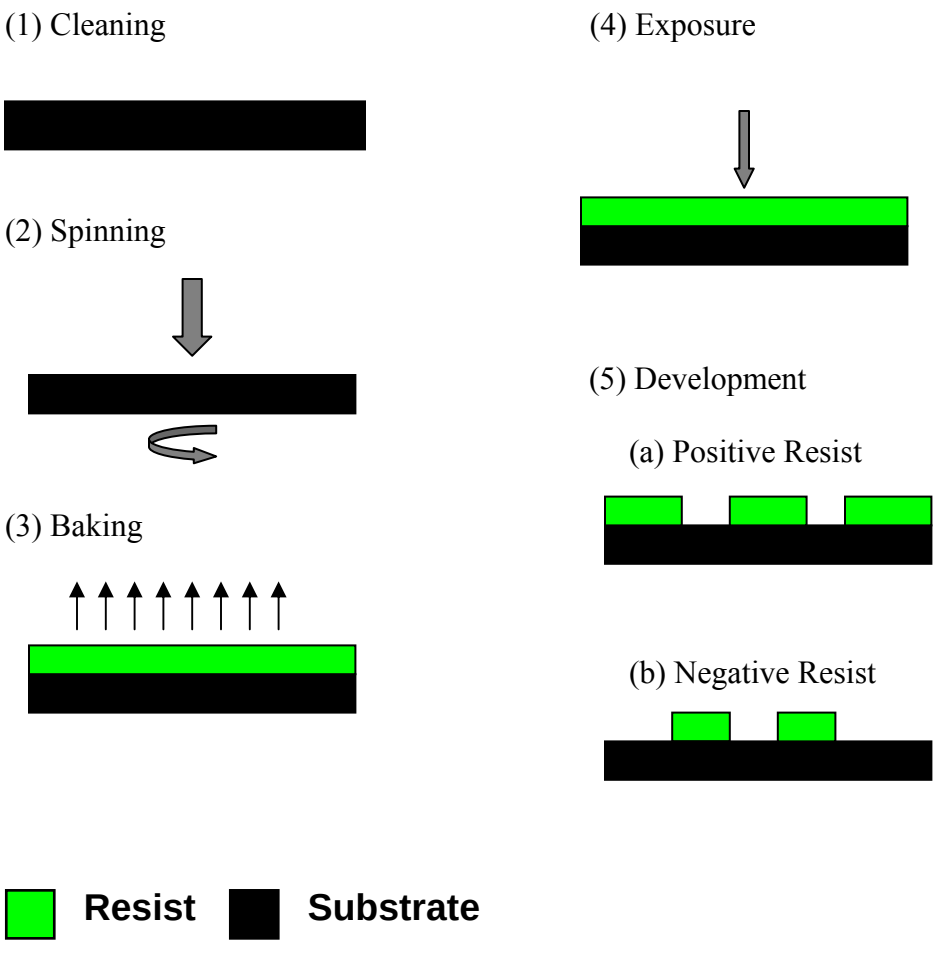


Figure 1.1: Schematic representation of the lithography process.

In 1965 Gordon Moore, one of the two founders of Intel made an observation that innovation in technology will allow the number of transistors on a wafer to double every two years. This observation is popularly known as “Moore’s Law”. Over the last few years, it was believed by many experts from the semiconductor industries that the Moore’s Law will no longer be a benchmark for the industry, but a recent report by Semiconductor International Association (SIA) [2], indicates that the Moore’s Law is to stay for the next decade or so. To ensure that the semiconductor industries go on the path as set by the Moore’s Law, in 1999, the International Technology Roadmap for Semiconductors (ITRS) was setup by leading semiconductor companies of the world. The objective of ITRS is to identify the technological difficulties and need to be faced by the semiconductor industries in the next fifteen years [3].

The International Technology Roadmap for Semiconductors (ITRS) uses the node size to identify the technology era for the semiconductor industries. Presently, we are in the 90nm technology and are expected to reach 65nm technology in year 2007. It is projected that by year 2016, we would be in the 22nm technology [4]. To achieve these goals, semiconductor companies are trying to improve the current technology and in some cases incorporate new technology. The current technology employs photolithography based on the excimer laser. The 193 nm ArF source is predominantly used for the 90nm technology. But as we enter the 65nm technology expected in year 2007, new source of excimer lasers are being studied. Tools using the 157nm ArF_2 excimer laser are currently being developed by some companies and may help in a smooth transition from 90nm technology to the 65nm technology by year 2007.

Moore's Law also states that with the exponential increase in the transistors, there should be decrease in the manufacturing cost for the transistors. To be inline with Moore's Law, semiconductor industries have made transition from the 200mm wafers to 300mm wafers. Intel has started using 300mm wafers in its Oregon and Arizona Fabs, while AMD in partnership with IBM has started using 300mm wafers at East Fishkill, NY facility of IBM. With the roadmap set by the ITRS, the next transition would be to 450mm wafers. Figure 1.2 gives the relation of chip size and area versus time. Photolithography is still the workhorse for the semiconductor industry, even with transition to 300mm wafers. Photolithography is one of the most critical operations involved in making microprocessors. It forms the base for the subsequent processes that would be carried on till the final product is obtained. Photolithography is also called as photomasking, masking and microlithography [5]. Photolithography employs two important goals. First, is to make and transfer the pattern on the silicon wafer, well within the design accuracy. This is also termed as the *resolution* of the patterns on the silicon wafer. Second, to align the different layers of patterns that would be stacked on top of the first layer. This is termed as *alignment* of the patterns on the wafers. Both the *resolution* and *alignment* play a critical role in the photolithography process. Any error in either of the two, will lead to stopping of the entire process and in turn the rejection of the product. With the increasing complexity of the devices, the feature size is becoming smaller as we speak, and the number of layers is also increasing. A lot of research is being carried out to ensure a good *resolution* of the images and a perfect *alignment* of the layers on the silicon wafers [5].

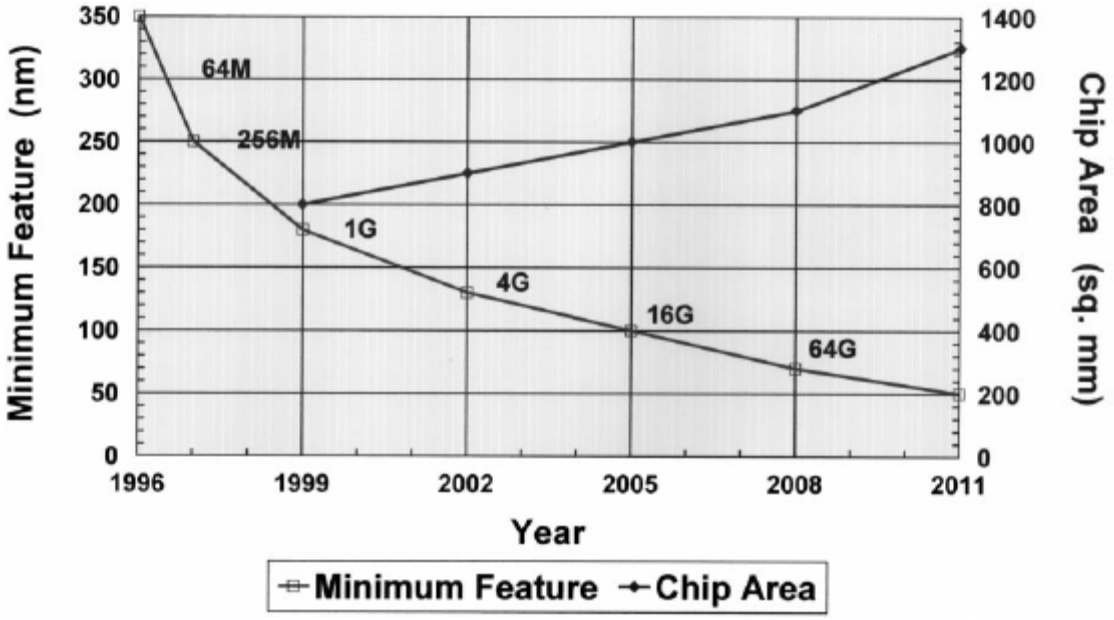


Figure 1.2: Minimum chip size and area versus time [15].

Photolithography is a multi step pattern transfer process. It involves transfer of pattern drawn on the photomask or the reitcle onto the silicon wafer by flashing a light source through the mask. This process is continued till all the layers are stacked in perfect alignment. First step for this process involves spinning light sensitive photoresists on the silicon wafer. This is carried out using industrial spinners which are automated to control the spinning and baking cycles, which in turn ensures correct thickness of the resist layers for all the wafers. Semiconductor companies first used the photoresists produced by Eastman Kodak and Shipley Company in the year 1950. Photoresists are of two types, *positive photoresists* and *negative photoresists*. Depending upon the requirement the photroresists are chosen for the photolithography process. Most photoresists are sensitive to the visible, ultraviolet and deep ultraviolet light source. With the advent of X-Ray Lithography and EUV Lithography, new photoresists, known as *Chemically Amplified Photoresists* are being manufactured. Commonly used photoresists are DNQ and DNQ-Novolac based resist. Each of these resists are sensitive to particular wavelength of light source and can be used only for that particular light source.

After the photoresist is spun on the wafer, light source illuminates the photomask with the pattern on it. Light passes through the transparent parts of the photomask and is deflected back by the opaque parts, thereby, forming the pattern image on the silicon wafers. Photomasks are normally made of quartz or borosilicate glass which have a good dimensional stability and transmission properties for the wavelength of the source. The mask is normally covered with a layer of chrome. Most advanced masks use layers of chrome, chromium oxide in the order the process parameters demand. Photomask or the reticles are generally produced using the Electron Beam Lithography. Electron beam

lithography does not involve any use of masks or reticle, hence it is also called as direct write lithography. The process involves scanning of an electron beam across the silicon wafer. This scanning of the beam can be done in two ways, *vector scan* and *raster scan.* *Vector Scan* involves scanning of the electron beam only in the area which needs to be developed, in other words, area of interest. While *Raster Scan* involves scanning the entire wafer. Due to this , the time required by *raster scan* is more than that by the *vector scan*. Most of the modern lithography machine use *vector scan* technique. With advances in the electron beam lithography machine, theoretical it is possible to get feature sizes as small as 5nm-6nm. In reality it is difficult to get very small feature size due to proximity effect. As quoted by T. H. P. Chang, "Proximity effect is a well known phenomenon that an uniform exposure causes a non uniform distribution of actually received exposure" [6]. Since electron beam lithography is a direct write process, the chances of errors in the pattern design due to any kind of contamination is eliminated. A proper CAD design incorporating the proximity effect correction is fed into the lithography machine. The machine uses the vector scan technique to write the pattern. Electron beam lithography helps in getting very accurate pattern shape, but the disadvantage is the time for writing. Electron beam lithography takes more time compared to photolithography, hence not used for mass production.

After the exposure is completed the mask is developed to obtain the patterns which would be later on transferred onto the silicon wafer. A number of masks are placed in the stepper and are used in the order in which the layer of the patterns on the silicon wafers are required. Each exposure is followed by developing, metal deposition and etching technique before the next exposure can be started.

Semiconductor companies employ processes which require a high degree of precision in imaging the pattern, alignment of the layers, the electrical properties of the wafers, film thickness measurement and few other parameters. Any mistake in either of these parameters can lead to a substantial loss of time and money. New techniques are employed to ensure thorough evaluation of the wafers in a fast, efficient and precise way. Device evaluation and characterization is required for production-line control and product stability. Most of the device evaluation is carried out along with the fabrication process (In line evaluation). Testing processes can be broadly classified as *Indirect Testing* and *Direct Testing* [5]. *Indirect Testing* is normally carried out on test wafers to prevent any damage on actual device wafer [5]. Most of the electrical measurement tests, ion implantation tests are carried on by *Indirect Testing*. *Direct testing* like linewidth measurement, film thickness measurement, and defect detection are carried on the actual device wafer [5].

With ever decreasing feature size, control and evaluation of these feature size is becoming more critical. Evaluation of the feature size is normally called as *Metrology of a linewidth.* This normally involves Critical Dimension(CD) and Overlay(OVL) measurement. Critical Dimension(CD) is normally measured using CD-SEM, CD-AFM and Scatterometry, while Overlay(OVL) is normally measured using bright field optical microscope [7]. Overlay measurement involves measuring the alignment of the various layers built to form the final product. Any error in this alignment of layers causes rejection of the product. This is an inline metrology process carried out during the fabrication process by registering the marks on the wafers and ensuring the position of these marks remain as precise as possible for each layer built in the microprocessor.

With increasing demand for faster, repeatable and accurate linewidth measurements, new techniques like scatterometry are being employed by the semiconductor industries to cut down the processing time and get accurate measurement as possible. Scatterometry is the analysis of light scattered or diffracted from the sample. In this technique, a scatter signature is obtained by varying the angle between the light source and the sample to be measured, and monitoring the power diffracted into the zeroth order. This signature contains the dimensional information about the scattering [8]. These reading are later on compared with an in built library and thus an accurate linewidth measurement can be done. Scatterometry evaluates a group of lines as compared with CD-SEM , which evaluates single line at one time.

Inspite of the new techniques for the metrology of linewidth, CD-SEM is still the most preferred by the semiconductor industries. CD-SEM is like any conventional SEM, modified with some special data processing capabilities for Critical Dimension Measurement. Charging and damage induced by the beam encountered in conventional SEM plays an important role in deciding key parameters like beam current, beam energy, beam size and scan speed. An optimum condition is required to ensure as minimum charging and damage due to beam as possible on the wafer [9]. As the number of the transistors on the wafers increases, the resolution offered by the CD-SEM becomes one of the most important criteria considered while buying a new CD-SEM. KLA-TENCOR, Hitachi High Technologies are some of the companies which are manufacturing the CD-SEM. The S-9380II CD-SEM manufactured by Hitachi High Technologies, Schaumburg, IL can handle 300mm wafers with a resolution of 2nm, precision of 0.8nm and throughput of 33 wafers per second [10].

1.3 Scope of the Project

As discussed earlier, CD-SEM is still considered as the benchmark for Critical Dimension Metrology. Efforts are being made to improve the resolution and the efficiency of CD-SEM. All the CD-SEM's are calibrated before they can be used for Critical Dimension Metrology. This calibration is done by using the standards provided by the CD-SEM manufacturer. Companies like Hitachi, KLA-TENCOR provide their own standards to their consumers. Thereby restricting the use of the standards to their consumers only. Though there are companies like VLSI Standards and government organization like NIST working on developing metrology standards which can be used by anyone interested in doing metrology.

To facilitate the measurement of the CD-SEM performance, an easy access to standard reference artifact traceable to international specifications is an added advantage. Considerable literature is available for CD-SEM performance, which relies on in-house artifacts or general test objects. The absence of commercially available artifacts hinders performance evaluation of different CD-SEM. The objective of this abstract is to introduce the fabrication and characterization of artifacts for the sub-100nm metrology, which can be made available in wafer form at low cost.

In this research work, artifacts have been designed and fabricated for precise magnification calibration of the CD-SEM. The designing of the artifacts takes into account the *proximity effect*, a problem associated with the e-beam exposure, to produce dense grid type structure in the sub-100nm region. The structures are fabricated using the e-beam lithography tool, operated at 50KeV. The artifacts have been fabricated on a thin layer of negative resist HSQ spun on silicon substrate. Subsequent development in 0.26N

TMAH gives a structure on silicon wafer, thereby eliminating contamination issues. The artifacts have 100nm pitch, with linewidth of the order of 40nm.

Furthermore, characterization of the artifacts for line pitch determination is carried out using standard software such as “Measure”, Spectel Research Corp. which provides an absolute calibration of the image pixel size that can then be used to measure other features. Line pitch determination carried out by the threshold method and the regression to baseline method gives out values close to 100nm, in accordance to designed values. The low values for the line edge roughness (LER) further facilitate precise linewidth metrology. Line pitch determination using optical metrology tools and the inbuilt laser interferometer in the electron beam lithography tool is being evaluated for precise measurements.

CHAPTER 2

LITERATURE REVIEW

2.1 Semiconductor Substrates

With the transition from 90nm technology to 65nm technology, the number of transistors on the silicon wafers is increasing. To accommodate this increase in the transistors, and also maintain the Moore's Law, the size of the silicon wafer has been increased. Currently the semiconductor industries are using the 300mm wafer. The next transition is expected to be at 450mm wafers, according to SIA Technology Roadmap. Though the size of the wafers has increased, the production methods have remained pretty much the same. This has lead to number of problems associated with weight of the cast, structural issues and electrical properties of the wafers.

Some of the manufacturing techniques for silicon wafer are Czochralski growth, float zone growth and Bridgman Growth. The latter is used more often for GaAs wafer production.

2.1.1 Czochralski Growth

Czochralski growth technique is the most used manufacturing method for silicon wafers. It was developed by Jan Czochralski in 1916 while studying the crystallization rate for some metals. It involves drawing of thin metal rod from a melt of pure single crystal silicon, the process would be further explained in the following paragraph. The first wafers produced were 100mm in diameter, while the present day wafers have 300mm diameter. The wafers thus produced have around 600-700μm thickness with a purity level of almost 99.99999999 % [11]. The biggest producers of silicon wafers are MEMC, SEH, SUMCO, Wacker Siltronic and Komatsu.

Czochralski growth involves solidification of a crystal from the melt. In this technique a ultra high purity grade polycrystalline silicon (purity= 99.99999999%), is placed in a fused silica crucible. To eliminate any impurities during melting, the crucible is encased in an evacuated chamber with an inert gas flowing. A small single crystal silicon is introduced in the melt of polycrystalline silicon. The orientation of this crystal is very important, since it decides the orientation for the entire silicon melt [11]. This small crystal just touches the surface of the melt and is pulled up and simultaneously rotated by hydraulic shafts. The pressure and the composition of the melt and the single crystal are almost same, hence there is reduction in the temperature as the surface area increases. The larger crystal thus obtained by this technique is known as *Boule* [11]. Modern boules have a diameter of the order of 300mm. In this technique the pulling rate is very important, any increase or decrease in this pulling rate can cause severe problems in manufacturing of silicon wafers. The steps involved in czochralski growth for silicon substrates are shown in figure 2.1.

The diameter of the silicon wafer determines the process parameters required to maintain the quality of the silicon wafers. As the diameter of the crystal increases, the pulling rate is decreased to ensure a uniform cooling of the boule. During the cooling the crystal orientation of the seed propagates in the melt. Also, the dopant atoms get incorporated to form the N-type of the P-type silicon wafers [5]. Moreover, a very low pulling rate may cause introduction of point defects in the crystal. *Dislocation loops*, the most common defects found in the crystal, are formed by improper pulling rate of the melt.

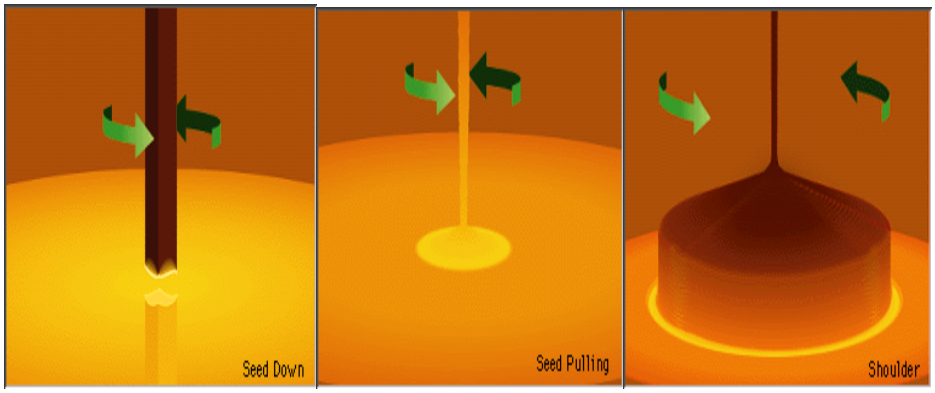


Figure 2.1: Czochralski growth for silicon wafers [13].

2.1.2 Wafer Preparation and Specifications

After the production of the boule is completed, the final step involves the preparation of the wafer. Grinding, slicing, etching, lapping, polishing and cleaning are some of the steps enroute to final wafer suitable for fabrication purposes. The boule is checked for electrical resistivity and crystal perfection, followed by grinding to the required diameter of the wafer. Every silicon wafer has a particular orientation which is indicated by providing a flat to the circular silicon wafer. The largest flat is known as *primary*, and oriented perpendicular to <110> direction. One or more minor flats may be given in some cases, while in large wafers with diameter more than 200mm, a notch is ground into the edge [11]. Figure 2.2 shows the different type of orientations for a silicon substrate. Table 2.1 gives the specification of silicon wafers.

Grinding to get a flat in the silicon wafer produces lot of residues, which are removed by etching the boule in a proprietary mixture. This is followed by slicing of the boule to obtain individual silicon wafers. Extreme care has to be enforced to prevent any breakage in the silicon wafers or damage to the boule. Slicing induces roughness in the edges of the silicon wafers, which is later on removed by lapping both sides of the wafers in alumina and glycerine slurry. Lapping reduces the stresses on the wafer edges, and also prevents pile up of liquid that is spun on the silicon wafer. Final polishing is achieved using Chemical Mechanical Polishing (CMP), which ensures a smooth mirror like finish on either one side or both sides of the wafers as per the requirement. Oxygen concentration, carbon concentration, wafer orientation, metal contaminants and resistivity are some of the specifications used to describe the quality and type of the wafer.

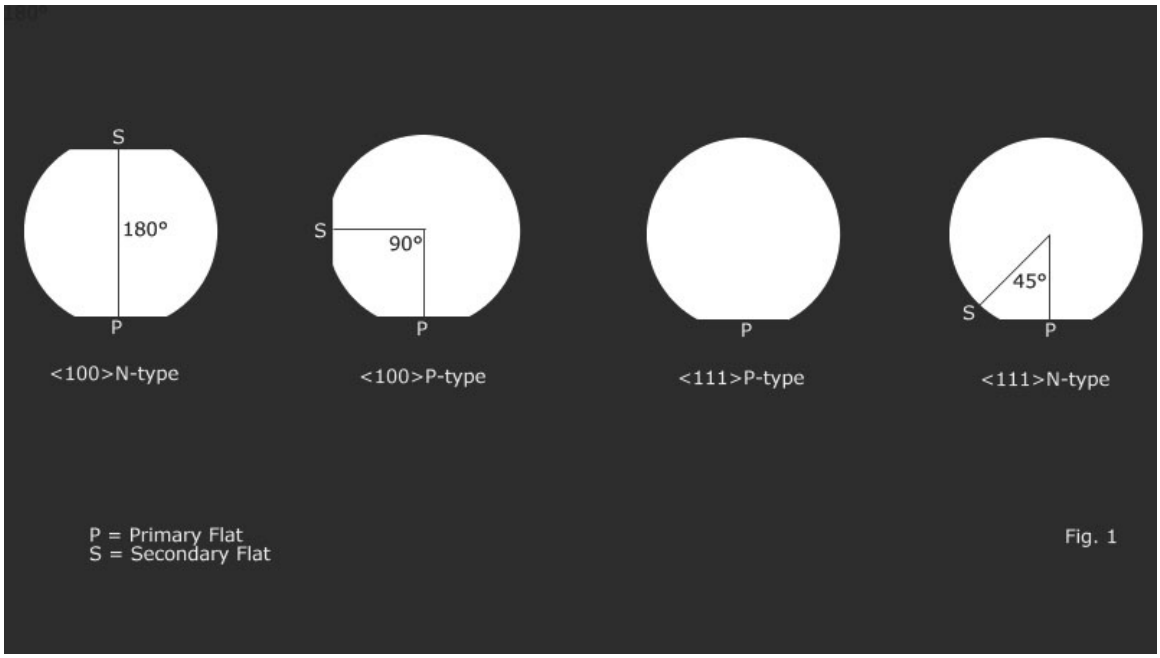


Figure 2.2: Wafer orientation indicated with primary and secondary flats [14].

Table 2.1: Specification of 2” silicon wafer.

Diameter:	50.8 mm	Resitivity:	1-20 Ohm-cm
Type:	N/Phos	Thickness:	250-300μm
Orientation:	(100)	Grade:	Test
Flats:	2<110>	Surface:	One side polished

Courtesy: Wafer World Inc

Some of the specification for a test grade silicon wafer.

Variation in the resistivity can be achieved by changing the amount of dopant atoms in the silicon melt. To decide the amount of dopant required, the weight of the melt is calculated, followed by determining the amount of impurity atom required and adding the weight of the impurity as needed. A rough calculation of the dopant weight is done by using the segregation coefficient k , defined as

$$k = \frac{C_s}{C_l}$$

where C_s and C_l are the impurity concentrations at the solids and liquid sides of the solid/liquid interface [11]. Some of the specification for a test grade silicon wafer.

2.2 High Resolution Lithography System

The key technology that drives the semiconductor industries are the high resolution lithography systems used to fabricate fine feature size. With the semiconductor industries preparing themselves for the 65nm technology, efforts are being made to improve and increase the throughput of these systems. A brief introduction to Optical Lithography, Next Generation Lithography (NGL) and the Electron Beam Lithography is provided in an effort to emphasize the importance of these systems.

2.2.1 Optical Lithography

Optical lithography, right from its inception till the present day, has been the workhorse for the semiconductor industries. Since this technique uses a light source, it is also called as *photolithography*. In this technique, light passes through a mask with the design features onto a photoresist coated silicon wafer, thereby transferring the design features from the mask to the photoresist. The masks used in photolithography are generally chrome on quartz or borosilicate glass. They are manufactured using the electron beam lithography to ensure a precise dimension control. Extreme care has to be taken to avoid any defects or pinholes on the masks, since these masks are used to pattern thousands of wafers. The design of the feature on the mask is done taking into account optical proximity correction. A typical wafer fabrication will need 10-15 masks to form the final microprocessor. The improvements in the wavelength of light and the numerical aperture (NA) of the projection lens have helped in the growth of the optical lithography system. These two factors are represented as,

$$\text{Resolution, } R \approx \frac{Wavelength(\lambda)}{2NA}$$

The present day photolithography use Deep Ultra Violet (DUV) source of the order of 193nm excimer lasers and 157nm excimer lasers. With the 157nm excimer lasers, the major cause of concern is the availability of material transparent to 157nm lasers [15]. Schematic of a simple optical lithography system and the potential of introduction of new tools are shown in figure 2.3 and figure 2.4 respectively.

Thus to ensure advancement in technology, problems associated with the new technology need to be solved before the technology can be used for mass production.

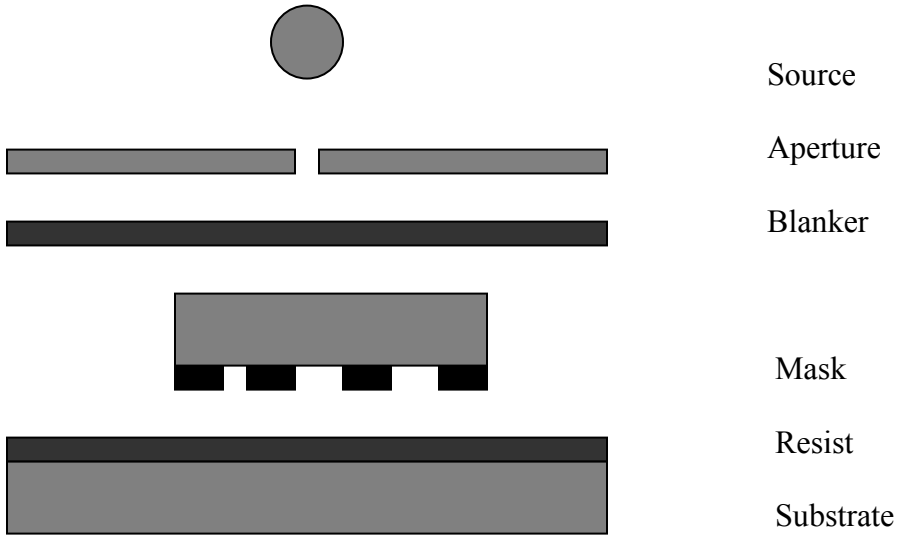


Figure 2.3: Schematic of a simple optical lithography system

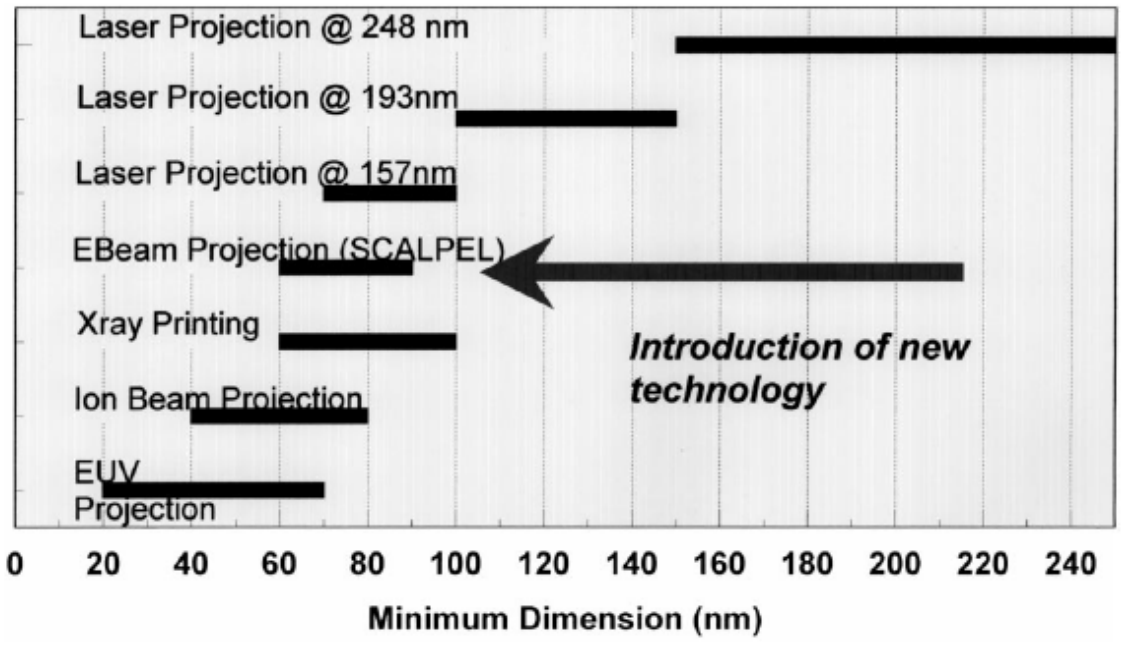


Figure 2.4: Potential introduction of new resolution lithography tools [15].

2.2.2 Next Generation Lithography (NGL)

With the Moore's Law still governing the future of the microprocessors, International SEMATECH through its Next Generation Lithography Task Force, has charted a roadmap till 2011 [15]. This will need the implementation of next generation lithography system like X-Ray Lithography, Extreme UV Lithography and Ion Beam Projection.

2.2.2.1 X-Ray Lithography

The concept of X-Ray Lithography was introduced in the early 1980s, and has been undergoing development since then. The major problems associated with this technique are the use of the mask and the x-ray source. Though the problem of the X-Ray source might be resolved with the introduction of X-Ray synchrotron source [16], there still remains the issue of manufacturing mask for this technique. The mask is thin membrane of patterned gold layer of the order of 500 nm, and is transparent to wavelength of 1 nm. The biggest limitation of this technique is the manufacturing of masks, which have the design dimensions same as the final pattern [15]. If this problem can be solved, X-Ray Lithography can be considered for mass production. Figure 2.5 and Figure 2.6 gives a schematic view of X-Ray Lithography.

2.2.2.2 Ion Beam Projection

A stencil mask of few micrometers in thickness and 100 keV hydrogen or helium ion source constitutes the ion beam projection system.

2.2.2.3 Extreme UV Lithography

EUV Lithography is still in its early stage of development, with various companies in USA and Europe. It uses 13 nm wavelength photons emitted from the high powered Nd:YAG laser [15].

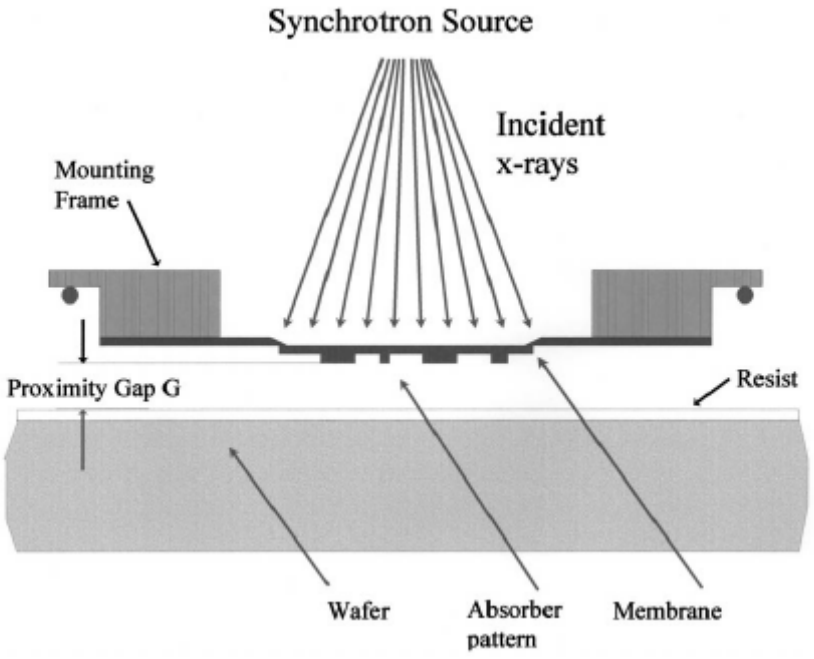


Figure 2.5: Schematic view of X-Ray Lithography [15]

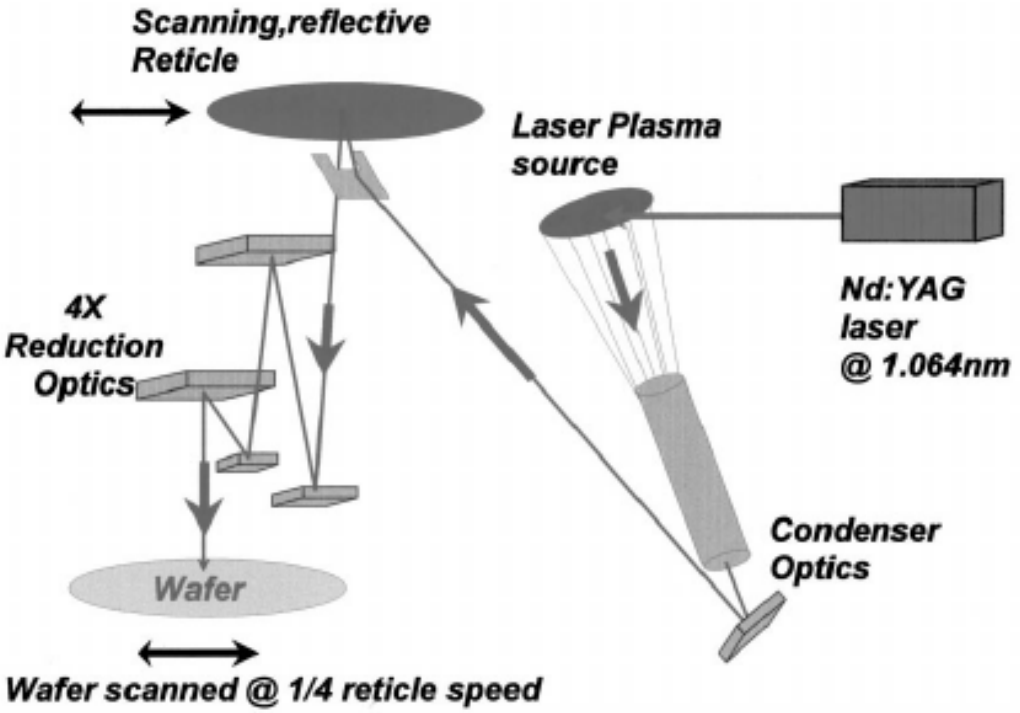


Figure 2.6: Schematic of experimental X-Ray Lithography [15].

2.2.3 Electron Beam Lithography

Electron beam lithography has come a long way from the first EBL systems like the Bell Labs EBES [11]. The new state of the art lithography systems are expensive, costing more than $ 2M per unit, and with a good resolution of the order of 5nm. Electron beam lithography is also called as direct write lithography, since it involves no mask for fabrication purpose. Inspite of the advantages offered by electron beam lithography, the use of this technique for mass production has been hampered by the slow throughput. Electron beam lithography is mainly used for fabrication of masks, which are later on used for photolithography.

2.2.3.1 Principle of Electron Beam Lithography

Most of the lithography system involves moving the electron beam across a wafer to expose the pattern on a pixel basis. The basic principle involves heating of the electrode gun, which produces an electron beam. The final size of the beam (around 5nm) is controlled by the electrostatic lens and a variety of apertures. There are three main types of electrode gun commonly used: *Thermionic emitter* and *field emission emitter.* *Thermionic emitter* is a tungsten (W) filament of about 100μm diameter, bent in a V-shape hairpin. Resistive heating of this tungsten filament gives thermionic emission. The lifetime of these emitters is around 30 to 100 hours for temperature of 2700 K , vacuum of order of 10^{-3} Pa and brightness of $\beta=10^{5}$ A/cm ^{2}sr. In thermionic emitters, the brightness typically increases with accelerating voltage. Energy spread, brightness, source size and lifetime are some of the factors which affect the performance of the thermionic emitters [17]. *Field emission emitters* are usually made from single-crystal tungsten in a form of a wire of a radius of about 100nm. Electrons are generated from

these emitters by field emission, thereby eliminating thermal drifts, evaporation of cathode material and low brightness. There is another set of field emission emitters, the *Schottky Emitters,* made from ZrO/W annealed in forming gas. These emitters have excellent emission stability, but larger demagnification is required, hence reducing current available [17].

The electron beam thus produced by the gun is further demagnified to the required size by using electrostatic lens and a variety of apertures. The final spot diameter on the silicon wafer is given by

$$d^2 = d_o^2 + d_s^2 + d_c^2$$

where d_o is the perfect lens diameter, d_s is the spherical aberration and d_c is chromatic aberration. The final electron beam has a Gaussian shape, with intensity increasing with radius from the center.

In direct write lithography, scanning is achieved either by *raster scan* or by *vector scan* (figure 2.7). *Raster scan* was used in the first EBL systems including those manufactured by Bell Labs. In this type of scanning, the beam is deflected from one point to another in one direction, thereby scanning the entire wafer. The time required by raster scanning is quite high, thereby decreasing the throughput of the machine. While *vector scan* EBL systems have high throughput on account of the electron beam scanning only the area of interest. In such EBL systems, the co-ordinates of the area of interest is fed to the X and Y digital and analog converters (DACs), which directs the beam to the exact location. This ensures that the time required for writing patterns on wafers is less compared to the raster scanned EBL systems.

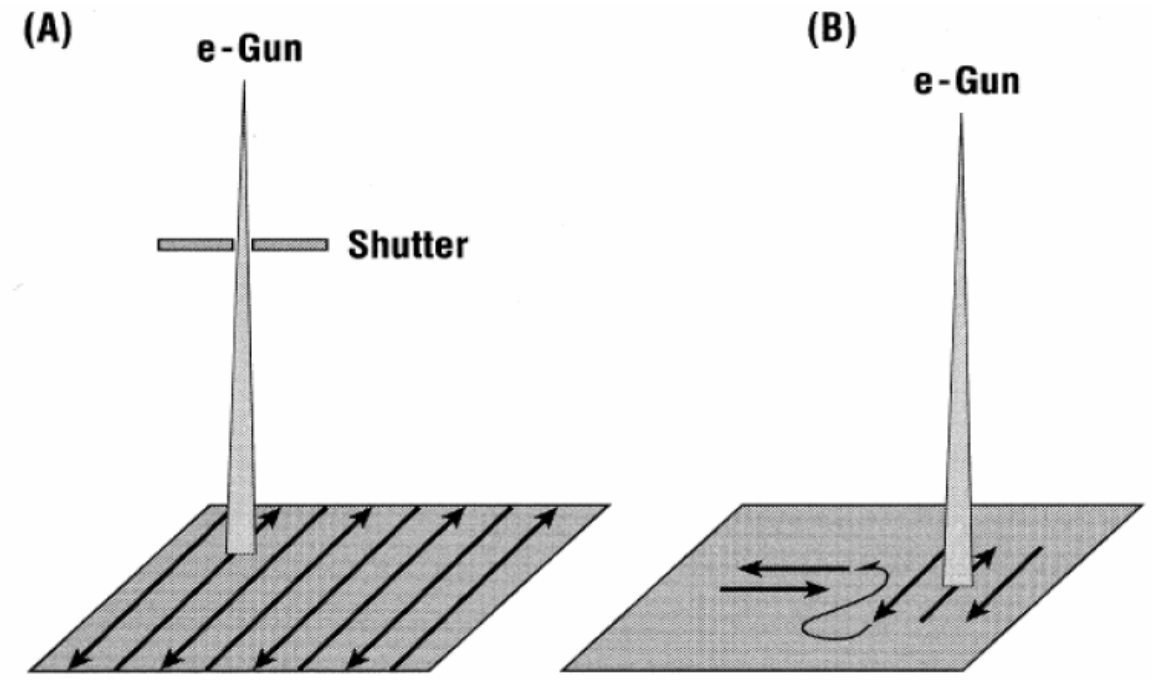


Figure 2.7: Comparing of scanning methodologies (A) Raster Scan (B) Vector Scan

2.2.3.2 JBX 6000 FS/E – Direct Write Lithography

(Courtesy: JEOL JBX 6000 FS/E, JEOL, Peabody, MA)

The JBX 6000 FS/E is an electron beam lithography system designed for production of GaAs FETs as well as process development and prototype engineering for optical elements and silicon devices. It is best suited for research work involving very high precision pattern fabrication.

The system employs a high-brightness electron gun using a zirconium oxide coated tungsten thermal field emitter (ZrO/W TFE) and an in-lens detector. The system is capable of high speed pattern exposure on high resolution resists. The JBX 6000 FS/E (figure 2.8) uses a single-stage in-lens electrostatic deflector free from hysteresis, assuring high stability. It incorporates two different objective lenses as standard for fine and ultra fine pattern with a beam diameter range of 5nm to 200nm. The operation mode is roughly divided into 4^{th} lens-mode and 5^{th} lens-mode each having distinct features.

The 4^{th} lens-mode is used for submicron electron beam lithography to write fine geometries on wafers. In addition to the primary application of direct submicron writing on the wafers, this mode is provided with the pattern writing functions for masks applied to small volume production.

The 5^{th} lens-mode is used for ultra fine electron beam lithography to write ultra-fine geometries on wafers. It has been developed for conducting basic researches on very large scale integrated circuits or new physical phenomenon. In the 5^{th} lens-mode, the beam diameter is around 5 nm, while for the 4^{th} lens-mode the beam diameter is in the order of tens of nanometers (Figure 2.9 and Figure 2.10). The JBX 6000 FS/E is a vector scanning type electron beam lithography system which facilitates faster writing time.

Figure 2.8: Electron Beam Lithography tool - JBX 6000 FS/E (JEOL)

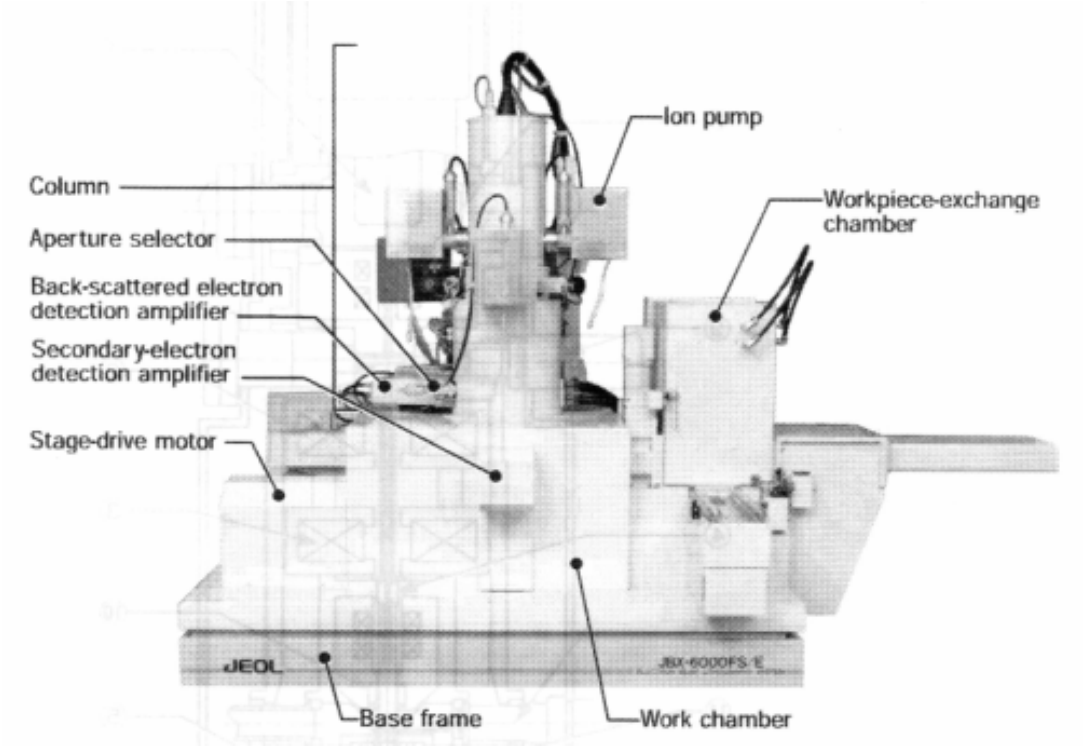


Figure 2.9: Main Console for JBX 6000 FS/E (Courtesy: JEOL- Peabody, MA)

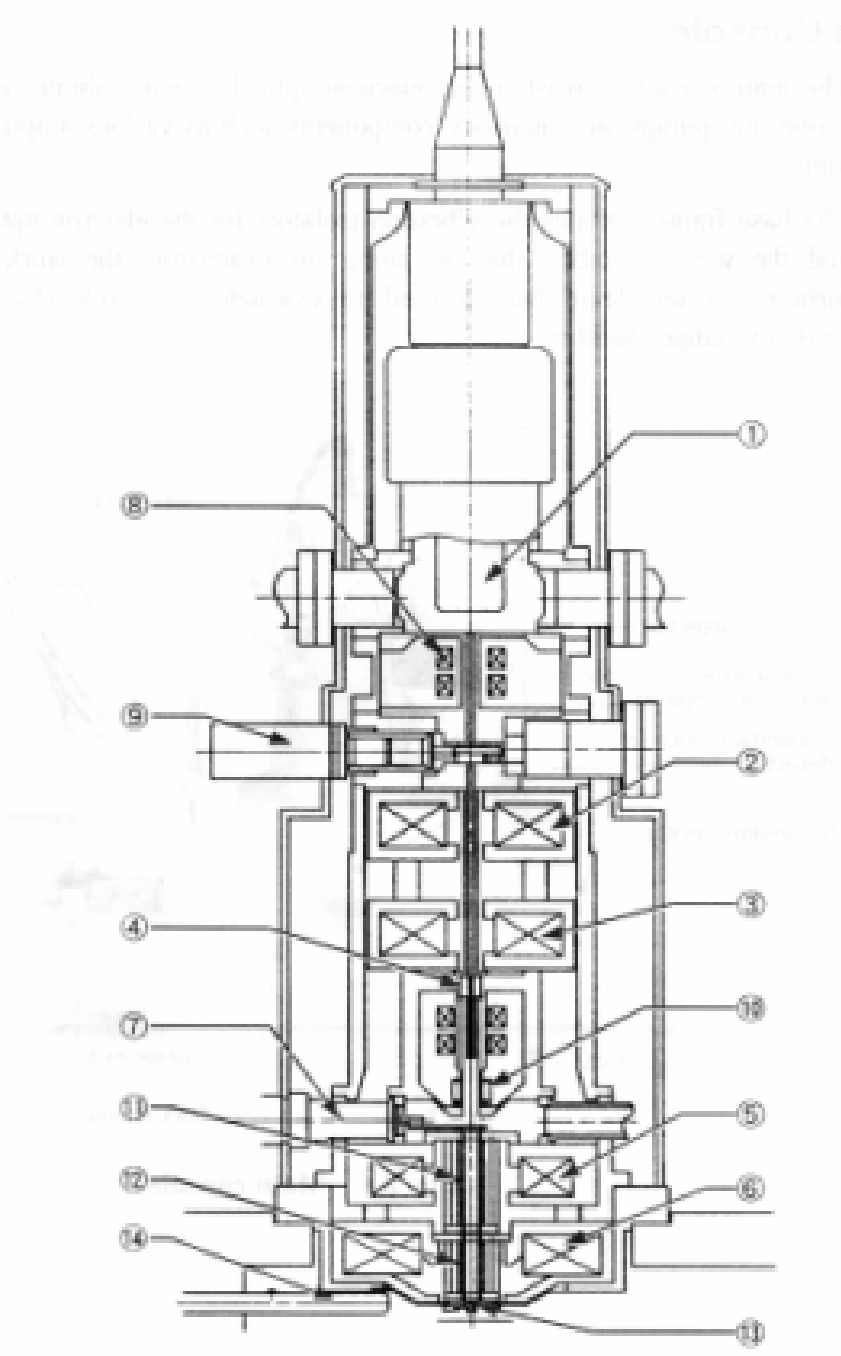


Figure 2.10: Gun Column for JBX 6000 FS/E (Courtesy JEOL – Peabody, MA)

(1) Electron Gun

(2) 2nd Lens (2nd demagnification lens)

(3) 3rd Lens (3rd demagnification lens)

(4) Blanking Electrode

(5) 4th Lens (Projector Lens)

(6) 5th Lens (Projector Lens)

(7) Aperture Selector

(8) 1st Beam Alignment Coil

(9) Astigmatism Correction Coil

(10) 1st Deflector

(11) 2nd Deflector

(12) Backscattered Electron Detector

(13) Secondary Electron Detector

The acceleration voltage provided to the system can be manually changed from 25 kV to 50 kV or vice versa. The workpiece stage movement is controlled by Laser Beam Control (LBC) to ensure high accuracies in the movement of the stage. The stage position is controlled in units of 0.62 nm, with a resolution of $\lambda/1024$.

To help in accurate writing conditions, the entire scanning method is based on scanning ranges which define the *field* and the *sub field*. The pattern to be written by the electron beam lithography system is divided into regions called *field*. To further ensure the accuracy in writing, decrease distortion in writing the field size is divided into small area called the *sub-field*.

Depending upon the type of the acceleration voltage used and the type of objective lens used, the field size varies. The following Table 2.2 gives an idea of the field and the sub-field size.

If the dimensions of the design are in the range of few hundreds of microns, it is advisable to use the combination of 4^{th} objective lens and 50 kV accelerating voltage. With this combination the time required for writing a pattern decreases drastically. Moreover, the field size has to be taken into account while designing the pattern, else stitching becomes an issue during fabrication.

In the quest of higher precision and accuracy in the dimensions of the pattern, it is advisable to go for a combination of 5^{th} objective lens, 50 kV accelerating voltage with 100pA current.

Table 2.2: Field and sub-field for an electron beam lithography system

(*Courtesy: JEOL, Peabody, MA*)

Sr. No.	**Accelerating Voltage (kV)**	**Objective Lens**	**Field Size (X and Y dir.) (µm)**	**Sub-Field Size (X and Y dir.) (µm)**
1	25	4	1600 X 1600	100 X100
2	25	4	800 X 800	50 X 50
3	50	5	160 X 160	10 X 10
4	50	5	80 X 80	5 X 5

2.3 Electron-Solid Interaction

When a beam of electrons is impinged onto a substrate, there is an interaction between the electrons and the atoms of the substrate. This electron-substrate interaction can be broadly classified as *Elastic Scattering* and *Inelastic Scattering.*

Elastic Scattering changes the path of the electrons within the specimen without affecting the kinetic energy of the electrons. This scattering event causes electron backscattering from the substrate and is the major imaging signal for scanning electron microscope. The amount of the backscattered electrons can be quantified by the backscattering coefficient η, defined as

$$\eta = \frac{n_{BSE}}{n_B} = \frac{i_{BSE}}{i_B}$$

Where, n_B is the number of electrons incident on the specimen and n_{BSE} is the number of backscattered electrons (BSE). The backscattering coefficient can also be expressed in terms of current [17]. The backscattering coefficient generally increases with the atomic number, thus forming the basis for *atomic number contrast*. Individual backscattering electrons involves angles less than 90°, but the cumulative effects of all the electrons together helps the BSE to escape the sample surface.

The backscattered electrons are the major cause of the proximity effect observed during the lithography. As a result of the proximity effect, the pattern design suffers from a high degree of deformation. This effect is dependant on beam voltage, resist material, substrate material, contrast characteristics and the development process used. Thus proximity correction is an important part of the lithography process.

Inelastic Scattering events involve transfer of energy from beam electrons to the atoms of the substrate. This scattering events lead to the generation of secondary electrons, auger electrons, x-rays, phonons and plasmons. Secondary electrons produced by inelastic scattering have energy less than 50 ev, and form an important imaging signal. The secondary electrons are quantified by secondary electron coefficient δ, defined as

$$\delta = \frac{n_{SE}}{n_B}$$

Where, n_B is the number of electrons incident on the specimen and n_{SE} is the number of secondary electrons (SE). Elastic scattering deviates the electrons from their original directions of travel, while the inelastic scattering progressively reduces the energy of the electrons as they travel through the substrate. This causes the formation of a region wherein the electrons interact and deposit their energy leading to the emission of secondary electrons, known as *interaction volume*.

The emission of the secondary electrons (SE) and the backscattered electrons (BSE) is schematically described in Figure 2.11 and Figure 2.12

During the electron beam lithography operation, the electrons penetrate through the resist, undergoing small angle scattering (forward scattering) and large angle scattering (backscattering) which greatly affects the feature design. *Forward scattering* causes broadening of the beam diameter at the base of the resist. This broadening effect can be minimized by using a very thin layer of the resist and highest possible accelerating voltage [18]. The broadening in the beam diameter can be empirically given as

$$d_f = 0.9(R_t / V_b)^{1.5}$$

where, R_t is the resist thickness and V_b is the beam voltage in KeV [18].

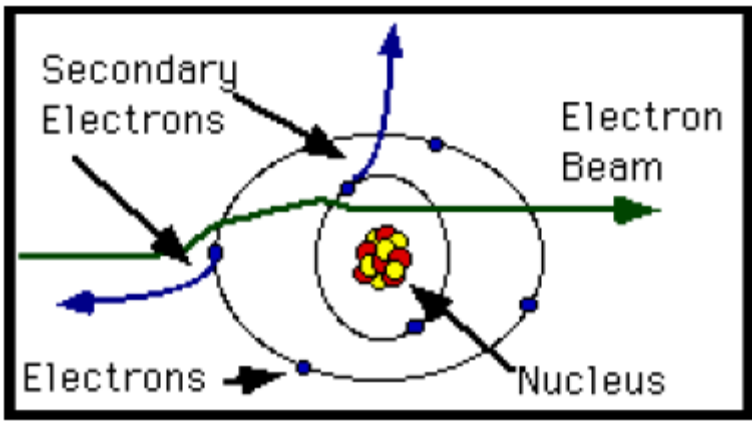


Fig 2.11 Secondary electron scattering

(Adapted from http://maic.mse.ufl.edu/Lecture-5.pdf)

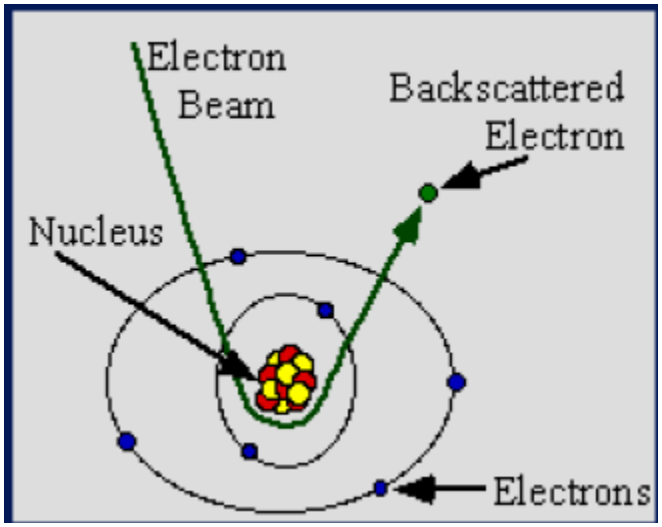


Fig 2.12 Backscattered electrons scattering

(Adapted from http://maic.mse.ufl.edu/Lecture-5.pdf)

Forward scattering can be useful in getting a good undercut of the sidewall in a pattern, by ensuring an optimum development time of the resist [18]. As discussed earlier, backscattering causes the proximity effect in the resist, thereby distorting the design feature.

These electron scattering can be modeled accurately by using some simulation modeling software. The most common technique is the Monte Carlo simulation which is used by many commercial available software. The input parameters for this program are electron energy, beam diameter and film thickness, while the output is a plot of energy deposited in the resist as the function of distance. This distance is calculated from the center of the beam. The following figure gives a Monte Carlo model for electron scattering using 50 KeV accelerating voltage and PMMA resist thickness of the order of 50 nm. The software used for the simulation is CASINO v2.42, developed by Alexandre Real Couture and others. The program uses Joy and Luo (1989) physical model for the Monte Carlo simulation (figure 2.13).

2.4 Proximity Effect in Electron Beam Lithography

The resolution of the electron beam is good on account of small wavelength, hence small diffraction. This resolution is limited by the optical aberration and the electron scattering events in the resist and substrate, mostly referred to as the proximity effect.

Extensive research has been done on the causes and correction of the proximity effect. There are number of research papers on this topic, and new ways are being developed to overcome the proximity effect. As quoted by T.H.P Chang , “proximity effect is a well known phenomenon that a uniform exposure by the incident beam can give rise to a non

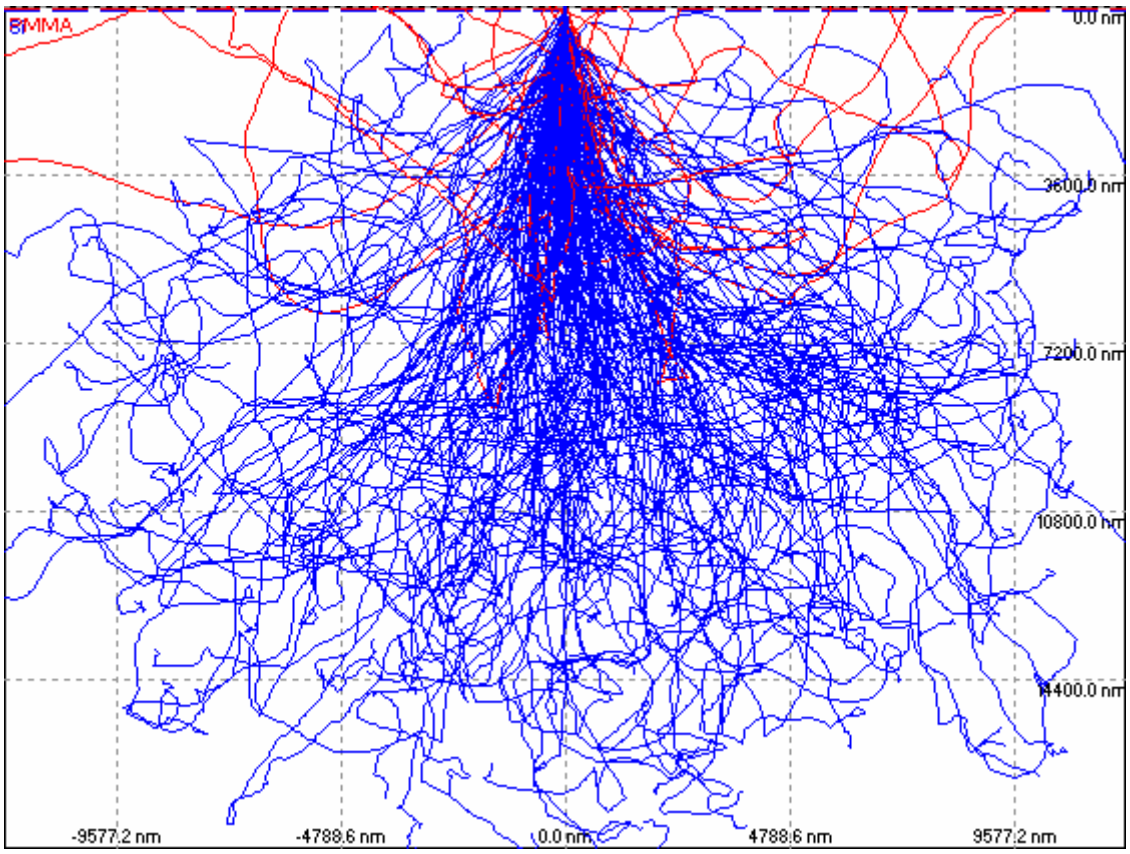


Figure 2.13: Monte Carlo simulation for 50 KeV electron beam

uniform distribution of actually received exposure in the pattern area." [19]. The backscattering electrons are the major cause for the proximity effect and depend on beam accelerating voltage, resist thickness, resist contrast and material, substrate and the development technique used.

Large feature size requires less development time compared to the small features, hence any attempt to develop the small features on the same wafer with large features leads to overdevelopment of the large features. This effect is defined as the *Intrashape proximity effect*. The most serious distortion of the patterns is shown by the *Intershape proximity effect*, wherein increasing packing density of features leads to overexposure of the feature size. This causes decrease in the spacing between the features and increase in the size of the feature size [20]. The degree of distortion due to proximity effect is different for the positive and the negative resists. As the feature size goes on decreasing with every technology node, the proximity effect is becoming more serious. In the sub 100 nm region, the proximity effect is extremely severe and is a major obstacle for transition to 45 nm node and the subsequent 32 nm node.

The type and the thickness of the resist used also govern the mathematical calculation used for proximity effect correction. Thicker the resist more would be the forward scattering, thereby increasing the final beam diameter. Since backscattered electrons travel through the substrate, the type of substrate used plays an important role in proximity effect. The severity in proximity effect increases with decrease in the linewidth and the gap width. The denser the patterns are on the substrate, the distortion in the linewidth increases rapidly. Over the years, it has been suggested that the scattering events are affected by the initial electron energy, but recent research carried out by Erik

H. Anderson et al [21], suggests that initial electron source does not govern the scattering and resist exposure mechanism. They have used 50 kV and 100 kV electron source on the same wafer coated with a thin layer of HSQ resist. The proximity effect can be corrected by incorporating a unique mathematical solution, for a particular function and pattern. This mathematical solution takes into account the factors leading to the proximity effect in the pattern and provides solution for the problem. Traditionally, proximity effect correction has been carried out using three basic techniques. These are *dose modulation, shape modification* and *background correction exposure*. Different program and software are used for the proximity correction. Commercial program like PROXECCO, as a component of CATS are used for dose modulation calculation. Shape and dose modulation are also carried out using the PYRAMID approach as suggested by S.Y. Lee [22]. The unique function of the PYRAMID approach is the use of the DSP model for finding the energy each pixel in the pattern. This cuts down the time required to find the amount of correction required for each pixel to take care of the proximity effect. The use of the DSP model also gives an accurate estimation of the correction required.

The PYRAMID approach for the proximity correction is different than other commercially available softwares like PROXECCO. In absence of any dose modulation software, proximity correction can be done using the shape modulation. This involves changing the design of the artifact to accommodate the increase in the dimension of the artifact on account of proximity effect. Proximity effect is seen more on sharp edges or corners due to high dose concentration. On account of this high dose concentration, the edges or the corners tend to round off. To avoid this problem, shape modulation is used for dimensional control of the design.

2.5 Resist Technology

The lithography tools have come a long way from its development period to be the forte of the current and the future technology nodes. The popularity of these lithography tools can be attributed not only to changes in the optics, the light sources, materials technology but also to the resist technology. Drastic changes in the resist technology enabled the lithography tools to define sub-micrometer structures with high precision. *Resists* are polymeric material dissolved in liquid solvent with varying molecular weights and compositions. Normally a thin layer of the resist is used for pattern definition. In places where overlaying of the patterns is required, multiple resist thicknesses are used. To achieve the multiple layers of the resists, the process flow is repeated as many times required. The resists are generally spun on the substrate, followed by baking the resist to get the required thickness and also to strengthen the bonds of the polymeric material. After radiation from the lithography tools, the resist undergoes a chemical reaction to facilitate the formation. The transfer of pattern design on the silicon wafer or other substrates is carried out after development, followed by etching. The selection of a resist and development of the resist process is a detailed research in itself. Once a resist process flow has been developed, it is rarely changed, unless a change ensures a substantial difference in the output of resist process. The International Technology Roadmap for Semiconductors (ITRS) has predicted the development of the resist technology over the next few years. The resist requirement as given by ITRS is in Table 2.3

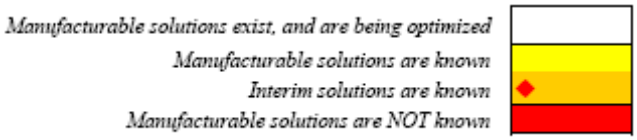
Depending on the type of radiation used to cause the chemical reaction, resists are classifieds as *Photoresists* or *Electron beam resists.*

Table 2.3: Resist requirements for near-term years [3].

(Adapted from http://public.itrs.net)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Flash ½ pitch (nm) (un-contacted poly)	*76*	*64*	*57*	*51*	*45*	*40*	*36*	*32*	*28*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU physical gate length (nm) [after etch]	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
MPU gate in resist length (nm)	**53**	**47**	**42**	**38**	**33**	**30**	**27**	**24**	**21**
*Resist Characteristics **									
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†*	**3.3**	**2.9**	**2.6**	**2.3**	**2.1**	**1.9**	**1.7**	**1.5**	**1.3**
*Resist thickness (nm, single layer) ****	**150–265**	**125–225**	**110–200**	**100–180**	**90–160**	**80–145**	**70–130**	**60–115**	**55–100**
PEB temperature sensitivity (nm/C)	**2**	**1.75**	**1.75**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1**
Backside particle density (particles/cm^2)	**0.57**	**0.57**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**
Back surface particle diameter: lithography and measurement tools (nm)	**160**	**120**	**120**	**120**	**100**	**100**	**100**	**100**	**75**
Defects in spin-coated resist films (#/cm^2) †	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
Minimum defect size in spin-coated resist films (nm)	**50**	**45**	**40**	**35**	**30**	**30**	**20**	**20**	**20**
Defects in patterned resist films, gates, contacts, etc. (#/cm^2)	**0.05**	**0.04**	**0.04**	**0.03**	**0.03**	**0.03**	**0.02**	**0.02**	**0.02**
Minimum defect size in patterned resist (nm)	**50**	**45**	**40**	**35**	**30**	**30**	**20**	**20**	**20**
*Low frequency line width roughness: (nm, 3 sigma) <8% of CD ******	**4.2**	**3.8**	**3.4**	**3.0**	**2.7**	**2.4**	**2.1**	**1.9**	**1.7**

† *Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*



2.5.1 Photoresists

The printing industry has been a user of the photoresist for quite a long time. In the 1950s the semiconductor industries used the photoresist for the wafer fabrication processes. In the late 1950s, Eastman Kodak and the Shipley Corporation (now Rohm and Hass), respectively, were the first to introduce the negative and the positive resists [5].

Photoresists are extensively used in the semiconductor industries for production of the sub micron level structures. The composition of the photoresist responds to a particular wavelength obtained from a set of defined exposure sources. The four most important ingredients of any photoresists are polymers, solvents, additives and sensitizes. The photoresist can be further characterized on the basis of its polarity. In a positive photoresists, the exposed part of the resist dissolve, while the unexposed part of the resist is unaffected by the developer reaction. While in the negative resist, the unexposed part dissolve in the developer, and the exposed part remains unaffected. As photolithography relies on the use of UV light source for fabrication, the resist used for pattern development changes as per the corresponding UV light source. The earlier UV sources had wavelength of the order of 405nm and 365nm, but with the further miniaturization of the features, 193nm ArF excimer laser is the current UV source for photolithography. The semiconductor industry would be making a transition to the 157nm light source in the near future. With this transition, a quest for new kind of resist which complies with the ITRS requirement is underway. The most common positive photoresist is the DQN resist, most suited for the i-line and g-line exposures (figure 2.14). As with every photoresist, DQN consists of a photoactive compound (DQ) and matrix material (N). The matrix material (Novolac) dissolves easily in aqueous solution. Though solvents are

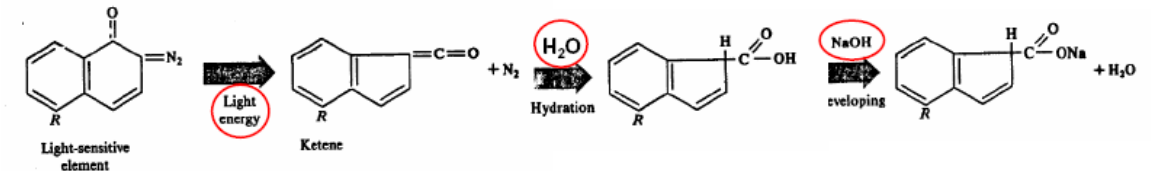


Figure 2.14: Chemical structure for positive photoresist – DQN [23]

added to obtain the required viscosity, most of the solvent evaporates from the resist before the exposure. The photoactive compound – Diazoquinone (DQ) is insoluble in base solution, and changes to carboxylic group on exposure to UV source. The popularity of DQN photoresist is its good resolution capability, environmentally friendly and makes a good mask for plasma etching. With the ever increasing control over the critical dimensions of the features, there is a demand for resists which will satisfy the requirement of the semiconductor industries. One of the most common negative resist used for optical mask production is the SU-8 photoresist (figure 2.15). SU-8 works pretty well in the near UV range and can also be used as an e-beam resist. Features with very high aspect ratio with vertical sidewalls can be easily fabricated using SU-8 photoresist. Other advantages of SU-8 are its high sensitivity, fairly good adhesion properties, and easy processing conditions. Moreover the drying time for film thickness of 50μm is pretty less, thereby saving a lot of processing time.

Both the negative and positive photoresist have almost the same process flow. The wafers are heated to remove any contaminants, followed by application of a adhesion promoter, hexamethyldisilazane (HMDS). The next step involves dispensing a predetermined amount of resist onto the wafer. After spinning, the wafer undergoes pre-bake or often called as soft bake. Pre-baking ensures that most of the solvent evaporates, leaving behind a uniform layer of resist. The temperature and time for pre-baking depends on many parameters which affect the final dimensions of the features. The wafers are later exposed to UV light source-photolithography to transfer the pattern design from the mask to wafers.

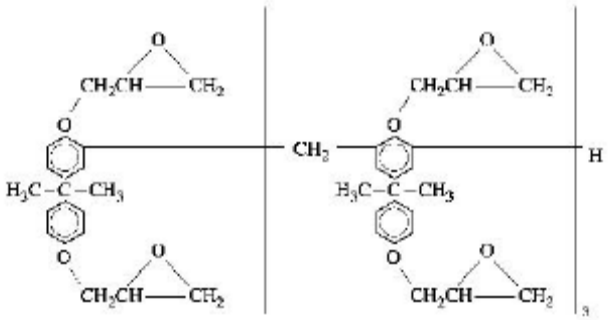


Figure 2.15: Chemical structure for negative photoresist - SU-8 [24]

2.5.2 Electron Beam Resists

Unlike the photoresists which corresponds to a particular wavelength of the UV source, electron beam resists are exposed to a wide range of high intensity secondary electrons with different energies. Hence, there is a complexity in the chemical reactions involved in the bond formation or bond scission. Due to high energy of the electron beam, there is some damage to the substrate which further contributes to the complexity of the chemical reactions. The electron beam resists consist of long chain of carbon polymer, which on irradiation undergoes a process known as cross linking. Materials in which cross linking is a dormant reaction upon exposure are know as *positive resists*, while the materials in which cross linking is the dominant reaction on exposure are known as *negative resists* [11]. Most commonly used positive resist is polymethyl methacrylate (PMMA), which is extensively used for electron beam lithography. There are few other positive resists like EBR-9, PBS and ZEP which also offer good process control, though not as good as PMMA. Some of most commonly used negative resists are COP, Shipley SAL and HSQ. In recent years, hydrogen silsesquioxane (HSQ) has gained importance in terms of its use as an negative resist. Process integration issues associated with HSQ have been extensively studied. Most of the studies suggest the unique chemical structure of HSQ is the main driving force for its use as the electron beam resist. Electron beam resists are primarily used to get high resolution, with very good sensitivity. Features of the order of 10nm or less have been successfully been fabricated using electron beam resists-both positive and negative. The basic resist mechanism for the positive and negative is schematically illustrated in figure 2.16 and in figure 2.17.

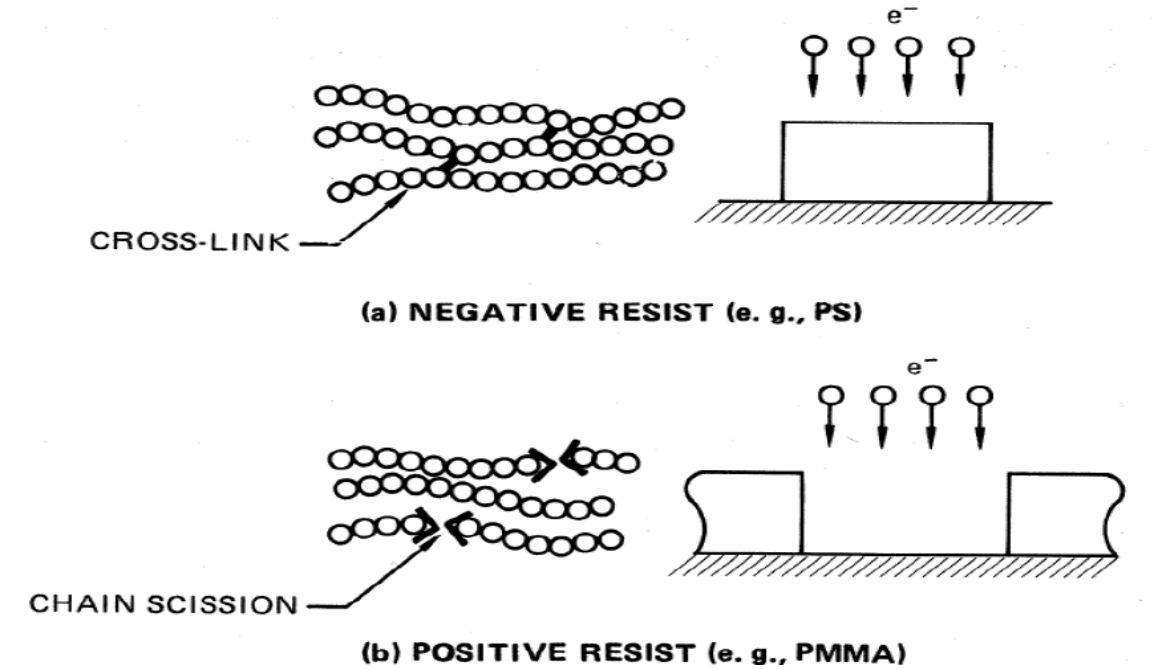


Figure 2.16: Schematic representation of basic resist mechanism

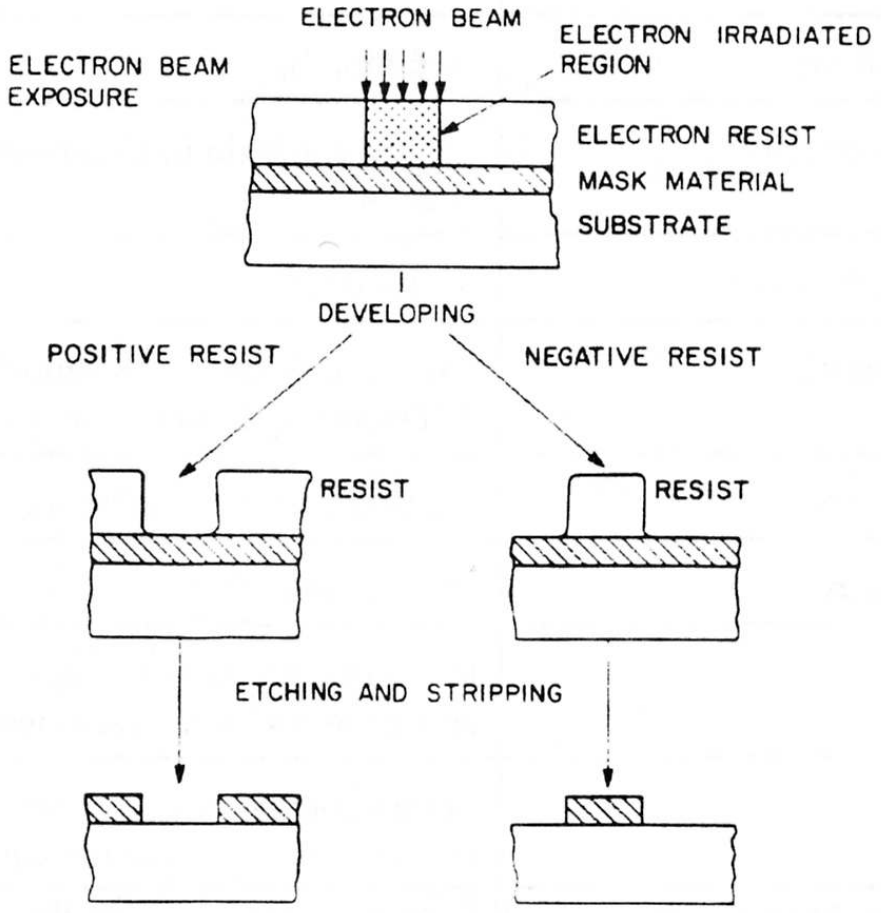


Figure 2.17: Positive resist and Negative resist profile.

2.5.2.1 Polymethyl Methacrylate (PMMA)

One of the most common electron beam resist is polymethyl methacrylate (PMMA). It is considered to offer the highest resolution in any organic resist, hence PMMA is extensively used in the research and development of new lithography process. PMMA is normally not used for manufacturing process due to its low sensitivity [25]. It is generally used for short wavelength lithography: deep UV (220-250nm), extreme UV and electron beam lithography. Cross linking and fragmentation are the key to the formation of polymeric chains in polymethyl methacrylate (PMMA). The monomer of PMMA:

$$-[CH_2\text{-}CCH_3(COO(CH_3))]-$$

Unlike other hydrocarbon polymer, PMMA has very poor etch resistance which is one of the reason for using PMMA as a mask material. MicroChem Corp is one of the leading companies manufacturing positive electron beam resist PMMA. Normally, 495K and 950K molecular weights of PMMA are available formulated either in acetone or cholorobenzene. Unlike, the photoresists which require a photoactive compound (PAC) for sensitization by radiation, PMMA itself sensitizes upon radiation. It offers high resolution with good contrast and fair amount of sensitivity. The ultimate resolution of PMMA is affected by various parameters like the edge roughness, surface roughness, swelling of the resist and most important scattering of the electrons (proximity effect). Extensive research has been carried out to reduce the problems which are hindering the resolution of PMMA. Contrast, sensitivity, molecular weight are some of the other parameters which can influence the resolution of the positive resist. Moreover, the developing conditions also have effect on final resolution limit of the positive resist - PMMA (figure 2.18).

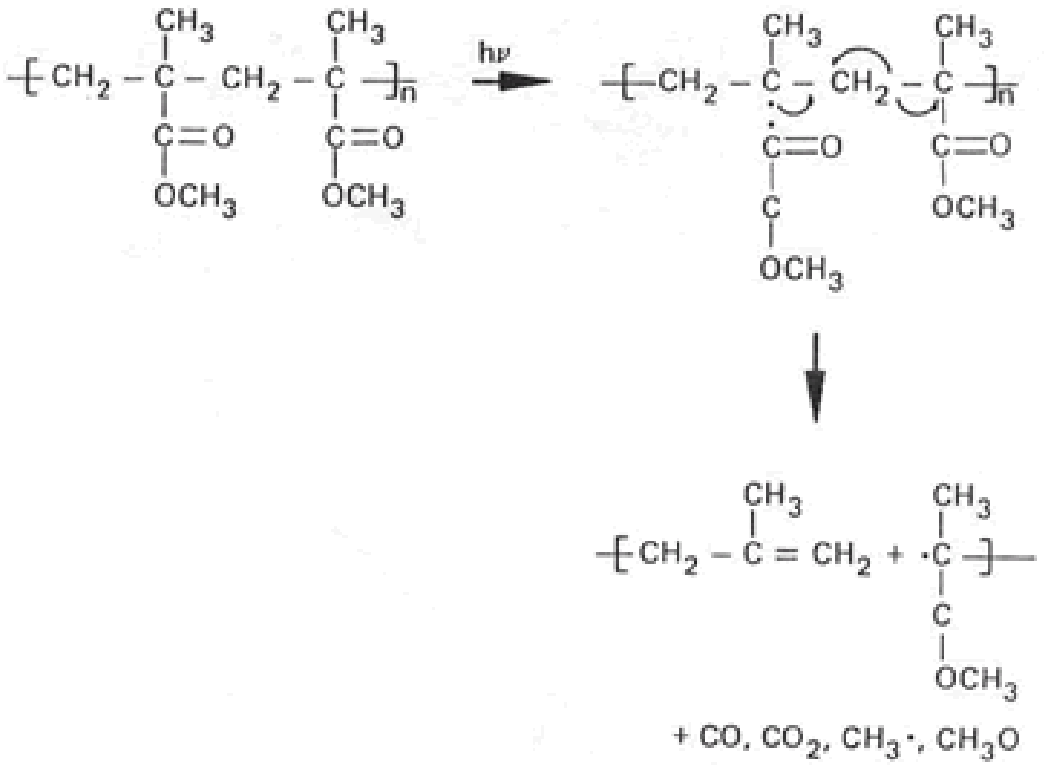


Figure 2.18: Chemical structure of PMMA : pre development and post development.

For electron beam resist, most of the development solutions consist of a strong solvent and a moderate non-solvent. The influence of these binary solutions on the developing conditions of any resist is complex reaction. One of the parameter which is affected by these binary solutions is the swelling, which in turn affects the resolution of the resists [26]. Molecular weight of a polymer determines the solubility of polymeric matrix after exposure. Plasticization and thermodynamic compatibility between the resist and the developer affects the solubilization rate [26]. The most common developer solution for PMMA is a mixture of Methyl Isobutyl Ketone (MIBK) and Isopropyl Alcohol (IPA) in varying proportion. MIBK:IPA (1:3) and MIBK:IPA (1:1) are some of commonly used development solution. The exposed part in the PMMA resist is removed, while the unexposed part of PMMA is unaffected when the development is carried out in MIBK:IPA. It is generally accepted that increasing the MIBK ratio, increases the sensitivity of the resist, but decreases the contrast value, thereby making it unsuitable for nanofabrication. S. Yasin et al have developed an alternative developer scheme for PMMA resist, which increases sensitivity (~40%), in contrast (~20%) compared to the MIBK:IPA 1:3 developer [26]. They used binary solution of Water:IPA (3:7) as a developer for PMMA to get best combination of sensitivity and contrast. When PMMA is developed in Water:IPA (3:7) solution, H_2O molecule causes swelling of the exposed region, which is later on removed by IPA. Main chain scission occurs when the carbon-carbon bond breaks into carbonyl carbon bond, causing volatile products as CO, CO_2, CH_3O and others [27]. This developer scheme ensures a low thickness loss for the unexposed region, thereby giving a good combination of contrast and sensitivity.

2.5.2.2 Hydrogen Silsesquioxane (HSQ)

A low-k dielectric material, Hydrogen Silsesquioxane (HSQ) has long been used as an interlayer dielectric (ILD) in the semiconductor. Ultra high purity grade of HSQ is available from Dow Corning Corp., in form of Flowable Oxide® (FOx®) in different concentration grade. In recent years, lot of research has been focused on use of HSQ as a high resolution electron beam resist. HSQ has a negative tone, can be imaged directly in a SEM, and has high contrast and moderate sensitivity. HSQ is an inorganic resist with three dimensional structure which undergoes cross linking on exposure to electron beam. The cross linking in HSQ creates a structure on same lines of silicon dioxide [28]. Thermal treatment greatly affects the final structure of HSQ, which in turn can affect the ultimate resolution of the resist.

In generality, HSQ has a cage like structure which further changes to network like structure. There are two different schemes which define the chemical structure for HSQ. In the first case, HSQ is assumed to have a structure with silicon (Si) atom bound to three oxygen (O) and single hydrogen (H) atom (figure 2.19). During curing, a cross linking takes place with condensation of Si-OH group to Si-O-Si group, thereby forming a three dimensional structure [29].

In second case, HSQ is considered to have a caged oligomer structures with the general formula $(HSiO_{3/2})_{2n}$. The caged oligomer structure open up to form a network like structure. For electron beam exposure, the energy deposition is pretty high, hence bond scission and network forming is more pronounced during the exposure period, than the development period [29]. Being a negative resist, on development the unexposed part is dissolved while the exposed part is unaffected due to cross linking or network formation.

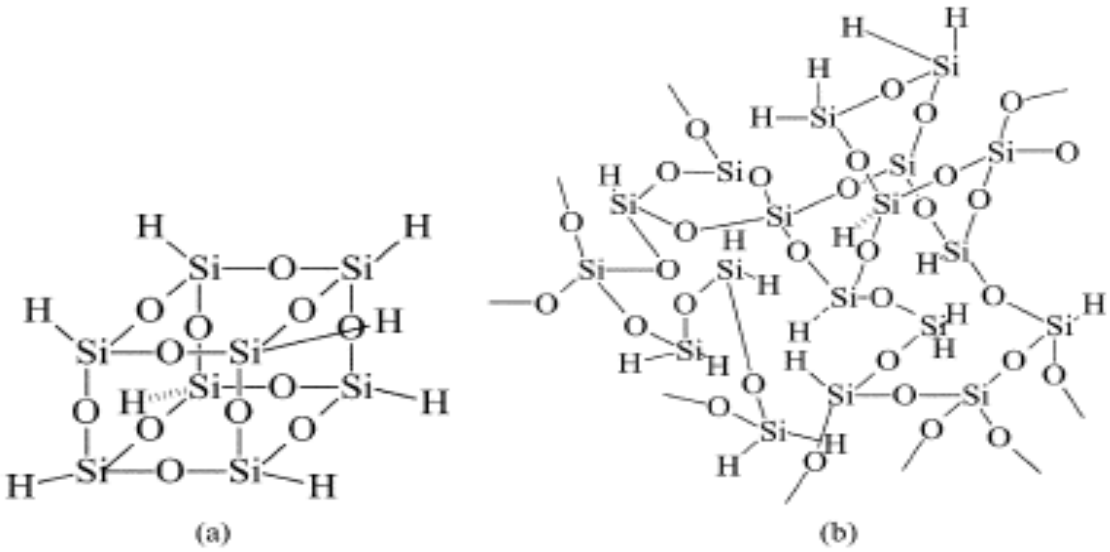


Figure 2.19: Chemical structures of HSQ (a) cage form (b) network form [30]

The development in tetramethyl ammonium hydroxide (TMAH) facilitates the bond scission in the unexposed part on the resist. The electron beam exposure gives rise to three dimensional network like structure, which decreases the dissolution rate in the exposed part of the resist during the development process in TMAH. Some of the factors like the exposure dose, baking time, baking temperature together with the developing conditions greatly affect the contrast and the sensitivity of the negative resist HSQ.

As the feature size continues to decrease, newer kind of resists are being produced to obtain the optimal conditions for fabrication. *Resolution* is the ability of the resist to reproduce smallest feature size within the standard deviation. Resolution of any resist depends on the interaction of the electron beam with the resist layer. Scattering caused by the electrons can affect the resolution of the resist, which in turn, causes increase in the dimension of the features. Resolution of a resist in more generic terms is related to the contrast of the resist.

Contrast of a resist relates to the polymeric chain breakage and the change in solubility of the resist. In general terms, *Contrast* is defined as the ability of the developer solution to distinguish the small changes in the exposure dose from one region to another. Since the exposure in the electron beam lithography is not localized due to the Gaussian nature of the beam, there is spread of exposure dose affecting the contrast of the resist. Contrast is also defined in terms of sharpness of the developing threshold of the developer-resist system [25]. This threshold value of the system can be obtained from the contrast curves (figure 2.20).

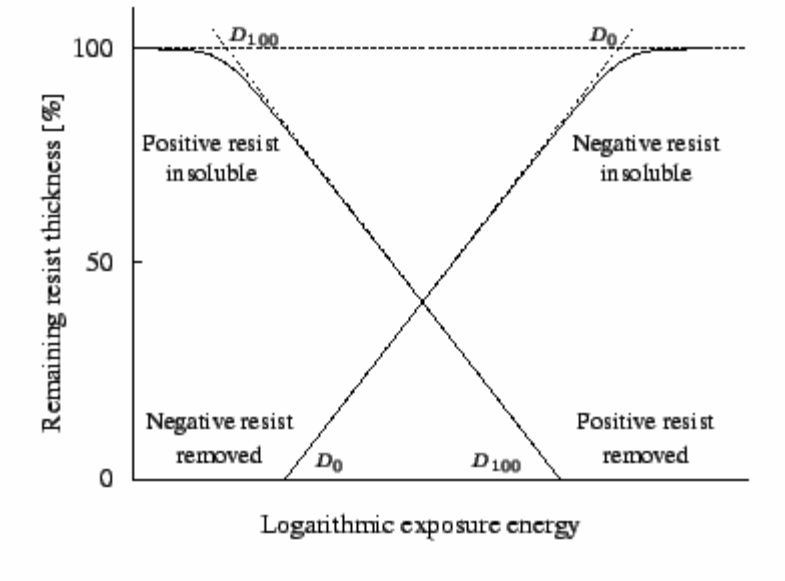


Figure 2.20: Contrast curves for both positive resist and negative resist [31].

As shown in the figure 2.20, D_{100} is the dose of the extrapolated curve at 100% remaining thickness, while D_0 is the dose of the extrapolated curve at 0% remaining thickness [31]. Thus, the contrast in the terms of γ [31] is given as

$$\gamma = \left[\log\left(D_{100} / D_0\right)\right]^{-1}$$

A surface profilometer measures the thickness of the resist before and after development cycle, and then contrast curve is plotted in terms of remaining resist thickness to logarithmic exposure.

Along with contrast, *Sensitivity* also plays an important role in determining the ultimate resolution of the resist. Sensitivity is defined as the minimum electron dose required to fabricate the defined feature size. M. Hatzakis has defined sensitivity as, "minimum electrical charge per unit area of resist film required for complete development of the area." [32] The sensitivity of a resist also depends on other parameters like the exposure dose, the baking condition, development temperature, scattering of the electrons (proximity effect) and molecular weight of the resist. In presence of an ideal developer, sensitivity can also be defined as minimum electron dose which produces distinct molecular distribution for both exposed and the unexposed part of the resist [33].

The sensitivity of the positive and negative resist is different in accordance with their respective reactions with the developer. For the negative resists, sensitivity drops with increasing developer concentration, while it increases with rise in the baking temperature. Irrespective of the type of resist used, the process flow for lithography is the same. The common steps in the process flow include wafer cleaning, spinning, baking, exposure, development followed by imaging or data analysis.

2.6 Lithography process flow

The process flow shown in the figure 2.21 and the following literature describing the process steps is exclusively for electron beam lithography fabrication for research activities. On an industrial scale, the process flow is somewhat similar with some additional steps required. The description of the process flow for semiconductor industries is not been touched upon for this literature review.

2.6.1 Cleaning of wafers

For a semiconductor process, a clean wafer with none or negligible contamination is very important part of fabrication. To ensure this cleanliness, the wafers undergo different cleaning process in accordance with the contaminants present. The cleaning process is normally carried out in clean room environment. The most common cleaning technique is the Piranha Etch. Piranha Etch is carried out in a hot mixture of hydrogen peroxide and sulphuric acid, and is normally used to remove hardened organic resists from the wafer surface.

While another form of cleaning is the RCA cleaning technique which is used during the front end processes. It is normally used to remove the contaminants formed during oxidation, diffusion processes. The RCA procedure involves three more stages:

(1) Organic Clean with a mixture of 5:1:1 H_2O:H_2O_2:NH_4OH solution.

(2) Oxide Strip with a diluted solution of 50:1 H_2O:HF solution.

(3) Ionic Clean with a mixture of 6:1:1 H_2O:H_2O_2:HCl solution.

The RCA cleaning technique does not affect the silicon, but a small amount of silicon dioxide. The cleaning prevents replating of metal contaminants from solution back to the wafer surface [38].

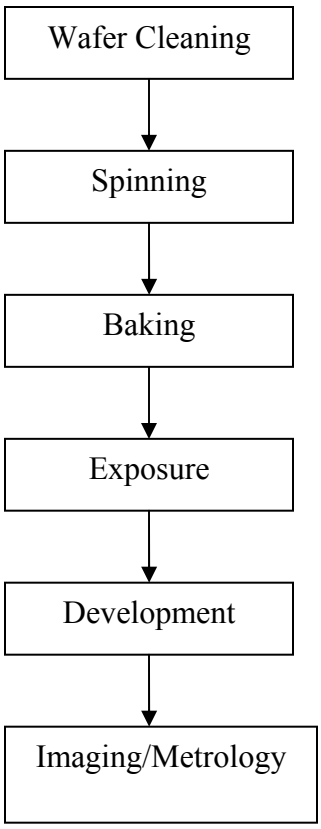


Figure 2.21: Flow sheet for lithography process

2.6.2 Spinning resist on wafer

After cleaning of the wafers, the next step involves spinning resist on wafers. This is normally done either by *static dispensing* or *dynamic dispensing*. Static Dispensing involves dispensing resist just before the wafer is spun, while dynamic dispensing involves dispensing the resist while the wafer is spun at low speeds (figure 2.22).

After dispensing the resist on the wafer, acceleration is provided to spread the resist over the surface of the wafer. Normally, spin speeds in the range of 2000-6000 rpm are used. The centrifugal force caused by the spin speeds and the time for spinning defines the final thickness of the resist. Along with the speed and the time for spinning, the physical properties of the resist, viscosity also affects the resist thickness. The higher is the acceleration and more is the spinning time, thinner is the thickness of resist. Depending on the type of the resist used, positive tone - PMMA or negative tone - HSQ the parameters for spinning changes.

Polymethyl Methacrylate (PMMA) used for the research work is being supplied by MicroChem Corp. PMMA is available in molecular weights of 495K and 950K formulated in a thinner called Anisole. The molecular weight of PMMA greatly affects the final thickness of the resist. At the same spin speeds, low molecular weight PMMA (495K) gives lesser resist thickness compared to high molecular weight PMMA (950K). In absence of a clean room environment, the surrounding room temperature plays a critical role is determining the spin speeds and spin time for the final resist thickness. Figure 2.23 and figure 2.24 , gives some spin curves for the 495K PMMA and 950K PMMA formulated in anisole.

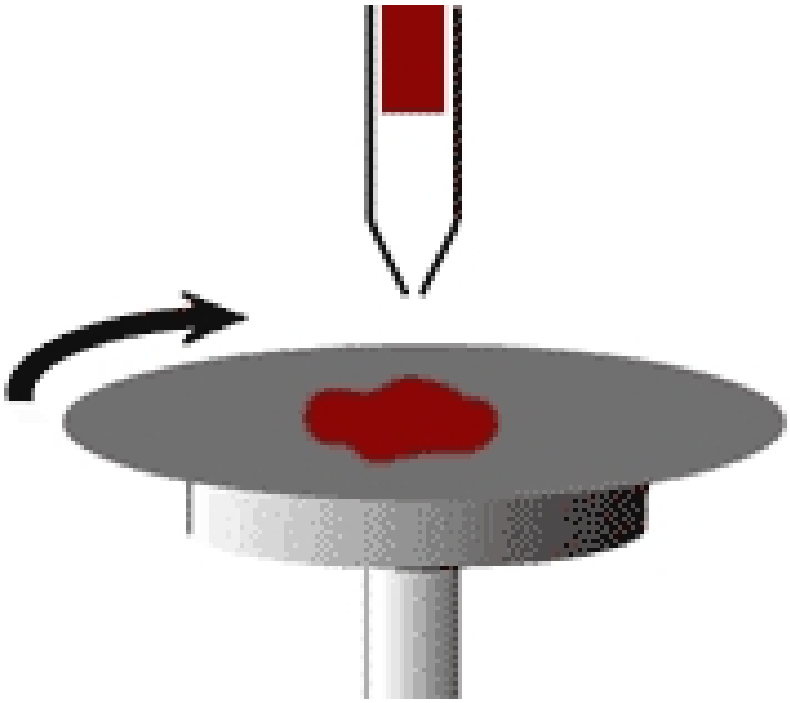


Figure 2.22: Schematic representation of resist spinning [39]

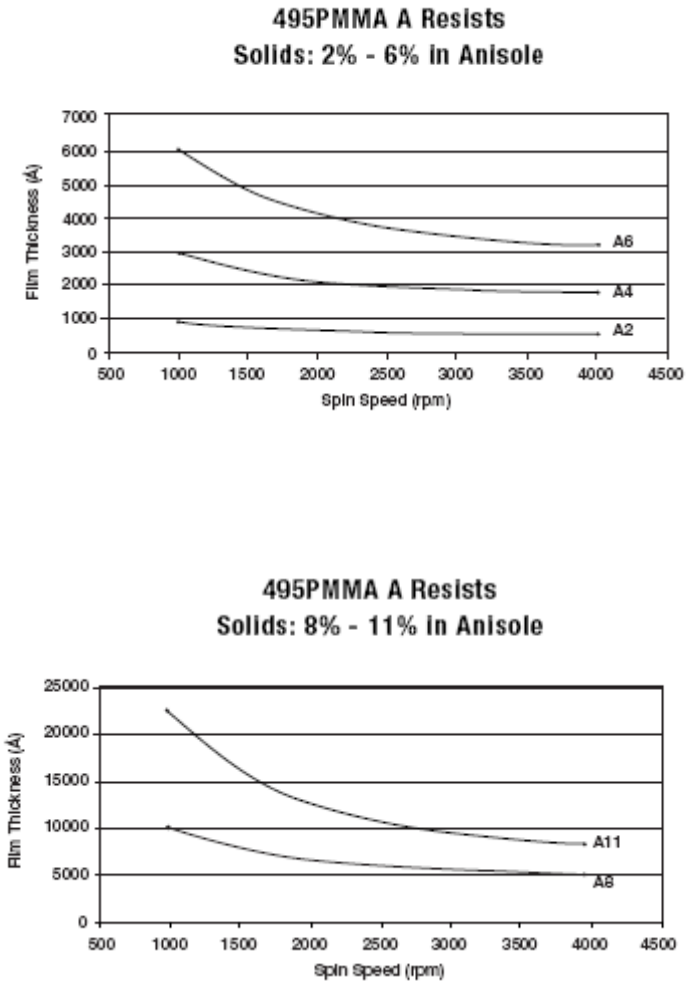


Figure 2.23: Spin Curves for 495K PMMA formulated in Anisole [40]

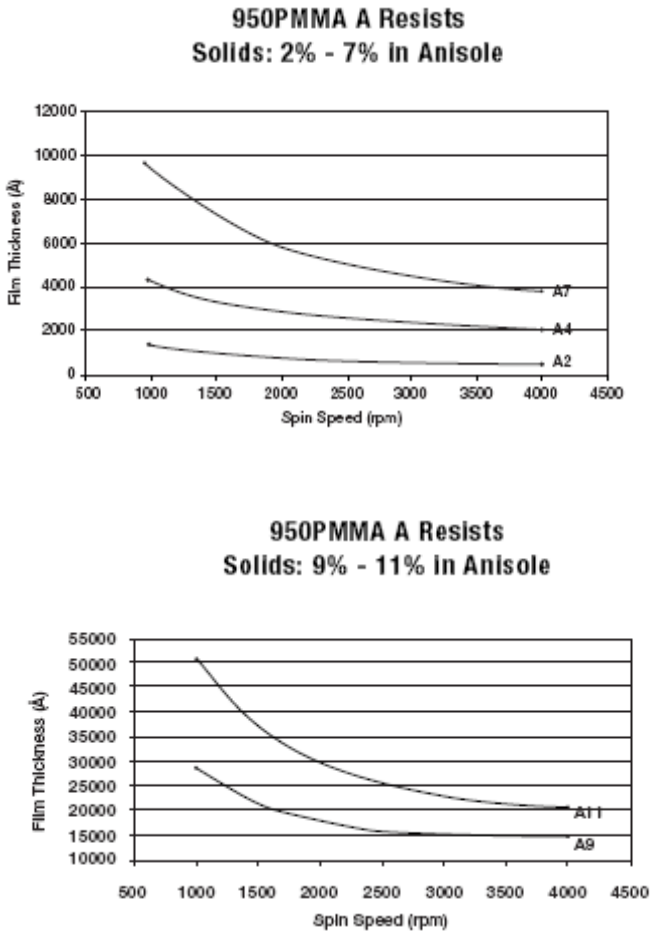


Figure 2.24: Spin Curves for 950K PMMA formulated in Anisole [40]

The dependence of spin speeds on the final resist thickness is graphically represented as the *spin curves*. Spin curves provides an approximate information regarding the type of spinning speed required for the resist thickness, though the actual results vary depending on the type of the equipment used, the surrounding room temperature, the various process parameters.

2.6.3 Baking of the resist

After spinning of the resist onto the wafer surface, another important step involves baking the wafer to remove the excess amount of solvent from the resist and strengthen the bonds in the resist (figure 2.25). The baking temperature influences the resist thickness to a large extent, a higher baking temperature and a longer baking time will give a thin resist layer. Baking is usually carried out in an oven or a hot plate. Heating mechanism in an oven employs heating from top surface to the bottom of the wafer. This causes a skin effect, wherein the topmost layer of the resist dries out without complete evaporation of the remaining solvents in the bottom layers. Industrially hot plates are gaining dominance because of their bottom to top heating approach. This ensures a thorough heating of the wafers without any skin effect. Baking of the wafers can be categorized into two groups: *Pre Exposure Bake* and *Post Exposure Bake*. *Pre Exposure Bake,* also called as soft bake is carried out before the exposure of the wafers, to obtain the final resist thickness. Electron beam resists like PMMA or HSQ undergoes pre exposure bake. *Post Exposure Bake* is normally carried out after the development process to harden the resist for the subsequent pattern transfer process like etching or liftoff. Photoresists like Shipley SU-8, DNQ are normally subjected to post exposure bake. Figure 2.26 shows the baking system (Brewer Science Cee 100CB) in our facility.

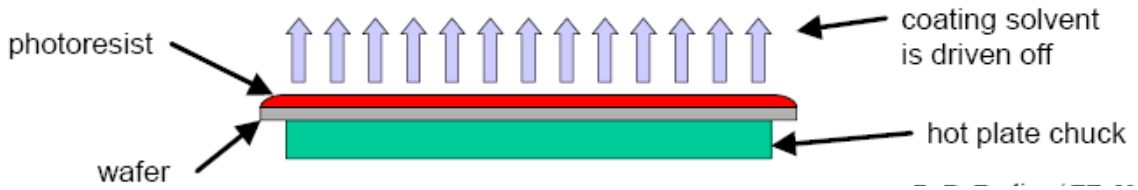


Figure 2.25: Baking of the resist spun on the wafer.

Figure 2.26: CEE 100CB for spinning and baking.

2.6.4 Exposure of the resist

After spinning and baking, the wafers are put through the exposure technique using either the electron beam lithography or photolithography. Electron beam lithography is a direct write lithography which is normally used for mask fabrication. It offers a high precision writing, but is a slow process compared to photolithography. Hence, commercial use for manufacturing wafers by electron beam lithography has not been established.

The mask fabricated using the electron beam lithography is being used for photolithography, which traditionally has been the workhorse for wafer manufacturing. In electron beam lithography, typically beam voltages of the order of 50KV to 100KV are used for fabrication purposes. Higher the beam voltage lower is the forward scattering which can reduce the proximity effect and small features require a higher electron dose to get minimum line edge roughness. Hence, a proper selection of the beam voltage and the amount of exposure ($\mu C/cm^2$) has to be determined to obtain features as small as possible and with minimum proximity effect.

Irrespective of the type of resist used, a broad range of exposure dose is determined using the contrast curve. This broad range of dose helps in determining the dose to be given for optimum resolution, though actual exposure dose is finalized after taking into consideration different parameters like the pattern design, proximity effect, proximity effect correction. In general, the exposure dose required for the positive resists is comparatively less than the negative resist. For most cases, the exposure dose for PMMA is in the range of 100 – 700 $\mu C/cm^2$, while for negative resist like HSQ the exposure dose can be more than 900$\mu C/cm^2$ and increases more as the size of the features decreases.

2.6.5 Developing of the resist

After undergoing irradiation either by electron beam or UV light, the polymeric resist undergoes both scission and crosslinking process. Polymeric resist with predominant scission process is termed as a positive resist, while the polymeric resist with crosslinking as a predominant process is termed as a negative resist [33]. The effect of the scission and crosslinking can be observed after the development process. In electron beam lithography, development of irradiated polymeric resist uses binary solvent mixtures typically consisting of a strong solvent and a mild non-solvent [26]. The influence of this binary solvent mixture on the swelling and dissolution behavior normally is determined by looking at the resist profile. Distortion in the resist profiles is normally associated with the swelling process, which increases with decrease in the pattern size and increase in the circuit density.

Thus the development process becomes really important since it influences the surface and edge roughness of the structure in the resist. Also, the development influences the phase separation of polymer rich and polymer poor phases [41]. The roughness is normally increased with increasing exposure dose and with delay in dissolution rate of the polymer rich phase which leaves behind some roughness in the structures [41]. The development mechanism is different for the positive and the negative resists. In case of the positive resists, the exposed part is removed by the developer and the unexposed part still remains on the substrate. While in case of negative resists during development cross linking takes place in the exposed part, thereby strengthening it, whereas the unexposed part is removed by the developer. After development the substrate is normally dried in a flow of ultra high pure nitrogen gas.

For positive resist-PMMA, the development process is carried out in a mixture of MIBK:IPA with varying concentration, followed by rinsing in IPA. Methyl isobutyl ketone (MIBK) is a strong solvent dissolving the exposed part and the unexposed part (to a lesser extent) [27]. Thus the sensitivity increases at the cost of loss of thickness of the unexposed region. To achieve optimum lithographic conditions a clear distinction between exposed and unexposed region is needed, which can be achieved by adding some amount of isopropyl alcohol (IPA). The role of IPA is to decrease the overall "development strength" of the developer [27]. Normally, mixtures of MIBK:IPA in concentration of the order of 1:3, 1:2 and 1:1 are used. Traditionally, MIBK:IPA 1:3 is used since it provides negligible thickness loss in the unexposed regions, higher contrast, high resolution and moderate sensitivity [27]. But on reducing the amount of MIBK in the mixture reduces sensitivity, but helps in increasing in the contrast of the system.

Besides the traditional MIBK:IPA mixture, efforts are being made to have a new developer for PMMA. S. Yasin et al [26] have successfully developed a new developer mixture consisting of 3:7 Water:IPA. Their experimental results clearly indicate an improvement in sensitivity (~40%), in contrast (~20%), in exposure dose latitude (~40%) and in roughness compared to the conventional MIBK:IPA mixture [26]. Since water and IPA separately are non solvents for PMMA, they act as co-solvent when used together as mixture. The dissolution mechanism of PMMA in water:IPA mixture has not been understood properly. One explanation suggests that since the molecule size of H_2O is small, it helps in diffusion of water molecules in the exposed part. Chain scission in PMMA is initiated by cleavage of carbon bond causing volatile product. The volatilization caused by the chain scission increases the free volume in the exposed part

of the polymeric resist. This facilitates the diffusion of water molecules which leads to swelling of the exposed part. This swelling is instantly removed by IPA, with diffusion proceeding smoothly and H_2O diffusion controlled [27]. In unexposed part the free volume of PMMA is very small, hence the diffusion rate of water molecules is less. Thus, low thickness loss of the unexposed part which in turn gives good resolution and contrast [27].

For negative resist-HSQ, the development process is normally a three step process which is complex to understand. Conventional developing sequence is development in 2.38% TMAH, followed by development in 1:9 TMAH:DI and finally development in DI. The development process is to some extent dependant on the baking conditions of the negative resist. The baking process promotes both the scission and crosslinking which helps in transition from the cage like structure to network like structure. During the baking, the number of free Si bonds increases with increase in the baking temperature, due to incomplete recombination of broken Si-O and Si-H bond. On development in alkaline solution like TMAH, the free Si bonds in the exposed region reduces the dissolution rate by forming a three dimensional network structure, in some cases as silica. While in the unexposed part, the unexposed HSQ is quickly dissolved and removed from the substrate (figure 2.27).

Along with the baking condition, the concentration of the alkaline solution TMAH is an important parameter which decides the development process. Most of the literature available for HSQ processing uses 2.38 % TMAH, though W. Henschel et al [29] have successfully done experiments using 25% TMAH for their research work.

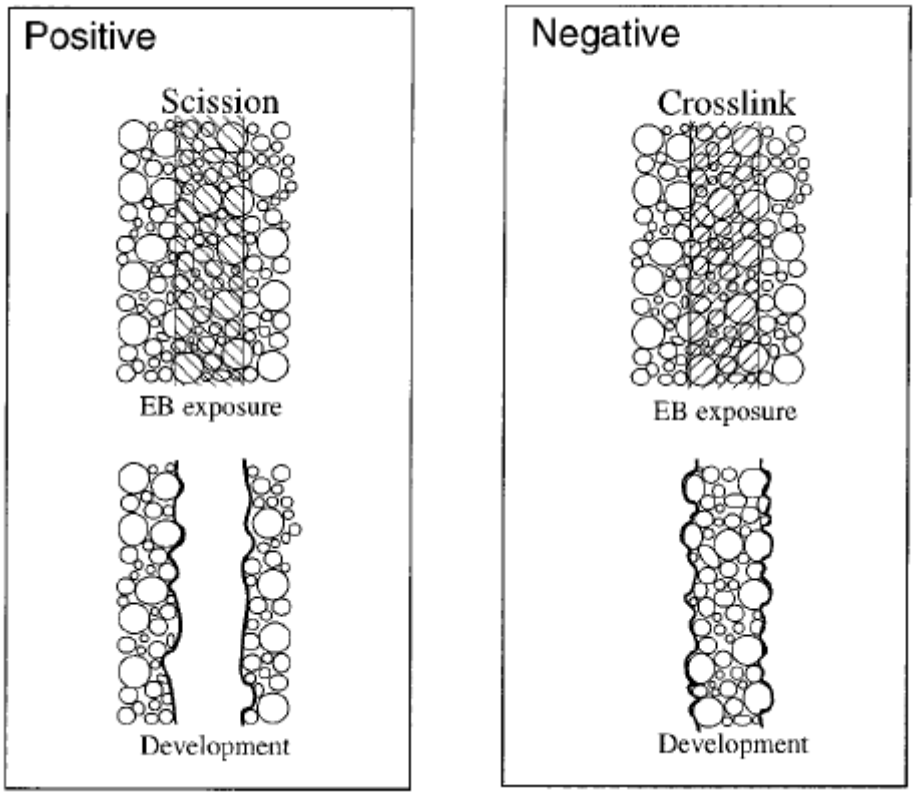


Figure 2.27: Schematic diagram showing development process for both positive and negative resist [42].

2.6.6 Imaging and Metrology

Development of the resist is the final step involved in the fabrication of the patterns. Depending upon the tone of the resist, a distinct profile of the patterns is obtained in the polymeric resist. The next step normally involves imaging of the pattern profile either using the SEM or the AFM. In most cases, the SEM is extensively used for imaging since it is useful in obtaining the lateral profile of the pattern structure. Imaging under the SEM involves putting the substrate in the working chamber of the SEM evacuated to a pressure of 10^{-6} Torr. The working chamber has detectors which can detect the secondary electrons as well as the backscattered electrons emissions. Imaging is done depending upon the type of the resist used on the substrate. Substrates coated with positive tone resists can be imaged at high voltages of the order of 12-15 kV. In case of substrates coated with negative resists, low voltages are needed. For the positive tone resist – PMMA, there is a need of a thin layer of gold or any other metallic film. In contrast to the positive tone resist, HSQ is highly stable under a SEM and requires no deposition of thin layer of gold for imaging.

Measurement of the patterns fabricated is typically referred to as *Metrology*. In a broader aspect, the *International Technology Roadmap for Semiconductors* (ITRS), defines Metrology as measurements that are done in situ, in-line and off-line [3]. *Off-line metrology* refers to measurements done outside the Fabs, typically in any research and development lab [36]. *In-line metrology* involves measurement done during the actual processing steps in a Fab [36]. While, *In-situ metrology* refers to measurements and process control done using sensors placed inside the process chamber or as a part of a loadloack or wafer transfer chamber [36]. Metrology requires a background in process

technology and the understanding of the measurement and physics of the semiconductors. Metrology can further be characterized in a broader sense as *Overlay Metrology* and *Critical Dimension Metrology*. Usually, a chip is manufactured by stacking multiple layers of resist, metal, oxide and other materials in perfect alignment. The measurement of any misalignment in stacking of these layers is referred to as *Overlay Metrology* [36]. While, the *Critical Dimension Metrology* involves measuring linewidth, pitch of the features of interest [36]. With the semiconductor industry in the sub-100nm region, the measurement of the small feature sizes is known as Nanometrology.

The ITRS is responsible for determining the tolerances for error in the processing of these fine features. The ITRS publishes all these tolerances for the current technology node and also for nodes coming in the future. Until recently with the current features sizes under production, the semiconductor industry heavily relied on the optical microscopy for metrology of the feature sizes. But with features sizes falling below the wavelength of line, more focus is being paid on metrology using the electron microscopes. Thus, over the period of time Critical Dimension – Scanning Electron Microscope (CD-SEMs) have gained importance. CD-SEMs are like any other conventional SEM, but with some special data processing capabilities for Critical Dimension measurement. These machines are expensive and are far from being perfect in terms of the results they give out.

Hence, alternative solutions for metrology have been seriously being considered in last few years. One such solution that is considered to be important for metrology is Scatterometry technique. Further, explanation regarding the CD-SEMs and the Scatterometry would be given in the following literature.

2.6.6.1 Critical Dimension – SEM (CD - SEM)

The CD-SEMs have been the workhorse for the metrology purposes in the semiconductor industry. With the feature sizes decreasing with every technology node, newer approaches such as optical Scatterometry and CD-AFM are being evaluated. CD-SEMs are like any other conventional SEM, but with a wafer handling system capable of handling the 200 mm and 300 mm wafers. It also equipped with a laser controlled stage and data processing software. Since the working of the CD-SEMs is more like conventional SEMs, the key parameters that define SEM operations are probe size, beam current, beam energy and scan speed [9]. The current trends in these parameters, the factors that govern them and implications following any change in the parameters are summarized in Table 2.4.

The two most important parameters which need to be controlled are the charging and the beam induced damage. Efforts are being spent to obtain an optimum correlation between the two parameters to ensure efficient operating conditions for the CD-SEMs.

Table 2.4: CD-SEM parameters and factors which drive their choice [9].

Parameter	**Trend**	**Drivers**	**Consequences**
Beam Energy	Lower	Charging Beam Damage	Degraded electron optical performance Diffraction limited Poor source brightness
Beam Current	Constant	Trade-off between throughput rate, damage and charging	Marginal signal to noise
Spot Size	Smaller	Resolution “Precision”	Lower beam current Degraded signal/noise Decreased depth of field
Scan Speed	Higher	Throughput Charge Control	Stress on video component Poor linearity

As quoted by David Joy, "The downward trend towards in beam energies, and the search of ever faster scan speeds, mostly represent a response to the desire to eliminate charge induced artifacts in the image and to minimize the shrinkage (or, occasionally the swelling) of the resist" [9]. The need to measure the small feature sizes necessitates the requirement of smaller beam spot, which in turn means higher beam current. But higher beam current may give unsatisfactory signal to noise ratio. Also, lower beam current means lower beam brightness, which again necessitates the need for an emitter with high intrinsic brightness [9]. A cold field emitter can resolve this problem, but produce more noise and drift compared to schottky emitter. Another disadvantage with lower current is the slow throughput. Higher scan speeds can improve the throughput, but at the expense of poor imaging and significantly degraded signal to noise ratio [9]. Hence, it is very important to determine the optimum combination of parameters for the CD-SEMs.

This uncertainty in the role of CD-SEMs as the future tool for metrology lies with its inherent fundamental limitations, and not the design [9]. To overcome this situation, rethinking of the very purpose of the CD-SEMs has to be evaluated (Table 2.5).

Table 2.5: Some key parameters, and their possible solutions [9].

Key parameters	**Possible solution**
Resolution	Aberration correction, Higher beam energy
Charge control	Lower beam energy, Low vacuum operation
Beam induced damage	Ultra low energy
Throughput	Multiple columns

In a conventional CD-SEM, the electron beam scans the specimen placed in the specimen chamber. The secondary electrons, backscattered electrons and other emissions are collected by their respective detectors. The images in CD-SEMs are usually formed by the secondary electrons (SE). Normally, at the edge of line the diffusion range of the SE signal causes an increase in the intensity at the line edges (figure 2.28). This increased intensity at the edges, typically referred to as "edge bright line" [9]. In most resists, the width of this line is of the order of few nanometers, thereby rendering inaccuracy in the line width measurements.

When the linewidth reaches the SE diffusion range, the signal intensity at the edges decreases, and finally merges to form the signal profile as shown in figure 2.29. Sharp intensity peaks typically referred as "blooms" decreases, indicating the ultimate resolution limit for the CD-SEMs [9]. For conventional CD-SEMs, the ultimate resolution is considered to be ~ 5nm for silicon lines [9].

This resolution limit of the CD-SEMs can be overcome by using high energy incident electron beam. But this also may result into charging and beam induced damage to the features of interest. Another, alternative is the use of the backscattered electrons for the imaging purposes. The backscattered signal is closely related to geometry of the feature, simplifying the analysis of profiles, and charging with negligible consequences [9].

The CD-SEMs have come a long way since its inception in the semiconductor industry couple of decades back. The CD-SEMs are best suited for the current technology node, and maybe for next couple of technology node. But with the feature sizes decreasing to 32nm in next decade or so, measurements of these small features is going to be major cause of concern for the semiconductor industry.

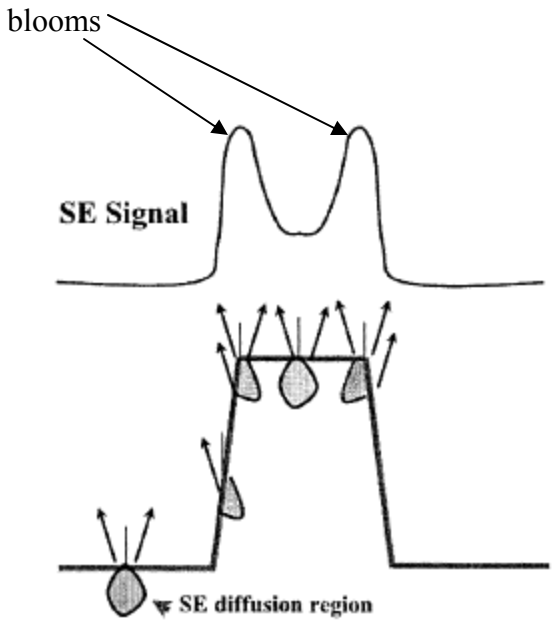


Figure 2.28: Schematic representation of signal intensity at the line edges [9].

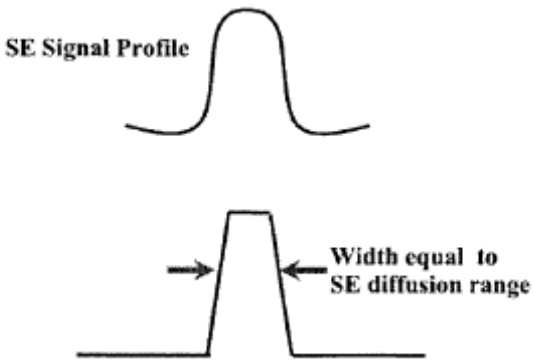


Figure 2.29: Schematic representation of the resolution of the CD-SEM [9].

With the feature sizes getting well below 100nm, accuracy in the linewidth measurement is becoming a critical problem for the semiconductor industry. With an accuracy control of the order of 1nm needed for the future technology node, measurements by CD-SEMs are an area of concern. There are no proven algorithms for linewidth measurement by the CD-SEMs. Tool manufacturers set up the edge detection voluntarily, as a rule, which is why the absolute errors in measurement occur [47].

S. Babin *et al* [47] have developed the CHARIOT software, which uses advanced Monte Carlo simulation for accurate determination of the line edge. The electron scattering by a beam irradiating a target can be determined with the help of Monte Carlo model [48]. The CHARIOT software uses this model, along with generation of fast and true secondary electrons, inelastic energy loss and plasmon mechanism.

A lot of research has been carried out to determine an alternative route for linewidth measurement, totally independent of the CD-SEM measurements. For quite some time, metrology using Atomic Force Microscope (AFM) has been strong considered as an alternative to the CD-SEMs. The ITRS predicts that AFM will be one of critical dimension (CD) metrology tools starting at the 65nm node. However, at the same time it presupposes there would be new probe tip technology which can be used for features well below 90nm [49]. It also predict that high stiffness probe materials , such as short carbon nanotubes (CNT) might be used for overcoming this problem [49].

B. C. Park *et al*[49] have done considerable work in using the CNT on the AFM probe tips for measurements. They have developed three different types of CNT tips which will sastisfy the requirements in both the size and accessibility to the re-entrant sidewall. [49] Though actual tests in the CD-AFMs are still awaited.

CHAPTER 3

EXPERIMENTAL PROCEDURES

3.1 Selection and Designing of the artifact

With ever decreasing device CDs, the characterization of these dimensions has become an important step in the semiconductor industry. With the technology node making a transition from the 90nm to 65nm, and later on to 45nm, the gate length would be in the range of 10-30nm. Since the performance of any device is directly related to the dimensions of the gate, controlling the dimensions of the gate is highly important. Fabricating such small dimensions of the gate would be a technological challenge, and measurements of these dimensions for the accuracy and precision would be a necessity.

The determination of the critical dimension of the feature size is broadly defined as *Metrology*. Current metrology measurements are mostly carried out using the CD-SEM, a high resolution SEM capable of low voltage imaging and equipped with software capable to process the dimensions of the device [9]. Metrology using CD-SEMs relies on an assumption that the magnification stated is correct, since the working distance and deflection angle of the beam are "known", but any charging of the sample during imaging makes this assumption incorrect [34].

Thus it becomes highly critical to measure the magnification calibration of the CD-SEMs on a regular basis to ensure the accuracy in the linewidth measurement. There are some calibration standards which are being provided by the SEM vendors, but not accessible to everyone. This hinders the evaluation of the magnification calibration of the CD-SEMs. Thus an easy access to a traceable calibration standard suited for sub 100nm metrology

will facilitate in the magnification calibration of CD-SEMs, and thus ensuring the precision and accuracy for the sub 100nm metrology area.

Taking into consideration this need for a calibration standard in the sub 100nm region, the project focuses on fabrication of sub 100nm artifact which can not only be used for the current technological node, but also for the future technological node [35].

3.1.1 Selection of the artifact

Since the artifact is to be used as calibration standards, an array of parameters like the linewidth, pitch, line edge roughness and line width roughness have to be incorporated while selecting the design for the artifact. Any discrepancy in any of the above parameters will affect the calibration of the CD-SEMs, which in turn will give a false performance review for the CD-SEMs. Wide spectrums of designs for the artifact covering the aforesaid parameters were evaluated. Artifacts with isolated line array or dense line array have long been used for calibration purposes. Thus efforts were spent to make a new design which can be used for making calibration standards.

Finally a design with dense grid of lines, with the horizontal lines intersecting the vertical lines at right angle was considered (figure 3.1). This design incorporates the *linewidth* and the *pitch* measurements, thereby serving the requirements of a calibration artifact. *Linewidth* is the size of an individual structure along a particular axis, while *Pitch* is the measurement of the separation between the same positions on two or more nearly identical structures [36]. A close dense array facilitates simultaneous pitch measurements in both the X and Y direction. Since the artifact has known dimensions it can be used to evaluate the performance of a CD-SEM under different conditions.

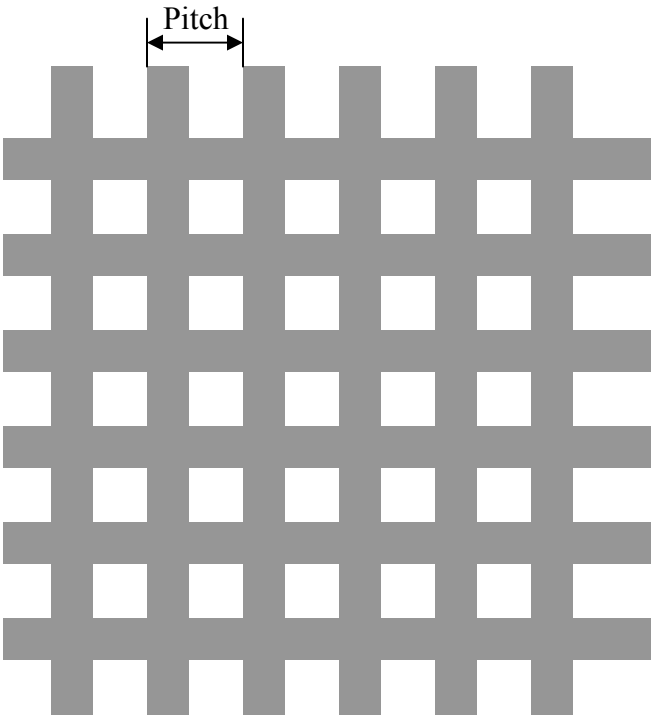


Figure 3.1: Schematic design of dense array of lines.

3.1.2 Designing of the artifact

The initial designing of the artifact was carried out using L-Edit®, layout editor software distributed by Tanner Research Inc. The design saved in the GDSII format is further transferred into the format acceptable by the lithography tool, JEOL 6000 FS/E. As the dimension of the artifact started decreasing from the micron level to sub 100nm region, the designing of the artifact was done using the functions available in the lithography tool – JEOL 6000 FS/E. The design is in JEOL01 data format, which is recognized by the lithography tool. The JEOL01 format is user friendly and provides a high accuracy in dimension control of the artifact design. It involves the use of pre defined commands which define the shape and dimensions of the required pattern. While designing the artifact, parameters like the role of proximity effect, electron exposure dose and the tone of the resist were considered.

The proximity effect caused by the backscattered electrons causes exposure away from the incident area. The proximity effect deteriorates the pattern definition, especially seen in dense array of lines. In most cases, the lines become wider than designed, while in worst cases they might merge. To avoid this problem, there are some proximity correction software's like PYRAMID, PROXECCO which basically deals with dose modulation to decreases the effect. In absence of any software, proximity effect can be corrected by shape modulation. While designing the pattern, shape modulation was extensively used to obtain the desired design dimensions after exposure and development. This involves changing the pattern design at strategic positions, and writing the patterns together or separately depending upon the final dimensions of the pattern required (figure 3.2).

Figure 3.2: Proximity correction based on shape modulation [37]

The strategic locations which have been designed to accommodate the distortion due to proximity effect are given exposure dose different compared to the rest of the pattern. Exposure dose is the amount of energy provided by the lithography system for exposure purposes on any substrate. The dose is calculated on per unit area basis, and given in terms of $\mu C/cm^2$. Higher energy dose helps in fabricating fine feature size, but in turn increases the number of backscattered electrons. This increases the proximity effect, causing distortion of the pattern shape. Also the type of the resist used influence the proximity effect. In positive resists the proximity effect tends to increase the linewidth, which has to be accounted for while designing the artifact.

The amount of the electron dose used for exposure depends on the type of the resist used. Positive resists like PMMA and negative resists like HSQ have different dose requirement for pattern exposure. In general, positive resists have low dose requirements compared to the negative resists. Also the chemistry involved in the developer-resist also influences the pattern designing, positive resist tend to dissolve in the developer faster compared to the negative resist. Hence, while designing the patterns the type of the resist to be used for coating the wafers is an important parameter. Since the post development profile for the positive resist is opposite to that of the negative resist, the design for the pattern used for both the resist has to be different.

3.2 Fabrication of the artifact

After designing the artifact with either using the L-EDIT® or the built in designing software of the lithography system, the fabrication of the artifact is the next important step. There are number of parameters to be considered for fabrication, mainly the tone of the electron beam resist used, the thickness of the resist and the development conditions

for the resist of interest. Besides the parameters concerning the resist used, the fabrication of the artifact is strongly influenced by the room temperature of the lithography system. Room temperature is an important parameter, since it affects the beam diameter. High room temperature causes broadening of the electron beam, which in turn affects the resolution of the writing. Broadening of the electron beam also increases the proximity effect, which adversely affects the artifact structure in the sub-100 nm region. Moreover, the developing conditions like the temperature of the developer, the developing time and the developer concentration also affects the final results of the fabrication.

Fabrication of the artifact has been done in negative resist-HSQ and the positive resist-PMMA, with primary focus on fabrication in the negative resist. Irrespective of the tone of the resist, fabrication is done at 50 kV using the electron beam lithography tool – JBX 6000 FS/E. The resolution of the lithography tool is around 5nm while using a current of 100pA. The movement of the stage in lithography tool is controlled by Laser Beam Control (LBC) to 0.62 nm, thereby ensuring a very high precision writing during the exposure of the substrate. It also ensures repeatability of structures with no/negligible deviation in the position of the artifact.

3.2.1 Fabrication in positive resist - PMMA

Polymethyl Methacrylate (PMMA) used for the research purposes is procured from MicroChem Inc. During the course of the research work, PMMA with molecular weight of 495k and 950k has been used. The molecular weight is an important aspect while considering the positive tone resist-PMMA. High molecular weight resists needs more development time compared to low molecular weight resists. PMMA grades of 5% and

11% are commercially available from MicroChem Inc. Dilution of these grades was achieved using Anisole, manufactured by MicroChem Inc. PMMA grades ranging from 2% to 11% have been used for the research activities.

The spin curves for PMMA gives a relation between the spinning speed and the grade of PMMA to be used. As a general rule, higher is the spinning speed thinner is the resist layer on the substrate. Also using a low grade of PMMA gives thinner resist layer on the substrate. Initial work for the artifact was carried out for 500 nm pitch, and with linewidth of 100nm on a silicon substrate. Spinning the silicon wafer with PMMA (5%) at speeds of 4000 rpm for 60 seconds yielded thickness of the order of 250 nm. Spinning of the resist was followed by baking of the resist. Baking at 180°C cures the resist, which in turn strengthen the bonding in the PMMA resist. After few experimental run, the resist sensitivity was determined to be in the range of 320-550 $\mu C/cm^2$. The exposure in the lithography tool was carried out at 50 kV using 100 pA current. At this current, the diameter of the electron beam is of the order of 5 nm. The selection of the current was due to the small beam diameter. Though the time required to write the artifact is long, a right amount of the exposure can be maintained. The exposure of the resist is followed by an important step of developing of the resist. Development of the resist is carried out in a mixture of MIBK:IPA 1:3 for 90 sec, followed by rinsing in IPA for 40 sec to remove the exposed part of the resist. Figure 3.3 shows the SEM image for 500nm pitch artifact.

The calibration artifact was imaged using a scanning electron microscope – LEO® 1525, Carl Zeiss, Thornwood, NY. The Leo 1525 workstation utilizes Gemini field emission column. The imaging was done by Inlens detector and secondary electron detector (SE2).

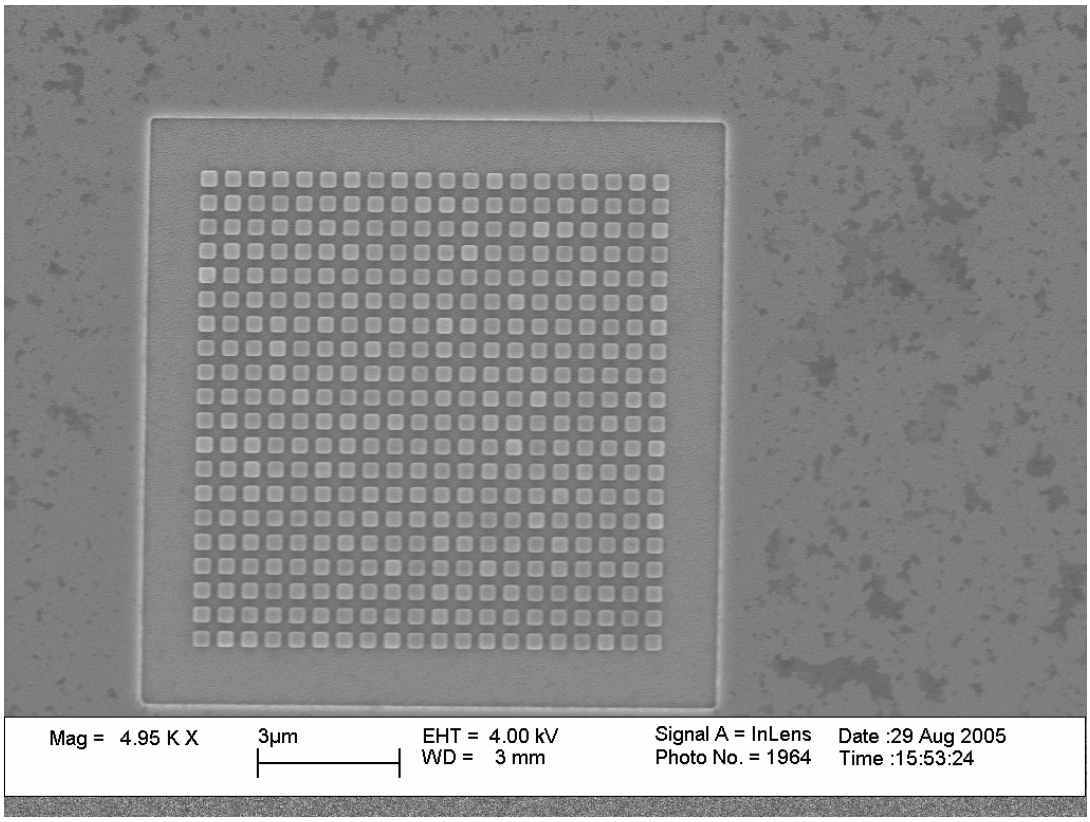


Figure 3.3: SEM micrograph of 500 nm pitch artifact in PMMA

Following parameters were used while imaging:

Working distance = 2-3 mm

Applied voltage = 12-15 kV

Detector = InLens

Magnification = Typically 45 kX – 70 kX

Scanning speed = 5

For carrying out SEM (Figure 3.4) the samples were gold coated. SPI® sputter coater was used for this purpose. The substrate is placed face up on the holder. After placing the glass chamber on top, the coating process begins. The argon pressure is 2 psi, and the current passing through the plasma is 20 mA and time required to coat sufficient amount of gold is on the order 10 seconds. Typically coating thickness depends on cleanliness of sputtering system. The thickness of gold coating is calculated using the following formula:

d = K*i*V*t

where,

d = Thickness of gold coating,

K = Constant for argon plasma system and equals 0.17

i = Plasma current

V = Applied voltage

t = Time in seconds

Figure 3.4: LEO® 1525 FEG SEM, Carl Zeiss, Thornwood, NY

As the size of the artifact is reduced the denser the artifact becomes, and more is the proximity effect. This effect is responsible for changes in the dimensions of the artifact, causing deterioration in the line edges. To achieve accurate pattern definition, it is necessary to apply some method of exposure distribution to compensate for proximity effect. Normally, there are two methods which are used to compensate the proximity effect- Dose modulation or Shape modulation. Dose modulation can be done with the help of software's like PROXECCO, PYRAMID. Dose modulation involves changing the exposure dose on pixel basis, which gives far better results compared to shape modulation. The biggest drawback of this technique is the time consuming computational steps involved for calculating the dose.

In absence of any dose modulation proximity correction software, shape modulation helps in sustaining the proximity effect. Shape modulation involves changing the shape of the artifact at strategic locations, wherein the distortion in the shape due to electron beam exposure would be high. Normally at sharp edges or corners the energy deposition is high compared to other areas in the pattern. Thus, the proximity effect at the edges is higher than other area of the pattern. To compensate the proximity effect, shape modulation at the edges and corners are carried out. The pattern is designed smaller than the actual dimensions required. Also the corners of the patterns are carved in to accommodate the increase in the exposed area due to proximity effect. Figure 3.5 shows the pattern design modification to accommodate shape modulation. Figure 3.6 shows SEM micrograph for 150 nm pitch artifact.

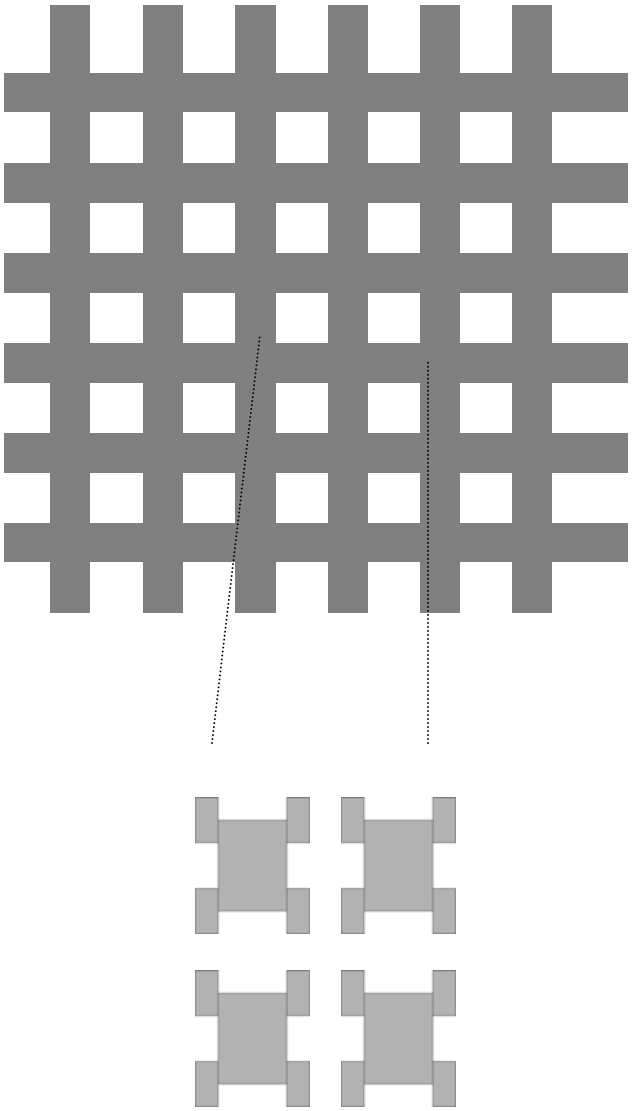


Figure 3.5: Schematic representation of shape modulation for proximity correction

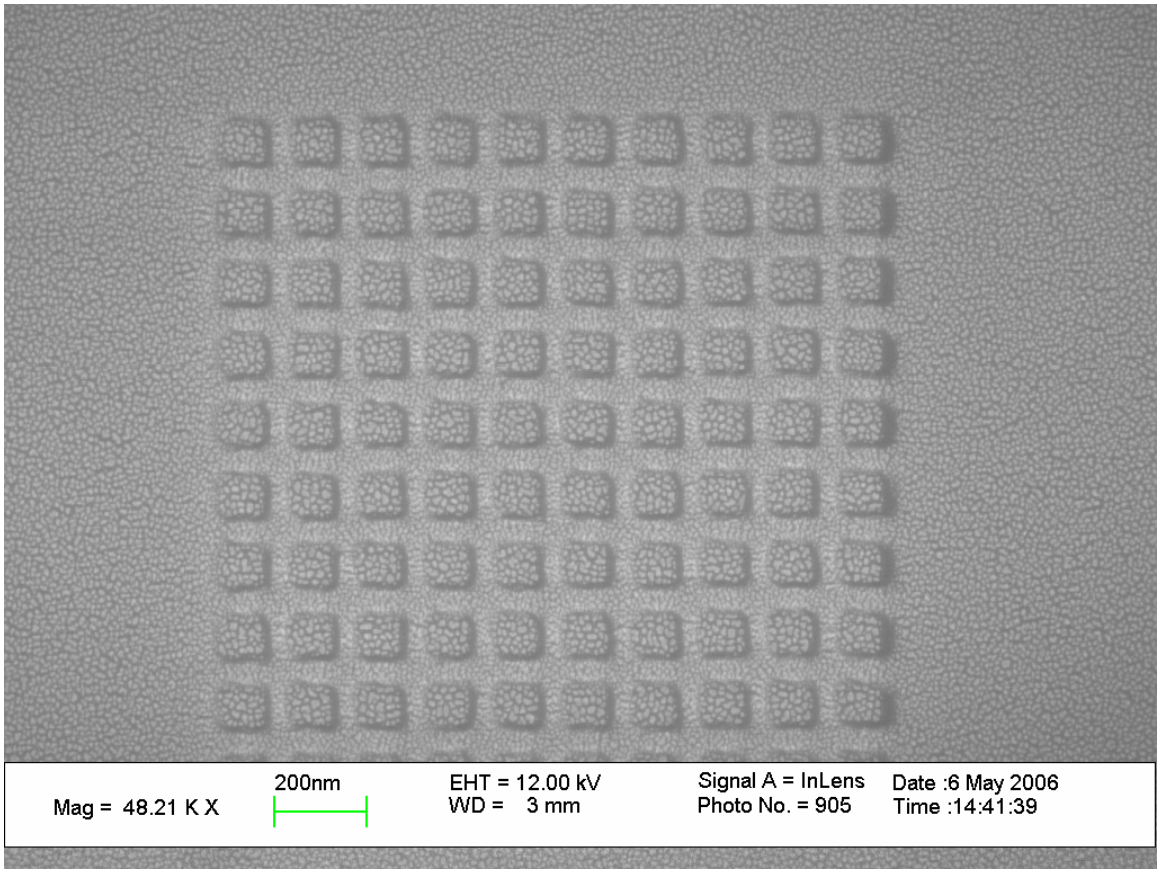
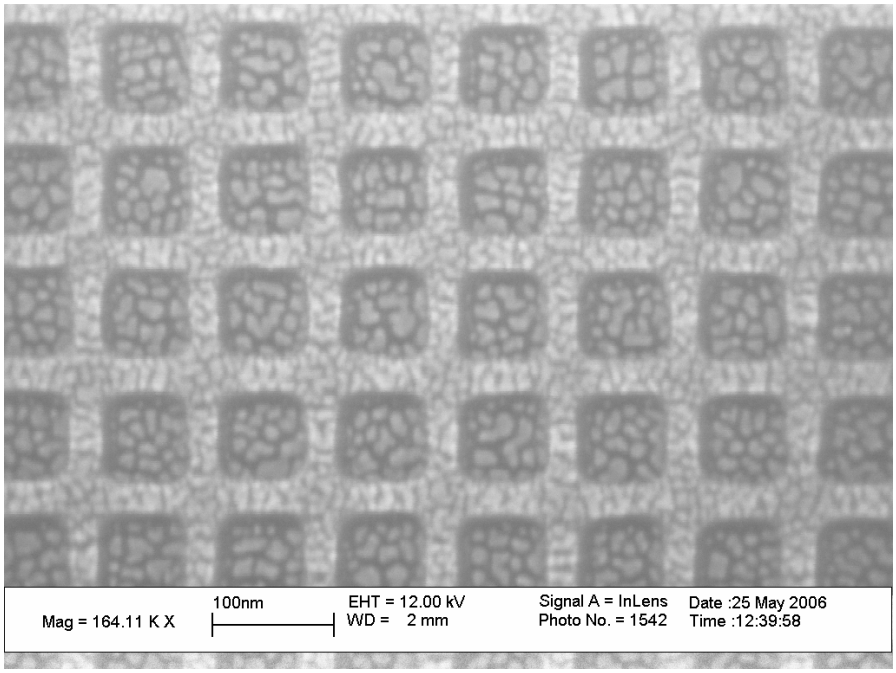


Figure 3.6: SEM micrograph of 150 nm pitch artifact in PMMA.

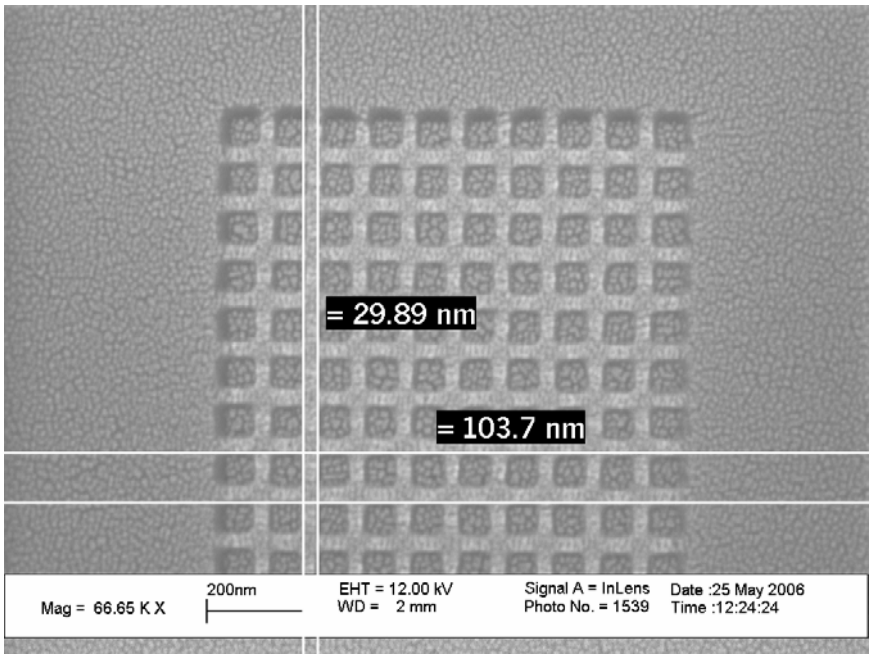
The positive resist PMMA being polymeric in nature it is susceptible to charging effects, thereby causing distortion while imaging. To overcome this charging effect, silicon substrates were coated with 99.999% gold (Au) using a physical vapor deposition (PVD) chamber from Cooke Vacuum Products, Inc. [43] The substrates were mounted 25 cm above and normal to the effusive source. Average mass thickness and deposition rates were monitored for each film using a water-cooled quartz crystal microbalance (QCM, from Maxtek, Inc.) mounted adjacent to the arrays. Deposition rates were calculated based on the mass density of the metal and its acoustic impedance. Nominal metal thickness and deposition rate were 5nm and 0.2 Å/sec, respectively [43].

When depositing onto polymer, the metallic nanoparticles are dispersed within the dielectric material. During the process of physical vapor deposition a vacuum of ~10^{-6} Torr is created around the inverted elastomer slab, deposition is carried out by resistively heating a tungsten boat containing 99.9% pure gold metal to approximately 250°C. The potential to be applied across the tungsten boat, the rate of deposition and particle size are determined based on energetics of the metal nanoparticles both in the sublimed plume as well as upon immediate entry into the elastomer surface [43]. The primary function of the thin gold film is to increase the surface electrical conductivity of the substrate, with additional attributes of increasing the thermal conductivity and sometime the secondary electrons (SE) and the back scattered electrons (BSE) signal from the substrate [17].

With the ultimate goal of sub-100nm artifact in sight, the design was further modified to accommodate 100nm pitch artifact in both X and Y direction. Figure 3.7 shows the SEM micrograph for sub 100nm artifact.



(A)



(B)

Figure 3.7: (A) SEM micrograph for 100nm pitch artifact (B) Sub-100nm artifact in PMMA

As the feature sizes decreases, the amount of exposure dose required increases. For the fabrication of 150 nm pitch artifact, electron exposure dose was in the range of 450 – 500 $\mu C/cm^2$. The development was carried out in MIBK:IPA 1:3 for around 60 sec, followed by rinsing in IPA for around 45 sec. For sub 100 nm artifact, still higher exposure dose of the order of 520 – 580 $\mu C/cm^2$ is required to fabricate the structures. The development system is kept same as the one used for 150 nm artifact. The dimensional control for artifact in PMMA is a big problem. Being a positive resist, PMMA tends to swell on development in MIBK:IPA 1:3 causing change in the dimension of the artifact. Inspite of the shape modulation incorporated into the design, the corners of the artifact tend to round off instead of sharp edges. The thin gold layer used for overcoming the charging effect, tend to increase the linewidth to some extent. Though the increment in the dimensions of the linewidth is in nanometer, it is substantial while thinking of accuracy of the artifact.

3.2.2 Fabrication in negative resist - HSQ

In quest of higher accuracies in the dimensions of the artifact, different electron beam resist were evaluated for fabrication of the artifact. Of all the resist, negative resist-hydrogen silsesquioxane (HSQ) showed some promising results. HSQ has very high resolution with moderate sensitivity, good etch resistivity, minimum line edge roughness [29] and highly stable under scanning electron microscope. HSQ used for research activities has been procured from Dow Corning Co. HSQ is commercially available as Flowable Oxide (FOx) in grades of FOx - 12, FOx – 14, Fox – 16. For research purposes, Fox-14 maintained at temperatures of 19°C - 22°C has been extensively used. Compared

to positive resist, HSQ needs a very high exposure dose for fabricating sub-100 nm features.

HSQ is highly sensitive to spinning conditions. Any change in temperature or the humidity level in the preparation room affects the thickness of HSQ. Efforts have been made to keep the thickness of the resist constant as much as possible over the course of the research. To achieve the constancy in the thickness of the resist, parameters like the spinning speed, the acceleration provided for spinning the chuck and the baking time and temperature had to been changed. Over the course of three months (July – Sept 2006), the variations in the thickness of the resist with the temperature were studied (Table 3.1).

The thickness of the resist is an area of concern on account of its effect on the exposure and development conditions in the later stage. And since the developing conditions are also temperature dependant, the final dimensions of the calibration artifact are affected.

Table 3.1: Thickness variation of the resist with temperature.

Date	**Temperature**	**Thickness (nm)**
19-Jul	21.9	52.6
25-Jul	21.4	53.05
8-Aug	20.9	51.54
	20.9	50.73
11-Aug	19.9	48.5
	19.9	50.5
14-Aug	19	49.6
18-Aug	19.4	49.83
	19.4	50.13
31-Aug	21.4	58.14
1-Sep	19.4	50.58
	19.4	51.28
	21.4	58.05
5-Sep	22.8	57.05
11-Sep	18.9	58.15
	18.9	58.33

The negative resist – FOx 14 consist of methyl isobutyl ketone (>60%) and hydrogen silsesquioxane (10%-30%) and toluene (< 1%) [44]. Different grades of HSQ were evaluated, and spin curves for the resist were developed. For optimum results, FOx 14 was considered to be the right candidate for our research activities. The negative resist HSQ is further diluted with methyl isobutyl ketone (Dow Corning) in the ratio of 1:4. This mixture of HSQ:MIBK (1:4) is maintained at a temperature of 19 – 20°C in a refrigerator, and removed couple of hours before spinning process. HSQ is highly viscous liquid, hence requires no acceleration for spinning. At a temperature of 19°C, spinning speeds in the range of 4500 – 5000 rpm gives a resist thickness of around 51 nm. But with change in temperature, the spinning speeds have to be varied to maintain the thickness.

The thickness of the resist was measured using Filmetrics Thin-Film Analyze F 20. The F20 measures thin-film characteristics by either reflecting or transmitting light through the sample, and then analyzing this light over a range of wavelengths. Because of its wave-like properties, light reflected from the top and bottom interfaces of a thin-film can be in phase so that reflections add, and in- or out-phase depends on the wavelength of the light, as well as the thickness and properties of the film. The result is characteristic intensity oscillations in the reflectance spectrum. In general, the thicker the film the more oscillations there are in a given wavelength range. The amplitude of the oscillations is determined by the refractive index and extinction coefficient of the films and substrate. Therefore, by analyzing the period and amplitude of these oscillations, the F20 can determine thickness and optical properties (n and k) of multiple thin films. Spinning of HSQ is followed by baking the resist to initiate the transformation of cage like structure

to network like structure [29]. The baking temperature affects the sensitivity and the contrast of the resist. Generally, higher baking temperature improves the sensitivity of the resist, but decreases the contrast of the resist. Unlike the positive resist, the baking process for HSQ is a two step process. First the substrate is heated at a low temperature, followed by heating at high temperature.

The as-spun HSQ resist have mixed structure consisting of cages/network with cages in dominance [29]. During the thermal process, a bond scission and recombination leads to the transition to the network structure. As the baking temperature is increased, the amount of hydrogen diffusing out increases [29]. The incomplete recombination of the Si-O and Si-H bonds gives out many free Si bonds, which gives imperfection in the thin film. The baking temperature determines the cage/network ratio, the amount of hydrogen content in the film. Generally in presence of oxygen the Si-H bonds breaks leading to the formation of the network like structure [29].

For research purposes, the baking temperatures were kept in range of 120°C – 200°C. For calibration artifact with a pitch of 150 nm, baking recipe had a combination of 120°C for 2 minutes, followed by 200°C for 2 minutes. At temperature of about 19°C, a thickness of the order of 50 nm was obtained. As the size of the artifact decreased, new baking recipes were developed. Optimum results were obtained using a combination of baking at 120°C for 2 min followed by baking at 180°C for 2 min. At the same room temperature it was found that the thickness of the resist increases, with increase in the development rate. Thus there is increase in the contrast of the resist, thereby giving clear line edge definition. Baking of the substrates was followed by exposure using the lithography tool .

The durability of the HSQ film after spinning and baking is for short period of time. Hence, to get optimum results the substrates with HSQ spun on it have to be exposed by the electron beam as early as possible. For the research purposes, a two hour time period between spinning/baking and exposure was consistently maintained. Since HSQ has to be maintained in a temperature range of 19°C to 22°C, it has to be kept in a refrigerator. The resist is removed from the refrigerator and placed at room temperature for two hours before it can be spun on the wafer. The wafers after spinning are kept in the sample chamber of the lithography tool for sometime. As with the positive resist, many trial runs were carried out to determine the exposure range for HSQ resist. Being a negative resist exposed part remains on the substrate, while the unexposed part is washed away after development. On account of this nature of the negative resist, substantially a high exposure dose is required for fabricating artifact in the resist.

As the size of the calibration artifact decreased from micrometer level to the nanometer level, proximity effect became an area of grave concern. All the proximity corrections were shape modulation based. After number of designing variations, a final proximity correction design was considered for the calibration artifact.

For calibration artifact with pitch of 150 nm and artifacts with 100 nm pitch, the dimensions of the artifacts were less than the actual ones desired. These changes in the dimensions of the artifact were made to accommodate the increases in the linewidth on account of proximity effect. To further ensure dimensional control of the artifact, the vertical lines were separated from the horizontal ones at the point of junction (figure 3.8). This ensured that the corners of the junction had clear line definition and were not rounded.

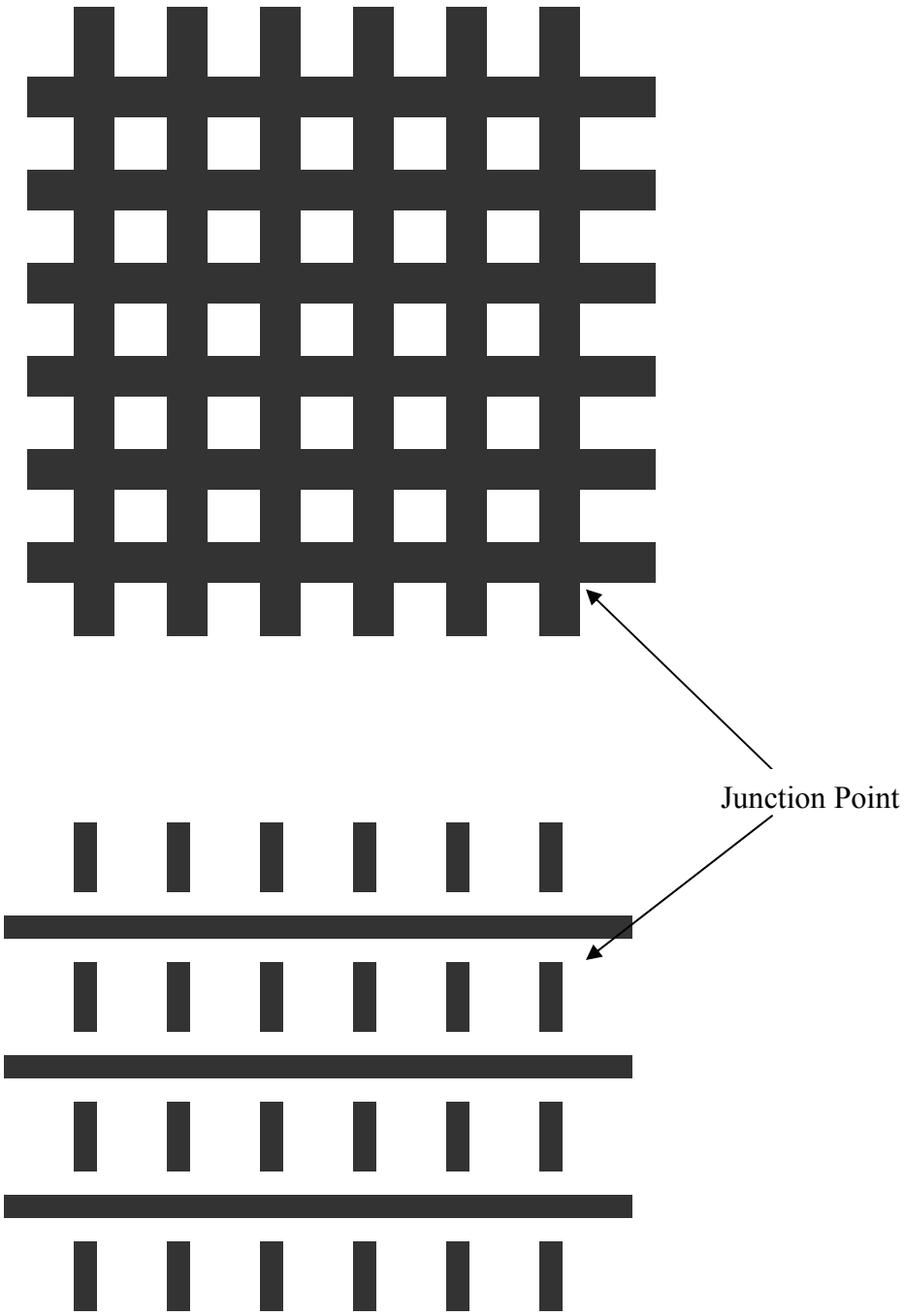


Figure 3.8: Schematic representation incorporating the proximity corrections into the design of the artifact.

The exposure on the wafers was carried out using electron beam lithography tool – JBX 6000 FS/E. A wide range of exposure doses were used to get the final shape of the artifact. Initial experiments were done at exposure dose of 520Cμ/cm^2 – 780μC/cm^2. The artifact as observed under a SEM didn't give good results (figure 3.9). The linewidth of the artifact was more than the specified dimensions and there was no clear edge definition. It is well established fact that increasing the exposure dose helps in fabricating small feature sizes. With that in mind, the exposure dose was further increased to a range of 800Cμ/cm^2 – 1200μC/cm^2. SEM imaging showed improvement in the line edge definition, but with rounding of the junction corners (figure 3.10).

With the goal set to sub – 100 nm region, new artifact designing was needed. The role of proximity effect was a big problem, which was taken care by proximity correction in the design of the artifact. The artifact has 100nm pitch, with a linewidth of 40nm. The artifact was designed with dimensions of the linewidth less than 40 nm, to compensate for increment in the dimensions by the proximity effect. The horizontal and the vertical lines were separated at the junction where they met. This helped in sharp corners of the junction.

The determination of the exposure dose for the sub – 100 nm region artifact was a big challenge. Initially, the exposure dose was given in the range of 1300Cμ/cm^2 – 1400μC/cm^2(figure 3.11). After some more experiments, it was found out that the exposure dose required is pretty high than the one previously used. The exposure dose for sub 100nm region is in the range of 1490Cμ/cm^2 – 1530μC/cm^2 (figure 3.12). The calibration artifact was exposed to these dose ranges as a whole. The exposure dose was same for both the horizontal and vertical lines.

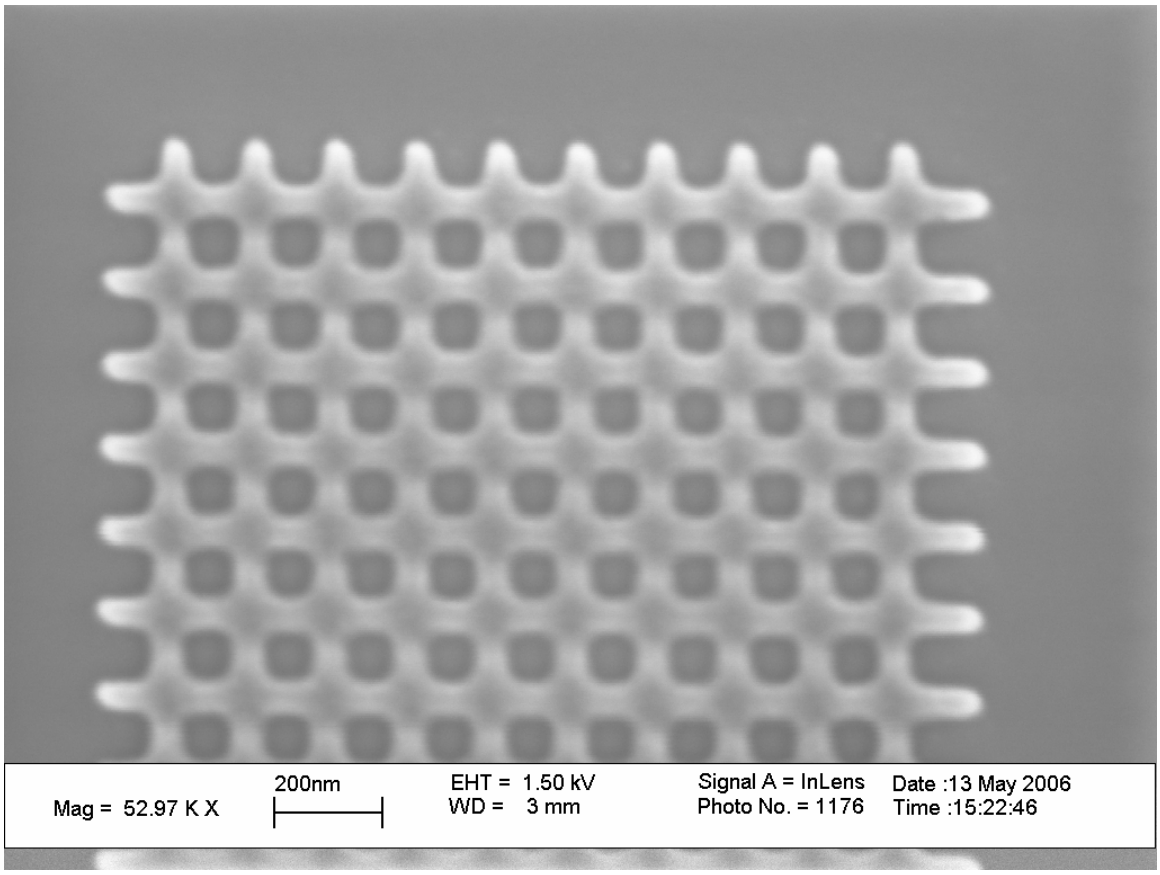


Figure 3.9: Calibration artifact with a pitch of 150 nm, and with dose in the range of $520\mu C/cm^2 - 780\mu C/cm^2$.

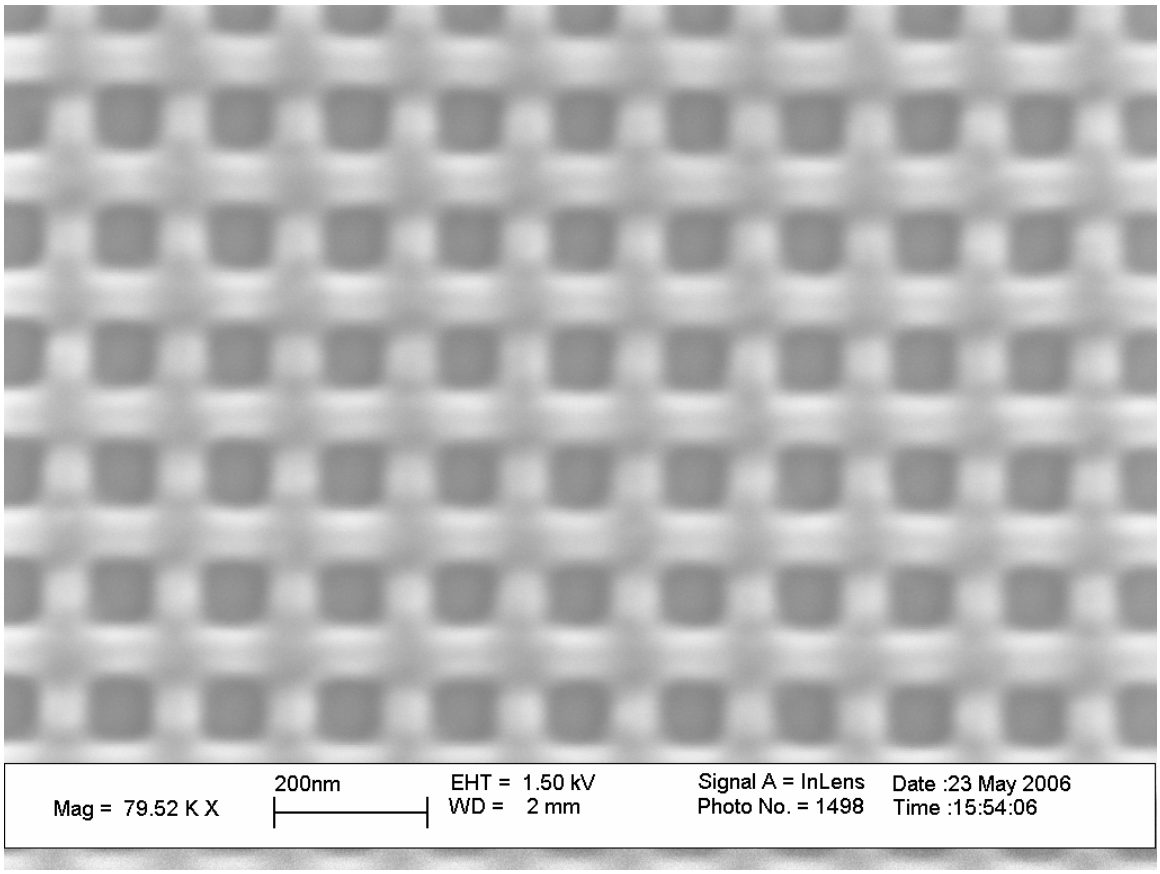


Figure 3.10: Calibration artifact with a pitch of 150 nm, and with dose in the range of $800\mu C/cm^2 - 1200\mu C/cm^2$.

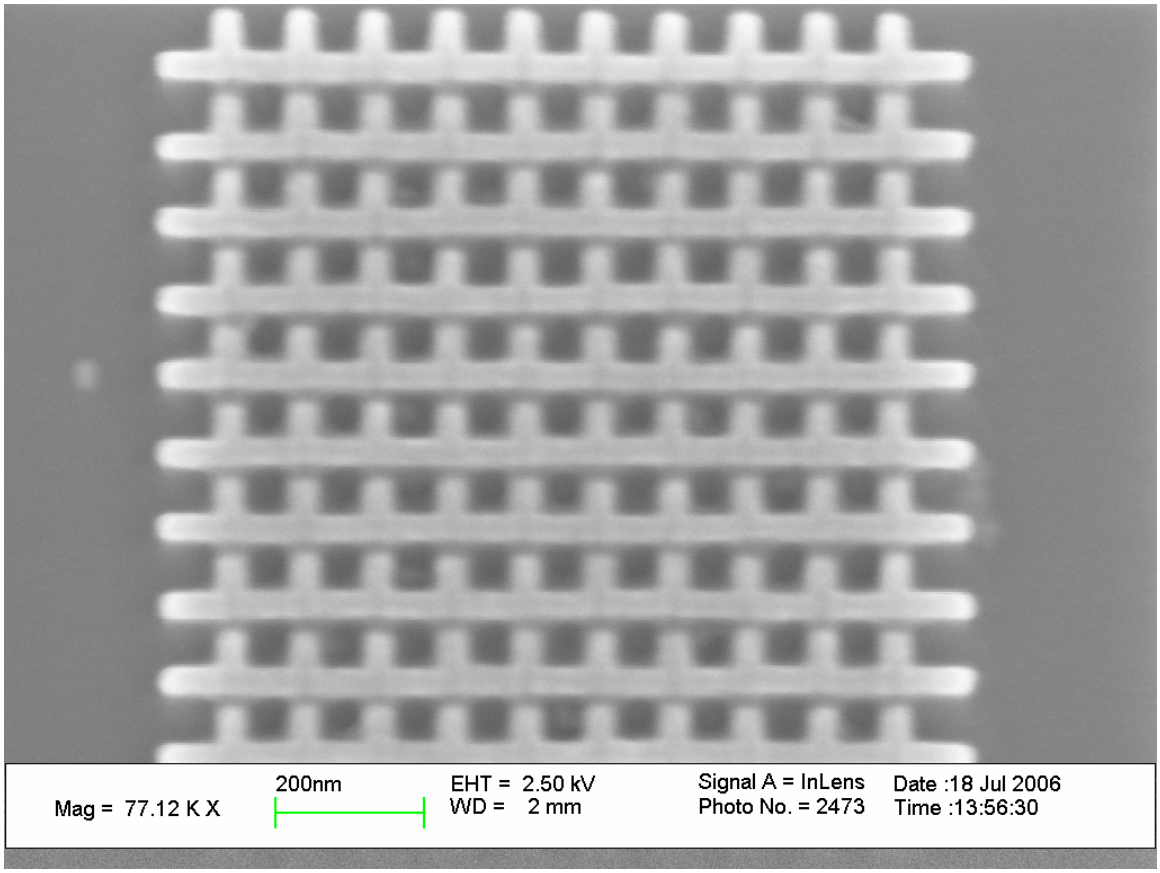


Figure 3.11: Calibration artifact with a pitch of 100 nm, and with dose in the range of 1300Cμ/cm^2 – 1400μC/cm^2.

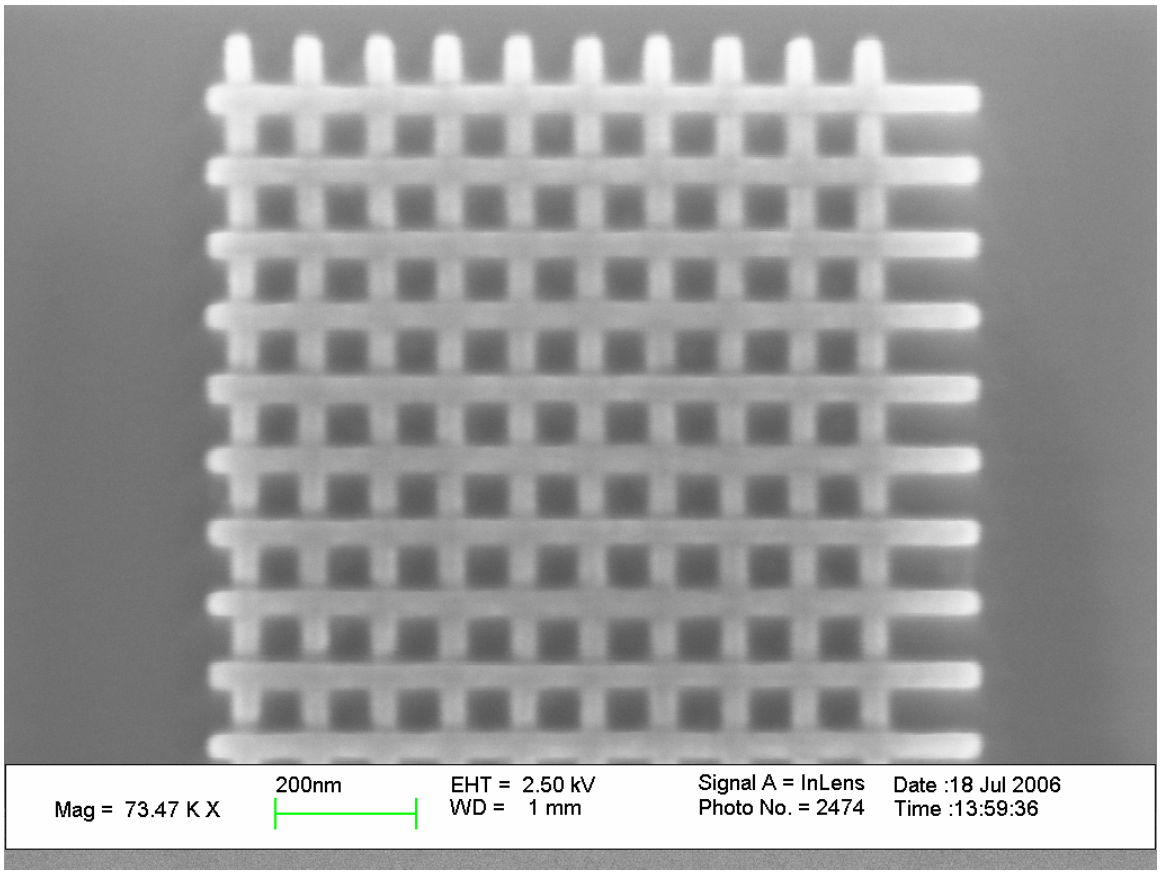


Figure 3.12: Calibration artifact with a pitch of 100 nm, and with dose of 1490 μC/cm^2.

There were further changes in the designing of the artifact to get clear edge definition, and no rounding of the corners. One such change was dividing the pattern into two different units. One unit consisted of only the horizontal lines, while the other unit consisted of only the vertical lines. Over the course of the research, it was figured out that horizontal lines with more surface area than the vertical lines had more problems with the proximity effect. With the same exposure dose for both lines, the horizontal lines tend to increase in its dimensions. To overcome this problem, the lines were given different exposure dose, with the dose for the horizontal lines lesser than the dose given for the vertical lines (figure 3.13). Also, the dimensions of both lines were smaller than the actual dimensions, thereby facilitating accurate dimensions of the artifact and low edge roughness. During exposure, the two units were later on joined through the inbuilt command in the lithography tool.

After the exposure part is completed, the substrate were subjected to development, this process is highly critical, and heavily depends on the temperature of the developer. The development was carried out in 0.26N Tetramethyl Ammonium Hydroxide (TMAH), followed by TMAH:DI 1:9 and finally rinsing in DI water (figure 3.14 and figure 3.15). It has been suggested by Namatsu et al. dissolution in TMAH is by bond scission, wherein the unexposed part is completely removed from the substrate surface [29]. While, in the exposed part of the resist, the dissolution rate is pretty slow. On account of this, the stable three dimensional network like structure initiated by the exposure for HSQ is obtained [29]. Moreover, it is important to have optimum development conditions, since they also affect the surface and line edge roughness of the artifact.

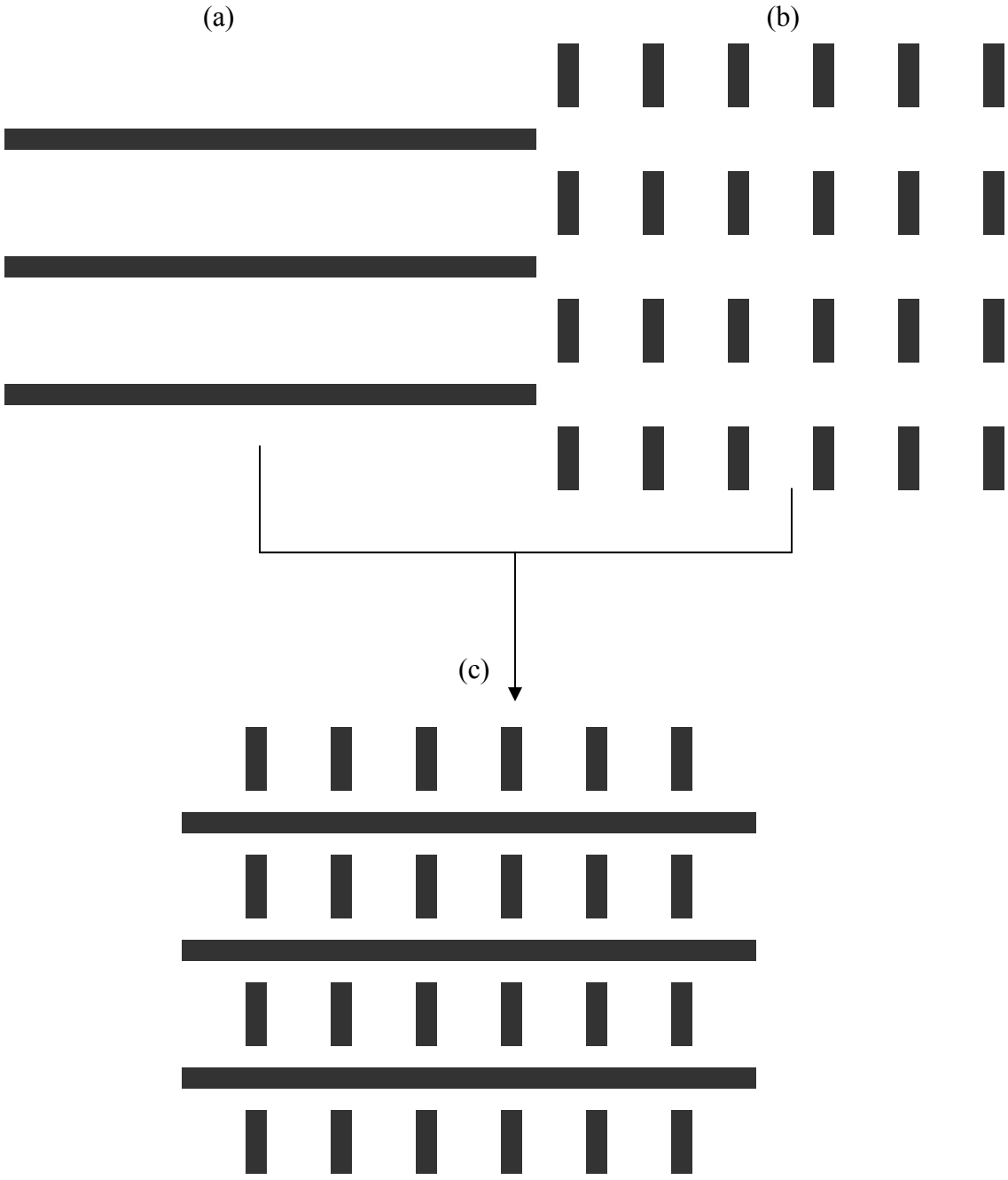


Figure 3.13: Schematic representation of (a) First unit with horizontal lines (b) Second unit with vertical lines and (c) the units combined to form the design of the artifact.

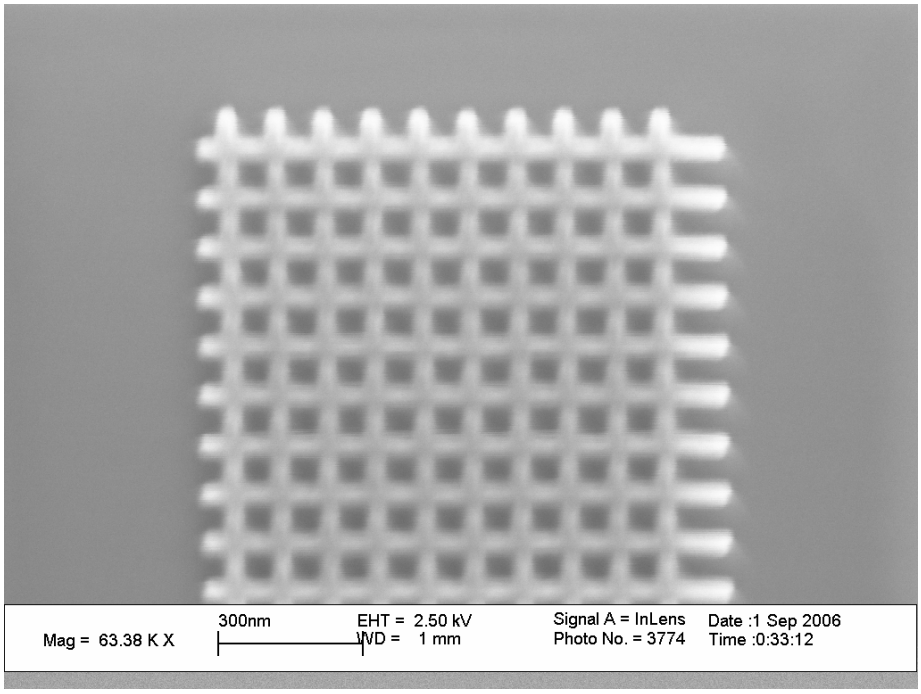


Figure 3.14: Calibration artifact with pitch of 100 nm and with the dose different for the horizontal and vertical lines.

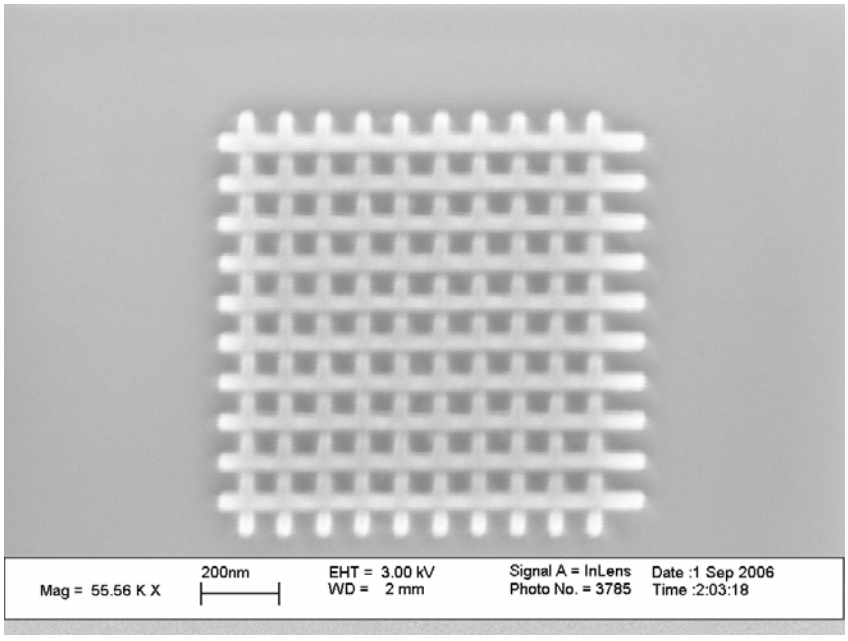


Figure 3.15: Calibration artifact with pitch of 100 nm and with different doses.

There are two main hypotheses for the development of the negative resist. One of the hypothesis states that the development process can be divided into two processes: (i) dissolution of single polymer and (ii) removal of polymer aggregates [45]. The development process is schematically shown in figure 3.16 [45]. The polymers in aggregate are packed densely compared to single polymer [Fig. 3.16 (a)]. When the resist is subjected to the development process, the dissolution rate for the single polymer in the unexposed region is very high resulting into easy rinsing of the unexposed part [Fig. 3.16 (b)]. While in the exposed part, the polymer aggregate are highly dense resulting into less development rate [Fig. 3.16 (c)].

The polymer aggregates which are not removed by the developer solution remain on the sidewalls of the exposed part, which in turn causes line edge roughness. On account of the development process, there is some amount of swelling in the exposed part and can be a cause of the line and surface roughness. This swelling behavior can be reduced by using optimum developer-system.

The swelling behavior is also dependant on the development time. Longer development time increases the output of more polymer aggregates since higher liquid has to flow out. Moreover, the sensitivity of the resist also determines the development time. A higher sensitivity enables shorter development time, hence less swelling [45].

After development of the substrate, they are blown dried by ultra high purity grade nitrogen. Efforts have been made to optimize this resist drying process, with research carried out for some new kind of drying system. Daniel Kupper et al [45] have made significant progress in an alternative drying system. They are concentrating on the use of CO_2 gas in air tight process chamber [45].

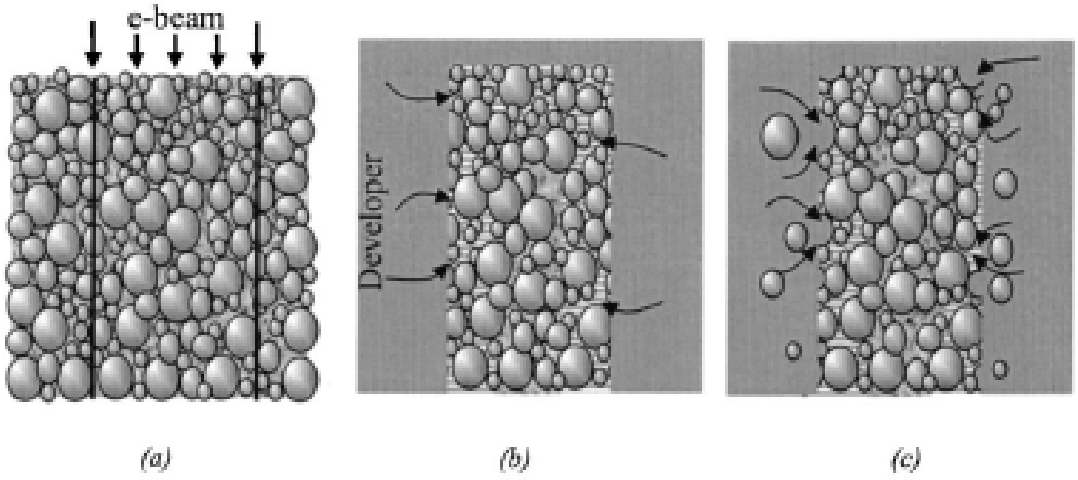


Figure 3.16: Schematic diagram of a development process of a negative tone resist including (a) exposure, (b) development and (c) polymer aggregate extraction (PAB) [45].

Development of the substrate was followed by imaging in LEO 1525 FEG SEM. The negative resist (HSQ) is stable under the secondary electron imaging. On account of this stability, there is no need for any kind of metallic coating. Some of the SEM conditions for imaging the HSQ resist:

Detector: InLens – SE detector

Working distance = 2-3 mm

Applied voltage = 2.00 – 3.00 kV

Magnification = Typically 45KX – 70KX

Scanning speed = 5

To get some measurement for the artifact fabricated on the HSQ resist, pitch measurements were done using the "Measure" software provided by the Spectel Research Corp. [46]. A SEM micrograph (Figure 3.17) has been selected for the measurement purposes. The software uses two algorithms to calculate the linewidth and the pitch measurements. It uses both the threshold method and regression to baseline method. Both these algorithms give out measurements close to 100 nm in pitch. The software gives out a line profile for the artifact (Figure 3.18) and the calculation made by the "Measure" software using both the algorithms (Table 3.2). Another interesting part of these results is the line edge roughness. The values are well below the values set by the semiconductor industry. This low value facilitates an accurate measurement of the linewidth and pitch. Moreover, it indicates a fairly good optimization of all the main processing steps like resist spinning, baking of the resist, exposure by the lithography tool and the development of the resist after exposure

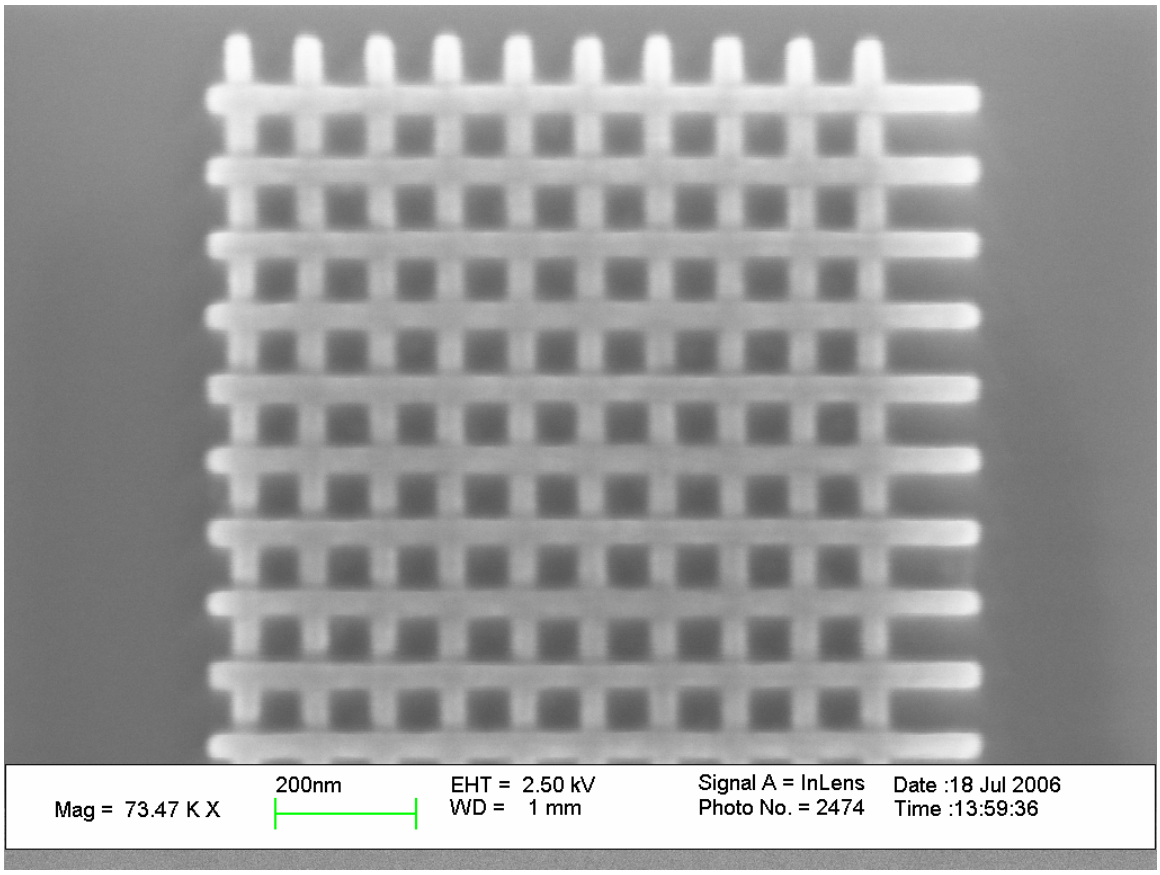


Figure 3.17: SEM micrograph used for "Measure" software, Spectel Research Corporation.

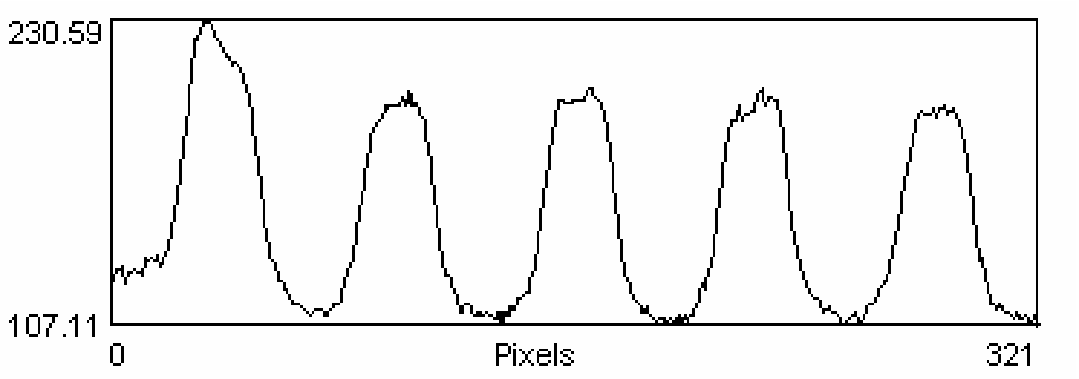


Figure 3.18: Measurements done using "Measure" software, Spectel Research Corp.

Table 3.2: Line width and line edge roughness measurements.

Algorithm	**Width (nm)**	**Roughness (nm)**
Threshold	99.58	0.31
Regression	101.73	0.63

Efforts are being made to have measurement of the artifact by lattice fringe counting of silicon. This technique involves thinning of the silicon substrate in the area of the interest, followed by observation under a high resolution TEM. The lattice fringes of silicon are of the order of 0.3 nm, hence making the task even more difficult. Alternatively, measurements using Optical / X-Ray Scatterometry are also being evaluated.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Results

All the metrology tools, in some way have certain areas of concern which are either unknown or overlooked by the users. On the same line, the magnification calibration of the CD-SEMs is a major area of concern. We understood the issues related with the magnification calibration of the CD-SEMs, and decided to address it as the main goal of our research project. CD-SEMs have long been the workhorse for metrology in the semiconductor industries. They can be operated at very low voltages, and with resolution of the order of 3nm. Also, they are best suited for the current 300mm wafers and for the future 450mm wafers. Moreover, CD-SEMs gives lateral image of the features with detailed information, and have good throughput (~65wph). With all these advantages associated with CD-SEMs, any irregularity in the functioning of these machines becomes a major area of concern.

We have come a long way in terms of the goals set for the project – fabrication of a calibration artifact, suitable for the current technology node and also for future technology node. The artifact has a pitch of 100nm, which makes possible magnification calibration in both X and Y direction simultaneously. The calibration artifact fabricated has a very high contrast, with low edge roughness. The artifact is fabricated on silicon wafers, thus making it Fab friendly.

Also, the artifact is very stable under SEM, with negligible charging. With the fabrication of the artifacts a success story, our focus is more on making the artifact traceable to some national standard – NIST.

4.2 Discussion

One of the key aspects in making standards is following the guidelines/protocols set by some national or international organization. In the United States, the national organization of interest is National Institute of Standards and Technology (NIST), to which the artifact should be made traceable. Traceable standards are the ones whose physical dimensions can be traced down to some known values – like, wavelength of light. Many measurement techniques are being evaluated for making our calibration artifact a standard. Some of these measurement techniques are:

(1)Lattice fringe counting by STEM or TEM – which is difficult with 0.3nm fringes for silicon.

(2)Optical or X-Ray Scatterometry.

(3)Fabrication with a stage controlled by laser interferometer in the lithography tool, and a stationary beam.

Of all the techniques being evaluated, scatterometry looks like the best candidate for measurement. Since scatterometry involves the use of visible light for measurements, we feel it is best suited for the calibration artifacts. Moreover, scatterometry does measurements for a group of lines, which further reinforces the measurements. We are looking forward to have technological collaboration with the leading semiconductor industries for measurement by scatterometry.

CHAPTER 5

COMMERCIAL APPLICATIONS AND FUTURE WORK

5.1 Commercial Applications

At the inception of this research project, it was decided that the calibration artifact designed should have some commercial application. Some of the possible commercial applications are:

(1) Once traceability of the calibration artifact, they can be mass produced using Nanoimprint technology.

(2) Easy and faster evaluation of the magnification calibration of the CD-SEMs can be achieved.

(3) Easy tool matching can be achieved.

(4) Most important, a low cost traceable standard can be provided to everyone.

5.2 Future Work

With the vast possibilities in improving the magnification calibration in the CD-SEMs, new structures for the artifacts are being evaluated. Also, new resist technology is being evaluated. Fabrication work is currently being carried out for calibration artifacts with a pitch of 80nm.

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Vita

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