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PVT Compensation for Single-Slope Measurement Systems

Kevin Vun Kiat Tham

ktham@utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Kevin Vun Kiat Tham entitled "PVT Compensation for Single-Slope Measurement Systems." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Charles Britton, Jeremy Holleman

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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PVT Compensation for Single-Slope Measurement Systems

A Thesis Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Kevin Vun Kiat Tham
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Finally, I would like to thank my family and friends who have been very supportive while I completed my master's degree. I would especially like to thank my fiancée who has shown great understanding and patience with this work. Xiaonan has been my best friend and constant source of strength through this entire process.

ABSTRACT

A pulse-width locked loop (PWLL) circuit is reported that compensates for process, voltage, and temperature (PVT) variations of a linear ramp generator within a 12-bit multi-channel Wilkinson (single-slope integrating) Analog-to-Digital (ADC). This PWLL was designed and fabricated in a 0.5-[μ]m Silicon Germanium (SiGe) BiCMOS process. The PWLL architecture that is comprised of a phase detector, a charge-pump, and a pulse width modulator (PWM), is discussed along with the design details of the primary blocks. Simulation and silicon measurement data are shown that demonstrate a large improvement in the accuracy of the PVT-compensated ADC over the uncompensated ADC.

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CHAPTER I

INTRODUCTION AND MOTIVATION

1.1 INTRODUCTION

An analog-to-digital converter (ADC) is a key interface between measurement systems and the physical world. For space and avionic applications, circuits are required to operate over a wide temperature range. For the application targeted in this work, the ambient temperature on the lunar surface can range from −180°C to 125°C. Besides temperature variations, supply-voltage variations as well as process and device mismatch can also impact the accuracy of an ADC. A 12-bit Wilkinson ADC [1] with an input signal range of 0 to 1.2 V requires 300 µV of least-significant-bit (LSB) accuracy. The PWLL circuit developed in this work helps optimize the accuracy of this ADC over temperature.

1.2 BASIC OPERATION OF WILKINSON ADC

The basic operation of a 12-bit Wilkinson ADC requires a ramp voltage and a 12-bit counter. The ramp time is determined by the counter with a total of 4,096 clock cycles. This is illustrated in Figure 1. The peak of the ramp voltage is determined by the total amount of charging current to a capacitor within 4,096 clock cycles. A comparator in the ADC core compares the analog input signal to the ramp voltage. Once the ramp voltage is above analog input signal, the comparator "trips" and latches the bit count of the counter. Therefore the stability of the ramp is critical for the ADC's accuracy. In this context, ramp stability refers to the consistency in ramp slope, time duration, and peak value across many conversion cycles. Fortunately for crystal derived clocked systems (as in this work), time duration is accurate and robust. However, ramp slope and peak value must be addressed.
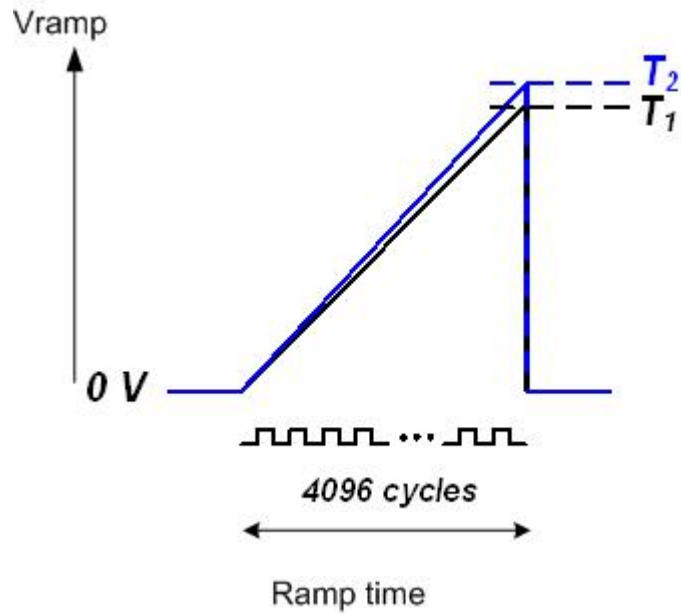
Figure 1. Ramp voltage relations with clock cycles

1.3 SOURCES OF INSTABILITY OF WILKINSON ADC

To provide the ability to maintain 12-bit accuracy over wider temperature range is a challenging task. The inaccuracy of the Wilkinson ADC is mainly due to the nature of the single slope measurement system that actually behaves as a ramp-time converter. The ramp can be generated through a circuit, as demonstrated in Figure 2, which is described by Equation (1), where dv is the ramp voltage range and dt is the ramp time duration.
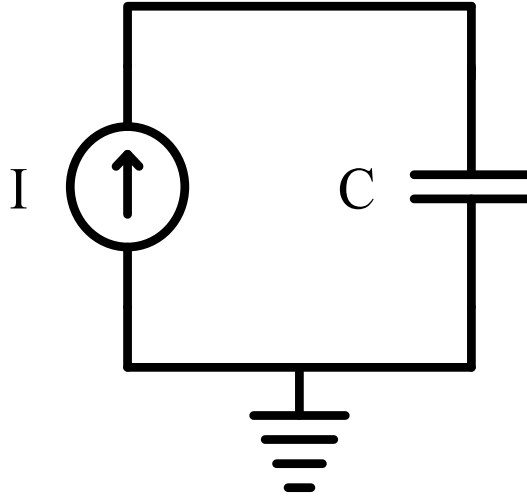
Figure 2. Simple ramp generator circuit

$$\frac{dv}{dt} = \frac{I}{C} \qquad (1)$$

The ramp slope (*dv/dt*) depends on the amount of current *I*, generated from a current source circuit charging the capacitor, *C*. PVT variations are one of the primary sources of slope instability. It should be obvious that in order to stabilize the slope, one must not stabilize *I* or *C* alone, but instead the ratio of *I* to *C*.

The architecture of the multi-channel Wilkinson ADC [2] is shown in Figure 3. The ADC consists of a ramp generator, a Gray code counter, and auto-zeroing comparators (one per channel). The accuracy of this integrating-type ADC is dependant on the linearity of the ramp voltage and the resolution of the comparator. The slope of the ramp voltage is determined by the current source and the size of the integrating capacitor. Both the ramp generator and the comparator have been designed to provide at least 12-bit accuracy across temperature. However,

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temperature variations affect the slope of the ramp voltage and thus the peak ramp voltage varies across temperature. The ADC's analog input range is set by the peak ramp voltage.
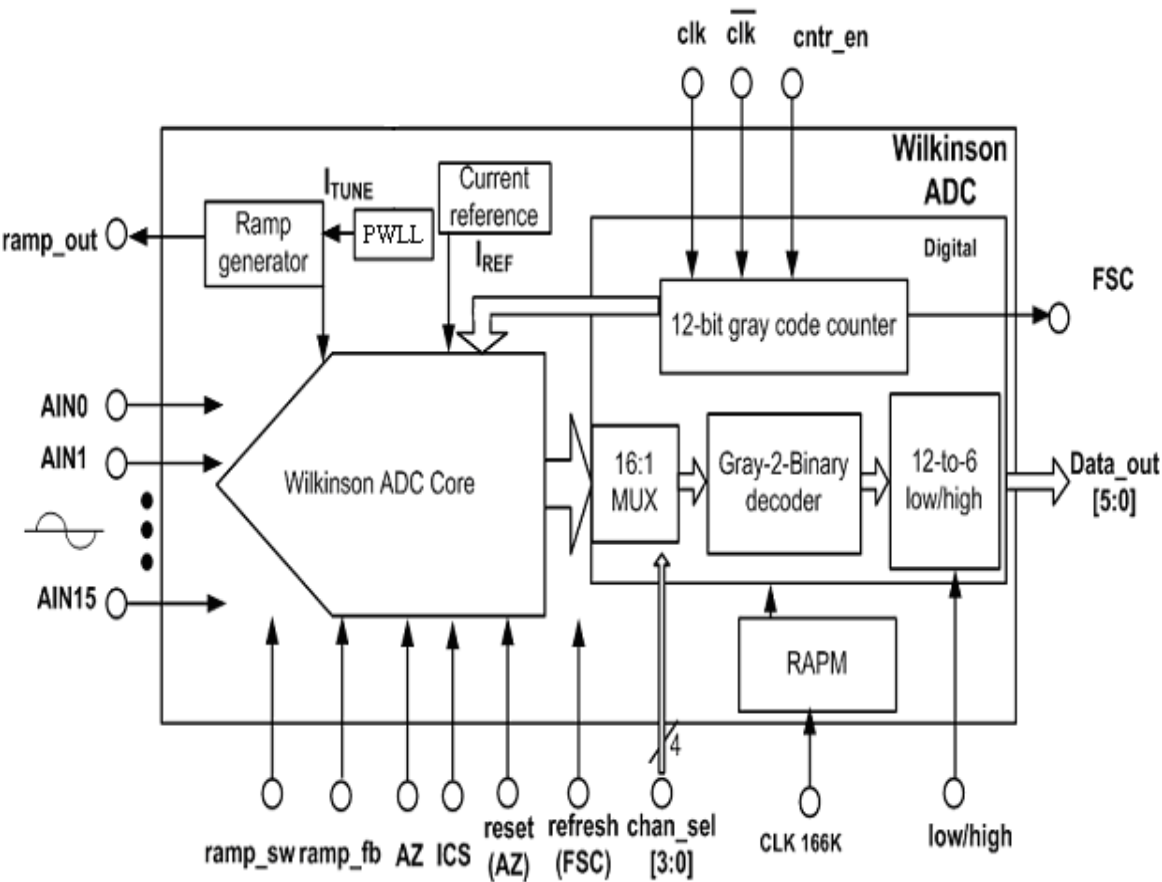
Figure 3. Functional block diagram of the Wilkinson ADC showing the PWLL

Figure 4 shows the measured variation of the peak ramp voltage versus temperature in the 12-bit Wilkinson ADC that was fabricated on a 0.5-µm SiGe process. The peak ramp voltage shows an error of 1.09 LSB per °C, which is unacceptable for extreme environment applications. The counter is assumed to be stable across process-voltage-temperature (PVT). The ramp voltage peak variations are caused partly by the current charging the capacitor and device mismatch within the ADC ramp generator which varies across PVT. The relation between LSB error and ramp variation is given by

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$$\Delta LSB = \frac{A \times 2^{12} \times \Delta v}{vref^2} \qquad (2)$$

where $vref = 0.5(V_{ramp1} + V_{ramp2})$, $\Delta v = V_{ramp1} - V_{ramp2}$, A = analog input voltage, ΔLSB = LSB error due to V_{ramp} shift, V_{ramp1} and V_{ramp2} are the peak voltages at two different temperatures.
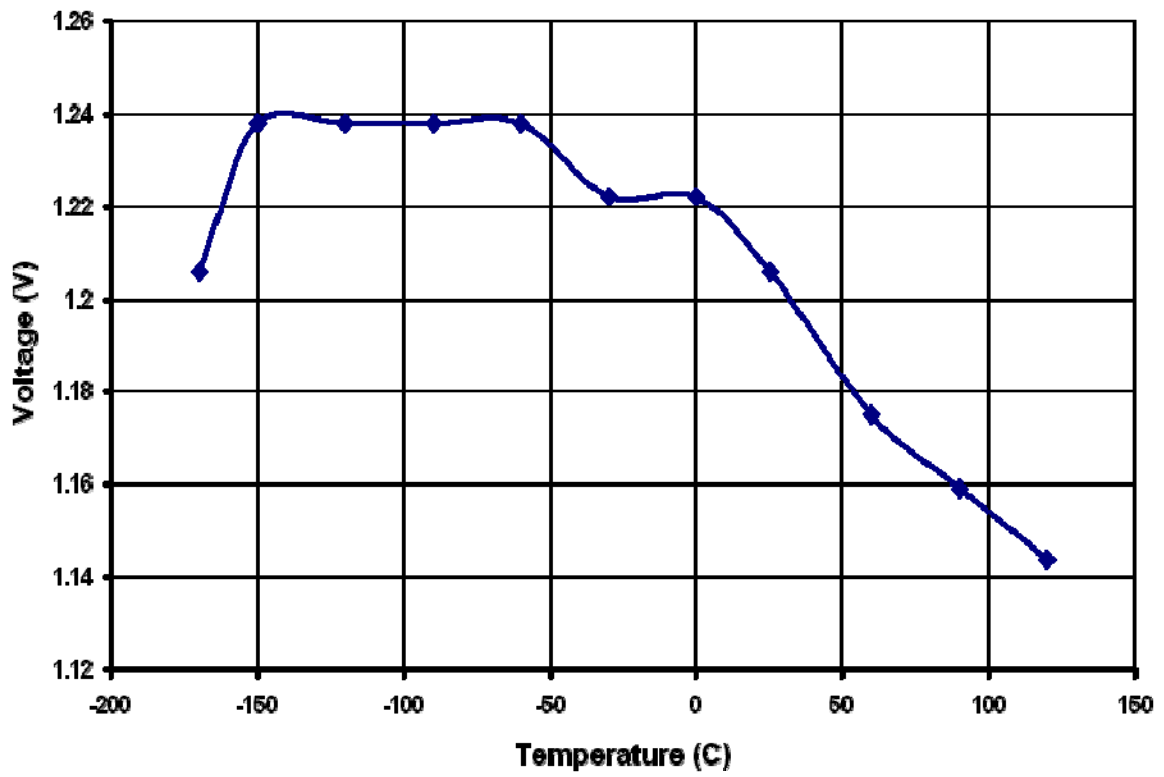
Figure 4. Measured peak ramp voltage across temperature

1.4 LITERATURE STUDY

An extensive literature search has been performed for papers dealing with PVT compensation techniques for single-slope based measurement systems especially for wide temperature operational range. To date there is only one paper reported for a cryogenic ADC which is a 8-bit Flash ADC operated from 4.2K to 300K [3]. However the paper does not shows resolution stability across wide temperature range. For the topology used in the work reported here, innovation has been made for single-slope based measurement systems to achieve wide temperature range operation. This work describes the first reported design approach to utilize a PWLL technique to perform PVT compensation for an ADC.

This thesis presents the design and implementation of a SiGe BiCMOS pulse-width-locked loop (PWLL) based PVT compensation for a 12-bit multi-channel Wilkinson ADC. Specifically, it addresses the ADC gain error induced by PVT variation in extreme environments. Chapter II provides PVT instability sources within the ADC and PWLL general architecture. Chapter III describes the PWLL mathematical model and its theoretical simulation result. In Chapter IV the operation and timing of the PWLL based PVT compensation technique are illustrated. Chapter V describes the PWLL building blocks and its operation. Chapter VI describes the test setup of the ADC testing. Chapter VII provides simulation and silicon measurement results. These include Monte Carlo simulations, results of the ramp peak voltage variation over PVT, and ADC max code variation measurement over PVT. A conclusion is provided in Chapter VII including suggestions for improving the design.

CHAPTER II

PVT INSTABILITY OF ADC

2.1 SOURCES OF RAMP VOLTAGE VARIATIONS
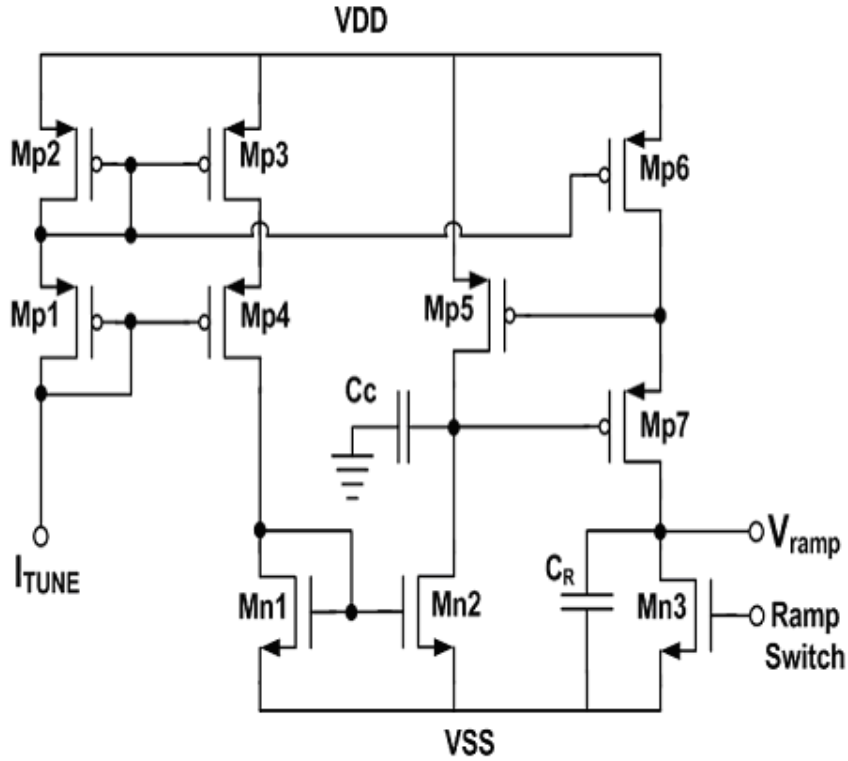
Figure 5. Schematic of a Ramp Generator Circuit [2]

Two key causes of variation of the ramp voltage are the Metal-Insulator-Metal (MIM) capacitor variation and the device mismatch within the current mirror. Equation (3) describes the ramp variation as a function of current mirror mismatch and capacitor variation [4, 5].

$$\frac{dv}{dt} \cong \frac{I_{TUNE}(1 + \Delta K / K - 2\Delta V_{TH} / V_{GS} - V_{TH})}{C_A \Delta L \Delta W + C_p \Delta L \Delta W} \tag{3}$$

where K is the device transconductance parameter, V_{TH} is the device threshold voltage, and W and L are the MIM capacitor width and length.

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The second main factor of ramp voltage variation is due to wide temperature range operation. The MIM capacitor variation over temperature is highly dependent on the process. For example, two variants of 0.5-μm SiGe BiCMOS from the same manufacturer provide MIM capacitor temperature variation of −57 ppm/ºC and 17 ppm/ ºC, respectively [4]. ADC ramp generator V_{TH} temperature variation is critical due to body effect at device Mp1 in Figure 5. Therefore, to achieve 300 μV of LSB accuracy for different processes, a mechanism to compensate MIM capacitor is critical. Providing a constant current source derived from a bandgap reference circuit to the ADC ramp generator does not eliminate the errors due to device mismatch and temperature variation in the current mirror. Equation (2) shows that instead of compensating bias current, a fixed *dv/dt* will achieve better overall immunity to device mismatch and temperature variation for the ramp voltage. Therefore the idea of the PWLL is to generate a temperature and process independent *dt* while *dv* is guaranteed by the bandgap reference voltage.

2.2 PWLL GENERAL ARCHITECTURE

The architecture of the Wilkinson ADC shown in [2] is modified as shown in Figure 3 by adding a PWLL design block to generate a PVT independent ramp voltage. Figure 6 shows the PWLL architecture which consists of a phase detector (PD), a charge pump (CP), and a pulse-width-modulation (PWM). The phase detector has a clock reference running at 10 KHz. The charge-pump converts the pulse-width difference generated by the phase detector to a control voltage. The PWM converts this control voltage to current through a 300 KΩ resistor, which is then mirrored to a ramp generator internal to the PWLL. The PWM essentially transforms the current to a time domain signal that is a pulse whose width is proportional to the current. This pulse signal is then fed back to the phase detector.

The PWLL design is a "type-I" control system with one pole contributed from the charge pump. The system bandwidth of the PWLL is designed to be approximately $(1/100^{th})$ of the PWM frequency for better steady-state resolution. Therefore, a 1.2 nF capacitor is required in the charge pump that is realized off-chip to save die area and more flexibility to adjust the system bandwidth during testing.
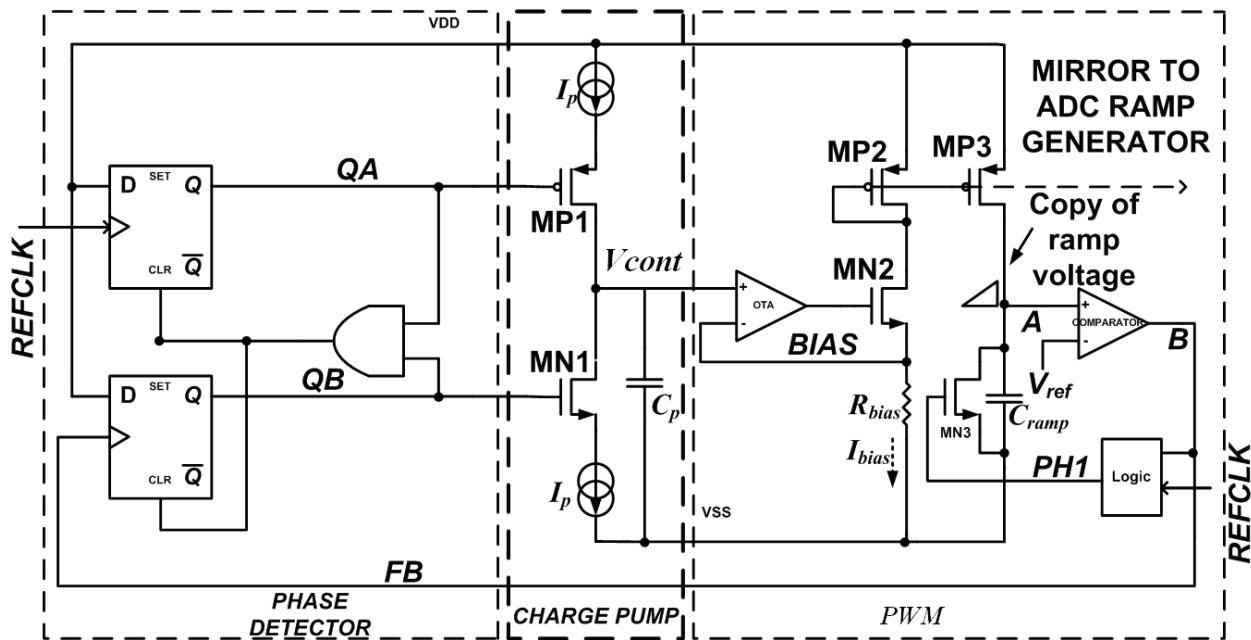
Figure 6. PWLL architecture

CHAPTER III

PWLL MODELING

3.1 PWLL LINEAR MODEL
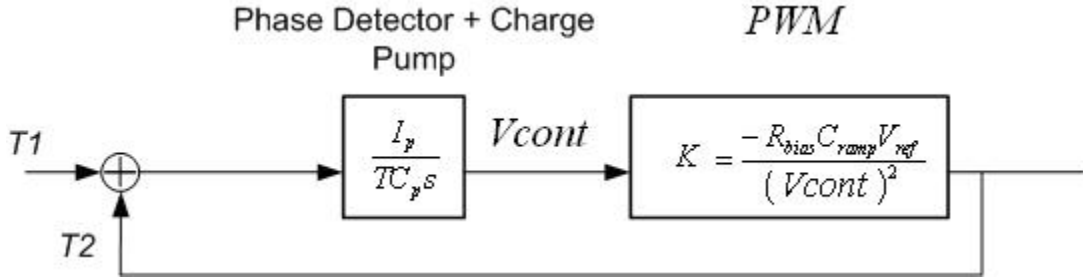
Figure 7. Linear model of PWLL

Figure 7 shows the linear model of the designed PWLL. To evaluate the system response, the transfer functions for CP and PD are shown where T is the period each time the charge pump is evaluated and $\Delta T = T2 - T1$. Equation (4) is the charge pump transfer function.

$$\frac{Vcont}{\Delta T}(s) = \frac{I_p}{TC_p s} \qquad (4)$$

The PWM regulates the duty cycle dt instead of changing frequency with respect to the $Vcont$ node.
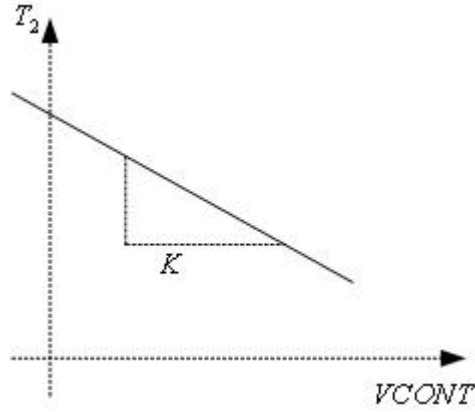
Figure 8. Definition of ideal PWM

From figure 6, I_{bias} set by the OTA regulated *Vcont* node and R_{bias}. Then I_{bias} is mirrored and supply ramp current to PWM capacitor (C_{ramp}).

$$I_{bias} = \frac{Vcont}{R_{bias}} \tag{5}$$

$$\frac{V_{ref}}{T_2} = \frac{I_{bias}}{C_{ramp}} \tag{6}$$

$$T_2 = \frac{R_{bias} C_{ramp} V_{ref}}{Vcont} \tag{7}$$

$$\frac{dT_2}{dVcont} = K = \frac{-R_{bias} C_{ramp} V_{ref}}{(Vcont)^2} \tag{8}$$

Equation (8) shows the *K* or PWM transfer function. Note that the relationship between T2 and *Vcont* is non-linear because *K* varies inversely with the square of *Vcont*.

To get open loop gain *H(s)* with T_2 as output signal and ΔT as input signal, Equation (4) is multiplied with Equation (8).

$$T_2 \Big/ \Delta T = H(s)\big|_{open-loop} = \frac{-R_{bias}C_{ramp}V_{ref}I_p}{C_p(Vcont)^2 s} \tag{9}$$

Since feedback gain in the linear system is 1, then the close loop transfer function can be written as

$$H(s)\big|_{close-loop} = \frac{H(s)_{open-loop}}{1 - H(s)_{open-loop}} \tag{10}$$

and therefore

$$H(s)\big|_{close-loop} = \frac{1}{\left[\dfrac{TC_p(Vcont)^2}{R_{bias}C_{ramp}V_{ref}I_p}\right]s + 1} \tag{11}$$

Thus a close-loop gain response is derived and a first-order control system is obtained in Equation (11). Using a unit step input to the close-loop system, the output *H(s)* can be expressed as:

$$H(s) = \frac{1}{s}\frac{1}{\left[\dfrac{TC_p(Vcont)^2}{R_{bias}C_{ramp}V_{ref}I_p}\right]s + 1} \tag{12}$$

By taking the inverse Laplace transform of Equation (12), the time-domain equivalent *h(t)* is provided.

$$h(t) = \left(1 - \exp\left(\frac{-t}{\dfrac{TC_p(Vcont)^2}{R_{bias}C_{ramp}V_{ref}I_p}}\right)\right) \tag{13}$$

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$$\Gamma \approx \frac{1}{\dfrac{-R_{bias}C_{ramp}V_{ref}I_p}{C_p(Vcont)^2 s}} \approx \frac{C_p(Vcont)^2}{R_{bias}C_{ramp}V_{ref}I_p} \tag{14}$$

From Equation (13), time constant Γ is derived in Equation (14).

Note that the time constant is proportional to $(Vcont)^2$. During system start-up, the $Vcont$ node is initialized to 0 V which gives Γ an infinitely small value that is not feasible. The PWLL is designed to prohibit T_2 from exceeding the period T. Therefore a well defined start-up condition is required. Thus $Vcont$ transient response during the initialization phase is not governed by the first-order equation derived in Equation (11).

In the initialization phase, I_{bias} is not large enough to drive C_{ramp} to V_{ref} within T. The ΔT during the initialization phase is the full pulse width of T_1 since T_2 is equal to T. To get the initialization phase transient response, substituting equation (4) into (5). During the initialization phase, equation (15) and (16) are obtained.

$$Vcont(t) = \frac{V_{ref}R_{bias}C_{ramp}}{T} \tag{15}$$

$$t_{initialized} = \frac{V_{ref}R_{bias}C_{ramp}C_p}{I_p \Delta T} \tag{16}$$

$Vcont(t)$ and $t_{initialized}$ indicate boundary conditions to initialize the first order-system. Equation (16) defines the time required for the PWLL to follow the first-order system model in Equation (11).

3.2 SIMULATIONS OF PWLL MATHEMATICAL MODEL

Figure 9 shows the comparison between first-order control system with initialization phase adjusted and simulation of the PWLL *Vcont* node voltage. The difference between the two curves is due to an approximation made by averaging *Vcont*. The close agreement between the two verifies the derived model.
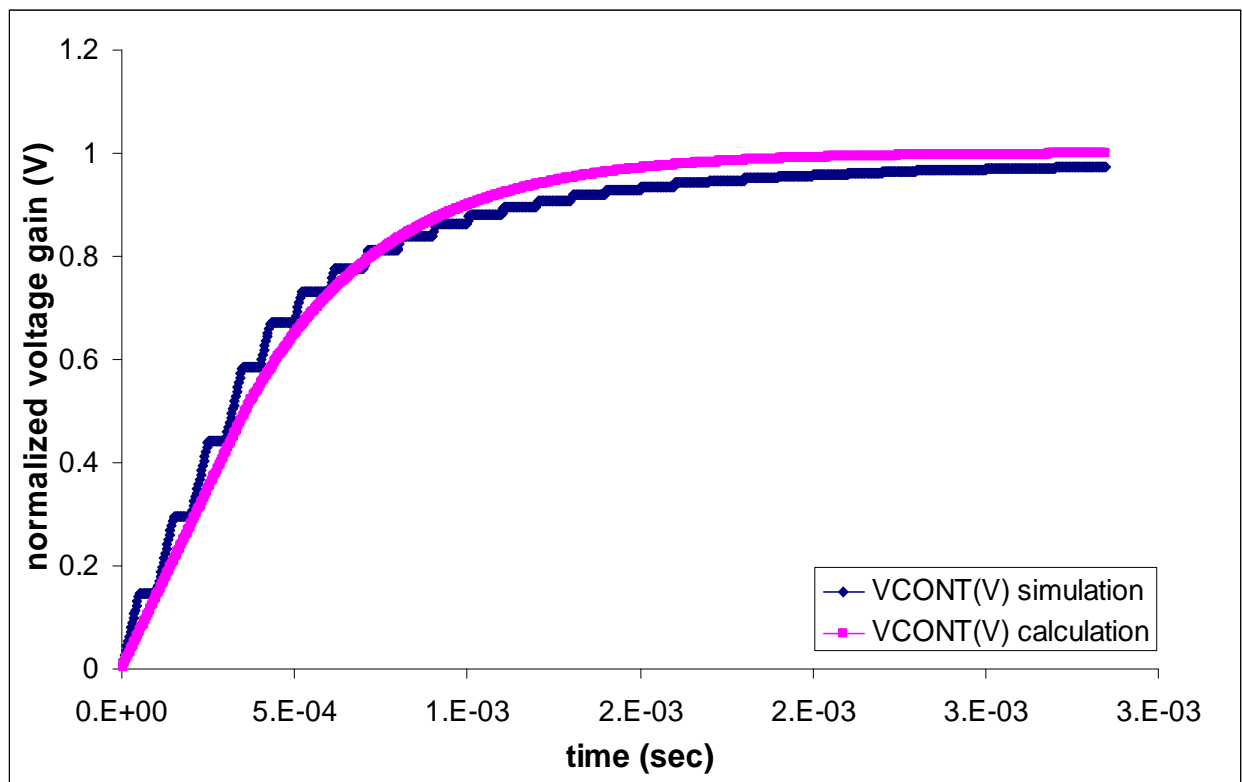

Figure 9. Plot of *Vcont* using theoretical derivation and PWLL simulation

CHAPTER IV

PWLL DESIGN BLOCK

4.1 PWLL DESIGN BLOCK

A. PHASE DETECTOR

The detector consists of two D-flip-flops and one NAND gate to control the reset of the D-flip-flops. Inputs to both the D-flip-flops are tied to the supply voltage (VDD). The D-flip-flops are clocked separately by *REFCLK* and *FB* signals. The *FB* signal is the output of the comparator that is being fed back to the phase detector. The *REFCLK* signal is an external signal which also controls the charging and discharging of the ramp generator circuit. The function of the phase detector is to sense the time difference between the rising edges of *FB* signal and the *REFCLK* signal. If the rising edge of the *FB* signal is leading the rising edge of *REFCLK*, *QB* is pulled up until the rising edge of *REFCLK*. On the rising edge of *REFCLK*, *QA* is pulled high. As a result, the reset signal to the D-flip-flops is activated. If the *FB* signal lags the *REFCLK* signal, *QA* is pulled high first, followed by *QB*, which then resets the D-flip-flops.

B. CHARGE PUMP

The overall PWLL is a type-I control system. The pole is contributed by the charge pump in the PWLL. From equation (3) the system bandwidth is computed. In this design a 5 µA current source and current sink are used to charge and discharge a 1.2 nF off-chip compensation capacitor.

MP1 acts as a pass gate to charge the compensation capacitor and increase the voltage at the *Vcont* node. MN1 acts as a pass gate to discharge the compensation capacitor and decrease the voltage at the *Vcont* node. Larger device width is chosen for the pass gate devices which reduces the on resistance and, in turn, reduces the voltage drops across these transistors.

C. PWM

A negative feedback network consisting of an operational transconductance amplifier (OTA) and a NMOS transistor allows the *BIAS* node to follow the *Vcont* node voltage level. The OTA is a two-stage amplifier and the NMOS transistor is in a common drain configuration. The current output of the PWM is determined as in equation 4. Hence, the generated current bias that compensates the ramp generator depends on the voltage at node *Vcont* and the R_{bias} resistance which is a poly resistor with a value of 300 KΩ.

The adjusted current that is mirrored by MP2 and MP3 charges C_{ramp}. C_{ramp} is matched with the 186 pF capacitor in the ramp generator. A comparator is used to convert a saw-tooth waveform generated across the MIM capacitor to a pulse waveform with a width equal to *dt* that is the ramp time. The comparator output, *FB*, is fed back to the phase detector to be compared with *dt* of *REFCLK*.

D. OTA

A simplified two-stage OTA is shown in Figure 10. It is designed to isolate the *Vcont* node and *BIAS* node. The OTA first stage consists of an N-channel differential input with a regulated cascode N-channel current source bias. The Second stage consists of a common-source amplifier with large small-signal gain. To improve the bandwidth of the OTA, a diode connected load for

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the first stage is used. However this will trade off the gain achievable in the first stage. To enhance the stability of the OTA, a Miller compensation scheme is used to improve OTA phase margin. Overall bandwidth achieved is 6.4 MHz with 45 dB small-signal gain. Phase margin is 60 degrees. The frequency performance is shown in Figure 11.
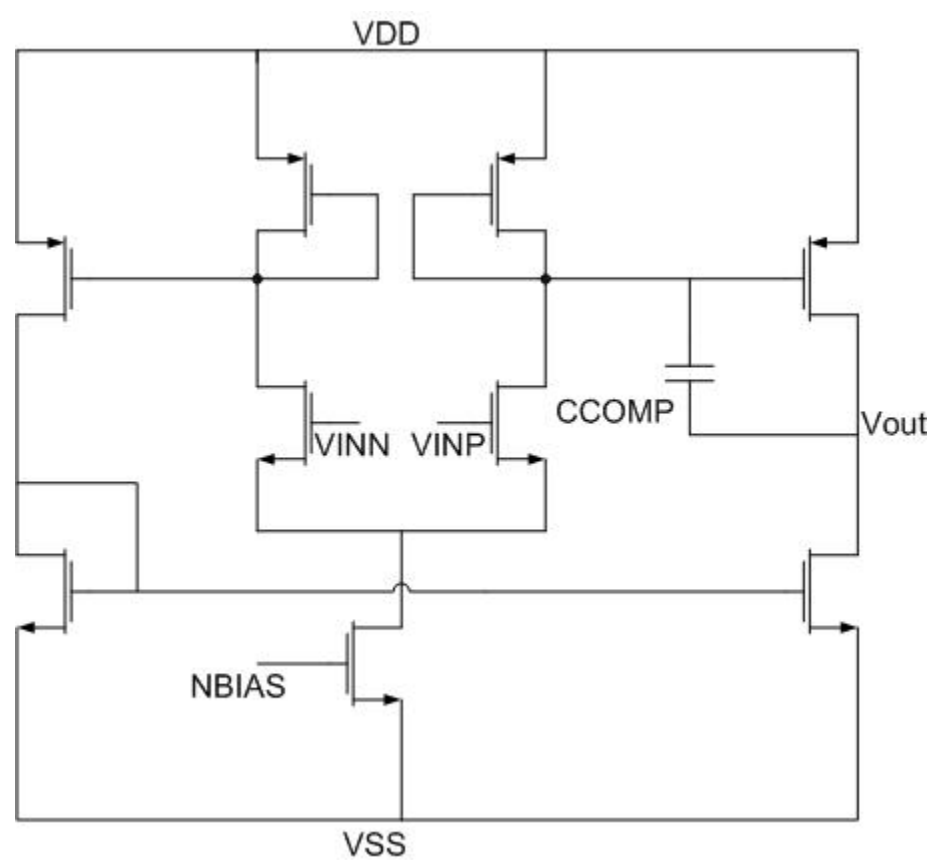

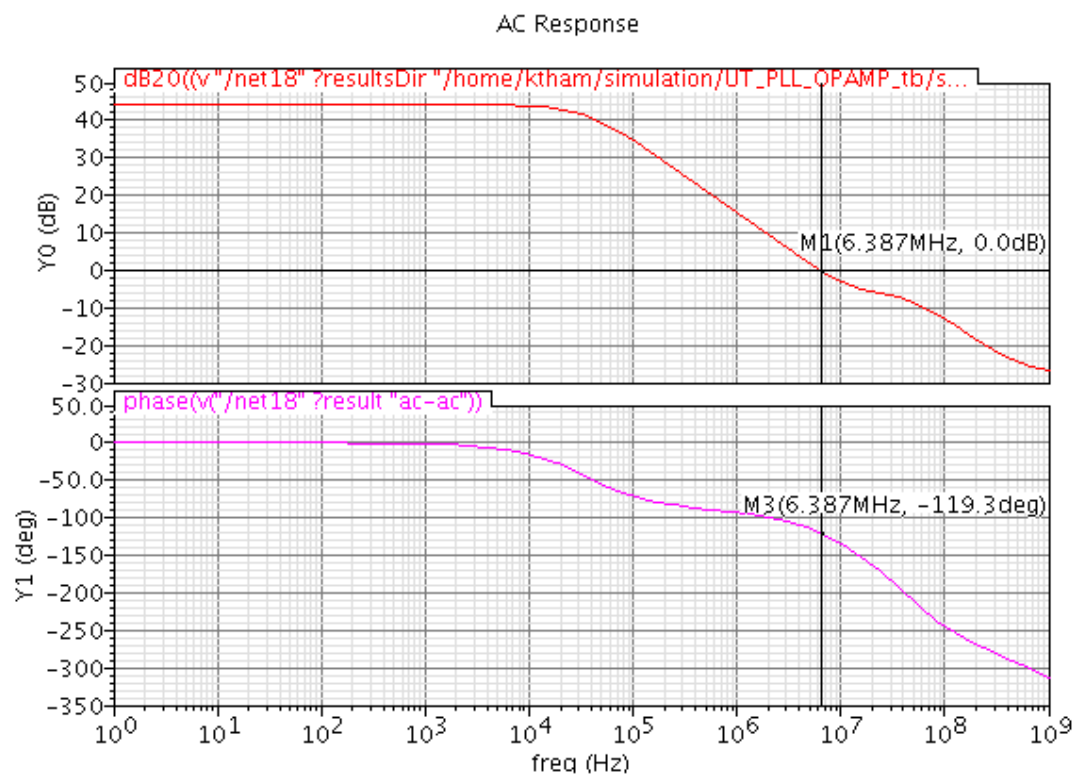Figure 10. Simplified schematic of OTA circuit

AC Response

Figure 11. Frequency response of OTA

Figure 12, shows the comparator architecture designed. The comparator designed is an internal positive feedback in the input stage of a high-gain, open-loop comparator. When INP > INN, majority current is flowing through MP5 to MN3. Drain voltage of MP5 is lower than drain voltage of MP2 and hence turn on MP3. The positive feedback action is further driving drain node of MP2 to VDD and shut off MP2, MP1 and MP4. The differential stage here does not provide enough voltage swings and output resistance to the output node. Therefore a Class AB output stage MP6, MP1, MN4 and MN1 to complete the differential to single ended conversion.

Figure 13 shows the transient response of the two stages comparator. The response time of INP to VOUT is about 70nsec. This response time requirement is more than enough for 10KHz switching frequency.
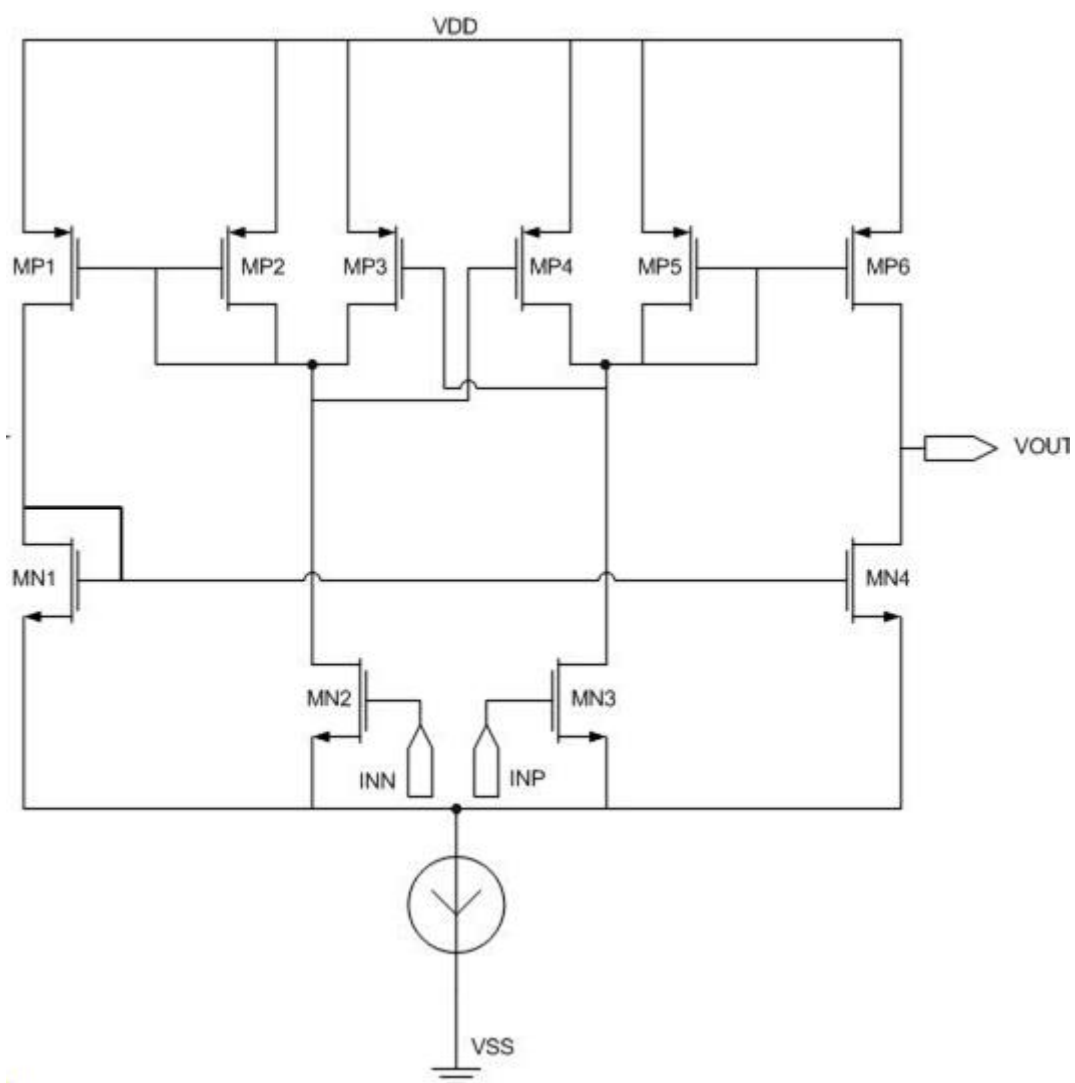
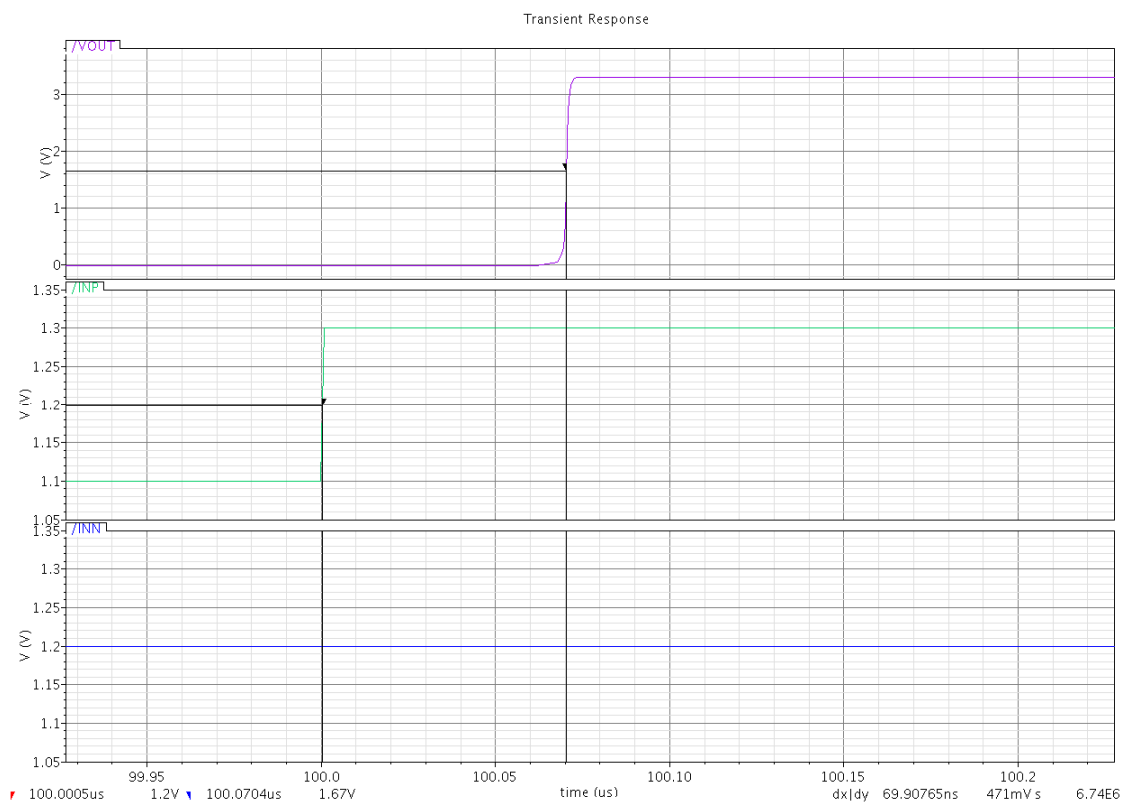Figure 12. Simplified schematic of comparator circuit

Figure 13. Transient response of the two stages comparator
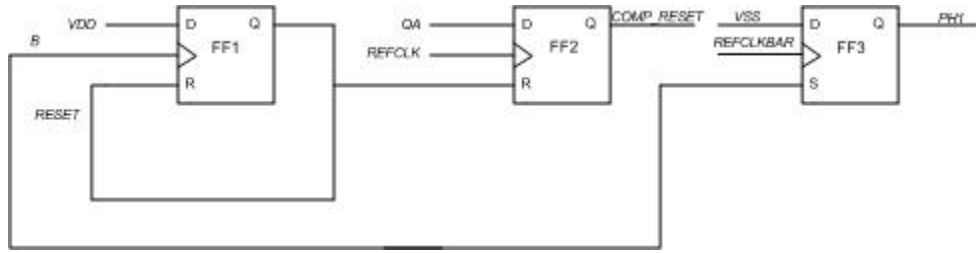
F. *Logic Block*

Figure 14. Simplified PWLL Logic Block Schematic

A digital circuit is designed to perform the logic operation of the PWLL(see Figure 12). This is an asynchronous digital system design that functions mainly to control the signal between the comparator and internal ramp switch. In the previous chapter the described PWLL prohibits overflow of ramp time beyond a clock cycle and the logic block is handling the overflow check logic operation. The logic block is clocked by the 10KHz by *REFCLK* signal. *COMP_RESET* is generated by FF2 to reset *B* at comparator output when *B* goes high (internal ramp exceed V_{ref}). FF3 generates *PH1* at the falling edge of *REFCLK*. *PH1* will continue to stay high to turn on the internal ramp switch until the comparator output, *B* goes high.

4.2 PWLL OPERATION

A 10 KHz clock is used as a reference clock to the phase detector. The PWM in Figure 6 converts the voltage to *dt* and feeds this back to the detector for *dt* error detection. The *dt* error is converted to a voltage *Vcont* using a charge pump circuit. The bias current generated by the PWM that is controlled by *Vcont* is mirrored out to bias the ADC ramp generator. *PHI1* is a switch that controls the charge/discharge of PWM capacitor. The falling edge of the *REFCLK* signal starts charging the PWM capacitor, C_{ramp}, which produces a linearly increasing voltage at node *A*. This is the ramp voltage internal to the PWLL.

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When the PWLL ramp voltage reaches the bandgap reference voltage, the comparator output node B changes from a logic low to a logic high voltage. Logic high at node B causes C_{ramp} to discharge. After C_{ramp} discharges, node B returns to a logic low level.

If ramp voltage is above the bandgap reference voltage, B is triggered earlier than the rising edge of $REFCLK$ which creates a pulse at QB. A pulse at QB reduces the voltage at node $Vcont$ which in turn reduces the I_{bias} generated by the PWM. If dv is below the reference, B is triggered later than the rising edge of $REFCLK$, creating a pulse at QA which increases the voltage at node $Vcont$ and increases the I_{bias} current produced by the PWM. A detailed timing diagram is shown in Figure 15. I_{bias} reference refers to the room temperature PWM I_{bias} generated for single-slope measurement system.
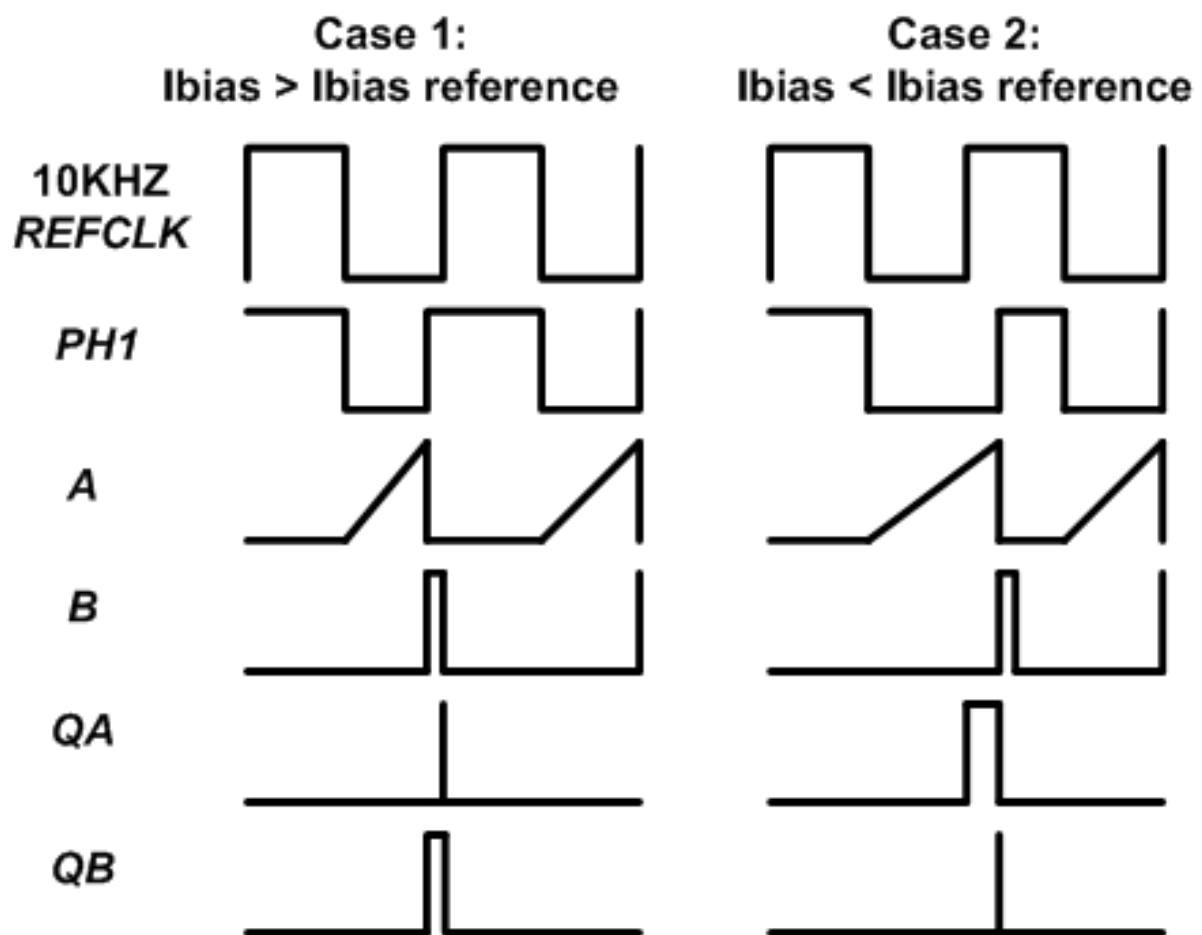
Figure 15. PWLL timing diagram

CHAPTER V

TEST SETUP

5.1 MOTHERBOARD DESIGN

The ADC PVT Compensation technique is implemented on remote sensor interface (RSI) chip on a 0.5-µm BiCMOS process. The hardware test path includes a motherboard consisting of voltage regulators, PCI interface and an interface to a daughter card. The daughter card consists of a RSI chip, LVDS transceiver and Actel FPGA.

The motherboard is shown below in Figure 16. This board contains all the required voltage and current supplies. Each of the power source sections are numbered and Table 1 shows their respective powered functionality.
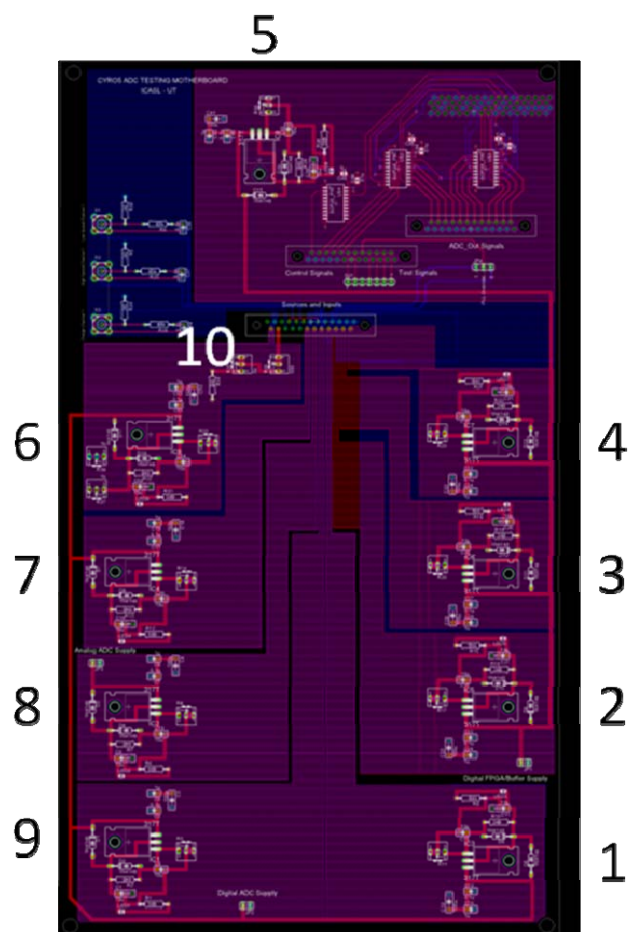
Figure 16. Motherboard Layout

Table 1. Supply requirements

# on Figure 14	Signal	Output
1	DIG_3P3V_ADC	3.3 V
2	VCCR	5 V
3	VCCI	3.3 V
4	VCCA	3.3 V
5	VDD_BUFFER	5 V
6	VREF_BGR	2.4 V
7	VDD_ESD	3.3 V
8	ANA_3P3V_ADC	3.3 V
9	DIG_3P3V_PWLL	3.3 V
10	ISRC_700U	700 µA

Voltage regulator 1 is mainly used to supply power to the on-chip ADC digital operation while voltage regulator 2, 3, and 4 is used to power Actel FPGA. Voltage regulator 5 is used by the buffer IC that resides at daughter card to strengthen digital signal integrity along the cable from the temperature chamber to the motherboard. Voltage regulator 6 is set to 2.4V on the motherboard and divided down to 1.2V to be used on-chip as a bandgap voltage reference. The purpose of using a divider to set the bandgap voltage at 1.2V is due to the minimum output voltage produced by LM317 voltage regulator is 1.25V. Voltage regulator 8 is to supply ADC and PWLL analog circuit operation while voltage regulator 9 is to supply digital operation of the PWLL circuit. Voltage regulator 10 is mainly used to supply the 700μA current source to the LVDS chip on the daughter card.
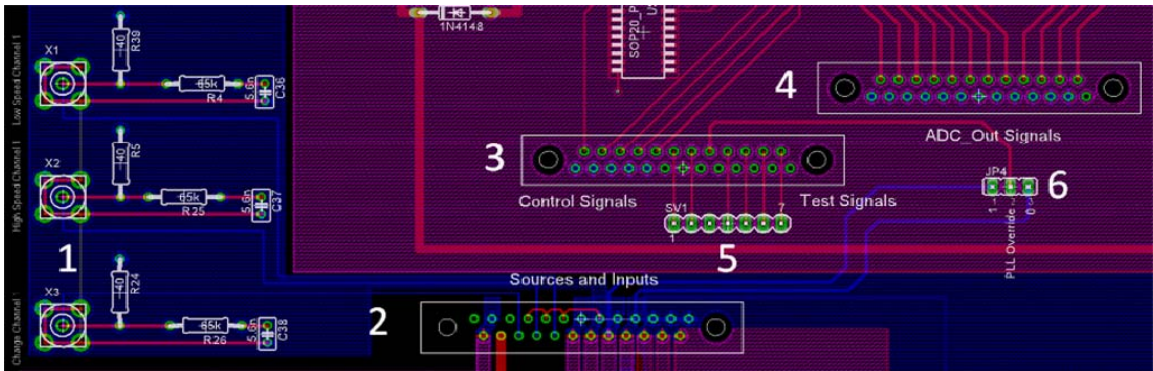

Figure 17. Motherboard section

Figure 17 shows the section of the board where the motherboard and daughterboard interface. Section 1 shows the analog input signals to each channel. These are clearly labeled on the board itself. Section 2 shows one of the 25-pin interfaces that connect to the daughterboard. This connector contains the necessary bias voltages and currents, as well as three analog inputs. Section 3 contains the control signals that will go to the NI (National Instruments) connector, 6 test signals, and the PWLL Override signal. Section 4 contains the 12 bit output from the ADC. These will go to the NI connector as well. Section 5 is a 7-pin header that contains 6 test signals.

Pin 1 is the left most pin whereas pin 7 is the right most. These signals are detailed in Table 2 below.

Table 2. Test pin locations

Pin #	Signal
1	MPC_SCN_OUT_GLBL
2	FSC_ADC
3	NOT USED
4	RAMP_OUT_ADC
5	COMP_5U_IOUT_ADC
6	MPC_SCN_IN_GLBL
7	SHFT_REG_TM_GLBL

Pins 6 and 7 must physically be connected with a jumper wire to VDD or ground depending on the mode of operation. Section 6 contains the PWLL_Override signal. This signal can either be tied to VDD or ground via a jumper. If the PWLL_Override signal tied to ground, PWLL is activated else deactivated.

5.2 DAUGHTERBOARD DESIGN

The daughterboard is shown below in Figure 18. It contains the 144-pin RSI, Actel A54SX32 FPGA, clock inputs, the oscillator, and the LVDS transmitter.
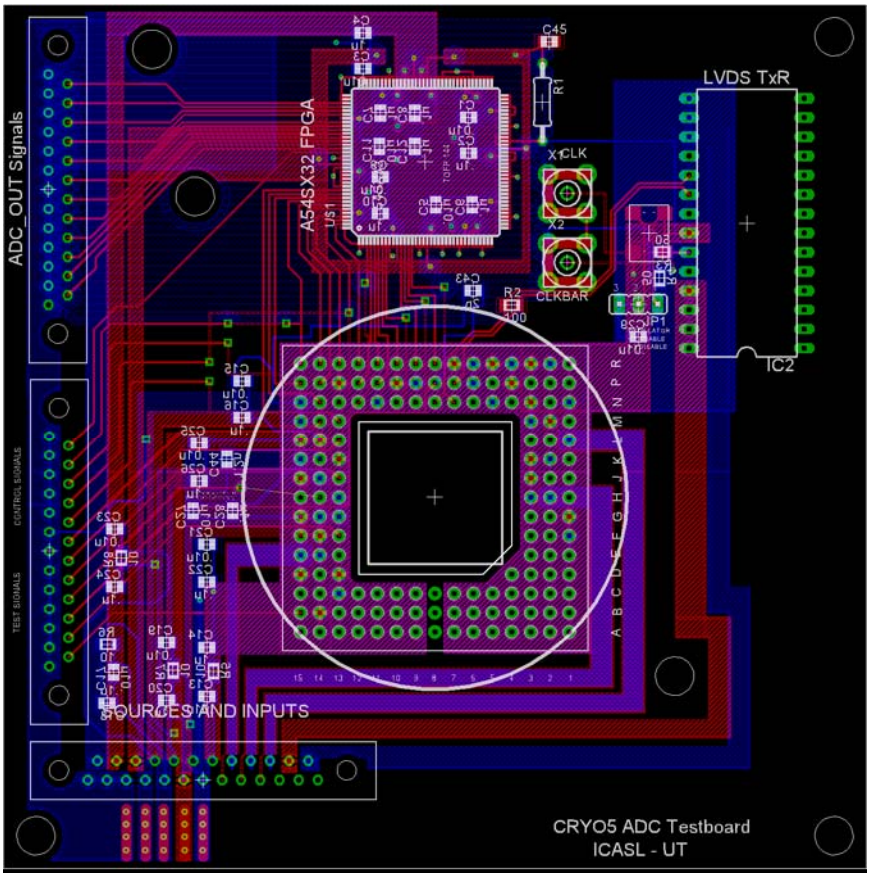

Figure 18. Daughterboard layout

The board also contains two sets of bypass capacitors per power supply, ceramic 0.01μF and 0.1μF. There is also a 10Ω resistor in series with the power supplies. If input power needs to be measured, it can be done by reading the voltage across this resistor.

A. Board Stackup

Due to the fact that we are using a pin grid array package, the board required two layers for digital signals. This meant that instead of the originally planned 6 layers, we had to increase that to 8 layers. The stackup for the board can be seen in Figure 19 below with the first layer of digital signals on the top and the analog signals layer on the bottom.

Digital Signals
_____
Digital Ground
_____
Digital Signals
_____
Digital Ground
_____
Digital VDD
_____
Analog VDD
_____
Analog Ground
_____
Analog Signals

Figure 19. Daughterboard stackup

B. Clock Setup

There are two methods to input a clock to the system: using high-speed cables to provide the clock and clockbar signals or using the on-board 80 MHz oscillator. To use the high-speed cables, the oscillator has to be disabled. This is done by setting the jumper on the board to position 2-3. To use the oscillator, the high-speed cables are not connected and jumper is set to position 1-2.

Both the clock and clockbar signals are terminated with 50Ω resistors. The clock signals as well as the oscillator output are both input to the LVDS transmitter. The transmitter then outputs the clock signals through 50Ω transmission lines into the differential-mode

100Ω termination resistor.

C. RAMP_OUT_ADC Signal

The ramp output signal is one of the test signals that go to the motherboard. This signal however should not be connected at all times because the ramp is generated by the charging and discharging of capacitors. If the ramp signal is physically connected to an output, it would add a capacitive load, thus changing the amount of capacitance used by the signal. The true RAMP_OUT_ADC signal cannot be measured, but if an approximate test signal is needed, one must physically connect the pin to certain via on the board with a jumper wire. This connection is shown in orange in Figure 20 below. It is also written on the board to indicate which pins to connect for clarity.
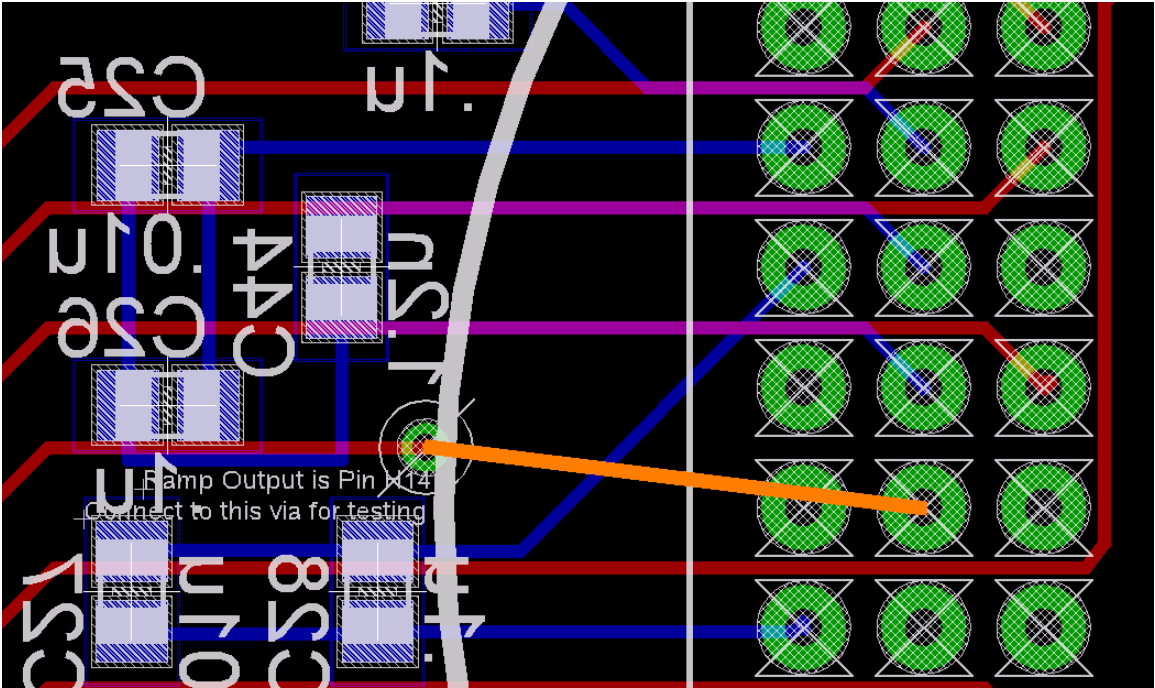

Figure 20. Jumper wire needed for Ramp_OUT_ADC testing

5.3 Equipment Setup

Test equipment setup is shown in Figure 21 and Figure 22. For ADC characterization, labview is used as the characterization interface. A Lecroy Clock Generator is setup to 50MHz to provide the system clock to the daughter card and mother card. A low-noise signal generator is used to provide an analog sine wave input signal to the ADC. The daughter card is placed in the chamber to sweep from −180 ºC to 125 ºC during the experiment. Liquid Nitrogen is used for cooling purposes.
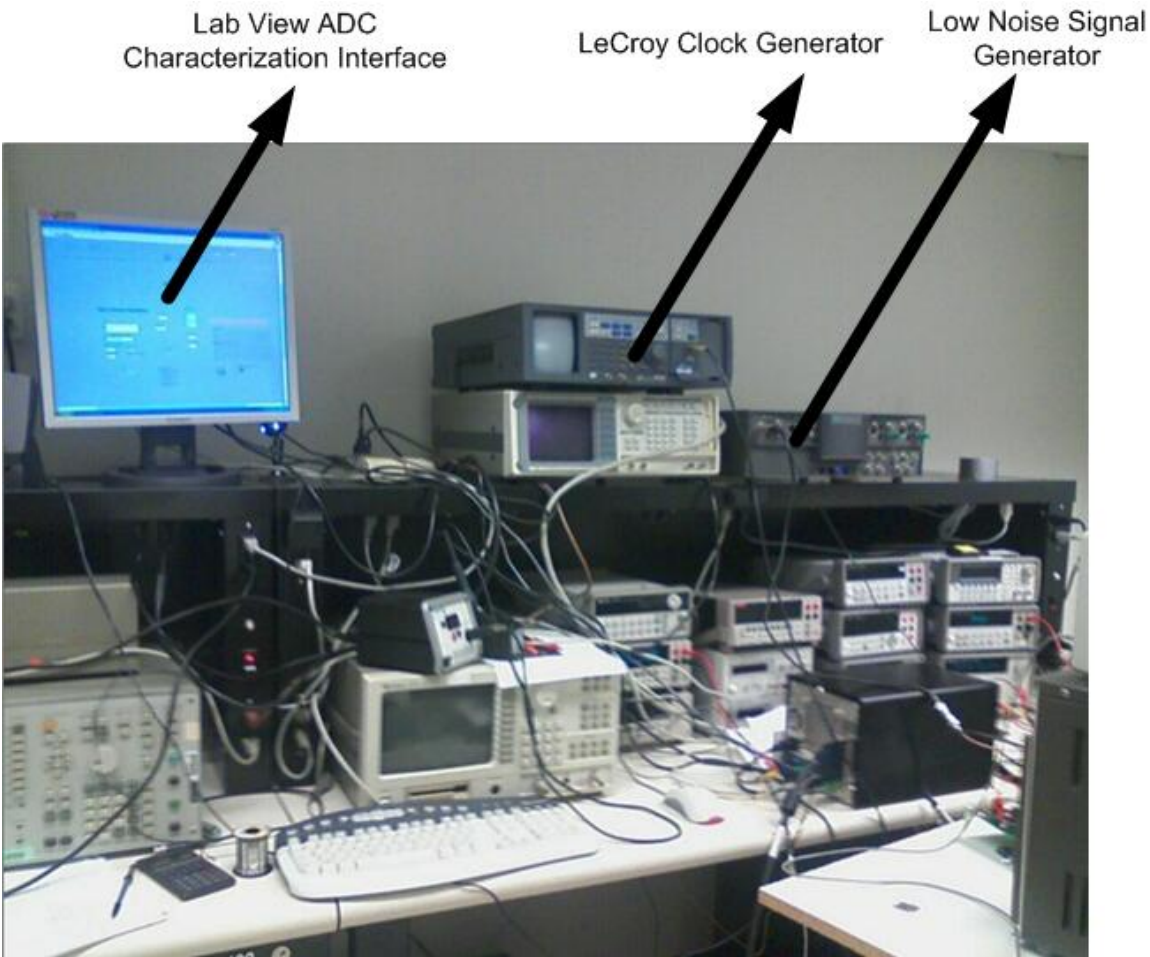

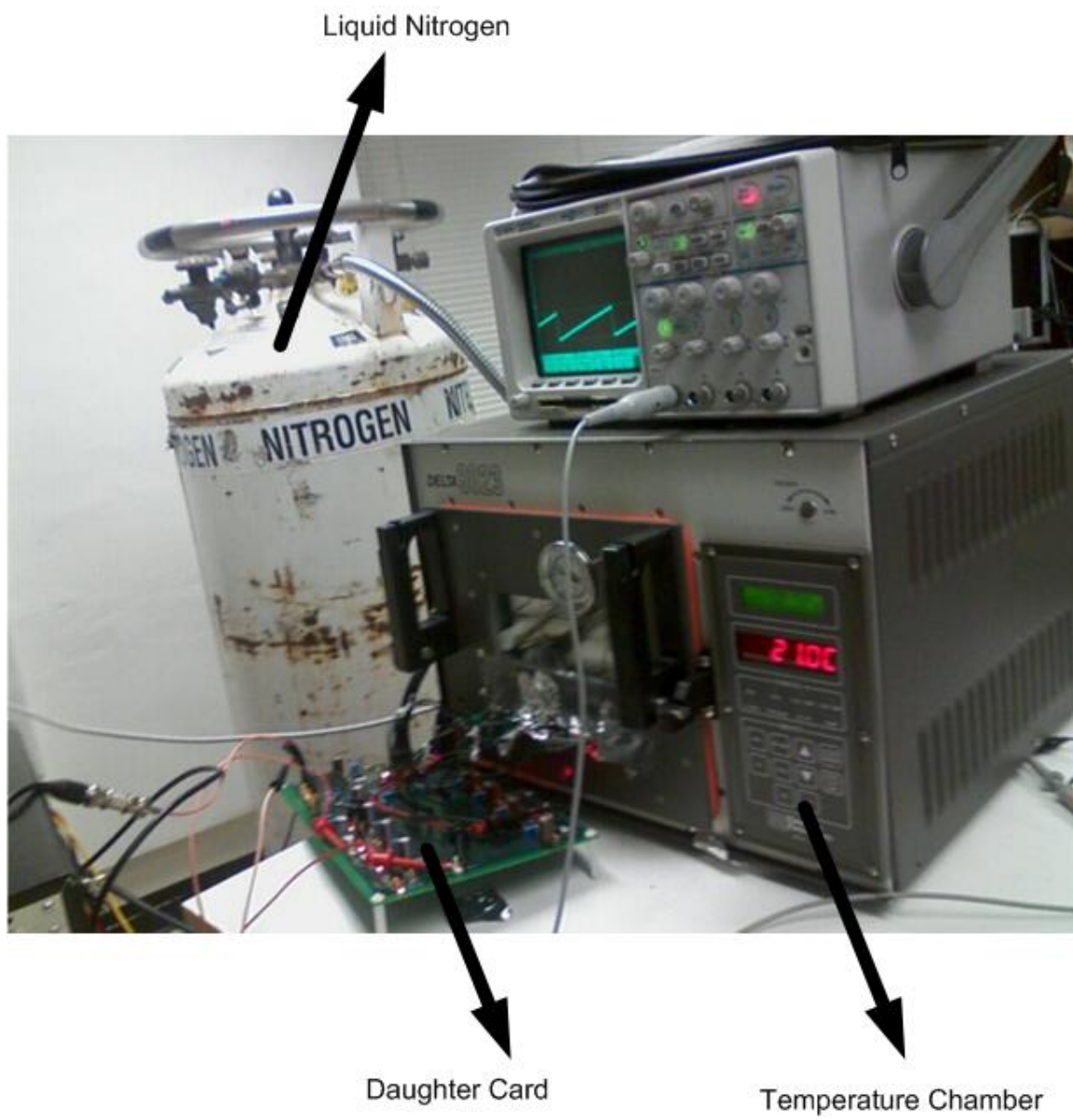Figure 21. Test Equipment Setup during ADC characterization I

Figure 22. Test Equipment Setup during ADC characterization II

CHAPTER VI

TEST RESULTS

6.1 PWLL TEST CHIP

A PWLL compensation scheme for a 12-bit multi-channel Wilkinson ADC is designed and fabricated in a 0.5-µm SiGe BiCMOS process. The layout is as shown in Figure 23. The PWLL occupies 1500x500 µm^2 of layout area. In order to reduce the noise coupling from the digital section to the analog section, separate power supplies are used for the analog and the digital circuitry. The *VCONT* node is sensitive and is hence shielded using an NWELL layer on chip to help block substrate noise from being injected into the *VCONT* node. Because of layout constraints, the current mirror and the C_{ramp} of the PWLL does not match with ramp generator current mirror and MIM capacitor. This mismatch is expected to degrade the performance of the PWLL.
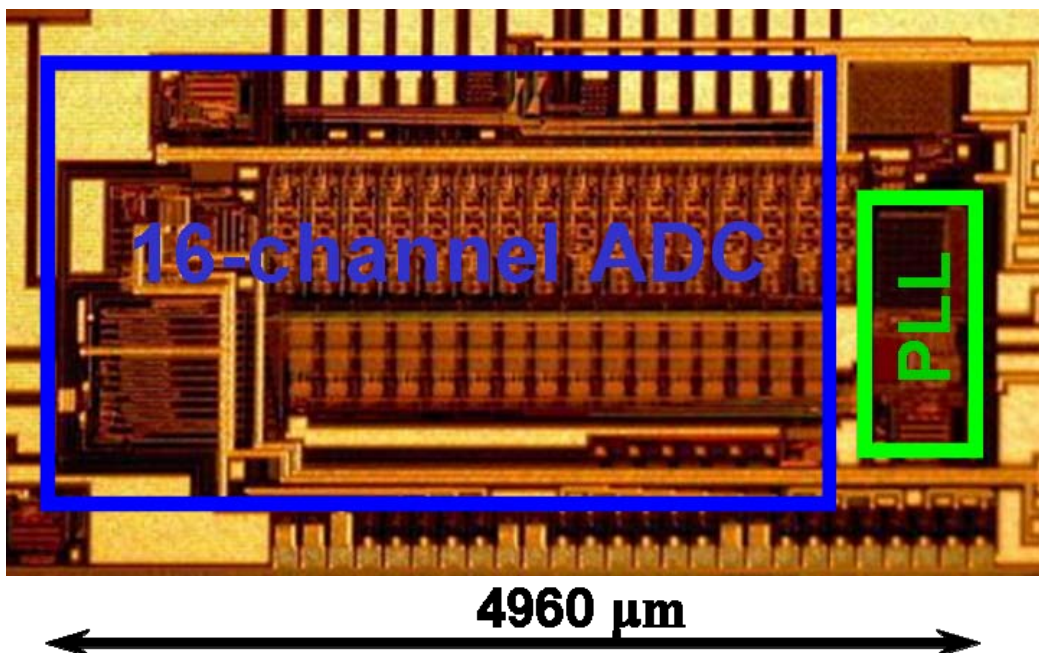

Figure 23. Die photo of PLL along with the Wilkinson ADC

6.2 12-BIT WILKINSON ADC CHARACTERIZATIONS

The 12-bit Wilkinson ADC is characterized in both PWLL and constant current mode. Figures 24–27 shows the respective characterization results from −180 °C to 125 °C. All the characterization shows DNL result of between −0.5 to 0.5. This is showing good ADC data collection through out the experiment. DNL refers to the difference between ideal and nonideal values [7]. It is defined as

DNL_n = Actual increment height of transition n − Ideal increment height

Where n is the number corresponding to the digital input transition.

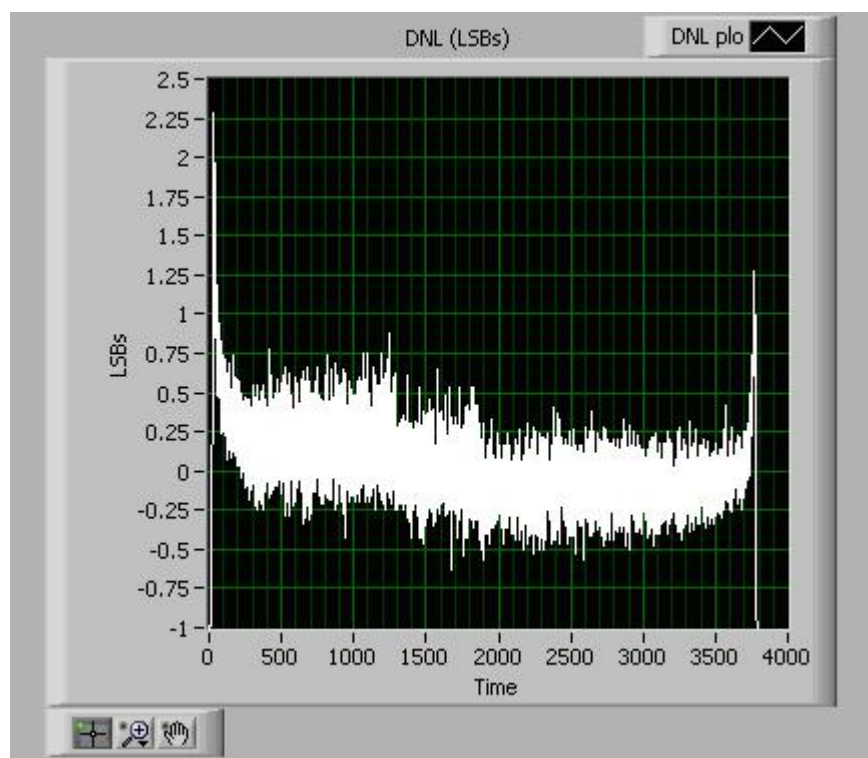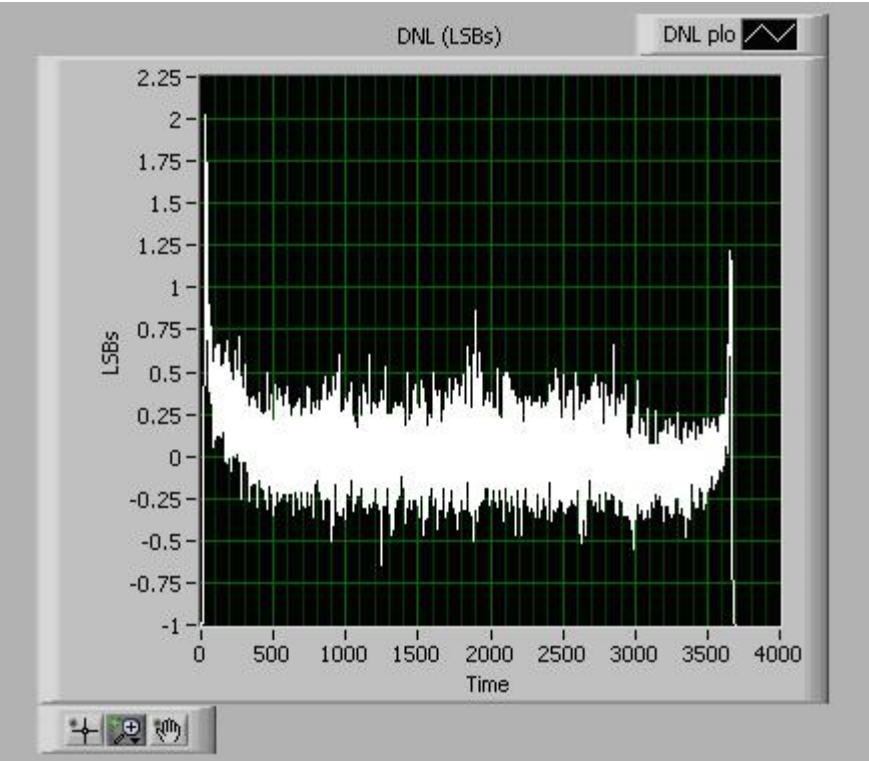Figure 24. 125 °C ADC DNL characterization in PWLL mode

Figure 25. −180 °C ADC DNL characterization in PWLL mode
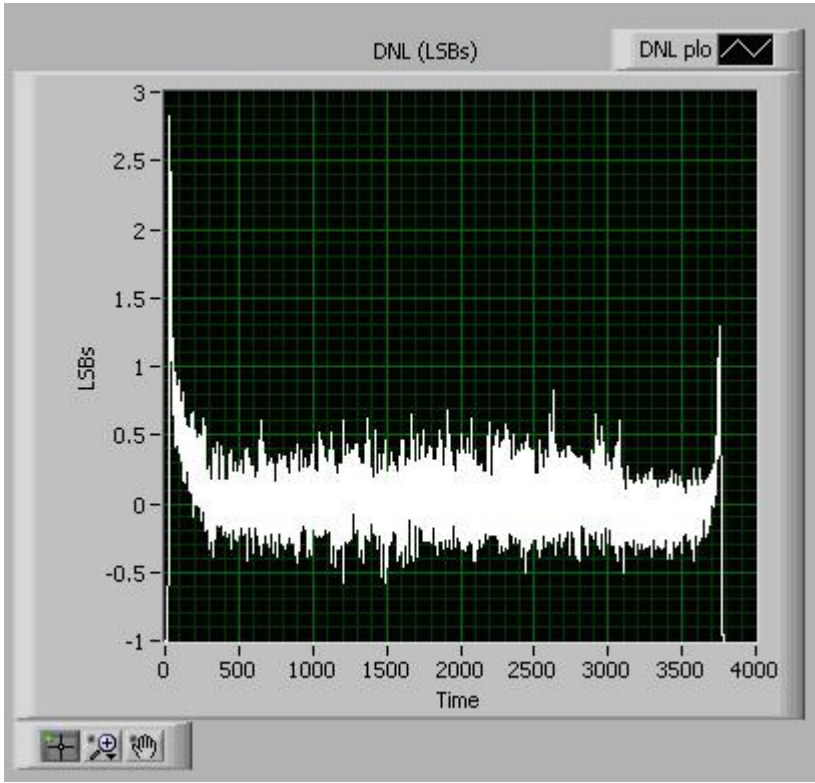

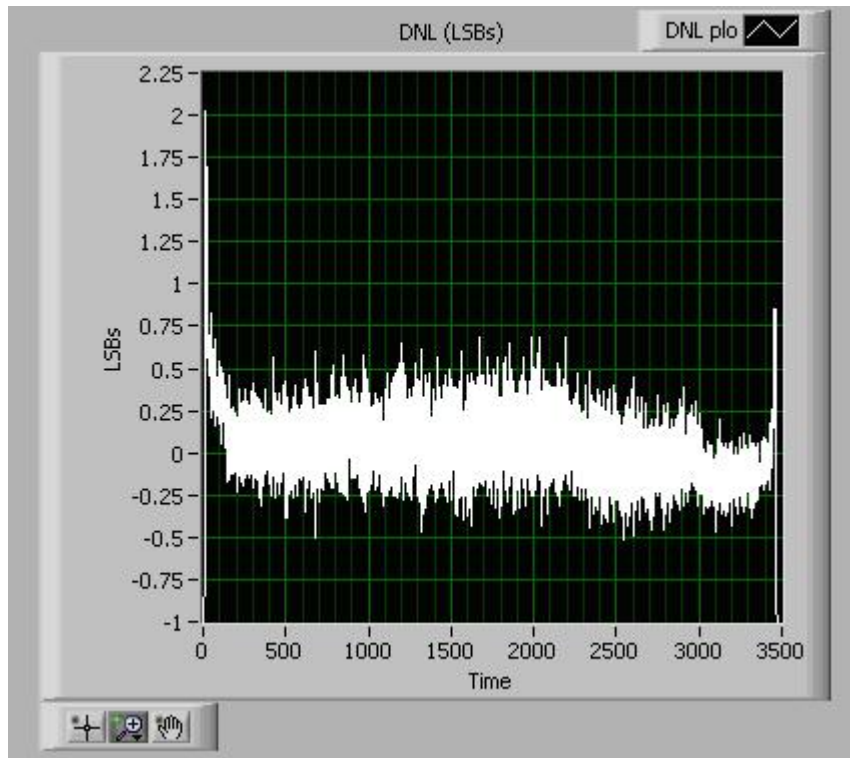Figure 26. 125 °C ADC DNL characterization in Constant Current mode

Figure 27. −180 °C ADC DNL characterization in Constasnt Current mode

Besides the DNL characterization, a digitized waveform is shown to observe the range of the digitized signal generated. Max code data is recorded to justify the implication of PVT variation to ADC data collection. From Figures 28 and 29, max code shifted from 3850 to 3774 across the 305 degree temperature sweep in PWLL mode.
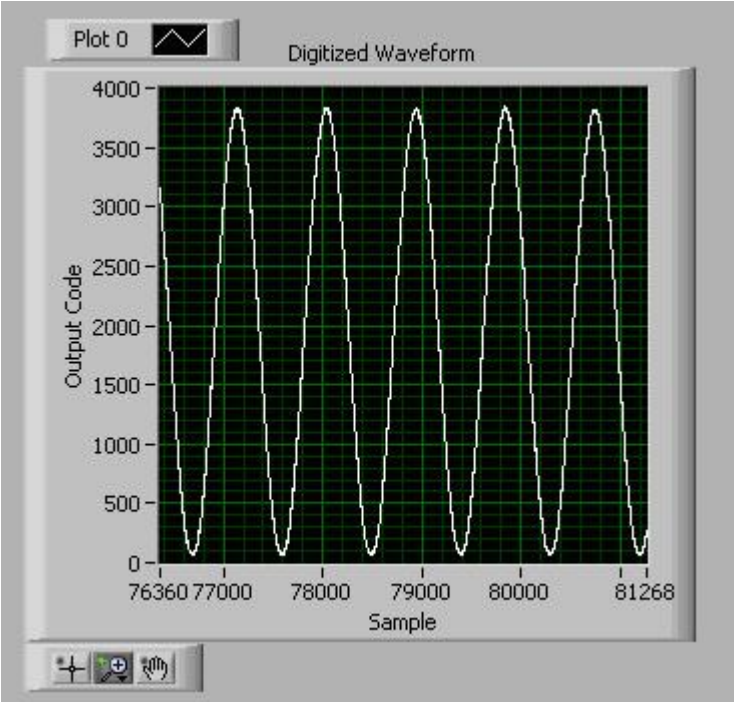
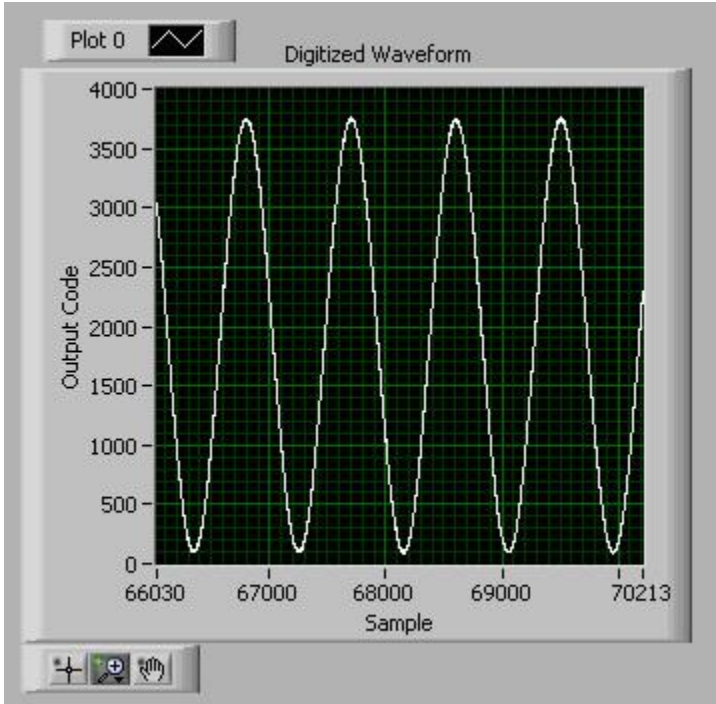Figure 28. 125 °C ADC digitized output waveform in PWLL mode

Figure 29. −180 °C ADC digitized output waveform in PWLL mode

Figure 30 and 31 shows the max code shifted from 3831 to 3550 across wide temperature range in constant current mode. Obviously the ADC operated in PWLL mode has better max code stability across wide temperature range compared to constant current mode.
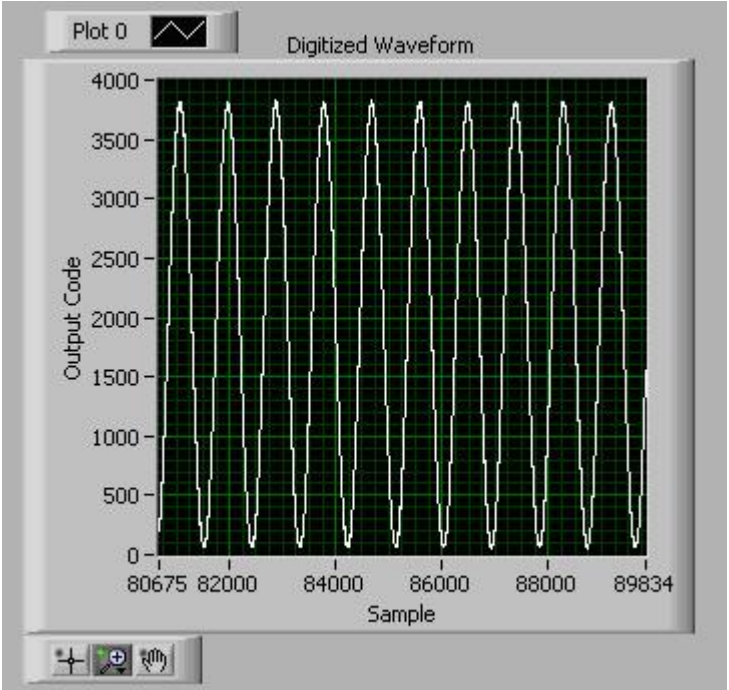

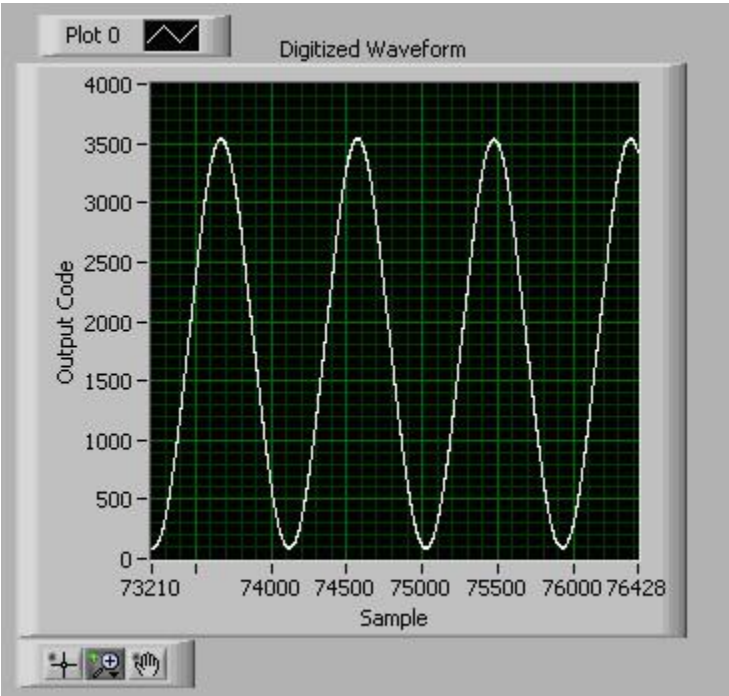Figure 30. 125 °C ADC digitized output waveform in Constant Current mode

Figure 31. −180 °C ADC digitized output waveform in Constant Current mode

6.3 PWLL PERFORMANCE CHARACTERIZATION

For the PWLL performance characterization, three separate post-layout simulations were performed to investigate the variation of *dv* of the ADC due to PVT variation. Figure 32 shows the impact of process and device mismatch on *dv* using Monte Carlo simulations. The ramp voltage internal to the PWLL shows less than 30 mV (100 LSB) variation due to process and device mismatch. The ADC's ramp voltage with PWLL compensation shows 140 mV (466 LSB) variation which is much lower compared to the ramp voltage without PWLL compensation showing a variation of 450 mV (1500 LSB). The difference in the LSB error between the PWLL internal ramp voltage and the PWLL compensated ramp voltage (output of the ramp generator) is due to layout mismatch of the current mirror and the ramp capacitor of these two blocks.

The impact of supply voltage variation on the ramp voltage for the ramp generator with the PWLL compensation scheme is negligible compared to the ramp generator without the PWLL compensation scheme for the ADC which has 20 mV (67 LSB) variations.

Figure 33 shows ADC Max Code variation over a wide temperature range (−150°C to 125ºC). The PWLL biased ADC shows 180 max code variation compared to the constant current source biased ADC showing a variation in max code of 325. The data was collected from the actual silicon ADC measurement. The PWLL biased ADC shows overall better max code stability across wide temperature variation compared to the constant current biased ADC. Notice however that at temperature from 75°C to 100 °C, there is a slightly faster degradation rate on the PWLL biased ADC compared to the constant current biased ADC. The reason for this region can be due to temperature effect between threshold voltage and device mobility. At higher V_{GS}, the mobility dominates and the drain current is inversely proportional to temperature. Since the constant current source has negative temperature coefficient at high temperature, a reduction of drain current can be expected. As the drain current reduces, V_{GS} will reduce as well to an extend that the threshold voltage temperature effect will cancel the mobility temperature effect within the circuit [7].
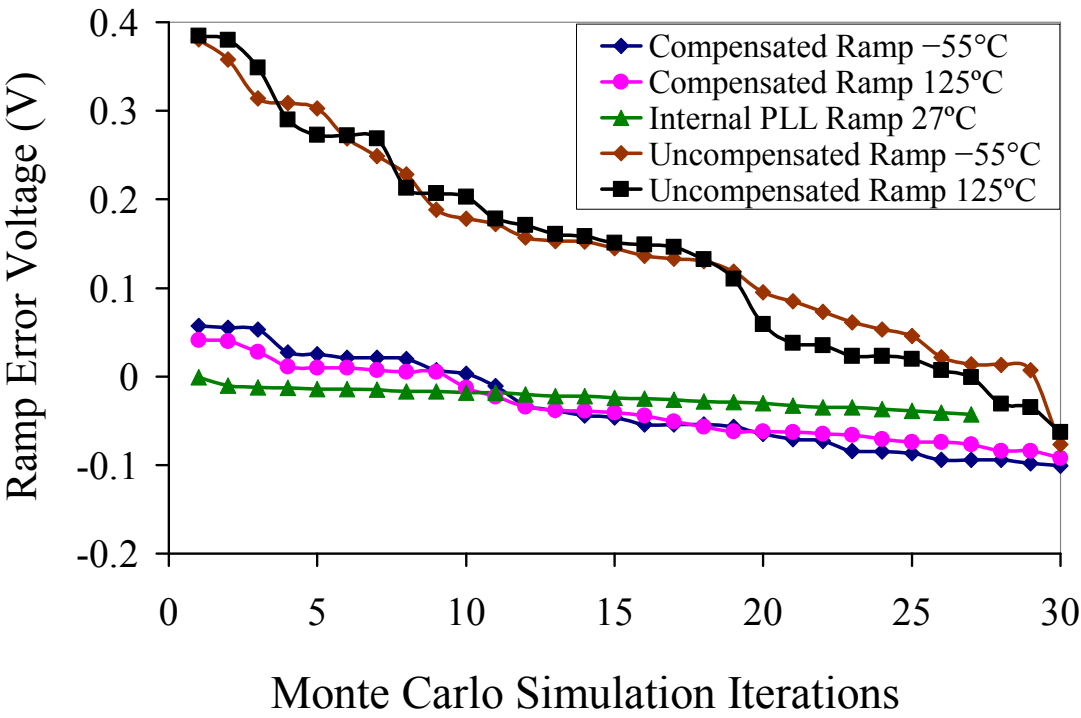
Figure 32. Post-layout Monte Carlo simulation *dv* variation due to process and device mismatch
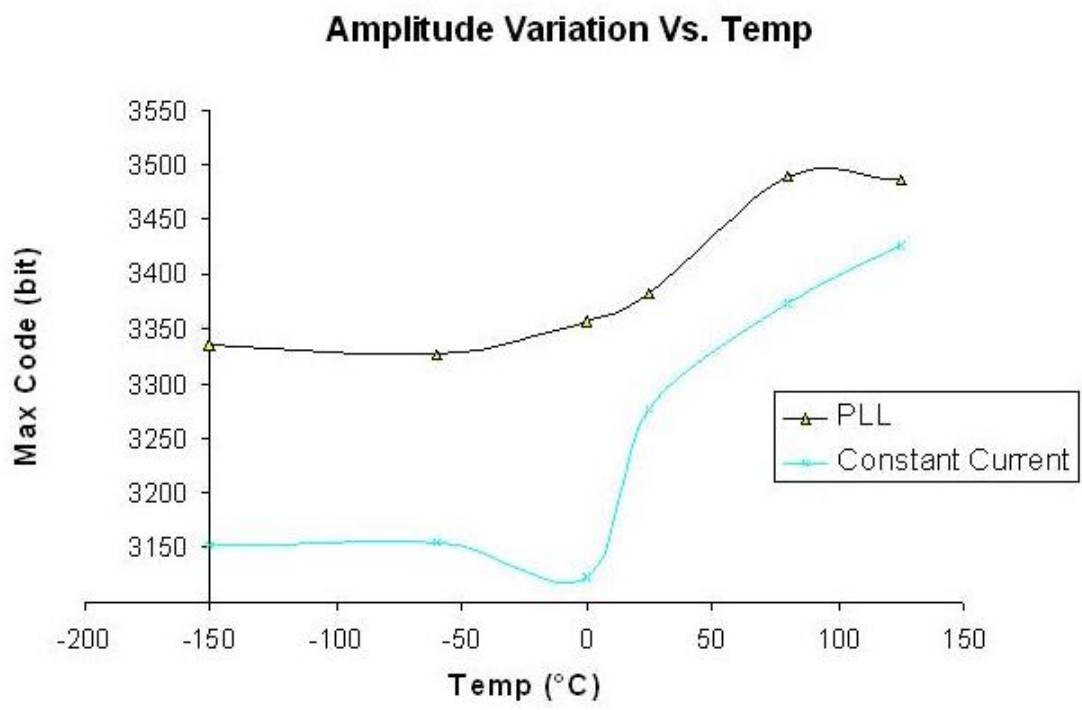
Figure 33. Silicon ADC Max Code variation over temperature

CHAPTER VII

CONCLUSION

A PWLL-based PVT compensation scheme for a 12-bit Wilkinson ADC was designed and fabricated in a commercial 0.5-um SiGe BiCMOS process. Measurement results show that the PWLL compensation scheme provides a 44.6% reduction in the ADC's maximum output variation across a wide temperature range. Future work on the PWLL compensation scheme includes improving the ADC accuracy, which is related to the mismatch between a ramp capacitor in the PWLL and the ADC's ramp generator. The accuracy can be improved by directly supplying the ramp voltage generated within the PWLL to the ADC. The accuracy can be below 50 code difference across 305 degree temperature range if the internal ramp voltage is used by the ADC.

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VITA

Kevin Tham was born in Kota Kinabalu, Malaysia on October 28, 1980. He grew up in Tawau, Malaysia. Kevin then entered Telecom University, and graduated with a Bachelor of Electronics Engineering in 2004. He joined Intel, Malaysia in 2004 as component design engineer until 2007.

Kevin began his research assistant at the Integrated Circuit and Systems Laboratory at the University of Tennessee while pursuing his Master of Science in Electrical Engineering at the University of Tennessee in the Integrated Circuits and Systems Laboratory under the direction of Dr. Benjamin Blalock.