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Development of a High-Efficiency, Low-Power RF Power Amplifier for Use in a High-Temperature Environment

Stephen Terry
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Stephen Terry entitled "Development of a High-Efficiency, Low-Power RF Power Amplifier for Use in a High-Temperature Environment." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed Islam, Major Professor

We have read this thesis and recommend its acceptance:

Charles Britton, Jr. Benjamin Blalock

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Benjamin Blalock

Accepted for the council:

Dr. Anne Mayhew

Vice Provost and
Dean of Graduate Studies

(Original signatures are on file in the Graduate Student Services Office.)

Development of a High-Efficiency, Low-Power RF Power Amplifier for Use in a High-Temperature Environment

A Thesis
Presented for the
Master of Science
Degree

The University of Tennessee, Knoxville

Stephen Christopher Terry
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Abstract

This thesis presents a study of the design of a high efficiency, low power, RF power amplifier that can operate over an extended temperature range. The amplifier has been implemented as a hybrid circuit with the active device fabricated in a 0.5μm silicon-on-sapphire CMOS technology and passive components implemented off-chip. First a review of power amplifiers is given. Next design considerations for low power, high efficiency amplifiers are presented. Finally design details and measurement results from a low-power Class E amplifier are presented. When operated with an output power of 1 mW, the Class E amplifier achieves an efficiency greater than 40% over the frequency band 250 MHz to 310 MHz at 25 C and from 265 MHz to 295 MHz at 200 C.

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Chapter 1

Introduction and Overview

1.1 Introduction

1.1.1 Low-Power Remote Sensors

Moore's law states that the density of integrated circuits will double roughly every eighteen months [1]. Because of this exponential growth in integrated circuit complexity, new applications become possible every year. For instance, the first integrated circuits in the late 1960's could only perform primitive functions, such as amplification [2]. The 1970's saw the first fully monolithic analog-to-digital converters (ADC) [3]. In the 1980's Intel produced computer chips that contained over one-million transistors [4]. One concept that has become very popular over the last decade is systems-on-a-chip (SOC). SOC is a very general term that refers to performing several different functions on a single integrated circuit. A system-on-a-chip might consist of analog signal processing blocks, an ADC, and a microprocessor combined on one monolithic circuit. The advantages of SOC are numerous, and include smaller area, lower power dissipation, and higher reliability; when compared to a printed circuit board solution that contains several individual chips [5].

One example of SOC that has received great attention in recent years is low-power, remote sensors [6]. Remote sensing involves coupling a transducer, which is measuring a physical process, directly with an integrated circuit. The integrated circuit would be capable of aqcuiring the measured analog signal, filtering, and then digitizing before it is

transmitted to a computer. To better understand the advantages of remote sensing, consider Figure 1.1 shown below. Part (a) shows how a typical harsh environment measurement would have been performed several years ago. The transducer converts a physical measurement to an analog electrical signal, which is then amplified and transmitted over a channel. The channel may be free space (the signal would first have to be modulated) or it may be directly sent over a 50 ohm cable. For this example, it will be assumed that the channel is a 50 ohm cable. As the signal travels along the cable, it will lose power due to resistive losses. In addition, noise will be added to the signal due to DC resistance in the cabling. Finally, noise will be added due to any signals in the harsh environment which are able to couple onto the cable. The net effect of all of these non-idealities is that the signal-to-noise-ratio (SNR) of the measurement will be degraded.

Now consider an example of a harsh environment measurement made using remote smart-sensors, as shown in part (b) of Figure 1.1. Again the transducer would map a physical process to an electrical signal. Except now, the signal is sent to a system-on-a-chip, which is coupled directly to the transducer. The integrated circuit would immediately filter and digitize the measured signal. The signal that is finally sent over the cable is digital data. The large signal digital data would have a high noise immunity, when compared with the low level analog signal that was transmitted in the previous case. The end result is that the SNR, and therefore the quality of the measurement, will be much higher for the latter case. Of course, harsh environment measurements are only one application of remote sensing technology. Other applications include smart sensors that can multiplex (frequency division, time division, code division) signals from several

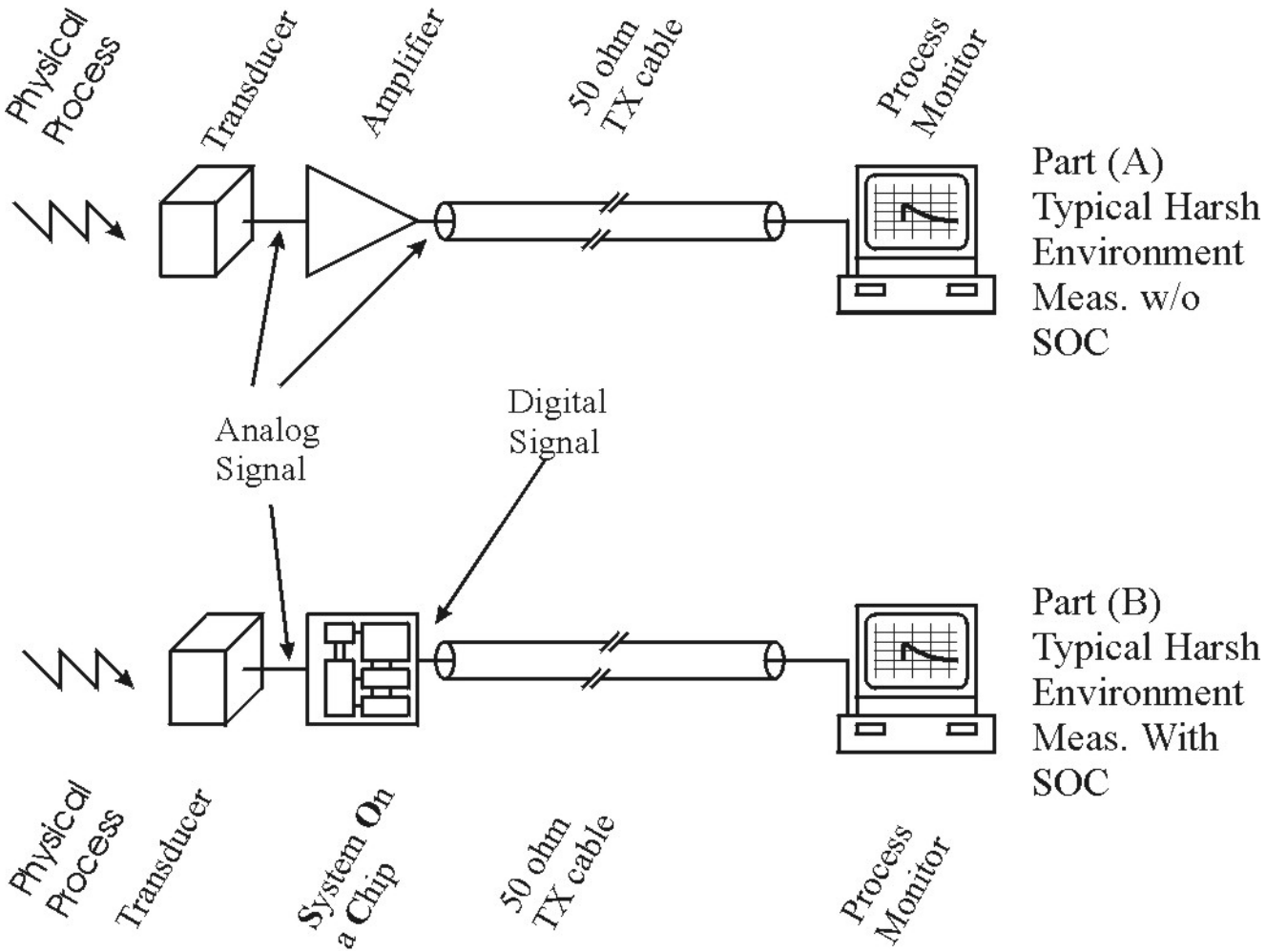

Figure 1.1: Two Examples of Harsh Environment Measurement Systems.
Part (a) shows how a harsh environment measurement may have been performed several years ago. Part (b) shows how a harsh environment measurement could be performed today using remote sensors.

different sensors onto a single channel, or low-power biological sensors that can operate autonomously inside the human body [6],[7].

1.1.2 General Architecture of a Remote Sensor

Figure 1.2 shows a block diagram of a typical remote sensor. As stated previously, the analog input is conditioned by analog signal processing circuits before being buffered to an ADC. The digital data goes to a DSP block for further processing, and is then sent to an RF transmitter. The RF block was not mentioned in the previous discussion, although it is becoming an increasingly important component in remote sensing systems. The purpose of the RF block is to modulate the data signal to a frequency well above baseband. If signals from several different sensors are modulated to different frequencies, then they can all be transmitted concurrently over the same channel, without significant interference from adjacent signals. Therefore, the purpose of the RF signal processing block is to better utilize the capacity of the channel, when transmitting several different signals.

A generalized block diagram of an RF transmitter is shown in Figure 1.3. It consists of a PLL frequency synthesizer for generating the proper carrier frequency. The mixer, which can be thought of as an analog multiplier, modulates the signal to RF. Finally the power amplifier drives the antenna or 50 ohm cable with the proper power level. A transmitter could contain more blocks, however almost all transmitters will contain this minimum set of blocks [8].

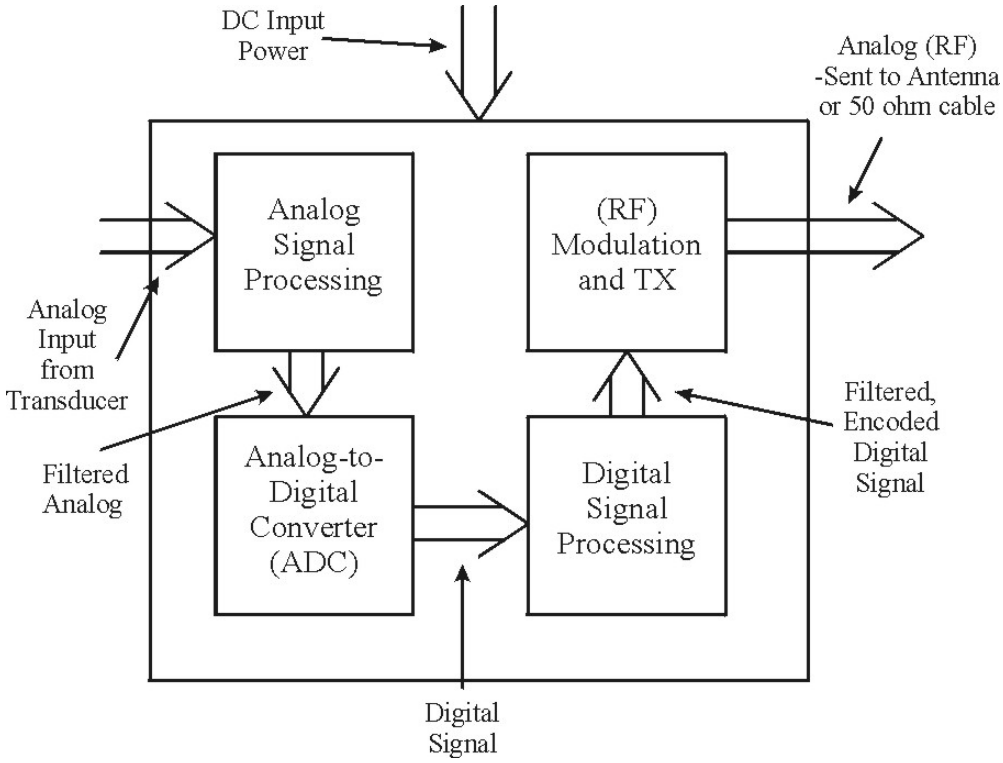

Figure 1.2: Top-Level Diagram of a Generic Remote Sensor.

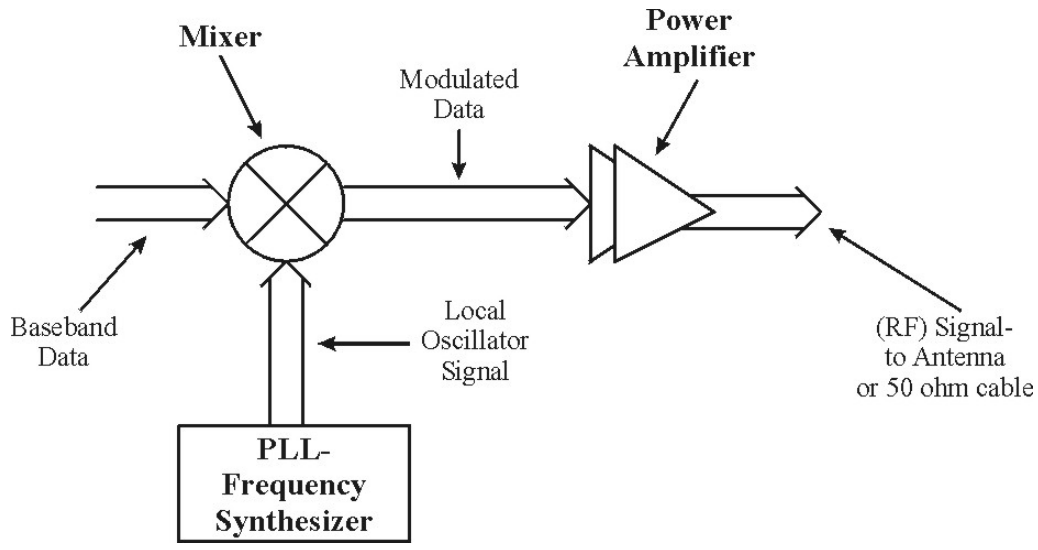

Figure 1.3: Block Diagram of a Simple RF Transmitter

1.2 Motivation

Since the current trend in IC technology is to bundle several different functions together on one chip, it would be highly desirable to have a single chip that performs all the functions shown in Figure 1.2. It has been very common in the past to have all of the analog and digital baseband signal processing performed on a single chip. However it is much more difficult to integrate the RF block with the baseband functions. The general reason for this is that traditionally the semiconductor technology used to realize the baseband functions did not have the performance necessary for the RF functions. Therefore a separate RF chip or discrete transistors were used for the RF blocks. The RF chip would be implemented in a more expensive, higher performance technology, such as Gallium Arsenide. In the past several years standard digital CMOS technology, which is used for a majority of the integrated circuits fabricated today, has become a viable

candidate for designing RF circuits [9]. Since RF circuits can now be realized in CMOS technology, it is possible to implement a complete remote sensor on a single Silicon chip.

While all of the RF functions shown in Figure 1.3 provide interesting and important design challenges, this thesis will focus on the power amplifier block. The traditional application of RF power amplifiers is high power radio transmitters. However high power operation is in direct conflict with the requirements of remote sensors. Remote sensors transmit at very low power levels because they are generally required to transmit over very short distances (e.g. from a harsh environment measurement to a monitoring station) and often operate from very limited power sources. Therefore this thesis will focus on the development of an RF power amplifier, which can operate efficiently at very low power levels. A power amplifier with these operating characteristics could be integrated into a remote sensor. Since harsh environment operation is an important characteristic of many remote sensors, the amplifier will be designed to operate over an extended temperature range.

1.3 Scope of Thesis

1.3.1 Power Amplifier Requirements

The purpose of this work is to design a power amplifier that can operate at very low power levels. Specifically, the amplifier should have an average output power of 0 dBm, at a frequency of 300 MHz. In addition, the amplifier needs to operate very efficiently, because energy is a precious resource for remote sensors. Finally, the amplifier needs to operate reliably up to a temperature of 200 degrees Celsius.

1.3.2 Literature Review

A thorough literature search has been performed for papers dealing with the design of integrated power amplifiers operating at relatively low power levels (1 Watt or less). Table 1.1 presents a summary of low power, high efficiency RF power amplifiers that were reported in the literature during the time period 1995 - 2002. One will immediately notice that the efficiencies reported were all in the range of 0.40 to 0.62. Several of the amplifiers also reported an efficiency for power levels closer to 0 dBm, however none of the amplifiers were optimized to operate at this power level and the efficiency was always lower than 20%. Also, none of the amplifiers were characterized over an extended temperature range.

Table 1.1: A Summary of High-Efficiency, Low Power RF Power Amplifiers

Reference	Architecture	P_{out} (dBm)	F (MHz)	Efficiency ()	Technology
[10]	Class - B	13	900	0.50	1-μm Bulk CMOS
[11]	Class - C	19	900	0.55	0.6-um Bulk CMOS
[12]	Class - C	30	1900	0.55	Silicon BJT
[13]	Class - E	24	835	0.50	0.8-μm GaAs
[14]	Class - E	30	1900	0.48	0.35-μm Bulk CMOS
[15]	Class - E	23	900	0.49	1.5-μm SOI CMOS
[16]	Class - E	29.5	900	0.41	0.25-μm CMOS
[17]	Class - E	30	700	0.62	0.35-μm Bulk CMOS
[18]	Class - F	23	1900	0.48	0.6-μm Bulk CMOS
[19]	Class - F	25	1400	0.43	0.25-μm Bulk CMOS

1.3.3 Contributions of Current Work

Since a high-efficiency power amplifier operating at very low power levels is a relatively novel concept, the design approach taken in this work is a very cautious one. A hybrid circuit has been designed with a transistor fabricated in a 0.5 micron CMOS technology acting as the power amplifier. Passive components are implemented off-chip so that the amplifier is as configurable as possible. Instead of relying on Spice simulations for the design, a great deal of hardware testing was used. This was done because it was uncertain how well Spice would be able to model all of the important RF effects.

There is no exact specification on how efficiently this amplifier must operate, nor on what degradation of performance is allowable over the specified temperature range. Instead the goal of this work is to pick an amplifier architecture that has promise for performing well; and fully characterize it in terms of efficiency, output power, and linearity over many combinations of drive signal, passive load components, frequency, and temperature. After the testing is performed many conclusions will be drawn as to how well the amplifier performed, and what changes could be made to improve its performance. It is hoped that this work will provide a good starting point for a designer who is developing an amplifier for which low power, high efficiency operation is required over an extended temperature range.

1.4 Organization of Thesis

Chapter two presents a review of RF power amplifier fundamentals. First a discussion of important power amplifier performance characteristics is given. Next power amplifier

types including A,B,C,D,E, and F are defined. Finally semiconductor technologies used for realizing RF power amplifiers are reviewed.

Chapter three presents an in-depth look at the design of high-efficiency low power amplifiers. First, the amplifier architectures presented in Chapter two are evaluated in terms of their ability to operate well at low power levels. It is shown that the Class E power amplifier is a good candidate for low-power operation. Next, the design of a Class E amplifier using first order theory is presented, and real world non-idealities are discussed. Finally an in-depth look at a Class E amplifier operating at very low power levels is given by examining the results of extensive hardware testing and characterization.

Chapter four presents a Class-E power amplifier design which has been optimized to operate at an average output power of 0 dBm. The design is based on the information gathered in chapter three. Measurement and simulation results are shown for the power amplifier.

Chapter five presents the conclusions for this work. The accomplishments of this thesis will be reviewed and suggestions for further work will be proposed.

Chapter 2

Power Amplifier Fundamentals

2.1 Introduction

Chapter two presents a review of power amplifier fundamentals. This discussion begins with a definition of a power amplifier, and then introduces several important power amplifier performance metrics and concepts. Section 2.3 discusses the current source power amplifiers, including classes A, B, and C. Section 2.4 discusses switch mode power amplifiers, including classes D, E, and F. Finally, chapter two concludes with a discussion of semiconductor technologies currently used for realizing RF power amplifiers.

2.2 Power Amplifier Performance Metrics

2.2.1 Definition of Power Amplifier

While one often encounters the term ‘power amplifier’ in engineering literature, it is very difficult to find a concise, universally accepted definition of a power amplifier. Therefore a definition will be given here, and it will be assumed that whenever the term is used in this text, it will fit the description given below. A definition of a small-signal amplifier will also be given, so that the two can be differentiated. Finally example waveforms of both power amplifiers and small signal amplifiers will be shown so that their differences can be more fully understood.

In this work a power amplifier will be regarded as an amplifier which has been optimized in terms of its ability to deliver power to a load in an efficient manner. In a power amplifier, output power and efficiency are optimized at the cost of reduced linearity. In fact, a defining characteristic of power amplifiers is that they will exhibit significantly more non-linearity than a small signal amplifier. Conversely a small signal amplifier is one which has been optimized in terms of its ability to operate linearly on an input signal. A direct consequence of the improved linearity of a small signal amplifier is that it operates with a relatively poor efficiency, and it must also operate 'backed-off' from its maximum possible output power. The fundamental trade-off between linearity and efficiency will become more evident as different power amplifier types are examined.

To better understand the concept of a power amplifier, consider the simple common source amplifier and waveforms shown in Figure 2.1. The curve on the top left of Figure 2.1 shows an idealized DC transfer characteristic of the NMOS common source amplifier. The curves on the bottom left represent a small signal and large signal input to the amplifier. The curves on the top right represent the corresponding small and large signal output. The small signal curve is representative of an input to a linear amplifier. Note that the signal swing is kept within the linear region of the gain curve, and therefore the output signal is a faithful replica of the input. A direct consequence of remaining in the linear gain region is that the power delivered to the load will be much less than the amplifier's maximum possible output power. Now consider the large signal input, which is representative of a power amplifier input. On the positive half of the swing the amplifier comes close to the cut-off region, and on the bottom half the amplifier comes close to the ohmic region. The large signal swing has caused the output signal to become flattened at

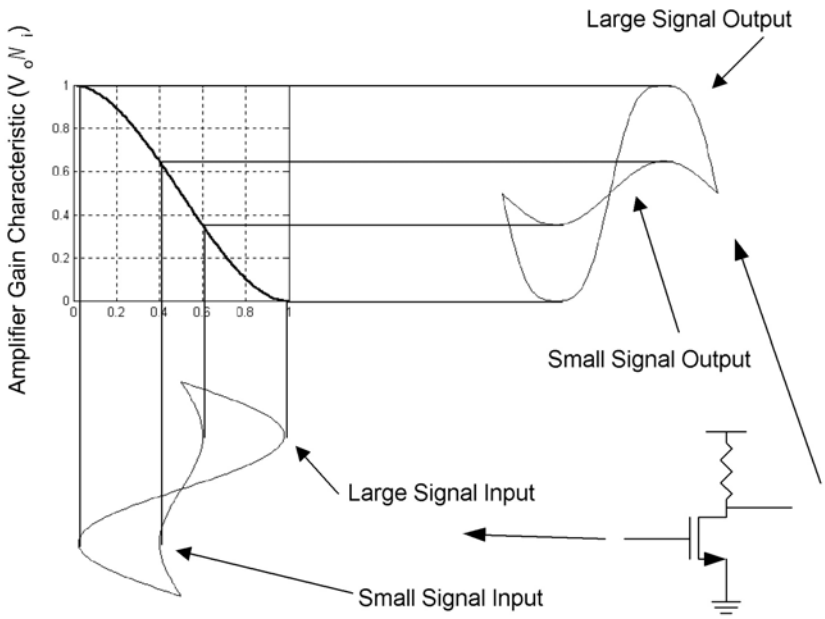

Figure 2.1: Small and Large Signal Amplifier Input-Output Signals

the top and bottom, indicating non-linearities. However, since the signal swings close to the rail the amplifier is delivering close to its maximum power.

Figure 2.1 shows the waveforms for only one class of power amplifiers, and is certainly not indicative of all power amplifiers. Although it does highlight a defining characteristic of power amplifiers, namely that output power and efficiency have been traded for linearity. Optimizing the trade-off between output power, efficiency and linearity is a recurring theme in power amplifier design.

2.2.2 Efficiency and Gain

2.2.2.1 Power

Efficiency and gain are two important power amplifier performance metrics. Efficiency describes how well an amplifier converts DC input power to RF output power. Gain refers to how well an amplifier converts input RF power to output RF power. However, before these quantities can be rigorously defined, the concept of power must be discussed.

Power is defined as the time derivative of energy. It can also be thought of as the instantaneous energy dissipated in a load. Using familiar electrical quantities, the power delivered to a load is given by the product of the voltage and current. The left hand curves in Figure 2.2 show a plot of the power and energy dissipated in a resistor versus time for a DC source. Since the power is constant versus time, the energy dissipated in the load starting at time t = t_0 and ending at time *t* is given by

$$E = \int_{t_0}^{t} P(t)dt = P(t - t_0) \qquad 2.1$$

Now consider a load that is driven by a sinusoidal voltage source. The power and energy dissipated in the load resistor versus time are shown in the right hand curves of Figure 2.2 for this case. Note that the power dissipated in the resistor could be characterized in terms of its average, rms, peak, or instantaneous value. However the sinusoidal power needs to be defined in such a way that it can be compared directly to DC power for efficiency calculations. Therefore RF power must be characterized in terms of its average power. The reason for this is that average power is equal to the net power delivered to a load over one RF cycle [20]. In other words, average RF power is directly proportional to

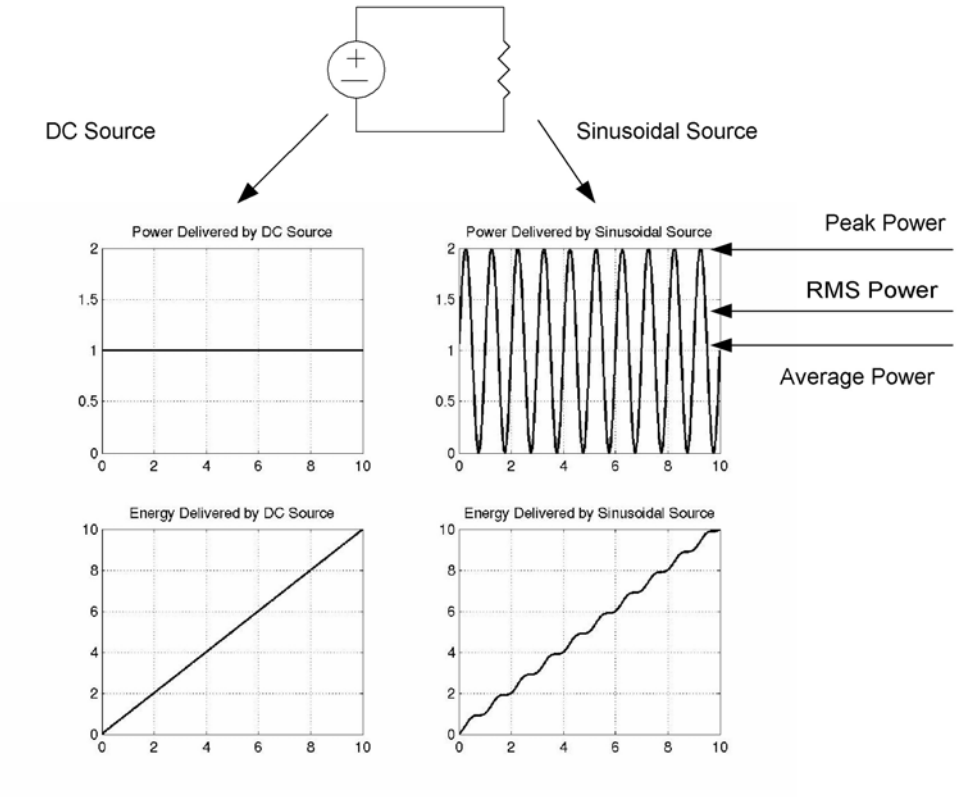

Figure 2.2: Power and Energy Dissipated in a Resistive Load versus Time

the energy delivered to the load. The energy delivered to a load from an AC source is given by

$$E = \int_{t_0}^{t} P(t)dt = P_{AV}(t - t_0) \qquad 2.2$$

Since both DC power and average sinusoidal power are directly related to energy, they will be used when calculating efficiencies. Unless otherwise stated, it can be assumed that whenever sinusoidal power is discussed, the discussion refers to average power.

2.2.2.2 Drain Efficiency and Power Gain

One important characteristic of a power amplifier is how well it converts DC supply power to RF output power. This is referred to as the DC-to-RF power conversion efficiency, and is often referred to as simply the drain efficiency. Drain efficiency is defined mathematically as the ratio of the average RF output power to DC input power or [21]

$$DE = \eta = \frac{P_{OUT, RF}}{P_{IN, DC}} \tag{2.3}$$

While drain efficiency describes the DC-to-RF conversion, power gain (G) describes the amplifiers conversion of RF input power to RF output power. Power gain is defined as the ratio of the average RF output power to the average RF input power

$$G = \frac{P_{OUT, RF}}{P_{IN, RF}} \tag{2.4}$$

2.2.2.3 Power Added Efficiency

One of the most important differences between designing RF circuits and baseband circuits is the great difficulty in developing power gain at RF. Amplifiers operating at very low frequencies generally use very high input impedances to limit the input current, therefore gain is generally characterized in terms of a voltage gain and the power required to drive the amplifier is simply ignored. However an RF designer does not have the luxury of high impedances, therefore an amplifier could have a significant input current and the power used to drive the device must be taken into account.

Since power gain is so critical at RF, it would be helpful to define a quantity which accounts for an amplifier's drain efficiency and power gain. This is needed so that a distinction can be made between an amplifier with a drain efficiency of 0.9 and a gain of 2 dB and an amplifier with a drain efficiency of 0.5 and gain of 15 dB. The quantity which characterizes an amplifier's drain efficiency and power gain is known as the power added efficiency (PAE). PAE is defined as the RF output power minus the RF input power divided by the DC supply power [21]

$$PAE = \frac{P_{OUT,RF} - P_{IN,RF}}{P_{IN,DC}} \quad 2.5$$

After rearranging Equation 2.5, it can be written as

$$PAE = DE(1 - 1/G) \quad 2.6$$

Equation 2.6 clearly shows the dependence of PAE on drain efficiency and gain. Note that as the gain becomes very large, the power added efficiency approaches the drain efficiency.

2.2.3 Linearity

2.2.3.1 Characterizing Linearity

Linearity is another extremely important amplifier performance characteristic, especially when the amplifier must process variable envelope signals. However, as discussed in Section 2.2.1, all power amplifiers will exhibit non-linearites to some degree. In power

amplifier design one must design for the maximum allowable non-linearity, so that efficiency can be maximized. Since non-linearity is an important part of power amplifier design, it is important to understand and quantify it. Therefore this section will discuss two methods of quantifying the non-linearity of an amplifier, gain compression and distortion.

2.2.3.2 Gain Compression

Gain compression refers to an amplifiers deviation from its ideal linear gain curve. Amplifiers are often characterized in terms of their 1-dB gain compression point. The 1-dB compression point is the point of the input-output transfer characteristic where the actual gain is 1-dB below the ideal linear gain [22]. The 1-dB compression point represents an arbitrary upper limit of input signal for which the amplifier will still approximate linear operation. This condition is clearly shown in Figure 2.3.

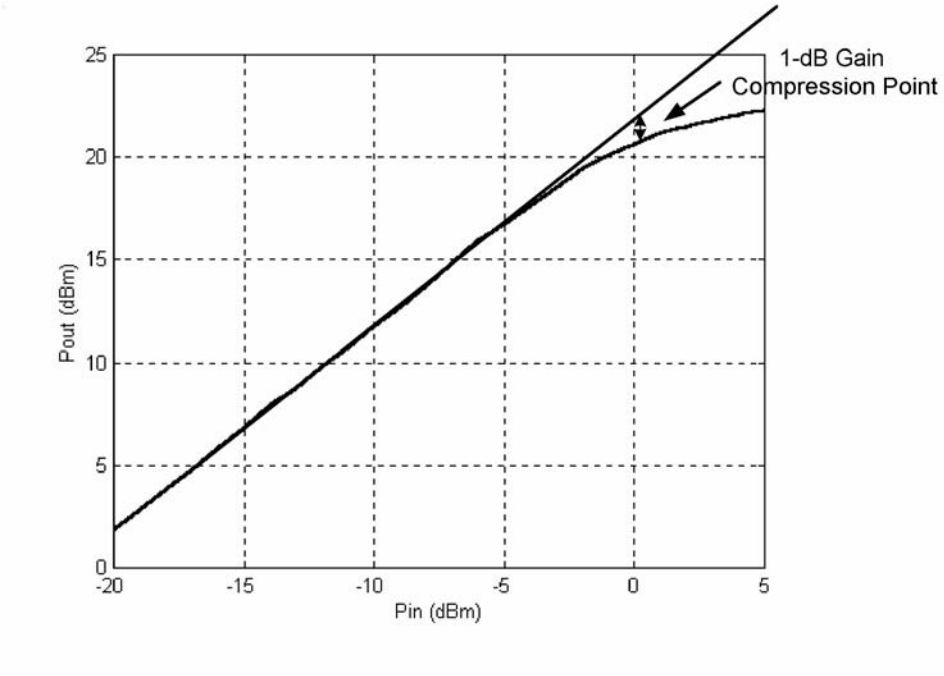

Figure 2.3: Pout v. Pin for a Generic Linear Amplifier
This plot clearly shows the 1-dB Compression Point

2.2.3.3 Total Harmonic Distortion

Since it may be desirable to operate a power amplifier with significant non-linearities (so that output power and efficiency can be maximized), it is important to quantify the effect of the non-linearities on the output signal. A very common method of characterizing an amplifiers non-linearity is total harmonic distortion (THD). To understand how non-linearities affect an amplifier's output and what THD is, first consider the general transfer function of an amplifier shown in Equation 2.7 [22].

$$V_{OUT} = \sum_{n=0}^{\infty} a_n (V_{IN})^n \tag{2.7}$$

If the input to the amplifier is a single tone, then the output will be of the form

$$V_{OUT} = a_0 + a_1 \cos(\omega_0 t) + a_2 \cos(\omega_0 t)^2 + a_3 \cos(\omega_0 t)^3 + \ldots \tag{2.8}$$

It is well known that raising a cosine of frequency ω_0 to a power *n* will create a harmonic at a frequency $n\omega_0$ plus other spectral components. Therefore the degree of non-linearity of an amplifier can be characterized by examining the spectral components in the output signal, when the input is driven by a 'clean' sine wave. This test is the basis for the measurement of THD which is defined as [23]

$$THD = \frac{\sum P_{Harmonics}}{P_{Fundamental}} \tag{2.9}$$

where $P_{Harmonics}$ is the total harmonic signal power and $P_{Fundamental}$ is the total fundamental signal power. As defined in Equation 2.9, THD is dimensionless, however

THD is often reported in dB. In this case THD is defined as

$$THD(dB) = -10\log\left(\frac{\sum P_{Harmonics}}{P_{Fundamental}}\right) \quad 2.10$$

Note that in the definition given in Equation 2.10 a large value (in dB) corresponds to a low distortion.

Finally, in a power amplifier the largest harmonic is generally the second [24], therefore a distortion metric known as 2^{nd} harmonic distortion will be defined as

$$2HD = \frac{P_{2^{nd}Harmonic}}{P_{Fundamental}} \quad 2.11$$

Second harmonic distortion will allow a quick determination of how much distortion is being caused by the second harmonic component of the signal.

2.3 Current Source Power Amplifiers

2.3.1 Introduction to Current Source Power Amplifiers

When an amplifying device operates only in saturation and cutoff (assuming an FET amplifier), it is said to be a current source power amplifier. The power amplifiers that fit this description are the Class A, Class B, Class AB, and Class C. This section will first discuss a circuit topology that can realize all of the above amplifiers. Next each of the amplifier types will be introduced and discussed.

Figure 2.4 shows a circuit topology that can be used to realize any current source power amplifier [25]. The amplifier is connected in a common source configuration because this yields the highest efficiency of the common amplifier configurations. The drain bias is brought to the amplifier using an RF choke. The RF choke essentially acts as a nearly ideal DC current source, it dissipates only nominal power and it can withstand positive and negative voltages. Finally the output signal is AC coupled into a resonant tank. The purpose of the tank is to reduce the harmonics that will be present in the output signal. Figure 2.4 also shows the important voltage and current waveforms associated with this amplifier. Several important current source power amplifier characteristics can be seen by examining these waveforms. First, the average and peak value of the signal V_{in} will set

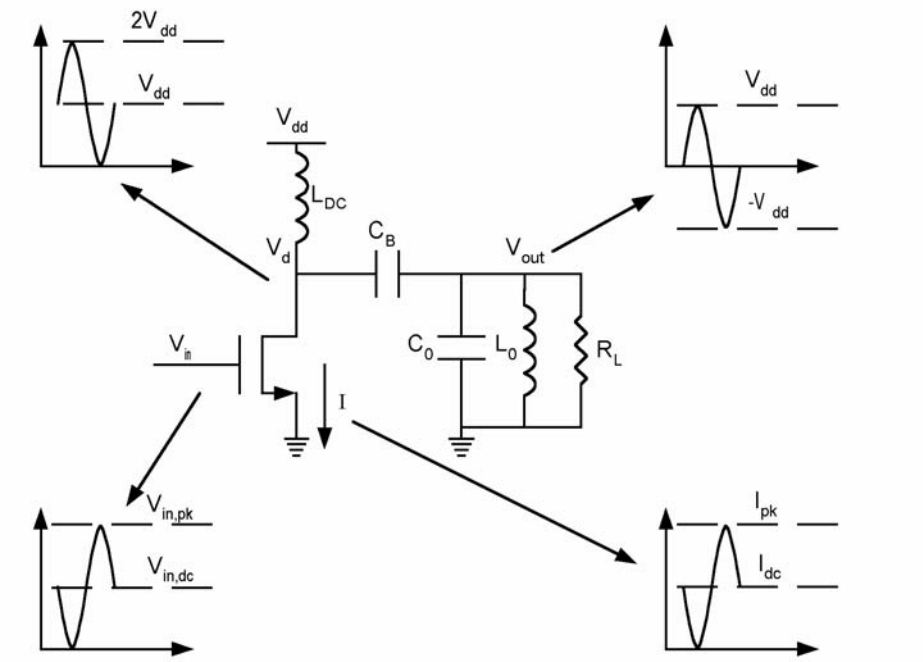

Figure 2.4: Basic Topology for a Current Source Power Amplifier

the conduction angle of the amplifier. The conduction angle is defined as

$$Conduction\angle = 360^{\circ}\left(\frac{T_{ON}}{T_{RF}}\right) \quad 2.12$$

where T_{ON} is the time which the active device conducts current, and T_{RF} is the period of the RF cycle. The conduction angle can be increased or decreased by simply increasing or decreasing the average and/or the peak value of the input signal. The conduction angle is 360 degrees for this case, as evidenced by the transistor current waveform. Next one will notice that the drain voltage swings above and below the power supply voltage. Although this might be a bit disconcerting at first, one can see that this must be the case because the inductor L_{DC} will have (ideally) zero voltage drop; therefore an AC signal on the drain must have a mean value of V_{dd}. Finally the output voltage has no DC offset because of the blocking capacitor.

2.3.2 Description of Current Source Power Amplifier Types

2.3.2.1 Class A Power Amplifier

The term class A amplifier is ubiquitous in analog design, and it is often used interchangeably with the term linear amplifier. Actually, a class A power amplifier is one in which the transistor conducts current for the full 360 degrees of the input cycle, and is not necessarily linear [24]. As discussed previously, a class A power amplifier will exhibit non-linearities because it must sustain a large voltage and current swing. The transistor voltage and current waveforms for a Class A amplifier are shown in Figure 2.5.

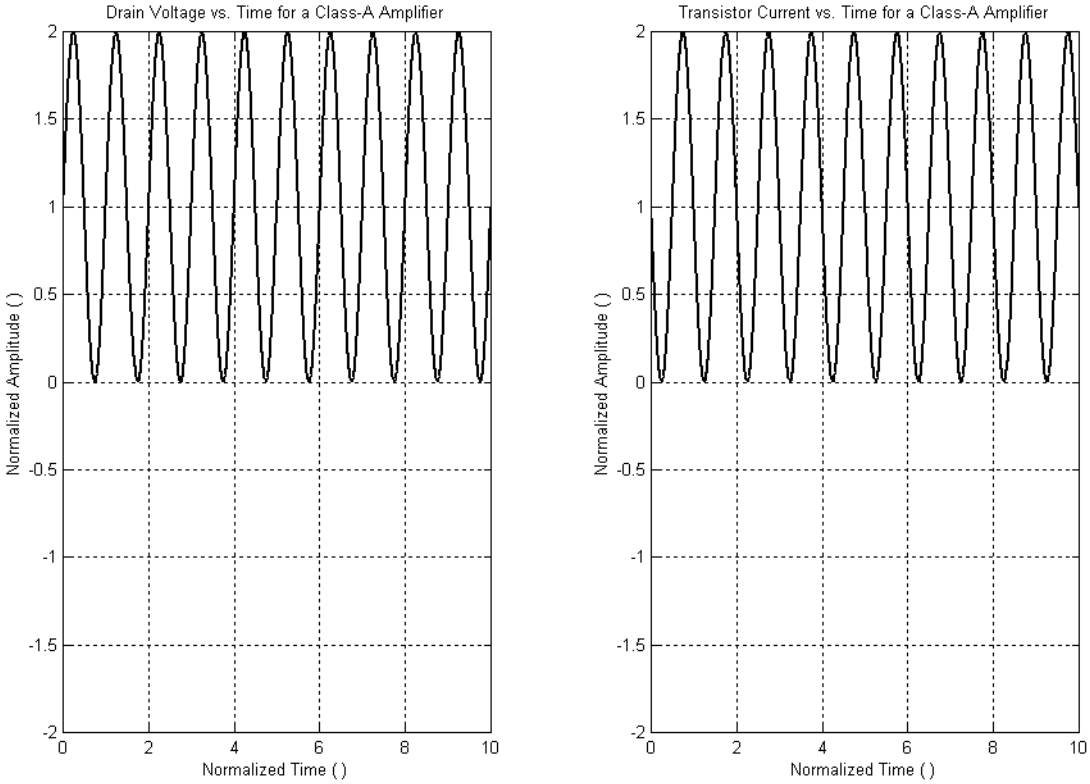

Figure 2.5: Class-A Amplifier Waveforms

The best case efficiency of the class A amplifier can be calculated by noting that the maximum efficiency will occur when the drain voltage swings from 0 to $2V_{dd}$. The input power for this case is

$$P_{in,dc} = V_{dd} I_{dd} = \frac{V^2_{dd}}{R_L} \quad 2.13$$

and the output power is

$$P_{out,RF} = \frac{V^2_{dd}}{2R_L} \quad 2.14$$

Finally the drain efficiency, as defined in Equation 2.3, is given by

$$DE = \frac{V^2_{dd}/R_L}{V^2_{dd}/2R_L} = \frac{1}{2} \quad 2.15$$

2.3.2.2 Class B Power Amplifier

The main limitation of the class A amplifier is that, due to its 360 degree conduction angle, the active device dissipates significant power compared to the peak RF output power. The power dissipation can be reduced by biasing the active device such that it conducts current for less than a full RF cycle. In other words the device is driven into cutoff for some portion of the RF cycle. When a device is biased as a Class B power amplifier it conducts current for only one-half of the RF cycle. Obviously the current will have significant spectral content at frequencies other than the fundamental. However the tank circuit loading the amplifier will help to reduce the harmonics to an acceptable level. The drain voltage and current waveforms for a Class B amplifier are shown in Figure 2.6.

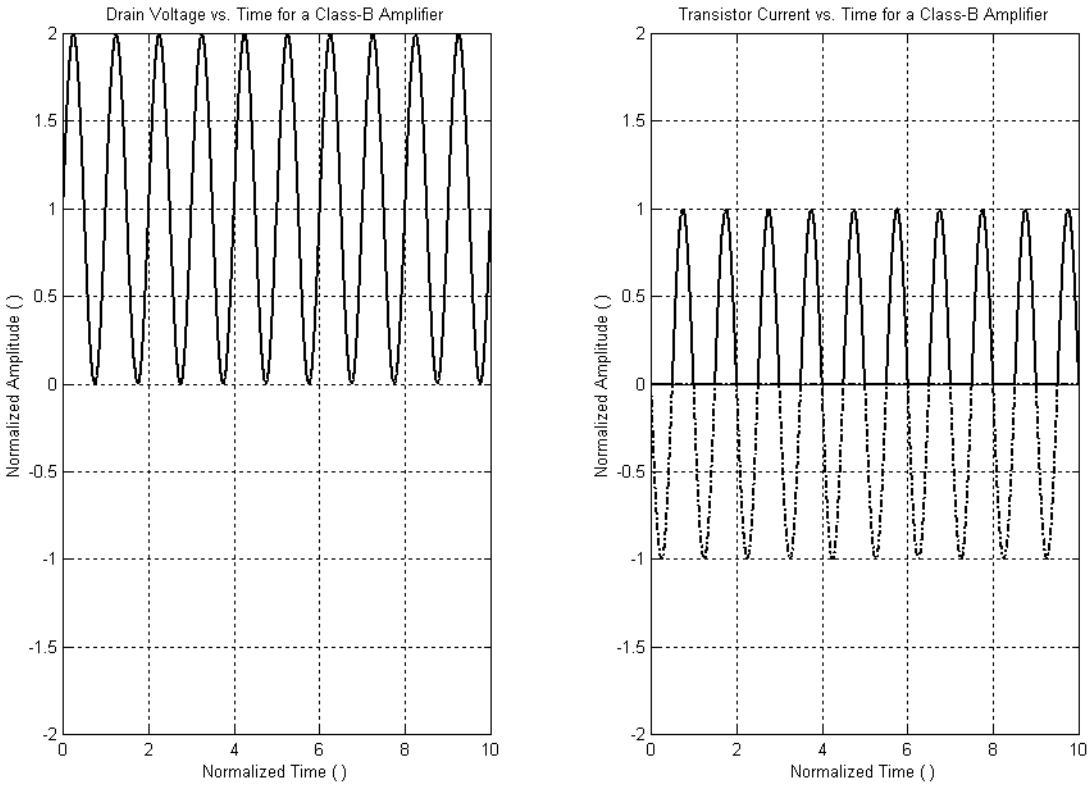

Figure 2.6: Class-B Power Amplifier Waveforms

One can see that the drain current is now only half of a sine wave. The negative half of the sine wave that is shown in dotted lines is only to highlight the portion of the signal that has been cutoff. The drain efficiency of the Class B power amplifier can be calculated by noting that the maximum output power is the same as for the Class A amplifier and is given in Equation 2.14.

The DC bias current can be found as the average value over one RF cycle of one half of a sine-wave

$$I_{dd} = \frac{1}{T_0}\int_0^{T_0/2} \sin\left(\frac{2\pi}{T_0}\cdot t\right)dt = \frac{2}{\pi}\frac{V_{dd}}{R_L} \qquad 2.16$$

and the drain efficiency can be calculated as

$$DE = \frac{V^2_{dd}/(2R_L)}{2(V^2_{dd}/(\pi R_L))} = \frac{\pi}{4} \cong 0.785 \qquad 2.17$$

2.3.2.3 Class A-B Power Amplifier

The class B power amplifier trades efficiency for linearity. However it may desirable to have an amplifier with better efficiency than the class A amplifier, and better linearity than the class B amplifier. The amplifier which meets these specifications is the class A-B amplifier. The class A-B amplifier operates with a conduction angle somewhere between 180 and 360 degrees. The efficiency of the class A-B amplifier will lie somewhere between 0.5 and 0.785. The Class A-B waveforms are shown in Figure 2.7. In this instance the conduction is roughly halfway in between Class A mode and Class B mode.

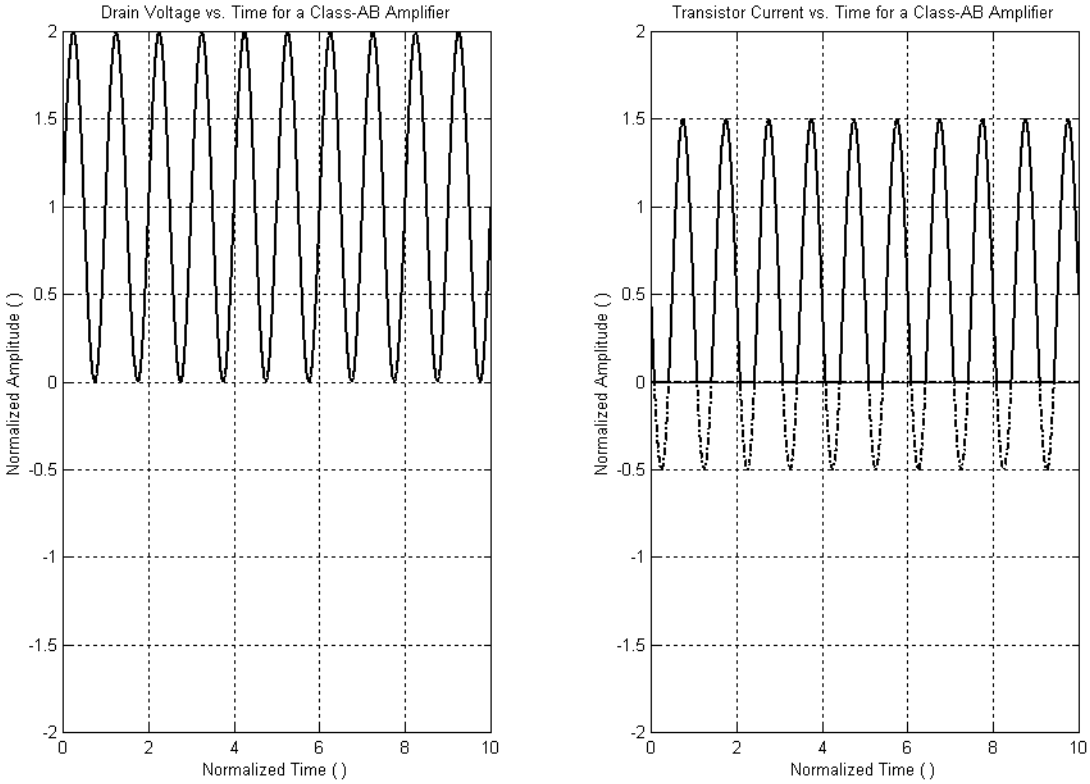

Figure 2.7: Class A-B Power Amplifier Waveforms

2.3.2.4 Class C Power Amplifier

The previously described power amplifiers can all be used as linear amplifiers in narrowband applications. However often in RF systems, a linear amplifier is not required (e.g. when constant envelope modulation is used) [26]. In these instances a Class C amplifier can be used to achieve very high efficiencies. A Class C amplifier has a conduction angle less than 180 degrees, and can achieve efficiencies greater than the Class B amplifier. The transistor drain current and drain voltage waveforms for an amplifier operating in Class C more are shown in Figure 2.8.

The theoretical maximum efficiency of the Class C amplifier is a function of the conduction angle and is given by [26]

$$\eta_{max} = \frac{2y - \sin 2y}{4(\sin y - y\cos y)} \qquad 2.18$$

Likewise the output power which corresponds to the maximum efficiency condition is given by [26]

$$P_{max} = \frac{2y - \sin 2y}{8\pi(1 - \cos y)} \qquad 2.19$$

It is interesting to note that when an amplifier is operated in Class-C mode the efficiency can be increased arbitrarily towards unity, however the output power will also decrease towards zero. The parameter *y* is equal to the conduction angle expressed as a percentage of the RF period.

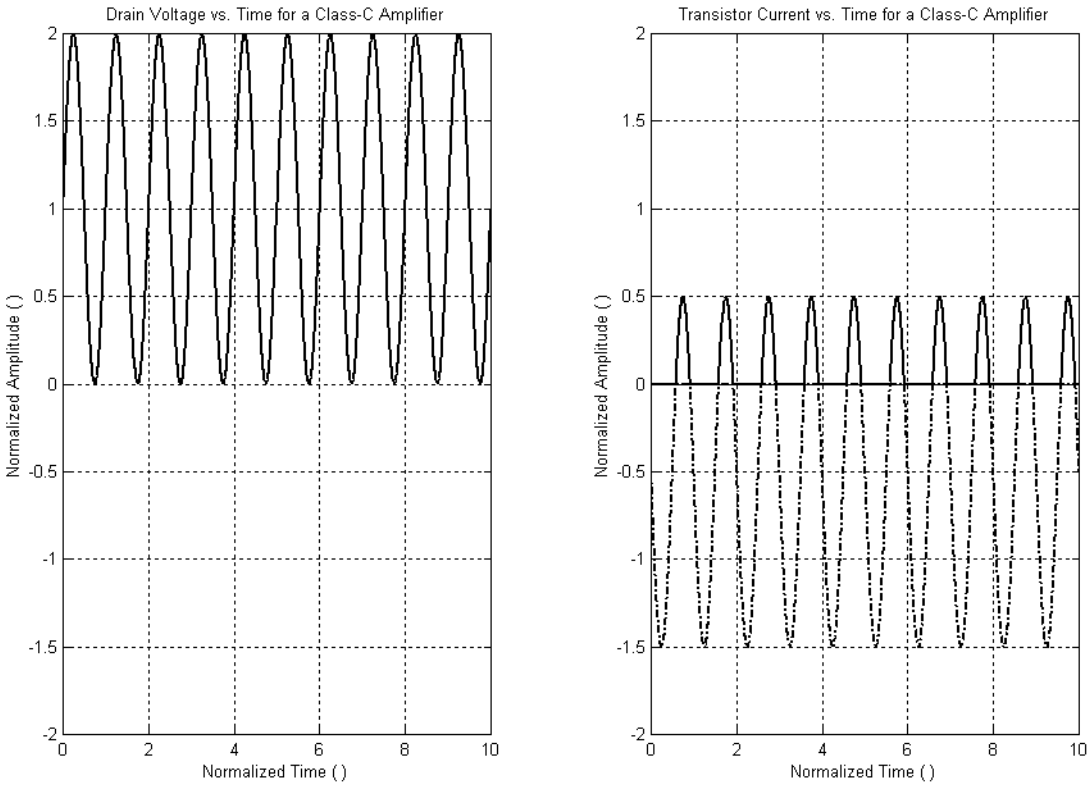

Figure 2.8: Class C Power Amplifier Waveforms

2.4 Switch Mode Power Amplifiers

2.4.1 Introduction

The fundamental limitation of current source power amplifiers is that the active device must always dissipate some power, therefore an efficiency of 100% can never be achieved. Switch mode power amplifiers circumvent this problem by employing a switch as the amplifying device. If the switch is ideal, that is zero switching time, zero on resistance, infinite off resistance; then an efficiency of 100% is theoretically possible.

Section 2.4 will first review some important switch mode power amplifier concepts and three switch mode amplifier topologies will be discussed; Class D, Class E, and Class F.

2.4.2 Important Concepts

2.4.2.1 Switch Non-Idealities

Section 2.4.1 stated that if a switch has zero switching time, zero on resistance, and infinite off resistance then efficiencies of 100% are theoretically possible. However in the real world, a switch must be implemented with a transistor that exhibits several deviations from the ideal case. The two most important non-idealities are that the switch will have non-zero on resistance and non-zero switching time.

Non-zero on resistance hurts the performance of a switch mode power amplifier because some of the DC supply power will be dissipated in this resistance, thus lowering efficiency. Assuming an FET is used to implement the switch function, the only way to reduce the on resistance, for a given semiconductor technology and input drive, is to make the switch larger. However as the size of the device increases so do the intrinsic

and extrinsic device capacitances, which slow down switching speed. A non zero switching speed reduces efficiency because when the device is switching it generally has non zero switch voltage and current, thus it dissipates power and efficiency is reduced.

The speed/on resistance trade off has generally limited the useful frequency range of switch mode power amplifiers to operation below 100 MHz. However the Class E and Class F power amplifiers both use tuned load networks to shape the switch voltage and current waveforms and achieve very high efficiencies at RF. Successful Class E and Class F designs have been reported at operating frequencies above 1 GHz.

2.4.2.2 Hard- and Soft- Switching

While it is true that if an ideal switch is used in a power amplifier an efficiency of 100% is theoretically possible, it is not certainly not guaranteed. The reason for this is what is known as “hard-switching” and “soft-switching.” To better understand these terms consider the simple switch mode power amplifier shown in Figure 2.9. This circuit is a simplified model of a switch mode power amplifier. In this model the switch is assumed ideal, note that the plot at the upper right of this figure shows the switch voltage as a function of time. First consider what would happen if the switch were to close at the instant T_1. At this instant in time the capacitor has a certain amount of stored energy equal to

$$E = \frac{1}{2} C_{SHUNT} V_D^2 \qquad 2.20$$

This energy was transferred to the capacitor from the power supply while the switch was

open. If the switch is closed at time T_1, then the charge stored on the capacitor will be shorted to ground and the energy will be simply wasted. Therefore even though the switch is ideal the efficiency will be less than 100%. This is known as hard-switching.

Now consider what would happen if the switch closed at time T_2. At this point the capacitor has been fully discharged, in other words all of the energy stored in the capacitor has been delivered to the load. Therefore it is possible under these conditions to achieve an efficiency of 100%. This condition is known as “soft-switching.”

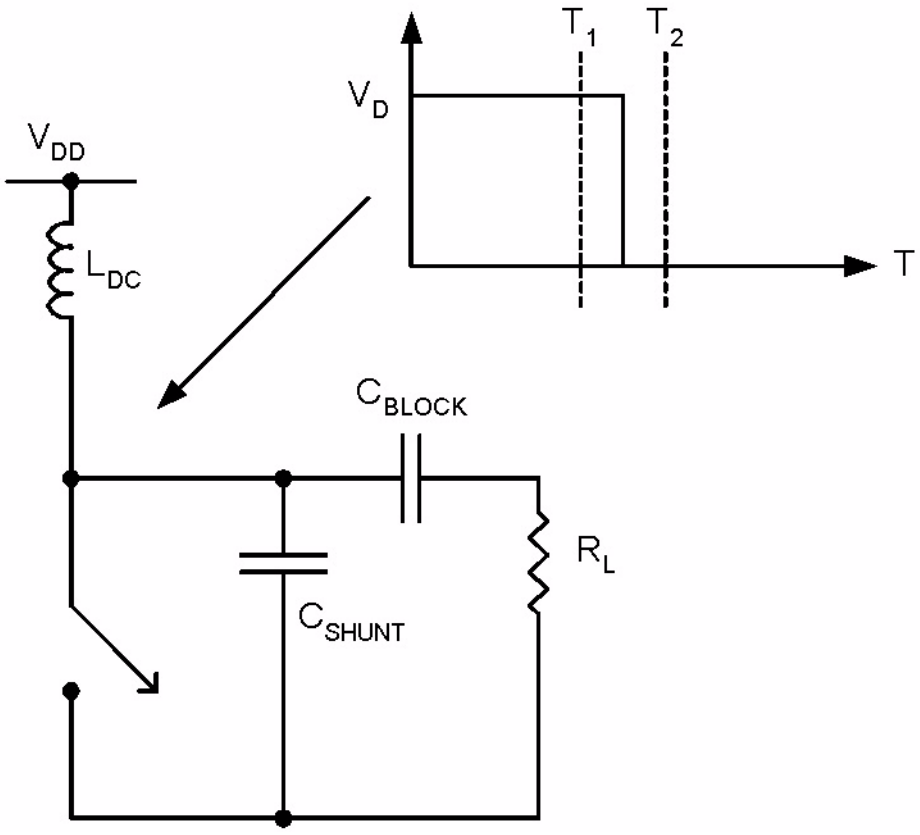

Figure 2.9: Simplified Model of a Switch-Mode Power Amplifier

2.4.2.3 Drain Modulation

One might question the use of the term “amplifier” for the switch-mode power amplifiers because the amplitude of the output signal has no relation to the amplitude of the input signal. In fact they could also be referred as power converters as their operation is very similar to that of a DC-DC power converter. However it is possible to use a switch-mode power amplifier in an application requiring linearity by using a technique known as ‘drain modulation’. In a switch-mode power amplifier the only voltage that determines the output power is the power supply voltage and the output power is always proportional to the square of the power supply voltage if the amplifier is operating correctly.

$$P_{OUT} \propto V_{DD}^2 \tag{2.21}$$

Therefore the output voltage of the power amplifier can be linearly modulated by varying the drain bias. This technique applies equally well to the Class D, E, and F amplifiers and can also be used with the Class C amplifier.

2.4.3 Description of Switch Mode Power Amplifier Types

2.4.3.1 Class D Power Amplifier

The Class D power amplifier is the most straight forward implementation of a switch mode power amplifier, and it is based on the design of a DC-DC power converter. Figure 2.10 shows one topology for realizing a Class D amplifier and the associated voltage and current waveforms. This amplifier uses an inductive current source as in the current source power amplifiers. The switch toggles between points *A* and *B* with a 50% duty cycle. The output is a series resonant tank tuned to the switching frequency and the load

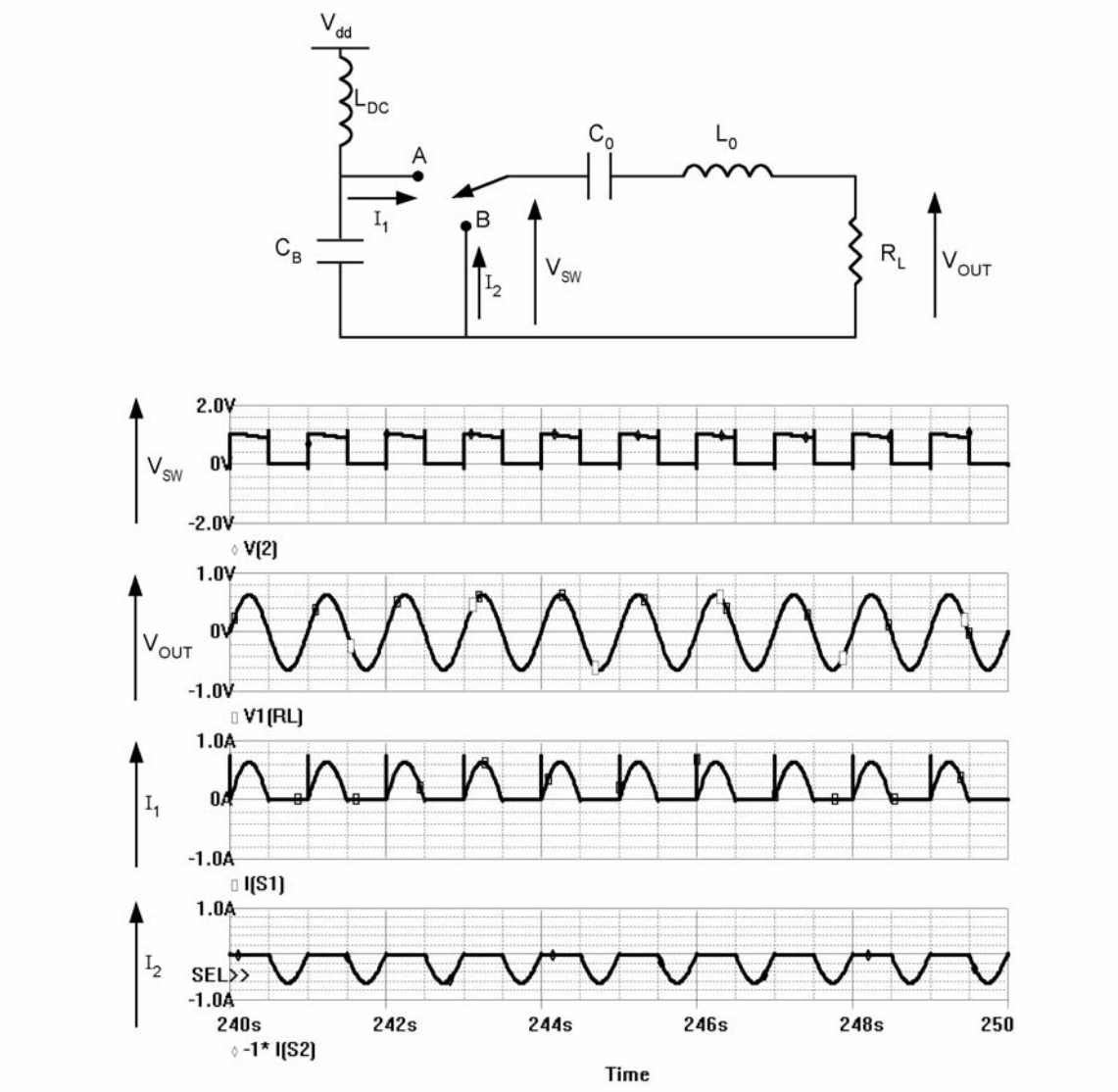

Figure 2.10: Class D Power Amplifier and Associated Waveforms

resistor could represent a 50 ohm load or the input of a matching network. One can see that the switch voltage has a 50% duty cycle and the risetime is a small fraction of the signal cycle. The output voltage is a very clean sinusoid due to the filtering of the L_0-C_0 tank. In this implementation the current I_1 represents the positive half of the load current and I_2 is the negative half of the load current.

Class D power amplifiers have been utilized extensively in applications ranging from audio frequencies to tens of MHz. The Class S amplifier, a variant of the Class D that uses the same topology but is driven with a pulse width modulated (PWM) signal, finds wide application in highly linear audio amplifiers. However the limitations discussed previously, namely switch on resistance and slow switching speeds and hard-switching, has limited the use of Class D amplification at the higher RF frequencies (>100MHz).

2.4.3.2 Class E Power Amplifier

The Class E power amplifier was invented by the Sokals in 1975 and it presents a clever means of guaranteeing soft-switching [27],[28]. There is no single topology that must be used to realize a Class E amplifier, instead the Class E amplifier is defined by the following conditions:

- The rise of the voltage across the transistor at turn-off should be delayed until after the transistor is off.
- The drain voltage should be brought back to zero at the time of transistor turn-on.
- The slope of the drain voltage should be zero at the time of turn-on.

The first statement guarantees that there is zero current in the transistor before the voltage starts to rise. The second statement is another way of stating that soft-switching will be employed. The third statement accounts for any non-idealities or any other timing-errors in the switching cycle.

A simple implementation of a Class E amplifier and the equivalent circuit when the switch is opened and closed is shown in Figure 2.11. In the circuit shown in Figure 2.11 it is assumed that the switch is ideal. The operation of the Class E amplifier is determined by the switch when the switch is closed, and by the load network when the switch is open. As one can see, when the switch is closed the equivalent circuit consists of only the inductor and the power supply voltage source. During this time the power supply is transferring energy to the inductor. When the switch opens the response of the amplifier is determined by the initial condition on the inductor and the quality factor of the load network. The operating waveforms for the Class E amplifier shown in Figure 2.11 are presented in Figure 2.12.

One of the main advantages of the Class E amplifier is that any parasitic capacitance at the drain of the active device can be absorbed into the shunt capacitance C_B. Since a ‘slow’ transistor switch can be modeled as an ideal switch with a capacitance connected to the drain node, any parasitic capacitance at the drain will become a design parameter and will thus not represent a parasitic component. Figure 2.12 also shows one of the major limitations of the Class E amplifier. In the simulation shown in Figure 2.12 the power supply voltage was 1.0V and the switch voltage swings to approximately 3.6V.

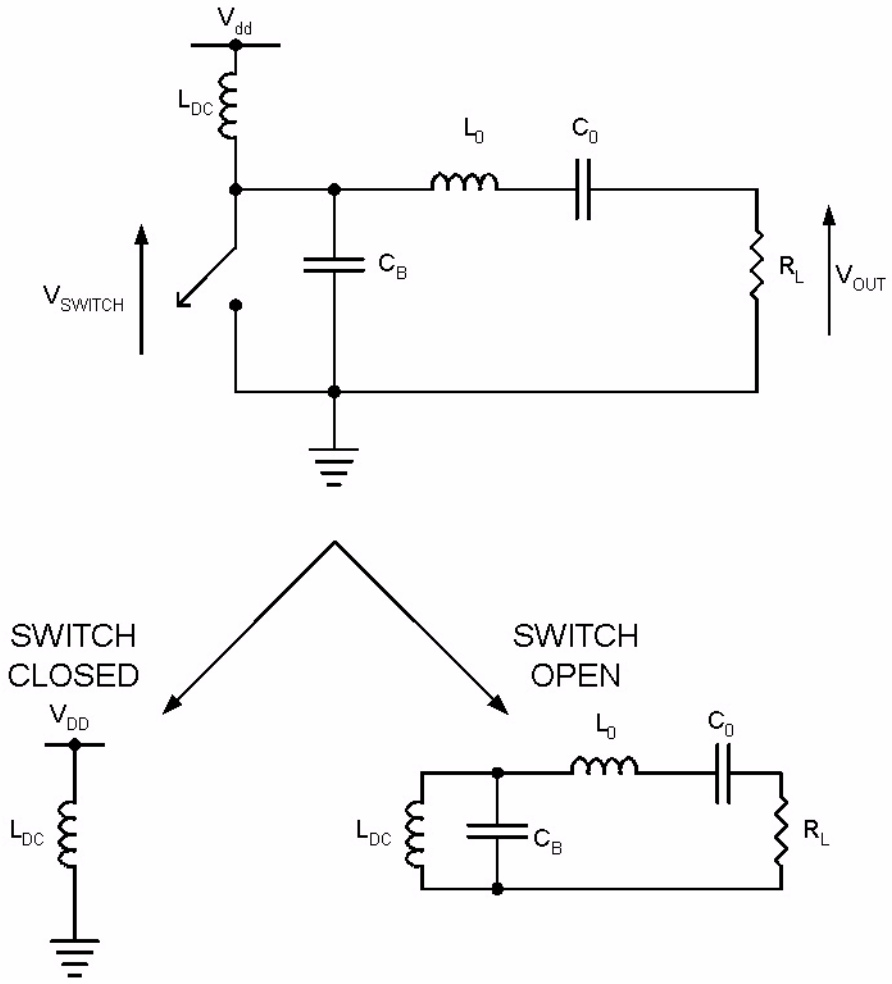

Figure 2.11: Class E Amplifier and Equivalent Circuit for Switch Opened and Closed.

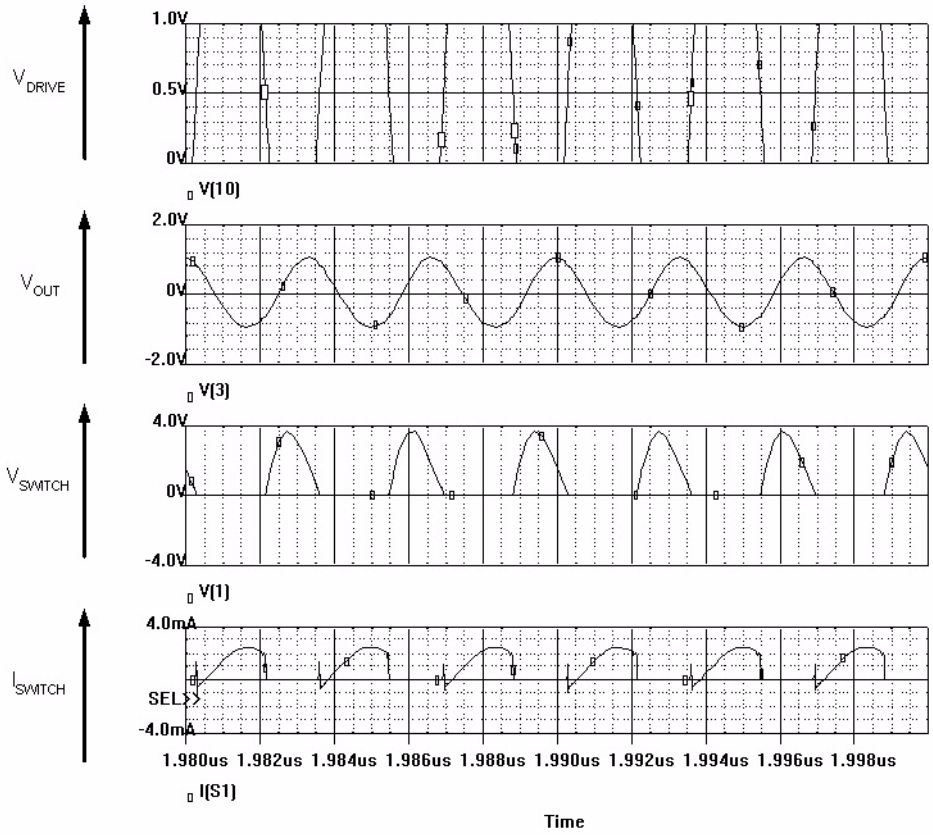

Figure 2.12: Class E Amplifier Operating Waveforms

When a Class E amplifier is operating at its maximum efficiency the peak switch voltage will be approximately 3.6 times the supply voltage.

2.4.3.3 Class F Power Amplifier

The Class F amplifier also uses a tuned load network to shape the switch voltage and current waveforms. Figure 2.13 below shows the schematic and the associated waveforms of the Class F amplifier. The load network in the Class F amplifier consists of a 1/4 wave transmission line (at the fundamental) and a parallel RLC circuit tuned to the fundamental frequency. The transmission line acts as a quarter wave transformer to the fundamental signal component according to the equation

$$Z_{IN} = \frac{Z_0^2}{Z_L} \qquad 2.22$$

The tank will have an impedance of Z_0 at the frequency f_0, therefore the impedance at the switch will simply be a real impedance Z_0. At every even harmonic the transmission line acts as a short circuit. Therefore the impedance seen by the switch will be zero, and the switch voltage will contain no even harmonics, however the switch current will contain even harmonic components. At every odd harmonic the transmission line appears as a quarter wave transformer and Equation 2.22 still holds. However the load impedance is now a short circuit because of the tank, so the switch sees an open circuit at every odd harmonic. Therefore the switch voltage will have odd harmonic components, but there will be no odd harmonic currents because of the infinite impedance seen by the switch. Since the switch in a Class F amplifier has even harmonic current and odd harmonic voltages,

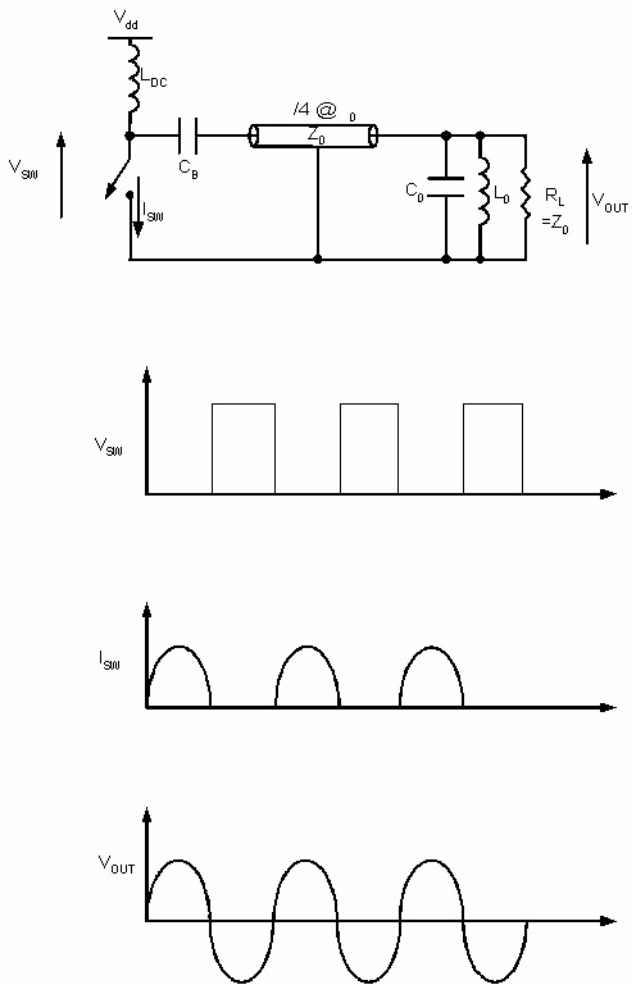

Figure 2.13: Class F Amplifier and Operating Waveforms.

and since the harmonics are orthogonal, the switch will ideally dissipate zero power and therefore very high efficiencies are possible.

2.5 Semiconductor Technologies for RF Power Amplifiers

2.5.1 Overview of RF Technologies

There are several semiconductor technologies which are currently very popular for realizing RF circuits. Among these are Silicon bulk CMOS, Silicon SOI CMOS, Silicon BJT, SiGe HBT, and GaAs. Of those just listed, only bulk CMOS and SOI CMOS were considered for this project. Other technologies were not considered because they were considerably more expensive and more difficult to obtain than the CMOS technologies.

The major factors affecting the choice of a semiconductor technology for implementing an RF power amplifier are speed, breakdown voltage, and cost. Depending on the application other factors might also be important. Since this application requires an amplifier that can operate over an extended temperature range, the ability for the technology to perform well at high temperatures is also critically important.

2.5.2 RF CMOS Technologies

2.5.2.1 Comparison of Bulk and SOS CMOS

Bulk CMOS is currently the workhorse of the semiconductor industry. In a bulk CMOS process all of the devices are fabricated in a common Silicon substrate. N-well technologies, which are currently the most popular, are formed from a p-type wafer. The NMOS devices are formed by making n+ source and drain diffusions directly in the p-substrate. PMOS devices are formed by forming an n-well in the p-substrate. The p+

source and drain diffusions are formed in this n-well. In bulk CMOS technology device isolation is provided by the reversed bias p-n junctions between the well and substrate and the source/drain and substrate.

Silicon-on-insulator (SOI) is a variant of bulk CMOS, which has been gaining popularity in the commercial sector over the past decade. SOI is actually a mature technology in its own right, however it has historically suffered from poor yield and therefore had only been considered for research. The technology considered for this project is Peregrine 0.5μm Silicon-on-sapphire (SOS) because it is available from the MOSIS foundry service. SOS is a type of SOI technology that uses sapphire as an insulating substrate. In SOS every device is formed in its own individual Silicon island. One of the main advantages of SOS is that the device can operate much faster because of the reduced junction capacitances at the drain. In addition cross-talk between analog and digital systems implemented on the same chip is reduced because there is not a common silicon substrate. Figure 2.14 shows the cross-section of an NMOS and PMOS device realized in a bulk CMOS technology and a SOS CMOS technology.

2.5.2.2 Technology Chosen for this Project

The Peregrine SOS 0.5μm process was chosen for this project over a bulk CMOS process. It was felt that a sub-micron bulk CMOS process could have provided the necessary RF performance, however the overriding concern was high-temperature operation. SOS is far superior to bulk CMOS in terms of high temperature performance because there is no source-body or drain-body diode, therefore leakage currents are significantly minimized.

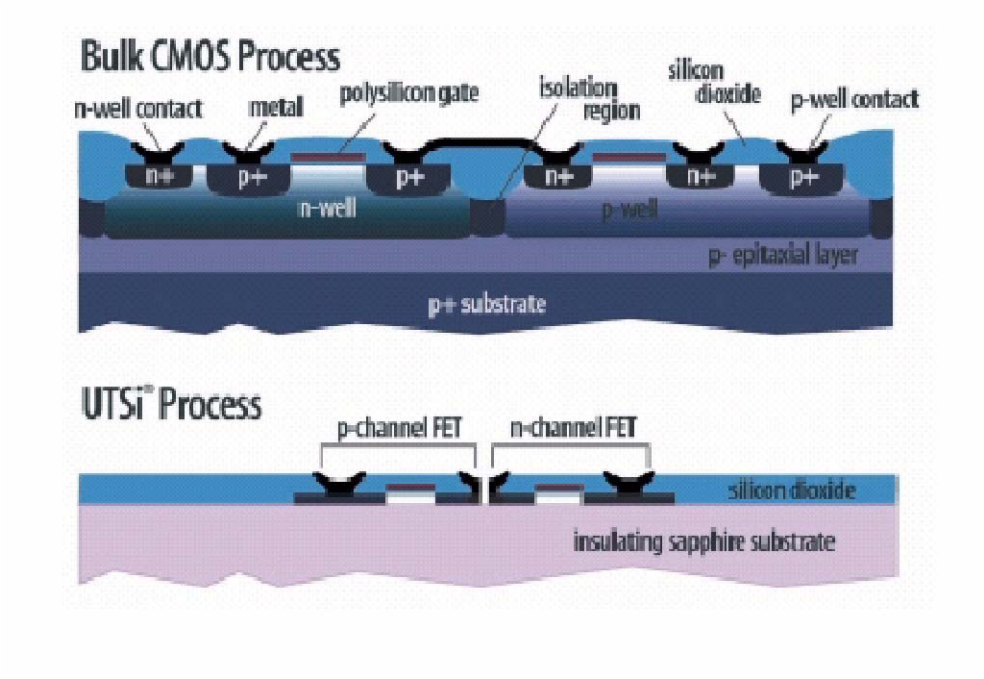

Figure 2.14: Cross Section of Bulk CMOS and SOS CMOS Transistors.
From *CMOS SOS for Mixed-Signal ICs*, available at http://www.peregrine-semi.com/prd_prodinfo.html

Chapter 3

Designing High Efficiency, Low Power, RF Power Amplifiers

3.1 Introduction

This chapter will examine in detail the issues related to the design of a high efficiency, low power, RF power amplifier. First the power amplifier types discussed in Chapter 2 will be re-examined in terms of their ability to operate at low power levels. It will be shown that the Class E power amplifier has great promise for performing well at low power levels and a more detailed analysis of the Class E amplifier will be shown. Next measured results from several Class E amplifier test cases will be presented. The test results will highlight the important trade-offs in the design of low power Class E amplifiers.

3.2 Power Amplifier Topologies for Low Power Operation

3.2.1 Current Source Power Amplifiers

This section will show that, in general, current source power amplifiers are not the best choice for a low-power, high-efficiency power amplifier. First one must consider that a current source power amplifier will operate at its highest efficiency when its average output power is maximum. The maximum output power of a current source power amplifier, which also corresponds to the maximum efficiency, is given by

$$P_{out,RF} = \frac{V_{dd}^2}{2R_L} \tag{3.1}$$

Therefore the required power supply voltage to achieve maximum efficiency can be

calculated.

$$V_{dd} = \sqrt{2R_L P_{out,RF}} \tag{3.2}$$

Assuming a load resistance of 50 ohms and an output power of one-milliwatt, the supply voltage that yields maximum efficiency can be calculated as

$$V_{dd} = \sqrt{2(50\Omega)(0.001W)} = 0.316V \tag{3.3}$$

Equation 3.3 shows that to achieve maximum efficiency a power supply voltage of approximately 300mV is required. A quick examination shows that a current source power amplifier is unrealizable at this bias voltage. For instance, consider a Class A implementation. Operation at RF demands that the transistor is biased well into strong inversion, generally a gate-overdrive voltage of 300mV or greater is required. Therefore there will simply not be enough power supply voltage for the device to remain in saturation over the entire RF cycle, especially when one considers the large voltage swing at the drain. The situation is even worse for Class B and Class C operation, because an even larger peak gate drive is required when operating in these modes.

One could argue that the power supply voltage problem could be reduced by transforming the 50 ohm load resistor upwards. For instance, consider that one wishes to use a 2-V

power supply, the required load resistance is given by

$$R_L = \frac{V^2_{dd}}{2P_{out,RF}} \tag{3.4}$$

For this case, the load resistance would be equal to 2000 ohms. However one encounters another implementation problem associated with the off-chip passive components. After searching the Coilcraft webpage, it was found that the largest inductance that could be used at 300MHz is approximately 300 nH [30]. Inductances greater than this value were limited by their self-resonant frequency to applications below 300 MHz. Since 300 nH is the largest available inductor, this is the value that would be used for the RF choke. The reactance of this inductor at 300 MHz would be

$$X_L = 2\pi(300MHz)(300nH) \cong 550\Omega \tag{3.5}$$

The requirement for the reactance of an RF choke is that it is much larger than the load resistance. The term 'much larger' is generally taken to mean a factor of ten or more. Therefore this rule of thumb generally limits the maximum load resistance to roughly 50 ohms. If a load resistance of 2000 ohms were used with a 300 nH inductor, a significant degradation in efficiency would occur because the inductor would not act like a DC current source.

3.2.2 Switch Mode Power Amplifiers

Section 3.2.1 showed that current source power amplifiers were not a good option for low power, high efficiency operation mainly because there would not be enough V_{DS} for the

active device to remain in saturation. Since a switch mode amplifier operates only in the ohmic and cutoff regions, there is no $V_{DS,SAT}$ requirement and it seems that this would be a good choice. Therefore this section will examine the use of a switch mode power amplifier for the application.

The Class D amplifier can be ruled out quickly, since the amplifier must operate at 300 MHz. Therefore the choices that are left are the Class E and Class F amplifiers. The main drawback of the Class E amplifier is the large switch voltages present. However the low power levels used in this application do not require a large power supply voltage, so the maximum voltage of $3.6V_{DD}$ should not be a problem. The Class F amplifier has limitations due to the requirement of a quarter wave transmission line; which would be 250mm long at 300 MHz. Therefore a greater study of the Class E amplifier will be made to investigate its viability as a low voltage, high efficiency RF amplifier.

3.3 Class E Amplifier - Design Considerations

3.3.1 Ideal Class E Amplifier

One of the first detailed analyses of the Class E amplifier was presented by Raab [31]. In his work, he studied the single ended Class E implementation presented in Figure 2.11. The assumptions that Raab made in his analysis are

- ideal RF choke
- ideal switch
- high Q output network

Table 3.1: Component Values Required for the Class E Amplifier
Assumes an output power of 1mW.

Vdd (V)	Ldc (nH)	CB (pF)	L0 (nH)	C0 (pF)	RL (ohms)
0.25	191	2.7	213	1.47	36
0.5	765	0.68	853	0.37	144
1.0	3000	0.17	3410	0.092	576

The analysis of the Class E amplifier is straightforward but complex. Raab analyzes the Class E waveforms using a Fourier analysis and finds an expression for the circuit components in terms of the power supply voltage, output power, and switch duty cycle. The derivations will not be repeated here, however some example component values calculated using Raab's method are shown in Table 3.1. One can see that the components listed in Table 3.1 are only realistic for the case of V_{dd} equal to 0.25 Volts. Of course it is questionable how well an amplifier will actually perform with such a small drain bias, especially considering that Raab's analysis assumed an ideal switch, whereas a transistor switch will have some finite output conductance when the device is in the ohmic region.

3.3.2 Class C-E Amplifier

Section 3.3.1 presented the component values required to implement an ideal Class E amplifier, that is an amplifier with 100% efficiency. This section will examine the design of a sub-optimal Class E amplifier, which is termed the Class C-E or mixed-mode amplifier. While a current source amplifier operates only in the saturation and cutoff regions, and a switch mode amplifier operates only in the ohmic and cutoff regions; a mixed-mode amplifier operates in the saturation, ohmic, and cutoff regions.

Kazimierczuk presented a detailed analysis of the Class C-E amplifier [32]. In his analysis, he modeled the active device as shown in Figure 3.1. In this model the active device operates in one of three modes; a switch with finite output conductance, an open-circuit, and a voltage controlled current source. The position of the switch is determined by the instantaneous value of the input signal.

The circuit shown in Figure 3.1 was used as a model in computer simulations. The operating region of the amplifier was varied from Class C to Class C-E, and then to Class E mode. Kazimierczuk showed that the major advantage of the Class C-E amplifier is that it can operate more efficiently than the Class C amplifier, however the value of the shunt capacitance, C_B, can be much larger than what is required by a Class E amplifier. Considering that a Class E amplifier operating at 300MHz with an output power of 1mW and a power supply voltage of 1 volt requires a shunt capacitance of 170 fF, this is certainly a great advantage. The main drawback of the Class C-E amplifier is that it will never achieve an efficiency of 100% because of hard-switching losses.

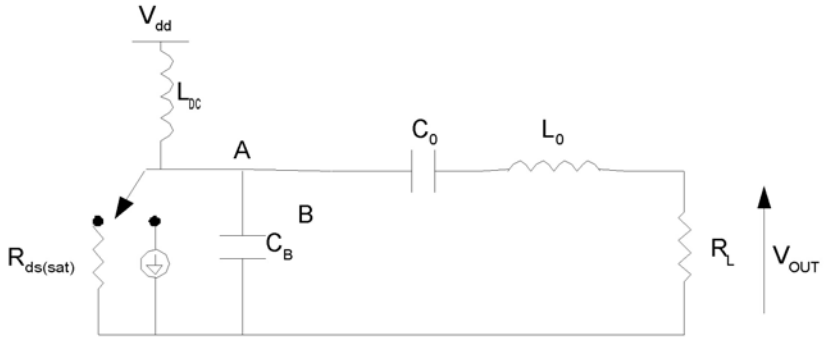

Figure 3.1: Idealized Model of a Mixed-Mode Power Amplifier
This model was used by Kazimierczuk in his analysis of the Class C-E amplifier.

Table 3.2: Component Values Required for a Class C-E Amplifier
Assumes an output power of 1mW and a shunt capacitance of 2pF

Vdd (V)	η ( )	Ldc (nH)	L0 (nH)	C0 (pF)	RL (ohms)
0.25	0.99	190	202	1.56	36
0.5	0.95	424	458	0.715	80
1.0	0.82	589	656	0.535	111

Table 3.2 shows the component values required for a Class C-E amplifier that were obtained using the method introduced by Kazimierczuk. In this method the shunt capacitance is chosen *a priori*, and one can then solve for the resulting efficiency. In Table 3.2 the case of V_{dd} = 0.25 V is roughly equal to the case of V_{dd} = 0.25 V in Table 3.1. This implies that ideal Class E operation is indeed possible at these power levels, however a power supply voltage of 0.25 V would be required. The case of V_{dd} = 0.5 V and 1.0 V again show that several of the component values would be unrealizable. For instance one will notice that the load impedance is greater than 50 ohms and the corresponding RF choke inductance is greater than 300 nH. As discussed in Section 3.2.1, an inductance greater than 300 nH is very difficult to obtain above 300 MHz.

3.4 Low Power Class E Amplifier Design Methodology

3.4.1 Introduction

Several important conclusions can be drawn from the discussions presented in Sections 3.3.1 and 3.3.2. First it seems that optimum Class E operation is not achievable at this power level and frequency unless a power supply voltage of 0.25 V is used. Furthermore the concept of a sub-optimal Class E power amplifier seems very promising, however component values required for this amplifier are also not obtainable. It is important to note that the major difficulty in implementing the Class E amplifier in this application are the

requirements of RF operation and very low power. If either of these requirements were relaxed, for instance if the output power were on the order of 100 mW, the component values become much simpler to achieve. However considering the difficulty in implementing a low power, high efficiency amplifier using other topologies; the Class E approach still has a great deal of merit.

Section 3.3 showed that the component values required to implement a low power, RF Class E amplifier are difficult to obtain. Therefore the design approach taken in this work will be to simply accept the component values which are obtainable, and characterize how well the amplifier performs with these component values. The first component that can be chosen is the load resistance, which will be 50 ohms. This impedance is chosen because it corresponds to one-tenth of the maximum obatainable RF choke inductance. Next a great deal of hardware testing will be performed. The purpose of this testing is to evaluate the performance of the amplifier and to ultimately choose the set of physically realizable components that yield optimum performance. The setup used for testing and characterization is discussed in Appendix A.

The first step in this design methodology is to pick a topology for the Class E amplifier. Figure 3.2 shows the amplifier topology that will be used for this project. This topology is very similar to the one introduced in Figure 2.11, except that an NMOS transistor has been explicitly included instead of the ideal switch and a second harmonic trap consisting of L_2-C_2 has been included.

Table 3.3: Important Circuit and Performance Parameters for the Class E Amplifier

Circuit Parameters	Performance Parameters
C_B	
Q_L	
	Pout
V_{dd}	η
$V_{in,pk}$	Distortion
V_b	
Temperature	

The L_2-C_2 combination will present a very high impedance to any second harmonic currents, therefore its purpose is to reduce second harmonic distortion in the output signal.Secondly the critical circuit parameters and performance parameters must be defined.

In Table 3.3 the circuit parameters represent the independent variables, and they can be sub-divided into three groups. The first group is comprised of circuit components, which

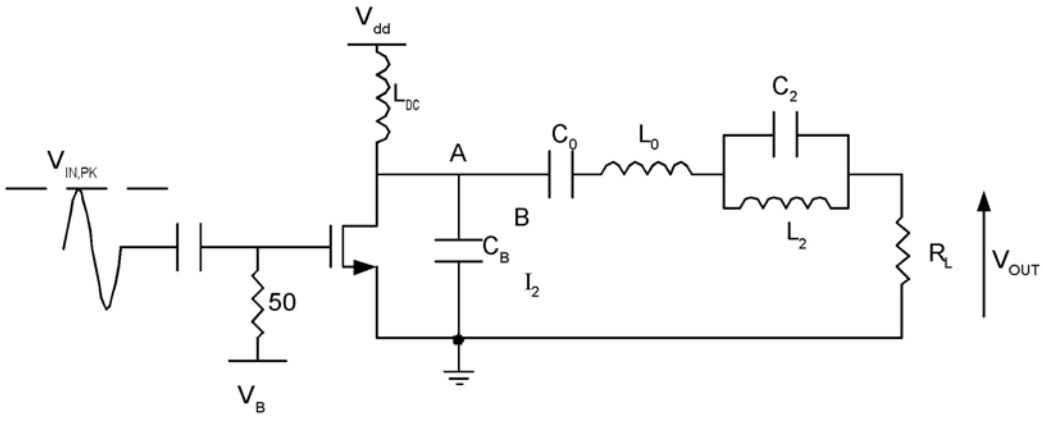

Figure 3.2: Single-Ended Output Class-E Power Amplifier

are C_B and Q_L, where

$$Q_L = \frac{\sqrt{L_0 / C_0}}{R_L} \tag{3.6}$$

The second group represents the circuit drive signals and includes V_{dd}, $V_{in,pk}$, and V_b. Finally the last circuit parameter is temperature. The performance parameters will be used to gauge the amplifier's performance. They are composed of output power (P_{out}), drain efficiency, and distortion.

The two groups presented in Table 3.3 represent the independent and dependent variables in this problem. Therefore the final step is to investigate the relationship between these variables. It can be assumed that the effect of varying the voltages and circuit components are independent of one another, therefore they will be treated separately. First a set of components will be chosen and used throughout all of the drive signal testing. In addition, all of the drive signal testing will be performed at one frequency. In the drive signal testing several combinations of signals will be tried and their effect on the amplifier's output power and efficiency will be measured. Next a fixed set of drive signals will be input to the amplifier and the circuit components will be varied. For every combination of circuit components, the input frequency to the amplifier will be swept and the output power, efficiency, and distortion will be measured. After all of the testing is completed, it is hoped that an optimum low-power Class-E amplifier using the given topology can be developed.

3.4.2 Drive Signal Testing

In all of the Class E analyses presented thus far an idealized model was used instead of an actual device. Ideally the Class-E amplifier is driven with an square wave, and thus approximates a switch. However generating a square wave at RF is difficult, and will certainly consume significant power when compared to the output power level of 0 dBm. Therefore it has been decided to drive the amplifier with a large sine wave that will drive the active device into the triode region for a portion of every cycle. The question then is, "What amplitude sine wave is required for the Class-E amplifier to operate efficiently?" The discussion presented in this section will help to answer that question.

Figures 3.3 thru 3.6 show the results of the drive signal testing. In this set of tests a load network was chosen, and all of the testing was performed at the resonant frequency of the load network. In all of the plots a sine wave was input to the amplifier, and the magnitude of the sine wave was increased from 0.5V to 1.6V in logarithmic steps. In addition the drain voltage was swept from 0.2V to 1.2V. The only difference between the drive signals used to generate the following plots is the offset voltage. The offset voltage for Figure 3.3 is 0V, and it is stepped in 0.2V steps for each of the following plots. Therefore the offset for Figure 3.6 is 0.6V.

Figure 3.3 presents the plots for the V_b = 0V case. One can see in this figure that the efficiency is very low when the peak input signal is below 1.0V. In addition, all of the curves show a relatively large variation in efficiency over the V_{dd} sweep, which is undesirable. Figure 3.4 shows the plots for the V_b = 0.2V case. One will first notice in this plot that the output power is much less sensitive to the magnitude of the input drive

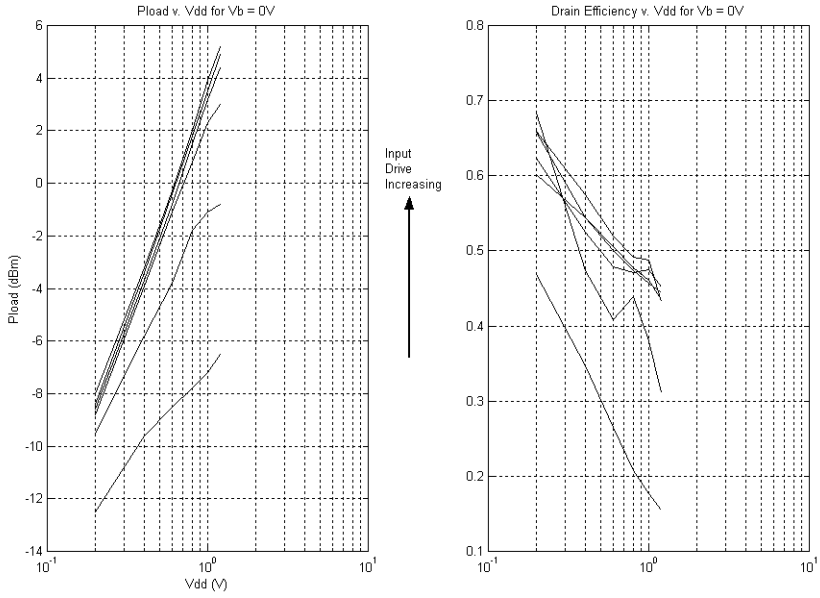

Figure 3.3: Pout and Efficiency v. Vdd with Input Drive Sweep and Vb = 0V

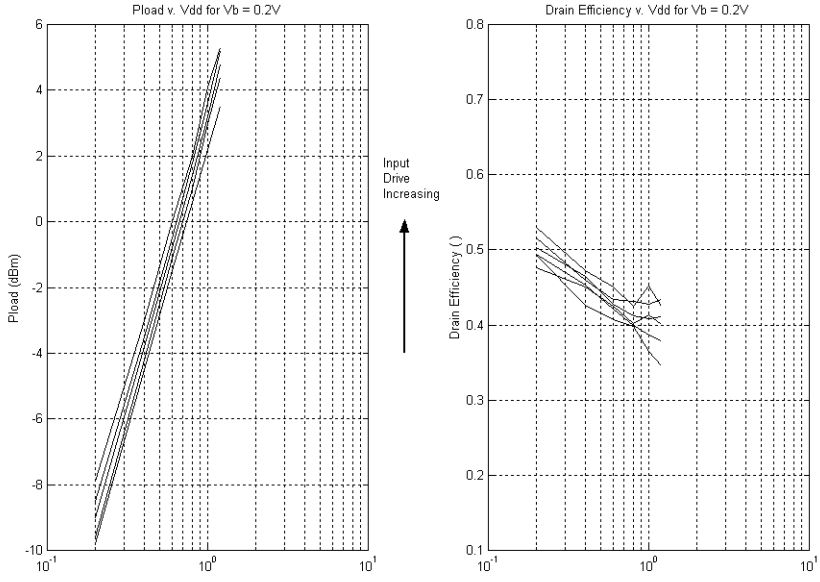

Figure 3.4: Pout and Efficiency v. Vdd with Input Drive Sweep and Vb = 0.2V

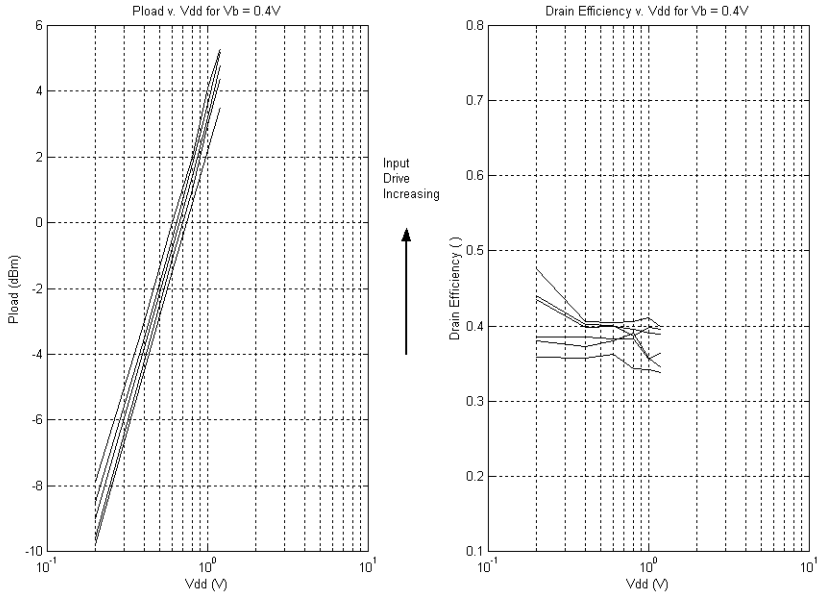

Figure 3.5: Pout and Efficiency v. Vdd with Input Drive Sweep and Vb = 0.4V

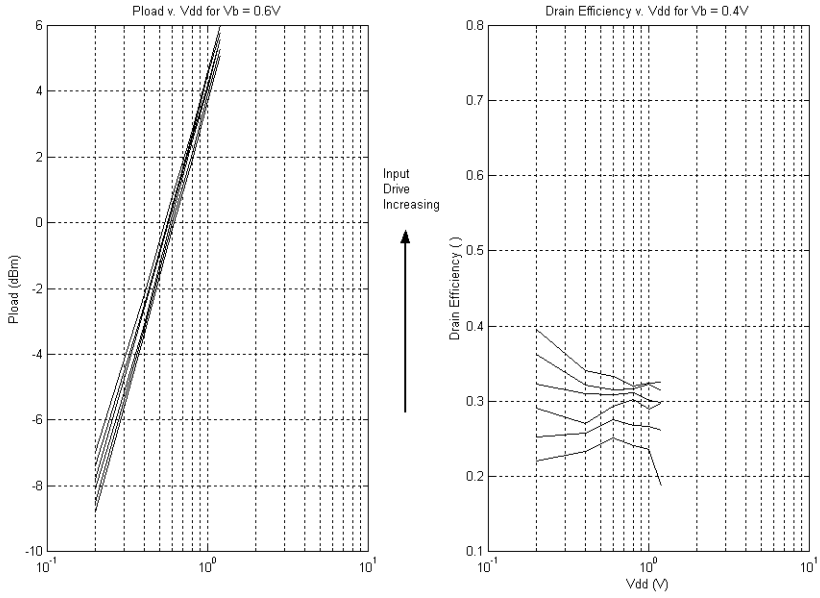

Figure 3.6: Pout and Efficiency v. Vdd with Input Drive Sweep and Vb = 0.6V

signal, when compared to Figure 3.3. Insensitivity to input drive signal is important in a non-linear amplifier because the output power is supposed to be independent of the gate drive signal. In addition one can see that the efficiency is still very good, and it varies over a much smaller range when compared with the V_b = 0V case. Figure 3.5 shows the V_b = 0.4V case and Figure 3.6 shows the V_b = 0.6V case. One can see in these plots that sensitivity of the output power to input drive signal is even lower than the V_b = 0.2V case. However the efficiency is much lower for these cases because of the increased gate bias. Therefore after examining all of these cases it seems that a 1.0V magnitude sine wave with a 0.2V offset is a very good choice.

3.4.3 Load Network Testing

The choice of the load network proceeds in a manner very similar to the drive signal testing. Except in this case, a drive signal is chosen and the frequency dependent load network is varied. A 1-Volt peak sine wave with a 0.2-Volt offset was chosen for this test. Then for each test case the input frequency was swept from 200MHz to 400MHz. The two circuit quantities varied in this case are the shunt capacitance C_b, and the quality factor of the load network. The test cases for C_b were 2pF, 5pF, and 10pF. The test cases for Q_L were one and five.

Figure 3.7 shows the frequency response plots for the Q = 1 case. One can see the that the output power has a very broad peak, as expected. In addition the output power in the passband seems to be very insensitive to the value of the shunt capacitance.

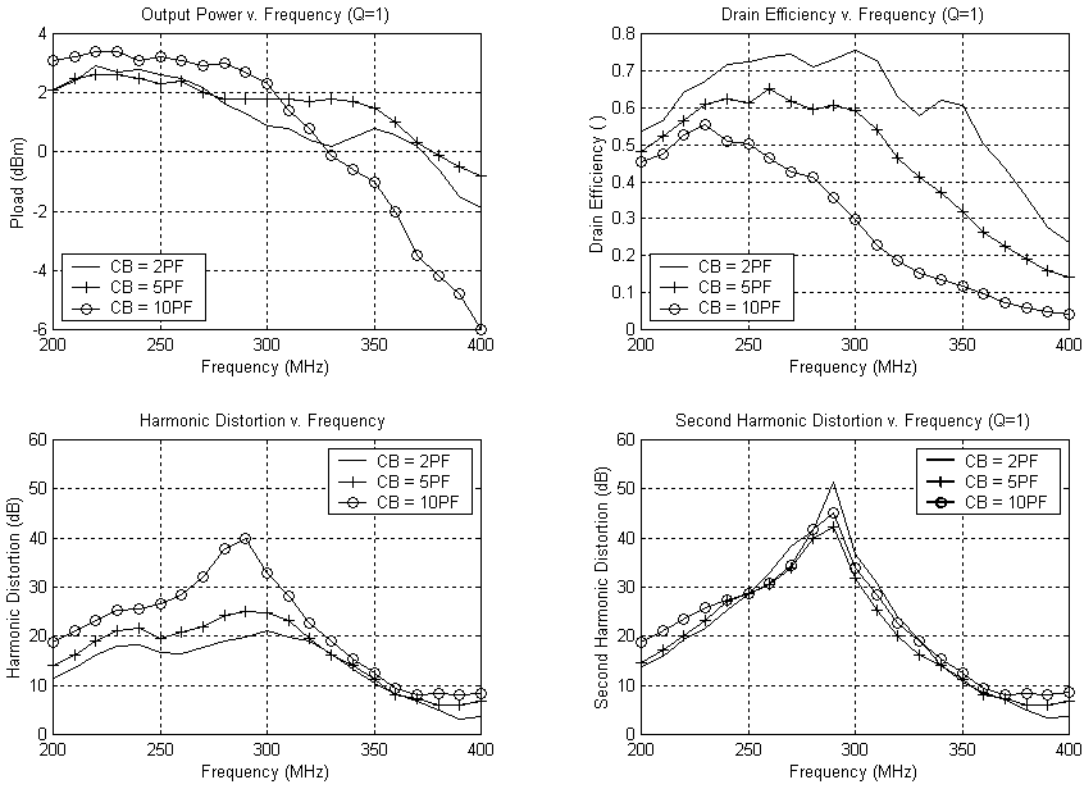

Figure 3.7: Frequency Response Plot for Q=1 Case.

However the drain efficiency is very sensitive to the value of C_b. Immediately one can see that a shunt capacitance of 2pF is probably the best choice. The distortion plots also have some interesting results. First the harmonic distortion is almost 15dB better for the C_b = 10pF case. However this improved distortion does not compensate for the poor efficiency exhibited by the 10pF case.

Figure 3.8 shows the frequency response plots for the Q = 5 case. As expected the output power rolls off much more quickly in this case. Also the output power is still relatively insensitive to variations in the shunt capacitance and the maximum efficiency occurs for the C_b = 2pF case. However the peak efficiency is lower for Q = 5 than it is for Q = 1. The distortion plots show that the Q=5 case is generally superior to the Q = 1 case, this is not surprising since the higher Q network will be able to filter the 3rd and higher order harmonics better. Finally one will notice that the total harmonic distortion and second harmonic distortion are almost equal, indicating that the distortion is due largely to second harmonic energy. It is important to note that in future revisions of the amplifier a differential architecture could be used that would significantly reduce the second harmonic distortion over the entire operating bandwidth.

Since the efficiency is better for the Q = 1 case, and the distortion is better for the Q = 5 case, it has been decided that a quality factor of 4 will be used. In addition a shunt capacitance of 2 pF will be used.

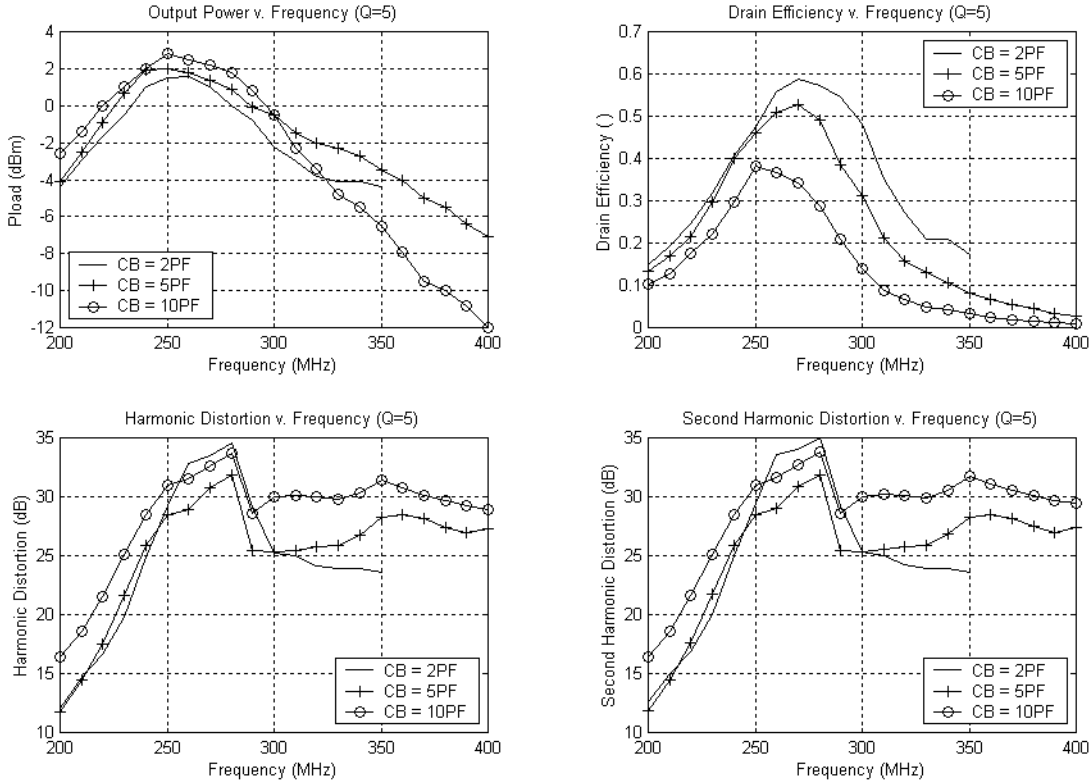

Figure 3.8: Frequency Response Plots for Q=5 Case.

3.4.4 Temperature Effects

The final step in developing the amplifier is to characterize its sensitivity to temperature effects. Figure 3.9 and Figure 3.10 show the amplifiers performance at several different temperatures. In this test a 1-V peak sine wave was input to the amplifier and a fixed load network was used. Also, all of these tests were conducted at the resonant frequency of the load network. Figure 3.9 shows the output power and efficiency for the case of a sine wave with no offset.

One can see that the output power changes by about 1-dB over the entire temperature range and the efficiency falls by as much as 15%. Figure 3.10 shows the output power and efficiency for the case of a 1-V peak sine wave with a 0.2-V offset. Again the output power falls by roughly 1dB and the efficiency falls by as much as 15%. These figures show that output power is relatively insensitive to large temperature changes, however efficiency is quite sensitive to large temperature changes. Nevertheless it seems that this power amplifier architecture should perform well over an extended temperature range.

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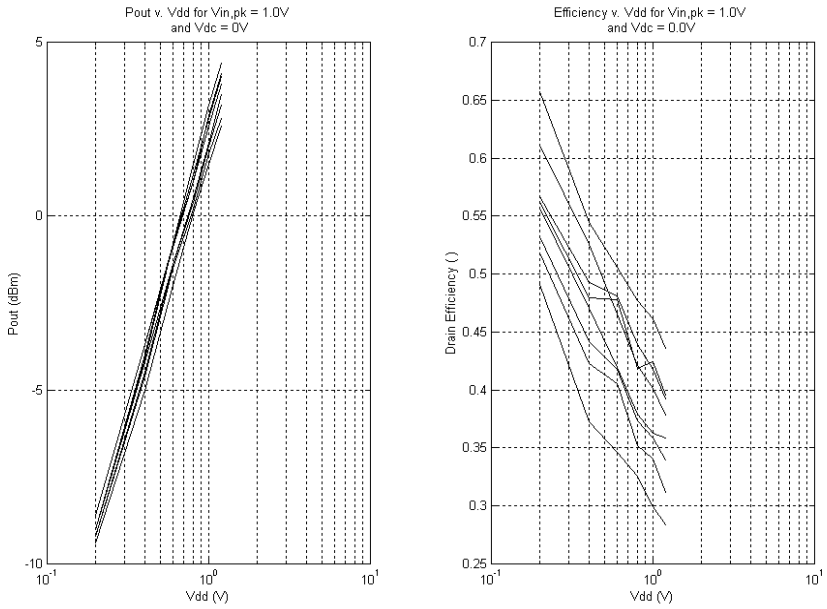

Figure 3.9: Output Power and Efficiency for Different Temperatures - Plot I
This plot was generated with Vb = 0V, Temperature was swept from 25C to 180C

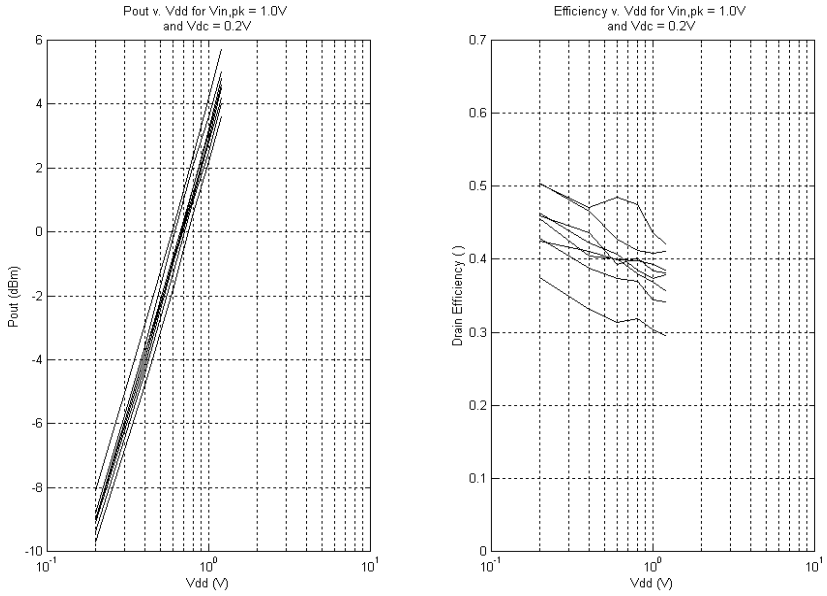

Figure 3.10: Output Power and Efficiency for Different Temperatures - Plot II
This plot was generated with Vb = 0.2V, Temperature was swept from 25C to 180C

Chapter 4

Low Power, High Efficiency Amplifier - Measured Results

4.1 Introduction

Chapter 4 will present the final measurement results for the low power, high efficiency amplifier. First the final design considerations, including component choices, will be discussed. Then the measured results will be presented along with simulation results. The simulations were run using the HSpice circuit simulator.

4.2 Final Design Considerations

4.2.1 Component Choices

As stated in Section 3.4, it was decided to use a Q_L of four and a C_B of 2pF for the final design. In addition a load resistance of 50 ohms and a DC feed inductance of 330 nH was used. A schematic of the final testboard is shown in Figure 4.1. The component values used on the testboard are shown in Table 4.1.

4.2.2 Final Testing Methodology

The final amplifier testing and characterization could be performed in several different ways. One method is to simply characterize the amplifier over its full range of output power at several temperatures from room temperature to 200 C and over a broad range of frequencies. However it was felt that this large amount of information might make it difficult to discern the most important aspect of the amplifier's performance, namely how

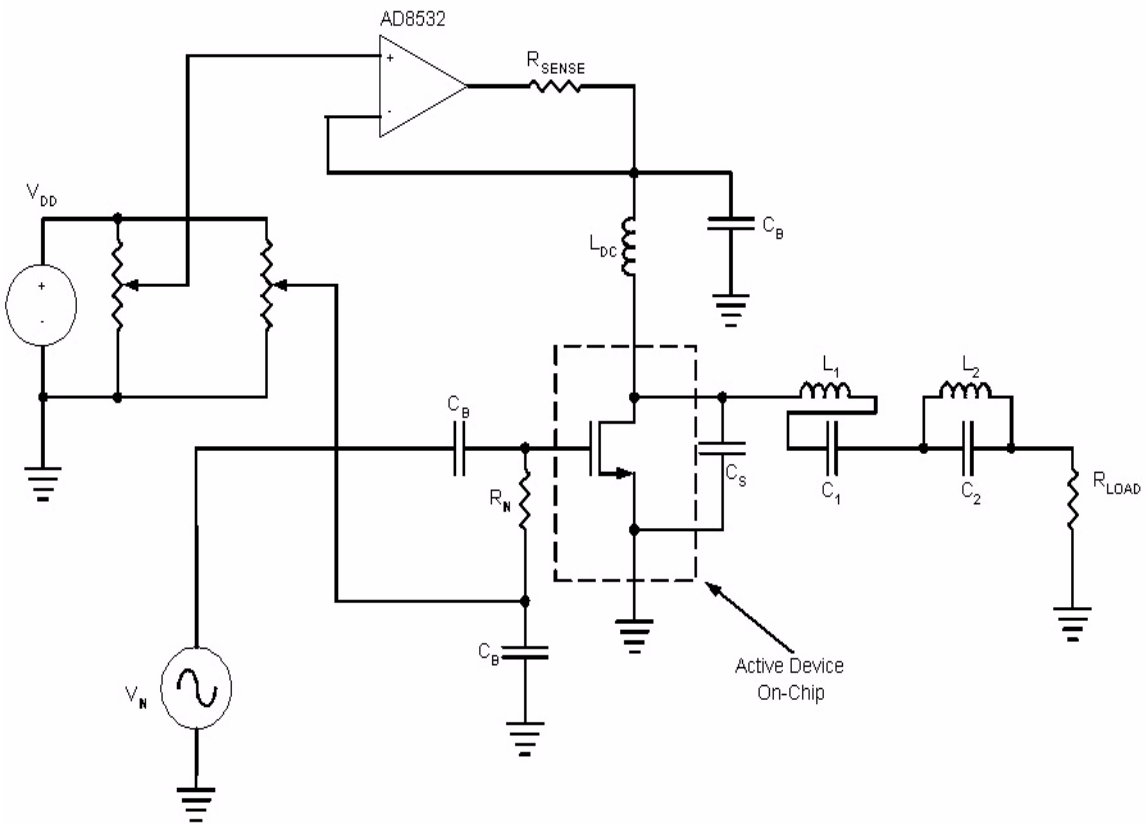

Figure 4.1: Final Test Board Schematic

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Table 4.1: Component Values for Final Testing

Component	Value
R_{SENSE}	100 Ω
R_{IN}	50 Ω
R_{LOAD}	50 Ω
C_B	100 pF
C_S	2 pF
C_1	3 pF
C_2	3 pF
L_{DC}	330 nH
L_1	100 nH
L_2	22 nH

will the amplifier perform with an average output power of 0 dBm? Therefore it was decided to test the amplifier assuming that it was part of the system shown in Figure 4.2. In power amplifier applications it is important that the output power be insensitive to variations in component tolerances, temperature, semiconductor process variations, and operating frequency. Therefore power amplifiers are often enclosed in a feedback loop as show in Figure 4.2. In this system the power amplifier drives the load and the power sensing device measures the power delivered to the load. This information is then sent to the error amplifier which adjusts the drain voltage up or down so that the power amplifier produces the desired output power.

In the testing of this power amplifier an electronic feedback loop was not implemented, instead a “human” feedback loop was used. Namely as the operating frequency and

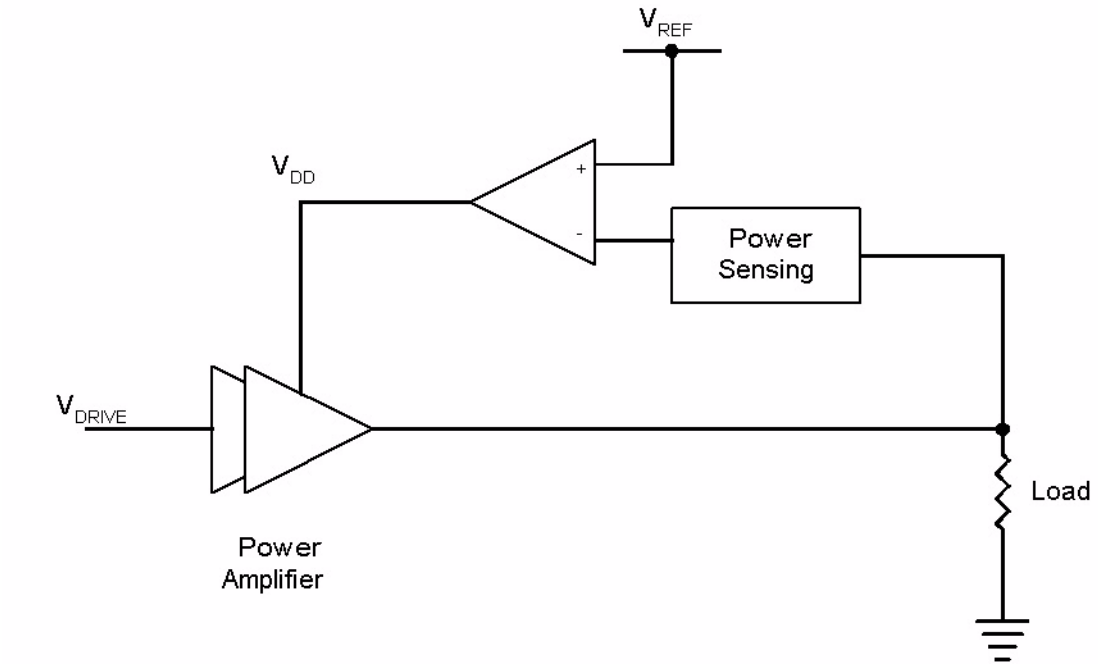

Figure 4.2: Typical Application of a Power Amplifier

temperature were varied, the drain voltage of the power amplifier was varied via a potentiometer until the output power was equal to 0 dBm. At every frequency and temperature point the amplifier's efficiency and harmonic distortion were measured. During the final testing measurements were taken every 10 MHz from 240 MHz to 340 MHz, and every 25 C from 25 C to 200 C. These tests were performed for two different test boards.

4.2.3 Simulation Methodology

Up to this point in the project no simulation results have been presented. This is quite different from most circuit design methodologies where extensive simulation is performed before finalizing the design. However in this instance it was felt that hardware testing would be a much more reliable means for designing the amplifier. One of the main reasons for this is the relative simplicity of this circuit in terms of devices and biasing, when compared to traditional analog circuit designs. For instance a typical op-amp design might contain twenty or more transistors, and the designer must run simulations to guarantee that these devices all remain in saturation over temperature and process variations. However this design only contains one active device and it is not biased in one region of operation during normal circuit operation. In addition, this design is dependent on the absolute value of off-chip components which can easily be changed during testing if the desired performance is not achieved. Finally, the performance of this amplifier is critically dependent on the value of certain parasitic components whose value is not accurately known and therefore their effect on circuit performance can not be simulated. Foremost among these parasitic components is the junction capacitance associated with the protection diodes. This capacitance is in parallel with the shunt capacitance C_B, and

therefore it can affect the performance of the amplifier considerably, as shown in Figures 3.7 and 3.8. Another important parasitic component is any series resistance that is between the source terminal of the active device and the ground plane on the test board.

While it is true that simulations may not be helpful during the initial design phases, it is certainly important to see how well they predict the amplifier's performance once the design has been completed. This will allow a future design engineer working on a similar project to know how much faith to put in the simulation results. Therefore simulation results will be shown in conjunction with the final design results. In the final hardware testing the operating frequency and temperature were varied, and the drain bias was also varied to guarantee that the output power was equal to 0 dBm. Therefore the testing results will show how V_{DD} varied with operating frequency and temperature. However in the simulations the measured V_{DD} for each case will be input to the amplifier and the resulting output power will be measured. This is much simpler than trying to adjust the V_{DD} in a transient simulation until the proper output power is reached. The simulation and measured results can be compared by noting that the measured output power was equal to 0 dBm for each case. Therefore any deviation in the simulation results from 0 dBm can be seen as an error. In addition to the output power simulation, the efficiency and harmonic distortion will be measured for each of the cases described in Section 4.2.2.

The host file used for the Class E amplifier simulations is shown in Appendix B. To model the parasitic components described previously, several simulations were run and the simulation results were compared to the measured results. Parasitic components were added until a reasonably good fit was seen between the measured results and the

simulation results. The model used for the bonding pad and bond wires is shown in Figure 4.3. In this model the 2.5 pF capacitor represents the depletion capacitance of the ESD diodes, and the L-R network represents the bondwire.

4.3 Measured Results

The final measurement and simulation results for the high efficiency amplifier will be presented in the next several figures. As stated in Section 4.2.2, during the final testing the operating frequency and operating temperature of the amplifier were varied, and at each measurement point the drain bias was adjusted until the output power was equal to 0 dBm. Figure 4.4 shows the measured response for the V_{DD} control voltage. All temperatures are presented on the same plot as a family of curves. No marker was used to identify a curve with its corresponding temperature, because it was felt that the markers would make the plot too cluttered. Instead an arrow has been included to show which direction represents increasing temperature. Therefore in each of the plots the top curve represents the measured performance at 25 C and the bottom curve represents the

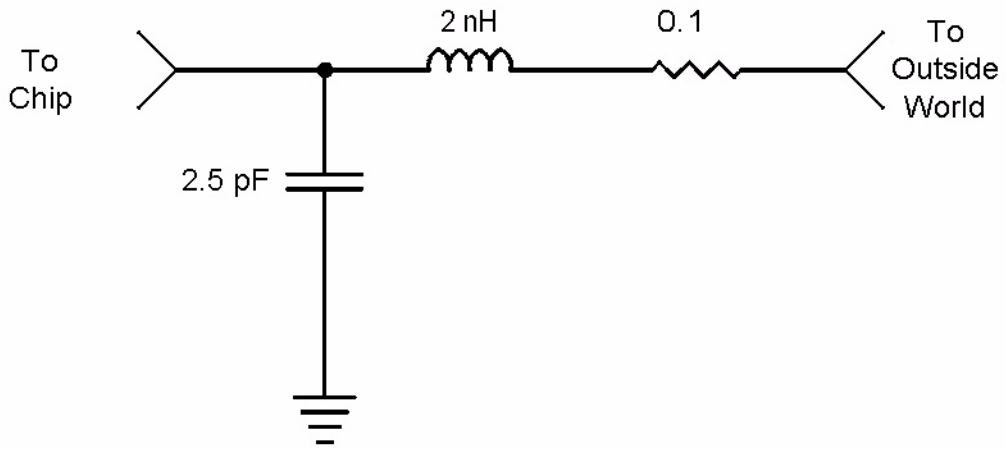

Figure 4.3: Pad and Bondwire Sub-circuit.

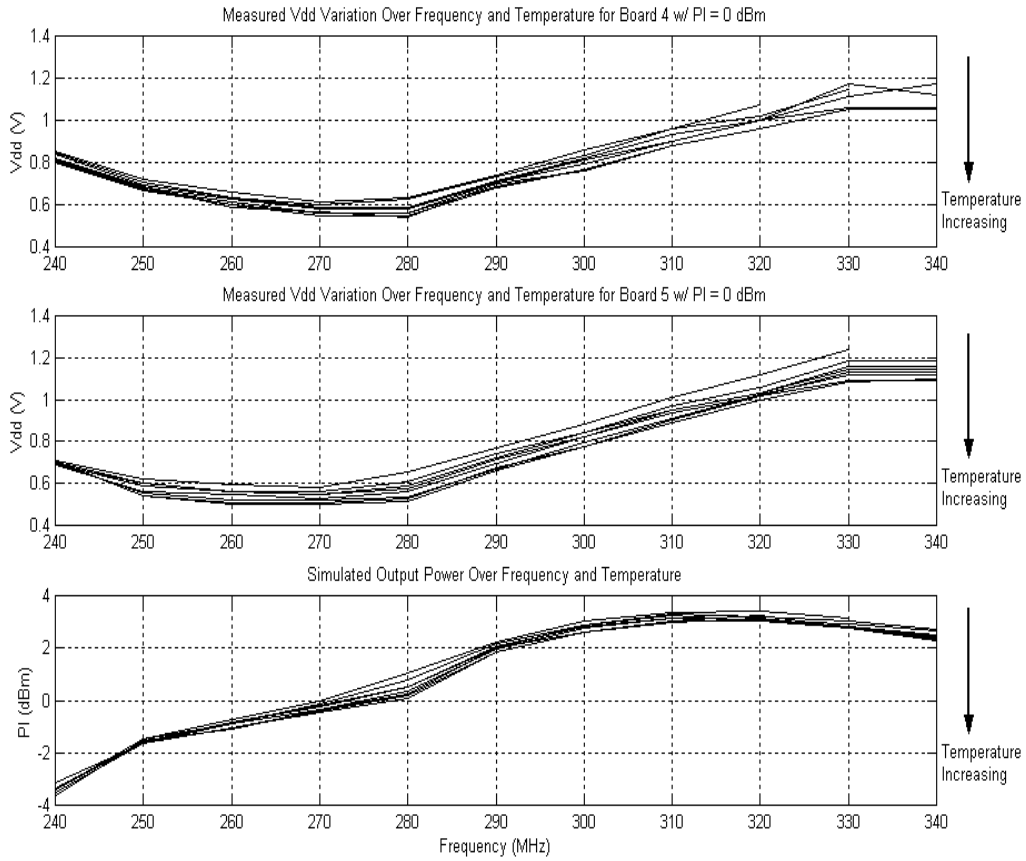

Figure 4.4: Final Testing - Measured Control Voltage and Simulated Output Power

measured performance at 200 C. In between the top and bottom curves the temperature was varied in 25 C steps. In Figure 4.4 the top two plots represent the measured control voltage for test boards 4 and 5, respectively. From these plots one can see that the control voltage varies over a range of roughly 0.5V to 1.2V as the frequency is swept from 240 MHz to 340 MHz. Assuming that the peak voltage at the switch $3.6*V_{DD}$, the peak voltage across the switch should be roughly 4.3 V, which is a safe drain voltage for a 0.5μm gate length device. The final plot in Figure 4.4 shows the simulated output power of the Class E amplifier over the same operating frequency and temperature ranges as the measurements were taken. In this simulation the V_{DD} bias for the amplifier was taken as the average of the V_{DD} measured for test boards 4 and 5. One can see in this plot that the simulated output power is within the range -3 to 3 dBm, therefore it is always within 3 dB of the correct value.

Figure 4.5 presents the measured and simulated efficiency. While the V_{DD} control voltage and thus the output power were relatively insensitive to variations in temperature, this plot shows that there is a significant variation in efficiency over temperature. The measured efficiency for test board 5 at 25 C is greater than 50% over the frequency range of 270 MHz to 290 MHz, it is greater than 40% over the frequency range of 250 MHz to 305 MHz. At 200 C the efficiency is never above 50%, however it is above 40% over the frequency range of 265 MHz to 290 MHz. Therefore the efficiency fell roughly ten percent in going from 25 C to 200 C. The results for test board 4 are very similar, although the efficiency is not quite as high. Of course, some variations in performance are to be expected because of variations in component values. Finally one can see that the simulated efficiency agrees reasonably well with the measured values. The efficiencies

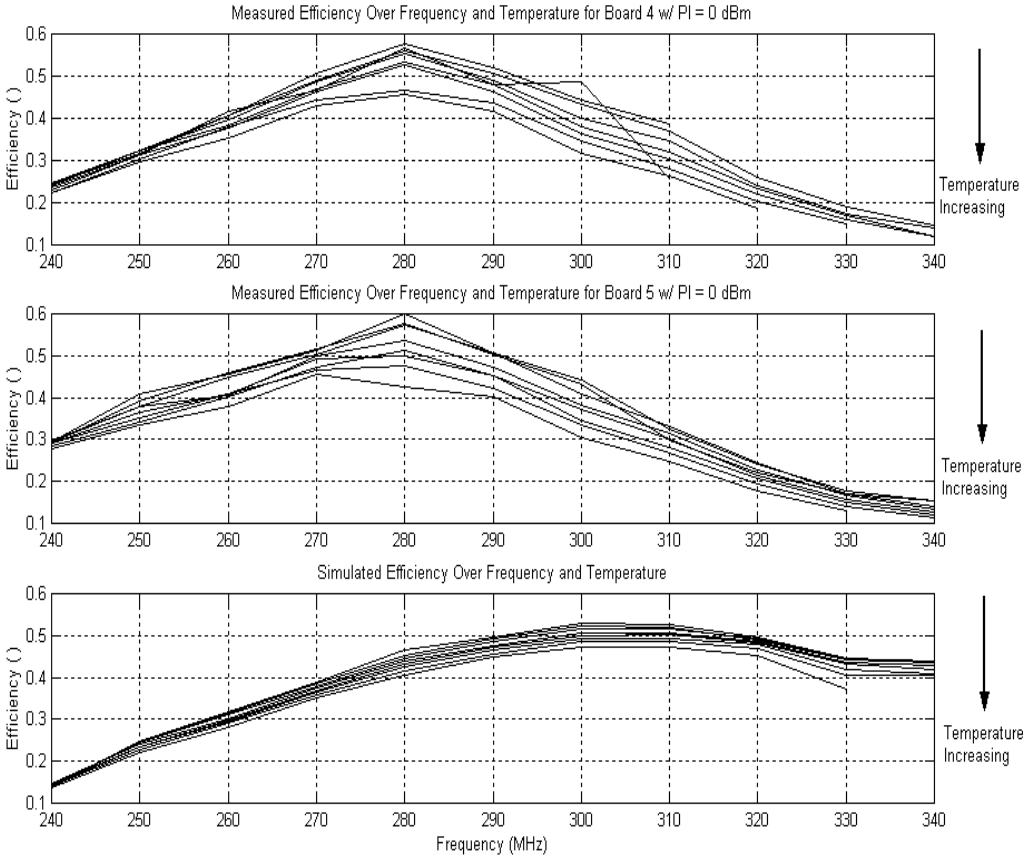

Figure 4.5: Final Testing - Measured and Simulated Drain Efficiency

are a bit lower in simulation, in addition the frequency response for the simulation has a peak at 300 MHz, while the measured peak is at 280 MHz. This difference could be due simply to component tolerances.

Figure 4.6 shows the total harmonic distortion. These plots show that the THD is fairly insensitive to temperature variations, which makes sense. Variations in THD over temperature are presumably to due to variation in the passive components over temperature. Since no temperature model was used for the passive components in simulations, the simulations show very little temperature sensitivity. These plots show that test boards 4 and 5 agreed reasonably well, although one test board showed an optimum at 270 MHz and the other was optimum at 280 MHz. This variation is due to the variation in the resonant frequency of the second harmonic trap. Finally, we can see that the THD is always better than 25 dB and peaks at roughly 40 dB.

Although there is no specification on the THD, it does seem that 25 dB is probably too low. Figures 4.7 and 4.8 shows the main components of THD, the second and third harmonics. First, it is interesting to note in Figure 4.7 that the second harmonic distortion is almost equal to the total harmonic distortion, indicating that the THD is dominated by the second harmonic component of the signal. This was also noted in Chapter 3. Next one will notice that the third harmonic distortion, shown in Figure 4.8, is significantly better than the second harmonic distortion. The reason for this is that the series resonant output circuit is better able to filter this higher order harmonic. One will also notice that the simulated distortion agrees better with the measured results in this case.

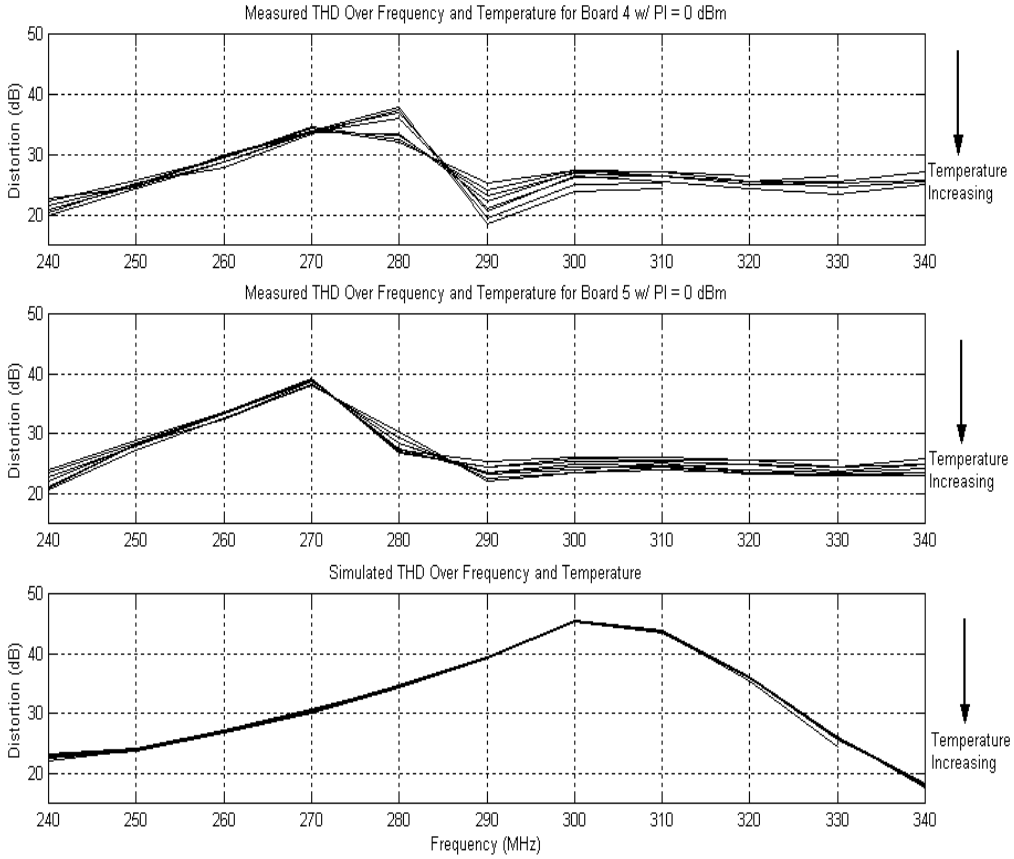

Figure 4.6: Final Testing - Measured and Simulated Total Harmonic Distortion

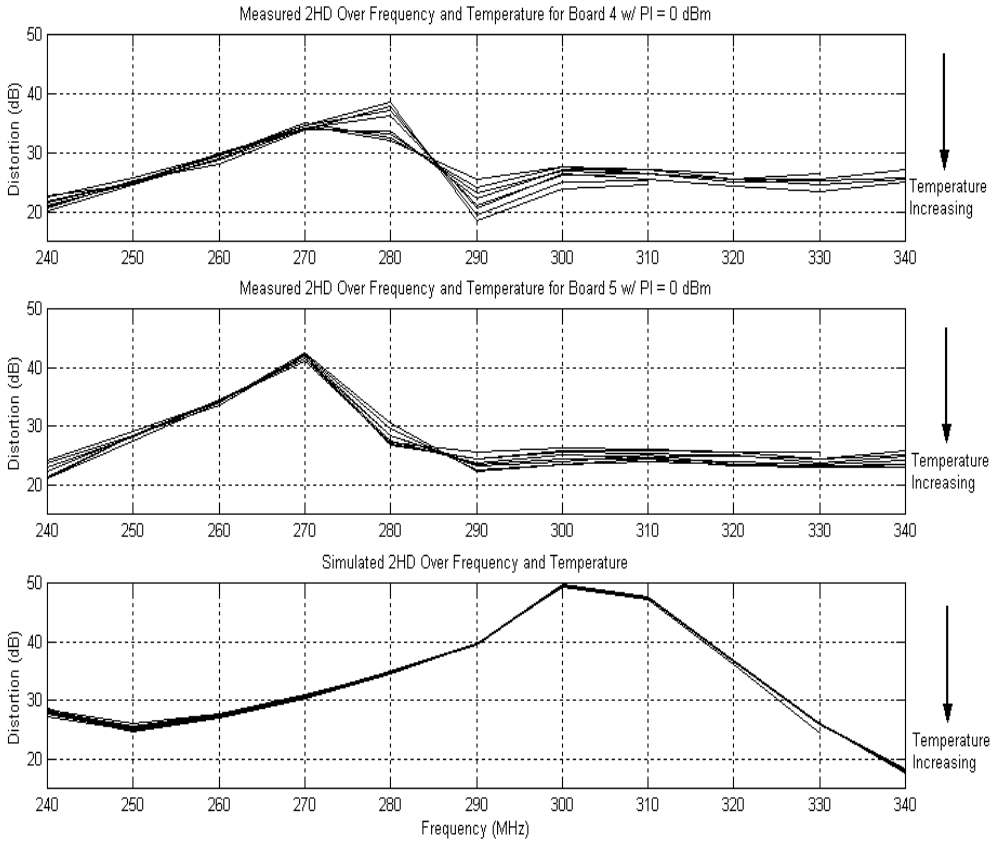

Figure 4.7: Final Testing - Measured and Simulated Second Harmonic Distortion

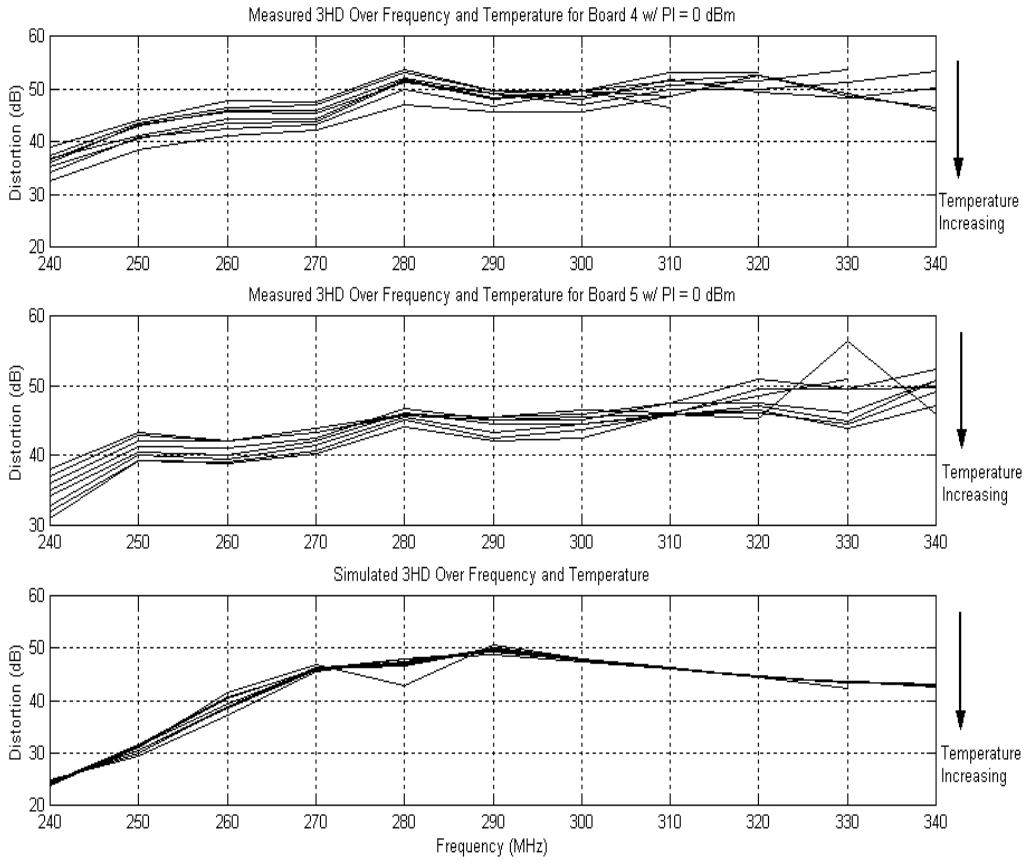

Figure 4.8: Final Testing - Measured and Simulated Third Harmonic Distortion

Chapter 5

Conclusion

5.1 Conclusion

This thesis has presented the design and analysis of a high-efficiency, low power, RF power amplifier. The amplifier was implemented in a 0.5μm CMOS SOS process. Hardware measurements showed that the amplifier performed reliably up to a temperature of 200 C. In particular, the amplifier achieved a drain efficiency greater than 40% over the frequency range 265 MHz to 290 MHz, with an output power of 1mW. The total harmonic distortion of the amplifier was better than 25 dB, or 0.316%, over the entire operating range of the amplifier.

This work has shown that it is possible to construct a high-efficiency RF power amplifier that operates at very low power levels. A literature search, the results of which were presented in Table 1.1, showed that very little work has been done regarding very low power, high efficiency power amplifiers. However, considering that remote systems are being forced to operate from very limited power sources, it seems that such an amplifier could be a very important part of next generation remote sensors.

5.2 Future Work

Although the results presented for this amplifier seem very good, there is certainly a great deal of improvement that could be made. First of all, consider the choice of *Q* for the output network. Figures 3.7 and 3.8 showed that a *Q* of 1 provided very good efficiency

over a very large bandwidth. However this *Q* was not chosen because the circuit exhibited a poor harmonic distortion. Thus a new architecture needs to be chosen that allows a low *Q* load network to be used, but still provides good rejection of harmonics. Since a differential architecture provides a first-order cancellation of all even-order harmonics, this provides an excellent means of reducing second-order distortion. Figures 4.7 and 4.8 show that the total harmonic distortion is dominated by the second harmonic component. Since second-order distortion would be reduced, a lower Q load network could be used, resulting in a higher efficiency. In addition, since the second order harmonic trap would not be required a third order harmonic trap could be used instead to reduce the third-order distortion. A circuit topology for realizing a low distortion, high efficiency Class E amplifier is shown in Figure 5.1.

Of course, one problem that will be encountered in using a differential architecture to reduce second harmonic distortion is that any mismatch between the two amplifiers will give rise to a second harmonic signal component. One method of reducing the mismatch would be to use a fully monolithic implementation. It is well known that the matching displayed by devices on an integrated circuit can be very good, therefore this provides a motivation for developing a monolithic implementation of the amplifier. It seems that all of the component values used could be implemented on-chip, except for the RF choke which would still have to be implemented as a discrete component. However the RF choke is not in the RF signal path so mismatch in this component would not degrade performance.

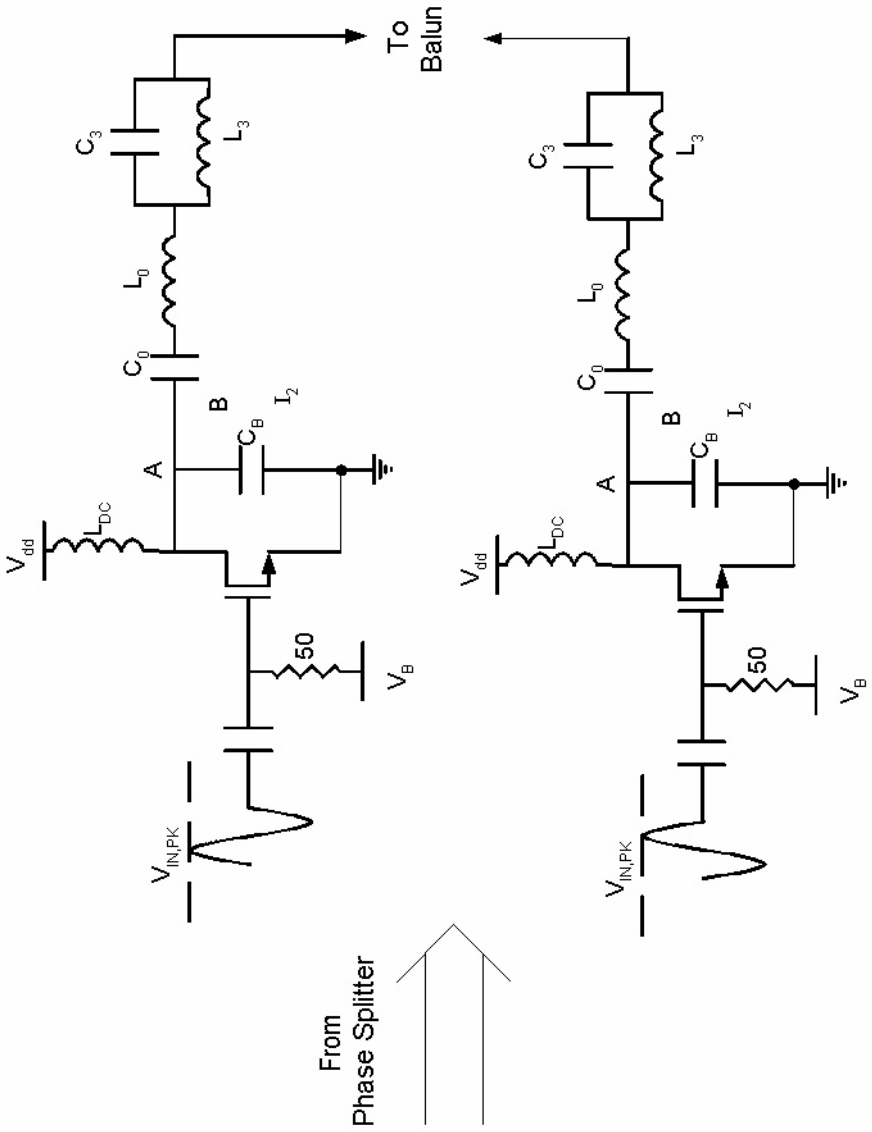

Figure 5.1: Proposed Class E Amplifier Topology I

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Appendices

Appendix A: Test and Measurement Setup

A.1: Test Board Construction

As stated in Section 2.5.2.2 the Peregrine SOS 0.5μm semiconductor process was chosen for this project because of its good RF performance and high temperature capabilities. The integrated circuit was fabricated using the MOSIS service [29]. Layout was completed on a Sun workstation using the Magic software package. Since the active device in this amplifier acts as a switch, a large device was required to guarantee low on-resistance. Therefore it was decided to size the transistor at (800u/0.5u). Since distributed gate resistance effects can become very important at RF, the device was laid using many parallel gate fingers. In particular, this device was laid as 16 gate fingers that were each 50um wide. The magic layout of this transistor is shown in Figure A.1.1.

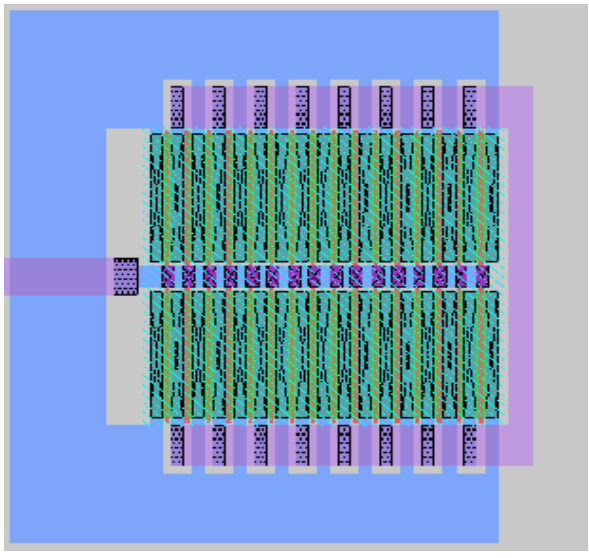

Figure A.1.1:Transistor Layout of Power Amplifier

Quality test board construction is critical when designing RF circuits. Therefore it was decided that the test board for the power amplifier will use a mother-board/daughter-board approach. The mother-board contains all of the DC biasing, including an op-amp voltage regulator that is used to provide the drain bias for the amplifier. The mother board was soldered on a proto-board using thru-hole components since it provides bias voltages only. However since high speed performance of the daughter board is critical, a custom-made surface mount printed circuit board (PCB) was developed. The PC board is a two layer board with an FR-4 dielectric. The capacitors and inductors are all size 0805. The capacitors were purchased from Panasonic, and use the NPO dielectric. The inductors were purchased from Coilcraft and use a wirewound plastic core construction. A picture of the motherboard-daughterboard is shown in Figure A.2.1.

A.2: Test Setup

As described in Chapter 3 the main parameters measured for this amplifier are efficiency, output power, and distortion. Efficiency was measured by sensing the DC drain current supplied to the amplifier. Figure A.2.2 shows how this measurement was accomplished. A simple op-amp connected as a unity gain buffer was used as the voltage regulator. A resistor, R_{SENSE}, was enclosed in the feedback loop of the op amp. The drain current is monitored by simply measuring the voltage across R_{SENSE}. Since the resistor is in the feedback loop, it will have a negligible effect on the low impedance seen by the inductor. Also a capacitor C_B has been included so that a low impedance can be maintained at the V_{DD} node at high frequencies.

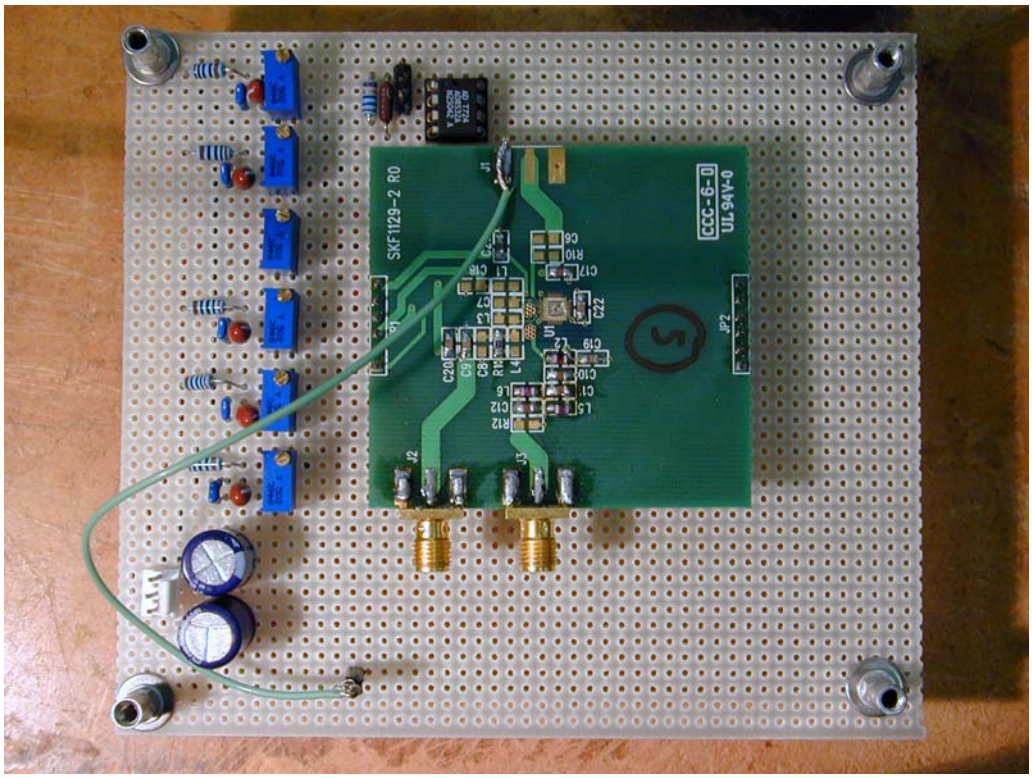

Figure A.2.1:RF Amplifier Testboard

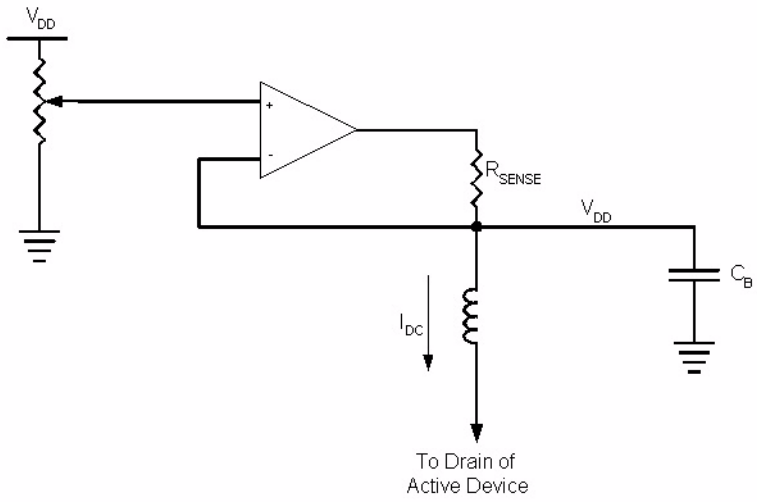

Figure A.2.2: Test Setup for Measuring Amplifier Drain Current

The output power was measured using the Tektronix 2782 100 Hz - 33 GHz spectrum analyzer. The signal generator was the HP 8656A 0.1 - 990MHz RF generator. A typical test setup showing the RF signal generator, spectrum analyzer, and test board is shown in Figure A.2.3.

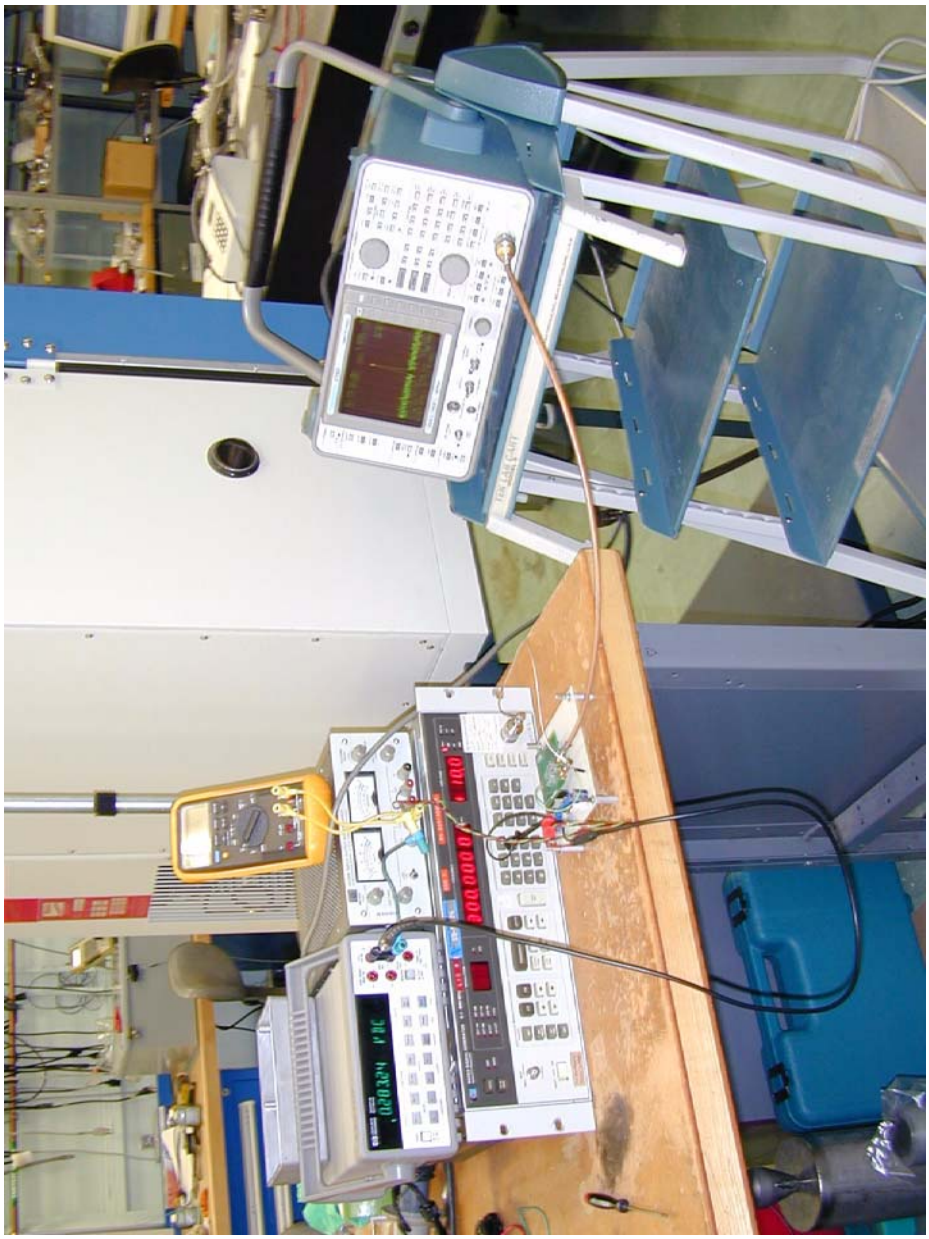

Figure A.2.3:Amplifier Measurement Setup

Appendix B: Host File for Class-E Amplifier Simulations

```
HOST FILE FOR CLASS-E AMPLIFIER - FINAL SIMULATIONS

.tran  10ps    3000ns  sweep   data=datafile
.options post = 0 method=gear delmax=2ps
.inc   'prgrnom.mod'
.inc   'passive.mod'
.inc   'datafile.swp'

.meas  tran    pavdc   avg     p(vdd)  from=2800ns     to=2900ns
 .meas  tran    p1      avg     p(r1)   from=2800ns     to=2900ns
 .meas  tran    p2      avg     p(r2)   from=2800ns     to=2900ns
 .meas  tran    p3      avg     p(r3)   from=2800ns     to=2900ns
 .meas  tran    p4      avg     p(r4)   from=2800ns     to=2900ns


 vin    30      0       sin(0.2 1.0     f0)

 xp3    30      3     pad
 $rlk   30      0      46.8

 vdd    200     0     vdd

 xdc2   200     40      l330
 xp2    40      4     pad


 m2     4       3       201     201     cmosnl  m=16    w=50u   l=0.5u dtemp = tmp
 xp1    201     202     pad
 rp1    202     0    10

 cs     40      0     2pf

 cs1    40      5      3pf
 xs1    5       6      l100

 xl4    6       7     l22
 c_4    6       7     3pf

 t1     7       0       15      0       z0=50   td=6n

 rl     15      test    50
 vfil   test    0   0

 ***post processing - decompose signal into harmonics

 f1     t1      0       vfil   1
 c1     t1      0    c1
 l1     t1      0    l1
 r1     t1      0    50

 f2     t2      0       vfil   1
 c2     t2      0    c2
 l2     t2      0    l2
 r2     t2      0    50

 f3     t3      0       vfil   1
 c3     t3      0    c3
 l3     t3      0     l3
 r3     t3      0    50

 f4     t4      0       vfil   1
 c4     t4      0    c4
 l4     t4      0    l4
 r4     t4      0    50


 .end
```

Vita

Stephen Terry was born in Abbington, Pennsylvania on August 16, 1978. He grew up in Germantown, Tennessee and graduated from Houston High School in 1996. Stephen entered the University of Tennessee in the fall of 1996 to pursue a degree in Electrical Engineering. While an undergraduate his studies focused on electronic design and communication systems. Stephen completed his undergraduate degree in May 2000 and received the Bachelor of Science in Electrical Engineering, *Cum Laude*. On May 20, 2000 Stephen was married to the former Rebecca Susan Moore of Memphis, Tennessee.

After completing his undergraduate education Stephen began work on the Master of Science degree in the UT/ORNL Joint Program. As a member of the Joint Program he worked as a part-time research assistant at the Oak Ridge National Laboratory and attended classes at UT. Stephen was awarded the Analog Devices Fellowship while he was a member of the Joint Program.

After completing his Master's degree he will pursue the Ph.D. in Electrical Engineering under the direction of Professor Benjamin J. Blalock. Stephen's professional interests include RF systems, high temperature electronics, and analog and digital signal processing.