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A LOW-POWER APPROACH FOR FRONT END BIOLOGICAL SIGNAL CONDITIONING

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To the Graduate Council:

I am submitting herewith a thesis written by Logan Smith Taylor entitled "A LOW-POWER APPROACH FOR FRONT END BIOLOGICAL SIGNAL CONDITIONING." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

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A Low-Power Approach for Front End Biological Signal Conditioning

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Dedication

This thesis is dedicated to my grandmother, Viola Siebenthal Ergen, who departed this life, May 21, 2013. She is greatly missed by all of her family. Without her wise words and support this would never have become what it is.

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For me, completing a project like this thesis was only possible because I had excellent guidance, insightful wisdom and constant support and encouragement from everyone mentioned above. I am deeply thankful for the opportunity to work with such a great group of people.

Abstract

In a lab-on-a-chip (LOC) application, the measurement of small analog signals such as local temperature variation often involves detection of very low-level signals in a noisy micro-scale environment. This is true for other biomedical monitoring systems as well. These systems observe various physiological parameters or electrochemical reactions that need to be tracked electrically. For temperature measurement pyroelectric transducers represent an efficient solution in terms of speed, sensitivity, and scale of integration, especially when prompt and accurate temperature monitoring is desired.

The ability to perform laboratory operations on a small scale using miniaturized LOC devices is a promising biosensing technique. The advantages of using LOC include faster time of analysis, low reagent costs, and reduced amount of chemical wastes. The application of portable, easy-to-use, and highly sensitive LOC biosensors for real-time detection could offer significant advantages over the currently used analytical methods.

This thesis presents design and analysis of a low frequency charge amplifier suited for biological sample applications, with a wide window for signal size and speed. The charge amp has been fabricated in a commercial 180nm CMOS process. The circuit has been tested for signals in 100Hz-100kHz range with a max charge of 250nC.

This thesis begins with a study of the transducer that produces the charge for the charge amplifier. Next it moves into the design of low power charge sensitive amplifiers, along with an analysis of various components essential to the makeup of the design. The charge amplifier circuit is simulated using analytical model as well as numerical simulation tools. Finally, the test setup is presented and the measurement results are compared with those obtained from simulation.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction and Basic of Amplifiers

1.1 Motivations

Human life can become more comfortable with the integration of technology. Elderly patients in hospitals, terminally ill, and even diabetic patients can regain their independence through the use of sensors and monitoring technology. The increasing presence of monitoring devices in everyday life has brought many benefits to the patients. With the advent of biomolecule detection methods the ability to monitor glucose, lactose, oxygen, and pH levels are allowing healthcare providers to follow diseases more closely and prescribe a more appropriate plan of care. [1] Not only do these new monitoring techniques allow for more individual treatment, they are also safer for the patient. Previous methods of obtaining the samples allowed for increased risk of infection due to the invasive nature of collection [1]. Aside from being more sanitary, implantable devices are capable of processing advanced measurements. The primary target of such devices is the diabetic patient. The ability to accurately and continuously monitor blood chemistry results in better control over the treatment of the disease.

A refocusing of biomedical research and improvement of CMOS processing technologies have led to the realization of minimally invasive, implantable biosensors. With a reduced risk of infection and the ability to continuously monitor a patient, the realization of this lab-on-a-chip (LOC) advancement will undoubtedly result in increased quality of healthcare. LOC is a multidisciplinary research field that combines different analysis techniques carried out using integrated circuits (IC), integrated sensors, and more general micro electro-mechanical devices on the same chip [2]. LOCs offer advanced diagnostics capabilities for continuous monitors. While most are not currently implantable, LOCs remain minimally invasive, and are characterized by the small blood volume sample needed for complex tests.

Development of continuous monitoring systems offers a substantial advancement over conventional measurement devices. Through the use of lab-on-a-chip and continuous monitors, doctors and other medical personal are able to examine patient data almost in real time. By decreasing the intervals between the sample collection and the test results, the doctors are able to provide more timely medical intervention. In addition to this time benefit, data recorded from the devices allow for up to date medical history on the go.

In addition to the benefit for healthcare in developed countries, LOC will soon be an important combatant against terminal illness in other parts of the world. Through humanitarian organizations and philanthropic corporations, LOC can be made cheap enough to build and transport to countries where clean water is still not an everyday reality.

By using the lab-on-a-chip systems, detection of HIV/AIDS, Human African Trypanosomiasis (HAT), or everyday pathogens can be done on site increasing the chances that medical care can be administered early enough to save lives. [3,4]

Wearable and implantable devices have the potential to provide significant saving in terms of human life and dollars. In order for this technology to be successful, the design must be directed to inexpensive reproducible devices as well as maintaining accuracy and reliability. CMOS technologies have advantages such as small volume and reliable operation, in addition to manufacturing repeatability. Through the use of CMOS design more individualized methods can be constructed. Fig. 1.1 presents a scheme for implementation of an integrated circuit in a lab-on-a-chip as a portable platform.
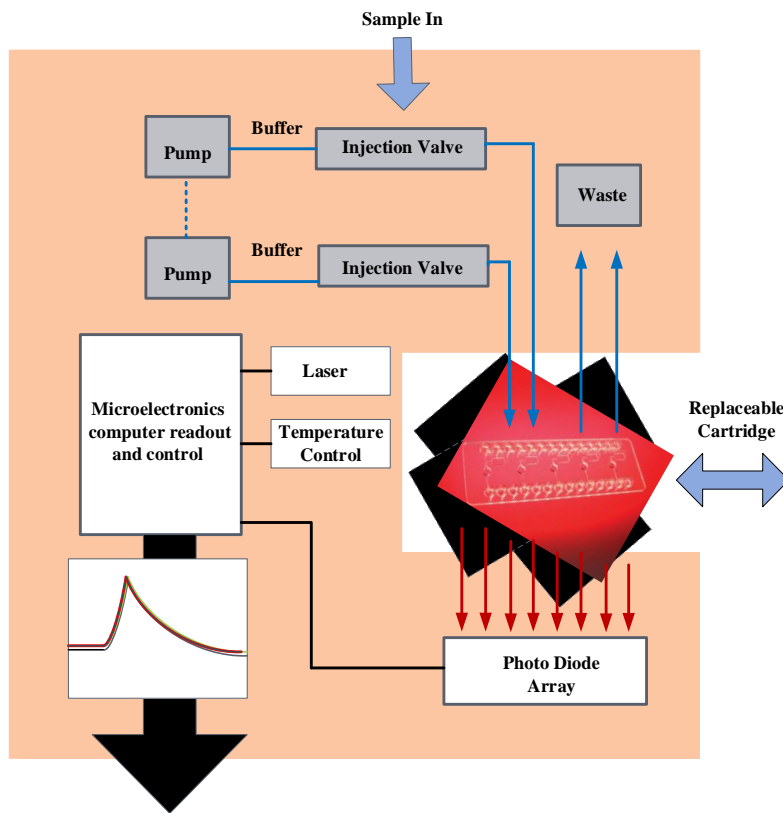
Figure 1.1 Schematic of an optical lab-on-a-chip system, for the analysis of enzymes within a biological sample.

Figure 1.2 shows examples of how implantable devices and lab-on-a-chip design can be integrated into the human body. Going from top to bottom, the first example is a contact lens that will measure the glucose concentration in tears for diabetic monitoring. It

connects wirelessly to a smart phone or designated wireless receiver to display and record the values. The second example is a microfluidic chamber that can be built to monitor the concentration of multiple biological enzymes or molecules. It would require about a micro liter of blood to operate, which is significantly less than using manual techniques. The third is an illustration of an electrochemical biosensor integrated on a microfluidic chip.

Soft Contact Lens
Glucose Sensor
Chip and Antenna

Glass lab on a chip for beta cell detection

Integrated Lab on a chip
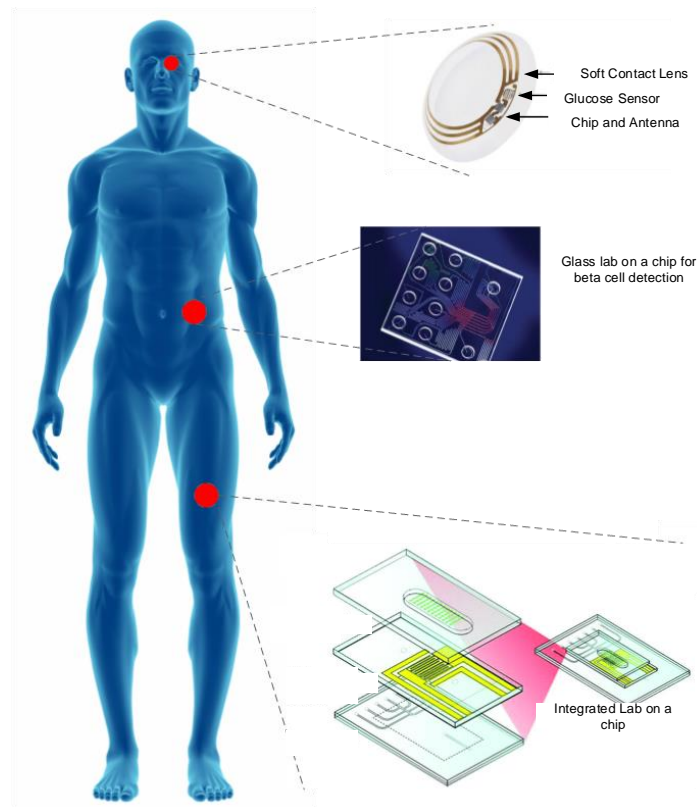
Figure 1.2 Examples of implantable and lab-on-a-chip technology. Top to bottom: contact lens glucose sensor, beta cell glass lab on a chip, and generic integrated circuit lab on a chip.

From the illustrations above, design of these systems emphasizes small size and easy maneuverability, while maintaining precision and accuracy of much larger systems. The system shown above is broken down into three main sections, the microfluidic chamber, followed by the signal processing and the power supply. A benefit of the microfluidic technique is that there is no need for a power supply, however for some more complicated measurements the integrated CMOS circuitry will require power supplies. However, advancement in CMOS technology has allowed both the power supply and the

processing circuitry to scale down. This can be explained by Koomey's Law and Moore's Law. By optimizing power distribution on-chip the overall size of the system can be minimized. The first place to start in optimization is to make more efficient topologies that make use of less complex power schemes. In order to minimize the power consumption of the circuits, higher-end CMOS process technologies can be employed [5]. The second step in reducing the area of a chip is realizing topologies that lump performance and accuracy into smaller circuits, which then goes back to having less of a power requirement.

Through this trend recent achievements include moving from the printed circuit board (PCB) design with discrete components to the application specific integrated circuit (ASIC) design. [6] However, some systems can be more easily employed through PCB design using discrete devices. The application of this proposed design will be to overcome the barriers of large component design and move to an ASIC system. In this thesis a pyroelectric sensor that outputs a large amount of charge will be analyzed and a preamplifier for converting the charge to voltage will be presented.

1.2 Research Goals

The purpose of this research is to develop a low-voltage and low-power preamplifier for integration with pyroelectric and piezoelectric sensors, which will be used in lab-on-a-chip platforms similar to the systems shown in Fig. 1.2. These systems differ from the traditional application of charge amplifier due to the slow signal and large amount of charge. The final design will be capable of preforming the conversion from charge to voltage at readable level in the hundreds of milliamps. The final design demonstrates the capability of ASIC design to be implemented in place of traditional discrete systems.

1.3 Overview

In Chapter 1, a lab-on-a-chip system and the corresponding circuit compositions are introduced. This is followed by a discussion on the importance of the low-voltage and low-power design and it implications for the overall system. A low-voltage charge sensitive pre-amplifier for current to voltage conversion is set to be the research goal of this thesis. In Chapter 2, various topologies are introduced, which is followed by a discussion their individual merits. In Chapter 3, the low-voltage design techniques use in this work will be explained. Following the selection of the appropriate preamplifier design technique as well as problems associated with the selected topology are discussed. To provide novel circuit design techniques for solving these problems, the details for the implementations of the charge amplifier are presented in the later part of Chapter 3 along with the simulation results. Experimental measurements of the proposed design are shown in Chapter 4. Finally in Chapter 5, conclusions and future work are presented.

Chapter 2

Literature Review

In this chapter, different types of biomedical systems, both implantable and portable lab-on-a-chip, and their working principles are introduced in Section 2.1. Lab-on-a-chip systems are designed to translate a biological signal into a digital signal that can be interpreted by trained individuals. The biological signal is commonly read using electrodes connected to a transducer, which creates a charge that can be altered by electronics to achieve a reliable accurate output. Section 2.2 will explain the flow from signal generation to signal output by discussing the many different components that make up a detector's system. The components of a detector system include the detector or the sensor itself, a charge sensitive preamplifier, a pulse shaper, a discriminator, and other stages that allow for the signal to amplified and filtered for user interaction. The main focus of this work will be the charge sensitive preamplifier and the signal input.

2.1 Introduction to Lab-on-a-Chip (LOC)

Since the introduction of soft lithography in the late 1990s, microfluidic and lab-on-a-chip technologies have given rise to vast numbers of scientific and technological developments [3]. However, the devices span a broad platform of biological testing concepts, including blood separation, chemical reactions, and integration with various sensing/detecting components. The last category includes working in combination with optical sensing, electrochemical signal sensing, field effect transistors (FET), and nuclear magnetic resonance (NMR) [3]. A lab-on-a-chip system in general consists of two main components, namely, the sensing component, and the microelectronics processing unit [7].

The sensing component is typically, a biosensor consisting of receptors that can sense changes in the sample, an interface architecture where a specific biological or biochemical signal is generated, and the transducer element converting the signal to another form of signals for detection [8]. Biosensors are divided into categories based on the method of signal transduction such as mass, electrochemical, thermal, or optical. Furthermore, biosensors can be classified as either direct-detection or indirect-detection systems. Direct-detection biosensors are designed such that the specific biochemical reaction, or target analyte, is measured directly by the transducer. In contrast, indirect-detection biosensors are those in which a preliminary biochemical reaction takes place and the products of this reaction are detected by the transducer [9]. Each of these is designed to detect certain biological element and its concentration at the site of testing. Some recognition elements used in biosensors are: enzymes, nucleic acids, antibodies, whole cells, and receptors. Among these, enzymes are the most commonly used [10].

This section attempts to describe operating principles of electrochemically-based biosensors by reviewing the structure and theory. The theory transcends the electrochemical approach, as it is applicable to other transducer types as they are responding to biostimuli and converting it to electrical signals.
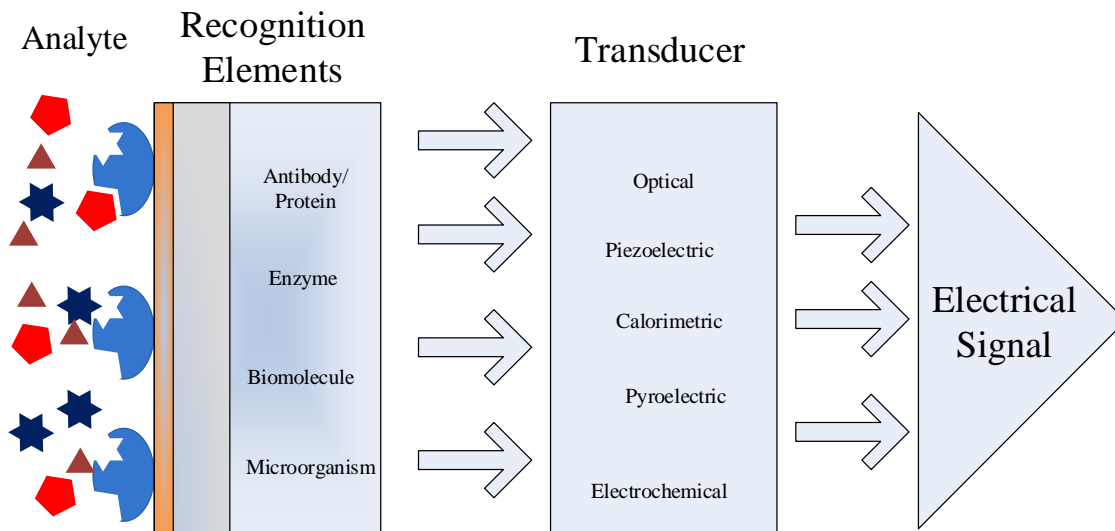
Figure 2.1: Flow chart of a biosensor.

As figure 2.1 demonstrates there are a vast number of combinations for biological sample collection and measurement. The primary means of transduction is electrochemical. By the natural of being electrochemical, the transduction element is served by a bioelectrochemical component. As mentioned above the bioelectrochemical components, include enzymes, nucleic acids, antibodies, whole cells, and receptors. Enzymes, due to their specific binding capabilities and biocatalytic activity, are often the predominant choice in implemented technique. [11]

Characteristically in electrochemistry, the reaction under investigation would either generate a measurable current (amperometric), a measurable potential or charge accumulation (potentiometric) or measurably alter the conductive properties of a medium (conductometric) between electrodes [9]. Each method will be introduced in this section. However something common to each case is that the reactions are generally detected only in close proximity to the electrode surface. Therefore the electrodes themselves are responsible for the performance of the biosensors. Detection ability and sensitivity are based on the chosen function, the electrode material, its surface modification, and its

dimensions. Electrochemical sensing usually requires a three electrode system. An example of the electrode system is shown in Figure 2.2.
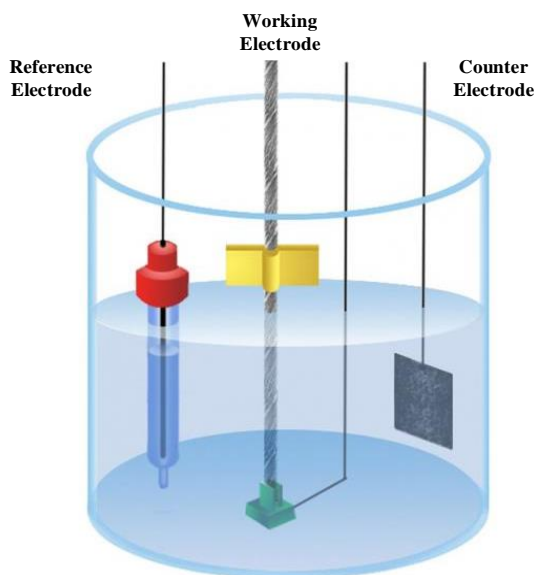
Figure 2.2: Electrochemical biological sensor using the three electrode system [12].

First a reference electrode, commonly made from Ag/AgCl, is kept at a distance from the reaction site in order to maintain a known and stable potential. Second a counter or auxiliary electrode, establishes a connection to the electrolytic solution so that a current can be applied to the working electrode. Lastly the working electrode, also known as the sensing or redox electrode, serves as the transduction element in the biochemical reaction. These electrodes should be both conductive and chemically stable. Therefore, platinum, gold, carbon (e.g. graphite) and silicon compounds are commonly used, depending on the analyte [12]. Most modern amperometric-based sensing methodologies typically employ a three-electrode sensor system, due to the difficulty for the system to control an electrode by supplying a constant voltage and a varying current at the same time. The three-electrode electrochemical cell can also be modeled by physical resistors and capacitors as shown in Fig. 2.3.

Here, the value of resistors R_{WE}, R_{RE} and R_{CE} represent the Faradic resistances of the working, reference and counter electrodes, respectively, while the value of resistors R_{S1} and R_{S2} represent the solution (analyte) resistances.

The resistance of R_{WE} can be calculated in Eq.(2.1) as,

$$R_{WE} = \frac{E_i}{I_F} \qquad\qquad (2.1)$$

The resistance of R_{CE} is much smaller than that of R_{WE} since the size of the counter electrode is normally developed to be much smaller than that of the working electrode. The resistances of R_{S2} and R_{S1} are even more negligible compared to the rest. The value of capacitors C_{WE} and C_{CE} correspond to the electrode double-layer capacitances. They are proportional to the surface areas of each electrode.
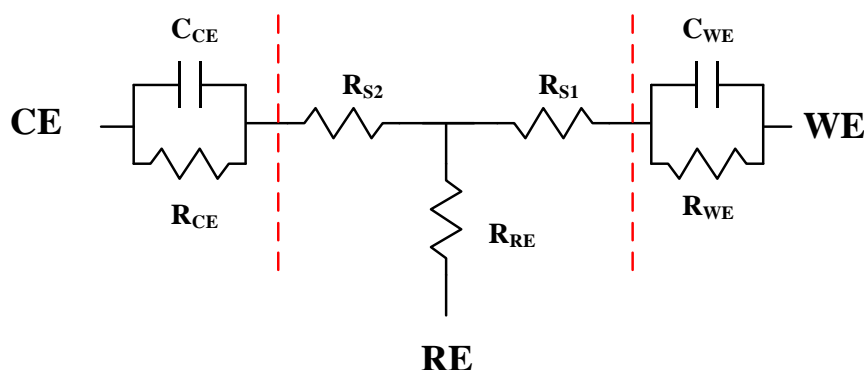
Figure 2.3: Equivalent circuit representation of three electrode system.

2.1.1 Amperometric Devices

The potentiostat system mentioned above is considered to be an amperometric device. Amperometric devices continuously measure current resulting from the oxidation or reduction of an electro-active species in a biochemical reaction [3]. The purpose of such sensors is to generate a potential difference E_i between the working and the reference electrodes such that specific analyte can be detected.

Another example of amperometric sensing is the Clark oxygen electrode. This is the most basic form of amperometric biosensors, where a current is produced in proportion to the oxygen concentration. This is measured by the reduction of oxygen at a platinum working electrode in reference to an Ag/AgCl reference electrode at a given potential [13]. The system is seen below in Figure 2.5 along with the chemical reaction occurring in the biosensor.
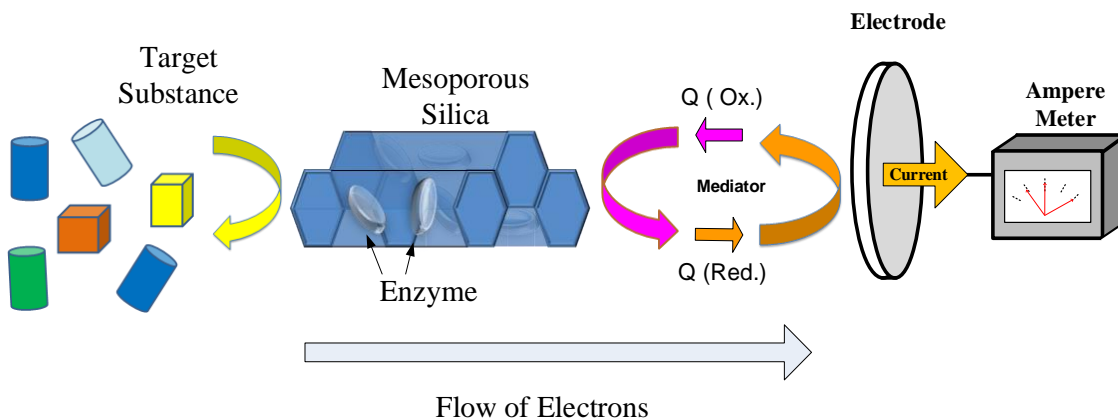
Figure 2.4: Amperometric biosensor with transduction element.

Ag anode $4Ag + 4Cl^- \rightarrow 4AgCl + 4e^-$
Pt cathode $O_2 + 4H^+ + 4e^- \rightarrow 2H_2O$
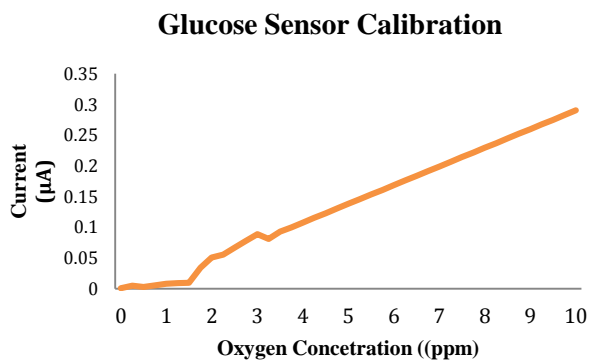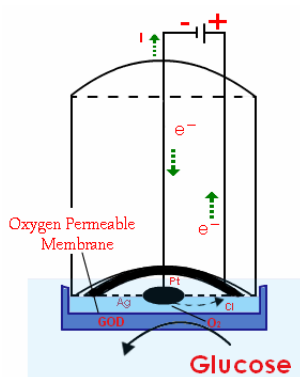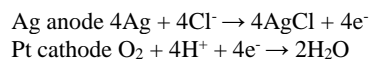
Figure 2.5: Clark oxygen sensor and example of an amperometric sensor.

The rate of electrochemical reduction depends on the rate of diffusion of the oxygen from the bulk solution, which is directly related to the concentration gradient and the bulk oxygen concentration. The reduction allows a current to flow, which generates a potential

difference that is recorded by the transducer. Despite the disadvantage of this often indirect sensing system, it is claimed that amperometric devices maintain sensitivity superior to many other devices [14].

2.1.2 Piezoelectric Devices

Biosensors are not limited to the detection of purely biological substances, some sensors measure physical characteristics such as luminescence, stress, or heat. Piezoelectric behavior is where an electric potential may be induced in the material through the application of a force and vice versa. Examples of naturally occurring materials that exhibit this type of behavior are quartz crystals and Rochelle salt. There are many artificial piezoelectric materials such as polyvinylidene fluoride (PVDF), barium titanate ($BaTiO_3$), lithium sulphate (LS), and lead zirconium titanate (PZT). The conversion of electrical pulses to mechanical movement and the conversion of mechanical movement back into electrical energy is the basis for piezoelectric crystals. The active element is the heart of the transducer as it converts the electrical energy to mechanical energy and vice versa. The active element is a piece of polarized material (i.e., some parts of the molecule are positively charged, while other parts of the molecule are negatively charged) with electrodes attached to two of its opposite faces. When an electric field is applied across the material, the polarized molecules will align themselves with the electric field, resulting in induced dipoles within the molecular or crystal structure of the material. This alignment of molecules cause the material to change dimensions. This phenomenon is known as electrostriction. In addition, a permanently polarized material, such as quartz (SiO_2) or barium titanate ($BaTiO_3$), will produce an electric field when the material changes dimensions as a result of an imposed mechanical force. This phenomenon is known as the piezoelectric effect.[15]

In order to utilize this physical principle to make a sensor to measure force, one must be able to measure the surface charge on the crystal. A common method of using a piezoelectric crystal to make a sensor is to use two metal plates to sandwich the crystal, thus making a capacitor. This capacitor is shown in the figure 2.6.

As mentioned previously, an external force causes a deformation of the crystal and results in a charge that is a function of the applied force. In its operating region, a greater force will result in more surface charge. This charge results in a voltage.

$$V = \frac{Q_f}{C}$$

<div align="right">(2.2)</div>
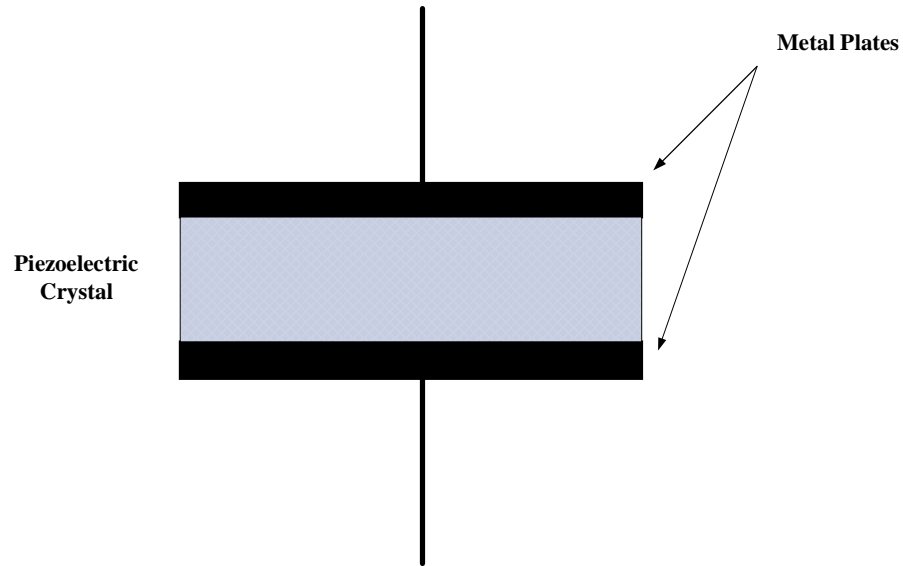
Figure 2.6: Piezoelectric crystal as a capacitor.

Where Q_f is the charge resulting from a force f, and C is the capacitance of the device. In the manner described above, piezoelectric crystals act as transducers that turn force or mechanical stress into electrical charge, which, in turn, can be converted into a voltage. Alternatively, if one were to apply a voltage to the plates of the system described above, the resultant electric field would cause the internal electric dipoles to realign, which would cause a deformation of the material. An example of this reverse piezoelectric effect is the functionality of speakers.

Figure 2.9 shows two possible configurations in which the piezoelectric sensor can be operated. In the first case, the force axis and the voltage difference that is being measured are both longitudinal, whereas in the second case, they are transverse. [14]

To model the piezoelectric sensors, one can take into account the following sets of relationships. The charge induced in the crystal is directly proportional to the deformation in the crystal and the voltage induced is similarly proportional to the force applied. Thus the relationships can be expressed as,

$$Q = n_{tr}\Delta x \qquad\qquad\qquad (2.3)$$

$$F = n_{tr}V \qquad\qquad\qquad (2.4)$$

where n_{tr} is the transformer modulus (or the proportionality factor). Relating force to stress and subsequently to strain and displacement this same equation can be modified such that:

Direct Piezo Effect : Mechanical Stress => Electrical Charges

Reverse Piezo Effect : Electrical Signal => Mechanical Strain
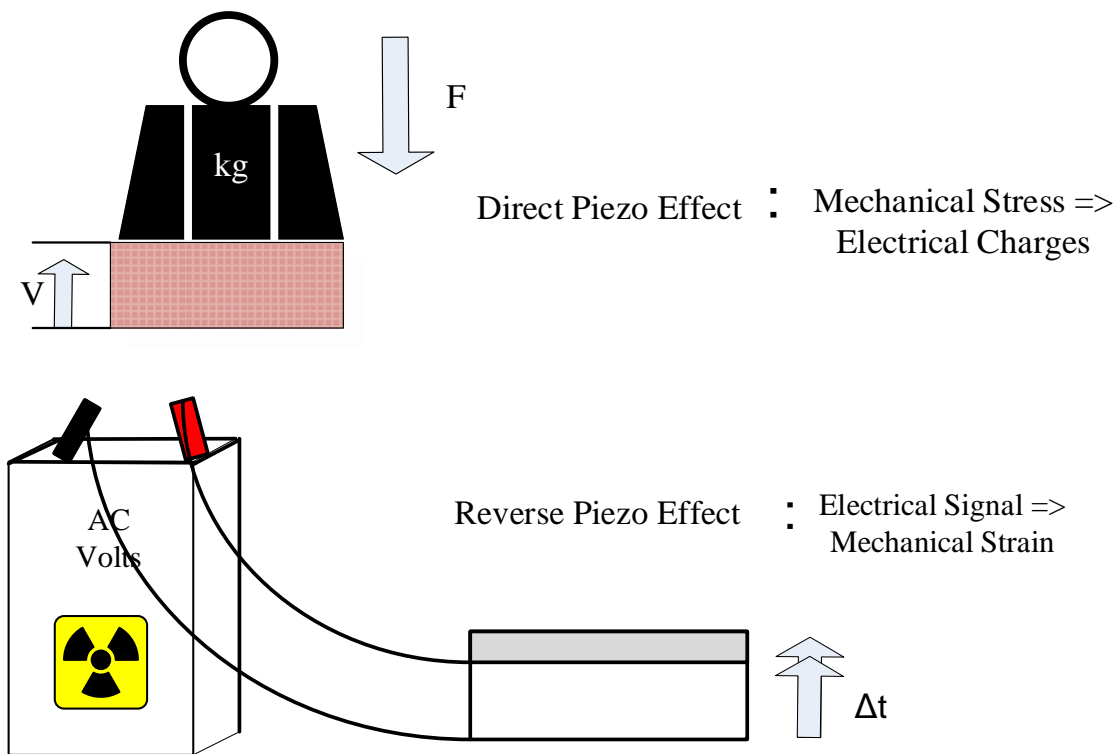
Figure 2.7: (a) Forward piezoelectric effect and (b) reverse piezoelectric effect.

$$n_{tr} = \frac{nd_{33}AE}{x} \qquad (2.5)$$

where d_{33} is the piezoelectric charge constant, also known as the piezoelectric coefficient, along the 3-3 direction or the longitudinal direction. If the force were perpendicular to the direction of voltage measurement, the constant would be different and it would represented using the symbol d_{31}. Finally, on the electrical side, the voltage and the charge are related

through the capacitance in the piezoelectric crystal in a similar manner. Where *n* is the number of layers [15]. The important thing to note here is the charge residing in the capacitor. The later sections of this chapter will describe how to remove this charge and use it as an electrical signal.

2.1.3 Pyroelectric Devices

Similar to piezoelectric devices in operation principals, pyroelectric devices sense heat change instead of motion. Heat monitoring is especially useful for enzymatic reactions, the generation of heat (enthalpy change) can be used easily and generally. The enzyme provides selectivity and the reaction enthalpy cannot be confused with other reactions from species in a typical biologic mixture. The ideal aim is to measure total evolved heat. In real systems there is always heat loss. As a result, temperature difference before and after evolution is measured most often. It has to be assumed that the heat capacity of the specimen and the container is constant over the small temperature range usually measured. The simplest transducer is a thermometer coated with the enzyme that permits the selected reaction to proceed. Thermistors are used rather than thermometers or thermocouples due to the sensitivity of heat change required for these measurements [3]. The evolving leader in temperature measurement however is the pyroelectric transducer.

As with the piezoelectric case above a pyroelectric material can be considered a composition of a large number of minute crystallites, where each behaves as a small electric dipole. All these dipoles are randomly oriented, however, along a preferred direction. Above a certain temperature, known as the Curie point, the crystallites have no dipole moment. This is illustrated by the figure below.
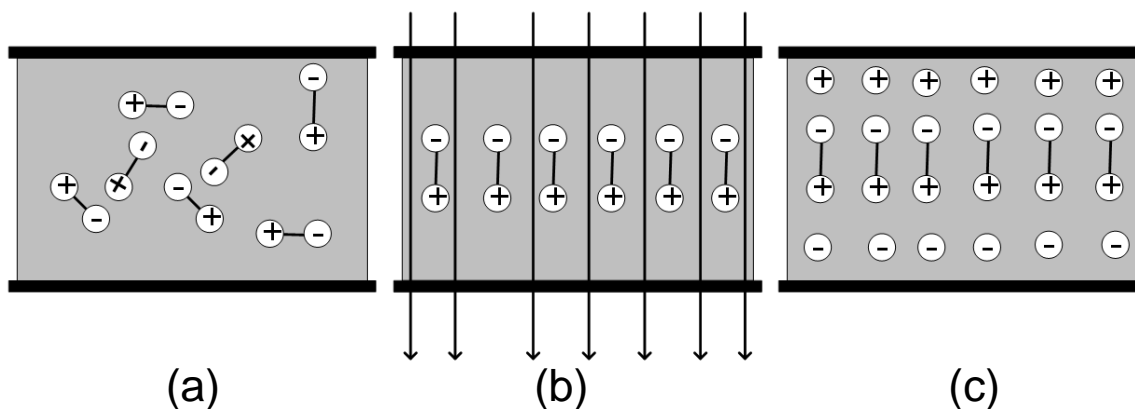
Figure 2.8: Poling of pyroelectric crystal in a strong electric field. (a) randomly oriented (b) dipoles aligning with electric field (c) dipoles frozen at high temperature.

When temperature of a pyroelectric material changes, the material becomes polarized. In other words, an electric charge appears on its surface. It should be clearly understood that the polarization occurs not as a function of temperature but only as function of a *change in temperature* of the material. Temperature changes can cause shortening or elongation of individual dipoles. It can also affect the randomness of the dipole orientations due to thermal agitation. These phenomena are called *primary pyroelectricity*. There is also *secondary pyroelectricity*, which, in a simplified way, can be described as a result of the piezoelectric effect, that is, a development of strain in the material due to thermal expansion [17]. Therefore some material can be both piezoelectric and pyroelectric.

The dipole moment, *M,* of the bulk pyroelectric sensor is

$$M \ = \ \mu A h \tag{2.6}$$

Where μ is the dipole moment per unit volume, A is the sensor's area, and h is the thickness. The charge, Q_a, which can be picked up by the electrodes, develops the dipole moment across the material:

$$M_0 = Q_a h \tag{2.7}$$

M must be equal to *M*$_0$ so that

$$Q_a \ = \ \mu A \tag{2.8}$$

As the temperature varies, the dipole moment also changes, resulting in an induced charge. Thermal absorption can be related to a dipole change so that μ must be considered a function of both temperature, T_a, and an incremental thermal energy, ΔW, absorbed by the material:

$$\Delta Q_a \ = \ A\mu(T_a, \Delta W) \tag{2.9}$$

Table 1: Various Effects in Ferroelectric Materials

Input \ Output	Charge Current	Magnetization	Strain	Temperature	Light
Electric field	Permittivity Conductivity	Electro magnetic effect	Converse piezoeffect	Electric caloric effect	Electro-optic effect
Magnetic field	Magnetic electric effect	Permeability	Magnetostriction	Magnetic caloric effect	Magnetic optic effect
Stress	Piezoelectric effect	Piezomagnetic effect	Elastic contant	----	Photoelastic effect
Heat	Pyroelectric effect	----	Thermal expansion	Specific heat	----
Light	Photovoltatic effect	----	Photostriction	----	Refractive Index

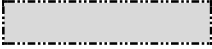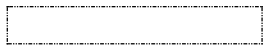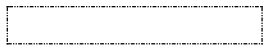Diagonal coupling   Actuator

Sensor

As the temperature varies, the dipole moment also changes, resulting in an induced charge. Thermal absorption can be related to a dipole change so that μ must be considered a function of both the temperature, T_a, and an incremental thermal energy, ΔW, absorbed by the material:

$$\Delta Q_a = A\mu(T_a, \Delta W) \hspace{3cm} (2.10)$$

The aforementioned equation shows the magnitude of electric charge resulting from absorption of thermal energy. To pick up the charge, the pyroelectric materials are fabricated in the shapes of a flat capacitor with two electrodes on opposite sides and the pyroelectric material serving as a dielectric, similar to figure 2.8.

2.2 System Electronics

This section will be focused on a specific design for a pyroelectric transducer and preamplifier. Lab-on-a-chip-based analysis has made significant progress towards acceptance as a viable tool for use in biomedical investigation. As far as microbiological systems are concerned, sensor technology plays a key role in measurement accuracy and, as the scale of integration increases, the realization of higher performance sensors becomes an essential requirement. In applications such as micro-electrophoresis and polymerase chain reaction (PCR), in which thermal monitoring of a biological fluid is required, conventional equipment is replaced by the lab-on-a-chip thanks particularly to its high surface-to-volume ratio and the short thermal path [18]. Different transducer technologies, such as those based on thermocouples, thin-film-on-silicon and bolometers were investigated for temperature and heat-flux monitoring. Infrared (IR) radiation has been used for non-intrusive measurements of local temperature [18]. In addition, techniques based on a temperature gradient were employed for the separation of analytes into microchannels through the use of the fluorescence thermometer. In the case of microelectrophoresis, the application of strong electric fields results in local heating, especially in the reservoirs, and thus the degradation of biological samples. It is in this degradation of samples that monitoring becomes difficult. One approach to gaining the ability to monitor the temperature of the sample is through the use of pyroeletric transducers. They are again composed of a material that does not require any electric source to work while only the signal itself requires electronics, making sample monitoring a good fit.

The main advantages of employing the pyroelectric transducer are faster response, greater flexibility in terms of shape and layout, and the lack of an energy supply. The drawback concerning its use as a temperature transducer is depolarization at relatively high temperatures and its dynamic response as compared to other devices.

In previous work [18] investigation into the application of the ferroelectric polymer polyvinylidene fluoride (PVDF) was done for the monitoring of temperature variations of biological substances in a microchannel system. The development of a polymertransducer

allows the use of active elements having reduced dimensions for localized temperature measurement. The result of the paper was a pyroelectric transducer that will monitor the temperature change in biological systems. The work also consisted of a readout circuit which will be the focus of this paper. The system will be broken down in the sections below.

2.2.1 Signal Formation

When a change in temperature is detected by a pyroelectric detector, ions are created. This change in the temperature event creates an accumulated charge proportional to the physical properties of the detector.

Electronically, a polyvinylidene fluoride (PVDF) pyroelectric detector is essentially a capacitor that can be charged by an influx of heat. The detector does not require any external electrical bias (excitation signal). It needs only an appropriate electronic interface circuit to measure the charge. Figure 2.11 shows a pyroelectric detector (pyrosensor) connected to a resistor R_b that represents either the internal leakage resistance or a combined input resistance of the interface circuit connected to the sensor. The equivalent electrical circuit of the sensor is shown in Figure 2.12.
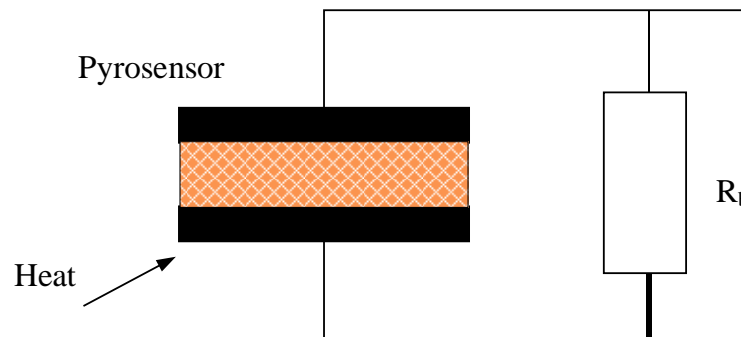
Figure 2.9: Schematic of a typical pyroelectric detector.

The circuit consists of three components: (1) the current source generating a heat-induced current, i (remember that a current is a movement of electric charges); (2) the sensor capacitance, C; and (3) the leakage resistance, R_b. Since the leakage resistance is very high and often unpredictable, an additional bias resistor is often connected in parallel with the pyroelectric material. The value of that resistor is much smaller than the leakage resistance, yet its typical value is still on the order of 10^{10} Ω (10 GΩ).

    The output signal from the pyroelectric sensor can be taken in the form of either charge (current) or voltage, depending on the application. Being a capacitor, the pyroelectric device is discharged when connected to a resistor, R_b. The electric current through the resistor and voltage across the resistor represent the heat flow–induced charge [17]. From the thermal point of view, the pyroelectric element can be modeled by an equivalent circuit, as shown in Fig. 2.12, where W [W/m^2] is the heat flux [19].
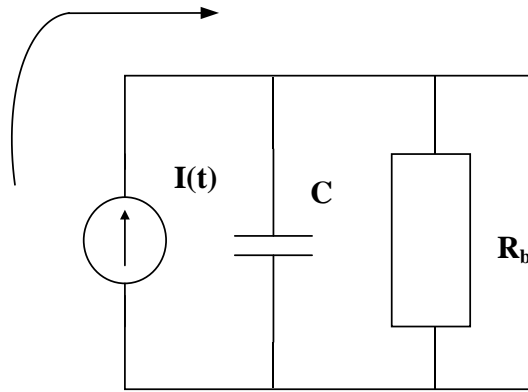
Figure 2.10: Equivalent circuit of pyroelectric transducer.

Its response is characterized by the thermal time constant τ_{th}, which is the time needed by the detector to electrically respond when a thermal input flux occurs. It can be defined as follows,

$$\tau_{th} = C\,R \tag{2.11}$$

Thus in the design of a temperature sensor, a reduction in thickness of the transducer element leads to a faster temperature transducer. By taking into account the temperatures of the lower $T_{L(t)}$ and upper T_U (maintained at constant room temperature) surfaces of the sensor, their difference $T_P(t)=T_L(t)-T_U$, is deduced by the transfer of energy into the sensor. Since the response is directly related to the thermal behavior of the device and the main transduction mechanism is the energy conversion due to variations in temperature along the channel, the theoretical response describing the thermal evolution onto the transducer surface can be expressed as,

$$W = C_{th} \frac{dT_p(t)}{dt} + \frac{T_p(t)}{R_{th}} \qquad\qquad (2.12)$$

The temperature response which produces pyroelectric activity when the temperature through the sensing area changes, is obtained by solving (2.14) as,

$$T_p(t) = T_f(1 - e^{\frac{-t}{\tau_{th}}}) \qquad\qquad (2.13)$$

where T_f is the steady-state over-temperature experienced by the transducer. As a thermal variation occurs it responds within a time characterized by a constant τ_{th}, generating, respectively, a variation of spontaneous polarization and an electric field. Compared to that of other thermal transducers, the time response of pyroelectric materials is much less because they do not need to reach thermal equilibrium as is the case for thermistors and thermocouples [19].This charge or voltage typically takes a sensing circuit to detect.

2.2.2 Sensing Circuit

The charge amplifier can be implemented in many topologies. The simplest is shown below in Figure 2.11. This configuration is just a sensing capacitor in parallel with the detector capacitor. This design would allow the charge to build in the capacitor C_A resulting in a voltage V_{out} across the leads of the capacitor. This design is not suitable as it does not provide a measure of the total charge at the output. With the topology such as in figure 2.11 the charge are shared among various components so the output will not be proportional to the entire signal.

In order to fix this problem most designers gravitate to using a transimpedance configurations. This is considered the archetypal design for a charge sensitive amplifier. One simple version is shown in figure 2.18. It works by having a virtual ground at the input with a resistor pulling the charge from the input. It can also be observed that a device used in this manner is acting as an integrator, which for the equation above results in voltage.

The charge from temperature variation can be estimated either by analyzing the charge or the voltage generated by the transducer, which, from the electrical point of view, can be modeled by a pyroelectric current generator $Ip(t)$, a capacitor with losses C_0, and a resistance R_0, connected in parallel as shown in Fig. 2.13.
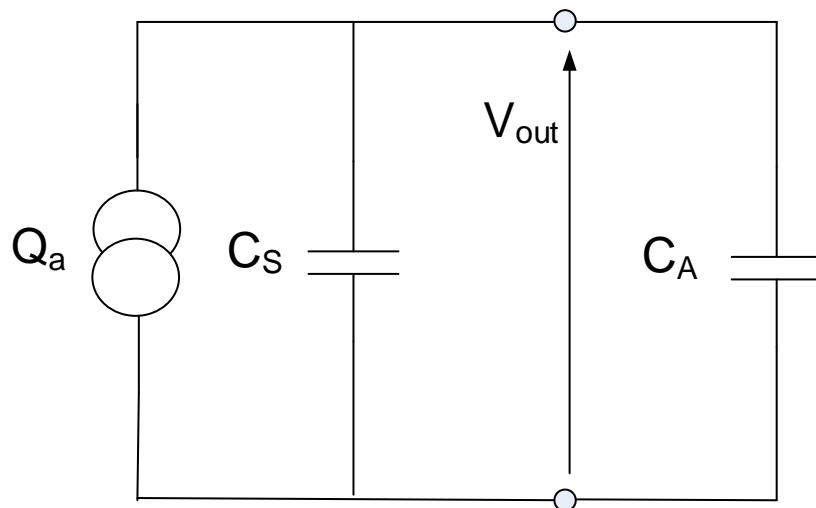
Figure 2.11: Schematic of a charge amplifier circuit.

A charge amplifier is designed to convert the temperature-dependent charge generated on the metal electrodes to a proportional voltage. The low input impedance of the charge amplifier is advantageous because C_0, R_0, and the connecting cable do not affect the signal even if they are subjected to thermal variations.
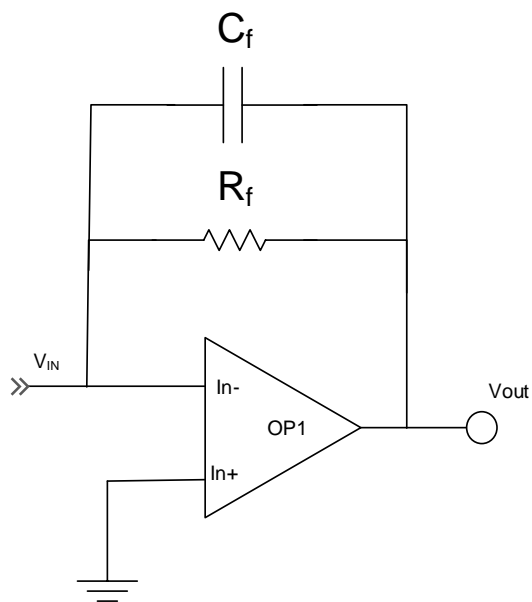
Figure 2.12: Schematic of a transimpedance charge amplifier circuit.
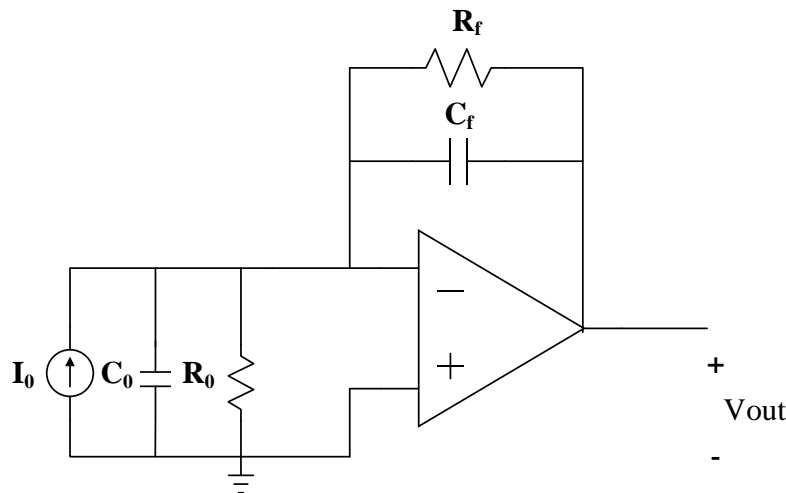
Figure 2.13: The basic sensing circuit using charge integrator at the core.

Moreover, it is less sensitive to electromagnetic interference and the frequency response is linear at higher frequencies. The charge generated, $Q_p(t)$ is forced to transfer itself from C_0 into the feedback capacitor C_f, which generates a proportional voltage across its terminals. The feedback capacitance is designed to be much larger than C_0 in order to make the transfer process independent from the transducer and any other stray capacitances. In order to render the charge generated by the pyroelectric effect suitable for further processing, an operational amplifier with a high gain-bandwidth product (GBW), a high signal-to-noise ratio (SNR) and a slew-rate (SR) is preferable. Moreover, the chief requirements of importance for the operational amplifier circuit are high input impedance for obtaining efficient charge transfer and a very large open loop gain [20].

The circuit below represents the equivalent circuit of the one displayed above in figure 2.13. By exampling the equivalent model the equation analyzing the components become similar allowing for quicker more accurate expectation of circuit performance.
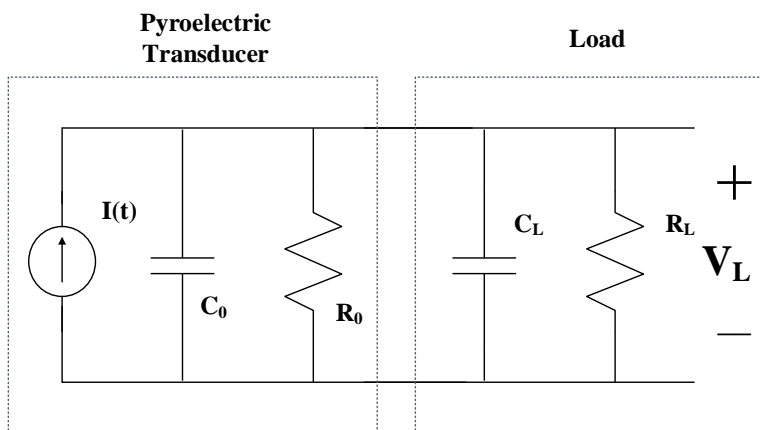
Figure 2.14: Equivalent circuit model of the sensing system.

2.3 Charge Sensitive Amplifiers

This section will discuss the subtleties in converting the signal produced in previous chapters to a usable voltage that can be processed. It will introduce the archetypal charge amplifier used for many circuit applications. Figure 2.13 is a simplified circuit of an entire preamplifier sensing and amplifying network. Below is an example of a full pyroelectric system.
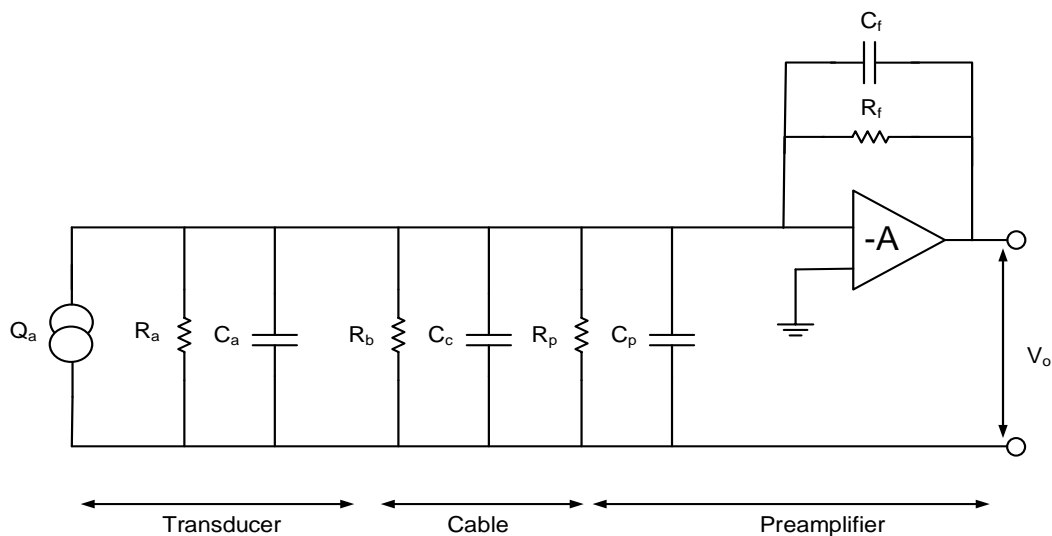
Figure 2.15: Example circuit of pyroelectric sensor with preamplifier connected.

In the circuit above there are three section described, a transducer element, a connecting medium and the preamplifier. The nomenclature is as follows.

Q_a: Charge generated by the pyroelectric transducer
R_a: Resistance of the transducer
C_a: Capacitance of the transducer
R_b: Resistance between the cable and center conductor (not always present)
C_c: Capacitance of cable
R_p: Resistance of the preamplifier
C_p: Capacitance of preamplifier
R_f: Feedback resistor
C_f: Feedback capacitance
A: Gain of operational amplifier
V_o: Voltage output of preamplifier

Using this model and analysis approach the conversion of charge to voltage will be described.

2.3.1 Theory of Conversion

The sensing circuit more often than not is a charge amplifier configured as seen in figure 2.15. The charge amplifier at is core has an operational amplifier. The amplifier is used to enhance the signal-to-noise ratio and for converting the charge into a useable voltage signal. Using the circuit above and associated microelectronic theory an understanding can be reached on how the charge is converted to voltage.

Taking the circuit in figure 2.15 into consideration and simplifying it to the base elements allows for simpler means of analysis. The figure below is the equivalent circuit of figure 2.15. Where the equations and the meanings are now:

Q_a: Charge generated by the pyroelectric transducer
R_t: Total resistance
C_t: Total Capacitance
R_f: Feedback resistor
C_f: Feedback capacitance
A: Gain of operational amplifier
V_o: Voltage output of preamplifier
I: Total current flowing out of transducer
I_c: current in feedback loop
I_i: current from total capacitive element.
V_c: Voltage across feedback resistance
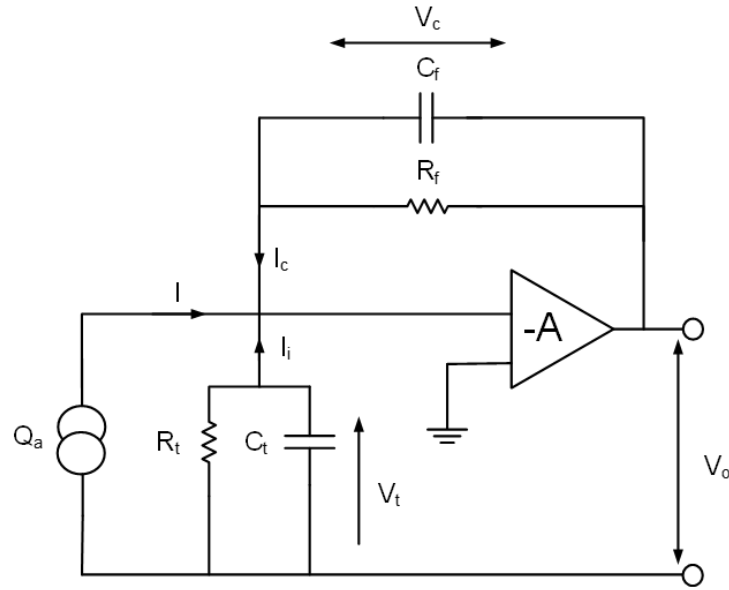
Figure 2.16: Equivalent circuit of pyroelectric transducer connected with preamplifier.

$$\frac{1}{R_t} = \frac{1}{R_a} + \frac{1}{R_b} + \frac{1}{R_p} \qquad (2.14)$$

$$V_o = -AV_i \qquad (2.15)$$

$$V_c = \left(1 + \frac{1}{A}\right) V_o \qquad (2.16)$$

$$I_c = C_f \frac{dV_c}{dt} + \frac{V_c}{R_t} = \left(1 + \frac{1}{A}\right)\left[C_f \frac{dV_o}{dt} + \frac{V_o}{R_f}\right] \qquad (2.17)$$

$$I_i = C_f \frac{dV_i}{dt} + \frac{V_i}{R_t} = \left(\frac{1}{A}\right)\left[C_t \frac{dV_o}{dt} + \frac{V_o}{R_t}\right] \qquad (2.18)$$

$$\frac{dQ_a}{dt} = -\left(1 + \frac{1}{A}\right)\left[C_f \frac{dV_o}{dt} + \frac{V_o}{R_f}\right] - \left(\frac{1}{A}\right)\left[C_t \frac{dV_o}{dt} + \frac{V_o}{R_t}\right] \qquad (2.19)$$

The final equation above can be further solved using integration and the final result comes out to be equation 2.21.

$$V_o = -\frac{Q_a}{\left(1+\frac{1}{A}\right)\left[C_f+\frac{1}{jwR_f}\right]+\left(\frac{1}{A}\right)\left[C_t+\frac{1}{jwR_t}\right]} \qquad (2.20)$$

This is very helpful in coming up with how the conversion is done. It also allows for sizing of the resistors and the capacitors to accommodate specifications of the circuit.

2.3.2 Design Problems with Charge Amplifiers

When dealing with charge there are some design constraints that have to be considered. Noise is a major concern for LOC systems. Past works have been done on optimizing the noise of any detector system.[6,18,25] In the conventional topology results have shown that the input MOSFET in the first front-end electronic system needs to dominate the noise of the entire system. Therefore the noise sources that contribute to the input MOSFET noise need to be modeled and defined and then optimized for each detector system. Figure 2.16 shows the noise model for the input MOSFET of the preamplifier. The input MOSFET contributes thermal and flicker noise to the system which can be optimized by the designer. The detector and the feedback resistor contribute parallel noise sources as well.

Since it is highly desirable to have only the input device of the preamplifier be the dominant noise source of the system, the feedback resistor must be very large, typically in the range of GΩs. Equation 2.21 describes the thermal noise which is characterized by a parallel current generator associated with the resistor [21].

$$\sqrt{\overline{i^2}} = \sqrt{\frac{4kT}{R}} \qquad (2.21)$$

It can be seen that a larger resistance value would yield a lower noise contribution than a smaller value. Unfortunately, a resistor on the order of GΩs would be very impractical to fabricate on silicon, therefore a CMOS feedback network must be implemented to emulate a large resistor. This discussion is continued below.

Detector and
Feedback Resistor
Parallel Noise

M1

$I^2_{therm} + i^2_M$
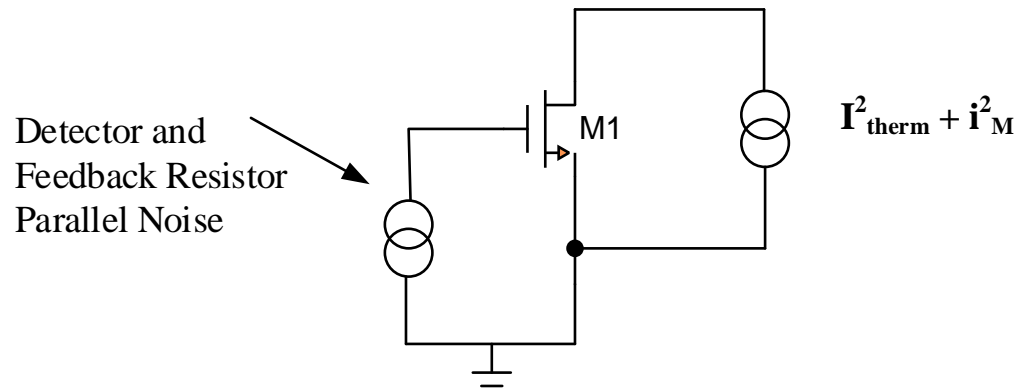
Figure 2.17: Amplifier input pair noise model.

2.4 Conclusion

Two topologies were mentioned above in this chapter. Each design has merit for applications. However for the scope of this work the topologies above require modification to attain the research goals. The overall operating principal of the designs presented above are used to develop the topology used in chapter 3 and 4.

Chapter 3

Design of Front-End Electronics

As discussed in the previous chapters charge sensitive amplifiers convert charge to voltage. Together with the sensor, charge amplifiers makes up the front-end components to a larger LOC system. Front-end components acquire the physical signal and output a usable signal for a signal processing system.

Front-end electronics define how well the remaining components of the readout system will operate. For example for the operational amplifier driven charge amplifier in figure 2.12, the operational amplifier input MOSFET must be designed and optimized to dominate the noise of the circuit. If this is not done the output can be unstable or give incorrect values. Modeling the test signal has to be done before designing a charge amplifier.

As the chapters above suggest the signal can vary greatly from application to application. Pyroelectric sensing films such as PVDF are used to monitor temperature of biological samples; one case [18] implements the film for a micro scale application. As the film itself does not need any power to operate, the current design can be considered power contentious. However, the circuit used to output the voltage is large and very power inefficient. This chapter will detail on the signal characterization, then move into the process of designing a low power circuit to read the change in temperature, down to the single degree level.

Once introduced to the design of the charge amplifier present in this work the following sections will highlight the preamplifier, feedback networks, and CMOS layout techniques used to realize the design. The final design shown in figure 3.7 was realized using a 180 nm CMOS process [25]. The simulations are presented in chapter 3, while the experimental test results are explained in chapter 4.

3.1 Signal Characterization of Pyroelectric Film

In [18] a discussion of the charge is presented. With a temperature change the transducer can provide a charge based on the physical size of the device. The charge produced by the PVDF transducer is proportional to the area. This is shown in the equation below.

$$dQ_P = p_Q A dT \qquad\qquad (3.1)$$

In the equation above the pyroelectric charge is represented by dQ_p, and p_Q is the charge pyroelectric coffecient and A is the area of the transducer. This is all with respect to change in temperature dT. [18]

From [18] the desired output signal from the transducer and charge amplifier is model below in figure 3.1. The signal is a slow moving charge build up over the frequency of mHz to Hz. This is considered a relatively slow signal in the world of electronics, where neutron detection and radio waves are the typical both operating well into the kHz to GHz range. [6]
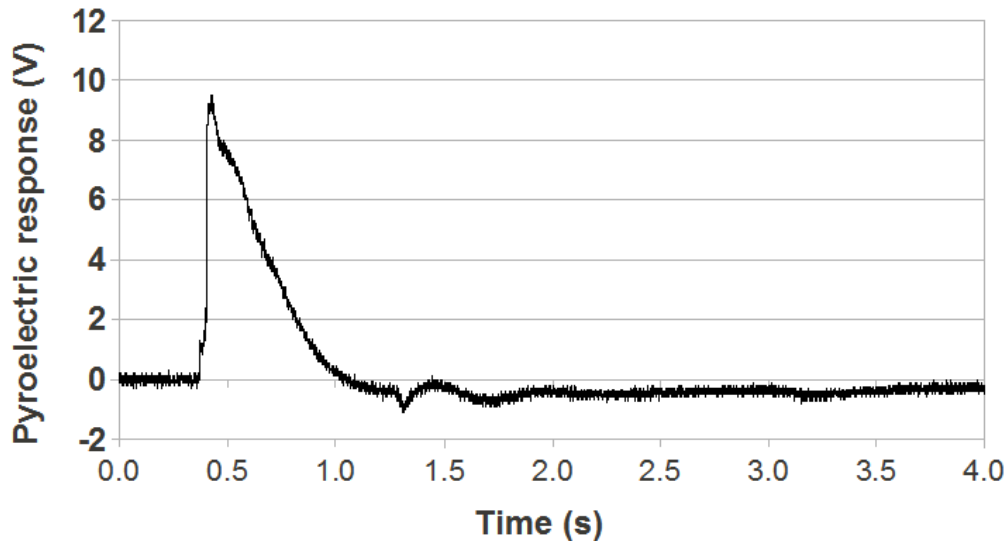
Figure 3.1: Results of design in [18] with 40°C temperature change.

From the test results in [18] the design can be reverse engineered. The values of importance are the rise time of the signal and the fall time of the decay, and the peak of the charge before decay. The rise time and fall time are important because if the circuit does not allow adequate time for the charge to build before it starts decaying, the output will run a ballistic deficit. The effect of ballistic deficit is incorrect or skewed output values.

From the work done in [18] the values of importance for the signal are summarized in the table below.

Table 2 : Comparison of Pyroelectric Sensor Properties

	Analytical	Experimental
Thermal Time Constant τ_{th}	3.2ms	3.2ms
Electrical Time Constant τ_e	102.4ms	200ms
Lower Cut-off Frequency f_L	1.6 Hz	0.8 Hz
Upper Cut-off Frequency f_H	49.7 Hz	49.7 Hz

From the table above and the circuit presented in [18] we can surmise that the peak signal is going to be about 100nA. The frequency of the signal will be from 2Hz to 50Hz. And the max charge over the time will be 1nA. This information will be used below to design the charge amplifier.

3.2 Preamplifier Design

Although the work done in [18] produced good results, the application can never move into field, or be consider LOC, as the circuit is large and require laboratory equipment to set up. In order to fulfil the design requirements the preamplifier will need to use alternate topologies to output the charge. From the work done in [18] it is concluded that the use of an operational amplifier drive charge amplifier is not the most well suited method for charge conversion in monitoring when PVDF transducers are used.

The limiting factor in the circuit presented in [18] is the feedback loop components. R_f amd C_f are 100MΩ and 1nF for the work in [18], these values are not realistic to implement on an integrated circuit chip as they will be monolithic in comparison to the rest of the circuitry. When the limit chip area is consumed by the large components other important devices downstream from the front end circuitry have to be eliminated. Therefore it is imperative that we minimized the footprint of the preamplifier.

Since a large capacitor such as the one implanted on the original design would not fit on an integrated circuit a few options to eliminate the constraints are examined. The goal of the amplifier is to convert a charge to a voltage. Following the approach from chapter 2, the most important feature for the signal is the feedback elements and the virtual ground on the inverting node of the operational amplifier. In order to replicate these analysis of a virtual ground and how to achieve one are examined.

3.3 Virtual Ground

An active virtual ground circuit is sometimes called a rail splitter. A circuit as shown in figure 2.12 uses an op-amp to achieve this concept. Since an op-amp has very high open-

loop gain, the potential difference between its inputs tend to be very close to zero when a feedback network is implemented. To achieve a reasonable voltage at the output, the output supplies the inverting input or the minus side via the feedback network, R and C, with sufficient voltage to reduce the potential difference between the inputs to microvolts. The non-inverting or the plus input of the operational amplifier is grounded; therefore, its inverting input, although not connected to ground, will assume a similar potential, becoming a virtual ground if the operational amplifier is working in its linear region. This effect allows for the voltage to peak and fall using the RC time constant of the feedback loop elements R_f and C_f. Therefore to design an amplifier that operate the same way a feedback loop has to be present to pull the voltage back to the quiescent point.

3.4 System breakdown
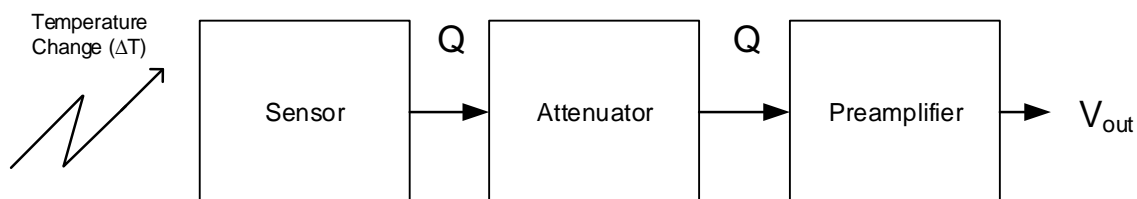
Figure 3.2: Block view of implemented amplifier design.

Figure 3.2 shows the general view of the design of the amplifier. In order to get the charge created in the transducer into a voltage, an amplifier with a large feedback capacitor, would have to be used, due to the slow signal which creats a large amount of charge. Though the traditional design could have been implemented by using an off-chip capacitance, as in [20]. Due to necessity for this system to be on a single chip, the size of the capacitor needed to be reduced to a value suitable for CMOS implementation.

Steps to reduce the feedback capacitor could have been taken such as using an attenuator to reduce the signal to a value that could be implemented on-chip. However, this does not offer much assistance due to the feedback resistance. As mentioned above in section 3.3. The RC time constant is very important because that is what drives the speed at which the voltage will decay. For the work done in [18] the decay time was 3.2ms, which makes sense with the large feedback components. Therefore if the feedback capacitance is reduced the feedback resistance must increase by the same amount.

By decreasing the capacitance the voltage signal is also being scaled back. The amount of voltage signal is limited by the feedback capacitance as explained in chapter 2. Because

of the limited signal and increasing size of the resistance scaling is not a good option. In order to maintain the response and fit it on a chip consideration of the original work had to be taken in to account. The limits imposed by the discrete design were not steadfast, they were just one approach to the design. With the limits of making an integrated circuit system the only signal that needed to be maintained is the output peak signal. In order to obtain the peak signal the system needed to have high impedance, gather the charge signal and hold it. The resulting target design is summarized by figure 3.1.

The breakdown of the circuit is the signal, sensor, gain component and feedback. Each of these are important and must be examined together to develop a circuit cable of converting the charge input to a voltage level above that of noise.

The first two components are static. By using the work in [18] the signal is set and the sensor for the signal is set. Therefore the only components open to changing are the amplifier or attenuation and preamplifier. Of the two the preamplifier must be defined before any signal modifications can be explored.

3.5 Feedback Loop

Chapter two explains in detail the equations used to size the feedback components. The feedback network for a charge sensitive preamplifier consists of a charge collecting capacitor and a resistive feedback network that allows charge in the feedback capacitor to dissipate.

In the typical charge amplifier shown in figure 2.12 one method for the charge bleed off would be to apply a resistor in parallel to the feedback capacitor. This is shown in Figure 3.3. However, for the designs that use operational amplifiers the resistor adds a noise source to the input MOSFET described in equation 2.21. This noise source can be detrimental to the signal. In order to reduce the noise contribution, the resistance value would have to be large. Also as mentioned before the decay time of the signal depends greatly on a large resistance. Discrete resistors are not practical in terms of chip area, therefore an active feedback network will allow for less area and can behave as a very large passive resistive element. This section explores different active feedback topologies and describes the design that was chosen.

In operational amplifier driven charge mode amplifiers the feedback elements will operate to balance the charge injected into the negative input by charging feedback capacitor C_f. After the charging is complete the resistor R_f bleeds the charge off capacitor C_f at a low rate to prevent the amplifier from drifting into saturation. Figure 3.3 illustrates one possible topology for the feedback network which is based on previous work [6].
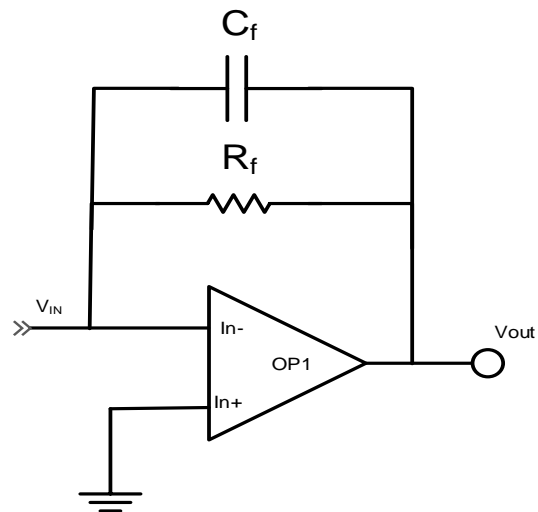
Figure 3.3: Basic feedback with capacitive and resistive element.
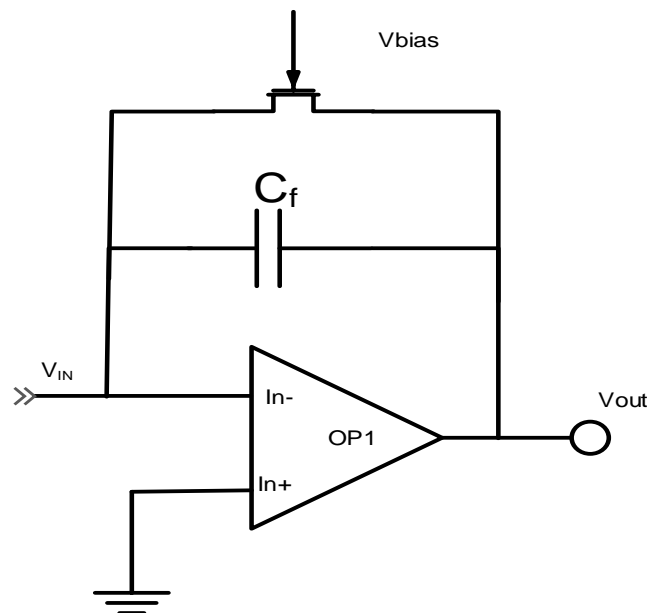
Figure 3.4: Single MOSFET feedback network.

A alternate topology is shown in figure 3.4 where the resistor is replaced by a MOSFET. The single MOSFET feedback network provides minimum thermal noise and high linearity, requires baseline stabilization, and can also be realized in multiple stages [6].

A MOSFET can easily be used as a variable resistor. Considerations tha need to be taken into account are the minimum resistance needed and the R_{dson} of the MOSFET being used. The second thing to consider is what area of operations the MOSFET is operating in. Which for adequate values of resistance will be the linear region. The resistance values can be taken from the characteristic curves of the MOSFET being used.
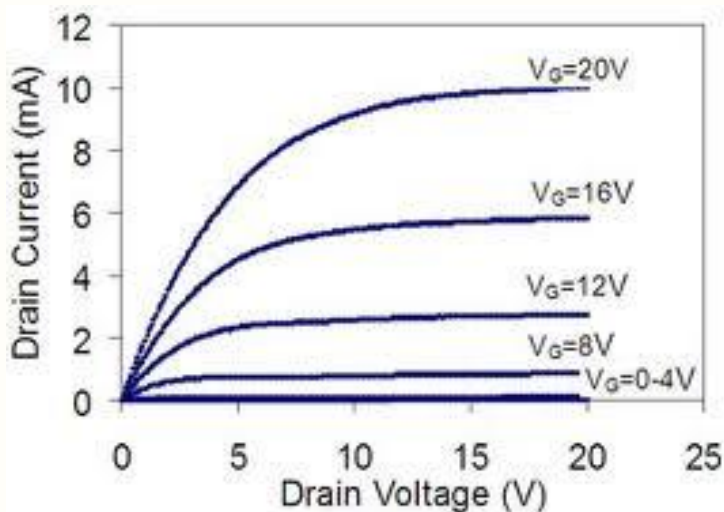
Figure 3.5: Characteristic curve for a MOSFET.

When the V_{GS} is below V_{th} of the MOSFETit is in a cut-off mode, which means the entire supply voltage comes appears across MOSFET. This means the MOSFET is operating as an open-load with infinite resistance. Is the gate voltage is increased the MOSFET will being to conduct current and enter the linear regions. In this region a voltage forms from the drain to source V_{ds}. In the linear regions the MOSFET acts as a resistance of finite value. If the gate voltage is increased too much the MOSFET enters the saturation region. In this region the resistance of the MOSFET is at its lowest and is equal to the R_{dson} of the MOSFET. Therefore to use a MOSFET as a resistor the gate voltage must be controlled very closely.

A second possible feedback network topology is shown in Figure 3.6. The system implemented is the basis of the work presented in [6]. The circuit shown is the complete setup of a charge sensitive amplifier for neutron detection.

Figure 3.6: Feedback network as presented in [6].

The basic operation of the feedback network in Figure 3.6 is when a charge pulse is introduced to C_f then there is a change in voltage on the gate of M2 which in turn will introduce a change in current between the drains of M1 and M4. The gate of M2 will stabilize back to the V_{ref} voltage on the gate of M1 because of the differential pair action of M1 and M2. This is effectively a resistor much as the MOSFET in figure 3.4 is a resistor, since a change in voltage gives a proportional change in current. The drawback of design is the nonlinearity of the pseudo resistor. Aside from the nonlinearity the design proposed in [6] is an effect means of reducing the footprint of a resistor in the MΩ or GΩ size. Another drawback presented in [6] is the use of an off chip capacitance.

Now that a resistor can be formed using MOSFETs, which are significantly smaller than any discrete resistors,, the design of the system can begin. By implementing the function of the system above a charge amplifier can be designed which operates similar to the transimpedance amplifier and its virtual ground. In order to model the system above the different components had to be simplified. Below is a simplified version of the final system. Here the current, I_{in}, is meant to simulate the charge coming from the transducer.
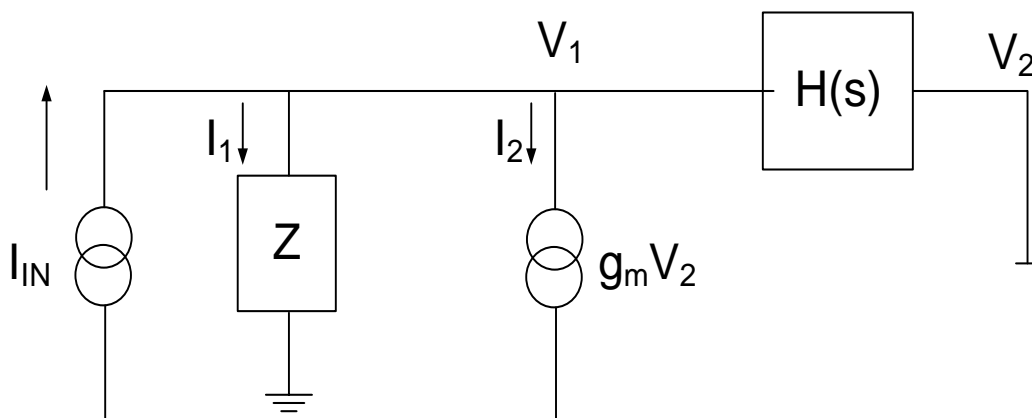
Figure 3.7: Functional view of implemented amplifier design

The design highlighted above shows why each component is necessary and what is expected to be achieved by this design that mimic the classic charge amplifier in figure 2.16. The equation below offer some insight as they represent how the above circuit will work.

In order to analyze the system the transfer function has to be analyzed. First the current or charge into the system will exit the system through a ground. Using Kirchhoff laws the system is solved in the following manner.

$$I_{in} = I_1 + I_2 \qquad\qquad (3.2)$$

The current will be divided by the two paths. The voltage V_2 is a multiplied voltage of the voltage at the node V_1.

$$V_2 = H(s) * V_1 \qquad\qquad (3.3)$$

This allows for solving the current through the I_2 branch as such,

$$I_2 = g_m * V_2 \qquad\qquad (3.4)$$

Leaving the V_1 voltage to be,

$$V_1 = I_1 * Z \qquad\qquad (3.5)$$

Now that the relationship between the different components is established the relationship of the input signal with the output voltage can be explored. In equations 3.5 through 3.10 this is done in a step wise manner. First the signal, I_{in} is isolated,

$$I_{in} = \frac{V_1}{Z} + g_m * V_2 = \frac{V_1}{Z} + g_m * (H(s) * V_1) \qquad\qquad (3.6)$$

Since the desire is to see how the output voltage will respond to the components the output signal is isolated as well.

$$\frac{I_{in}}{V_1} = \frac{1}{Z} + g_m * H(s) \qquad\qquad (3.7)$$

Rearranging the factors allows the form signal out over signal in with relation to the circuit,

$$\frac{V_1}{I_{in}} = \frac{1}{\frac{1}{Z} + g_m * H(s)} = \frac{Z}{1 + g_m * Z * H(s)} \qquad\qquad (3.8)$$

The using the relation,

$$Z = \frac{1}{S*C} \qquad\qquad (3.9)$$

The final result looks as below,

$$\frac{V_1}{I_{in}} = \frac{\frac{1}{S*C}}{1 + \frac{g_m}{S*C} * H(s)} * \frac{S*C}{g_m} \qquad\qquad (3.10)$$

$$\frac{V_1}{I_{in}} = \frac{\frac{1}{g_m}}{\frac{S*C}{g_m} + H(s)} \qquad\qquad (3.11)$$

From the equation above jt is obvious that the capacitance is only a small part of the circuit while. the resistance factor, H(s), is where the focus of the design will begin. H(s) can be expressed in terms of the effective resistance as shown below in equation 3.11.

$$R = R_{eff} = \frac{1}{g_m H(s)} \qquad (3.12)$$

The knowledge taken away from the above is that the transconductance of a device will greatly affect the effective resistance of a circuit such as the one in figure 3.2. In the next section this design is realized with circuit elements.

3.6 Pseudo- Resistor

Since the size of the feedback resistance needs to be large the result of the equation above allows for the resistance to be set by the transconductance. From the work done in [18] the resistance can be calculated from the decay time. τ is 3.2ms for the design in [18]. Using this value in equation 3.12 the resistance to maintain the decay time if a 10pF capacitor is used as the feedback capacitor comes to be 320MΩ.

$$\tau = RC \qquad (3.13)$$

The design implemented in this work to achieve the resistance above is similar to that of figure 3.6. A feedback loop is implemented to mimic a high resistance. The feedback loop is considered to be a pseudo-resistor. The implemented pseudo-resistor is shown in figure 3.8.

This pseudo resistor is made up of a source follower (M2) and a resistor to bias the follower as well as a path for current to travel (M1). The source follower is there to control the gate of the current path. It will behave by taking in the input voltage which may have a relatively large Thevenin resistance and replicates the voltage at the output port, which has a low output resistance. This output resistance in series with the resistor result in a voltage divider at the gate of M1. The source follower works under conservation. If the voltage increases at the output , then the current changes. The current follows the voltage, therefore the voltage at the source of M2 must increase following the input. This will then drive the gate of M1 creating a path to ground for the current.

From the work done in [6] a similar approach was taken for biological signals. The main difference between the signals is speed. Neutrons tend to be incidence on sensing material at a rate of 10^9 particle per/sec while in the biological signal community the typical frequency can be from 1 Hz to 1500 Hz. This drastic change however does not mean that the processing circuits need to be dramatically different. The principles still apply allowing for the circuit presented in this thesis to use the same concepts as the work done in [6].
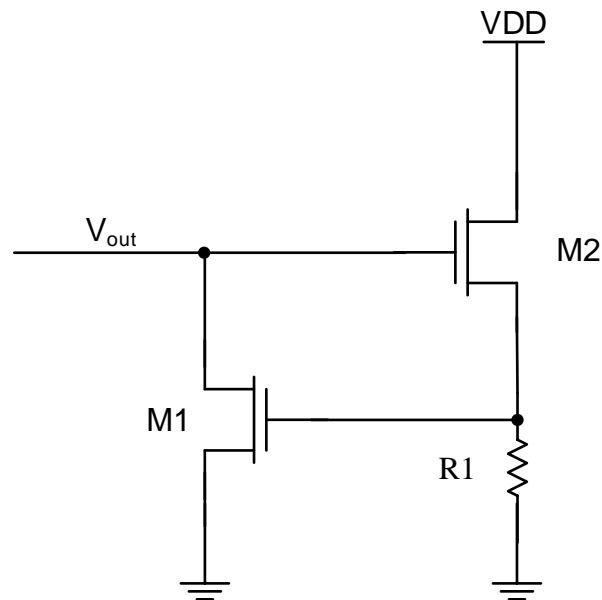
Figure 3.8: Pseudo-resistor implemented on charge amplifier.

Once the design highlighted above is simulated and the response is characterized as a possible approach for the intended signal, optimizing the system began. The goal of the design is provide a voltage with respect to a charge that changes with temperature. A 25 degree Celsius has a peak charge of 100nC and a minimal detectable charge of 2nC.

As chapter 2 shows the voltage conversion is mainly attributed to the capacitor in the feedback loop. Therefore in order to create a voltage on the output node a capacitor was selected. As shown above a 10pF capacitor requires a 320MΩ resistance. In order to keep the final footprint to a minimum 20pF was selected to be the preamplifier capacitance. By selecting the capacitor it was possible to set the value of the effective resistance, R_{eff}, of the pseudo resistor. Using the same equation from above the effective resistance needed to become 160MΩ.

From the analysis in the section above a transistor can be used to mimic this value of resistance. However, a single transistor cannot mimic the value needed. Therefore the feedback loop shown above is implemented. Due to the nonlinearity of the pseudo resistor decisions have to be made in order to size M1 and M2 to operate in the regions designed.

After many attempts to bias the network to attain this resistance, a limit of what current can be supplied to the circuit was found. In order to attain the required effective resistance the bias current source needed to be a stable picoampere source. Such a small source was not feasible for this application. With a more reasonable biasing current the effective resistance attainable is 100MΩ. This resistance would keep the decay time of the

signal much greater than the collection time allowing for the signal to peak before it decays. This avoids the ballistic deficit typically present in applications involving large signals and small capacitors.

Now that a resistance has been set a careful consideration of the size of M1 and M2 can begin. Since these devices will be operating in weak inversion the W/L is related as such in subthreshold

$$I_D = I_{D0}\frac{W}{L}e^{q(V_{GS}-V_{THN})/n*kT} \qquad (3.14)$$

This combined with the desire for a large transconductance which is

$$g_m = KP_N\frac{W}{L}(v_{gs} + V_{GS} - V_{THN}) \qquad (3.15)$$

It can be elicited that large narrow devices are going to work best for the purpose of achieving a large resistance.

3.7 Current Attenuator

After the other two portions of the design in figure 3.2 were analyzed the signal itself needed to be manipulated. In order to use the selected capacitance and therefore the circuit used to create the resistance the charge signal needed to be attenuated as not to saturate the capacitor resulting in no signal. The large amount of charge in the signal allows for a decreased signal to accommodate the smaller capacitance. In order to reduce the charge an attenuator or step down current mirror was designed. There were two designs deliberated with the chosen design being better suited for low power consumption. The first is a traditional current mirror. A basic current mirror can be composed of as few as two MOSFETs. The figure below is the most basic design for an NMOS current mirror. This approach was used on the final design as a way of including two separate current sources on the same node.
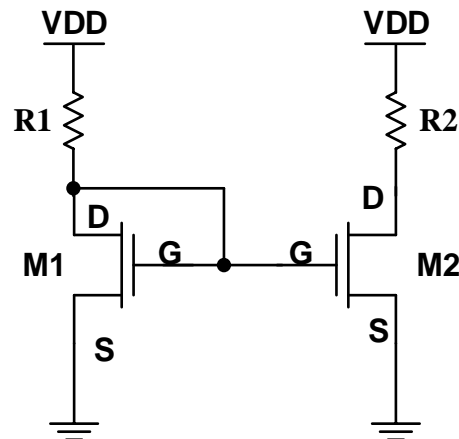
Figure 3.9 : Circuit schematic of a basic current mirror.

The basic current mirror is formed as shown above. Assuming the length and width of the MOSFETs are the same, this would also assume that $V_{GS1} = V_{DS1} = V_{GS2}$. Since the MOSFETs have the same gate-to-source voltages, it can also be assumed that they have the same drain current. If $R_1 = R_2$ in the figure above then the drain of both FETs will be at the same potential. Therefore by matching the size, V_{GS1} , and I_D of the two transistors it can be assured that the two MOSFETs have the same drain-to-source voltage, meaning that $V_{GS1} = V_{DS1} = V_{GS2} = V_{DS2.}$
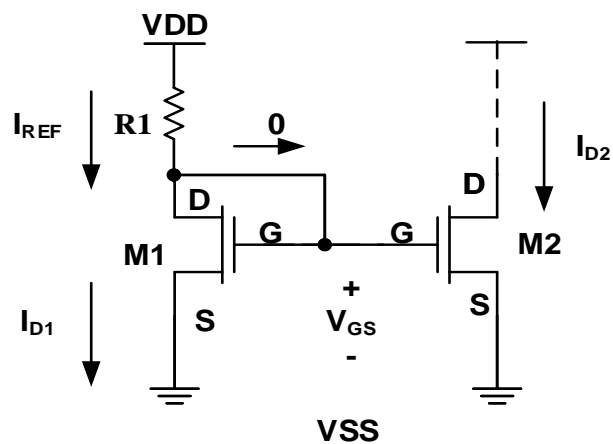

Figure 3.10 : A basic current mirror with currents.

By connecting the gate to the drain in M1 the MOSFET is forced to operate in the saturation region. The equation to describe the current moving through M1 is:

$$I_{D1} = \frac{1}{2} k'_n \frac{W_1}{L_1} (V_{GS} - V_{t1})^2 \qquad (3.16)$$

With a zero gate current,

$$I_{REF} = I_{D1} \qquad (3.17)$$

Where the reference current can be seen to be

$$I_{REF} = \frac{V_{DD} - V_{GS} - (-V_{SS})}{R} \qquad (3.18)$$

Again as mentioned earlier the two MOSFETs have the same V_{GS} therefore the current was the same. The equation would look as follows.

$$I_{D2} = \frac{1}{2} k'_{n2} \frac{W_2}{L_2} (V_{GS} - V_{t2})^2 \qquad (3.19)$$

Additionally, if they were perfectly matched then the k values and V_t values would be equal. When setting the current in secondary stages assume the k values are equal, given the following.

$$I_{D2} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} I_{D1} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} I_{REF} \qquad (3.20)$$

A mirror operating in this manner is considered a current sink. The PMOS version is similar in design but would source the current. A PMOS mirror is shown in Figure 3.3. [21]
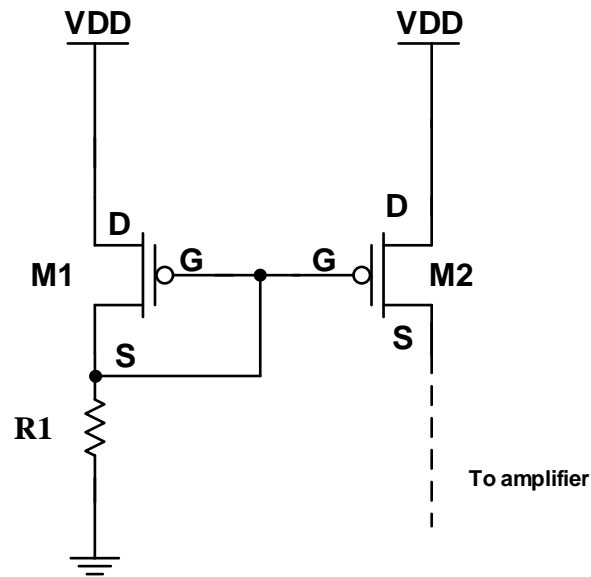
Figure 3.11 : A basic PMOS current mirror.

After understanding the basic current mirror a lower power approach was taken. The current mirror in figure 3.4 is a small improvement on the simple current mirror in figure 3.3. Cascode current mirrors provide an improvement of output resistance over simple current mirrors. The small-signal output resistance (R_o) of the cascade current source in Figure 3.4 is given by

$$R_o = r_{o2}(1 + g_{m2}r_{o4}) + r_{o4} \qquad (3.21)$$

This then simplifies to

$$R_o \approx g_{m2}r_o^2 \qquad (3.22)$$

where $r_o = r_{o2} = r_{o4}$ are the MOSFET small-signal output resistance and g_m is the MOSFET small-signal transconductance. If M_1 and M_2 were removed from Figure 3.4, a simple current mirror would be left whose small-signal output resistance would be equal to r_{o4}.

Although this cascode current mirror provides high output impedance, it does not allow for a high output voltage swing. The dynamic range of this cascode current mirror with respect to V_{DD} is limited to less than

$$V_{OUT} = V_{DD} - 2_{SD,Sat} - |V_{THP}| \approx V_{DD} - 1.3V \qquad (3.23)$$

where $V_{SD,Sat}$ is the saturation voltage of a pMOS transistor and V_{THP} is the pMOS threshold voltage.
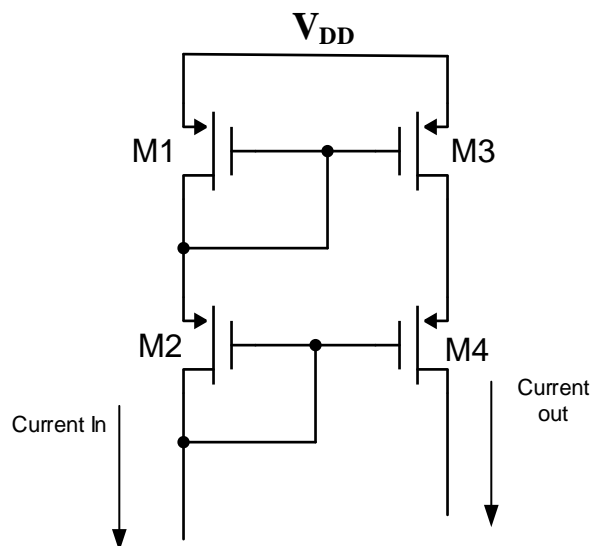

Figure 3.12: Cascode current mirror.

Alternate schemes of biasing cascode current mirrors for wide-swing or low-voltage applications exist [21]. One of the suggestions is shown below in figure 3.13.

A typical wide-swing, low-voltage cascode current mirror is presented in Figure 3.13. For this wide-swing current mirror to work efficiently, V_{Bias} must be set at $V_{DD} - 2V_{SD,Sat} - |V_{THP}|$, leaving a $V_{SD,Sat}$ across mirror devices M_3 and M_4. This is called a wide-swing current source because the minimum voltage across the current source for proper operation is $2V_{SD,Sat}$ [21], which is one threshold voltage drop less than the regular cascode mirror shown in Figure 3.12. This current mirror is dependent on the voltage of V_{Bias} remaining constant and only works well for a small variation of input current. For a large change of the input current, additional circuitry is required to track the V_{SG} of the cascode devices M_1 and M_2, so that the output characteristics of the current mirror do not vary.
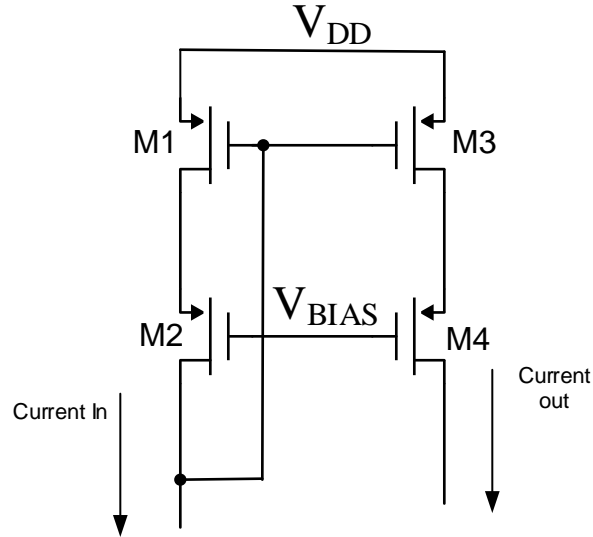
Figure 3.13: A wide swing current mirror.

The current mirror used in this operational amplifier is a wide-swing cascode circuit. Figure 3.6 shows implemented current mirror. The major advantages of using this current mirror is the elimination of the possibility of mismatch between the two branch currents and thus reducing the power consumption. Power is scarce in CMOS design inherently, but especially with the LOC design. The reduced power consumption is achieved by maintaining the desired difference between the gate voltages of M_3 and M_4 of one overdrive voltage, V_{OV}. In order to achieve this, it is required to bias M_1 at the active region and subsequently requiring gate voltages of M_3 and M_4 to be $V_t + V_{OV}$ and $V_t + 2V_{OV}$, respectively. As shown in Figure 3.1, since M_6 is diode connected, it operates in the saturation region. Since the gate-source voltage of M_6 is equal to the gate-drain voltage of M_5, a channel exists at the drain of M_5 when it exists at the source of M_6. In other words, M_6 forces M_5 to operate in the triode region.

To obtain the drain-source voltage of M_5 to be V_{ov}, we need to design the aspect ratio of the transistors appropriately. Since M_6 operates in the active region, the equation for the bias current is shown in 3.1.

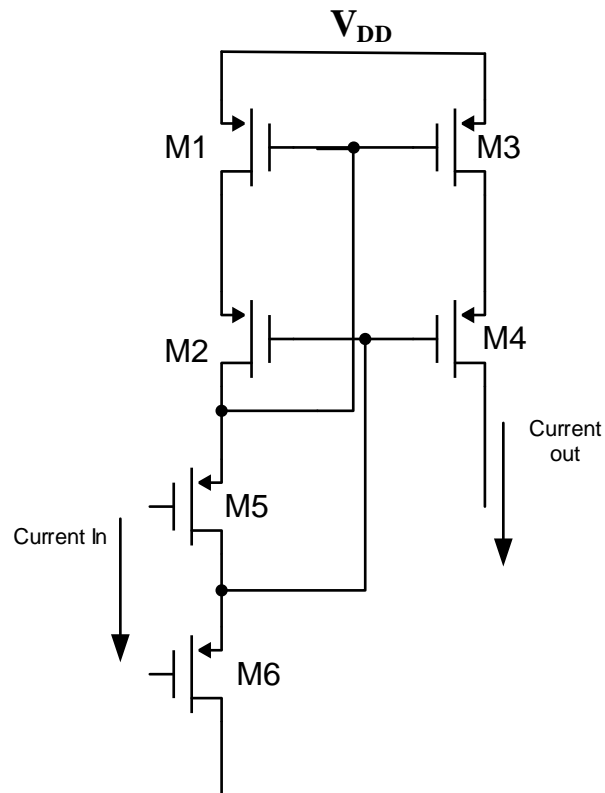$$I_{BIAS} = \frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_t)^2 \qquad (3.24)$$

Figure 3.14: Implemented current mirror.

Since M_5 operates in the triode region the bias current equation is shown in 3.2,

$$I_{BIAS} = \frac{k'}{2}\left(\frac{W}{L}\right)_5\left((V_{GS6} - V_t)V_{DS5} - (V_{DS5})^2\right)$$ *(3.25)*

The goal is to set

$$V_{DS5} = V_{ov}$$ *(3.26)*

When

$$V_{GS6} = V_t + V_{ov} \qquad\qquad (3.27)$$

From eqn. (3.3) and (3.4),

$$V_{GS5} = V_{GS6} + V_{DS5} = V_t + 2V_{ov} \qquad\qquad (3.28)$$

Substituting eqn. (3.2) – (3.5) into eqn. (3.1) gives,

$$\frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{ov})^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (2(2V_{ov})V_{ov} - (V_{ov})^2) \qquad (3.29)$$

which is further simplified to ,

$$\left(\frac{W}{L}\right)_5 = \frac{1}{3}\left(\frac{W}{L}\right)_6 \qquad\qquad (3.30)$$

After implementing a low power current mirror the charge is then transferred at a reduced value to the feedback loop. Using the method above the current divider uses a 10:1 ratio for the charge division. [27]

The current mirror replaces the need for an operational amplifier at the core of the circuit. However the important novelty to this approach is the use of feedback to drive a resistance to bleed the current off the capacitor.

3.8 Implemented Design

Manipulating the signal is to work with the total design is the only step left. The size of each component is shown below in table 3. In setting the signal the biasing of the devices becomes important. There are two currents moving through the attenuator designed above. The first is a DC bias current, I_{bias}. The second is the signal being attenuated. In order for the circuit to operate the bias current needs to set the point of

operation of the circuit. This means that a set basing current has to be selected. From the previous sections the limit of the biasing current is hundreds of picoampre. Though calculations based on the design it was determined that a good trade off would be to use 1uA biasing current. The result was being able to see the effect of the bias current in setting the effective resistance. By having a 1 μA bias current the effective resistance on the selected W/L ratio was 166MΩ. The effect of reducing the bias current affect the effective resistance as shown above in equation 3.12. The effect of the signal also has some effect on the resistance. Further increase in the signal amplitude results in lower the resistance.

After deciding the W/L ratio of M1 the size of M2 also needed to be decided. The gate of this device needed to be wide so that a large amount of voltage on the gate would turn the transistor on only after the initial biasing current is set. The signal spike will cause this to turn on. When this transistor turns on the gate of M1 is moved up, which means that it turns on as well. This effect gives the current the path to ground. After all the sized of the components were decided the final design was implemented.

3.9 Layout Techniques in CMOS Design

The previous sections describe the components of the final design. The final circuit schematic is shown below in figure 3.15. In the schematic each of the sections in chapter 3 can be found. The realized circuit contains an attenuator, and preamplifier consisting of a capacitor and resistor. The table below has the values for the different components. Each component was selected to provide either current or voltage that would allow the circuit in figure 3.15 to operate similar to the circuit in 2.12.

*Table 3: Component Values of Circuit Parameters*

Transistor	W/L (μm/ μm)	Transistor	W/L (μm/ μm)
M1	**1/1**	M5	**2/1**
M2	**1/1**	M6	**2/1**
M3	**20/1**	M7	**8/2**
M4	**20/1**	M8	**3/0.7**
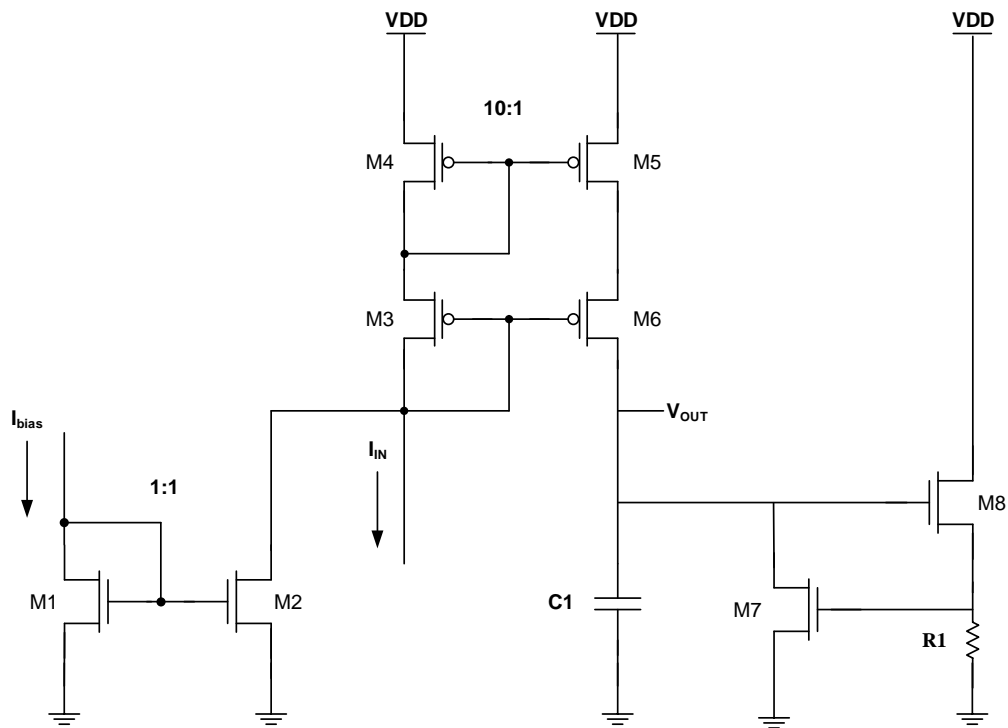
Figure 3.15: Circuit Schematic of the Final Design.

After settling on a final design. The circuit had to be evaluated as a whole in order to determine if it would be acceptable to use for biological signal processing. To test this the circuit was simulated using a very slow 100nC charge at the terminal labeled I_{IN}. The voltage was selected using the process standard of 1.8V and the bias current as explained in detail earlier was 1μA. The results are shown below in figure 3.16.
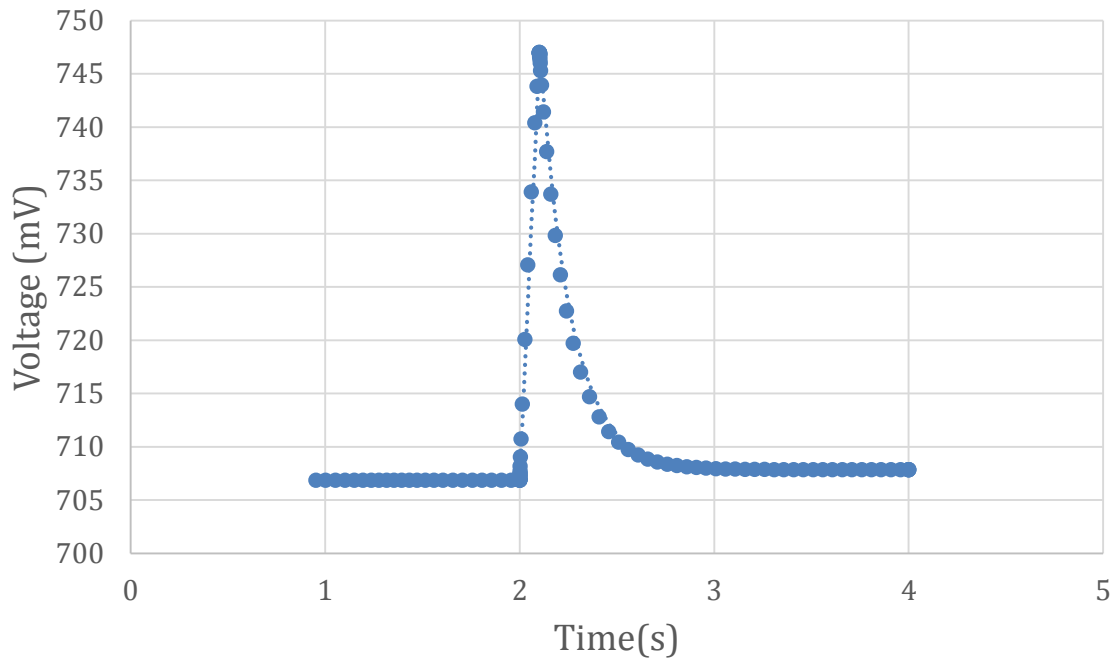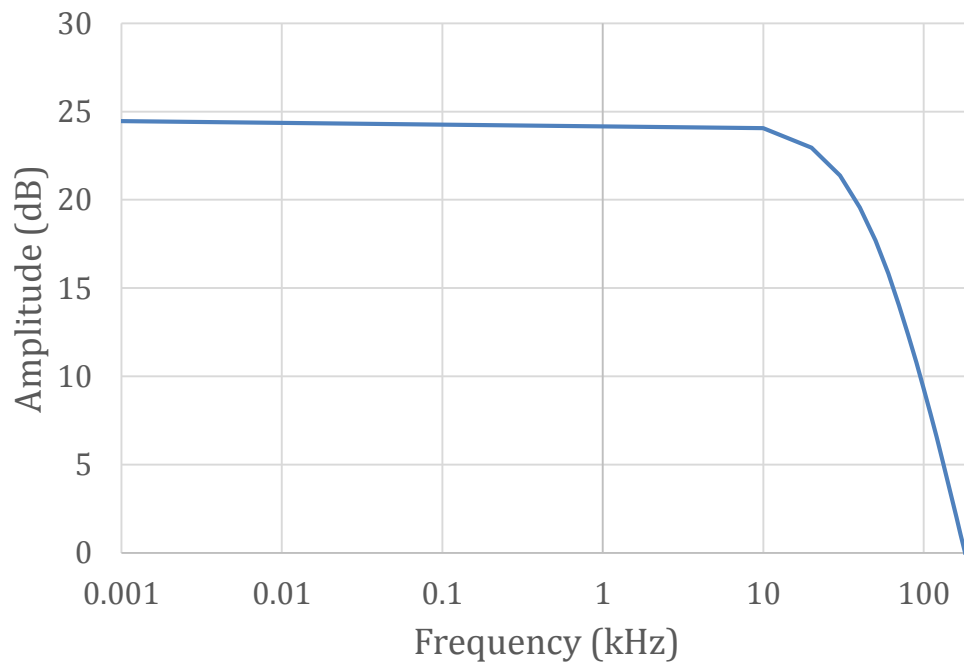
Figure 3.16: Simulation of proposed circuit, response is 50mV peak for 50nC signal.

After completing simulations of the design, and determining the overall shape of the curve match that of what is needed for temperature monitoring, the level of the output voltage was determined to be above that of the noise of the circuit. To affirm this assumption the input referred noise analysis was simulated. Below in figure 3.17 the input referred noise graph is shown. This curve marks the minimal signal needed to produce a response on with this design.

After testing that the circuit would work the final test was to confirm that the circuit would work for biological signals from 1mHz to 1kHz. The graph below in figure 3.18 is the result of simulation testing the bandwidth of operation. The graph below shows that the design should work from the mHz range well into the kHz range.
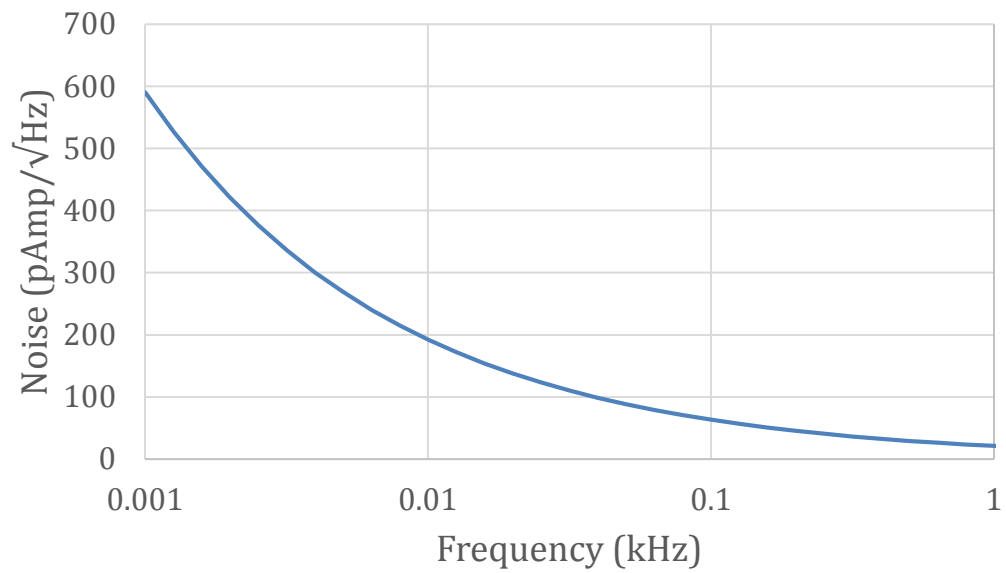
Figure 3.17: Simulation of input referred noise and the signal floor for the design in figure 3.15

Figure 3.18: Simulation of proposed circuit, response is the bandwidth of circuit.

Chapter 4

Results and Discussion

The previous chapter provided insight for the development of this work. In chapter 3 the simulated results were presented for the charge output expected from the PVDF film. Chapter 4 will present the operation of the charge amplifier in a laboratory setting. The focus of this work is the charge amplifier therefore all tests were simulated using a voltage to current test board. Section 4.1 gives a brief characterization of the voltage to current test circuit. Section 4.2 is the experimental test results of the charge amplifier.

All measurements were taken with an active FET oscilloscope probe with 2 pF input capacitance, 1GHz bandwidth, 10 attenuation, and 1MΩ input impedance. The circuit was tested for operation within the dynamic range of the pyroelectric film transducer presented in [18].

The two works analyzed and compare are the original work [18] and the design fabricated in figure 3.7. This chapter wraps up with an overview of the circuits performance and how the goals of the design were reached.

4.1 Test Board Characterization

Table 4: Values for Test Board and Charge Amplifier Circuit

Generator Signal or Supply	Value	Units
Board level V_{dd}	5	Volts
Board level V_{ss}	0	Volts
GND	0	Volts
Chip level V_{dd}	1.8	Volts
Chip level V_{ss}	0	Volts
I_{bias}	1	μA

A test board was built for the purpose of analyzing two of the designs. The circuit used on the test board is a TI AD811ANZ operational amplifier and a 2N7000 N- channel MOSFET. The topology and board are shown below. The values used during the test are summarized in table 4 and 5.

Table 5: Component Values for Test Board Parameters

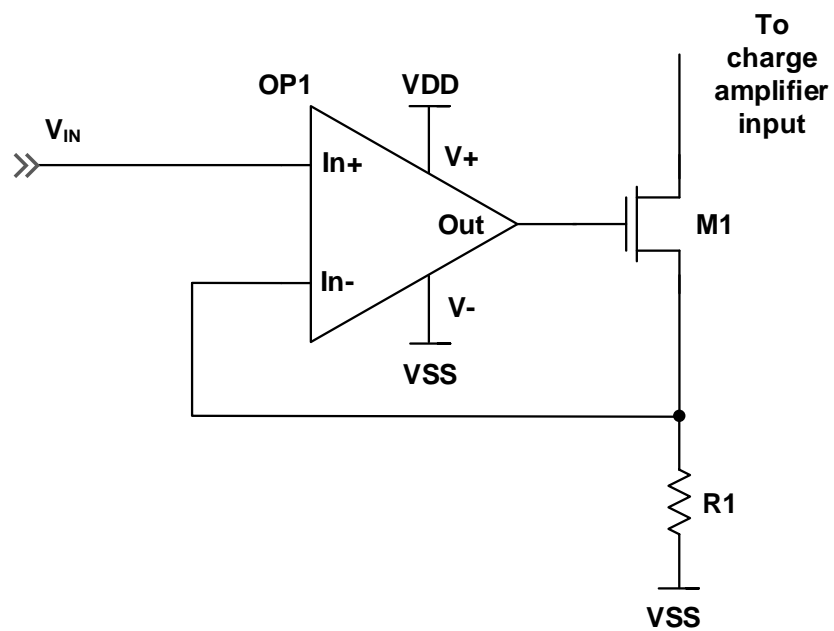| Device	Value
R1	100MΩ
M1	2N7000
VDD	5V
VSS	0
OP1	AD811ANZ
Vin	Function Generator

Figure 4.1: Discrete test circuit for converting voltage signals to current.

From the circuit it can be found that:

$$V_{in-} = V_{SS} + I_{out} + R_1 \qquad\qquad (4.1)$$

But if the operational amplifier is in the high-gain region, we can ideally have:

$$V_{in-} = V_{in+} = V_{in} \qquad\qquad (4.2)$$

Therefore comparing the right term of both equations one can obtain:

$$V_{in} = V_{SS} + I_{out} + R_1 \qquad\qquad (4.3)$$

$$I_{out} = \frac{V_{in}}{R_1} \qquad\qquad (4.4)$$

The transistor is meant to drive the output current depending on the gate voltage. The operational amplifier will try to make its input equals, and this will in turn supply a voltage so that R1*I_{out} is equal to V_{in}. The relationship between I_{out} and the output of the operational amplifier will be set by the transistor. Therefore the transistor will perform the *real* V-I conversion, creating a feedback loop with the op-amp. Using this circuit allows for the conversion of a voltage signal to current. Using this current one can emulate the charge that would be produced by a transducer. A photograph of the test circuit with no connections to any power or signal sources is shown below.

This board was tested under various input signals to verify that it was producing the expected current and therefore charge. The figure below is the result of modulating the pulse width and taking the current waveform.
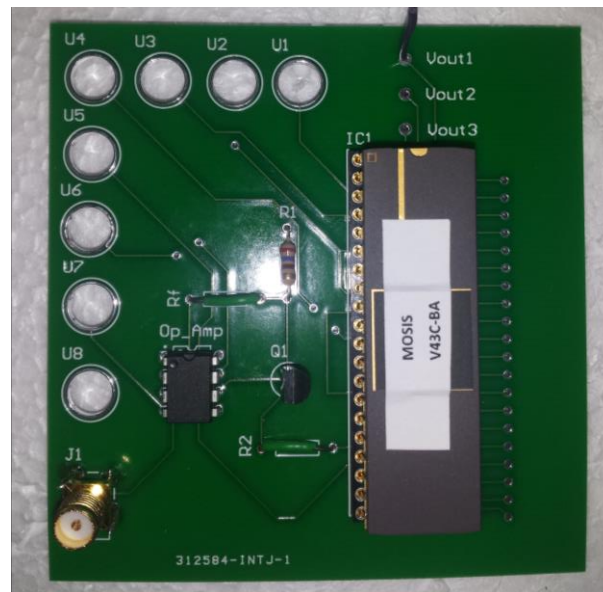
Figure 4.2: Photograph of the test board.

Table 6: Current Output from the Test Board Varying the Pulse Width.

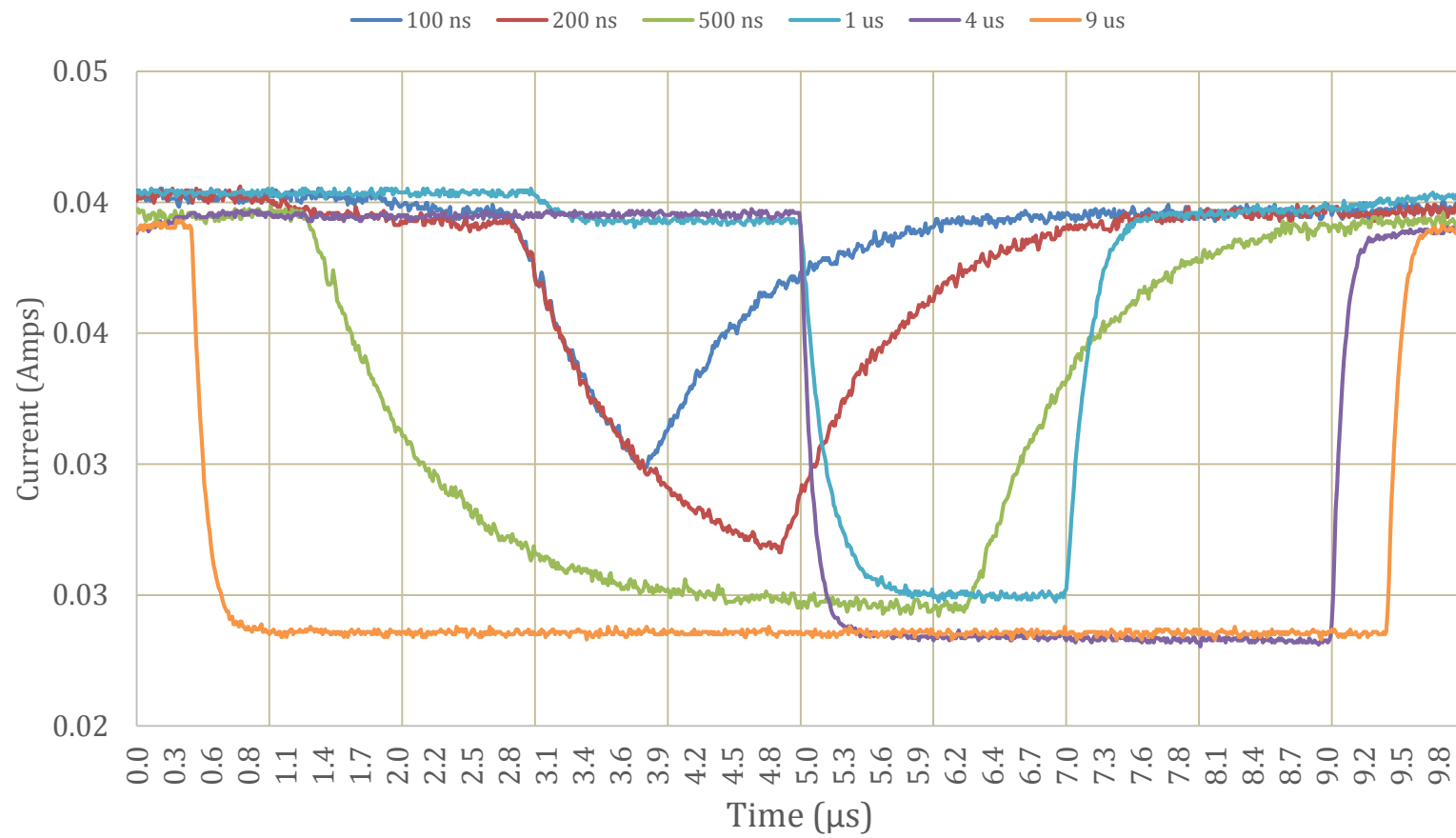| Frequency (kHz)	Peak Voltage (mV)	Voltage Pulse width (ns)	Current Pulse Width (ns)	Peak Current (mA)	Charge (C)
100	100	100	275	10	2.75E-09
100	100	200	301	14.1	4.24E-09
100	100	500	700	16.6	1.16E-08
100	100	1000	1200	16.8	1.99E-08
100	100	4000	4200	16.6	6.97E-08
100	100	9000	9190	16.6	1.53E-07

Figure 4.3: Current output from test board.

4.2 Commercial Charge Amplifier Results

The breadboard design is the original design that this project was attempting to mimic using ASIC design. As with most first attempt devices this is the basis for the measurement of power consumption and speed in subsequent testing. However, functionality and conversion of the intended signal are also important. The fabricated working device is pictured below in Figure 4.2. The board is comprised of two layers with discrete devices that can be identified in the Appendix of this paper.
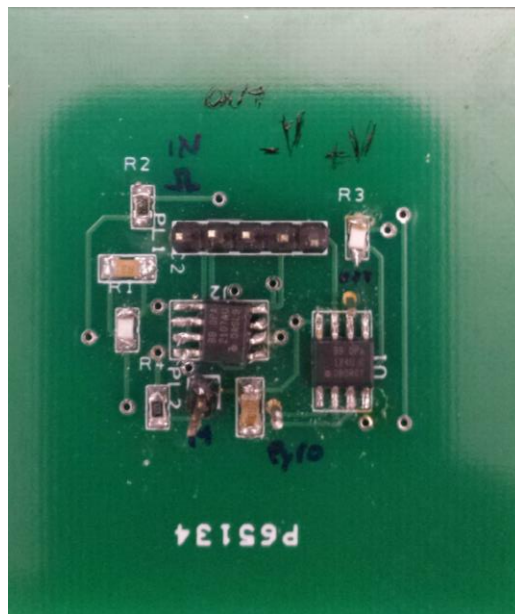
Figure 4.4: Work as presented in [25].

The design of the board is based on the material presented in chapter 3. This design is based loosely on the presented material from chapter 3. An equivalent circuit of the picture above is given below.
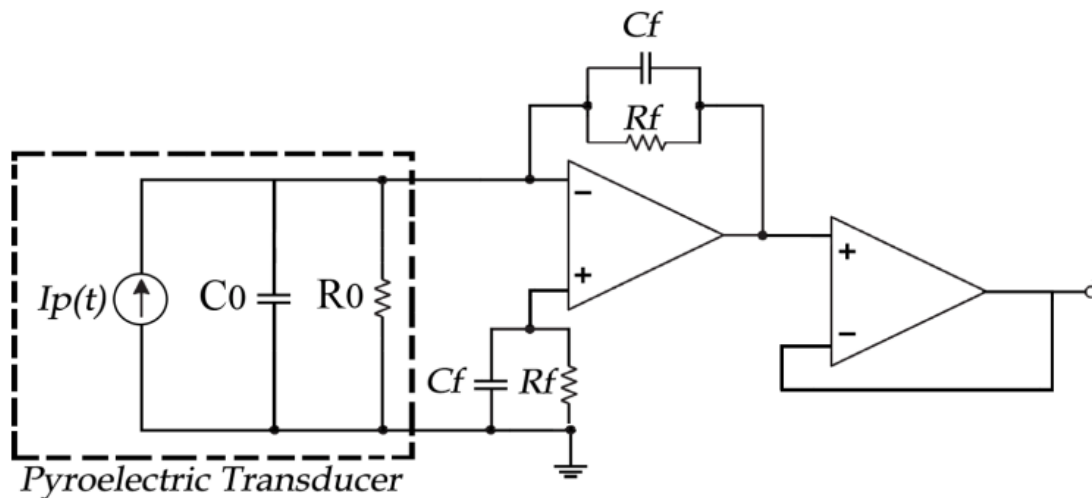
Figure 4.5: Schematic diagram of the implemented circuit, composed of a charge amplifier, which detects charge variations above PVDF surfaces followed by a buffer used to separate the stages. [25]

This system is the core means of transferring the signal to a readable form. This circuit is the charge amplifier. The first stage is that of the basic charge amplifier designed in the previous chapters. The first measurements that needed to be made was how the charge amplifier preformed so that the ASIC design could try to meet the same specifications. Figure 4.5 shows the results of the preamplifier with an average biological signal. The signal was to mimic temperature change in biological samples. This means that the signal is very slow with a time constant of 5ms. The resulting charge on average with the discrete setup was on the order of 9V.

The resulting charge can be calculated to be 9nC which is a large amount of charge. For the purpose of this design the peak value is only used to set a regression for the actual temperature. Therefore this knowledge can be used in the material presented in chapter 3 to test the final design against two other works. The comparison will be analyzed in section 4.3.
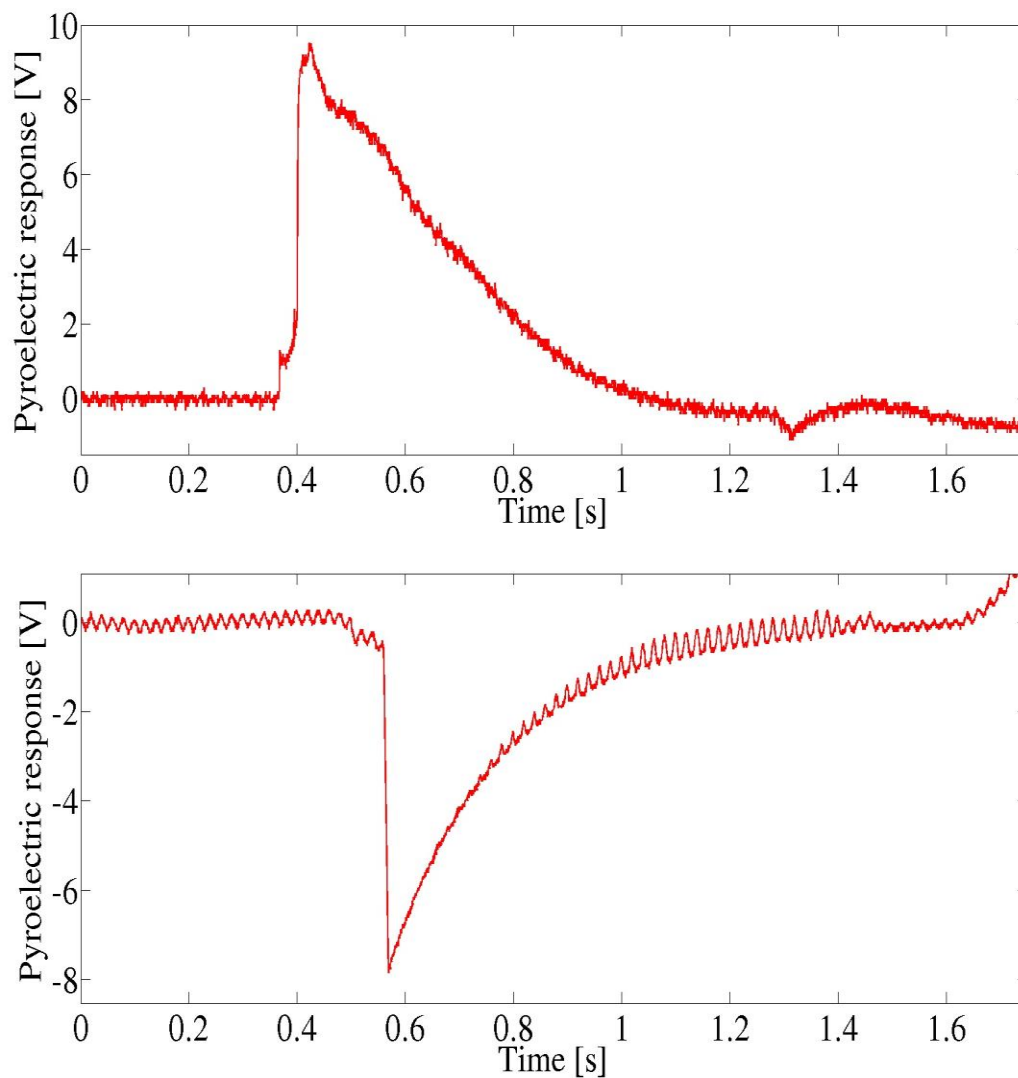
Figure 4.6: Response of discrete charge amplifier with 25° C temperature change. [25]

4.3 ASIC Laboratory Results

As was done with the previous design the first measurement taken into account was that of how the amplifier, or in this case the current mirror, would be affected by different signal inputs. Both the previous designs implemented an off-chip capacitance, due to the goals of this design the internal capacitance was again only 20pf. The design was highlighted in chapter 3.

The preamplifier measurements that needed to be made were how rise time, gain, and noise were affected by preamplifier bias current. This is important because all of these parameters are dependent on the value of the bias current for the input MOSFET. Figure 4.8 shows the results of the preamplifier rise time with changes in bias current. As the current is increased the output of the charge amplifier also increases.As the preamplifier bias current is increased, the rise time remains fairly constant at 2.6µs. This result is expected because the input MOSFET changes from weak inversion to strong inversion saturation operation. Also, the input charge polarities were changed between the positive and the negative input that show there is not much change in the rise time with either input polarity. It is also expected that as the gain is decreased, the rise time should increase because the gain bandwidth product (GBP) should remain constant.

The rise time of the preamplifier shown in Figure 4.1 was expected to be approximately 75µs according to simulation results. The measured results show that at -1µA bias current the rise time is approximately 100µs. The slower rise times are most likely caused by scope loading and/or circuit board capacitance.

The rise time was calculated by the 90-10% rule. The figure below shows the results highlighting the different rise time from different chips. The signal across multiple chips shows the variation in manufacturing processes. This test was done on two different charge amplifiers with a 100µs signal at 2Vpp equivalent to about 100nC from the test highlighted above. The amplifier was biased using -1µA bias current.
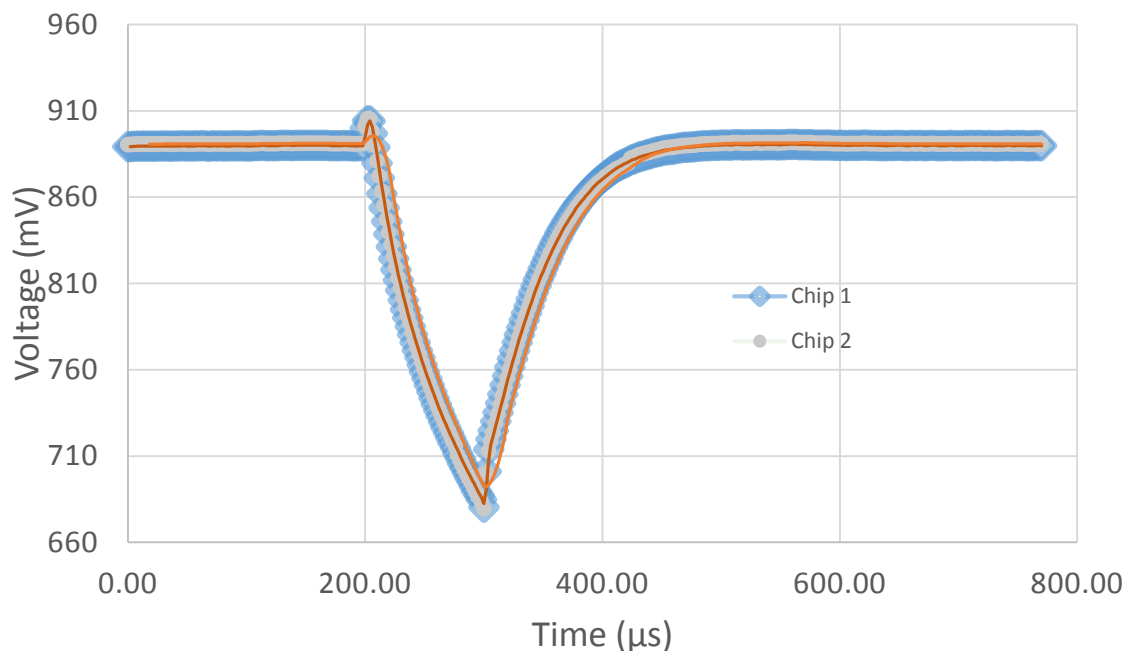

Figure 4.7: Response of chip 1 and chip 2 with 100nC charge on the input

From the chart above, two different chips are taking the signal and providing a voltage on the output with a magnitude of about 100mV across a time range of about 100μs. This circuit is of the same shape as the response of the target circuits..

The final test of this charge amplifier was to try and meet the original specification presented above. The signal is a 0.1ms wide pulse with variations of rise time that depend on the temperature variation with the average peak current output of100nA. Through testing of biological sample in work [25] the signal that is the input to the proposed charge amplifier is 9nC. The charge represents the temperature variation of a biological sample from 0 to 25 degrees Celsius. The test signal in the figure below is 0.1ms wide with the equivalent peak voltage to set the charge to 9nC at the input. The following test results represent the signal dynamic range from 2nC to 200nC. Simulating the different values of charge a PVDF transducer would produce give a temperature change of 0 to 25 degrees Celsius.
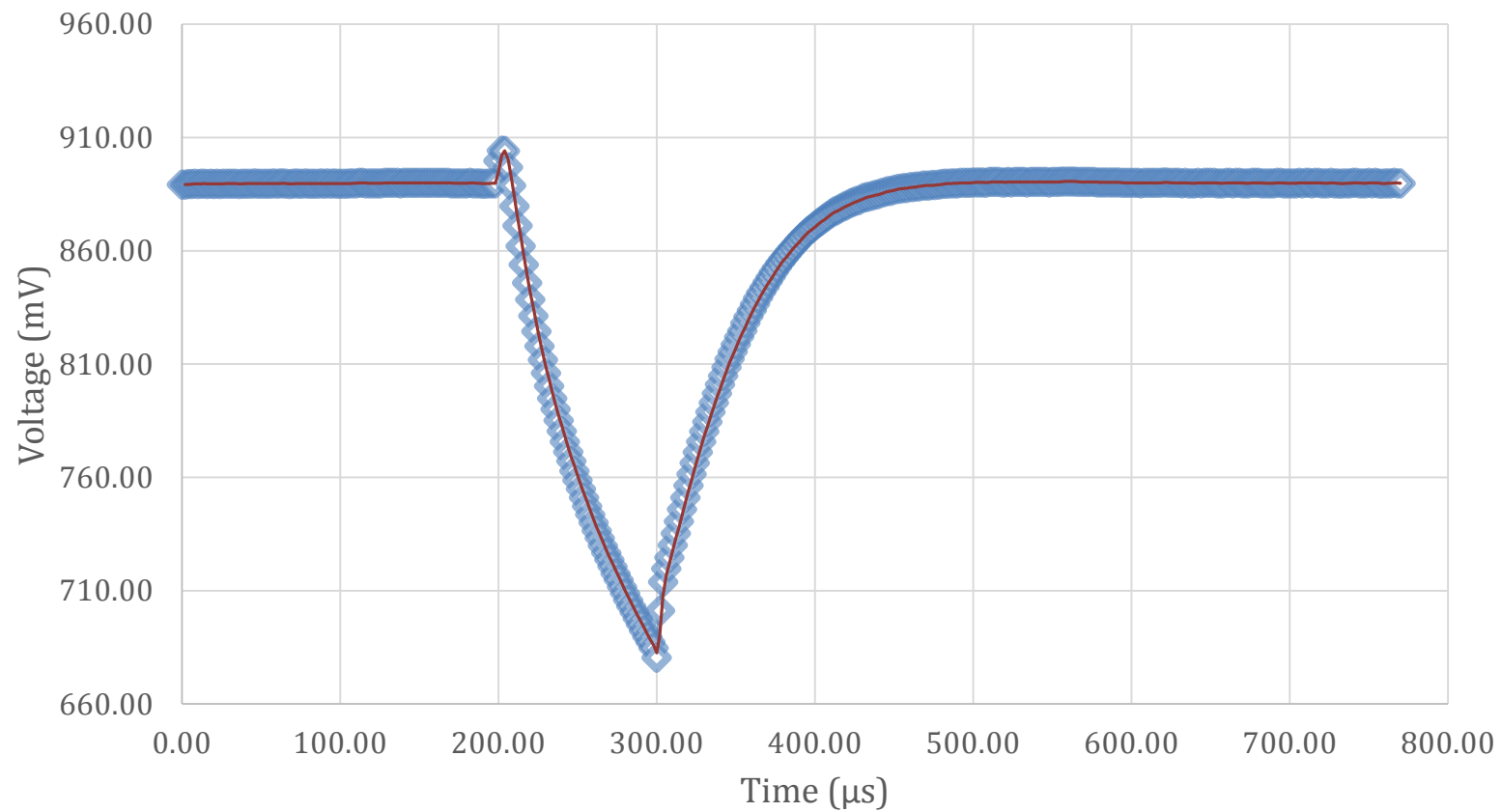
Figure 4.8: Response of circuit with 100nC charge on the input. Line is the average value of the closest two data points, this provides a line to model the signal with.
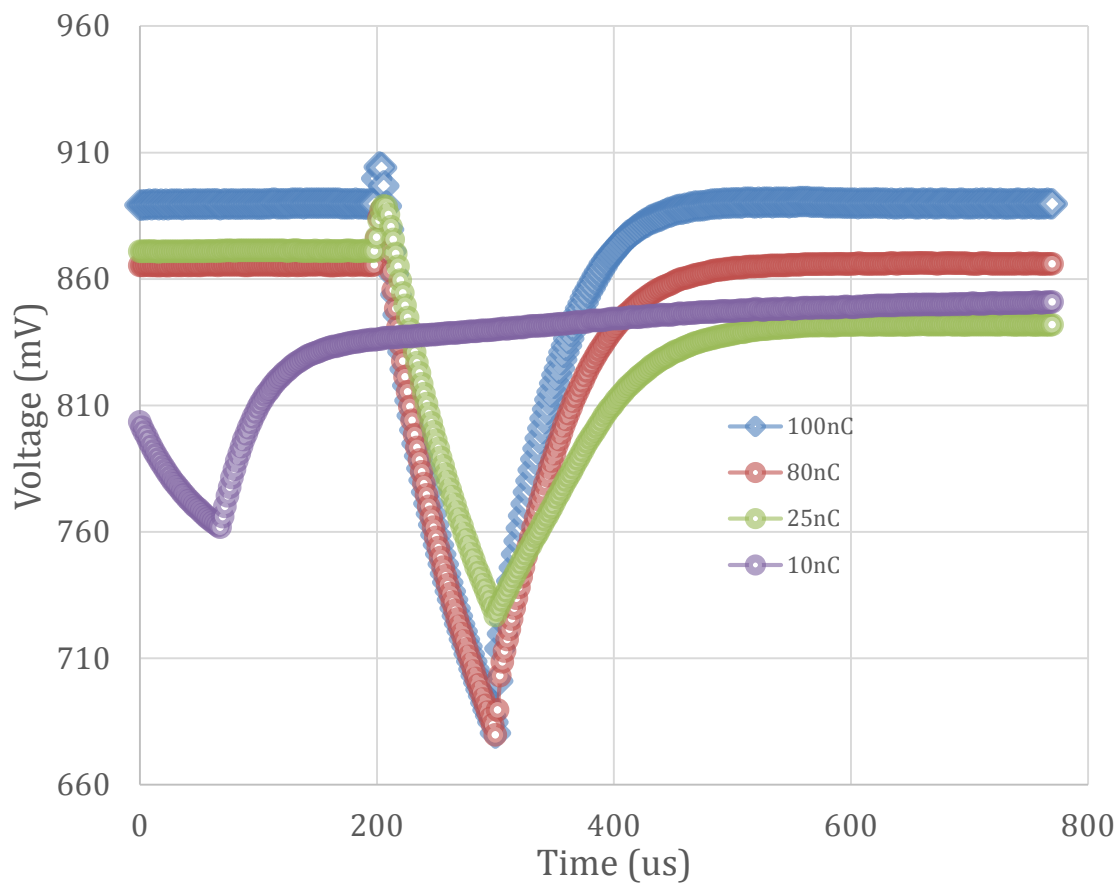
Figure 4.9: Response of circuit measuring the dynamic range of the transducer 10nC to 100nC

From the graph above it can be seen that the circuit is able to handle signals down to 10nC but it becomes unstable. The upper end of the range is 100nC but the circuit is able to perform with larger charges as the figure below demonstrates. The figure below shows the results of the circuit at 10nC and 2nC.
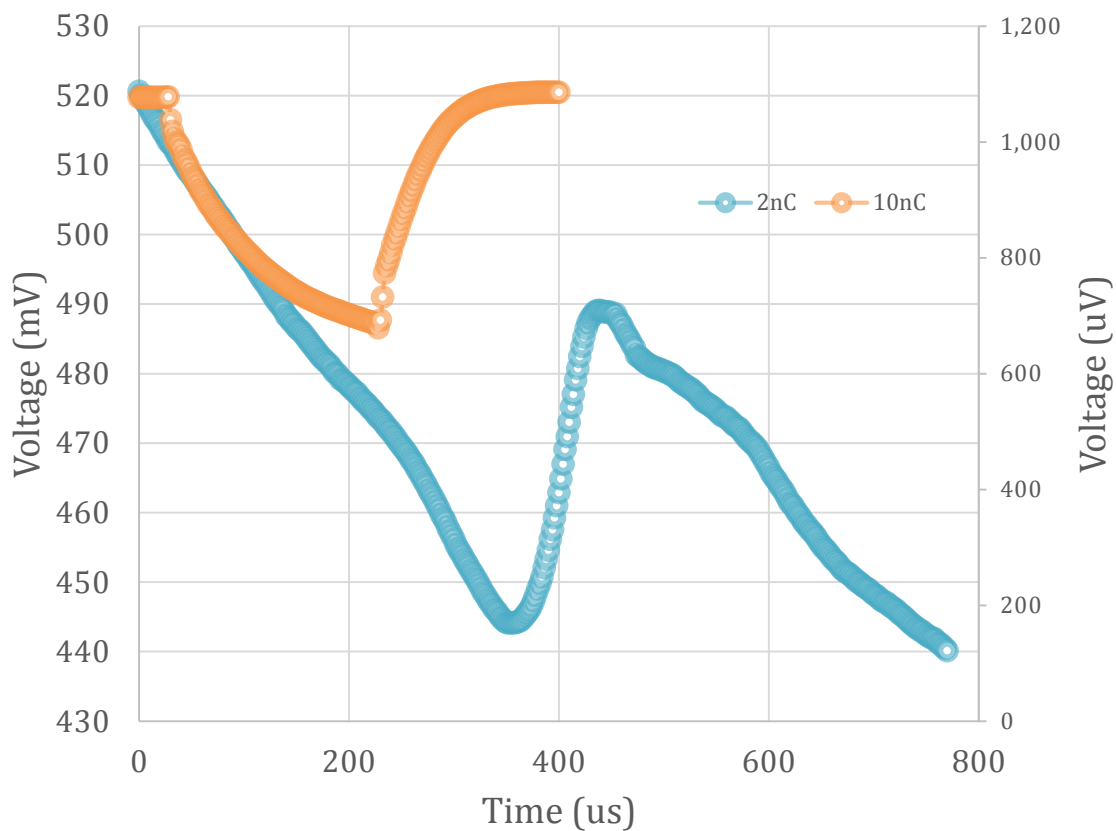
Figure 4.10: Response of small charge signals between 10nC and 2nC unstable response occurs. .

In testing the dynamic range for the signals. It was found that the signal becomes unstable at low incident charge. The experimental design was tested for 2nC of charge and the signal was not stable enough to get clear results. Even though the lower end of the dynamic range could not be meet the test of charges over the expected 100nC gave decent results. This means that design needs to be reexamined for the lower end of the dynamic range spectrum. The response in the graph below is for a larger charge than expected.
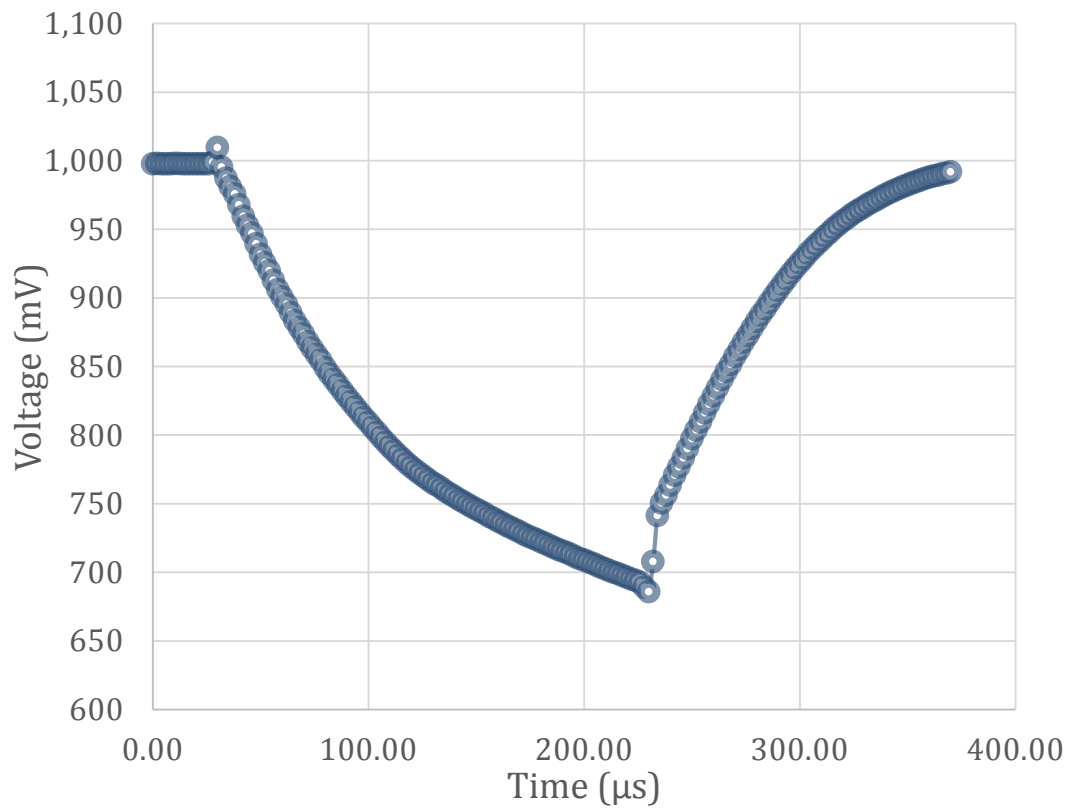
Figure 4.11: Response of larger charge signal than designed for,200nC pulse.

This design was tested with the constraints of the transducer. The overall comparison is summed in the table below.

Table 7: Comparison between the Different Designs and Simulation

	This work	This work Simulation	[4]	[44]
Process	180nm	-	0.35µm	Discrete
Power Consumption (µW)	1.8µW	165µW	0.84µW	1mW
Max Input Signal	8µA	10µA	--	1A
Rise Time	2.6µs	1.5µs	260ns	--
Chip area	.03301mm^2	--	10mm^2	--
Capacitor Size	20pF	20pF	0.2pF	1nF

Chapter 5

Conclusions and Recommendations

5.1 Conclusion

In the future bioelectronics will be used to manage the health of human population. Circuits such as the one described in this thesis will have to be implemented, in order to maintain a balance between performance and size. The ultimate direction is to move into implantable circuits with the power supply derived from body heat. In order to reach the goal of implantable devices finer CMOS processes must be utilized. Novel approaches to avoid using larger circuits will drive the production of such circuits.

Front-end signal acquisition is the most important stage in signal analysis, because it is the interface with the real world. This main purpose of this work is to convert input charge from a ferroelectric transducer into a voltage output signal. In order to achieve high signal integrity, it is critical that the preamplifier does not introduce much noise into the signal and also dominate the noise of the system.

Special design considerations were made to ensure stability of the preamplifier and to maintain the low design profile mentioned in chapter 3. The active resistive feedback network used in this project is a revised approach to large effective resistors. The measurement results shown in Chapter 4 are very encouraging, especially for the breadboard testing setup. The testing prototype chip for charge detections had a few more problems due to the low voltage levels produced. However the preamplifier successfully performed as it was designed.

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Appendix
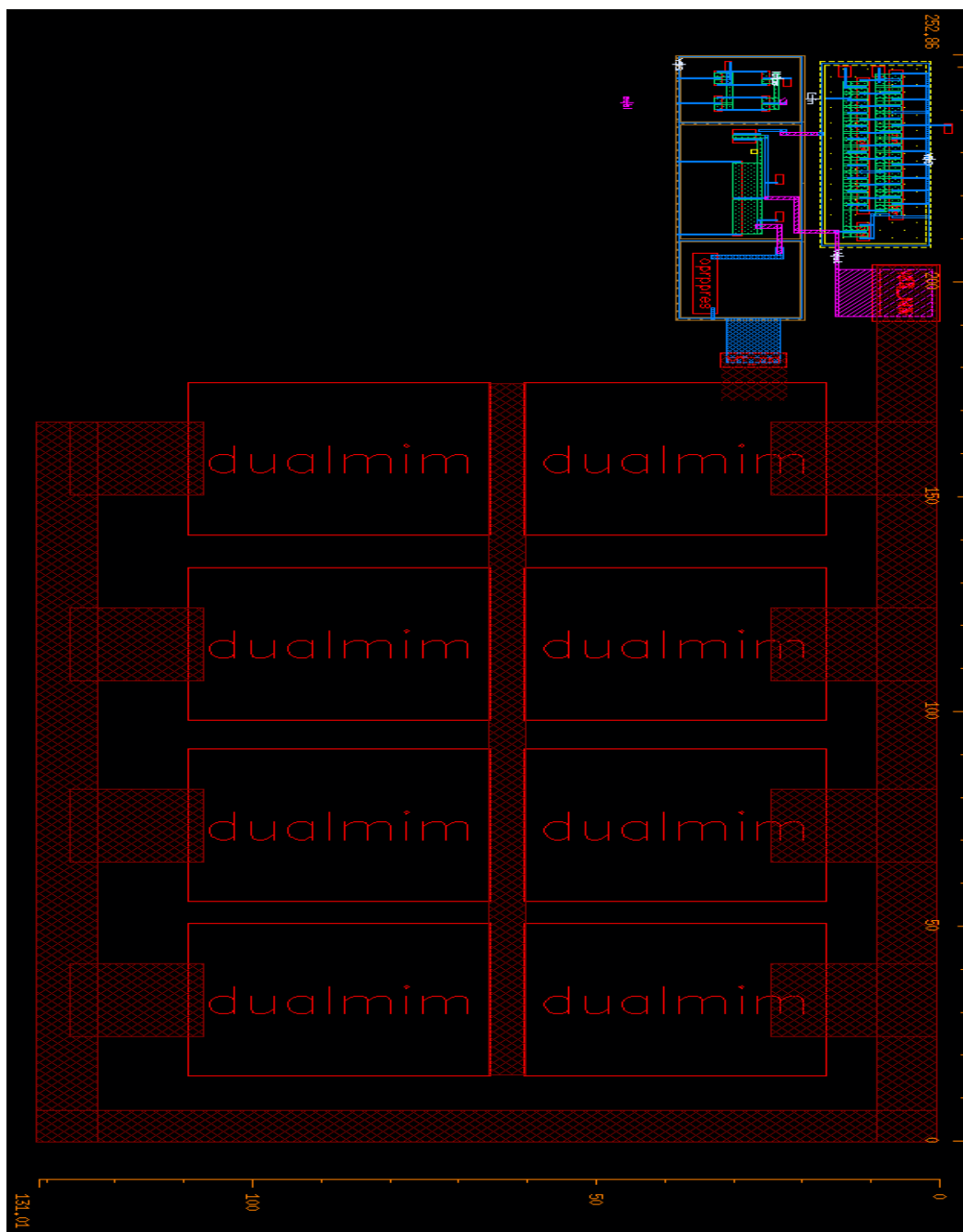
FigureA1: Chip size (131.01μm x 252 μm)

Vita

Logan Taylor was born in Nashville, Tennessee, to the parents of Mary and Chris Taylor. He is the oldest of three children: Mason and Juliana. He grew up in the north Nashville city of Goodlettsville. He attended Beech Elementary School until his third year, being rezoned for Madison Creek Elementary, following matriculation into T.W. Hunter Middle school in Hendersonville, TN. During his eighth year, he tested and was admitted to Pope John Paul II High School. During his time there he was very active in sports and academic clubs. Upon his graduation, and admission to the University of Tennessee, he was introduced to Engineering Fundamentals and quickly found a passion for electronics and computer aided design (CAD). During his sophomore year, Logan, was given the opportunity to learn from professionals, at Denso Manufacturing Tennessee, in a 15 month long internship. Not wanting his studies to fall by the wayside, he enrolled in night classes each semester of his internship. After receiving excellent instruction in manufacturing Logan thought to explore electrical engineering with a focus on power, at TVA where he work through his junior year as an intern in their Knoxville headquarters. Wanting to expand his horizons, he enrolled in a study abroad in Barcelona Spain to experience Spanish culture and language. As his senior design project, Logan worked on a SMART HOME device for the University of Tennessee CURENT conglomerate. His teams work on this project allowed him to accept a summer internship in Texas working for L-3 Communications, expanding on the skills he acquired during the project. His performance in the classroom allowed him to graduate in the Spring of 2013, and enroll in the 1 year Master of Science in Electrical Engineering. With admission into this program he was also awarded a graduate assistantship with the Fundamental of Engineering Dept. Logan Graduated in December of 2014 and is currently looking to continue his education with a Master of Business Administration.